1.5MHz, 1.3A, High-Efficiency Synchronous-Rectified Buck Converter

General Description

The uP1722 is a high efficiency synchronous-rectified buck converter with internal power switches. Fixed 1.5MHz PWM operation allows possible smallest output ripple and external component size. With high conversion efficiency and small package, the uP1722 is ideally suitable for portable devices and USB/PCIE-based interface cards where PCB area is especially concerned.

With internal low $R_{DS(ON)}$ switches, the uP1722 is capable of delivering 1.3A peak output current over a wide input voltage range from 2.6V to 5.5V. The output voltage is adjustable from 0.6V/0.5V (uP1722P/uP1722Q) to V_{IN} by a voltage divider. Other features include internal soft-start, chip enable, under-voltage, over-temperature and over-current protections. The uP1722 is available in space-saving WDFN2x2-6L, TSOT23-5L and SOT23-5L packages with fixed or adjustable output voltage options.

Ordering Information

Order Number	Package	TopMarking
uP1722PMT5-XX	TSOT23-5L	N45PXX
uP1722QMT5-XX		N45QXX
uP1722PMA5-XX	SOT23-5L	N45PXX
uP1722QMA5-XX		N45QXX
uP1722PDE6-00	WDFN2x2-6L	DF
XX: Output Voltage 00: adjustable 10: 1.0V; 12: 1.2V; 15: 1.5V; 18: 1.8V; 25: 2.5V; 33: 3.3V		
Status: In Production: uP1722PMA5-00, uP1722PMT5-00 Others: Please check the sample/production availability with uPI representatives.		

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Features

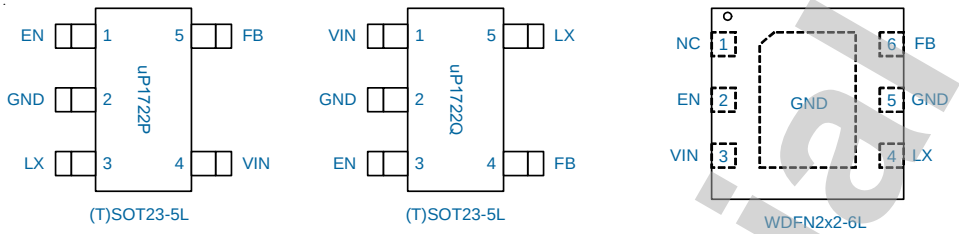
- 2.6V to 5.5V Input Voltage Range
- 1.3A Peak Output Current
- Accurate Reference with +/- 2% Accuracy
  - 0.6V (uP1722P)
  - 0.5V (uP1722Q)
- Up to 95% Conversion Efficiency
- Typical Quiescent Current: 60uA
- Integrated Low $R_{DS(ON)}$ Upper and Lower MOSFET Switches: 300mΩ and 250mΩ
- Current Mode PWM Operation
- Fixed Frequency: 1.5MHz
- 100% Maximum Duty Cycle for Lowest Dropout
- Internal Soft-Start
- Under-Voltage Protection
- Over-Temperature and Over-Current Protection
- Space-Saving WDFN2x2-6L, TSOT23-5L and SOT23-5L packages
- RoHS Compliant and Halogen Free

Applications

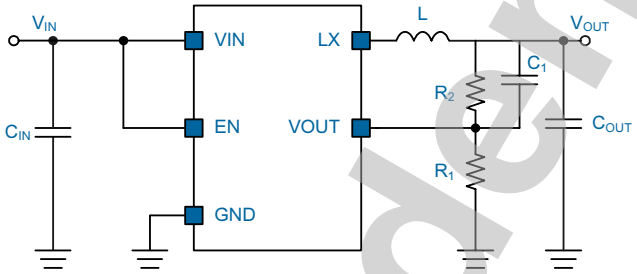
- Battery-Powered Portable Devices
  - MP3 Players
  - Digital Still Cameras
  - Wireless and DSL Modems
  - Personal Information Appliances
  - Cellular Telephones
- 802.11 WLAN Power Supplies
- FPGA/ASIC Power Supplies
- Dynamically Adjustable Power Supply for CDMA/WCSMA Power Amplifiers
- USB-Based xDSL Modems and Other Network Interface Cards

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Pin Configuration



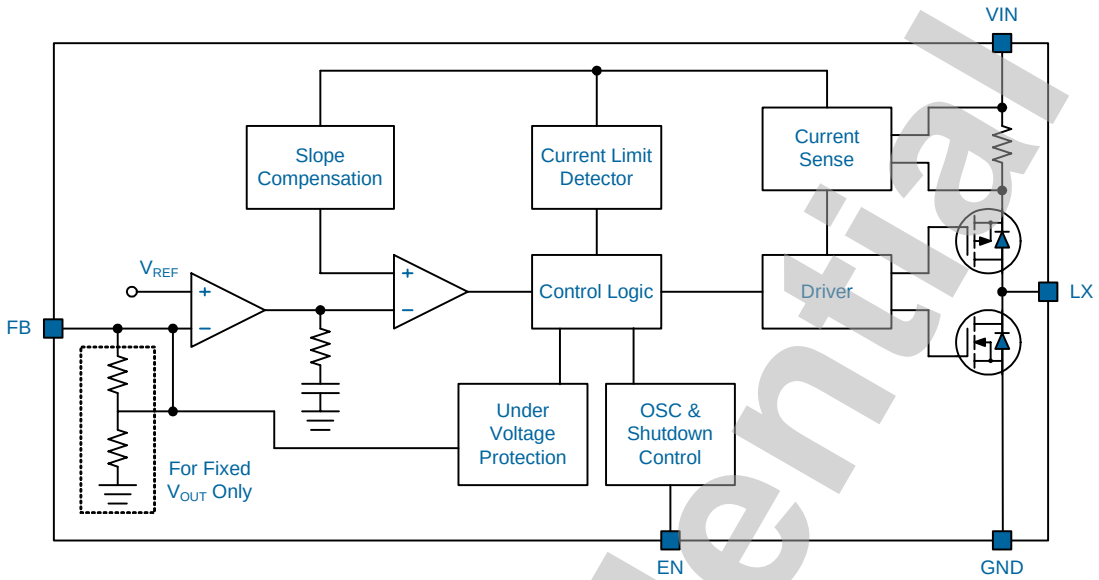
Typical Application Circuit



V_{IN}	V_{OUT}	C_{IN}	L	C_{OUT}	C1	R1	R2
3.3V	1V	4.7uF	2.2uH	10uF	180pF	10K	6.8K
3.3V	1.2V	4.7uF	2.2uH	10uF	120pF	10K	10K
3.3V	1.8V	4.7uF	2.2uH	10uF	47pF	10K	20K
5V	1V	4.7uF	2.2uH	10uF	180pF	10K	6.8K
5V	1.2V	4.7uF	2.2uH	10uF	120pF	10K	10K
5V	1.8V	4.7uF	2.2uH	10uF	47pF	10K	20K
5V	3.3V	4.7uF	2.2uH	10uF	27pF	15K	68K

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Functional Block Diagram



Functional Pin Description

Pin No.			Pin Name	Pin Function
PMT/PMA	QMT/QMA	PDE		
1	3	2	EN	**Chip Enable** (Active High). Logic low shuts down the converter.
2	2	5	GND	**Ground.** Tie the pin directly to the cathode terminal of C_{IN}, C_{OUT} and ground plane with the lowest impedance.
3	5	4	LX	**Internal Switches Output.** Connect this pin to the output inductor.
4	1	3	VIN	**Power Supply Input.** Input voltage that supplies current to the output voltage and powers the internal control circuit. Bypass input voltage with a minimum 4.7uF X5R or X7R ceramic capacitor.
5	4	6	FB	**Switcher Feedback Voltage.** This pin is the inverting input of the error amplifier. VOUT senses the switcher output through an external resistor divider network. For the fixed voltage version, connect this pin to the output voltage.
--	--	1	NC	**Not Internally Connected.**

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Functional Description

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Input Supply Voltage, V_{IN}

VIN pin provides power for the internal control circuit and supplies current to the output voltage. The supply voltage range is from 2.6V to 5.5V. A power on reset (POR) continuously monitors the input supply voltage. The POR level is typically 2.5V at V_{IN} rising.

The uP1722 draws pulsed current with sharp edges each time the upper switch turns on, resulting in voltage ripples and spikes at supply input. A minimum 1uF ceramic capacitor with shortest PCB trace is highly recommended for bypassing the supply input.

Chip Enable/Disable and Soft Start

Pulling EN pin lower than 0.4V shuts down the uP1722 and reduces its quiescent current lower than 1uA. In the shutdown mode, both upper and lower switches are turned off.

Pulling EN pin higher than 1.5V enables the uP1722 and initiates the soft start cycle. The uP1722 limits the in-rush current at start-up. This prevents unwanted shutdown otherwise may be triggered by voltage drop due to large inrush current.

PWM Operation

The uP1722 adopts slope-compensated, current mode PWM control capable of achieving 100% duty cycle. During normal operation, the uP1722 operates at PWM mode to regulate output voltage by transferring the power to the output voltage cycle by cycle at a constant 1.5MHz frequency. The uP1722 turns on the upper switch at each rising edge of the internal oscillator allowing the inductor current to ramp up linearly. The switch remains on until either the current-limit is tripped or the PWM comparator turns off the switch for regulating output voltage. The upper switch current is sensed, slope compensated and compared with the error amplifier output COMP to determine the adequate duty cycle. The FB pin senses output feedback voltage from an external resistive divider.

When the load current increases, it causes a slight decrease in the feedback voltage relative to the 0.6V/0.5V reference, which in turn causes the error amplifier output voltage to increase until the average inductor current matches the new load current.

Low Dropout Mode

The uP1722 increases duty cycle to maintain output voltage within its regulation as the supply input drops gradually in the battery-powered applications. The uP1722 operates with 100% duty cycle and enters low dropout mode as the supply input approaches the output voltage. This maximizes the battery life.

Current Limit Function

The uP1722 continuously monitors the inductor current for current limit by sensing the voltage drop across the upper switch when it turns on. When the inductor current is higher than current limit threshold (1.5A typical), the current limit function activates and forces the upper switch turning off to limit inductor current cycle by cycle. If the load continuously demands more current than what the uP1722 could provide, the uP1722 can not regulate the output voltage. Eventually under voltage protection will be triggered and shuts down the uP1722 if V_{FB} is too low.

Under Voltage Protection

Undervoltage Protection is triggered if the output voltage is lower than 17% of its target level and shuts down uP1722. The uP1722 can only be reset by POR of V_{IN} or toggling the EN pin.

Output Voltage Setting and Feedback Network

The output voltage can be set from V_{REF} to V_{IN} by a voltage divider as:

$$V_{OUT} = \frac{R1+R2}{R1} \times V_{REF}$$

The internal V_{REF} is 0.6V/0.5 with 2.0% accuracy. In real applications, a 22pF feedforward ceramic capacitor is recommended in parallel with R2 for better transient response. The feedforward is internally implemented for the fixed voltage versions.

Preliminary

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, V_{IN} ---------- -0.3V to +6V

LX Pin Voltage

DC ---------- -0.3V to +(V_{IN} +0.3V)

< 30ns ---------- -3.5V to +7V

Other Pins ---------- -0.3V to +6V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature (Soldering, 10 sec) ---------- 260°C

ESD Rating (Note 2)

HBM (Human Body Mode) ---------- 2kV

MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

(T)SOT23-5L θ_{JA} ---------- 250°C/W

(T)SOT23-5L θ_{JC} ---------- 100°C/W

WDFN2x2-6L θ_{JA} ---------- 155°C/W

WDFN2x2-6L θ_{JC} ---------- 20°C/W

Power Dissipation, P_D @ T_A = 25°C

(T)SOT23-5L ---------- 0.4W

WDFN2x2-6L ---------- 0.6W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Supply Input Voltage, V_{IN} ---------- +2.6V to +5.5V

Electrical Characteristics

(V_{IN} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Current						
Input Under Voltage Lockout	V_{UVLO}	V_{IN} rising	2.6	--	--	V
		V_{IN} falling	--	--	2	
Quiescent Current	I_Q	V_{EN} = 3.3V, V_{FB} > V_{REF}, I_{OUT} = 0mA, (No switching)	--	60	100	uA
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	0.01	1	uA
Reference						
Soft-Start Time		Guaranteed by design	--	250	--	us
Reference Voltage	V_{REF}	uP1722P I_{OUT} = 10mA	0.588	0.6	0.612	V
		uP1722Q I_{OUT} = 10mA	0.490	0.5	0.510	
Output Voltage Line Regulation	ΔV_{OUT}	V_{IN} = 2.6V to 5.5V	--	0.04	0.4	%/V
Output Voltage Load Regulation	ΔV_{OUT}	I_{OUT} = 10mA to 1A	--	0.5	--	%

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Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Oscillator						
COMP to Current Sense Transconductance		Guaranteed by design	--	2	--	A/V
Switching Frequency Range	f_{OSC}		1.25	1.5	1.75	MHz
Maximum Duty Cycle	DC	V_{IN} = V_{OUT} ; V_{FB} = 0.45V	100	--	--	%
Power Switches						
$R_{DS(ON)}$ of Upper Switch	R_{P_FET}	V_{IN} = 3.3V, I_{LX} = 100mA	--	300	--	mΩ
$R_{DS(ON)}$ of Lower Switch	R_{N_FET}	V_{IN} = 3.3V, I_{LX} = -100mA	--	250	--	mΩ
Logic Input						
EN Logic Low Threshold	V_{IL}	V_{IN} = 2.6V to 5.5V, Shutdown	--	--	0.4	V
EN Logic High Threshold	V_{IH}	V_{IN} = 2.6V to 5.5V, Enable	1.5	--	--	V
Protection						
FB Under Voltage Protection	ΔFB_UVP	FB Falling	--	0.133	--	V
Over Current Protection	I_{OUT_OCP}		1.3	1.5	--	A
Thermal Shutdwon Temperature	T_{SHDN}	Guaranteed by design	--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SHDN}	Guaranteed by design	--	20	--	°C

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

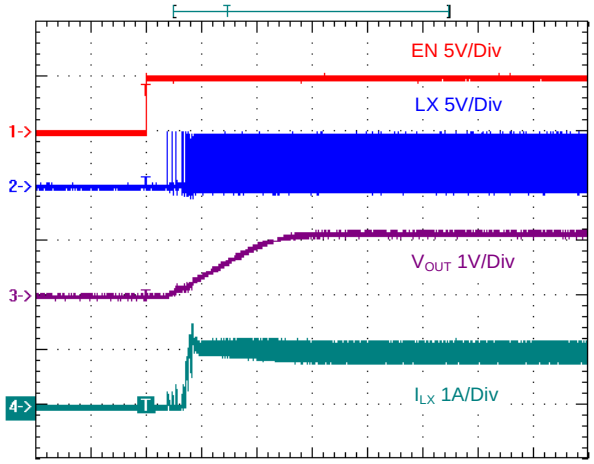
Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

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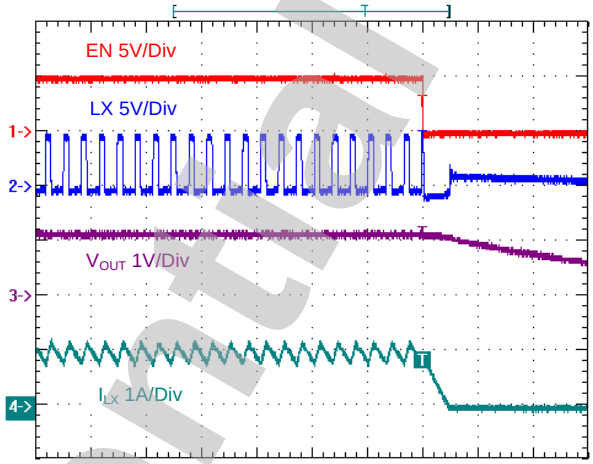
Typical Operation Characteristics

Power On from EN



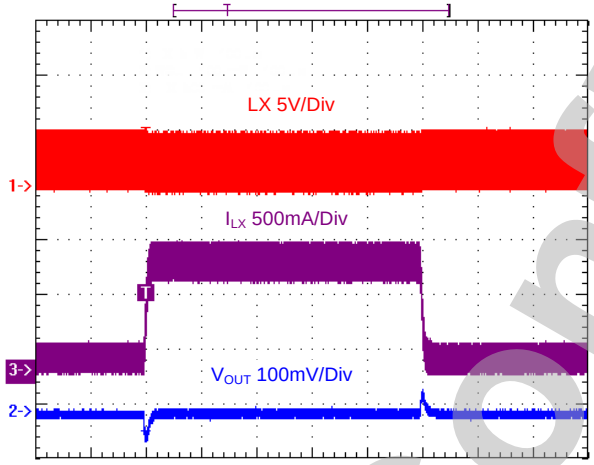
Time (100us/Div)
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 1A

Power Off from EN



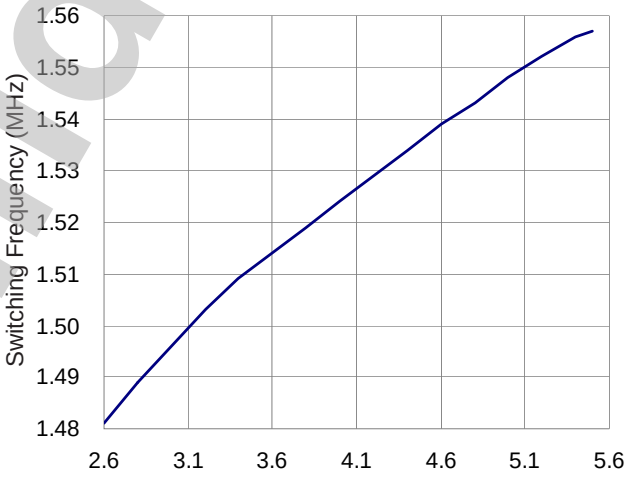
Time (2us/Div)
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 1A

Load Transient



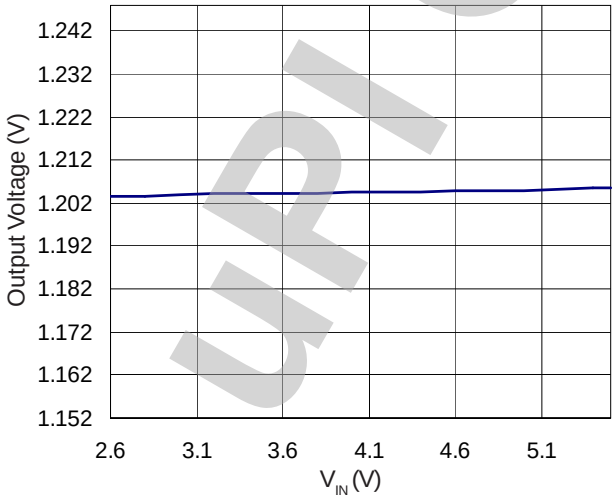
Time (100us/Div)
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A ~ 1A

Switching Frequency vs. Input Voltage

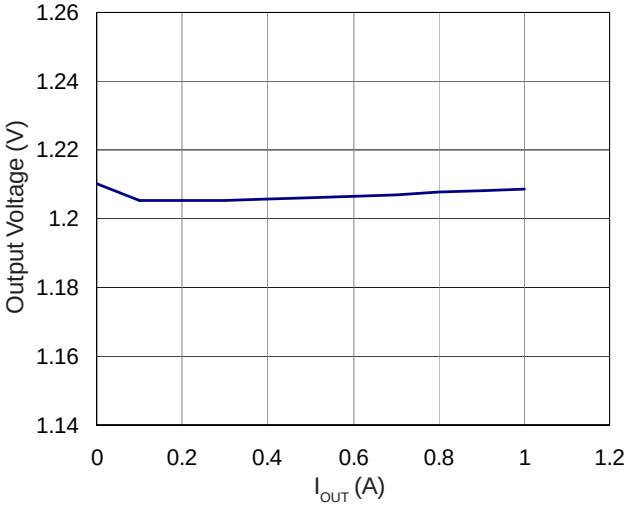


I_{OUT} = 500mA

Line Regulation

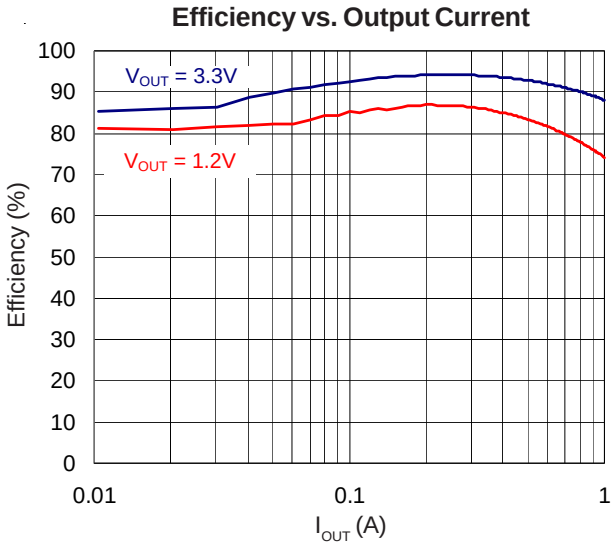


Load Regulation



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Typical Operation Characteristics



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Application Information

Output Inductor Selection

Output inductor selection is usually based on the considerations of inductance, rated current value, size requirements and DC resistance (DCR).

The inductance is chosen based on the desired ripple current. Large value inductors result in lower ripple currents and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in the equation below. A reasonable starting point for setting ripple current is ΔI_L = 390mA (30% of 1.3A). For most applications, the value of the inductor will fall in the range of 1uH to 10uH.

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} \times V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40°C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current. If possible, choose an inductor with rated current higher than 1.0A so that it will not saturate even under current limit condition.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends on the price vs. size requirements and any radiated field/EMI requirements.

Input Capacitor Selection

The uP1722 draws pulsed current with sharp edges from the input capacitor resulting in ripple and noise at the input supply voltage. A minimum 4.7uF X5R or X7R ceramic capacitor is highly recommended to filter the pulsed current. The input capacitor should be placed as near the device as possible to avoid the stray inductance along the connection trace. Y5V dielectrics, aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

The capacitor with low ESR (equivalent series resistance) provides the small drop voltage to stabilize the input voltage during the transient loading. For input capacitor selection, the ceramic capacitors larger than 4.7uF is recommend. The capacitor must conform to the RMS current requirement. The maximum RMS ripple current is calculated as:

$$I_{IN(RMS)} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2xV_{OUT}$, where $I_{IN(RMS)} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

Output Capacitor Selection

The uP1722 is specifically design to operate with minimum 4.7uF X5R or X7R ceramic capacitor. The value can be increased to improve load/line transient performance. Y5V dielectrics, aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

The ESR of the output capacitor determines the output ripple voltage and the initial voltage drop following a high slew rate load transient edge. The output ripple voltage can be calculated as:

$$\Delta V_{OUT} = \Delta I_C \times (ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}})$$

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where f_{OSC} = operating frequency, C_{OUT} = output capacitance and $\Delta I_C = \Delta I_L$ = ripple current in the inductor.

The ceramic capacitor with low ESR value provides the low output ripple and low size profile. Connect a 4.7uF ceramic capacitor at output terminal for good performance and place the input and output capacitors as close as possible to the device.

Using Ceramic Capacitors

Higher value, lower cost ceramic capacitors are now available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the uP1722 control loop does not depend on the output capacitor's ESR

for stable operation, ceramic capacitors can be used to achieve very low output ripple and small circuit size.

However, care must be taken when these capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN}, large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Thermal Considerations

In most applications, the uP1722 does not dissipate much heat due to its high efficiency. However, overtemperature protection is implemented in case of applications where the uP1722 is operating at high ambient temperature. If the junction temperature reaches approximately 150°C, the OTP turns both power switches and let the LX node become high impedance. The uP1722 restores to normal operation if the junction temperature drops to 130°C.

It is helpful to analysis the power dissipation of uP1722 for avoiding the uP1722 from exceeding the maximum junction temperature. In typical applications, the conduction loss dominates the total power loss in uP1722. The conduction loss has its maximum at high duty-ratio, low input voltage, and high ambient temperatures.

Consider the uP1722 in dropout mode operation at an input voltage of 2.6V, a load current of 400mA and an ambient temperature of 75°C. The on-resistance of the upper switch is about 500mΩ at this condition. Therefore the power dissipation P_D is:

$$PD = I_{OUT}^2 \times R_{DS(ON)} = 80mW$$

This results in 250 x 0.08 = 20°C temperature raise at junction. The juction temperature is 95°C and is lower than its maximum rating 125°C.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to (ΔI_{OUT} x ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{OUT} also begins to discharge or charge C_{OUT}, which generates a feedback error signal. The regulator loop then acts to return V_{OUT} to its steady state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

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PCB Layout Considerations

High switching frequencies and relatively large peak currents make the PCB layout a very important part of switching mode power supply design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Follow the PCB layout guidelines for optimal performance of uP1722.

1 For the main current paths, keep their traces short, direct and wide.

2 Put the input/output capacitors as close as possible to the device pins.

3 LX node is with high frequency voltage swing and should be kept in small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.

4 Connect feedback network behind the output capacitors. Place the feedback components near the uP1722 and keep the loop area small. .

5 A ground plane is preferred, but if not available, keep the signal and power grounds sepregated with small signal components returning to the GND pin at one point. They should not share the high current path of C_{IN} or C_{OUT}.

6 Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to V_{IN} or GND.

Examples of 2-layer PCB layout are shown in Figure1, 2 and 3 for different part number, respectively.

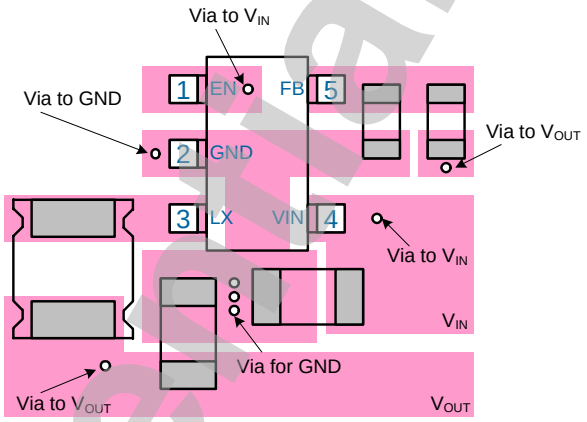


Figure 1. Top Layer Layout Example for uP1722PMT5 and uP1722PMA5

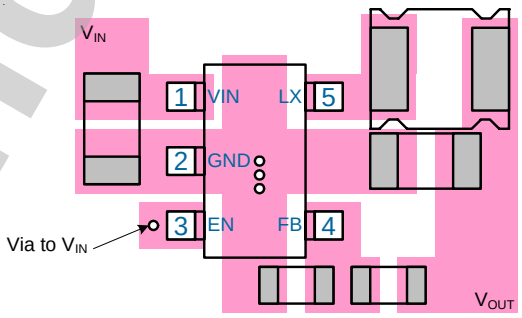


Figure 2. Top Layer Layout Example for uP1722QMT5 and uP1722QMA5

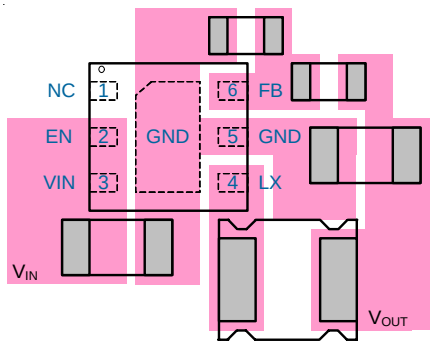
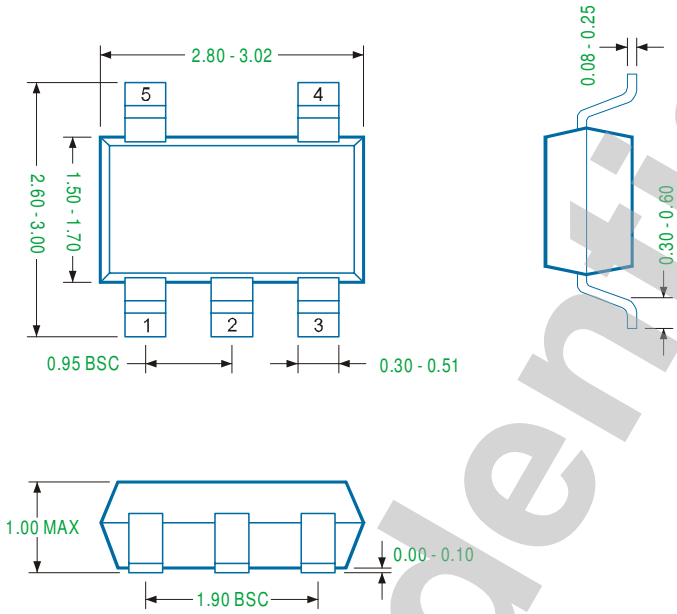


Figure 3. Top Layer Layout Example for uP1722PDE6

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Package Information

TSOT23-5L Package



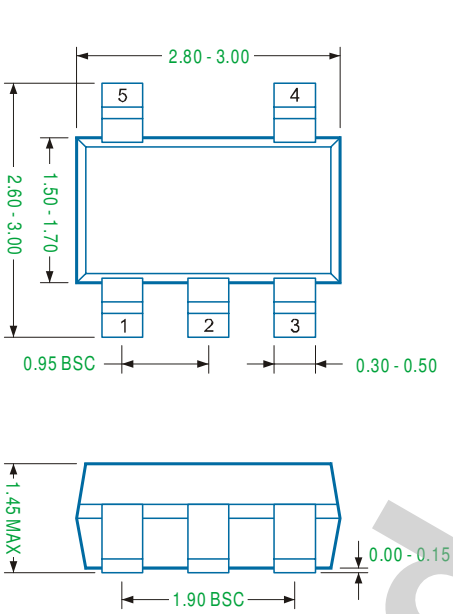
Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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Package Information

SOT23-5L Package



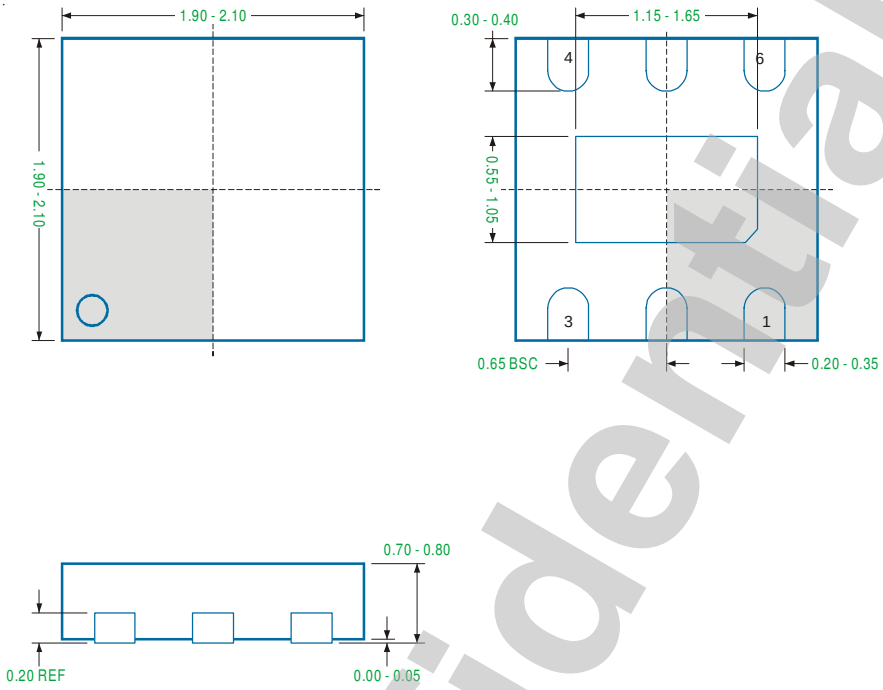
Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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Package Information

WDFN2x2-6L Package



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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