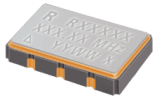
RXO5032P

SMD Clock Oscillator (Preliminary)

High Performance XO in 5 x 3.2 mm Surface Mount package



Product description

The RXO5032P XO combines very low RMS phase jitter and tight frequency stability in a small 5 x 3.2 mm SMD package. Available in hundreds of industry standard frequencies from 8 MHz to 800 MHz for fast delivery and reduced inventory levels.

Applications

- Basestation
- Communications
- Consumer Products
- DSL/ADSL
- Ethernet
- WiFi
- WiMAX/WLAN

Features

- 0.5 ps integrated RMS phase jitter (12 kHz to 20 MHz)
- Fast sample turnaround available
- LVCMOS, LVPECL, or LVDS Output options
- Wide frequency range
- Low power differential outputs
- Small form factor

Specifications

1.0 SPECIFICATION REFERENCES

Line	Parameter	Description
1.1	Model Description	RXO5032P XO
1.2	RoHS Compliant	Yes
1.3	Reference Number	
1.4	Rakon Part Number	

2.0 FREQUENCY CHARACTERISTICS

Line	Parameter	Test Condition	Value	Unit
2.1	Frequency		8 to 1500	MHz
2.2	Operating Temperature Range		-40 to 85	°C
2.3	Frequency Stability	Including Temperature range, Supply variation, Load variation and 10 years aging at 25°C	±30 to 50	ppm
2.4	Temperature Stability	Temperature range only	±10 to 20	ppm

3.0 POWER SUPPLY

Line	Parameter	Test Condition	Value	Unit
3.1	Supply Voltage (VDD)	With a tolerance of ±10%	3.3	V
3.2	Supply Voltage (VDD)	With a tolerance of ±5%	2.5	V
3.3	Supply Current	For LVCMOS	30 max	mA
3.4	Supply Current	For LVPECL	65 max	mA
3.5	Supply Current	For LVDS	40 max	mA

Preliminary

4.0 OUTPUT CHARACTERISTICS - LVCMOS UP TO 200MHz ONLY

Line	Parameter	Test Condition	Value	Unit
4.1	Output Voltage (Vol)	15pF load	10 max	%VDD
4.2	Output Voltage (Voh)	15pF load	90 min	%VDD
4.3	Duty Cycle	@ 50% VDD	48 to 52	%
4.4	Rise Time / Fall Time	90%/10%	3 max	ns
4.5	RMS Phase Jitter	Integrated 12kHz to 20MHz	0.5	ps

5.0 OUTPUT CHARACTERISTIC - LVPECL ONLY

Line	Parameter	Test Condition	Value	Unit
5.1	Output Voltage (Vol)	50Ω nominal load. (VDD - 1.6V) max.		
5.2	Output Voltage (Voh)	50Ω nominal load. (VDD - 1.03V) min.		
5.3	Duty Cycle	@ VDD-1.3V (45 to 55% 600MHz+)	48 to 52	%
5.4	Rise Time / Fall Time	80%/20% at 50Ω output load	0.6 max	ns
5.5	RMS Phase Jitter	Typical integrated 12kHz to 20MHz	0.5	ps

6.0 OUTPUT CHARACTERISTICS - LVDS ONLY

Line	Parameter	Test Condition	Value	Unit
6.1	Differential Output: Voltage Swing (Vod)		350	mV
6.2	Duty Cycle	Measured at 1.25V (45 to 50% for 600MHz+)	48 to 52	%
6.3	Output Load	RL = 100 Ω / CL = 10 pF		
6.4	Rise Time / Fall Time	RL = 100 Ω / CL = 10 pF	0.6 max	ns
6.5	RMS Phase Jitter	Typical integrated 12kHz to 20MHz	0.5	ps

7.0 PIN CONNECTIONS

Line	Parameter	Description
7.1	Pin 1	E/D* or NC
7.2	Pin 2	E/D* or NC
7.3	Pin 3	GND
7.4	Pin 4	OUTPUT
7.5	Pin 5	COMPLIMENTARY OUTPUT (LVPECL/LVDS only), or E/D*, or NC
7.6	Pin 6	VDD
7.7	* Output Enabled	>70% of VDD on E/D pin, or E/D pin left open (connected to internal pull-up resistor)
7.8	* Output Disabled	<30% of VDD on E/D pin, or E/D pin to GND

8.0 PACKAGE DETAIL

Line	Parameter	Description
8.1	Package	F
8.2	Top line	[R ######] Part identifier
8.3	Middle line	[######] Part information
8.4	Bottom line	[o FYWW] Pin 1, Manufacturing code, Year code* and Week code**
8.5	* Year code	A = 2010, B = 2011, C = 2012, D = 2013, ... Z = 2035
8.6	** Week Code	WW = 01 = Week of first Monday of the year

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9.0 ENVIRONMENTAL SPECIFICATION

Line	Parameter	Description
9.1	Mechanical Shock	MIL-STD-883, Method 2002
9.2	Storage Temperature Range	-55 to 125 °C
9.3	Humidity	After 48 hours at 85 °C±2 °C 85 % relative humidity non-condensing
9.4	Thermal Shock	MIL-STD-883, Method 1011
9.5	Vibration	MIL-STD-883, Method 2007
9.6	Gross and Fine Leak	MIL-STD-883, Method 1014
9.7	RoHS Compliant	Yes

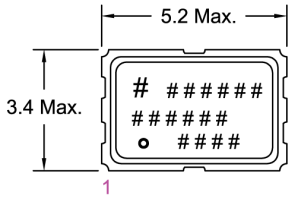
10.0 MANUFACTURING INFORMATION

Line	Parameter	Description
10.1	Packaging Description	Tape and Reel. Standard packing quantity is 2000 per reel
10.2	Reflow	Solder reflow process as per attached profile

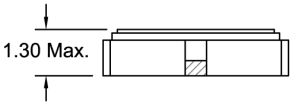
Preliminary

Drawing Name: XO/VCXO 5032 6-Pin Model Drawing

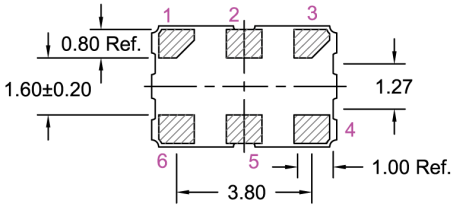
PACKAGE G65



TOP VIEW

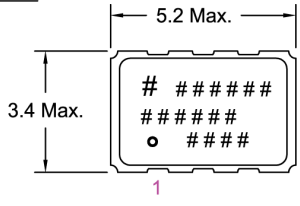


FRONT VIEW

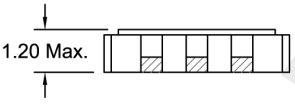


BOTTOM VIEW

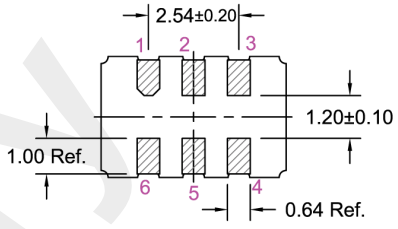
PACKAGE GV5



TOP VIEW

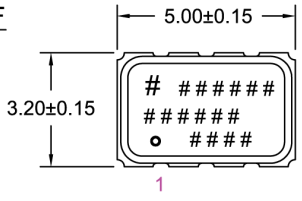


FRONT VIEW



BOTTOM VIEW

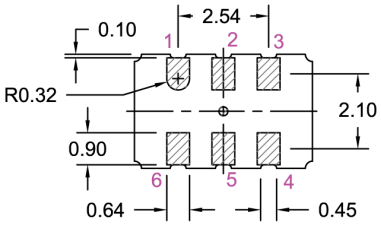
PACKAGE F



TOP VIEW



FRONT VIEW

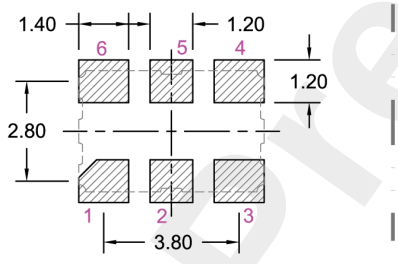


BOTTOM VIEW

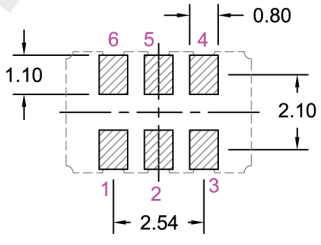
NOTE : 1. PIN CONNECTIONS ARE DETAILED IN THE SPECIFICATION.
2. MARKING INFORMATION IS DETAILED IN THE SPECIFICATION.

RECOMMENDED PAD LAYOUT - Top View

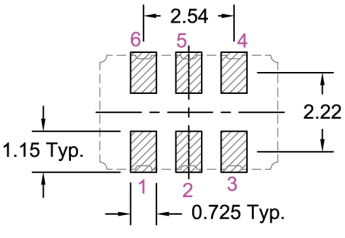
PACKAGE G65



PACKAGE GV5



PACKAGE F



TITLE: XO/VCXO 5032 6-PIN MODEL	FILENAME: CAT026	TOLERANCES:	
RELATED DRAWINGS:	REVISION: C	XX =	
	DATE: 01-May-12	X.X = ±0.15	
	SCALE: 5 : 1	X.XX = ±0.10	
	Millimetres	X.XXX =	
		X° =	
		Hole =	

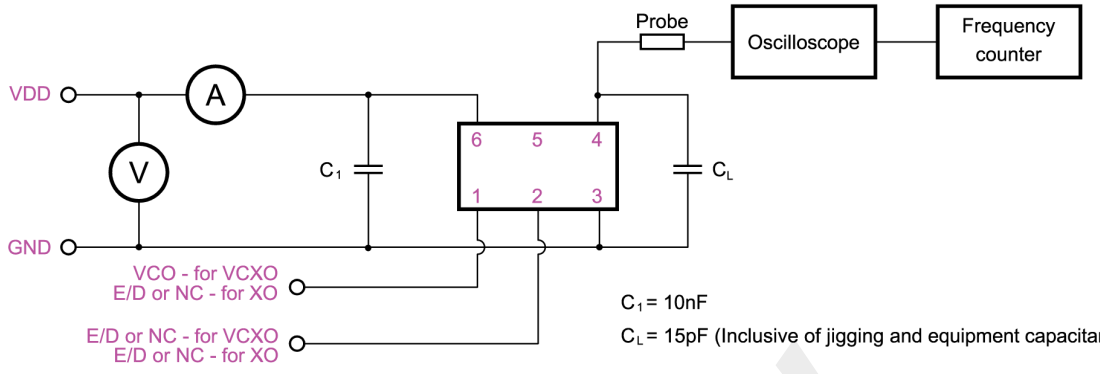
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Drawing Name: XO/VCXO 6 Pin Series Test Circuit

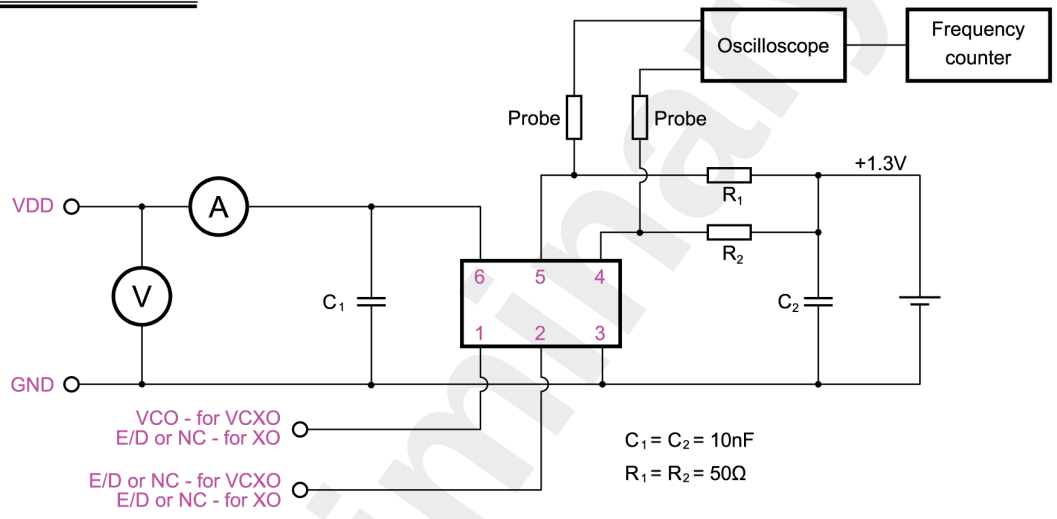
LVCMOS TEST CIRCUIT:



C_1 = 10nF

C_L = 15pF (Inclusive of jigging and equipment capacitance)

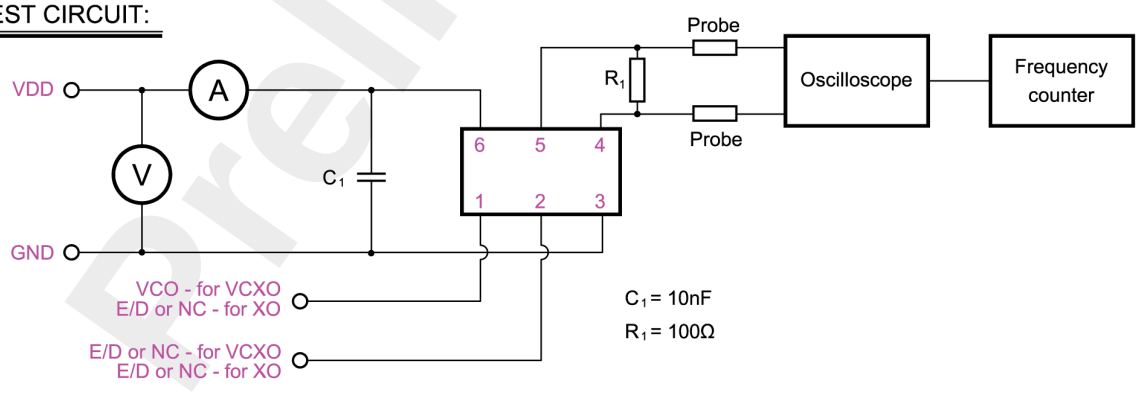
LVPECL TEST CIRCUIT:



$C_1 = C_2$ = 10nF

$R_1 = R_2$ = 50Ω

LVDS TEST CIRCUIT:



C_1 = 10nF

R_1 = 100Ω

Preliminary

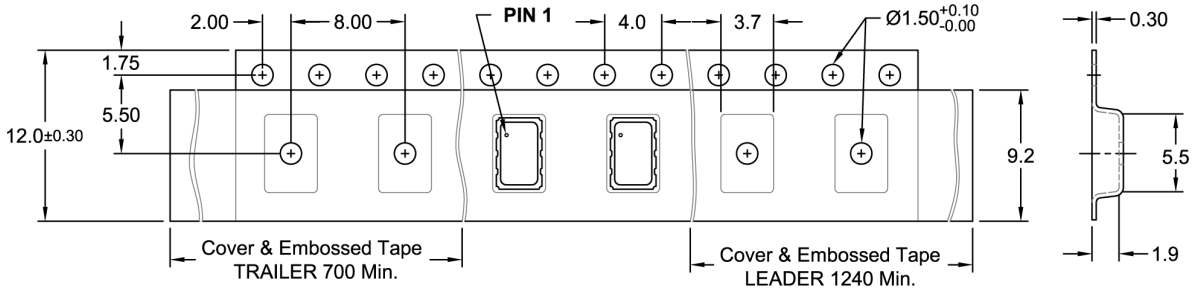
TITLE: XO/VCXO 6 PIN SERIES TEST CIRCUIT	FILENAME: CAT088
RELATED DRAWINGS:	REVISION: F
	DATE: 03-May-12
	SCALE: 1 : 1
	Millimetres

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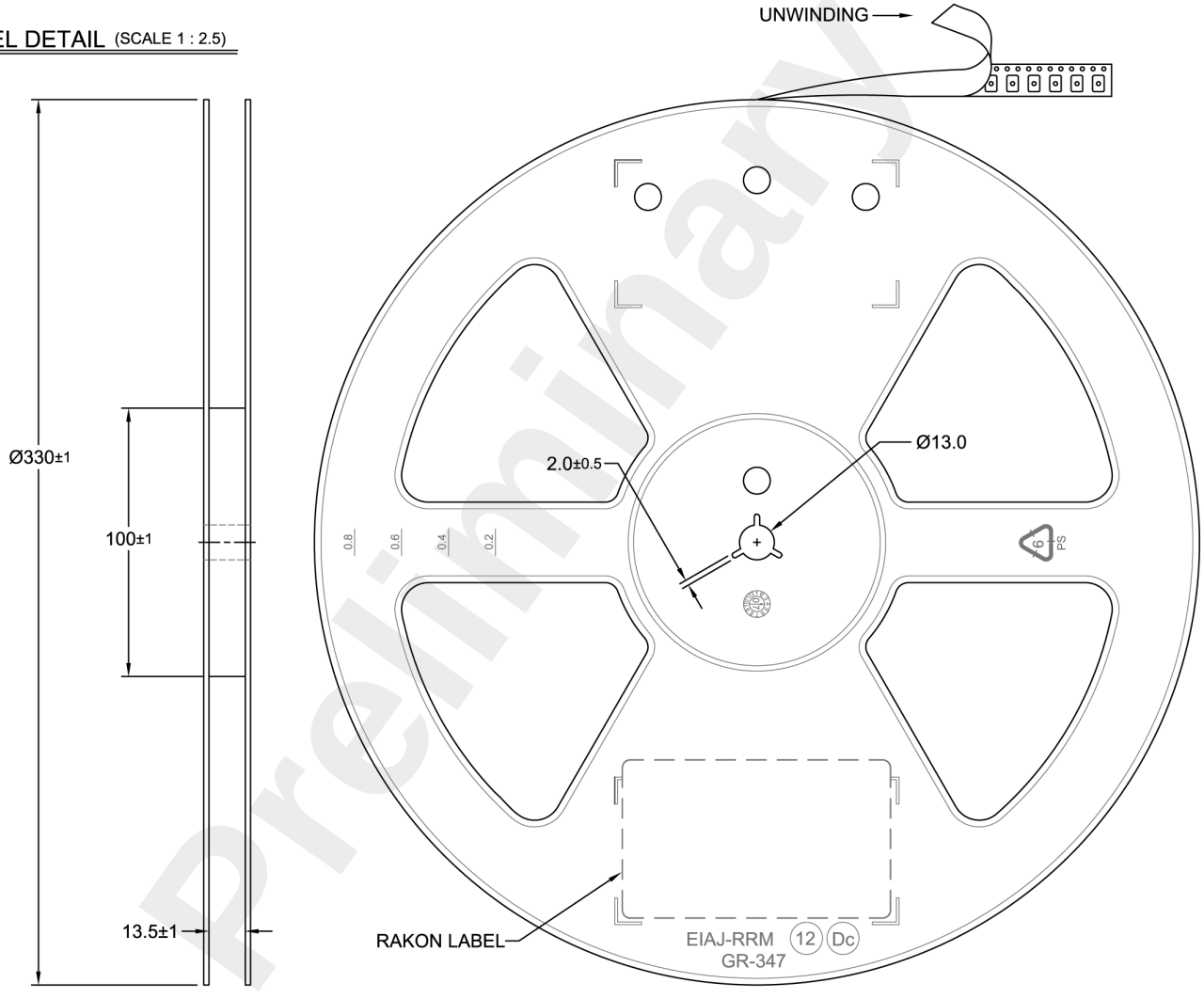
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Drawing Name: XO/VCXO5032 F Series Tape & Reel

TAPE DETAIL (SCALE 2 : 1)



REEL DETAIL (SCALE 1 : 2.5)



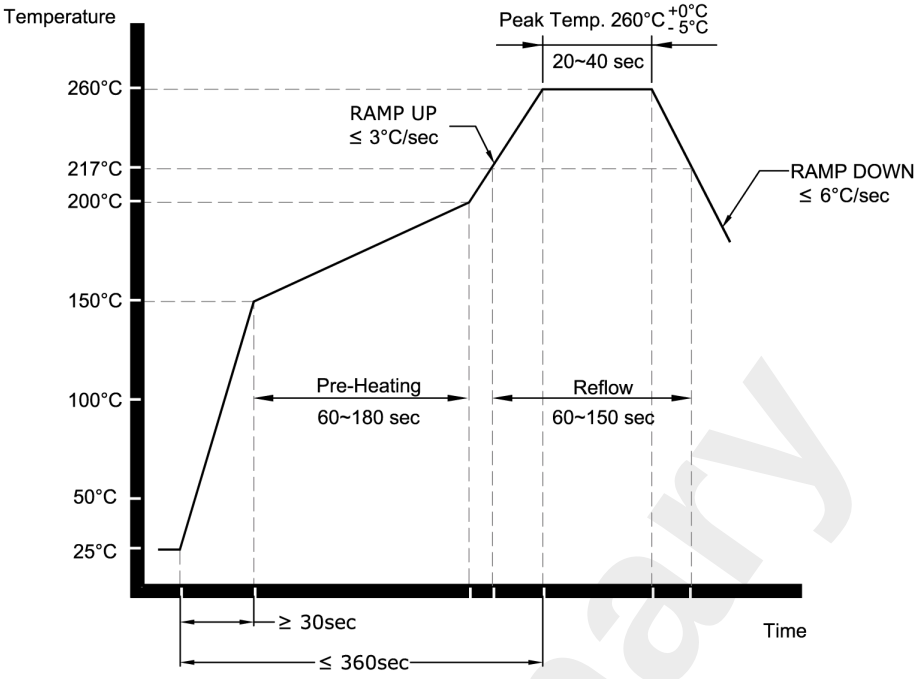
Preliminary

TITLE: XO / VCXO 5032 F SERIES TAPE & REEL	FILENAME: CAT029	TOLERANCES:
RELATED DRAWINGS:	REVISION: B	XX =
	DATE: 14-Oct-11	X.X = ±0.1
	SCALE: 2 : 1	X.XX = ±0.05
	Millimetres	X.XXX =
		X° =
		Hole =

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Drawing Name: Pb-Free Reflow



NOTE:
The product has been tested to withstand the Reflow Profile shown. The Reflow Profile used to solder Rakon products is determined by the solder paste Manufacturer's specification. It is recommended that the Reflow Profile used does not exceed the one shown above.

TITLE: Pb-FREE REFLOW	FILENAME: CAT541
RELATED DRAWINGS:	REVISION: B
	DATE: 05-Sep-11
	SCALE: NTS
	Millimetres

Preliminary

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