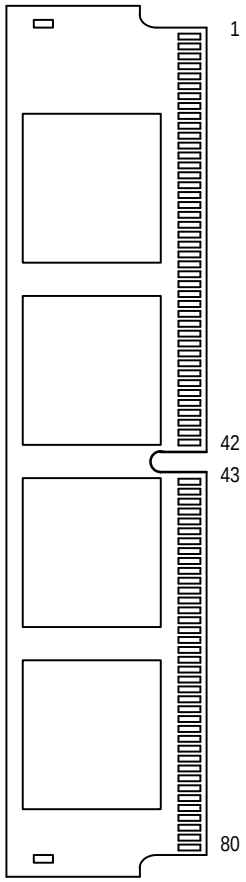
MCM72JG32
MCM72JG64

Advance Information

256K and 512K Pipelined BurstRAM™ Sedcondary Cache Module for Pentium™

160–LEAD CARD EDGE
CASE 1113A–01
TOP VIEW



The MCM72JG32 and MCM72JG64 are designed to provide a burstable, high performance, 256K/512K L2 cache for the Pentium microprocessor in conjunction with Intel's Triton chip set. The modules are configured as 32K x 64 and 64K x 64 bits in a 160 pin card edge memory module. Each module uses four of Motorola's 5 V 32K x 18 or 64K x 18 BurstRAMs and one Motorola 5 V 32K x 8 FSRAM for the tag RAM.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or cache address status ($\overline{CADS}$). Subsequent burst addresses are generated internal to the BurstRAM by the cache burst advance ($\overline{CADV}$) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (CLK0, CLK1) input. Eight write enables are provided for byte write control.

PD0 – PD4 map into the Triton chip set for auto–configuration of the cache control.

Module family pinout supports 5 V and 3.3 V components. It is recommended that all power supplies be connected.

These cache modules are plug and pin compatible with the MCM64AF32SG15, a 256K byte asynchronous module also designed for the Pentium microprocessor in conjunction with Intel's Triton chip set.

- Pentium–Style Burst Counter on Chip
- Pipelined Data Out
- 160 Pin Card Edge Module
- Address Pipeline Supported by $\overline{ADSP}$ Disabled with $\overline{E}x$
- All Cache Data and Tag I/Os are TTL Compatible
- Three State Outputs
- Byte Write Capability
- Fast Module Clock Rates: 66 MHz
- Fast SRAM Access Times: 15 ns for Tag RAM
  9 ns for Data RAMs
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB with Separate Power and Ground Planes
- I/Os are 3.3 V Compatible on Data RAMs
- Burndy Connector, Part Number: CELP2X80SC3Z48
- Series 20 Ω Resistors for Noise Immunity

BurstRAM is a trademark of Motorola.
Pentium is a trademark of Intel Corp.

This document contains information on a new product. Motorola reserves the right to change or discontinue this product without notice.

REV 1
5/95

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MOTOROLA

PIN ASSIGNMENT
160–PIN CARD EDGE MODULE
TOP VIEW

V_{SS}	81	1	V_{SS}
TIO1	82	2	TIO0
TIO7	83	3	TIO2
TIO5	84	4	TIO6
TIO3	85	5	TIO4
(RSVD) NC	86	6	NC (RSVD)
$V_{CC}5$	87	7	$V_{CC}3$
(RSVD) NC	88	8	$\overline{TWE}$
*(CAA4) CADV	89	9	CADS (CAA3)*
V_{SS}	90	10	V_{SS}
$\overline{COE}$	91	11	$\overline{CWE4}$
$\overline{CWE5}$	92	12	$\overline{CWE6}$
$\overline{CWE7}$	93	13	$\overline{CWE0}$
CWE1	94	14	CWE2
$V_{CC}5$	95	15	$V_{CC}3$
CWE3	96	16	CCS (CAB4)*
*(CAB3) NC	97	17	NC ($\overline{GWE}$)**
*(CALE) NC	98	18	NC (BWE)**
V_{SS}	99	19	V_{SS}
(RSVD) NC	100	20	A3
A4	101	21	A7
A6	102	22	A5
A8	103	23	A11
A10	104	24	A16
$V_{CC}5$	105	25	$V_{CC}3$
A17	106	26	NC (A18)†
V_{SS}	107	27	V_{SS}
A9	108	28	A12
A14	109	29	$\overline{A13}$
A15	110	30	$\overline{ADSP}$ $\overline{\quad}$
(RSVD) NC	111	31	NC ($\overline{ECS1}$, CS)
PD0	112	32	NC (ECS2)
PD2	113	33	PD1
PD4	114	34	PD3
V_{SS}	115	35	V_{SS}
CLK0	116	36	CLK1
V_{SS}	117	37	V_{SS}
DQ63	118	38	DQ62
$V_{CC}5$	119	39	$V_{CC}3$
DQ61	120	40	DQ60
DQ59	121	41	DQ58
DQ57	122	42	DQ56
V_{SS}	123	43	V_{SS}
DQ55	124	44	DQ54
DQ53	125	45	DQ52
DQ51	126	46	DQ50
DQ49	127	47	DQ48
V_{SS}	128	48	V_{SS}
DQ47	129	49	DQ46
DQ45	130	50	DQ44
DQ43	131	51	DQ42
$V_{CC}5$	132	52	$V_{CC}3$
DQ41	133	53	DQ40
DQ39	134	54	DQ38
DQ37	135	55	DQ36
V_{SS}	136	56	V_{SS}
DQ35	137	57	DQ34
DQ33	138	58	DQ32
DQ31	139	59	DQ30
$V_{CC}5$	140	60	$V_{CC}3$
DQ29	141	61	DQ28
DQ27	142	62	DQ26
DQ25	143	63	DQ24
V_{SS}	144	64	V_{SS}
DQ23	145	65	DQ22
DQ21	146	66	DQ20
DQ19	147	67	DQ18
$V_{CC}5$	148	68	$V_{CC}3$
DQ17	149	69	DQ16
DQ15	150	70	DQ14
DQ13	151	71	DQ12
V_{SS}	152	72	V_{SS}
DQ11	153	73	DQ10
DQ9	154	74	DQ8
DQ7	155	75	DQ6
$V_{CC}5$	156	76	$V_{CC}3$
DQ5	157	77	DQ4
DQ3	158	78	DQ2
DQ1	159	79	DQ0
V_{SS}	160	80	V_{SS}

PRESENCE DETECT TABLE

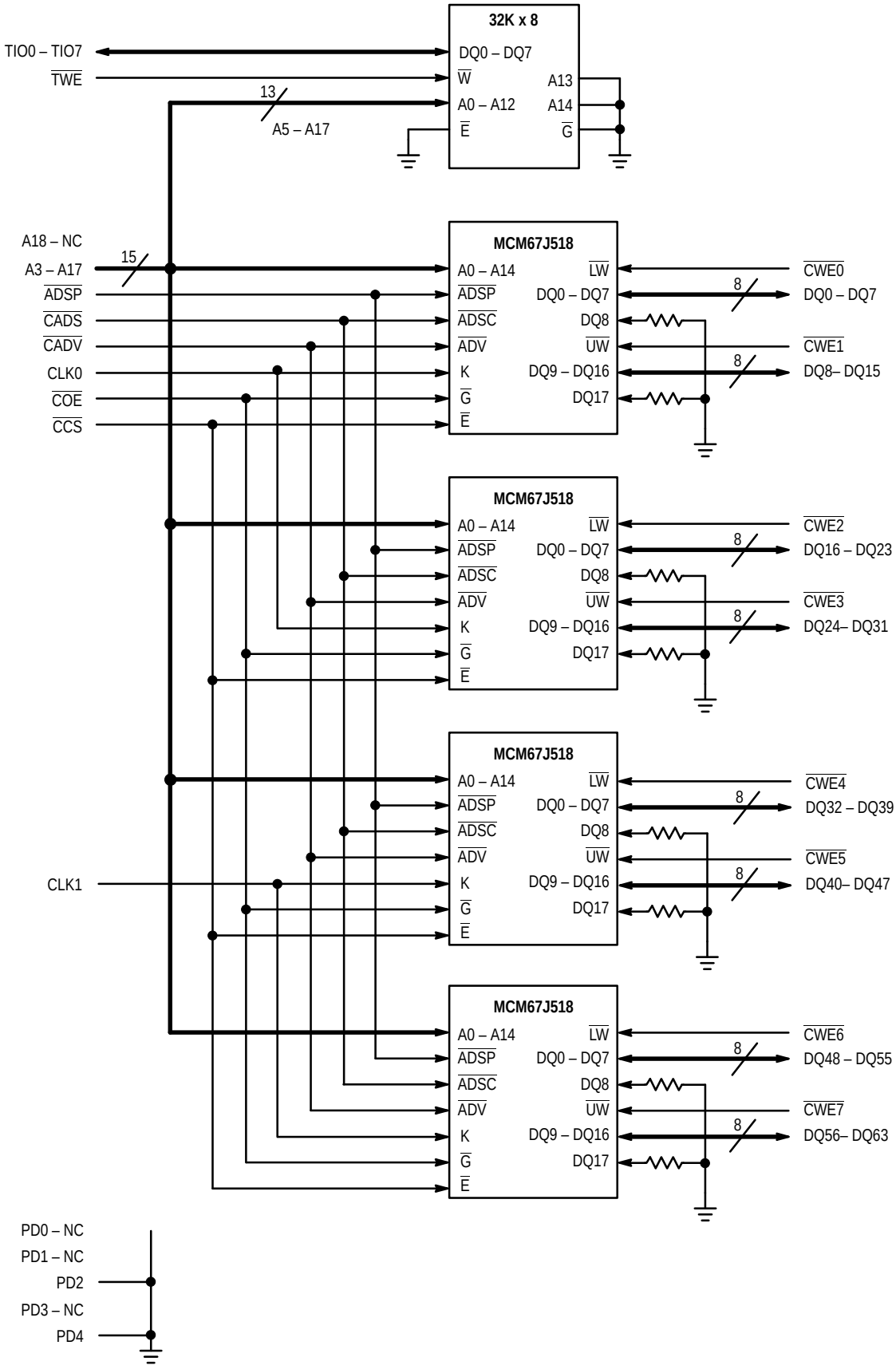
Cache Size and Functionality	Module	PD4	PD3	PD2	PD1	PD0
256K Async	MCM64AF32	V_{SS}	NC	V_{SS}	V_{SS}	NC
512K Async	—	V_{SS}	V_{SS}	NC	V_{SS}	NC
256K Burst	—	V_{SS}	NC	V_{SS}	NC	V_{SS}
256K Pipe Burst	MCM72JG32	V_{SS}	NC	V_{SS}	NC	NC
512K Burst	—	V_{SS}	V_{SS}	NC	NC	V_{SS}
512K Pipe Burst	MCM72JG64	V_{SS}	V_{SS}	NC	NC	NC
512K 2–Bank Burst	—	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}

PIN NAMES

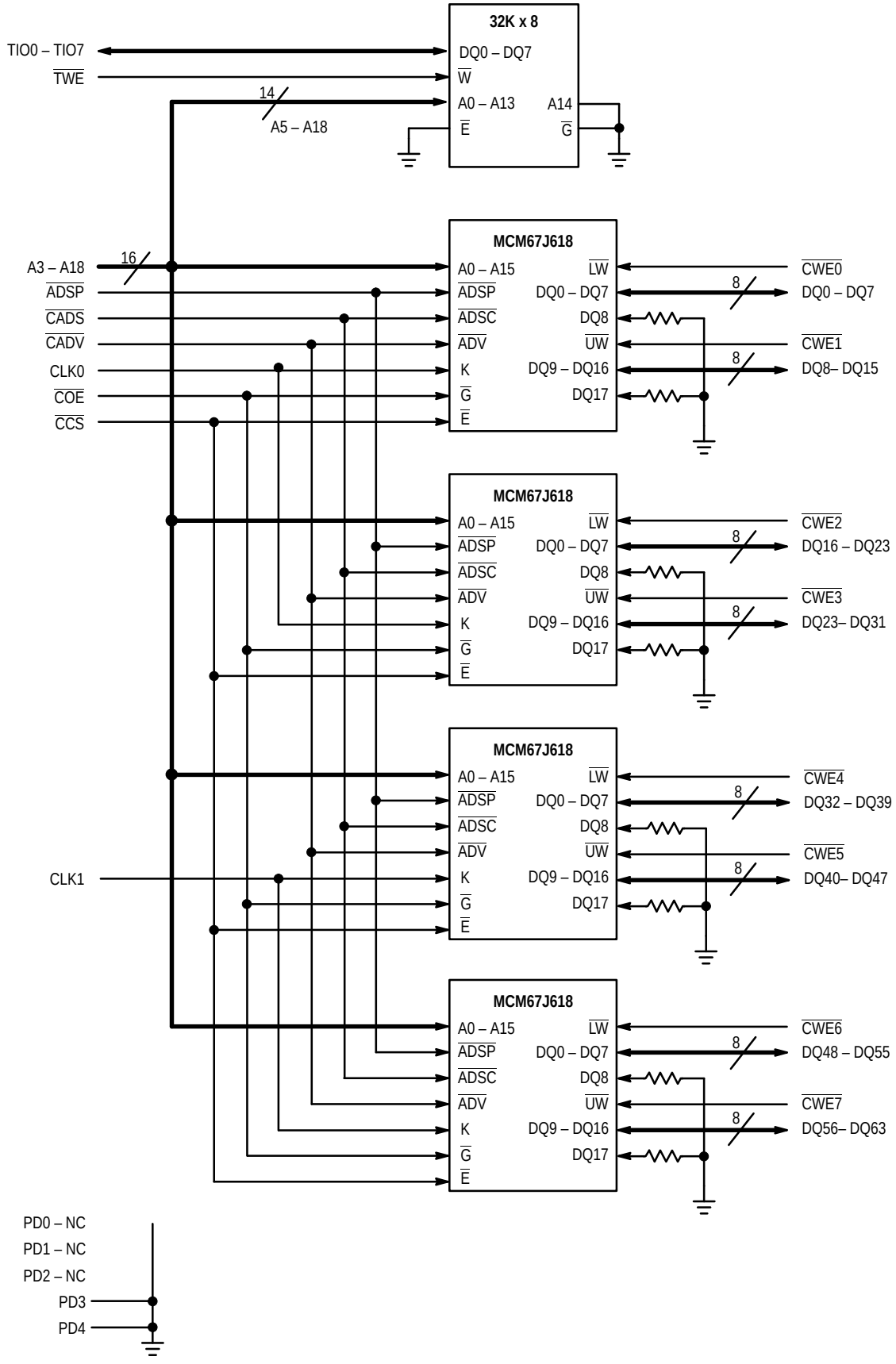
A3 – A18	Cache Address
DQ0 – DQ63	Data Input/Output
CLK0, CLK1	Clock
$\overline{CWE0}$ – $\overline{CWE7}$	Cache Write Enable
$\overline{BWE}$**	Byte Write Enable
$\overline{GWE}$**	Global Write Enable
TIO0 – TIO7	Tag Input/Output
$\overline{TWE}$	Tag Write Enable
$\overline{CADS}$	Cache Address Status
$\overline{ADSP}$	Address Status Processor
$\overline{CADV}$	Cache Burst Advance
$\overline{COE}$	Cache Output Enable
$\overline{CCS}$	Cache Chip Select
RSVD	Reserved for Future Use
PD0 – PD4	Presence Detect
$V_{CC}5$	+ 5 V Power Supply
$V_{CC}3$	+ 3.3 V Power Supply
V_{SS}	Ground
NC	No Connect

NOTES:
- * Signals in parentheses indicate pin descriptions for asynchronous Triton chip set module.
- ** Signals in parentheses will be implemented in future burstable Triton modules.
- † NC for MCM72JG32, A18 for MCM72JG64.

MCM72JG32 MODULE BLOCK DIAGRAM



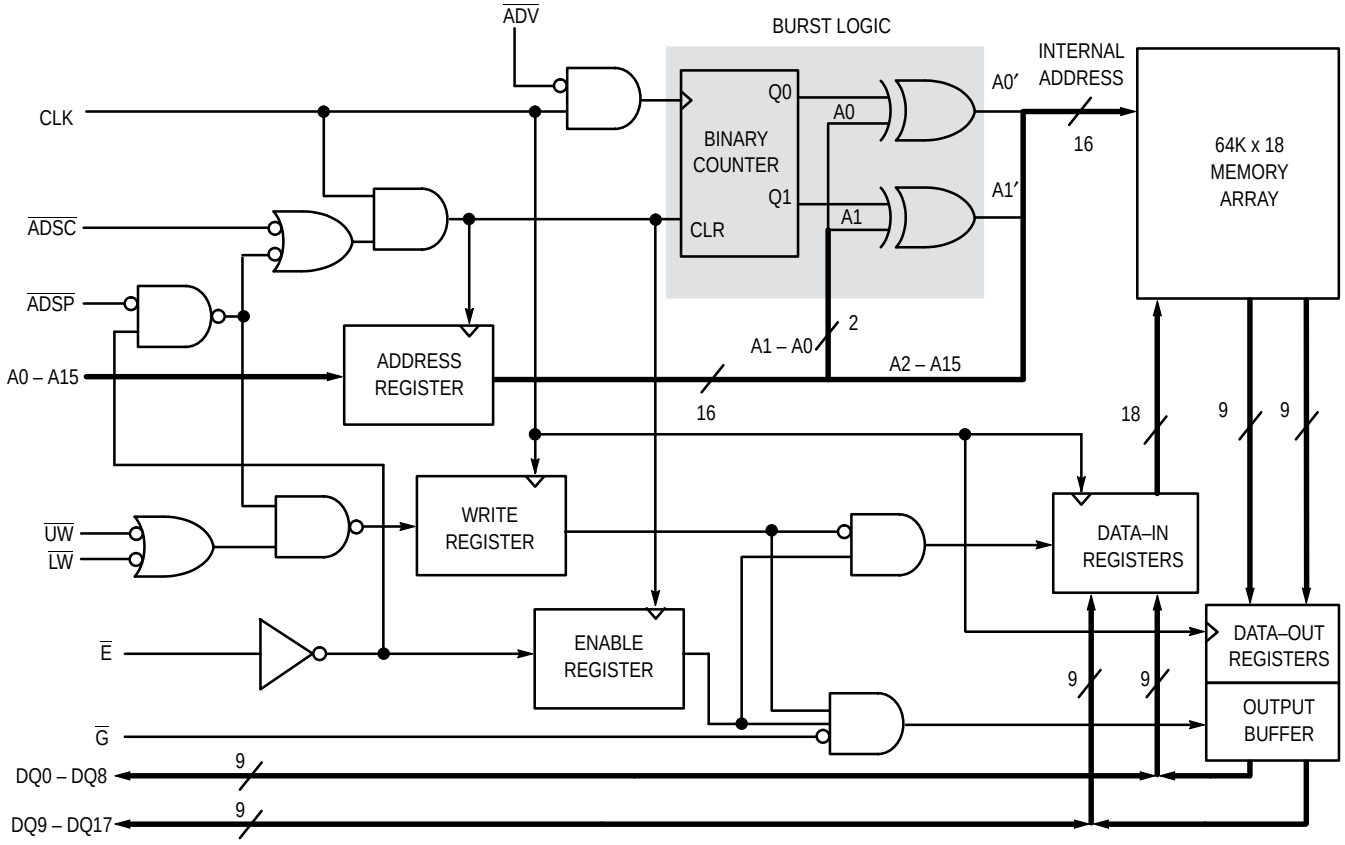
MCM72JG64 MODULE BLOCK DIAGRAM



PIN DESCRIPTIONS

160–Lead Card Edge Pin Locations	Symbol	Type	Description
20, 21, 22, 23, 24, 28, 29, 101, 102, 103, 104, 106, 108, 109, 110	A3 – A18	Input	Address Inputs: These inputs are registered into data RAMs and must meet setup and hold times. The tag RAM addresses are not registered.
36, 116	CLK0, CLK1	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{\text{COE}}$.
11, 12, 13, 14, 92, 93, 94, 96	$\overline{\text{CWE0}}$ – $\overline{\text{CWE7}}$	Input	Cache Data Byte Write Enable: Active low write signal for data RAMs.
8	$\overline{\text{TWE}}$	Input	Tag Write Enable: Active low write signal for tag RAMs.
—	$\overline{\text{BWE}}$	Input	Byte Write Enable: To be used in future modules.
—	$\overline{\text{GWE}}$	Input	Global Write Enable: To be used in future modules.
16	$\overline{\text{CCS}}$	Input	Chip Select: Active low chip enable for data RAMs.
30	$\overline{\text{ADSP}}$	Input	Address Status Processor: Initiates READ, WRITE, or chip deselect cycle (Exception–chip deselect does not occur when $\overline{\text{ADSP}}$ is asserted and $\overline{\text{CCS}}$ is high.
9	$\overline{\text{CADS}}$	Input	Cache Address Status: Initiates READ, WRITE, or chip deselect cycle.
89	$\overline{\text{CADV}}$	Input	Cache Burst Advance: Increments address count in accordance with interleaved count style.
91	$\overline{\text{COE}}$	Input	Cache Output Enable: Active low asynchronous input. Low–enables output buffers (DQ pins) High–DQx pins are high impedance.
38, 40, 41, 42, 44, 45, 46, 47, 49, 50, 51, 53, 54, 55, 57, 58, 59, 61, 62, 63, 65, 66, 67, 69, 70, 71, 73, 74, 75, 77, 78, 79, 118, 120, 121, 122, 124, 125, 126, 127, 129, 130, 131, 133, 134, 135, 137, 138, 139, 141, 142, 143, 145, 146, 147, 149, 150, 151, 153, 154, 155, 157, 158, 159	DQ0 – DQ63	I/O	Synchronous Data I/O: Drives data out of data RAMs during READ cycles. Stores data to data RAMs during WRITE cycles.
2, 3, 4, 5, 82, 83, 84, 85	TIO0 – TIO7	I/O	Tag RAM I/O: Drives data out during tag compare cycles. Stores data to tag RAM during tag WRITE cycles.
33, 34, 112, 113, 114	PD0 – PD4	—	Presence Detect: See Presence Detect Table
7, 15, 25, 39, 52, 60, 68, 76	$V_{CC}3$	Supply	Power Supply: 3.3 V ± 5%.
87, 95, 105, 119, 132, 140, 148, 156	$V_{CC}5$	Supply	Power Supply: 5.0 V ± 5%.
1, 10, 19, 27, 35, 37, 43, 48, 56, 64, 72, 80, 81, 90, 99, 107, 115, 117, 123, 128, 136, 144, 152, 160	V_{SS}	Supply	Ground
6, 17, 18, 26, 31, 32, 86, 88, 97, 98, 100, 111	NC	—	No Connection: There is no connection to the module.

64K x 18 BurstRAM BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{\text{ADSC}}$ or $\overline{\text{ADSP}}$ signals control the duration of the burst and the start of the next burst. When $\overline{\text{ADSP}}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{\text{CWE}}$ and $\overline{\text{ADSC}}$) is performed using the new external address. Alternatively, an $\overline{\text{ADSP}}$–initiated two cycle WRITE can be performed by negating both $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ and asserting $\overline{\text{LW}}$ and/or $\overline{\text{UW}}$ with valid data on the second cycle (see Single Write cycle in WRITE CYCLES timing diagram). When $\overline{\text{ADSC}}$ is sampled low (and $\overline{\text{ADSP}}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{\text{CWE}}$) is performed using the new external address. Chip enable ($\overline{\text{E}}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{\text{ADV}}$ controls subsequent burst cycles. When $\overline{\text{ADV}}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{\text{ADV}}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{\text{LW}}$, $\overline{\text{UW}}$).

64K x 18 BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{\text{A0}}$
2nd Burst Address	A15 – A2	$\overline{\text{A1}}$	A0
3rd Burst Address	A15 – A2	$\overline{\text{A1}}$	$\overline{\text{A0}}$

NOTE: The burst wraps around to its initial state upon completion.

NOTE: The above BurstRAM Block Diagram and Burst Sequence Table apply specifically tothe 64K x 18 chip. The 32K x 18 chip is functionally identical but has no A15.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{CCS}$	$\overline{ADSP}$	$\overline{CADS}$	$\overline{CADV}$	$\overline{CWEx}$	CLK0/1	Address Used	Operation
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{COE}$ must meet setup and hold times for the low–to–high transition of clock (CLK0/1).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{COE}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}5$	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{COE}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
TTL Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
TTL Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

POWER SUPPLY CURRENTS

Parameter	Symbol	Max	Unit
AC Supply Current ($\overline{COE}$ = V_{IH}, $\overline{CCS}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	1300	mA
AC Standby Current ($\overline{COE}$ = V_{IH}, $\overline{CCS}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	340	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	(Address and Control)	C_{in}	28	pF
Input Capacitance	(CLK0, CLK1)	C_{in}	12	pF
Input/Output Capacitance	(DQ0 – DQ63)	$C_{I/O}$	10	pF

DATA RAMs AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

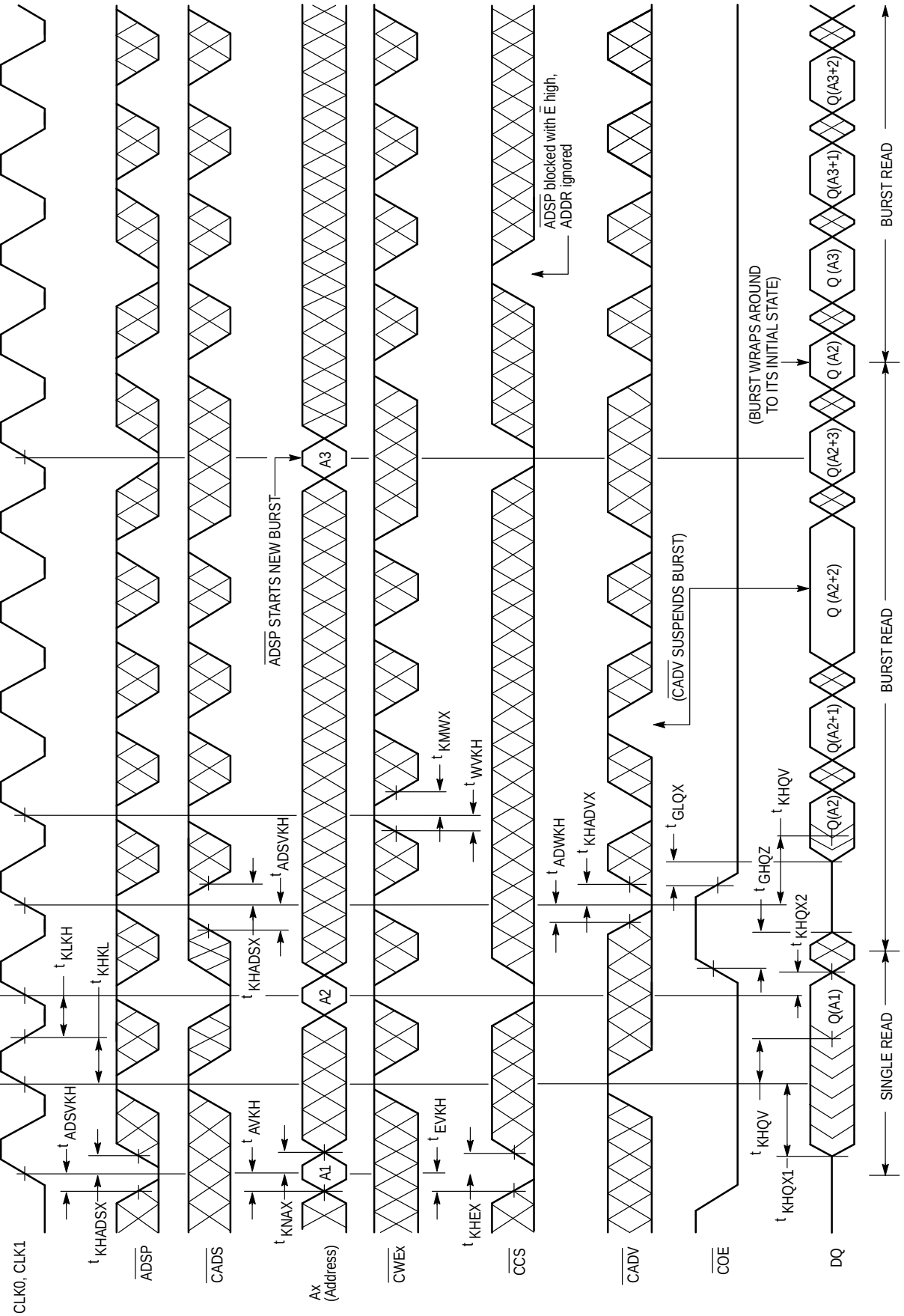
Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A Unless Otherwise Noted

DATA RAMs READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

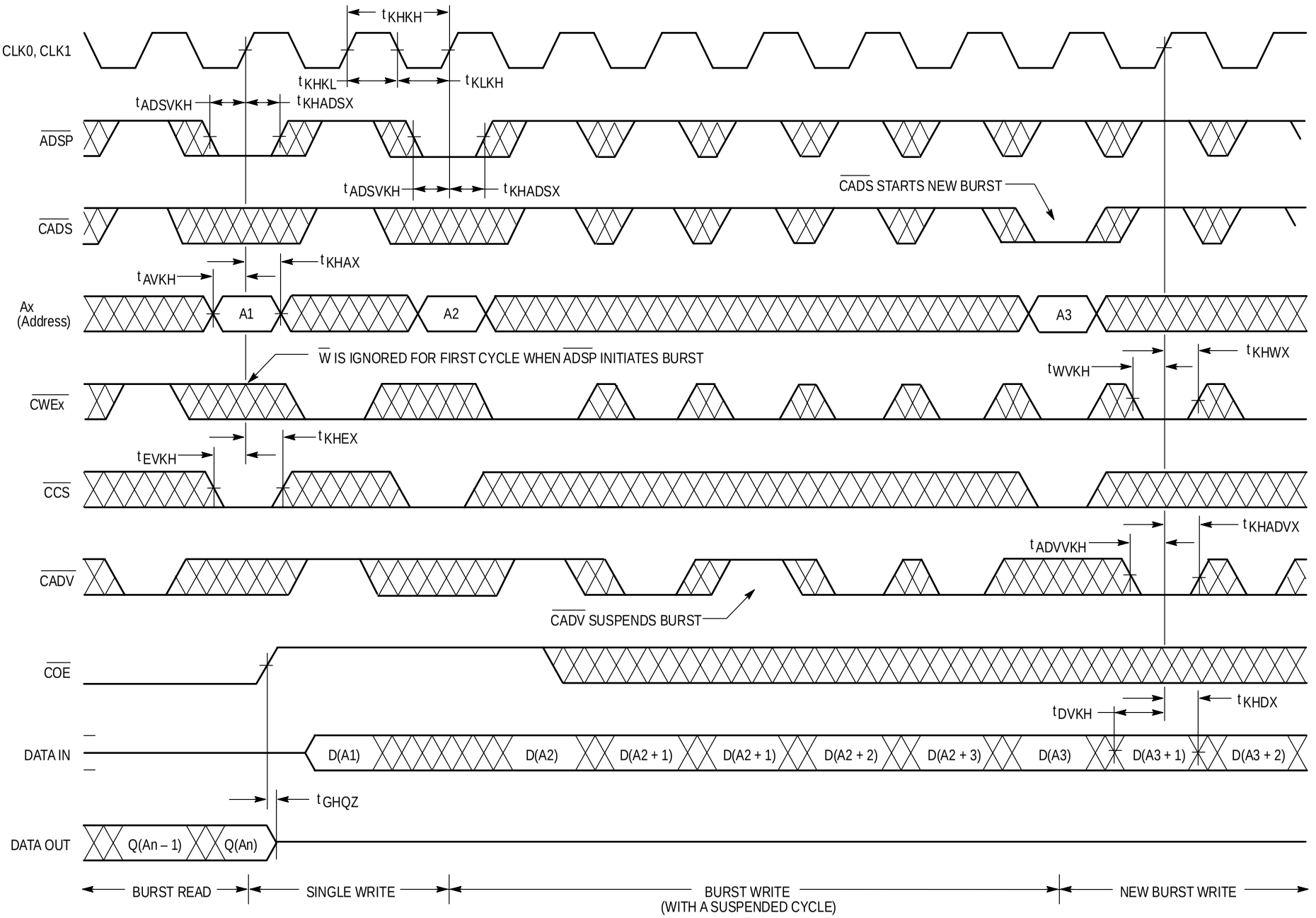
Parameter	Symbol	MCM72JG32–66 MCM72JG64–66 Min	Max	Unit	Notes
Cycle Time	t_{KHKH}	15	—	ns	
Clock Access Time	t_{KHQV}	—	7	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	ns	
Clock High to Output Active	t_{KHQX1}	2	—	ns	
Clock High to Output Change	t_{KHQX2}	2	—	ns	
Output Enable to Output Active	t_{GLQX}	1	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	ns	6
Clock High to Q High–Z	t_{KHQZ}	2	6	ns	
Clock High Pulse Width	t_{KHKL}	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Enable	t_{AVKH} t_{ADSVKH} t_{DVKH} t_{WVKH} t_{ADVVKH} t_{EVKH}	2.5	—	ns	7
Hold Times: Address Address Status Data In Write Address Advance Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHADVX} t_{KHEX}	0.5	—	ns	7

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from CLK or $\overline{COE}$.
4. $\overline{COE}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 amd Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of CLK whenever $\overline{ADSP}$ or $\overline{CADS}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of CLK when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{CADS}$ is low) to remain enabled.

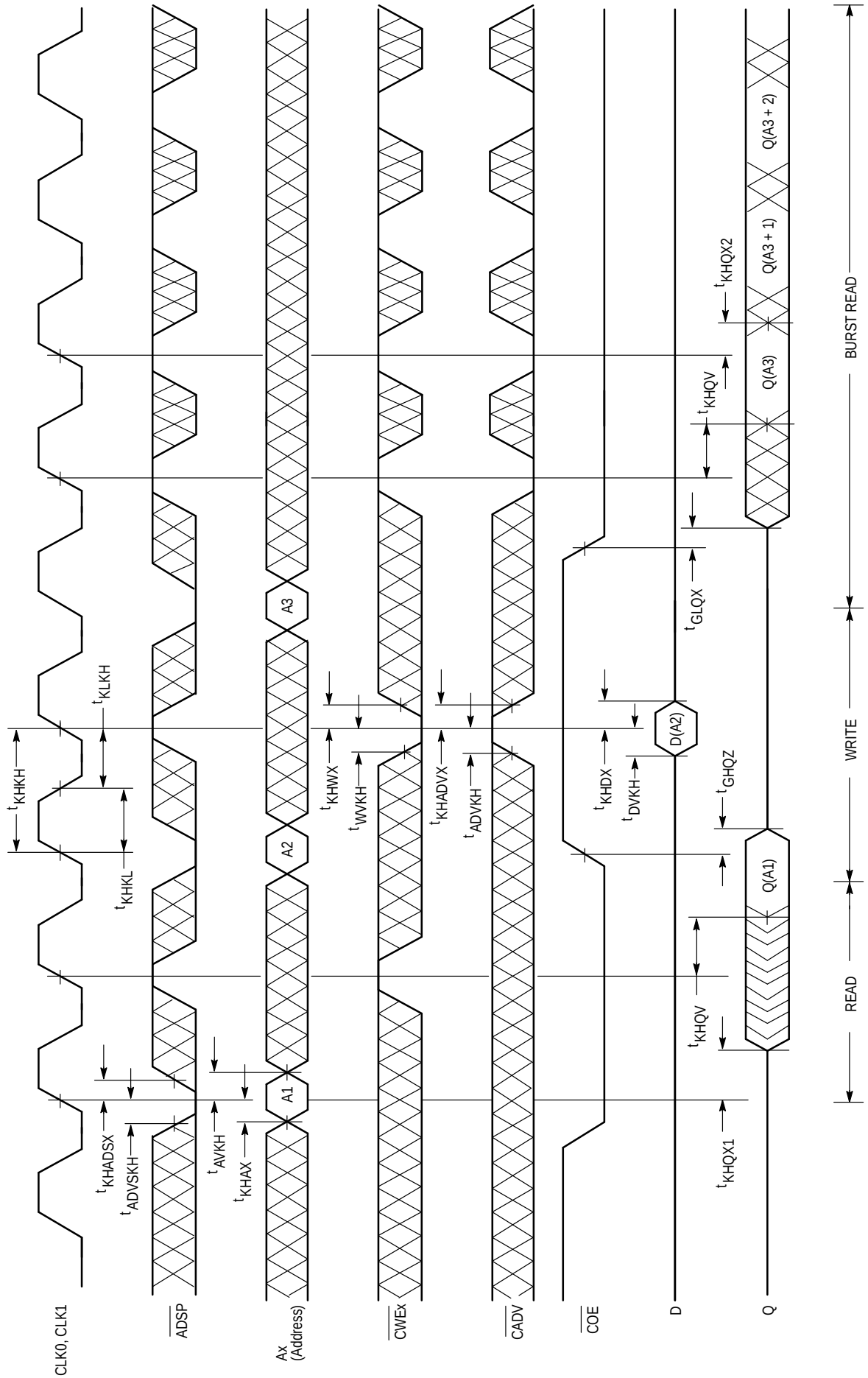
DATA RAMs READ CYCLES



DATA RAMs WRITE CYCLES



DATA RAMs COMBINATION READ/WRITE CYCLES ($\overline{CCS}$ low, $\overline{CADS}$ high)



TAG RAM AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

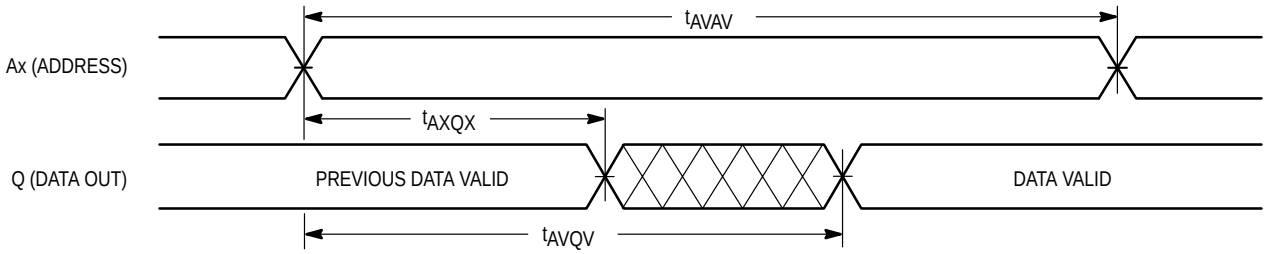
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

TAG RAM READ CYCLE (See Note 1 and 5)

Parameter	Symbol	– 15		Unit	Notes
		Min	Max		
Read Cycle Time	t_{AVAV}	15	—	ns	2
Address Access Time	t_{AVQV}	—	15	ns	
Output Hold from Address Change	t_{AXQX}	4	—	ns	3, 4

NOTES:
1. $\overline{CWE}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first address transition.
3. Transition is measured ±500 mV from steady–state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.
5. Device is continuously selected ($\overline{COE}$ = V_{IL}).

TAG RAM READ CYCLE (See Note 5)

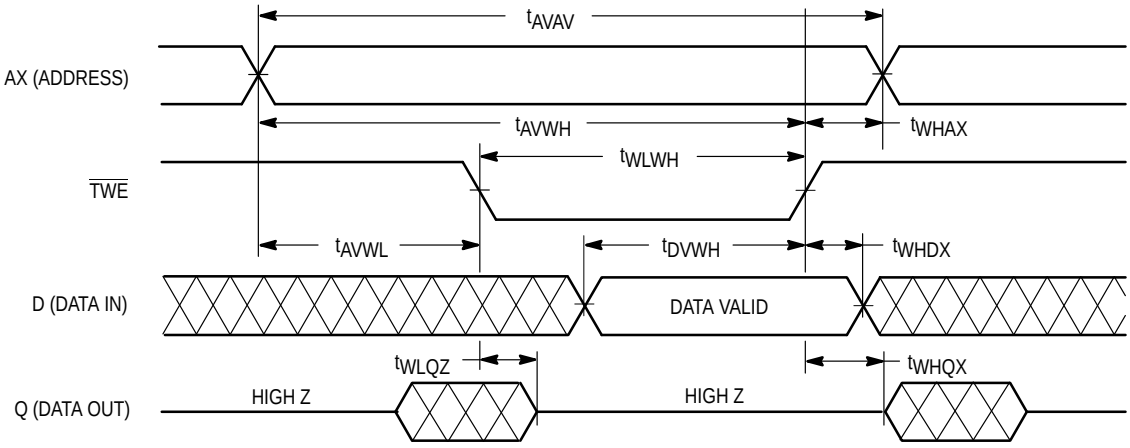


TAG RAM WRITE CYCLE (See Notes 1 and 2)

Parameter	Symbol	– 15		Unit	Notes
		Min	Max		
Write Cycle Time	t_{AVAV}	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	7	ns	5,6,7
Write High to Output Active	t_{WHQX}	4	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	0	—	ns	

NOTES:
1. A write occurs when $\overline{CWE}$ is low.
2. If $\overline{COE}$ goes low coincident with or after $\overline{CWE}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first address transition.
4. If $\overline{COE} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
6. Transition is measured ±500 mV from steady–state voltage with load of Figure 2B.
7. This parameter is sampled and not 100% tested.

TAG RAM WRITE CYCLE (See Notes 1 and 2)



AC TEST LOADS

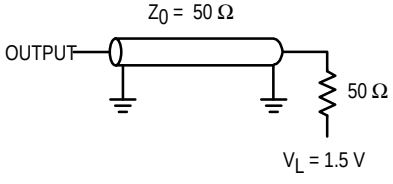


Figure 1A

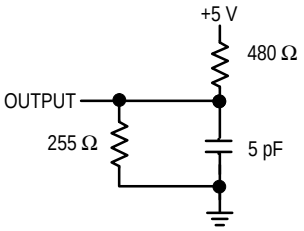
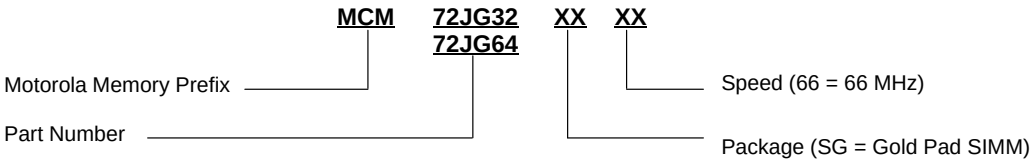


Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

ORDERING INFORMATION
(Order by Full Part Number)

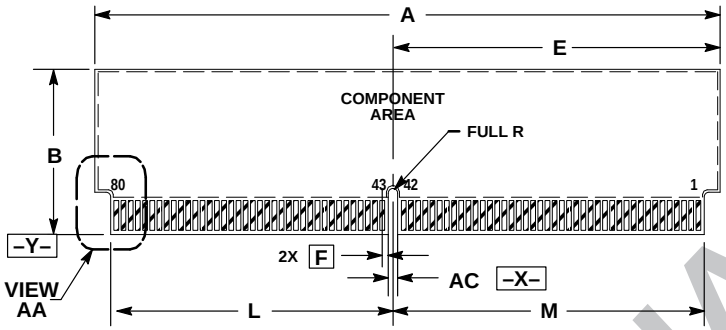


Full Part Numbers — MCM72JG32SG66 MCM72JG64SG66

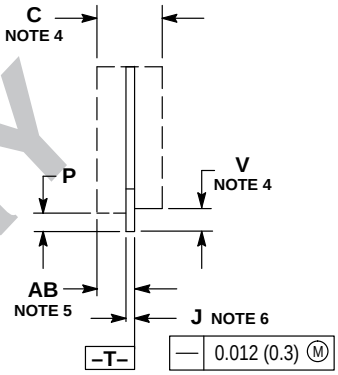
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PACKAGE DIMENSIONS

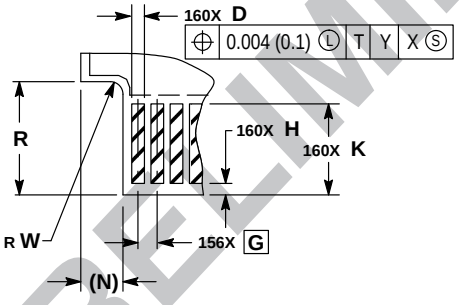
160–LEAD
CARD EDGE MODULE
CASE 1113A–01



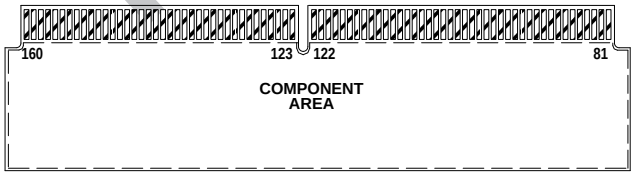
FRONT VIEW



SIDE VIEW



VIEW AA



BACK VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS C AND V DEFINE A DOUBLE–SIDED MODULE.
5. DIMENSION AB DEFINES OPTIONAL SINGLE–SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.330	4.350	109.98	110.49
B	1.270	1.310	32.26	33.27
C	—	0.454	—	11.53
D	0.033	0.037	0.84	0.94
E	2.265	2.275	57.53	57.79
F	0.075 BSC		1.91 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.030	—	0.51
J	0.055	0.069	1.40	1.75
K	0.210	—	5.33	—
L	1.955	1.965	49.66	49.91
M	2.155	2.165	54.74	54.99
N	0.110 REF		2.79 REF	
P	0.125	—	3.18	—
R	0.285	0.305	7.24	7.75
V	0.157	—	3.99	—
W	0.040	0.060	1.02	1.52
AB	—	0.262	—	6.66
AC	0.072	0.076	1.83	1.93

PRELIMINARY

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