100V Linear Bias Supply

ISL6719

The ISL6719 is a low cost linear regulator for generating a low voltage bias supply from intermediate distributed voltages commonly used in telecom and datacom applications. It provides a single adjustable output rated at 100mA from either the input source or an auxiliary source such as a transformer winding. The auxiliary source is selected whenever it has sufficient voltage to sustain the output.

The ISL6719 may be used as a start-up or a continuous low power regulator. When operating as a start-up regulator, it is capable of sourcing 100mA from a 100V source for short durations. This period of time allows the power supply to start-up and provide an alternate power source, such as the output of a transformer winding, to the AUXIN input. This allows the regulated output to operate from a lower source voltage to minimize power loss.

Features

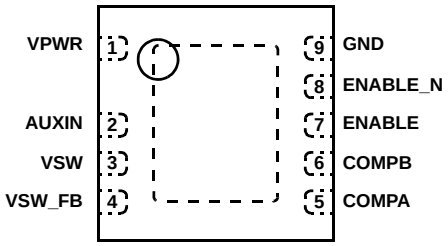
- 100V+ input capability
- Adjustable output from 1.5V to 20V
- Up to 100mA output current
- Overcurrent protection
- Over-temperature protection
- ENABLE and ENABLE_N inputs
- Package compliant with IPC2221A, creepage and clearance spacing requirements

Applications

- Telecom/datacom DC/DC converters
- Low power bias supplies

Pin Configuration

ISL6719
(9 LD DFN)
TOP VIEW



Ordering Information

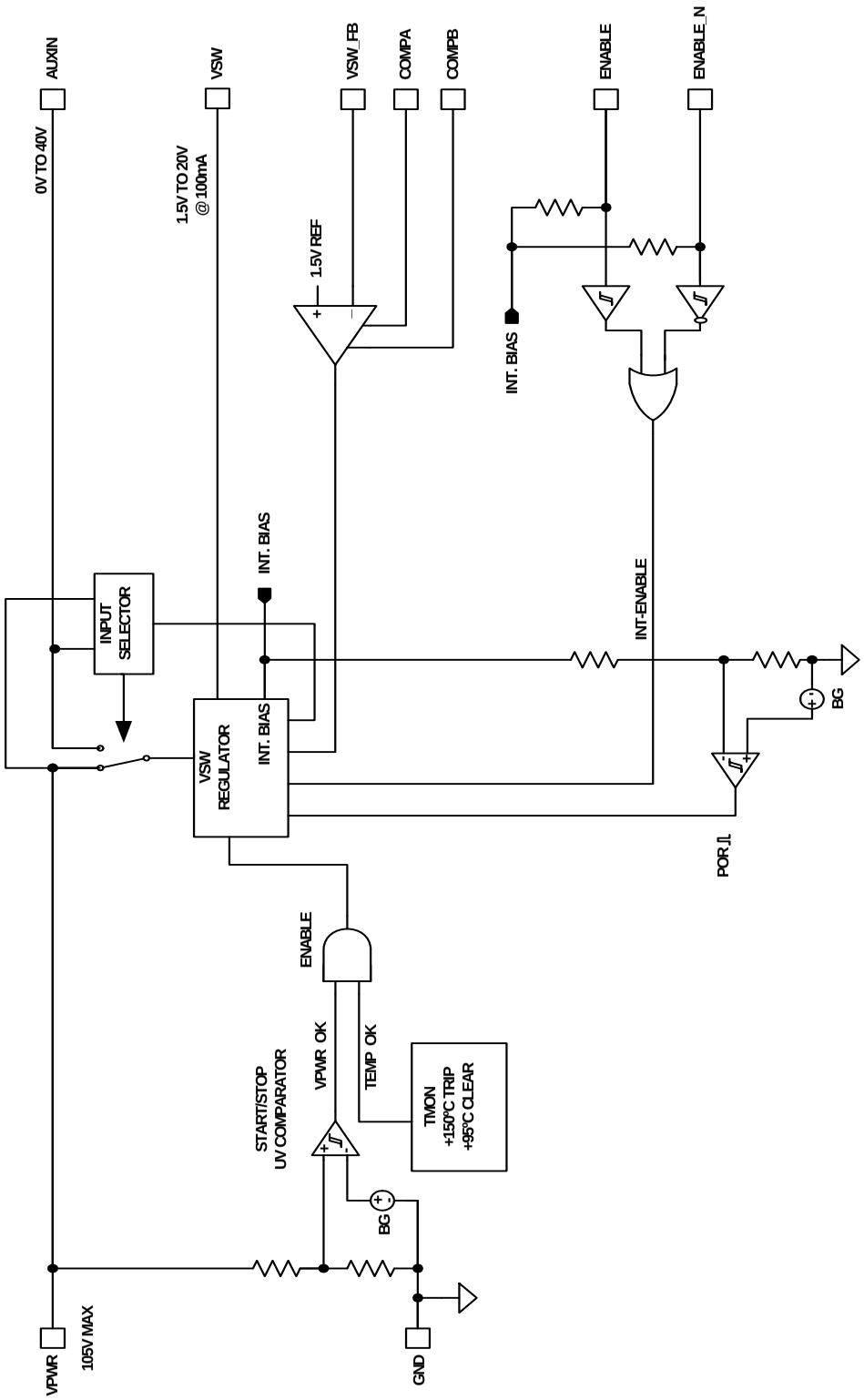
PART NUMBER (Note 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6719ARZ	19AZ	-40 to +105	9 Ld DFN	L9.3x3

NOTES:

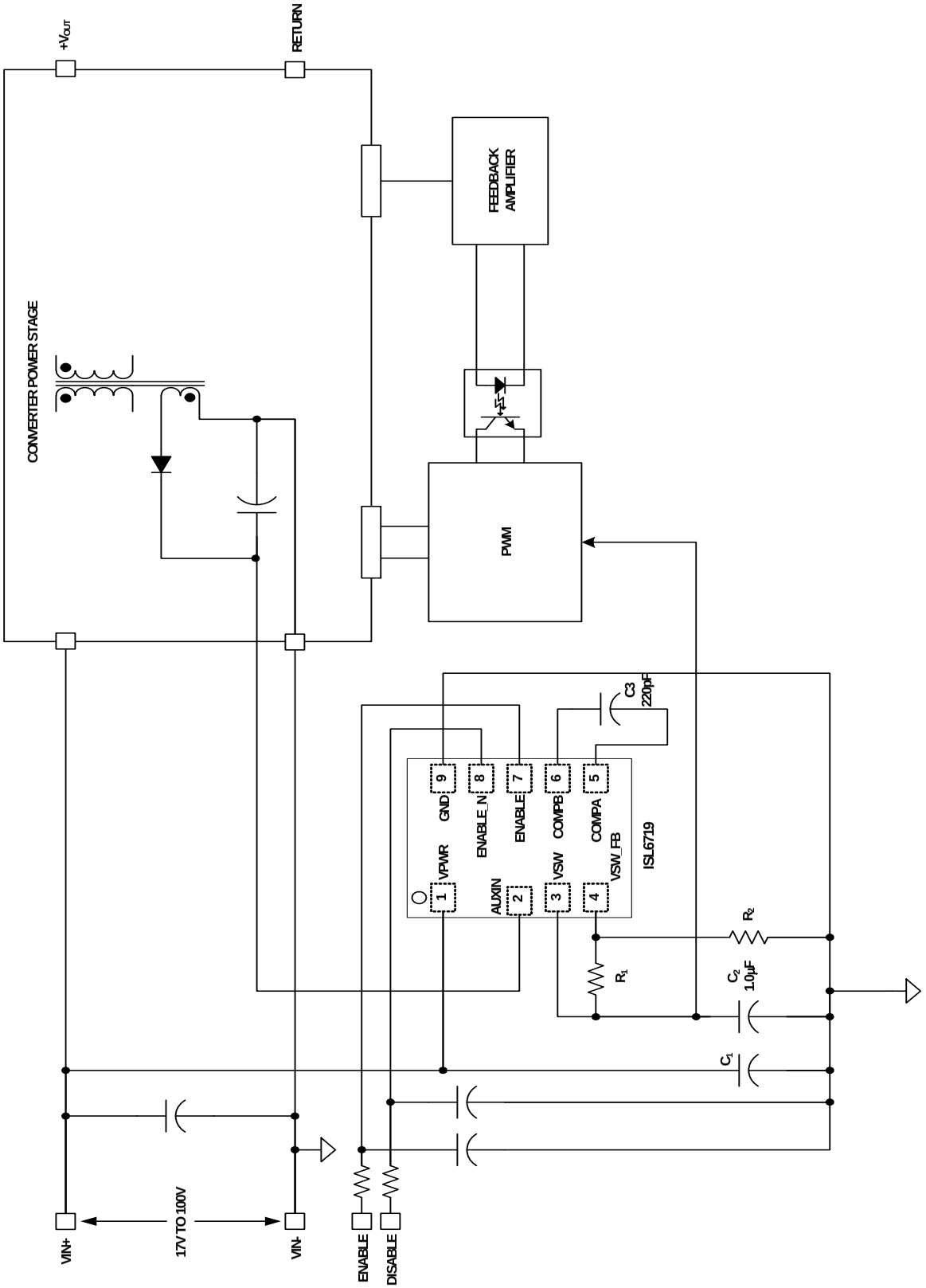
1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6719. For more information on MSL, please see tech brief TB363.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Functional Block Diagram



Typical Application



Absolute Maximum Ratings

Supply Voltage, VPWR . . . . . GND - 0.3V to + 105V
AUXIN, VSW_FB . . . . . GND - 0.3V to + 40V
COMPB . . . . . GND - 0.3V to + 30V
VSW . . . . . GND - 0.3V to + 25V
All Others . . . . . GND - 0.3V to + 6.0V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
9 Ld DFN (Notes 4, 5)	54	2.8

Maximum Junction Temperature . . . . . -55°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +105°C
Supply Voltage Range (Typical) . . . . . 18VDC to 80VDC

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. All voltages are with respect to GND.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 2 and "Typical Application" on page 3. 17V < VPWR < 100V, C_{VSW} = 1µF, I_{VSW} = -3mA, VSW Enabled, T_A = -40°C to +105°C (Note 7), Typical values are at T_A = +25°C.

PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
SUPPLY VOLTAGE (VPWR)					
Supply Voltage				100	V
Start-Up Current (I_{VPWR})	VPWR = 12V		250	450	µA
Operating Current (I_{VPWR})	VSW Enabled, VPWR = 100V, VSW = 10V, 20V, I_{VPWR} - I_{VSW}		1.1	2.0	mA
	VSW Disabled, VPWR = 100V,		1.1	2.0	mA
	AUXIN Biased at 40V, VSW Enabled, VPWR = 100V, VSW = 10V, 20V, I_{VSW} = -100mA		1.1	2.0	mA
UVLO START Threshold	VSW Disabled	13.0		16.5	V
UVLO STOP Threshold	VSW Disabled	12.0		15.0	V
Hysteresis	UVLO START - UVLO STOP	0.8	1.2	1.7	V
AUXILIARY VOLTAGE (AUXIN)					
Maximum Bias	VPWR = 17V, 100V			40	V
OUTPUT VOLTAGE (VSW)					
Load Capacitance Range	(Note 9)	0.47	1.0	1.5	µF
Overall Accuracy	VPWR = 18V, 100V, VSW = 5V, 10V, 12V AUXIN = 15V, I_{VSW} = -3mA to -100mA	-5		+5	%
Setpoint Range	VPWR = 100V, AUXIN = 30V	1.55		20	V
Reference	VSW_FB = VSW	1.45	1.50	1.55	V
Source Voltage Headroom (AUXIN - VSW)	VPWR = 17V, VSW = 10V, I_{AUXIN} = 0.95*I_{VSW}				
	I_{VSW} = -100mA		1.8	3.0	V
	I_{VSW} = -50mA		1.4	2.0	V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 2 and "Typical Application" on page 3. 17V < VPWR < 100V, C_{VSW} = 1µF, I_{VSW} = -3mA, VSW Enabled, T_A = -40°C to +105°C (Note 7), Typical values are at T_A = +25°C. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Source Voltage Headroom (VPWR - VSW)	VSW = 20V, AUXIN = 0V				
	I_{VSW} = -100mA			6.2	V
	I_{VSW} = -50mA			5.2	V
Minimum Required Load				-3	mA
Maximum VOUT, Faulted VSW_FB	VSW_FB = 0V, VPWR = 100V, AUXIN = 40V	21		25	V
Long Term Stability	T_A = +125°C, 1000 hours (Note 8), VPWR = 48V, VSW = 10V, I_{VSW} = -10mA, AUXIN = 15V		0.3		%
Operational Current (source)	VPWR = 48V, AUXIN = 17V, VSW = 15V	-100			mA
Current Limit	VPWR = 48V, AUXIN = 15V, VSW = 10V	-100	-230	-400	mA
VSW_FB Bias Current	VPWR = 100V, AUXIN = 40V, VSW = 10V, VSW_FB = 1.5V	-0.5		1.5	µA
COMPA, COMPB Recommended Capacitance	(Note 9)	170	220	270	pF
COMPA Voltage			0.7		V
COMPB Voltage			VSW + 5.0		V
ENABLE, ENABLE_N					
High Level Input Voltage (VIH)	VPWR = 48V, AUXIN = 0V	2.5	3.0	3.6	V
Low Level Input Voltage (VIL)	VPWR = 48V, AUXIN = 0V	1.6	2.0	2.5	V
Hysteresis	VPWR = 48V, AUXIN = 0V	0.7	1.0	1.3	V
Pull-Up Resistance	V_{ENABLE} = V_{N_ENABL} = 0V	-	100	-	kΩ
Turn-On Delay	$T_{VSW,\ 10\%}$ - T_{ENABLE}, $T_{VSW,10\%}$ - T_{ENABLE_N}, I_{VSW} = -3mA		25		µs
Turn-Off Delay	$T_{VSW,\ 10\%}$ - T_{ENABLE}, $T_{VSW,10\%}$ - T_{ENABLE_N}, I_{VSW} = -50mA		40		µs
THERMAL PROTECTION					
Thermal Shutdown			150		°C
Thermal Shutdown Clear			95		°C
Hysteresis			55		°C

NOTE:

7. Specifications at -40°C and +105°C are guaranteed by +25°C test with margin limits.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
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Typical Performance Curves

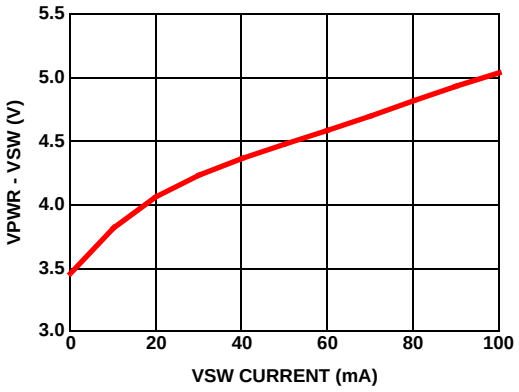


FIGURE 1. VPWR - VSW vs I_{VSW} @ AUXIN = 0V, +25°C

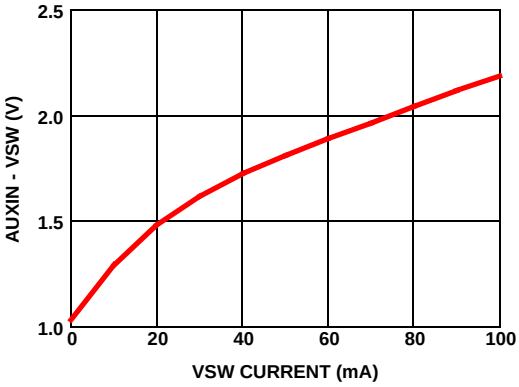


FIGURE 2. AUXIN - VSW vs I_{VSW} @ VPWR = 17V, +25°C

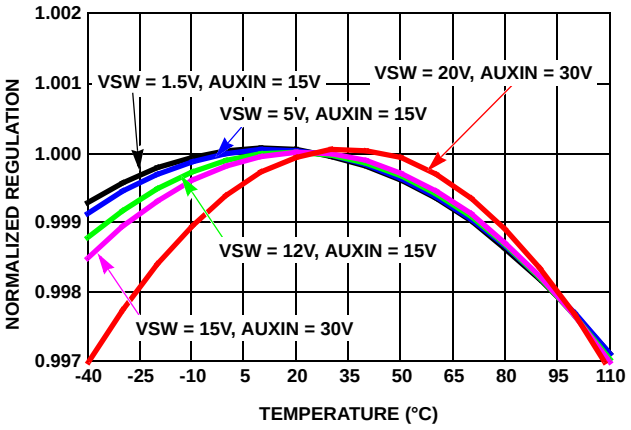


FIGURE 3. VSW REGULATION vs TEMPERATURE @ VPWR = 100V, I_{VSW} = 3mA

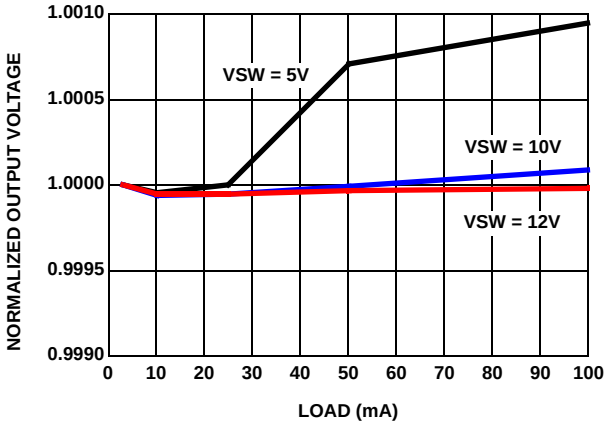


FIGURE 4. VSW REGULATION vs LOAD @ VPWR = 18V, AUXIN = 15V, +25°C

Pin Descriptions

VPWR

VPWR is the power connection for the IC. UVLO enables/disables the output and places the device into a standby mode even if AUXIN is externally biased.

To optimize noise immunity, bypass VPWR to GND with a ceramic capacitor as close to the VPWR and GND pins as possible.

AUXIN

This is the input for an external bias source typically provided by an auxiliary transformer winding. This input is not required and may be grounded or left open. Maximum input bias is 40V.

ENABLE

The positive logic on/off control input. A logic high enables VSW. Asserting this signal low turns off VSW. ENABLE and ENABLE_N are logically ORed. Either signal can enable VSW, but both must be false to disable VSW.

ENABLE_N

The negative logic on/off control input. A logic low enables VSW. Asserting this signal high turns off VSW. ENABLE and ENABLE_N are logically ORed. Either signal can enable VSW, but both must be false to disable VSW.

GND

Signal and power ground connections for this device.

VSW

This is the switched regulated low voltage output supply that is derived from VPWR or AUXIN. Its output is adjustable from 1.5V to 20V using an appropriate divider from VSW to VSW_FB. Protection circuitry prevents the output from exceeding 25V in the event of a fault on VSW_FB (short high or low). The minimum output current capability is 100mA. VSW requires a minimum load of 3mA.

VSW_FB

The feedback pin for VSW. A divider from VSW to ground sets feedback for VSW and determines the output voltage.

COMPA, COMPB

A compensating capacitor is placed between COMPA and COMPB to stabilize the control loop. The values may vary depending on the output load and capacitance applied between VSW and GND, but for all applications having a 1.0µF load capacitor, a 220pF compensation capacitor is recommended. The voltage at COMPA is nominally 0.7V. The voltage at COMPB is nominally VSW +5.0V.

Functional Description

Features

The control circuitry used in Telecom/Datacom DC/DC converters typically requires an operating bias voltage significantly lower than the source voltage available to the converter. Many applications use a discrete linear regulator from the input source to create the bias supply. Often an auxiliary winding from the power transformer is used to supplement or replace the linear supply once the converter is operating. The auxiliary winding bias voltage may require regulation as well to minimize the voltage variation inherent in slave windings. When implemented discretely, this circuitry occupies significant PWB area, a considerable problem in today's high density converters.

The ISL6719 linear regulator simplifies the start-up and operating bias circuitry needed in Telecom and Datacom DC/DC converters by integrating these functions, and more, in a small 3mm x 3mm DFN package.

AUXIN

AUXIN is the auxiliary input of the ISL6719, accepting bias voltage whenever the input source voltage, VPWR, is above its undervoltage lockout (UVLO) threshold. The VSW selects AUXIN as its source when it is capable supporting the load on VSW. Otherwise VPWR is selected.

AUXIN can accept voltages up to 40V maximum. Voltages in excess of 40V, including transients, will cause permanent damage to the device. Care should be taken when connecting external sources through very long traces or lead wires. The lead inductance may cause unexpected transients in excess of the device's ratings. In such circumstances it is recommended that a small resistor be placed between AUXIN and the external source to dampen the transient. A value of 10Ω to 100Ω is usually sufficient.

VSW

The VSW is the switched output and may be turned on and off using the ENABLE or ENABLE_N pins. The VSW is adjustable from 1.5V to 20V, but must always be at least 6.2V lower than VPWR at rated load. Additionally, VSW must be at least 3.0V lower than AUXIN for it to function as the source for VSW. As the differential voltage between AUXIN and VSW drops below 3.0V, the input current will shift from AUXIN to VPWR. The voltage headroom required is load dependent (see Figures 1 and 2). The VSW preferentially uses AUXIN as its input source, but if AUXIN is unable to supply adequate voltage, VPWR is selected as the alternate input source. The VSW is capable of delivering up to 100mA continuously, depending on power dissipation and the thermal environment in which the device is placed.

The output voltage is adjusted using the VSW_FB input. The VSW is set with a resistor divider from VSW to ground with the central node connected to VSW_FB. Refer to Figure 5.

Referring to Equation 1, the V_{REF} is nominally 1.5V and I_{BIAS} has a maximum value of 1.5µA. The error introduced by the VSW_FB bias current can be minimized by making the product of R_1 x I_{BIAS} small, relative to the magnitude of the desired output voltage. For example, setting R_1 x I_{BIAS} equal to 0.5% of VSW yields a value for R_1 equal to 3.33 x VSW (kΩ).

$$VSW = V_{REF}\frac{R_1 + R_2}{R_2} - I_{BIAS}R_1 \quad V \qquad \text{(EQ. 1)}$$

The VSW requires an external compensation capacitor to remain stable across the output adjustment range, output capacitance and loading. A value of 220pF between COMPA and COMPB is recommended for all operating conditions with a nominal load capacitance of 1.0µF (0.47µF to 1.5µF). The VSW requires a minimum load of 3mA.

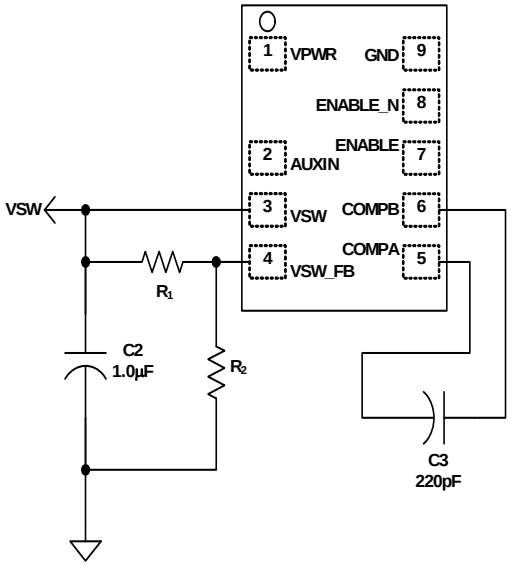


FIGURE 5. VSW ADJUSTMENT AND COMPENSATION

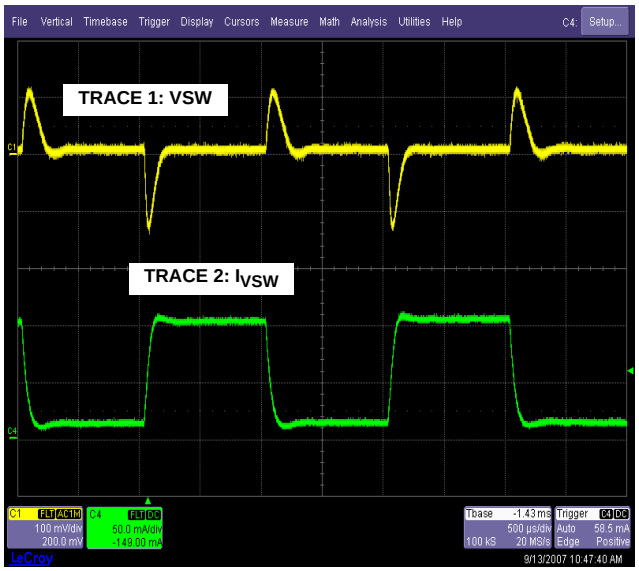


FIGURE 6. VSW TRANSIENT RESPONSE, 10mA TO 100mA STEP, VPWR = 18V, AUXIN = 15V, VSW = 12V

Figure 6 depicts the transient response of VSW during a 10mA to 100mA step load when AUXIN is set to 15V and VPWR is set to 18V.

VPWR

VPWR provides the source voltage for the IC and load until AUXIN is back biased. VSW is disabled and the IC operates in a standby (low power consumption) mode when UVLO is active.

If the application requires high currents or longer start-up times than the thermal protection allows, the device dissipation may be reduced by adding a resistor or resistors in series between the input voltage and VPWR. The dropping resistance must be selected such that VPWR remains above the UVLO threshold of VPWR and at least 6.2V greater than VSW under maximum load and minimum input voltage to maintain regulation.

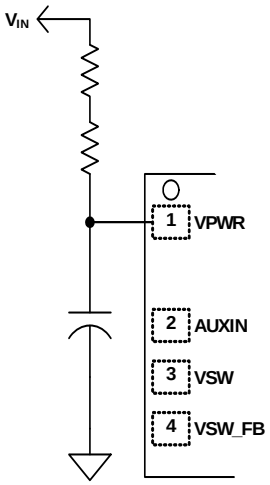


FIGURE 7. ADDING DROPPING RESISTORS TO VPWR

ENABLE, ENABLE_N

The ENABLE and ENABLE_N are complementary inputs used to turn VSW on and off. Both polarities of the enable function are provided to ease the interface to the application. The VSW may be enabled by either ENABLE or ENABLE_N, but both inputs must be logically false to disable the output. Each enable input has a nominal 100kΩ pull-up resistor to 5V.

TABLE 1. ENABLE, ENABLE_N TRUTH TABLE

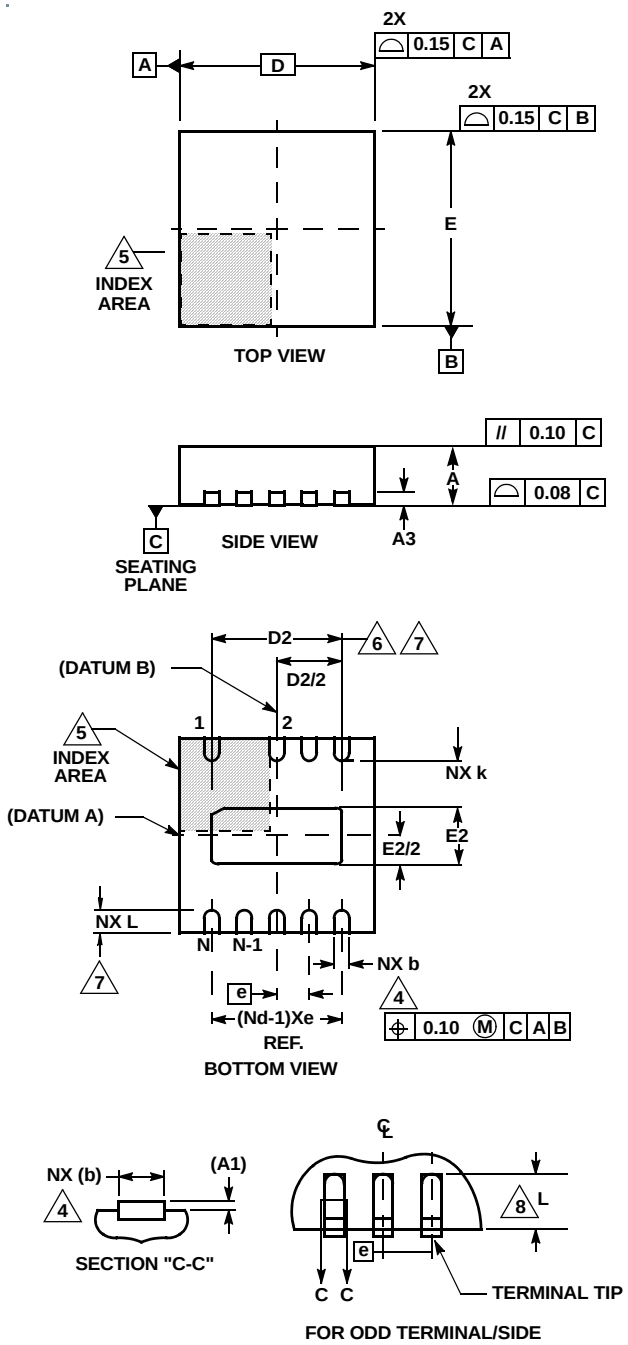
INPUTS		OUTPUT
ENABLE	ENABLE_N	VSW
0	0	ON
0	1	OFF
1	0	ON
1	1	ON

The inputs can accept voltages up to 6V maximum down to 0.3V below signal ground. Voltages beyond these limits, including transients, may cause permanent damage to the device. Care should be taken when connecting signal sources through long connections or if significant ground shift could occur between the source and the input. In such circumstances, it is recommended that appropriate clamping networks be used to prevent possible electrical overstress.

Over-Temperature Protection

The ISL6719 has an over-temperature shutdown mechanism to protect the device from excessive dissipation. The VSW shutdown occurs approximately at +150°C. The hysteresis is large so that the IC has sufficient time to operate at start-up loading levels without re-triggering the over-temperature protection.

Dual Flat No-Lead Plastic Package (DFN)



L9.3x3

9 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	4, 7
D		3.00 BSC		-
D2	1.85	2.00	2.10	6, 7
E		3.00 BSC		-
E2	0.80	0.95	1.05	6, 7
e		0.50 BSC		-
k	0.60	-	-	-
L	0.25	0.35	0.45	7
N		9		2

Rev. 0 3/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. All dimensions are in millimeters. Angles are in degrees.
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
7. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
8. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.

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