PAS6329 CMOS VGA DIGITAL IMAGE SENSOR

General Description

The PAS6329 is a highly integrated CMOS active-pixel image sensor that has output of 640 x 480 pixels. It embedded the new FinePixel™ sensor technology to perform the excellent image quality. PAS6329 outputs 8-bit YUV/YCrCb 4:2:2 or RGB565/555/444 data through a parallel data bus. It is available in CSP-22L package.

The PAS6329 can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register set, it performs on-chip frame rate adjustment, offset correction DAC and programmable gain control.

Features

- **Resolution: 640 x 480 pixels, 1/7" Lens**
- **Bayer-RGB color filter array**
- **Output format (parallel 8-bit):**
  - **YUV/YCrCb 4:2:2**
  - **RGB565/555/444**
- **I2C™ Interface**
- **Power dissipation: operating typical 25mA @ 2.8V (VGA YUV 30fps output, without loading), power-down typical 10uA @ 2.8V**
- **Automatic Background Compensation**
- **DSP function:**
  - **AEC & AGC**
  - **AWB**
  - **Gamma**
  - **Color matrix**
  - **Sharpness**
  - **De-noise**
  - **Color saturation**
  - **Defect compensation**
  - **Lens shading compensation**
  - **Decimation**
- **WOI & Sub-sampling**
- **Dummy line & pixel timing**
- **Output Hsync at Vsync**
- **Module size : 6.0mm * 6.0mm**

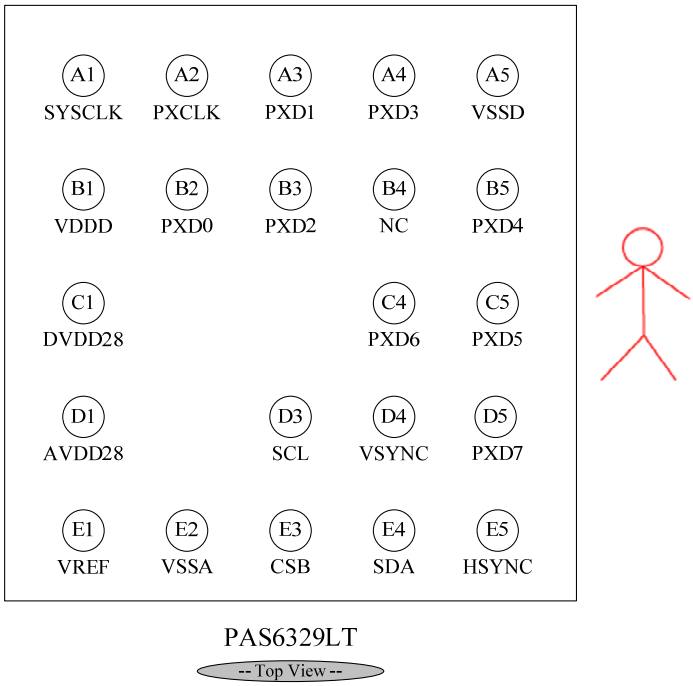
Key Specification

Resolution		**640 (H) x 480 (V)**
Pixel Size		**3.15um * 3.15um**
Array diagonal		**1/7" Lens**
Lens Chief Ray Angle		**25 degree**
Color filter		**RGB Bayer Pattern**
Power	**Analog**	**2.8V typical**
	I/O	**2.8V typical**
	Core	**1.8V typical**
Max. input clock		**52MHz**
Max. output clock		**26MHz**
Max. Frame rate		**30fps**
Scan Mode		**Progressive**
Exposure Time		**~ Frame time to Line time**
Sensitivity		**1500mV/Lux-Sec**
S/N Ratio		**41dB**
Dynamic range		**60dB**
Package		**CSP-22L**

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1. Pin Assignment



PAS6329LT

-- Top View --

Pin No.	Name	Type	Description
A1	SYSCLK	IN	External clock input
A2	PXCLK	OUT	Pixel clock output
A3	PXD1	OUT	Digital pixel data [1]
A4	PXD3	OUT	Digital pixel data [3]
A5	VSSD	GND	Digital ground
B1	VDDD	PWR	Digital core power, 1.8V
B2	PXD0	OUT	Digital pixel data [0], LSB
B3	PXD2	OUT	Digital pixel data [2]
B4	NC	- -	- -
B5	PXD4	OUT	Digital pixel data [4]
C1	DVDD28	PWR	I/O power, 2.8V typical
C4	PXD6	OUT	Digital pixel data [6]
C5	PXD5	OUT	Digital pixel data [5]
D1	AVDD28	PWR	Analog power, 2.8V typical
D3	SCL	IN	I2C clock input
D4	VSYNC	OUT	Vertical synchronization signal output
D5	PXD7	OUT	Digital pixel data [7], MSB
E1	VREF	Ref	Voltage reference
E2	VSSA	GND	Analog ground
E3	CSB	IN	Power down mode enable, active high
E4	SDA	I/O	I2C data
E5	HSYNC	OUT	Horizontal synchronization signal output

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2. Specifications

Absolute Maximum Ratings

Operating Temperature		-30℃ ~ 85℃
Stable Image Temperature		0℃ ~ 50℃
Ambient Storage Temperature		-40℃ ~ 125℃
Supply Voltage (with respect to ground)	V_{DDA}	4.5V
	V_{DDD}	3.0V
	V_{DDIO}	4.5V
All Input / Output Voltage (with respect to ground)		-0.3V to V_{DDIO} + 0.5V
Lead-free temperature, Surface-mount process		245℃
ESD rating, Human Body model		2000V

DC Electrical Characteristics (Ta = 0℃ ~ 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V_{DDA}	DC supply voltage – Analog	2.6	2.8	3.0	V
V_{DDD}	DC supply voltage – Digital core		1.8		V
V_{DDIO}	DC supply voltage – I/O	2.6	2.8	3.0	V
I_{DD}	Operating Current (VGA YUV 30fps / 2.8v)		25		mA
I_{PWDN}	Power Down Current (VGA YUV 30fps / 2.8v)		10		µA
Type : IN & I/O					
V_{IH}	Input Voltage HIGH	V_{DDIO} * 0.7			V
V_{IL}	Input Voltage LOW			V_{DDIO} * 0.3	V
Type : OUT & I/O					
V_{OH}	Output Voltage HIGH	V_{DDIO} * 0.9			V
V_{OL}	Output Voltage LOW			V_{DDIO} * 0.1	V

AC Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{sysclk}	System clock frequency		24		MHz
t_{sysclk_dc}	System clock duty cycle	45		55	%

Sensor Characteristics

Parameter	Typ.	Unit
Sensitivity	1500	mV/Lux-Sec
Signal to Noise Ratio	41	dB
Dynamic Range	60	dB

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3. I2C™ Bus

PAS6329 supports I2C bus transfer protocol and acts as slave device. The 7-bits unique slave address is "1000000" and supports receiving / transmitting speed as maximum 400KHz.

I2C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 2.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 2.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

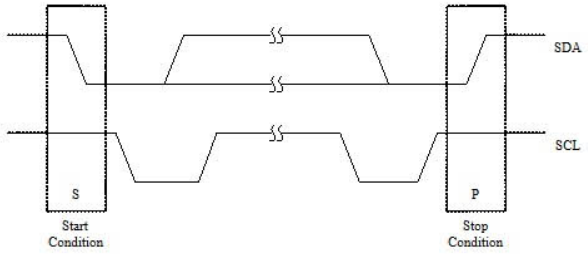


Figure 2.1 Start and Stop conditions

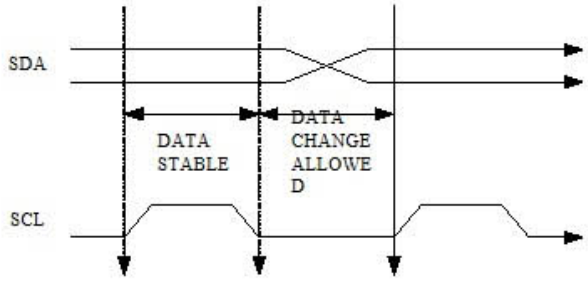


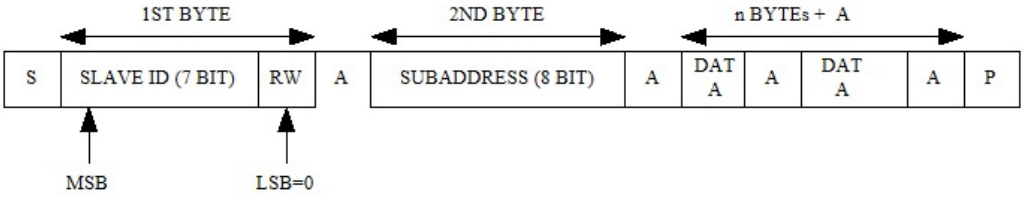
Figure 2.2 Valid Data

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Data Transfer Format

Master transmits data to salve (write cycle)

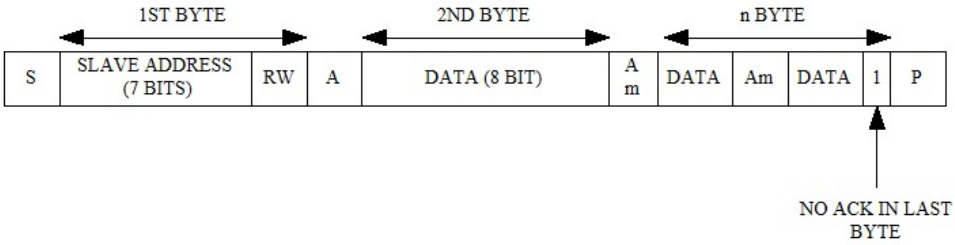
- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of PAS6329 internal control registers. (Please refer to PAS6329 register description)



During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (PAS6329) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the PAS6329 acknowledgment, the master places the 8 bits data on SDA line and transmit to PAS6329 control register (address was assigned by 2nd byte). After PAS6329 issues acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAS6329 sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside PAS6329 can be programming via this way.

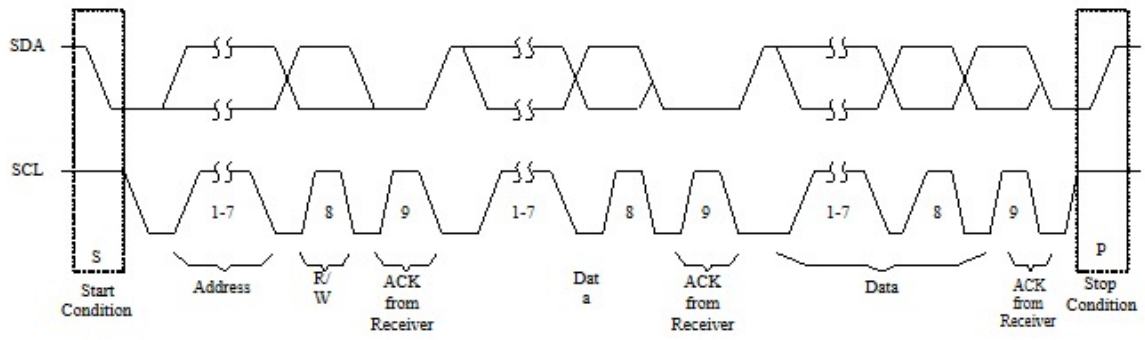
Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.



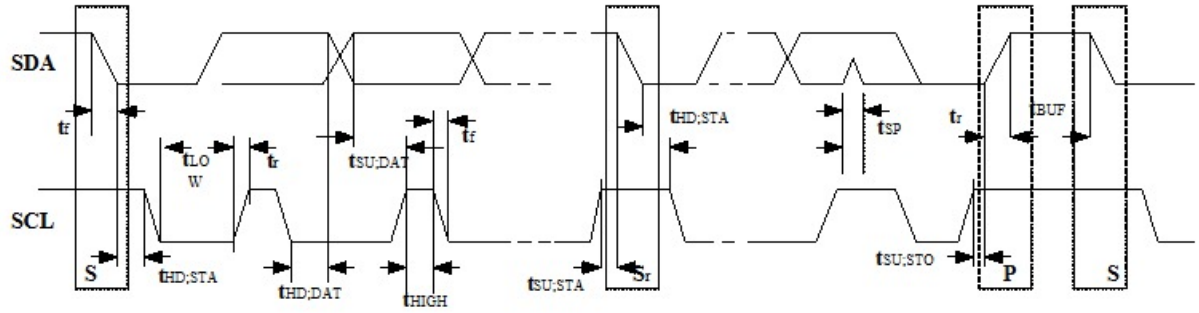
During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PAS6329. The 8 bits data was read from PAS6329 internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAS6329 place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PAS6329) must releases SDA line to master to generate STOP condition.

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I2C™ Bus Timing



I2C™ Bus Timing Specification

Parameter	Symbol	Standard Mode		Unit
		Min.	Max	
SCL clock frequency.	f_{scl}	10	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	µs
Low period of the SCL clock.	t_{LOW}	4.7	-	µs
High period of the SCL clock.	t_{HIGH}	0.75	-	µs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-	µs
Data hold time. For I2C-bus device.	$t_{HD;DAT}$	0	3.45	µs
Data set-up time.	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals.	t_r	30	N.D.	ns (notel)
Fall time of both SDA and SCL signals.	t_f	30	N.D.	ns (notel)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-	µs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	µs
Capacitive load for each bus line.	C_b	1	15	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-	V

Note : It depends on the “high” period time of SCL.

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4. Registers

Register Table

Bank	Address		Register Name	Bits	Default Value	Notes
	Hex	Dec				
0	0	0	PartID[15:8]	[7:0]	0x63	Part ID
0	1	1	PartID[7:0]	[7:0]	0x27	Part ID
0	2	2	VersionID[3:0]	[3:0]	0x00	VersionID
0	3	3	SubID[3:0]	[3:0]	0x0a	SubID
0	4	4	R_AE_stage_indoor_Sel	[0]	0x0	AE indoor stage select 0:11 , 1:12
0	8	8	R_ne_clamp_by8[7:0]	[7:0]	0x50	ne upper bound (clamp to R_ne_clamp_by8*8)
0	9	9	R_ISP_TestValueLo[7:0]	[7:0]	0x00	ISP test mode low data value
0	A	10	R_ISP_TestValueHi[7:0]	[7:0]	0xff	ISP test mode high data value
0	C	12	R_ISP_TestMode[4:0]	[4:0]	0x00	ISP test mode data generation Bit[4] : defect test pixel insertion Bit[3:0] : 0:no test; 1:white; 2:black; 3:red; 4:green; 5:blue; 6:vertical&horizontal color bar; 7:random data; 8:vertical gray bar; 9:horizontal gray bar; 12-15: motion test;
0	F	15	R_AWB_Window_X[7:0]	[7:0]	0x90	AWB window width (by4)
0	11	17	R_AWB_Window_Y[7:0]	[7:0]	0x64	AWB window height (by4)
0	13	19	R_lpf_min[7:0]	[7:0]	0xf6	Lpf minimum value for AE
0	14	20	R_ny_min[3:0]	[7:4]	0x21	Ny minimum value for AE
			R_lpf_min[10:8]	[2:0]		Lpf minimum value for AE
0	19	25	R_AWB_DGnR_LB_by2[7:0]	[7:0]	0x30	AWB digital gain lower bound for R
0	1A	26	R_AWB_DGnR_UB_by2[7:0]	[7:0]	0x49	AWB digital gain upper bound for B
0	1B	27	R_AWB_DGnB_LB_by2[7:0]	[7:0]	0x3a	AWB digital gain lower bound for B
0	1C	28	R_AWB_DGnB_UB_by2[7:0]	[7:0]	0x78	AWB digital gain upper bound for R
0	1D	29	R_Y8bit_Saturate_Thd[7:0]	[7:0]	0xfe	Ycap_Very_Saturate =(Ycap8bit[7:0] >= R_Y8bit_Saturate_Thd);
0	1E	30	R_Y8bit_Bright_Thd[7:0]	[7:0]	0xc8	Ycap_Very_bright_2X =(Ycap8bit[7:0] >= R_Y8bit_Bright_Thd);
0	29	41	R_ISP_Gamma_EnH	[0]	0x01	ISP gamma correction enable
0	2A	42	R_ISP_Y00	[7:0]	0x0d	ISP Gamma Y0
0	2B	43	R_ISP_Y01	[7:0]	0x19	ISP Gamma Y1
0	2C	44	R_ISP_Y02	[7:0]	0x2f	ISP Gamma Y2
0	2D	45	R_ISP_Y03	[7:0]	0x53	ISP Gamma Y3
0	2E	46	R_ISP_Y04	[7:0]	0x62	ISP Gamma Y4
0	2F	47	R_ISP_Y05	[7:0]	0x6f	ISP Gamma Y5
0	30	48	R_ISP_Y06	[7:0]	0x7c	ISP Gamma Y6
0	31	49	R_ISP_Y07	[7:0]	0x87	ISP Gamma Y7
0	32	50	R_ISP_Y08	[7:0]	0x9a	ISP Gamma Y8
0	33	51	R_ISP_Y09	[7:0]	0xaa	ISP Gamma Y9
0	34	52	R_ISP_Y10	[7:0]	0xb8	ISP Gamma Y10
0	35	53	R_ISP_Y11	[7:0]	0xc5	ISP Gamma Y11
0	36	54	R_ISP_Y12	[7:0]	0xd8	ISP Gamma Y12
0	37	55	R_ISP_Y13	[7:0]	0xe8	ISP Gamma Y13
0	38	56	R_ISP_Y14	[7:0]	0xf5	ISP Gamma Y14
0	3A	58	R_Ycap_Very_dark_16X_steps[5:0]	[5:0]	0x20	Step change when Ycap < Ytar/16
0	3B	59	R_Ycap_Very_dark_8X_steps[5:0]	[5:0]	0x18	Step change when Ycap < Ytar/8
0	3C	60	R_Ycap_Very_dark_4X_steps[5:0]	[5:0]	0x10	Step change when Ycap < Ytar/4
0	3D	61	R_Ycap_Very_dark_2X_steps[5:0]	[5:0]	0x08	Step change when Ycap < Ytar/2
0	3E	62	R_AE_HIST_BackLight[2:0]	[2:0]	0x00	AE histogram backlight, 0~7

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0	3F	63	R_AE_HIST_Step_V[4:0]	[4:0]	0x0C	Distance of two vertical AE histgram sample points
0	40	64	R_AE_HIST_HStart[7:0]	[7:0]	0x58	Horizontal start point location of AE histgram sample points
0	41	65	R_AE_HIST_VStart[7:0]	[7:0]	0x44	Vertical start point location of AE histgram sample points
0	42	66	R_AE_HIST_LCS_OFFSET[2:0]	[7:5]	0x02	Reserved
			R_AE_HIST_PCS_OFFSET[4:0]	[4:0]	0x01	Reserved
0	43	67	R_AE_LumaEstimation_mode	[4]	0x00	0= histogram based, 1=block-based
			R_AE_Hist2Avg_POWER_SEL	[0]	0x00	0=8, 1=9
0	46	70	R_AG_delay_EnH	[0]	0x10	AG gain delay for one frame
			R_DG_delay_EnH	[1]		AG DGn delay for one frame
			R_AWB_DGn_delay_EnH	[4]		AWB gain delay for one frame
0	47	71	R_AWB_ShowActivePix	[7]	0x34	AWB test mode to show active region
			R_AWB_CountThd	[6:4]		AWB pixel in region count threshold 0: 0; 1: AWB_Window_PixCnt>>8; 2: AWB_Window_PixCnt>>7; 3: AWB_Window_PixCnt>>6; 4: AWB_Window_PixCnt>>5; 5: AWB_Window_PixCnt>>4; 6: AWB_Window_PixCnt>>3; 7: AWB_Window_PixCnt>>2;
			R_AWB_Speed	[1:0]		AWB adjust speed. The more, the slower 0: 1 x; 1: 1/2 x; 2: 1/4 x; 3: 1/8 x;
0	49	73	R_AWB_SumRatio_B	[7:0]	0x80	AWB B sum ratio = 128/X
0	4A	74	R_AWB_SumRatio_R	[7:0]	0x80	AWB R sum ratio = 128/X
0	4B	75	R_AWB_CThdL	[7:0]	0x42	AWB Cthd LB
0	4C	76	R_AWB_CThdH	[7:0]	0x05	AWB Cthd HB
0	4D	77	R_AWB_CbThdL[7:0]	[7:0]	0x64	AWB region test Cb Low threshold -128 ~ +127 (2's complement)
0	4E	78	R_AWB_CrThdL[7:0]	[7:0]	0x87	AWB region test Cr Low threshold -128 ~ +127 (2's complement)
0	4F	79	R_AWB_CbCrThdL[7:0]	[7:0]	0x00	AWB region test Cb+Cr Low threshold -128 ~ +127 (2's complement)
0	50	80	R_AWB_CbThdH[7:0]	[7:0]	0x75	AWB region test Cb High threshold -128 ~ +127 (2's complement)
0	51	81	R_AWB_CrThdH[7:0]	[7:0]	0x96	AWB region test Cr High threshold -128 ~ +127 (2's complement)
0	52	82	R_AWB_CbCrThdH[7:0]	[7:0]	0xff	AWB region test Cb+Cr High threshold -128 ~ +127 (2's complement)
0	53	83	R_Ylow	[7:0]	0x1e	Low bound of “light-pixel”Y in AWB
0	54	84	R_Yhigh	[7:0]	0xff	High bound of “light-pixel”Y in AWB
0	56	86	R_AE_stage_YlowLL_thd[4:0]	[4:0]	0x12	(AE stage >= thd) --> use AWB Lockrange_LL
0	57	87	R_AWB_LockRange__In[3:0]	[3:0]	0x02	AWB Lockrange In (NL)
0	58	88	R_AWB_LockRange_Out[5:0]	[5:0]	0x04	AWB Lockrange Out (NL)
0	59	89	R_AWB_LockRange__In_LL[5:0]	[5:0]	0x04	AWB Lockrange In (LL)
0	5A	90	R_AWB_LockRange_Out_LL[5:0]	[5:0]	0x06	AWB Lockrange Out (LL)
0	5B	91	R_AWB_MinStep_th[2:0]	[2:0]	0x00	AWB mininum step size 0:1, 1:2, 2:4, 3:8, 4:16, 5:32, 6:64, 7:128
0	5C	92	R_AE_HIST_Step_H[4:0]	[4:0]	0x0C	Distance of two horizontal AE histgram sample points
0	5F	95	R_AE_LockRange_Out_LB[7:0]	[7:0]	0x14	AE Lockrange Out LB
0	63	99	R_ISP_EnH	[5]	0x20	ISP enable
			ISP_EnH_update	[4]		Flag: ISP enable is sync by vsync
0	64	100	R_AE_LockRange_Out_UB[7:0]	[7:0]	0x14	AE Lockrange Out UB
0	65	101	R_AE_LockRange__In[3:0]	[7:4]	0x41	AE Lockrange In
0	66	102	R_AE_EnH	[4]	0x00	AE enable

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			R_TGWr_buf_EnH	[1]	0x01	Enable I2C buffer for TG when AE on
			R_freq_60	[0]	0x01	Set de-flicker frequency 0/1: 50/60Hz
0	67	103	R_SysClk_freq[7:0]	[7:0]	0x97	Input_frequency/2048
0	68	104	R_SysClk_freq[14:8]	[6:0]	0x31	Input_frequency/2048
0	6B	107	R_AE_minStage[4:0]	[4:0]	0x07	Minimum AE stage
0	6C	108	R_AE_maxStage[4:0]	[4:0]	0x1c	Maximum AE stage (AE_maxStage<=31)
0	6D	109	R_AG_stage_UB	[7:0]	0x3f	AG_stage upper bound at max AE_stage
0	6F	111	R_Ytar8bit	[7:0]	0x82	0~255, Target luminance of AE
0	70	112	R_AE_wait_state	[2:0]	0x00	Frame wait-state for AE adjust
			R_AWB_wait_state	[6:4]	0x00	Frame wait-state for AWB adjust
0	72	114	R_AWB_EnH	[0]	0x00	Auto-white balance enable
			R_AWB_Gain_rst	[4]	0x01	AWB gain reset
0	73	115	R_AWB_BalGain_R[7:0]	[7:0]	0xbe	AWB Balance gain R
0	74	116	R_AWB_BalGain_B[7:0]	[7:0]	0x9c	AWB Balance gain B
0	76	118	R_AWB_HCT_WeightThd[7:0]	[7:0]	0x5e	Reserved
0	79	121	R_ISP_HOffset[7:0]	[7:0]	0x16	ISP Hsize Offset
0	7B	123	R_ISP_VOffset[7:0]	[7:0]	0x04	ISP Vsize Offset
0	81	129	R_AE_Speed	[5:4]	0x00	AE speed, the more, the slower 0: 1 x; 1: 1/2 x; 2: 1/4 x; 3: 1/8 x;
			R_AE_MinStep_th[1:0]	[1:0]	0x00	AE Minimun step threshold select 0: 16; 1:32; 2:64; 3:128;
0	84	132	R_AE_StageChg_Saturate	[5:0]	0x20	AE StageChg when (Average Lumiance > saturate threshold)
0	86	134	R_AE_StageChg_Bright2X	[5:0]	0x10	AE StageChg when (Average Lumiance > 2*Target Lumiance)
0	8E	142	R_AE_chg_wait	[2:0]	0x00	AE wait state when AE change Texp
0	8F	143	R_ImgEffect_c0	[7:0]	0x00	Image Effect parameter 0 (ISP_UpdateFlag=1, update)
0	90	144	R_ImgEffect_c1	[7:0]	0x00	Image Effect parameter 1 (ISP_UpdateFlag=1, update)
0	91	145	R_ImgEffect_c2	[7:0]	0x00	Image Effect parameter 2 (ISP_UpdateFlag=1, update)
0	92	146	R_ImgEffect_c3	[7:0]	0x00	Image Effect parameter 3 (ISP_UpdateFlag=1, update)
0	93	147	R_ImgEffectMode	[3:0]	0x00	Image Effect mode 0: monochrome; 1: negative; 2: x-ray; 3: Sepia / Cold / Warm / Sunset; 6: Solarize; 10: Pixelate; (ISP_UpdateFlag=1, update)
0	94	148	R_ISP_ImgEffect_En	[0]	0x00	Image effect enable (ISP_UpdateFlag=1, update)
0	95	149	R_SENCLK_delay[3:0]	[3:0]	0x00	Senclk output deley select
			R_SENCLK_Inv	[4]	0x00	Sensor clock output inversion
0	97	151	R_Shading_EnH	[4]	0x01	Lens shading enable
0	99	153	R_OffsetX_R[6:0]	[6:0]	0x00	Horizontal distances between shading center and sensor array center of R-channel, MSB:sign bit, -63~+63
0	9A	154	R_OffsetY_R[6:0]	[6:0]	0x00	Vertical distances between shading center and sensor array center of R-channel, MSB:sign bit, -63~+63
0	9B	155	R_OffsetX_G[6:0]	[6:0]	0x00	Horizontal distances between shading center and sensor array center of G-channel, MSB:sign bit, -63~+63
0	9C	156	R_OffsetY_G[6:0]	[6:0]	0x00	Vertical distances between shading center and sensor array center of G-channel, MSB:sign bit, -63~+63
0	9D	157	R_OffsetX_B[6:0]	[6:0]	0x00	Horizontal distances between shading center and sensor array center of B-channel, MSB:sign bit, -63~+63
0	9E	158	R_OffsetY_B[6:0]	[6:0]	0x00	Vertical distances between shading center and sensor array center of B-channel, MSB:sign bit, -63~+63

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0	9F	159	R_LSC_R1[6:0]	[6:0]	0x00	Quartic parameter of R-channel
0	A0	160	R_LSC_G1[6:0]	[6:0]	0x00	Quartic parameter of G-channel
0	A1	161	R_LSC_B1[6:0]	[6:0]	0x00	Quartic parameter of B-channel
0	A2	162	R_LSC_R2[6:0]	[6:0]	0x50	Square parameter of R-channel
0	A3	163	R_LSC_G2[6:0]	[6:0]	0x50	Square parameter of G-channel
0	A4	164	R_LSC_B2[6:0]	[6:0]	0x50	Square parameter of B-channel
0	A5	165	R_LSFT_1[2:0]	[2:0]	0x04	Reserved
0	A6	166	R_LSFT_2[1:0]	[1:0]	0x00	Reserved
0	A7	167	R_LSFT_3[2:0]	[2:0]	0x02	Reserved
0	AE	174	AWB_Valid__PixCnt_vs[15:8]	[7:0]	0x00	AWB valid pixel cnt (by8)
0	AF	175	AWB_Valid__PixCnt_vs[7:0]	[7:0]	0x00	AWB valid pixel cnt (by8)
0	B0	176	Total_Gain[14:8]	[6:0]	0x00	Total gain (FG * GG, 7.8 format)
0	B1	177	Total_Gain[7:0]	[7:0]	0x00	Total gain (FG * GG, 7.8 format)
0	B2	178	AWB_Sum_R[15:8]	[7:0]	0x00	AWB Sum R
0	B3	179	AWB_Sum_R[7:0]	[7:0]	0x00	AWB Sum R
0	B4	180	AWB_Sum_G[15:8]	[7:0]	0x00	AWB Sum G
0	B5	181	AWB_Sum_G[7:0]	[7:0]	0x00	AWB Sum G
0	B6	182	AWB_Sum_B[15:8]	[7:0]	0x00	AWB Sum B
0	B7	183	AWB_Sum_B[7:0]	[7:0]	0x00	AWB Sum B
0	B8	184	LineCnt_Sensor[7:0]	[7:0]	0x00	Line counter
0	B9	185	LineCnt_Sensor[9:8]	[1:0]	0x00	Line counter
			FrameCnt[2:0]	[6:4]	0x00	Frame counter (0~7)
0	BA	186	Ycap8bit	[7:0]	0x00	Y sum report
0	BB	187	AWB_EnH_vs	[6]	0x00	AWB enable sync by vsync
0	BB	187	AE_EnH_vs	[7]	0x00	AE enable sync by vysnc
0	BC	188	AG_stage[7:0]	[7:0]	0x00	AG Stage
0	BD	189	AE_stage[4:0]	[4:0]	0x00	AE Stage
0	BE	190	Reg_lpf[7:0]	[7:0]	0x00	Line Per Frame Register
0	BF	191	Reg_lpf[13:8]	[5:0]	0x00	Line Per Frame Register
0	C0	192	Reg_ny [7:0]	[7:0]	0x00	Ny Register
0	C1	193	Reg_ny [10:8]	[2:0]	0x00	Ny Register
0	C2	194	Reg_ne[7:0]	[7:0]	0x00	Ne Register
0	C3	195	Reg_ne[12:8]	[4:0]	0x00	Ne Register
0	CC	204	DGn_R_vs[7:0]	[7:0]	0x00	R Digital Gain sync by vsync
0	CD	205	DGn_R_vs[8]	[0]	0x00	R Digital Gain sync by vsync
0	CE	206	DGn_G_vs[7:0]	[7:0]	0x00	G Digital Gain sync by vsync
0	CF	207	DGn_G_vs[8]	[0]	0x00	G Digital Gain sync by vsync
0	D0	208	DGn_B_vs[7:0]	[7:0]	0x00	B Digital Gain sync by vsync
0	D1	209	DGn_B_vs[8]	[0]	0x00	B Digital Gain sync by vsync
0	D4	212	reg_FG_stage_6329[7:0]	[7:0]	0x00	AE computed Front gain
0	D5	213	reg_cgh_6329[1:0]	[1:0]	0x00	AE computed CGH
			reg_DG_6329[3:0]	[7:4]	0x00	AE computed DG
0	DE	222	AE_Already_Locked_vs	[0]	0x00	1=locked, 0=not locked
0	E0	224	R_ISP_HSize[7:0]	[7:0]	0x80	ISP output Horizontal size, (before skip function)
0	E1	225	R_ISP_HSize[9:8]	[1:0]	0x02	ISP output Horizontal size, (before skip function)
0	E2	226	R_ISP_VSize[7:0]	[7:0]	0xe0	ISP output Vertical size, (before skip function)
0	E3	227	R_ISP_Vsize[9:8]	[1:0]	0x01	ISP output Vertical size, (before skip function)
0	E6	230	R_ISP_FastUpdate	[0]	0x00	ISP Fast Update mode
0	EB	235	R_SwTristate	[0]	0x0	Sw Tristate
0	ED	237	ISP_Update	[0]	0x00	ISP_UpdateFlag
			ISP_FrameSkip	[4]	0x00	(ISP_UpdateFlag=1, update)
0	EE	238	RegBank_SWRstn	[0]	0x00	SW reset for RegBank0, RegBank1
			Sensor_IF_SWRstn	[1]	0x00	SW reset for Sensor interface
			ISP_Top1_SWRstn	[2]	0x00	SW reset for ISP_Top1
			ISP_Top2_SWRstn	[3]	0x00	SW reset for ISP_Top2
			AE_AWB_SWRstn	[4]	0x00	SW reset for AE_AWB

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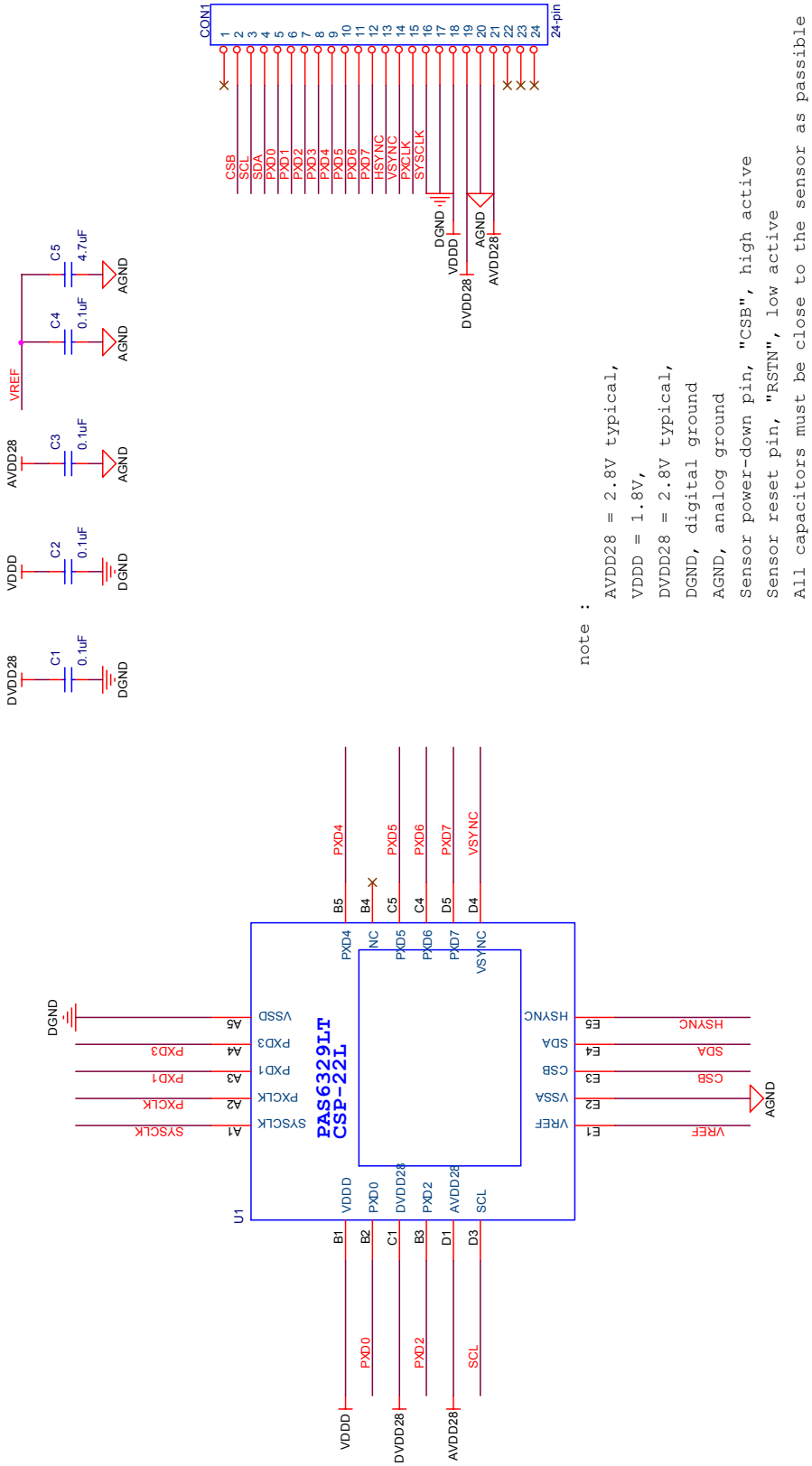
			Other_SWRstn	[5]	0x00	SW reset for Others
1	EF	239	R_RegBankSel	[2:0]	0x00	Register Bank Select 0: ISP1 Register Bank (default); 1: Sensor Register Bank; 2: ISP2 Register Bank;
2	0	0	ISP2_Update	[0]	0x00	ISP2_UpdateFlag
2	B	11	R_AUTO_Contrast_EnH	[4]	0x00	Auto contrast enable
			R_AUTO_Contrast_Strength	[3:0]	0x07	Contrast strength, 0~15
2	C	12	R_AUTO_Contrast_UB	[7:0]	0x50	Contrast strength UB
2	D	13	R_AUTO_Contrast_LB	[7:0]	0x40	Contrast strength LB
2	18	24	R_Curve_Y3[7:0]	[7:0]	0x6f	ISP tone curve Y3: Before Histogram, real value=R_Curve_Y3[7:0]<<2
2	19	25	R_Curve_Y6[7:0]	[7:0]	0xa5	ISP tone curve Y6: Before Histogram, real value=R_Curve_Y6[7:0]<<2
2	26	38	R_DefectThd_NL[4:0]	[4:0]	0x0c	Defect test threshold @ Normal Light
2	27	39	R_DefectThd_LL[4:0]	[4:0]	0x0c	Defect test threshold @ Low Light
2	2A	42	R_FlatRatio[3:0]	[3:0]	0x08	ISP edge enhancement flat ratio
			R_Flat_En	[6]	0x01	ISP edge enhancement flat enable
			R_ISP_Edge_En0	[7]	0x01	ISP edge enhancement enable
2	2C	44	R_Edge_UB[7:0]	[7:0]	0x20	ISP edge enhancement value upper bound
2	2D	45	R_Edge_LB[7:0]	[7:0]	0x19	ISP edge enhancement value lower bound
2	2E	46	R_EdgeThdLB[7:0]	[7:0]	0x10	ISP edgethd LB
2	2F	47	R_AE_stage_LL[4:0]	[4:0]	0x13	AE_stage > R_AE_stage_LL =>Low Light
2	30	48	R_AE_stage_NL[4:0]	[4:0]	0x11	AE_stage < R_AE_stage_NL =>Normal Light
2	35	53	R_Gamma_Strength_NL[4:0]	[4:0]	0x10	Gamma Strength @ NL
2	36	54	R_Gamma_Strength_Delta[4:0]	[4:0]	0x08	Increment when AE/AG stage change
			R_Manual_Gamma_Strength	[5]	0x00	Fix setting to NL
2	37	55	R_Gamma_Strength_LL[4:0]	[4:0]	0x08	Gamma Strength @ LL
2	3E	62	R_CCMbSign[5:0]	[5:0]	0x33	CCM matrix coefficient
2	3F	63	R_CCMb0_0[7:0]	[7:0]	0x26	CCM matrix coefficient
2	40	64	R_CCMb0_1[7:0]	[7:0]	0x4b	CCM matrix coefficient
2	41	65	R_CCMb0_2[7:0]	[7:0]	0x0f	CCM matrix coefficient
2	42	66	R_CCMb1_0[7:0]	[7:0]	0x18	CCM matrix coefficient
2	43	67	R_CCMb1_1[7:0]	[7:0]	0x52	CCM matrix coefficient
2	44	68	R_CCMb1_2[7:0]	[7:0]	0x6a	CCM matrix coefficient
2	45	69	R_CCMb2_0[7:0]	[7:0]	0x6a	CCM matrix coefficient
2	46	70	R_CCMb2_1[7:0]	[7:0]	0x68	CCM matrix coefficient
2	47	71	R_CCMb2_2[7:0]	[7:0]	0x02	CCM matrix coefficient
2	55	85	R_Manual_EdgeRatio	[4]	0x00	Fix setting to normal light
2	56	86	R_EdgeRatio_Delta[4:0]	[4:0]	0x08	Increment when AE/AG state change
2	57	87	R_EdgeRatio_LL[4:0]	[4:0]	0x04	Edge ratio @Low Light
2	58	88	R_EdgeRatio_NL[4:0]	[4:0]	0x0a	Edge ratio @Normal Light
2	59	89	R_Manual_Edge_th	[4]	0x00	Fix setting to normal light
2	5A	90	R_Edge_th_Delta[4:0]	[4:0]	0x08	Increment when AE/AG state change
2	5B	91	R_Edge_th_LL[7:0]	[7:0]	0x0a	Edge threshold @ Low Light
2	5C	92	R_Edge_th_NL[7:0]	[7:0]	0x08	Edge threshold @ Normal Light
2	5D	93	R_Saturation_Fast	[0]	0x01	1: fast change, +-Delta; 0: slow change, +-(1/Delta);
			R_Saturation_2X	[1]	0x00	Color Saturation double
			R_Manual_Saturation	[4]	0x00	Fix setting to normal light
2	5E	94	R_Saturation_Delta[4:0]	[4:0]	0x01	Increment when AE/AG state change
2	5F	95	R_Saturation_LL[4:0]	[4:0]	0x0b	Color Saturation @ Low Light
2	60	96	R_Saturation_NL[4:0]	[4:0]	0x16	Color Saturation @ Normal Light
2	61	97	R_Shading_CP_R_Fast	[0]	0x00	1: fast change, +-Delta; 0: slow change, +-(1/Delta);
			R_Manual_Shading_CP	[4]	0x00	Manual Shading percentage

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2	62	98	R_Shading_CP_R_Delta[4:0]	[4:0]	0x02	Increment when AE/AG state change
2	63	99	R_Shading_CP_R_NL[3:0]	[3:0]	0x0f	Shading compensation percentage @Normal Light
			R_Shading_CP_R_LL[3:0]	[7:4]	0x00	Shading compensation percentage @Low Light
2	64	100	R_Contrast_En	[0]	0x01	Contrast Enable
2	65	101	R_Contrast_Str[7:0]	[7:0]	0x40	Contrast Strength (ISP2_UpdateFlag=1, update)
2	66	102	R_Contrast_CP[7:0]	[7:0]	0x82	Contrast CP (ISP2_UpdateFlag=1, update)
2	69	105	R_Brightness_LL[7:0]	[7:0]	0x00	Brightness @ Low Light
2	6A	106	R_Brightness_NL[7:0]	[7:0]	0x00	Brightness @ Normal Light
2	9B	155	R_ISP_WOI_HSize[9:8]	[1:0]	0x02	(ISP2_UpdateFlag=1, update)
2	9C	156	R_ISP_WOI_HSize[7:0]	[7:0]	0x80	(ISP2_UpdateFlag=1, update)
2	9D	157	R_ISP_WOI_VSize[9:8]	[1:0]	0x01	(ISP2_UpdateFlag=1, update)
2	9E	158	R_ISP_WOI_VSize[7:0]	[7:0]	0xe0	(ISP2_UpdateFlag=1, update)
2	9F	159	R_ISP_WOI_HOffset[9:8]	[1:0]	0x00	(ISP2_UpdateFlag=1, update)
2	A0	160	R_ISP_WOI_HOffset[7:0]	[7:0]	0x00	(ISP2_UpdateFlag=1, update)
2	A1	161	R_ISP_WOI_VOffset[9:8]	[1:0]	0x00	(ISP2_UpdateFlag=1, update)
2	A2	162	R_ISP_WOI_VOffset[7:0]	[7:0]	0x00	(ISP2_UpdateFlag=1, update)
2	A4	164	R_ScalingFIFO_Out_NP[4:0]	[4:0]	0x02	(ISP2_UpdateFlag=1, update)
2	B2	178	R_EncDecimationNo_X[3:0]	[3:0]	0x00	ISP decimation no in X-direction (ISP_Zoom_UpdateFlag=1, update)
			R_EncDecimationNo_Y[3:0]	[7:4]	0x00	ISP decimation no in Y-direction (ISP_Zoom_UpdateFlag=1, update)
2	BF	191	R_UV_Swap	[1]	0x00	U V Swap
			R_YC_Swap	[2]	0x01	Y C Swap
2	C0	192	R_RGB565_mode[3:0]	[3:0]	0x00	RGB565_mode
			R_Format_Sel	[5:4]	0x00	Output Data format select 0:YUV; 1:RGB565; 2:RGB555; 3:RGB444; (ISP2_UpdateFlag=1, update)
2	C1	193	R_Vsync_INV	[0]	0x01	Vsync inverse
			R_Hsync_INV	[1]	0x01	Hsync inverse
			R_Pxclk_INV	[2]	0x00	Pxclk inverse
			R_Pxclk_Gated_InHVSync	[3]	0x00	Gate PXCLK in hsync/vsync
			R_SenVsync_En	[4]	0x00	Reserved
			R_HsyncInVsync	[5]	0x00	hsync toggle when vsync high
2	C2	194	R_PxclkO_dly	[6:4]	0x00	Pxclk Delay Cell Select
			R_HsyncO_dly	[2:0]	0x00	Hsync Delay Cell Select

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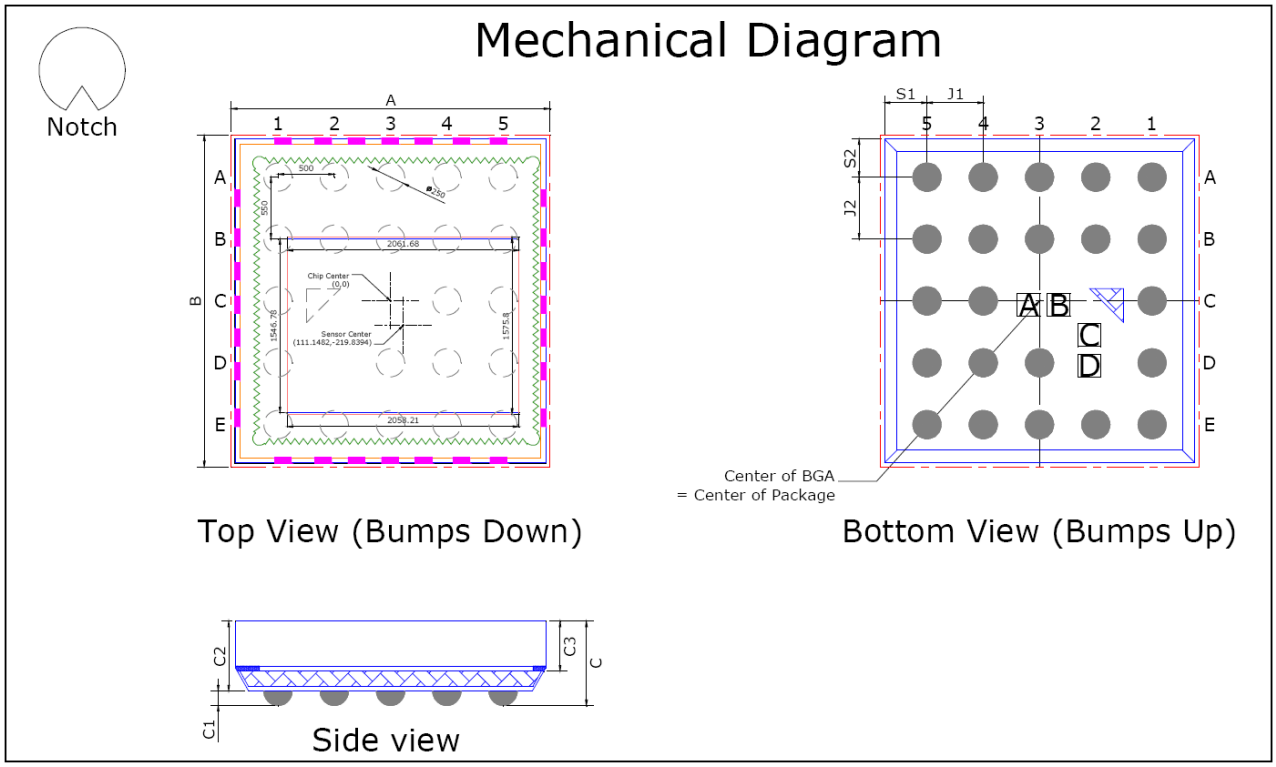
5. Reference Circuit Schematic



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6. Package Information

	Symbol	Nominal	Min.	Max.
			µm	
Package Body Dimension X	A	2759	2734	2784
Package Body Dimension Y	B	2878.8	2853.8	2903.8
Package Height	C	750	690	810
Ball Height	C1	130	100	160
Package Body Thickness	C2	620	575	665
Thickness of Glass surface to wafer	C3	445	425	465
Ball Diameter	D	250	220	280
Total Pin Count	N	22		
Pin Count X axis	N1	5		
Pin Count Y axis	N2	5		
Pins Pitch X axis	J1	500		
Pins Pitch Y axis	J2	550		
Edge to Pin Center Distance along X	S1	379.5	349.5	409.5
Edge to Pin Center Distance along Y	S2	339.4	309.4	369.4



*Note

The formation of image is the result formed by package Top view(A1 : left-up) and general Lens(invert and mirror the image).

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