TS5A4597
SINGLE-CHANNEL 8-Ω SPST ANALOG SWITCH

SCDS182 − FEBRUARY 2005

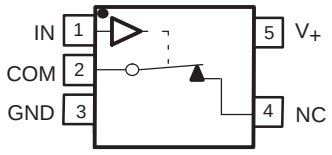
Description

The TS5A4597 is a single-pole single-throw (SPST) analog switch that is designed to operate from 2 V to 5.5 V. This device can handle both digital and analog signals, and signals up to V_+ can be transmitted in either direction.

Applications

- **Sample-and-Hold Circuits**
- **Battery-Powered Equipment (Cellular Phones, PDAs)**
- **Audio and Video Signal Routing**
- **Communication Circuits**
- **PCMCIA Cards**

SOT-23 OR SC-70 PACKAGE (TOP VIEW)



FUNCTION TABLE

IN	NC TO COM, COM TO NC
L	ON
H	OFF

Features

- **Low ON-State Resistance (8 Ω)**
- **ON-State Resistance Flatness (1.5 Ω)**
- **Control Inputs Are 5.5-V Tolerant**
- **Low Charge Injection (5 pC Max)**
- **450-MHz −3-dB Bandwidth at 25°C**
- **Low Total Harmonic Distortion (THD) (0.04%)**
- **2-V to 5.5-V Single-Supply Operation**
- **Specified at 5-V and 3.3-V Nodes**
- **−85-dB OFF Isolation at 1 MHz**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **0.5-nA Max OFF Leakage**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **TTL/CMOS-Logic Compatible**

Summary of Characteristics

V_+ = 5 V, T_A = 25°C

Configuration	Single Pole Single Throw (SPST)
Number of channels	1
ON-state resistance (r_{on})	8 Ω
ON-state resistance flatness ($r_{on(flat)}$)	1.5 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	17 ns/14 ns
Charge injection (Q_C)	5 pC
Bandwidth (BW)	450 MHz
OFF isolation (O_{ISO})	−85 dB at 1 MHz
Total harmonic distortion (THD)	0.04%
Leakage current ($I_{COM(OFF)}/I_{NC(OFF)}$)	±0.5 nA
Power-supply current (I_+)	0.25 μA
Package option	5-pin SOT-23 or SC-70

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
−40°C to 85°C	SOT (SOT-23) − DBV	Tape and reel	TS5A4597DBVR	JSD_
	SOT (SC−70) − DCK	Tape and reel	TS5A4597DCKR	JV_

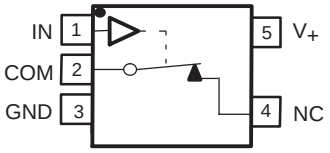
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

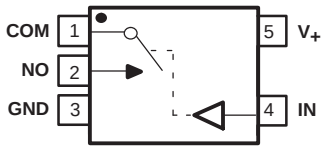
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Pin Configurations

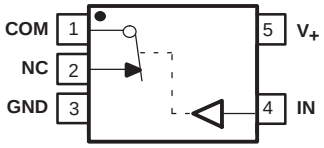


TS5A4597

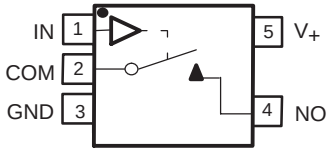
Available in Other Pin Configurations



TS5A4594



TS5A4595



TS5A4596

Absolute Minimum and Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		−0.3	6	V
V_{NC} V_{COM}	Analog voltage range(3)(4)		−0.3	V_+ + 0.3	V
I_K	Analog port diode current	V_{NC}, V_{COM} < 0	−50		mA
I_{NC} I_{COM}	On-state switch current	V_{NC}, V_{COM} = 0 to V_+	−20	20	mA
V_I	Digital input voltage range(3)(4)		−0.3	6	V
I_{IK}	Digital input clamp current	V_I < 0	−50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		−100		mA
θ_{JA}	Package thermal impedance(5)	DBV package		206	°C/W
		DCK package		252	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 5-V Supply(1)

V_+ = 4.5 V to 5.5 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	V_{NC} = 3.5 V, I_{COM} = 10 mA,	Switch ON, See Figure 13	25°C	4.5 V		5	8	Ω
				Full				10	
ON-state resistance flatness	$r_{on(flat)}$	V_{NC} = 1.5 V, 2.5 V, 3.5 V, I_{COM} = 10 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.5	1.5	Ω
				Full				2	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 4.5 V, or V_{NC} = 4.5 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	−0.5	0.01	0.5	nA
				Full		−5		5	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 4.5 V, or V_{COM} = 4.5 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	−0.5	0.01	0.5	nA
				Full		−5		5	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = 1 V, or V_{NC} = 4.5 V, V_{COM} = 4.5 V, or V_{NC} = 1 V, 4.5 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	5.5 V	−1	0.01	1	nA
				Full		−10		10	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = 1 V, or V_{COM} = 4.5 V, V_{NC} = 4.5 V, or V_{COM} = 1 V, 4.5 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	5.5 V	−1	0.01	1	nA
				Full		−10		10	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		2.4		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V	−0.5	0.01	0.5	nA
				Full		−5		5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 5-V Supply(1) (continued)

V_+ = 4.5 V to 5.5 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{NC} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V		12	17	ns
				Full	4.5 V to 5.5 V			19	
Turn-off time	t_{OFF}	V_{NC} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V		9	14	ns
				Full	4.5 V to 5.5 V			17	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF,	See Figure 20	25°C	5 V		2	5	pC
NC OFF capacitance	$C_{NC(OFF)}$	V_{NC} = 0, f = 1 MHz,	Switch OFF, See Figure 16	25°C	5 V		6.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = 0, f = 1 MHz,	Switch OFF, See Figure 16	25°C	5 V		6.5		pF
NC ON capacitance	$C_{NC(ON))}$	V_{NC} = 0, f = 1 MHz,	Switch ON, See Figure 16	25°C	5 V		13		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = 0, f = 1 MHz,	Switch ON, See Figure 16	25°C	5 V		13		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Signal = 0 dBm,	Switch ON, See Figure 18	25°C	5 V		450		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz, V_{NC} = 1 V_{RMS},	Switch OFF, See Figure 19	25°C	5 V		−85		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF, V_{SOURCE} = 5 V_{p-p},	f = 20 Hz to 20 kHz, See Figure 21	25°C	5 V		0.04		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.25	μA
				Full				0.5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 3-V Supply(1)

V_+ = 2.7 V to 3.6 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	V_{NC} = 1.5 V, I_{COM} = 10 mA,	Switch ON, See Figure 13	25°C	2.7 V		9.5	16	Ω
				Full				20	
ON-state resistance flatness	$r_{on(flat)}$	V_{NC} = 1.5 V, 2.5 V, I_{COM} = 10 mA,	Switch ON, See Figure 13	25°C	2.7 V		1.8	6	Ω
				Full				7	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 3 V, or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	−0.5	0.01	0.5	nA
				Full		−5		5	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 3 V, or V_{COM} = 3 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	−0.5	0.01	0.5	nA
				Full		−5		5	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = 1 V, or V_{NC} = 3 V, V_{COM} = 3, or V_{NC} = 1 V, 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	3.6 V	−1	0.01	1	nA
				Full		−10		10	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = 1 V, or V_{COM} = 3 V, V_{NC} = 3 V, or V_{COM} = 1 V, 3 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	3.6 V	−1	0.01	1	nA
				Full		−10		10	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		2		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = V_+ or 0		25°C	3.6 V	−0.5	0.01	0.5	nA
				Full		−5		5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 3-V Supply(1) (continued)

V_+ = 2.7 V to 3.6 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	3 V		20	30	ns
				Full	2.7 V to 3.6 V			35	
Turn-off time	t_{OFF}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	3 V		15	25	ns
				Full	2.7 V to 3.6 V			30	
Charge injection	Q_C	V_{NC} = 0, C_L = 1 nF,	See Figure 20	25°C	3 V		1	4	pC
NC OFF capacitance	$C_{NC(OFF)}$	V_{NC} = V_+ or GND,	Switch OFF, See Figure 16	25°C	3 V		6.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND,	Switch OFF, See Figure 16	25°C	3 V		6.5		pF
NC ON capacitance	$C_{NC(ON)}$	V_{NC} = V_+ or GND,	Switch ON, See Figure 16	25°C	3 V		13		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND,	Switch ON, See Figure 16	25°C	3 V		13		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	3 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Signal = 0 dBm,	Switch ON, See Figure 18	25°C	3 V		450		MHz
OFF isolation	O_{ISO}	V_{NC} = 1 V_{RMS}, f = 1 MHz, C_L = 5 pF,	Switch OFF, See Figure 19	25°C	3 V		−85		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF, V_{SOURCE} = 3 V_{p-p},	f = 20 Hz to 20 kHz, See Figure 21	25°C	3 V		0.09		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		0.01	0.25	µA
				Full				0.5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

TYPICAL PERFORMANCE

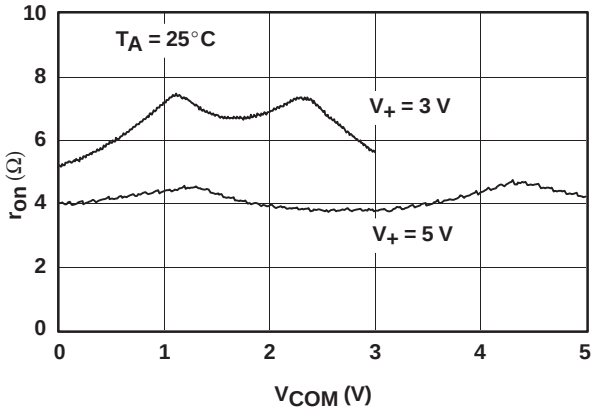


Figure 1. r_{on} vs V_{COM}

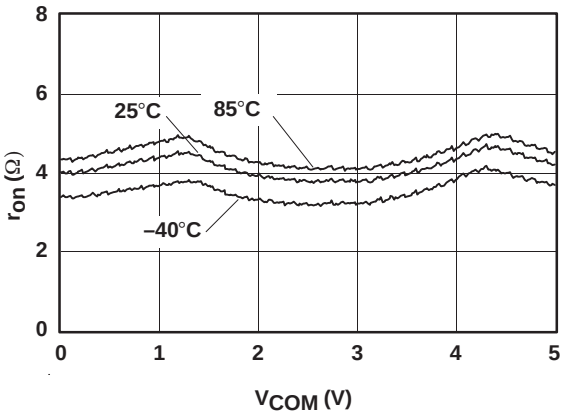


Figure 2. r_{on} vs V_{COM} (V_+ = 5 V)

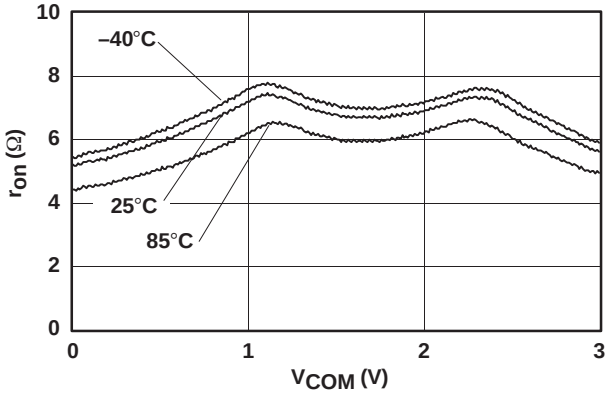


Figure 3. r_{on} vs V_{COM} (V_+ = 3 V)

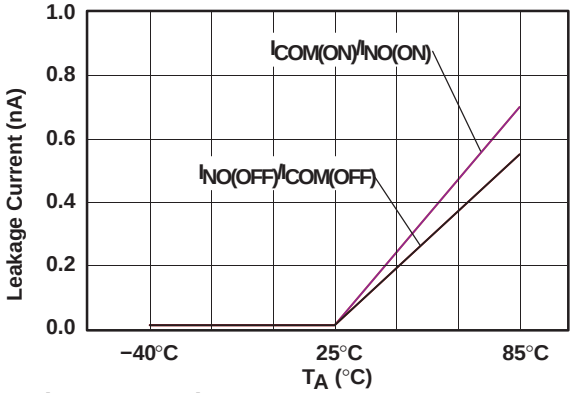


Figure 4. Leakage Current vs Temperature (V_+ = 5 V)

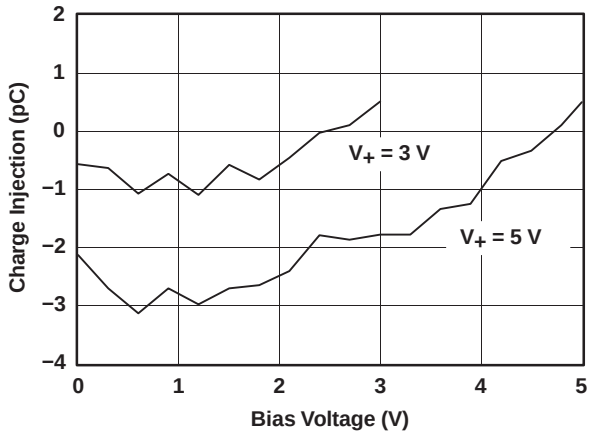


Figure 5. Charge-Injection (Q_C) vs V_{COM}

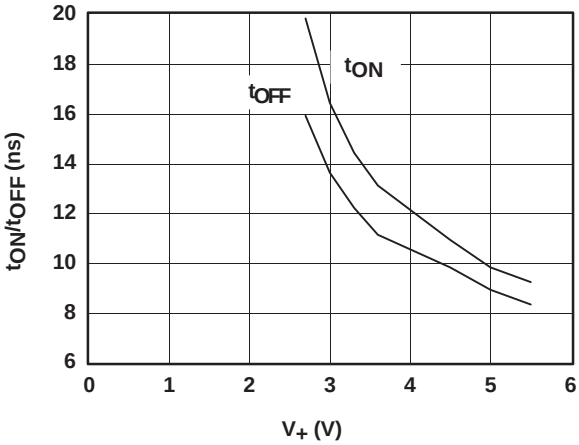


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

TYPICAL PERFORMANCE (continued)

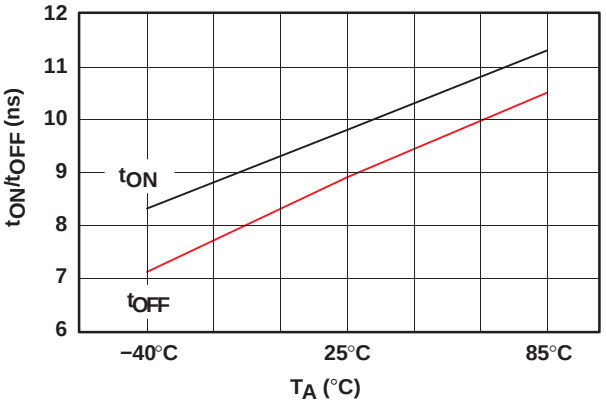


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

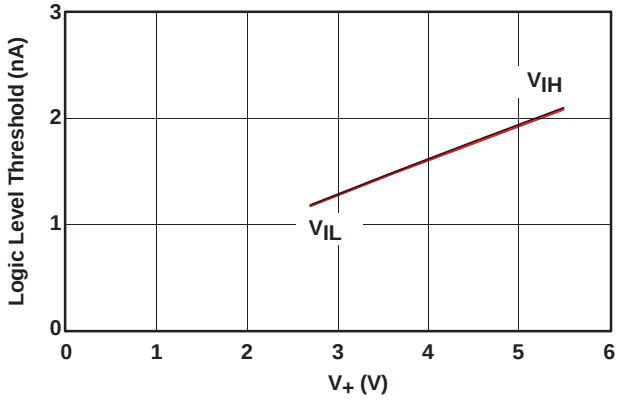


Figure 8. Logic-Level Threshold vs V_+

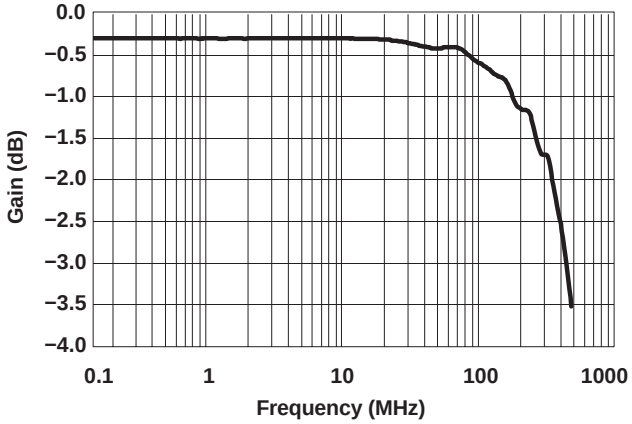


Figure 9. Bandwidth (Gain vs Frequency) (V_+ = 5 V)

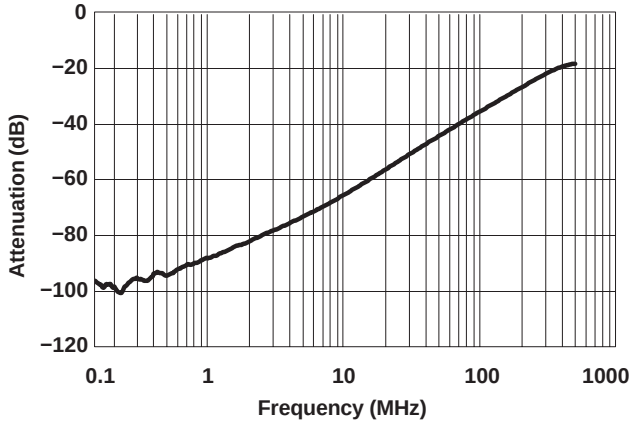


Figure 10. OFF Isolation vs Frequency

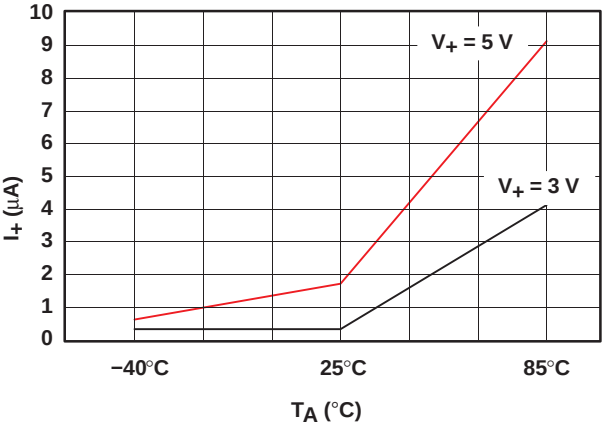


Figure 11. Power-Supply Current vs Temperature

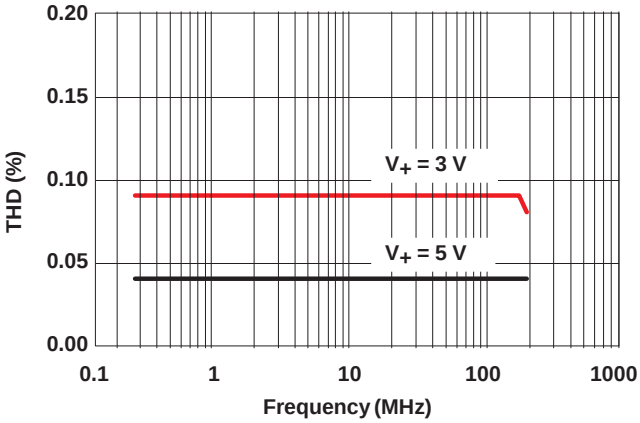


Figure 12. Total Harmonic Distortion vs Frequency

PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	IN	Digital control pin to connect COM to NC
2	COM	Common
3	GND	Digital ground
4	NC	Normally closed
5	V_+	Power supply

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
r_{on}	Resistance between COM and NC ports when the channel is ON
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC) in the OFF state
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC) in the ON state and the output (NC) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NC) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NC) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance, and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is OFF
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is −3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

PARAMETER MEASUREMENT INFORMATION

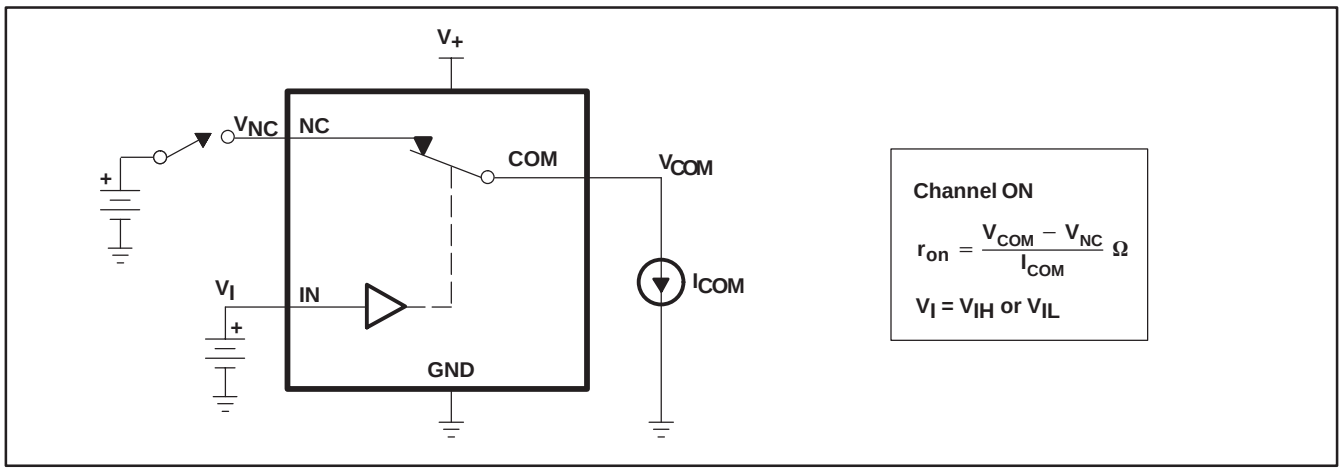


Figure 13. ON-State Resistance (r_{on})

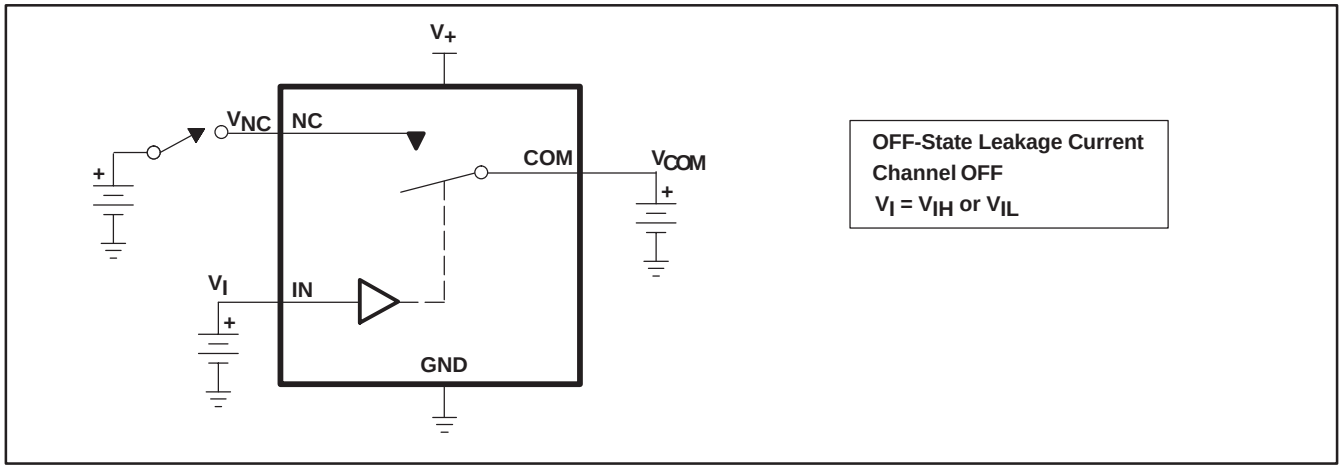


Figure 14. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$)

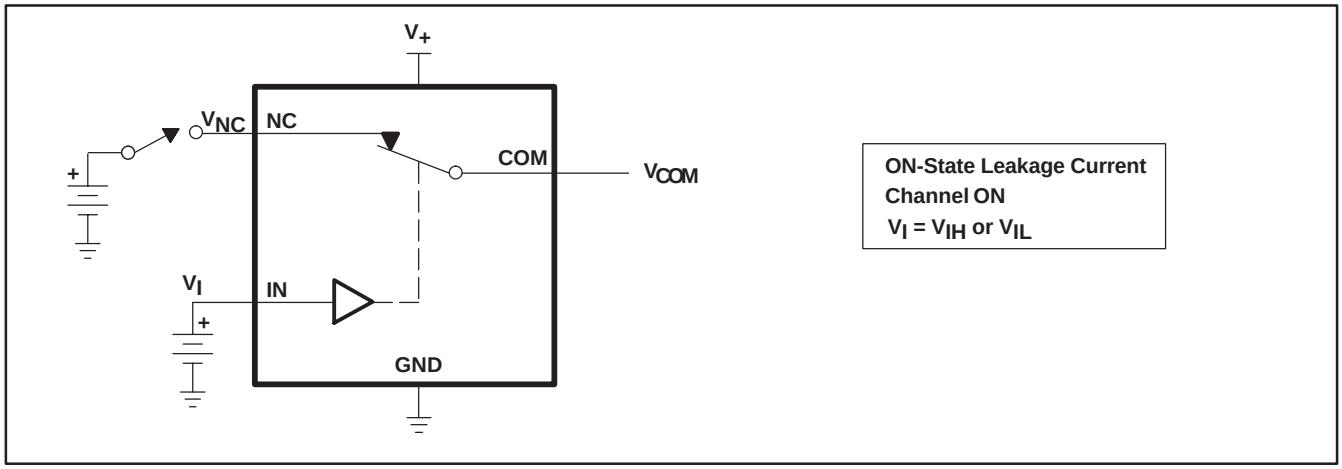


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

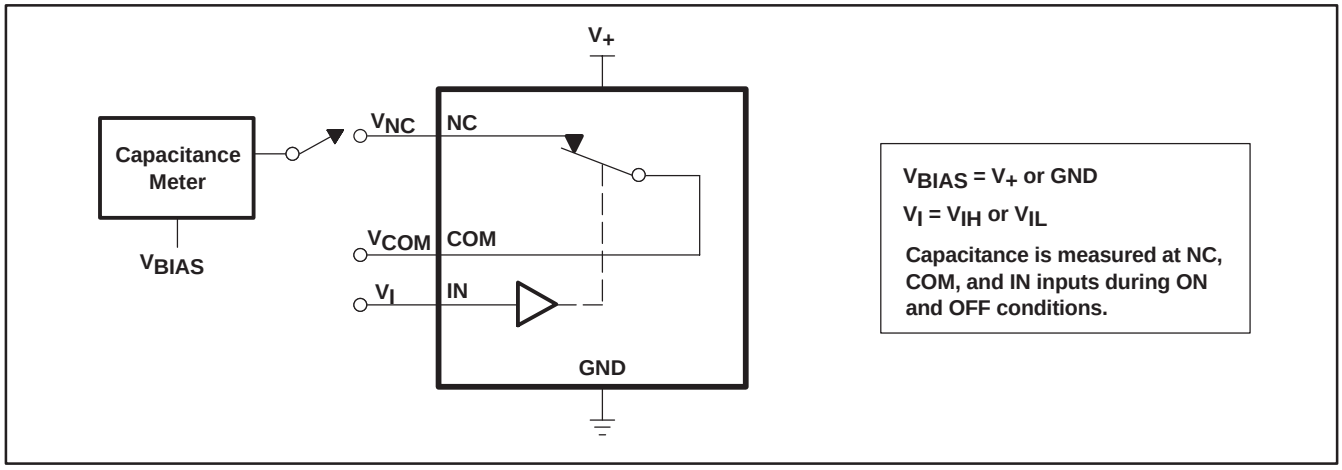
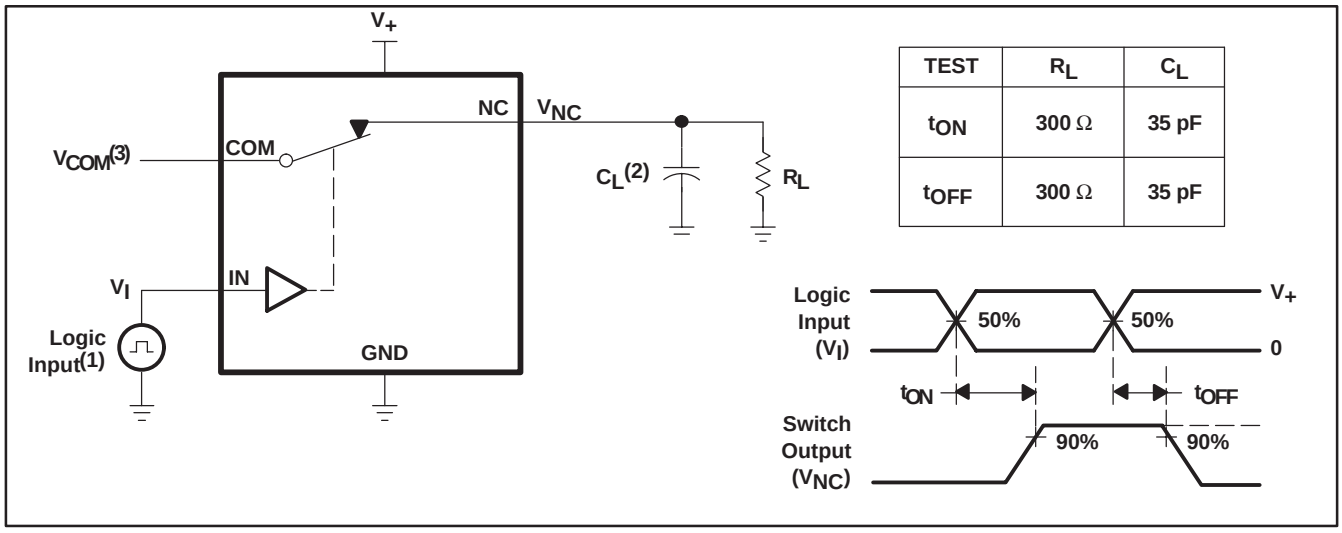


Figure 16. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.
(3) See Electrical Characteristics for V_{COM}.

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

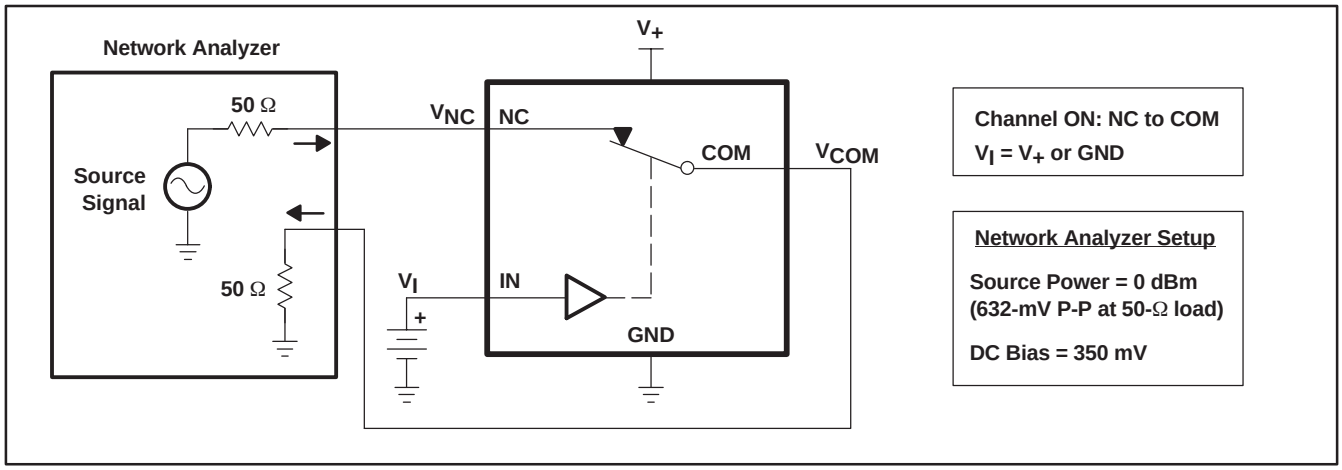


Figure 18. Bandwidth (BW)

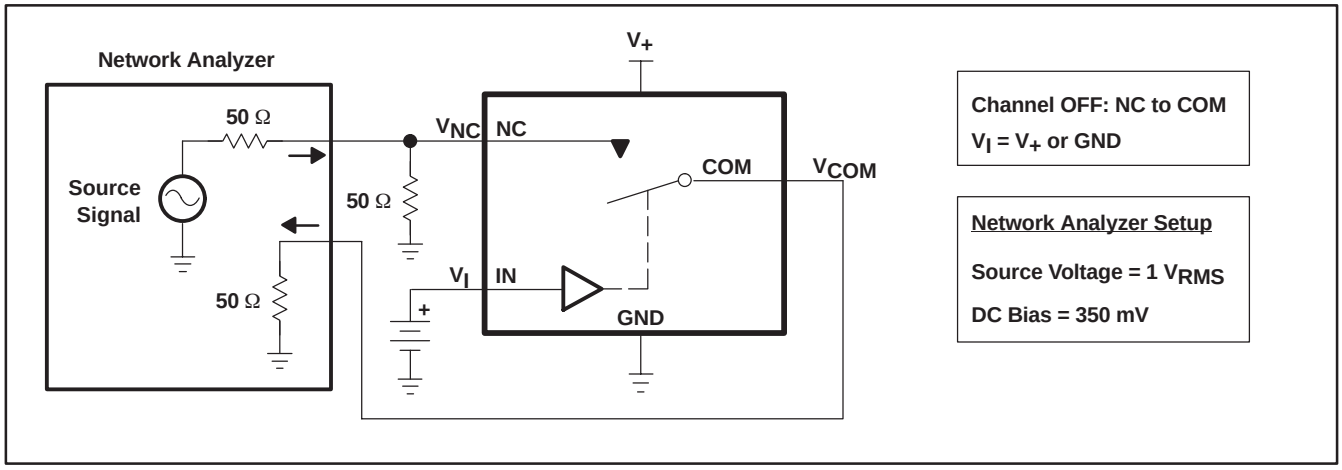
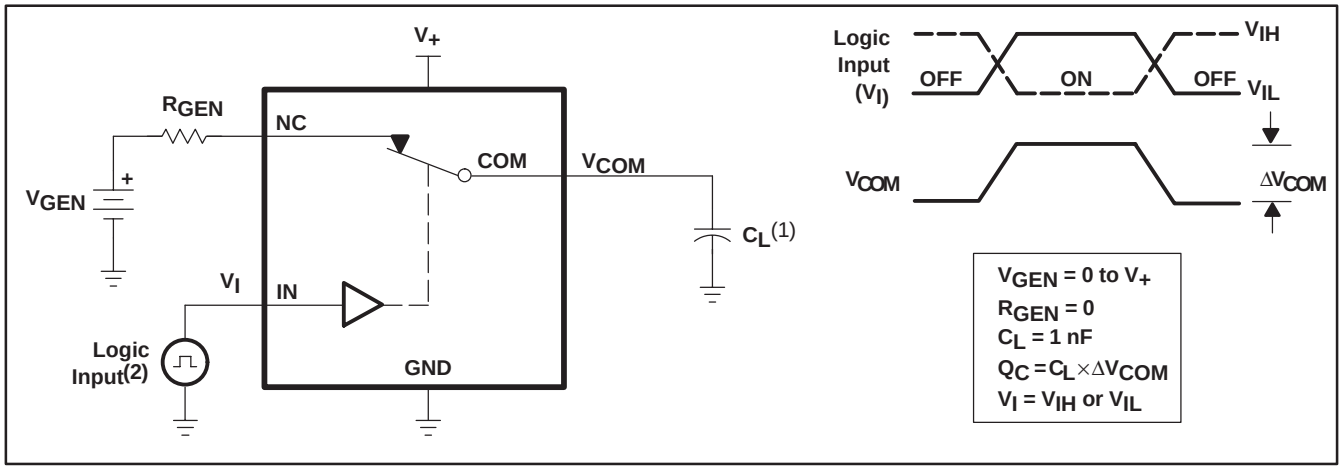
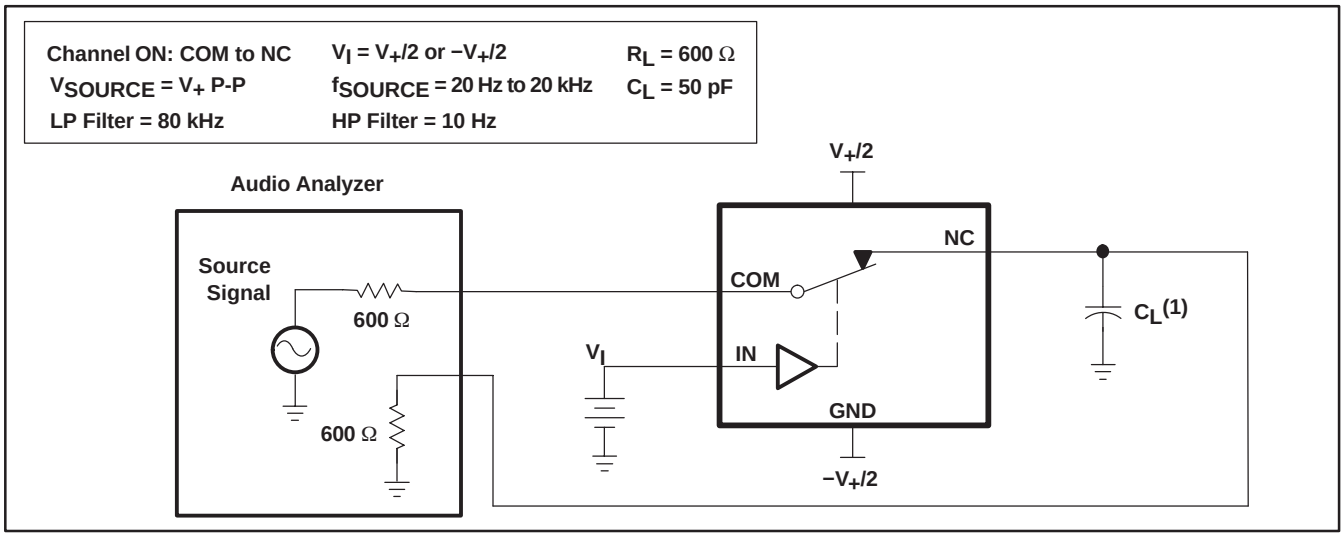


Figure 19. OFF Isolation (O_{ISO})



(1) C_L includes probe and jig capacitance.
(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 20. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 21. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A4597DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JSDR	Samples
TS5A4597DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JSDR	Samples
TS5A4597DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JVR	Samples
TS5A4597DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JVR	Samples
TS5A4597DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JVR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

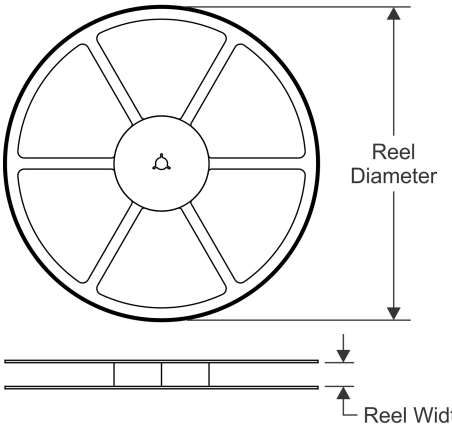
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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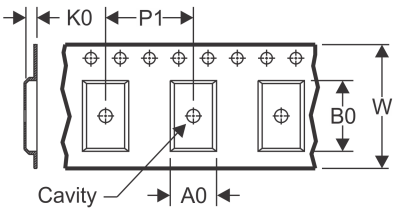
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

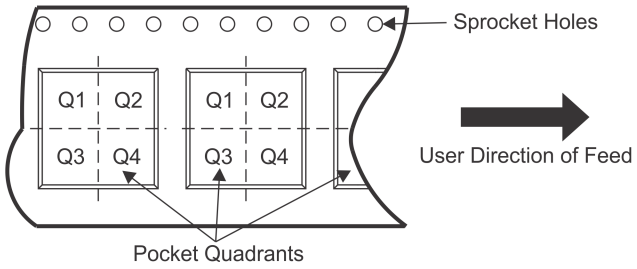


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

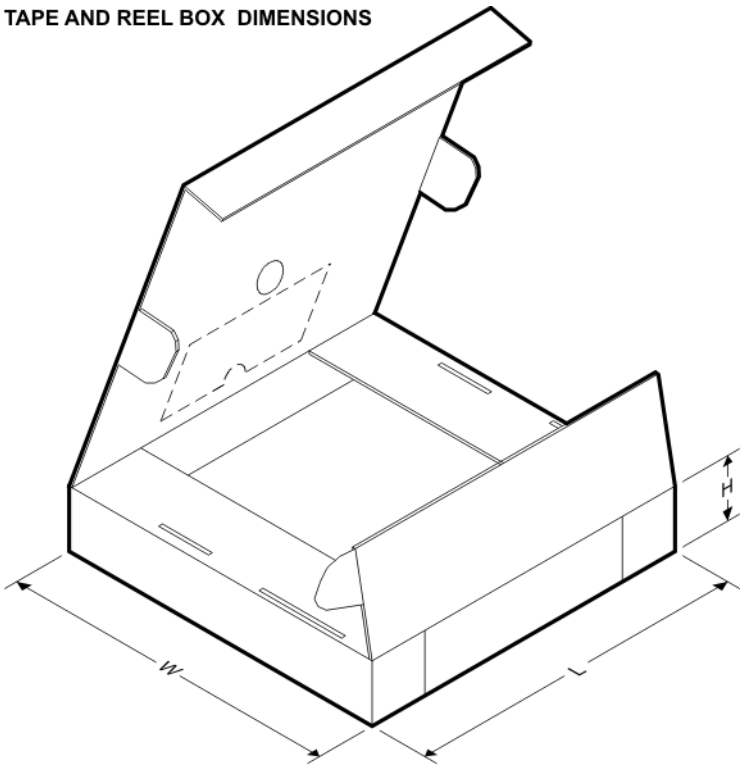
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A4597DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A4597DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A4597DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TS5A4597DCKR	SC70	DCK	5	3000	202.0	201.0	28.0

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