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January 2015

FSA2380 — Low R_{ON} (0.75 Ω) 3:1 Negative Swing Audio Source Switch

Features

- 10 μ A Maximum I_{CCT} Current Over An Expanded Control Voltage Range ($V_{IN}=2.6$ V, $V_{CC}=4.3$ V)
- C_{ON} Capacitance 70 pF Typical
- 0.75 Ω Typical On Resistance (R_{ON})
- 1Bn, 2Bn Ports Support Negative Swing Audio to -2 V
- 3 db Bandwidth: > 120 MHz
- Low Power Consumption (1 μ A maximum)
- Power-Off Feature for 1 A/2 A Pin ($I_{IN} < 2$ μ A)
- Packaged in Pb-Free 14-Pin TSSOP and DQFN

Description

The FSA2380 is a Double-Pole, Triple Throw (DP3T) multiplexer that routes three dual-channel sources of data or audio under the control of a single pair of select pins. The FSA2380 has special circuitry on the 1A/2A pins to allow a power-off feature. With the V_{CC} supply removed and voltage on the 1A/2A pins, there is minimal leakage current into the 1A/2A data pins. The FSA2380 also features very low quiescent current and a power-off feature to extend battery life. The low quiescent current feature allows mobile handset applications direct interface with the baseband processor general-purpose I/Os. Typical applications involve switching in portables and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers.

Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

Ordering Information

Part Number	Top Mark	Packing Description
FSA2380BQX	2380	14-Terminal Depopulated very thin Quad Flat-pack No leads (DQFN) 2.5 x 3.0 mm, JEDEC MO-241
FSA2380MTCX	FSA2380	14-Lead Thin Shrink Small Outline Package (TSSOP) 4.4 mm wide, JEDEC MO-153

Analog Symbol

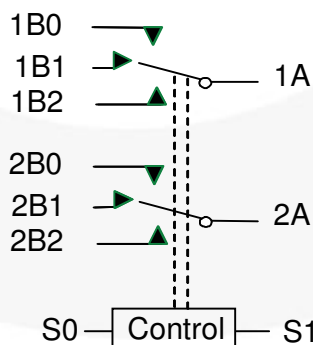


Figure 1. FSA2380 Analog Symbol

Pin Assignments

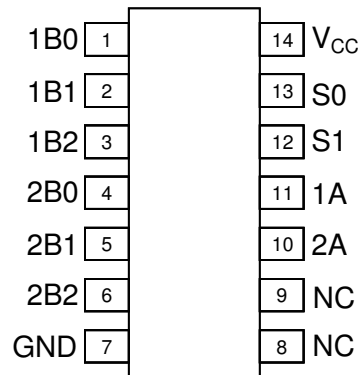


Figure 2. TSSOP-14 (Top Through View)

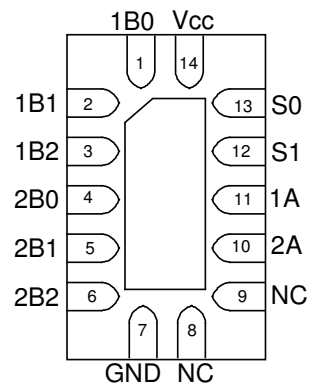


Figure 3. DQFN-14 (Top Through View)

Pin Descriptions

Name	Description
S0, S1	Switch Control Selects
1A, 2A	A Data Bus (Common)
1Bn, 2Bn	Multiplexed Source inputs

Truth Table

S1	S0	Function
LOW Logic Level	LOW Logic Level	Disconnected (Hi-Z)
LOW Logic Level	HIGH Logic Level	1B0 = 1A; 2B0 = 2A
HIGH Logic Level	LOW Logic Level	1B1 = 1A; 2B1 = 2A
HIGH Logic Level	HIGH Logic Level	1B2 = 1A; 2B2 = 2A

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V _{CC}	Supply Voltage		-0.5	6.0	V
V _{SW}	Switch I/O Voltage ⁽¹⁾	1Bn, 2Bn Pins	V _{CC} -5.5	V _{CC} +0.3	V
		1A, 2A Pins	V _{CC} -5.5	V _{CC} +0.3	V
V _{CNTRL}	Control Input Voltage ⁽¹⁾ S0, S1 Pins		-0.5	6.0	V
I _{IK}	Input Clamp Diode Current		-50		mA
I _{SW}	Switch I/O Current (Continuous)			350	mA
I _{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)			500	mA
P _D	Power Dissipation at 85°C	DQFN-14		2.5	μW
		TSSOP-14		2.5	μW
T _{STG}	Storage Temperature Range		-65	+150	°C
T _J	Maximum Junction Temperature			+150	°C
T _L	Lead Temperature (Soldering, 10 seconds)			+260	°C
ESD	Human Body Model (JEDEC: JESD22-A114)	All Pins		5500	kV
		I/O to GND		8000	
		VCC to GND		8000	
	Charged Device Model (JEDEC-JESD22-C101)				2000

Note:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.7	5.0	V
V_{CNTRL}	Control Input Voltage ($V_{S0:S1}$)	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	$V_{CC}-5.5$	V_{CC}	
T_A	Operating Temperature	-40	+85	°C
θ_{JA}	Thermal Resistance (free air)	DQFN-14	145	°C/W
		TSSOP-14		

DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = - 40°C to +85°C			Unit
				Min.	Typ.	Max.	
	Analog Signal Range			V _{CC} - 5.5		V _{CC}	V
V _{IK}	Clamp Diode Voltage					1.2	V
V _{IH}	Control Input Voltage HIGH		2.7 to 3.6	1.2			V
			3.6 to 4.3	1.5			
V _{IL}	Control Input Voltage LOW		2.7 to 3.6			0.5	
			3.6 to 4.3			0.7	
I _{IN}	Control Input Leakage	V _{IN} = 0 to V _{CC}	4.3			±1	μA
I _{OFF}	Power Off Leakage Current (Common Port Only 1A, 2A)	Common Port (1A, 2A) V _{SW} = 0 to 4.3 V V _{CC} = 0 V	0V			±10	μA
I _{NO(OFF)}	Off-Leakage Current of Port (1Bn, 2Bn)	1Bn, 2Bn or 1A, 2A = 0.3 V, V _{CC} -0.5 V, or Floating	4.3	-50	10	50	nA
I _{NC(ON)}	On-Leakage Current of Port 1Bn, 2Bn	1Bn, 2Bn or 1A, 2A = 0.3 V, V _{CC} -0.5 V, or Floating	4.3	-50	10	50	nA
R _{ON}	Switch On Resistance ⁽²⁾	1Bn or 2Bn = 0 V, 0.7 V, 2.0 V, 2.7 V; I _{ON} = -100 mA See Figure 7, Figure 8	2.70		0.75	2.00	Ω
ΔR _{ON}	Delta On Resistance ⁽³⁾	1Bn or 2Bn = 0.7 V, V _{CC} , I _{ON} = -100 mA	2.70		0.50		Ω
R _{FLAT(ON)}	On Resistance Flatness ⁽⁴⁾	1Bn or 2Bn = 0V, 0.7 V, 2.0 V, 2.7 V; I _{ON} = -100 mA See Figure 7, Figure 8	2.7 to 4.3		0.23	0.40	Ω
I _{CC}	Quiescent Supply Current	V _{SW} = 0 or V _{CC} -0.3 I _{OUT} = 0	4.3		22	500	nA
I _{CCT}	Increase in Quiescent Supply Current per Control Voltage and V _{CC}	V _{CNTRL} = 2.6 V	4.3		2.0	10.0	μA
		V _{CNTRL} = 1.8 V			6.5	15.0	

Notes:

- R_{ON} measured by the voltage drop between 1Bn (2Bn) and 1A (2A) pins at identical current through the switch. R_{ON} is determined by the lower of the voltage on the two pins.
- Guaranteed by characterization, not production tested.
- Flatness is defined as the difference between the maximum and minimum values of on resistance over the specified range of conditions.

AC Electrical Characteristics

All typical value are for $V_{CC} = 3.3\text{ V}$ at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
t_{ON}	Turn-On Time S[0:1] to Output	$V_{Bn} = 1.5\text{ V}$, $R_L = 50\Omega$, $C_L = 35\text{ pF}$ Figure 10, Figure 12	2.7 to 4.3		30	60	ns
t_{OFF}	Turn-Off Time S[0:1] to Output	$V_{Bn} = 1.5\text{ V}$, $R_L = 50\Omega$, $C_L = 35\text{ pF}$ Figure 10, Figure 12	2.7 to 4.3		22	45	ns
t_{PD}	Propagation Delay ⁽⁵⁾	$R_L = 50\Omega$, $C_L = 5\text{ pF}$ Figure 13	3.3		0.25		ns
t_{BBM}	Break-Before-Make ⁽⁵⁾	$R_L = 50\Omega$, $C_L = 5\text{ pF}$ $V_{IN1} = V_{IN2} = V_{IN3} = 1.5\text{ V}$ Figure 11	2.7 to 4.3	1	6		ns
Q	Charge Injection	$R_{GEN} = 0\Omega$, $C_L = 100\text{ pF}$, $R_L = \text{OPEN}$ Figure 14	2.7 to 4.3		9		pC
O_{IRR}	Off-Isolation	$f = 100\text{ kHz}$, $R_L = 50\Omega$ Figure 4, Figure 16	2.7 to 4.3		-68		dB
Xtalk	Non-Adjacent Channel Crosstalk	$f = 100\text{ kHz}$, $R_L = 50\Omega$ Figure 5, Figure 17	2.7 to 4.3		-60		dB
THD	Total Harmonic Distortion	$f = 20\text{ Hz to } 20\text{ kHz}$, $R_L = 600\Omega$, $V_{SW} = 0.5V_{pp}$, Figure 20	2.7 to 4.3		0.01		%
BW	-3 db Bandwidth	$R_L = 50\Omega$, $C_L = 0, 5\text{ pF}$ Figure 6, Figure 15	2.7 to 4.3		120		MHz

Note:

5. Guaranteed by characterization, not production tested.

Capacitance

Symbol	Parameter	Conditions	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	Unit
			Typical	
C_{IN}	Control Pin Input Capacitance	$V_{CC} = 0\text{ V}$	2.75	pF
C_{ON}	A/B On Capacitance	$V_{CC} = 3.3\text{ V}$; S[0:1] = 01, 10, 11; $f = 1\text{ MHz}$ Figure 19	70	pF
C_{OFFA}	Port 1A, 2A Off Capacitance	$V_{CC} = 3.3\text{ V}$, S[0:1] = 00 Figure 18	42	pF
C_{OFFB}	Port 1Bn, 2Bn Off Capacitance	$V_{CC} = 3.3\text{ V}$, S[0:1] = 00 Figure 18	20	pF

Typical Characteristics

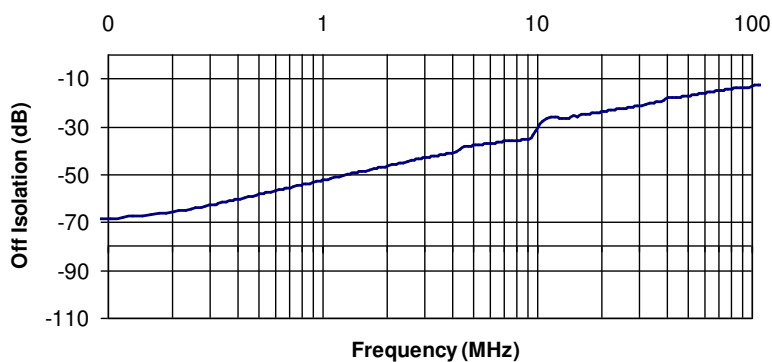


Figure 4. Off Isolation $V_{CC} = 3.3\text{ V}$, $C_L = 0\text{ pF}$

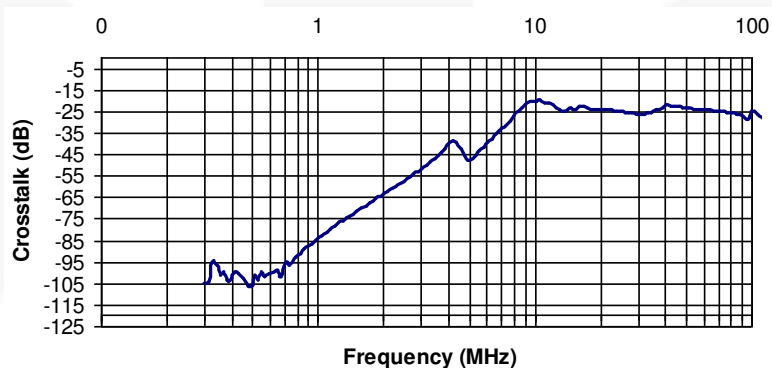


Figure 5. Non-Adjacent Crosstalk $V_{CC} = 3.3\text{ V}$, $C_L = 0\text{ pF}$

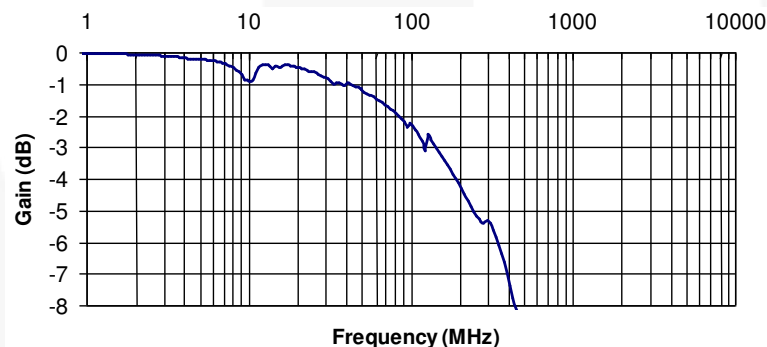


Figure 6. Bandwidth $V_{CC} = 3.3\text{ V}$, $C_L = 0\text{ pF}$

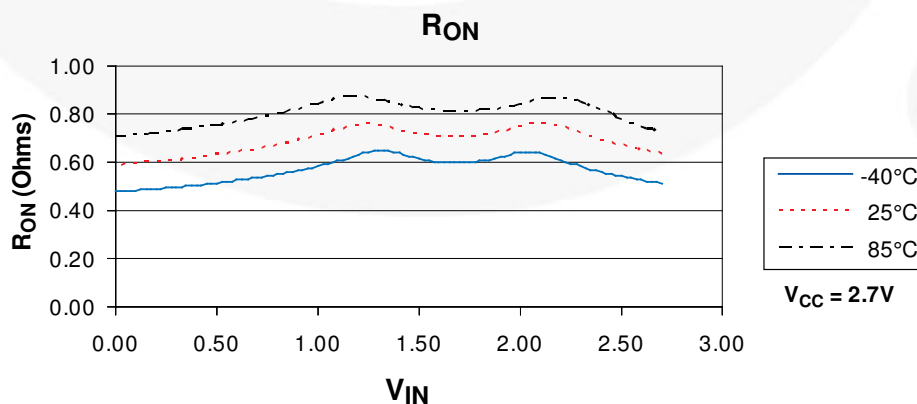


Figure 7. Switch On Resistance, R_{ON} $V_{CC} = 2.7\text{ V}$

Test Diagrams

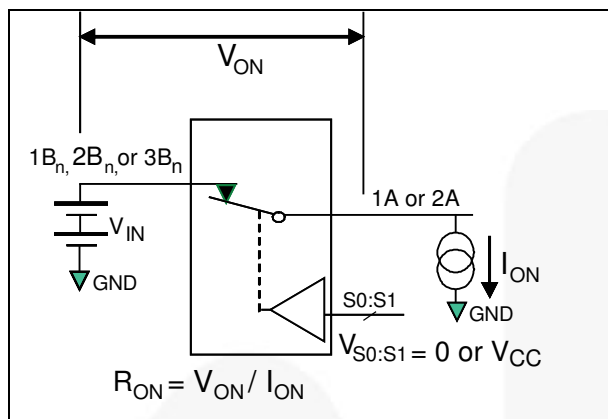


Figure 8. On Resistance

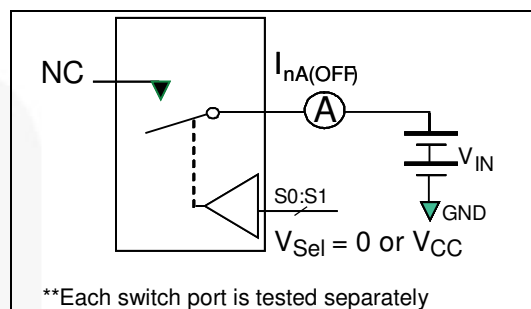


Figure 9. Off Leakage

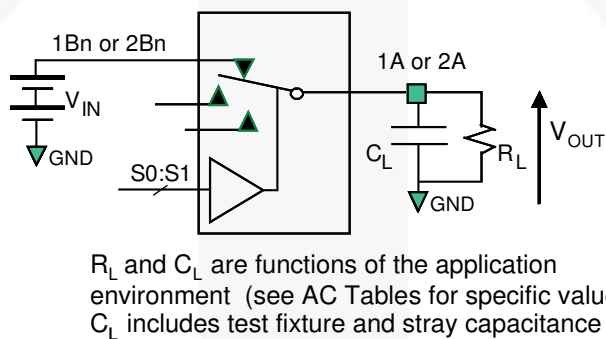


Figure 10. AC Test Circuit Load

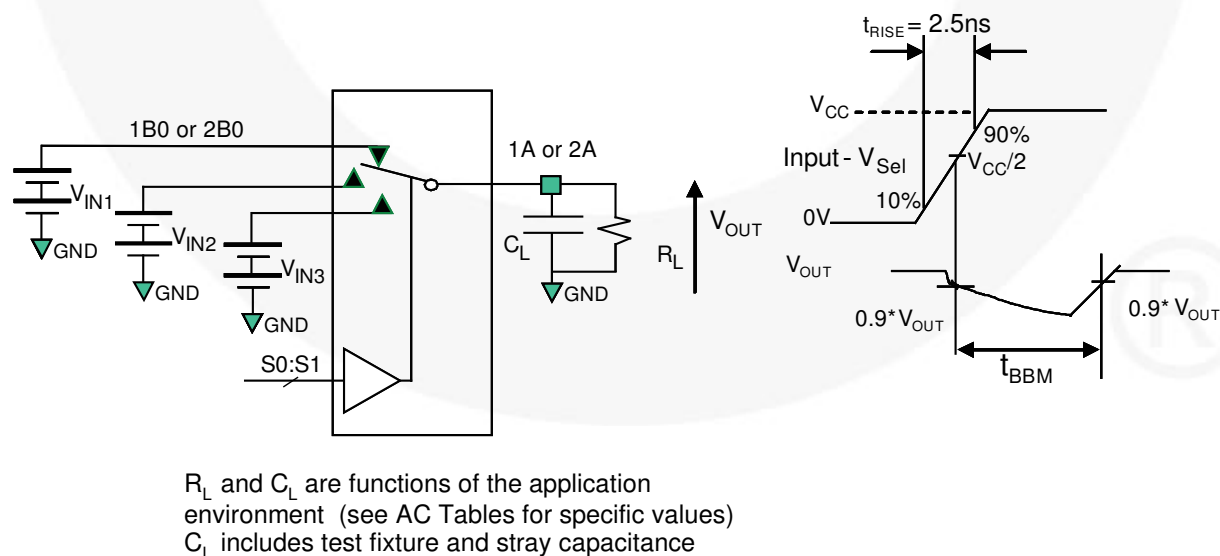


Figure 11. Break-Before-Make Timing

Test Diagrams (Continued)

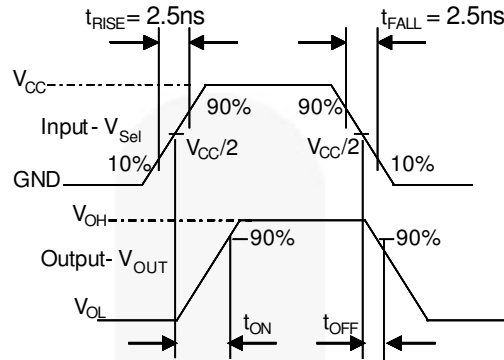


Figure 12. Turn-On / Turn-Off Waveforms

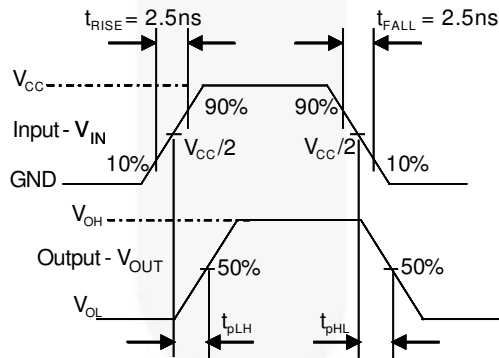


Figure 13. Switch Propagation Delay Waveforms

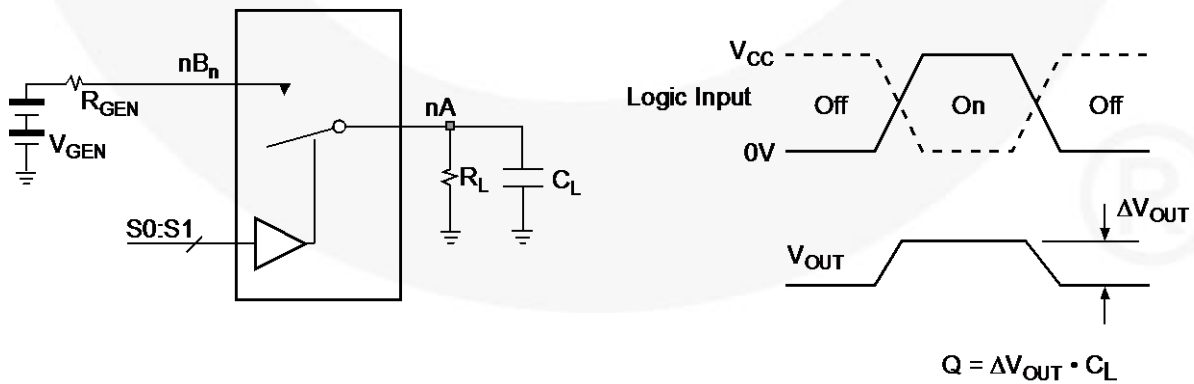


Figure 14. Charge Injection Test

Test Diagrams (Continued)

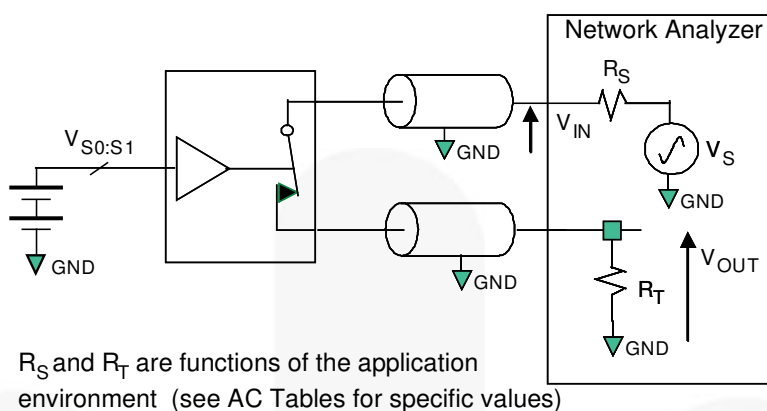


Figure 15. Bandwidth

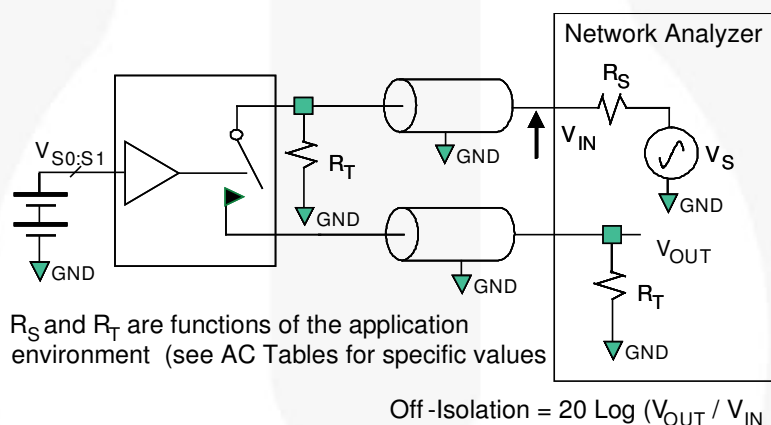


Figure 16. Channel Off Isolation

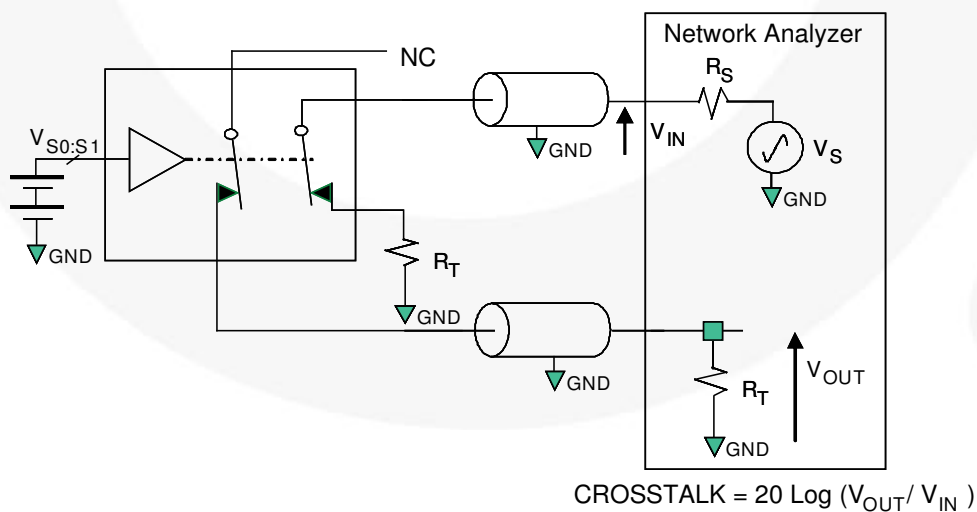


Figure 17. Non-Adjacent Channel-to-Channel Crosstalk

Test Diagrams (Continued)

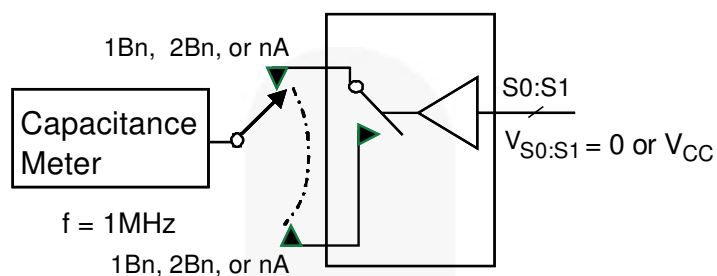


Figure 18. Channel Off Capacitance

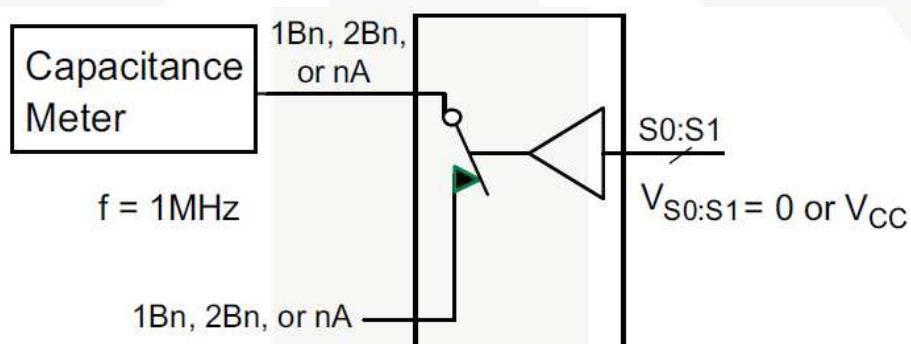


Figure 19. Channel On Capacitance

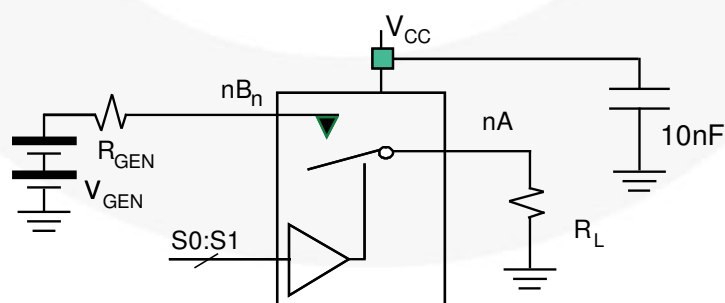
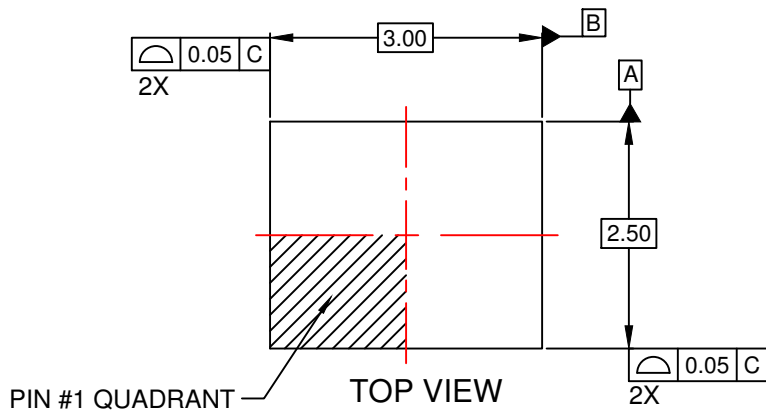
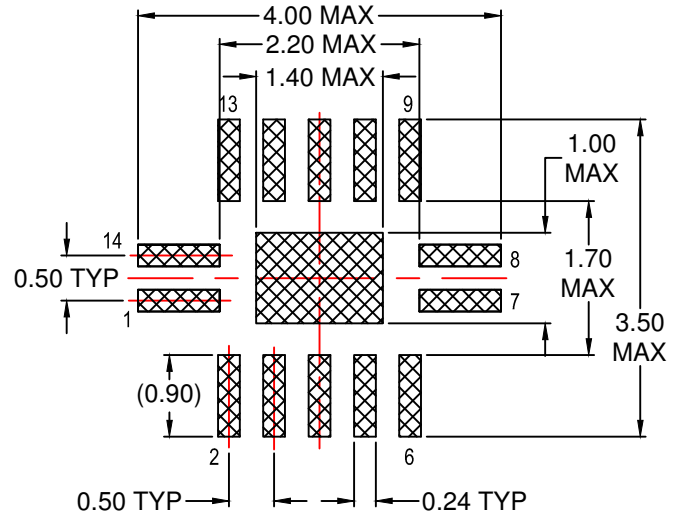
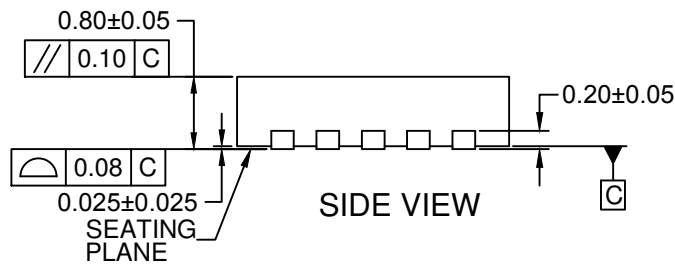
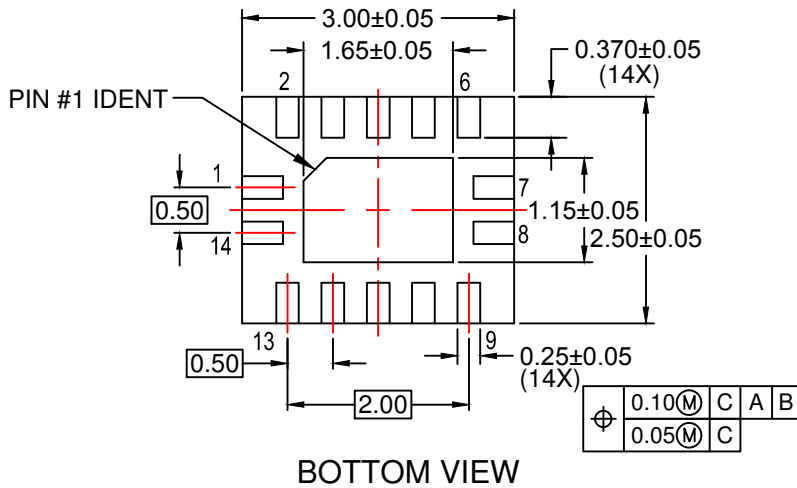


Figure 20. Total Harmonic Distortion



RECOMMENDED LAND PATTERN



NOTES:

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