ADNS-5095

Low Power Optical Mouse Sensor

Data Sheet

Description

The Avago Technologies ADNS-5095 is a low power, small form factor optical mouse sensor. It has a new low-power architecture and automatic power management modes, making it ideal for battery, power-sensitive applications – such as cordless input devices.

The ADNS-5095 is capable of high-speed motion detection – up to 30ips and 8G. In addition, it has an on-chip oscillator and LED driver to minimize external components.

The ADNS-5095 along with the ADNS-5100-001 trim lens, ADNS-5200 clip and HLMP-EG3E-xxxxx LED form a complete and compact mouse tracking system. There are no moving parts and this translates to high reliability and less maintenance for the end user. In addition, precision optical alignment is not required, facilitating high volume assembly.

The sensor is programmed via registers through a four-wire serial port. It is housed in an 8-pin staggered dual in-line package (DIP).

Features

- Low Power Architecture
- Small Form Factor
- Programmable Periods / Response Times and Downshift Times from one mode to another for the Power-saving Modes
- 'Smart' LED Current Switching depending on surface brightness
- High Speed Motion Detection up to 30ips and 8G
- External Interrupt Output for Motion Detection
- Internal Oscillator – no clock input needed
- Selectable Resolution up to 1750cpi
- Operating Voltage: as low as 2.8V
- Four wire Serial Port Interface
- Minimal number of passive components

Applications

- Optical mice and optical trackballs
- Integrated input devices
- Battery-powered input devices

Theory of Operation

The ADNS-5095 is based on Optical Navigation Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

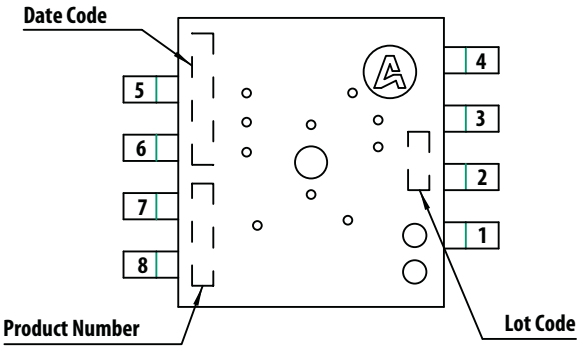
The ADNS-5095 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a four wire serial port.

The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Dx and Dy relative displacement values.

An external microcontroller reads and translates the Dx and Dy information from the sensor serial port into PS2, USB, or RF signals before sending them to the host PC.

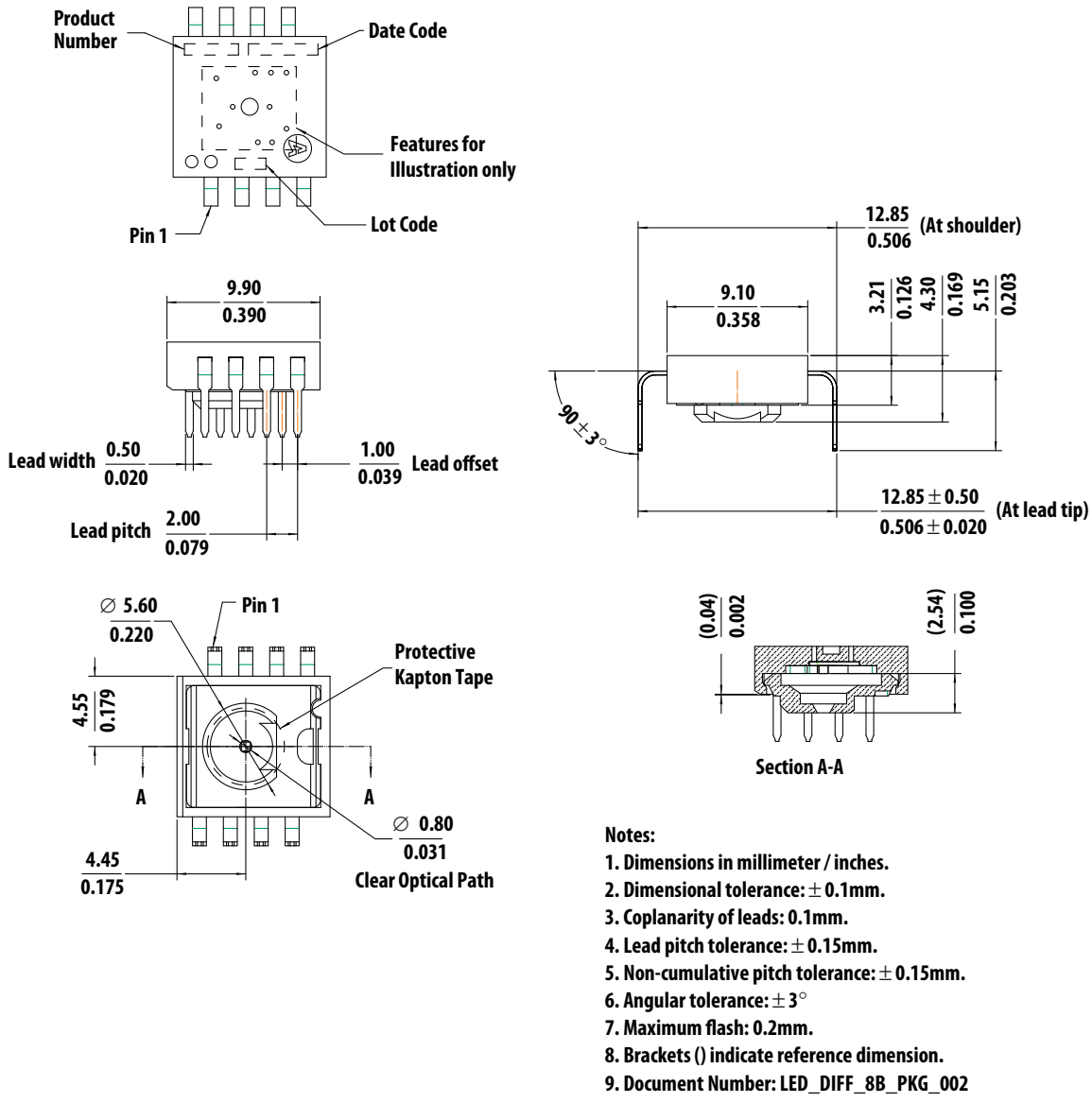
Pinout of ADNS-5095 Optical Mouse Sensor

Pin	Name	Input/ Output	Description
1	MISO	O	Serial Data Output (Master In/ Slave Out)
2	LED	O	LED Illumination
3	MOTION	O	Motion Interrupt Output (Default active low)
4	NCS	I	Chip Select (Active low input)
5	SCLK	I	Serial Clock
6	GND	Gnd	Ground
7	VDD	Power	Supply Voltage
8	MOSI	I	Serial Data Input (Master Out/ Slave In)



Item	Marking	Remarks
Product Number	A5095	
Date Code	XYYWWZ	X = Subcon Code YYWW = Date Code Z = Sensor Die Source
Lot Code	VVV	Numeric

Figure 1. Package outline drawing (top view)



Notes:

1. Dimensions in millimeter / inches.
2. Dimensional tolerance: ±0.1mm.
3. Coplanarity of leads: 0.1mm.
4. Lead pitch tolerance: ±0.15mm.
5. Non-cumulative pitch tolerance: ±0.15mm.
6. Angular tolerance: ±3°
7. Maximum flash: 0.2mm.
8. Brackets () indicate reference dimension.
9. Document Number: LED_DIFF_8B_PKG_002

Figure 2. Package Outline Drawing

CAUTION: It is advised that normal static precautions be taken in handling and assembling of this component to prevent damage and/or degradation which may be induced by ESD.

Overview of Optical Mouse Sensor Assembly

Avago Technologies provides an IGES file drawing describing the base plate molding features for lens and PCB alignment. The ADNS-5095 sensor is designed for mounting on a through-hole PCB. There is an aperture stop and features on the package that align to the lens. The ADNS-5100-001 lens provides optics for the imaging of the surface as well as illumination of the surface at the optimum angle. Features on the lens align it to the sensor, base plate, and clip with the LED. The ADNS-5200 clip holds the LED in relation to the lens. The LED must be inserted into the clip and the LED's leads formed prior to loading on the PCB.

The HLMP-EG3E-xxxx LED is recommended for illumination.

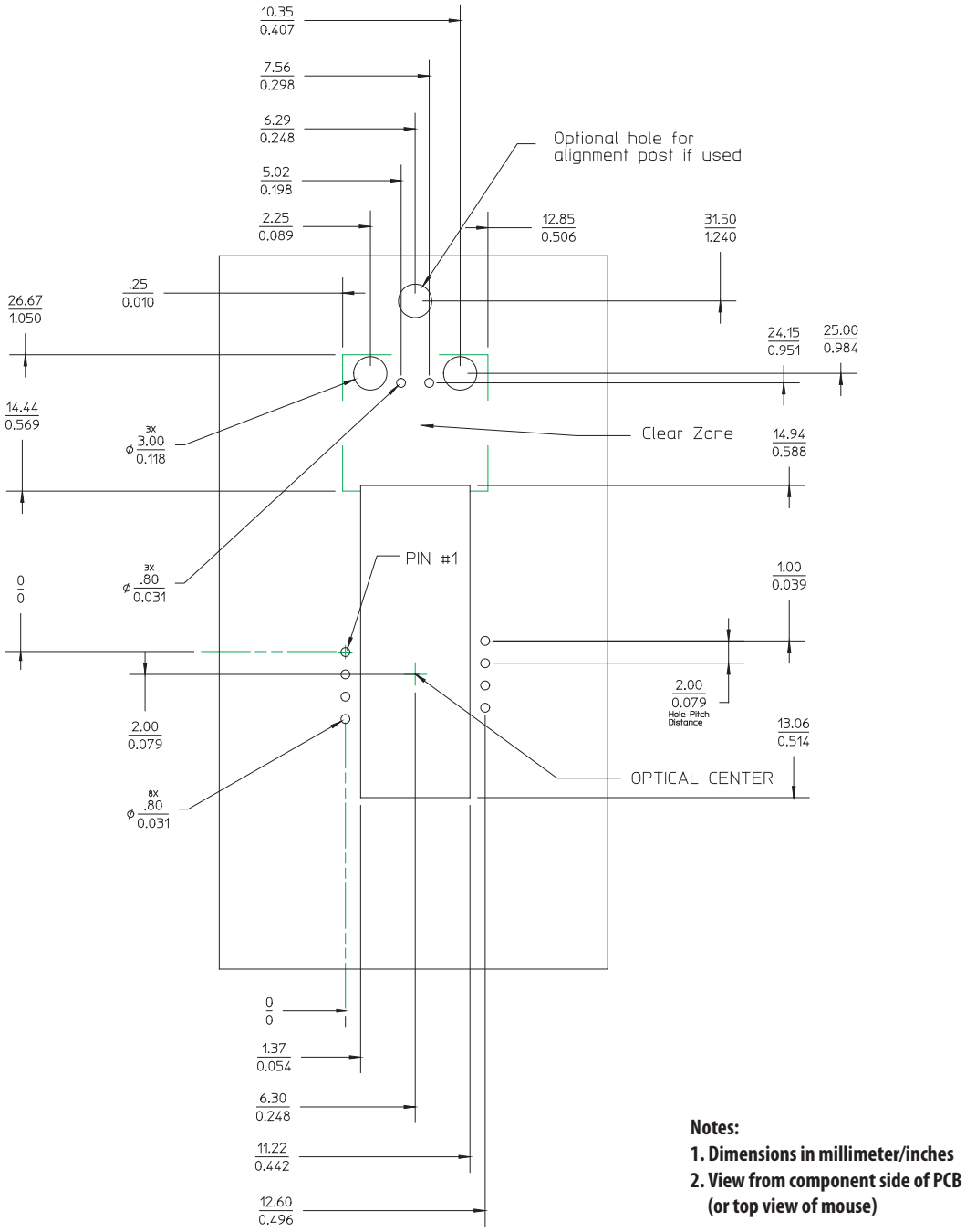
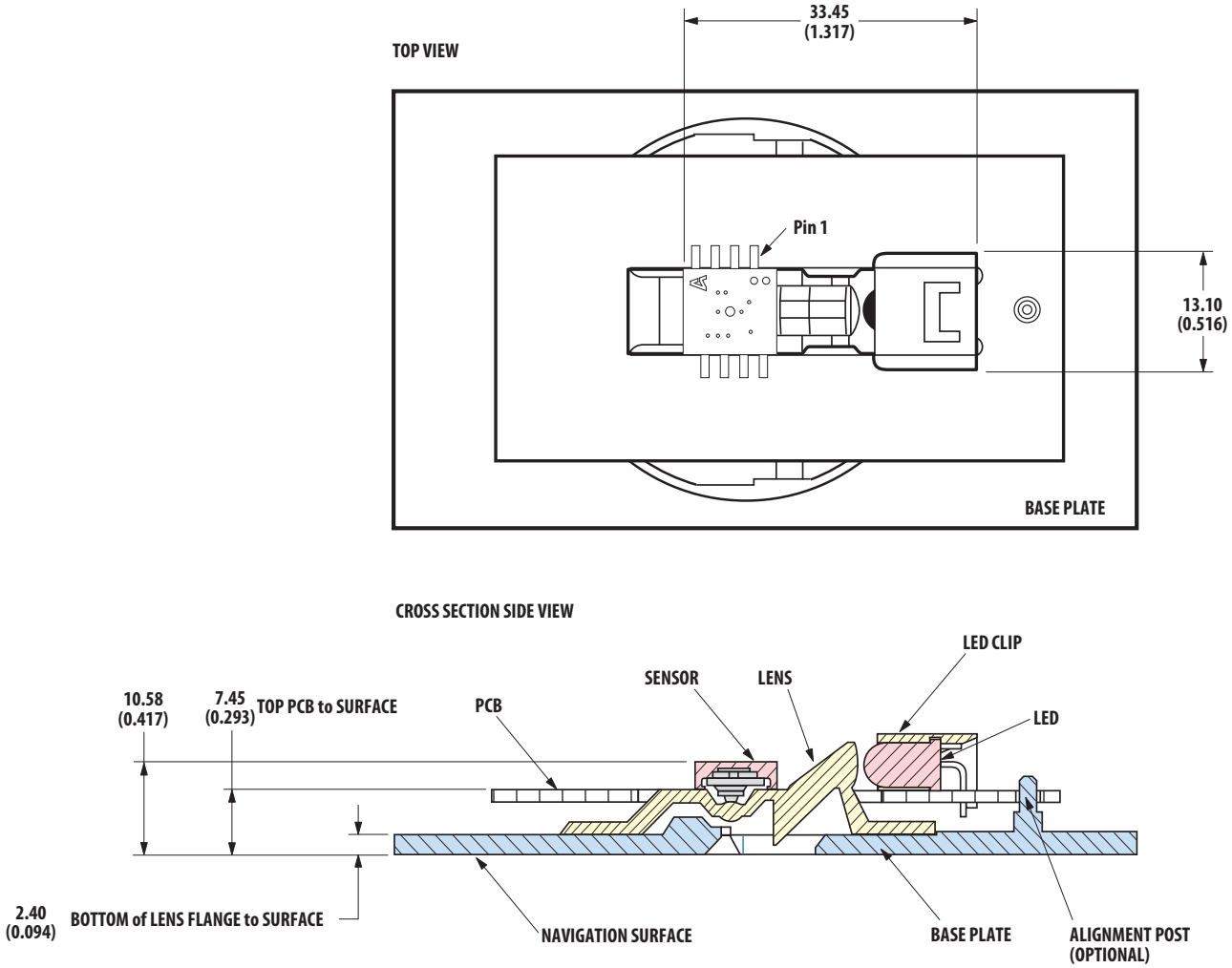


Figure 3. Recommended PCB Mechanical Cutouts and Spacing (Top View)



Important Note: Pin 1 of sensor should be located nearest to the LED

Figure 4. 2D Assembly drawing of ADNS-5095 (Top and Side View)

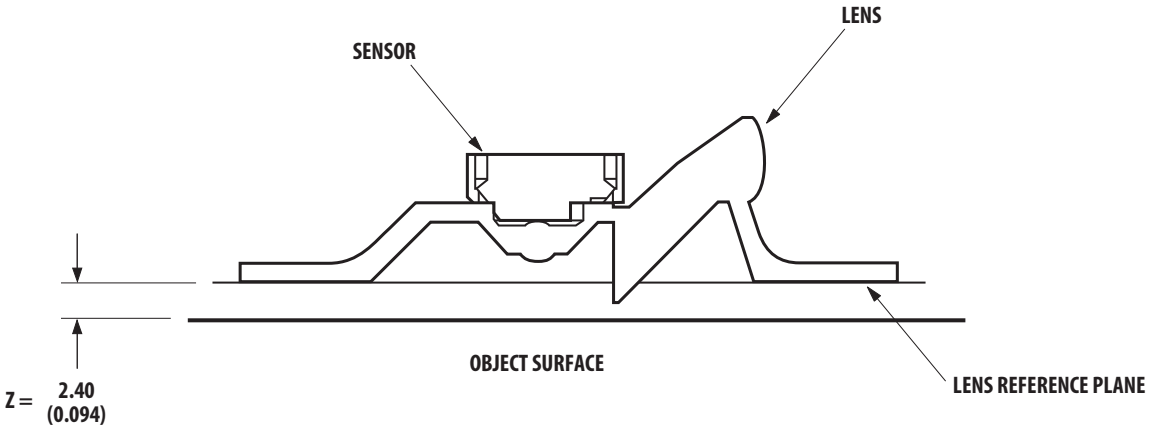


Figure 5. Distance from lens reference plane to tracking surface (Z)

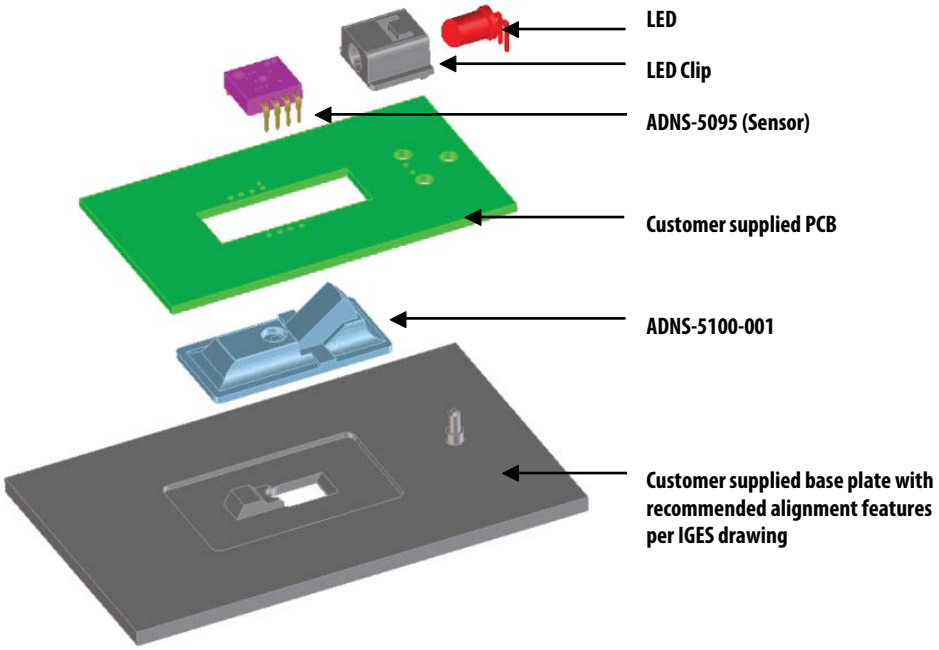


Figure 6. Exploded View of Assembly

PCB Assembly Considerations

1. Insert the sensor and all other electrical components into PCB.
2. Insert the LED into the assembly clip and bend the leads 90 degrees.
3. Insert the LED clip assembly into PCB.
4. This sensor package is only qualified for wave-solder process.
5. Wave solder the entire assembly in a no-wash solder process utilizing solder fixture. The solder fixture is needed to protect the sensor during the solder process. It also sets the correct sensor-to-PCB distance as the lead shoulders do not normally rest on the PCB surface. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact.
6. Place the lens onto the base plate.
7. Remove the protective kapton tape from optical aperture of the sensor. Care must be taken to keep contaminants from entering the aperture. Recommend not to place the PCB facing up during the entire mouse assembly process. Recommend to hold the PCB first vertically for the kapton removal process.
8. Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly. The sensor aperture ring should self-align to the lens.
9. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
10. Install mouse top case. There MUST be a feature in the top case to press down onto the PCB assembly to ensure all components are interlocked to the correct vertical height.

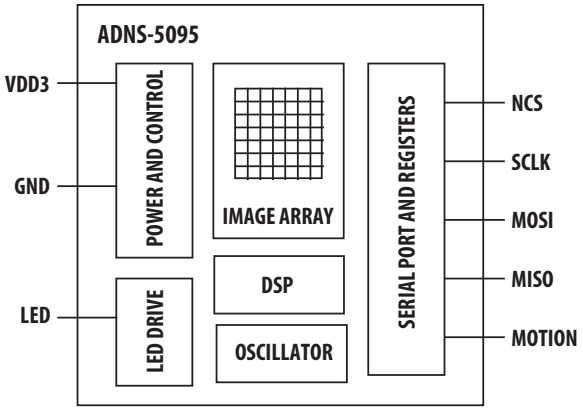


Figure 7. Block diagram of ADNS-5095 optical mouse

Recommended Typical Application (Receiver Side)

Recommended Typical Application (Transmitter Side)

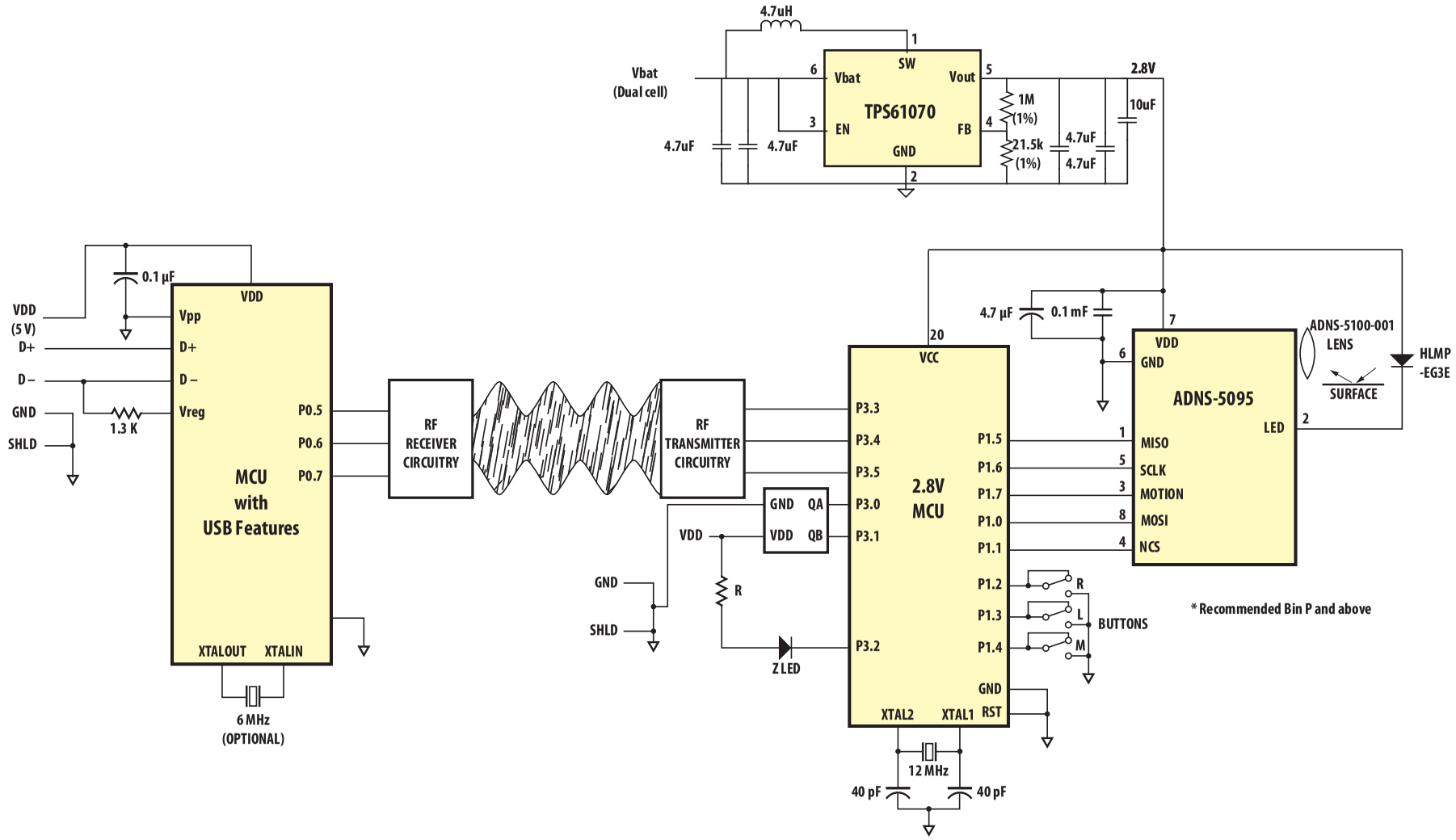


Figure 8. Schematic diagram for interface between ADNS-5095 and microcontroller (cordless application)

Design Considerations for Improved ESD Performance

For improved electrostatic discharge performance, typical creepage and clearance distance are shown in the table below. Assumption: base plate construction is as per the Avago Technologies supplied IGES file and ADNS-5100-001 trim lens. Note that the lens material is polycarbonate or polystyrene HH30. Therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should NOT be used.

	Typical Distance (mm)
	ADNS-5100-001
Creepage	15.43
Clearance	7.77

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- UL flammability level UL94 HB.

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Operating Temperature	T_A	-15	55	°C	
Lead Solder Temperature			260	°C	For 7 seconds, 1.6mm below seating plane.
Supply Voltage	V_{DD}	-0.5	3.7	V	
ESD (Human Body Model)			2	kV	All pins
Input Voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	All I/O pins
Output Current	Iout		7	mA	MISO pin

Table 2. Recommended Operating Condition

Parameter	Symbol	Min	Typ.	Max	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	2.8		3.0	V	
Power Supply Rise Time	T_{RT}	0.005		100	ms	0 to VDD min
Supply Noise (Sinusoidal)	V_{NA}			100	mVp-p	10kHz –50MHz
Serial Port Clock Frequency	f_{SCLK}			1	MHz	50% duty cycle
Distance from Lens Reference Plane to Tracking Surface (Z)	Z	2.3	2.4	2.5	mm	
Speed	S	0		30	ips	At default frame rate
Acceleration	a			8	G	At run mode
Load Capacitance	Cout			100	pF	MISO

Table 3. AC Electrical Specifications

Electrical characteristics over recommended operating conditions. Typical values at 25 °C, VDD = 2.8 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Motion Delay after Reset	$t_{MOT-RST}$			50	ms	From RESET register write to valid motion
Forced Rest Enable	$t_{REST-EN}$			1	s	From Rest Mode(RM) bits set to target rest mode
Wake from Forced Rest	$t_{REST-DIS}$			1	s	From Rest Mode(RM) bits cleared to valid motion
Power Down	t_{PD}			50	ms	From PD active (when bit 1 of register 0x0d is set) to low current
Wake from Power Down	t_{WAKEUP}	50		55	ms	From PD inactive (when write 0x5a to register 0x3a) to valid motion
MISO Rise Time	t_{r-MISO}		40	200	ns	C_L = 100 pF
MISO Fall Time	t_{f-MISO}		40	200	ns	C_L = 100 pF
MISO Delay after SCLK	$t_{DLY-MISO}$			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO Hold Time	$t_{hold-MISO}$	500		$1/f_{SCLK}$	ns	Data held until next falling SCLK edge
MOSI Hold Time	$t_{hold-MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI Setup Time	$t_{setup-MOSI}$	120			ns	From data valid to SCLK rising edge
SPI Time between Write Commands	t_{SWW}	30			µs	From rising SCLK for last bit of the first data byte, Commands to rising SCLK for last bit of the second data byte
SPI Time between Write and Read Commands	t_{SWR}	20			µs	From rising SCLK f or last bit of the first data byte, to rising SCLK for last bit of the second address byte
SPI Time between Read and Subsequent Commands	t_{SRW} t_{SRR}	250			ns	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the next address
SPI Read Address-Data Delay	t_{SRAD}	4			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read
NCS Inactive after Motion Burst	t_{BEXIT}	250			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK Active	$t_{NCS-SCLK}$	120			ns	From NCS falling edge to first SCLK falling edge
SCLK to NCS Inactive (for Read Operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK to NCS Inactive (for Write Operation)	$t_{SCLK-NCS}$	20			µs	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS to MISO high-Z	$t_{NCS-MISO}$			250	ns	From NCS rising edge to MISO high-Z state
Transient Supply Current	I_{DDT}			60	mA	Max supply current during a VDD ramp from 0 to VDD

Table 4. DC Electrical Specifications

Electrical characteristics over recommended operating conditions. Typical values at 25 °C, VDD = 2.8 V.

Parameter	Symbol	Min	Typ.	Max	Units	Notes
DC Supply Current in Various Mode	I_{DD_AVG}		8.23	20.41	mA	Average run current, including LED current, at max frame rate. No load on MISO
	I_{DD_REST1}		0.79	1.65	mA	
	I_{DD_REST2}		0.08	0.18	mA	
	I_{DD_REST3}		0.026	0.054	mA	
Power Down Current			10		µA	
Input Low Voltage	V_{IL}			0.5	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	Vdd-0.5			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		200		mV	SCLK, MOSI, NCS
Input leakage current	I_{leak}		±1	±10	µA	Vin=VDD-0.6V, SCLK, MOSI, NCS
Output Low Voltage	V_{OL}			0.7	V	Iout=1mA, MISO, MOTION
Output High Voltage	V_{OH}	Vdd-0.7			V	Iout=-1mA, MISO, MOTION
Input Capacitance	Cin		50		pF	MOSI, NCS, SCLK

Typical Performance Characteristics

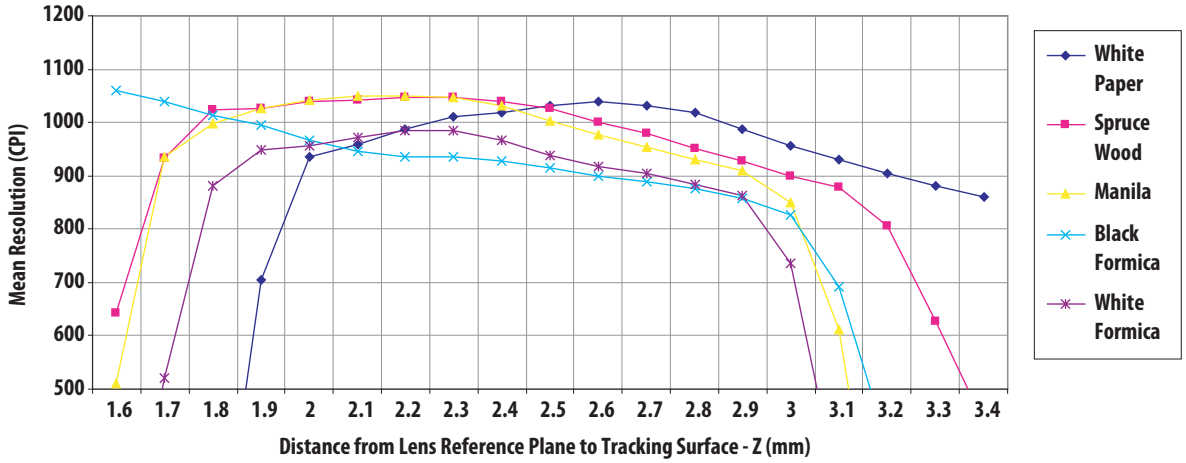


Figure 9. Mean resolution vs. distance from lens reference plane to surface.

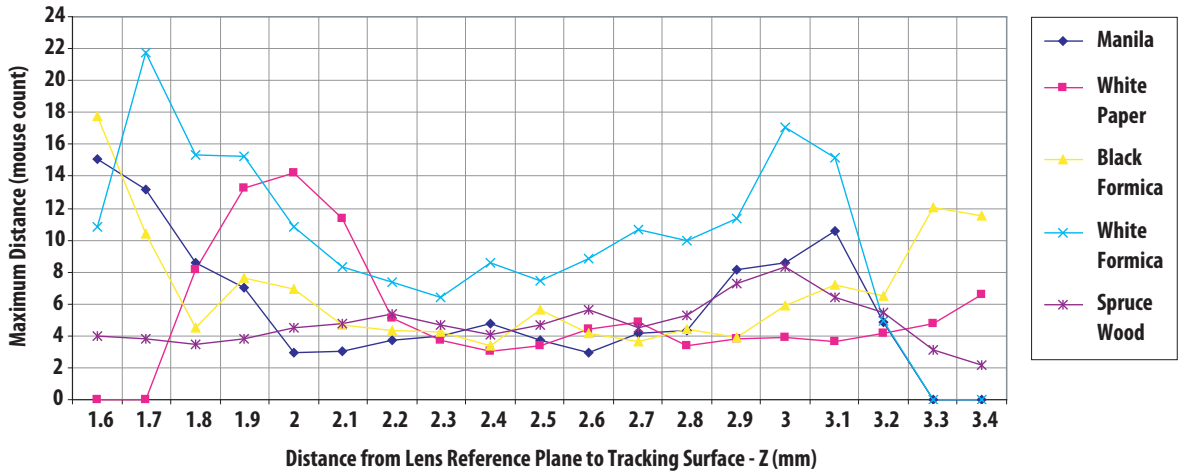


Figure 10. Typical path deviation.

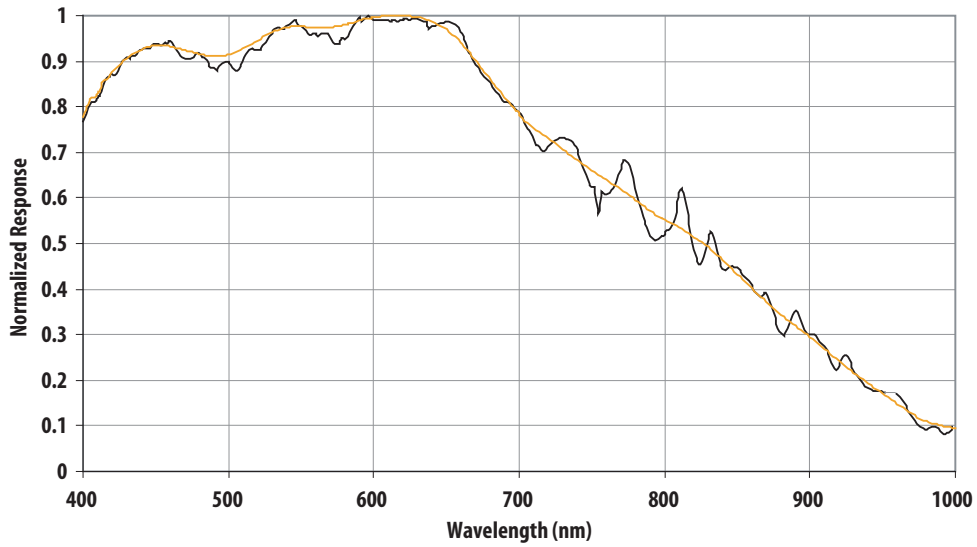


Figure 11. Relative wavelength responsivity.

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-5095, and to read out the motion information. The port is a four wire serial port. The host micro-controller always initiates communication; the ADNS-5095 never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is at tri-state.

The lines that comprise the SPI port:

SCLK: Clock input. It is always generated by the master (the micro-controller).

MOSI: Input data. (Master Out/Slave In)

MISO: Output data. (Master In/Slave Out)

NCS: Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

'Smart' LED Current Switching

ADNS-5095 is designed with 'smart' LED feature, an auto or self-adjusting LED current switching between the low and high current settings depending on the brightness of the tracking surface. If the surface is sufficiently bright to the sensor, lower LED current will be selected. When tracking on a darker surface, the higher current setting will be used. This feature is one of the power saving features in this sensor controlled by AUTO_LED_CTRL register (0x43).

Power Management Modes

The ADNS-5095 has three power-saving modes. Each mode has a different motion detection period with its respective response time to mouse motion. Response Time is the time taken for the sensor to 'wake up' from rest mode when motion is detected. When left idle, the sensor automatically changes or downshift from Run mode to Rest1, to Rest2 and finally to Rest3 which consumes the least current. Do note that current consumption is the lowest at Rest3 and highest at Rest1, however time required for sensor to respond to motion from Rest1 is the shortest and longest from Rest3. Downshift Time is the elapsed time (under no motion condition) from current mode to the next mode for example, it takes 10s for the sensor that is in Rest1 to change to Rest2. The typical response time and downshift time for each mode is shown in the following table. However, user can change the default time setting for each mode via register 0x0e through 0x13.

Mode	Response Time (Typical)	Downshift Time (Typical)
Rest 1	10ms	<1s
Rest 2	100 ms	9s
Rest 3	500 ms	430s

Another feature in ADNS-5095 that can be used to optimize the power consumption of the optical mouse system is the Motion Interrupt Output or MOTION pin (pin 3). It allows the host controller to be in sleep mode (or lowest operating current mode) when there is no motion detected after some time instead of consistently be in active mode and polling motion data from the sensor. When motion is detected, the sensor will send the motion interrupt signal through pin 3 to the controller to wake it up from sleep mode to resume its motion detection routine for navigation position and direction update.

MOTION Detection Routine

Typically in the motion detection routine, MCU will poll the sensor for valid motion data by checking on the MOTION_ST bit in MOTION_ST register. If MOTION_ST bit is set, motion data in DELTA_X and DELTA_Y is valid and ready to be read by the MCU.

MOTION Function

MOTION output signal (pin 3) can be used as interrupt input to the microcontroller of the mouse to trigger the controller to read the motion data from the sensor whenever there is motion detected by the sensor. The MOTION signal can be configured to be level or edge triggered, active high or low by setting the bits in MOTION_CTRL register.

For active high level-triggered configuration, the MOTION pin level will be driven high as long the MOTION bit in register 0x02 is set and there is motion data in DELTA_X and DELTA_Y registers ready to be read by the microcontroller. Once all the motion data has been read, DELTA_X and DELTA_Y values become zero, MOTION bit is reset and the MOTION pin level is driven low.

For active high edge-triggered configuration, a pulse of 230us will be sent through the MOTION pin when there is motion detected by the sensor during rest modes. The pulse can be used as interrupt input to activate the microcontroller from its sleep mode to enter into run mode to start polling the sensor for motion data by monitoring MOTION_ST bit (set whenever there is valid motion data) in MOTION register (0x02) and reading DELTA_X and DELTA_Y registers until MOTION_ST bit is reset.

Write Operation

Write operation, defined as data going from the micro-controller to the ADNS-5095, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate write sequence. The second byte contains the data. The ADNS-5095 reads MOSI on rising edges of SCLK.

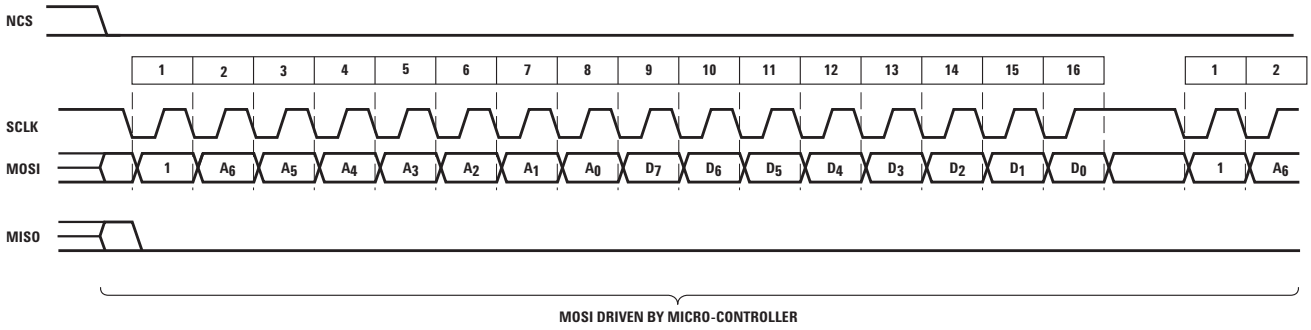


Figure 12. Write Operation

MOSI setup and hold time during write operation

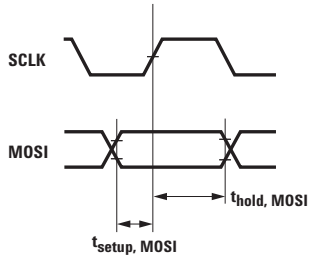


Figure 13. MOSI setup

Read Operation

A read operation, defined as data going from the ADNS-5095 to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-5095 over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

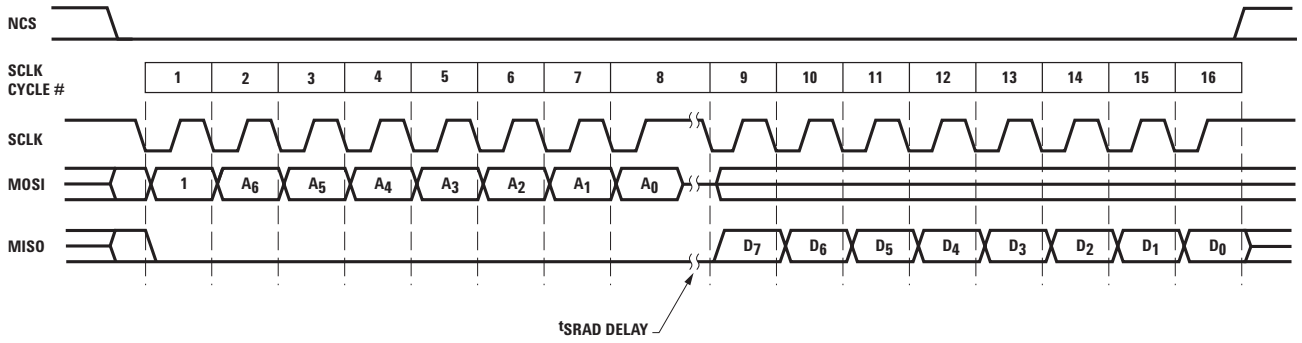


Figure 14. Read Operation

MOSI delay and hold time during read operation

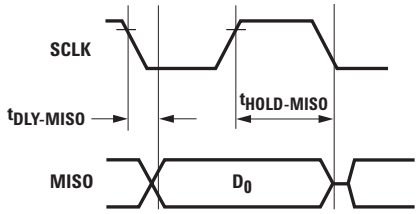


Figure 15. MISO delay

NOTE: The 500 ns minimum high state of SCLK is also the minimum MISO data hold time of the ADNS-5095. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-5095 will hold the state of data on MISO until the falling edge of SCLK.

Required Timing between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port.

Timing between Two Write Commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (t_{SWW}), then the first write command may not complete correctly.

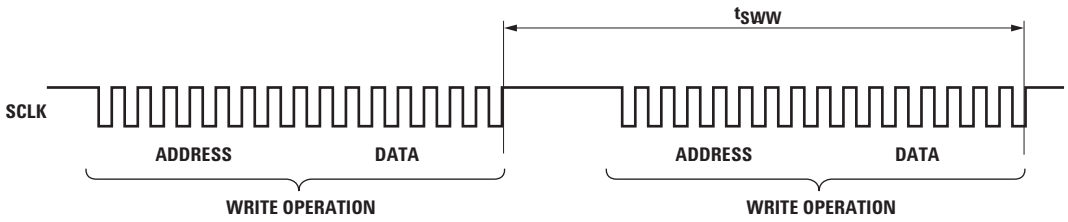


Figure 16. Timing between Two Write Commands

Timing between Write and Read Commands

If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (t_{SWR}), the write command may not complete correctly.

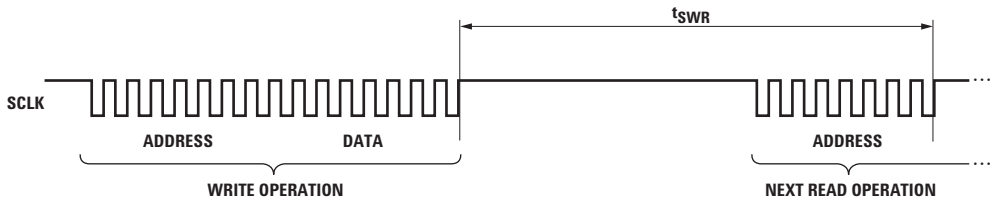


Figure 17. Timing between Write and Read Commands

Timing between Read and Subsequent Write or Read Commands

During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the ADNS-5095 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation.

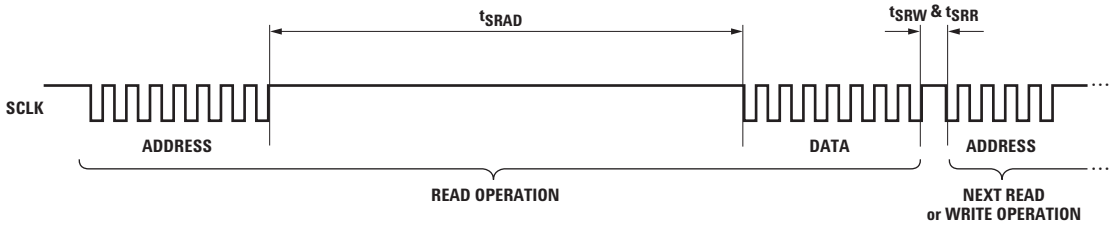


Figure 18. Timing between Read and Subsequent Write or Read Commands

Motion Burst Timing

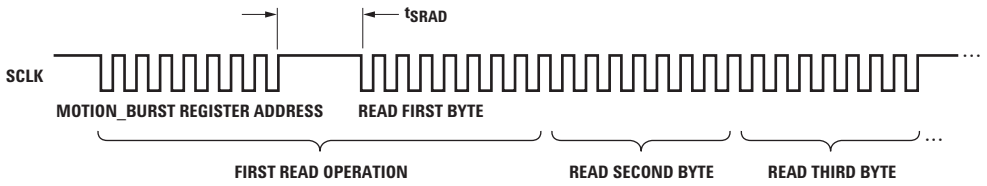


Figure 19. Motion Burst Timing

Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is initiated by reading the MOTION_BURST register (0x63). The ADNS-5095 will respond with the contents of the DELTA_X, DELTA_Y, SQUAL, SHUT_HI, SHUT_LO, and PIX_MAX and PIX_ACCUM registers in that order. The burst transaction can be terminated anywhere in the sequence after the DELTA_Y value by bringing the NCS pin high. The default "Read First Byte" is DELTA_X content and is specified in register 0x42 (BURST_READ_FIRST). The address that specifies the "Read First Byte" can be changed to address 0x00 – 0x02 (PROD_ID – MOTION_ST) or 0x05 – 0x08 (SQUAL – PIX_MAX) by writing to register 0x42.

After reading the MOTION_BURST address (0x63), the microcontroller must wait t_{SRAD} before starting to read the continuous data bytes. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

Prior to reading MOTION_BURST register (0x63), MOTION_ST bit in MOTION_ST register (0x02) should be read. Alternatively, read MOTION_BURST register (0x63) only after MOTION pin is triggered.

Avago Technologies highly recommends the usage of burst mode operation in optical mouse sensor design applications.

Power Up Reset

Although ADNS-5095 does have an internal power up self reset circuitry, it is still highly recommended to follow the power up sequence below:

i. Apply power

ii. Drive NCS high, then low to reset the SPI port.

iii. Write 0x5a to register 0x3a

iv. Write 0x80 to register 0x18

v. Write 0x04 to register 0x43

vi. Write 0x00 to register 0x22

Reset

ADNS-5095 can be reset by writing 0x5a to register 0x3a. A full reset will thus be executed and any register settings must be reloaded. The table below shows the state of the various pins during reset.

State of Signal Pins after VDD is Valid

Pin	During Reset	After Reset
NCS	Ignored	Functional
MISO	Low	Depends on NCS
SCLK	Ignored	Depends on NCS
MOSI	Ignored	Depends on NCS
XY_LED	High	Functional

Power Down

The ADNS-5095 can be set to Power Down mode by writing 0x02 to register 0x0d to disable the sensor. In addition, the SPI port should not be accessed during power down. Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted. The table below shows the state of various pins during power down. To exit Power Down, write 0x5a to register 0x3a to reset the sensor in order to wake it up. A full reset will thus be executed. Wait t_{WAKEUP} before accessing the SPI port. Any register settings must then be reloaded.

Pin	During Power Down
MOTION	Undefined
NCS	Functional*
MISO	Undefined
SCLK	Functional*
MOSI	Functional*
XY_LED	Low current

Notes:

* NCS pin must be held to 1 (HIGH) if SPI bus is shared with other devices. It can be in either state if the sensor is the only device in connected to the host micro-controller.

* Reading of registers should only be performed after exiting from the power down mode. Any read operation during power down will not reflect the actual data of the registers.

Startup Initialization

The commands below should be implemented in the startup initialization routine each time the sensor is reset:

- Write 0x80 to register 0x18
- Write 0x04 to register 0x43
- Write 0x00 to register 0x22

Registers

The ADNS-5095 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register Name	Register Description	Read/Write	Default Value
0x00	PROD_ID	Product ID	R	0x29
0x01	REV_ID	Revision ID	R	0x01
0x02	MOTION_ST	Motion Status	R	0x00
0x03	DELTA_X	Delta_X	R	0x00
0x04	DELTA_Y	Delta_Y	R	0x00
0x05	SQUAL	Squal Quality	R	0x00
0x06	SHUT_HI	Shutter Open Time (Upper 8-bit)	R	0x01
0x07	SHUT_LO	Shutter Open Time (Lower 8-bit)	R	0x00
0x08	PIX_MAX	Maximum Pixel Value	R	0x00
0x09	PIX_ACCUM	Average Pixel Value	R	0x00
0x0a	PIX_MIN	Minimum Pixel Value	R	0x00
0x0b	PIX_GRAB	Pixel Grabber	R/W	0x00
0x0d	MOUSE_CTRL	Mouse Control	R/W	0x01
0x0e	RUN_DOWNSHIFT	Run to Rest1 Time	R/W	0x46
0x0f	REST1_PERIOD	Rest1 Period	R/W	0x00
0x10	REST1_DOWNSHIFT	Rest1 to Rest2 Time	R/W	0x4f
0x11	REST2_PERIOD	Rest2 Period	R/W	0x09
0x12	REST2_DOWNSHIFT	Rest2 to Rest3 Time	R/W	0x2f
0x13	REST3_PERIOD	Rest3 Period	R/W	0x31
0x21	MOUSE_CTRL_EN	Mouse Control Enable Register	W	0x00
0x35	FRAME_IDLE	Frame Idle Setting	R/W	0xf0
0x3a	RESET	Reset	W	0x00
0x3f	NOT_REV_ID	Inverted Revision ID	R	0xfe
0x40	LED_CTRL	LED Control	R/W	0x00
0x41	MOTION_CTRL	Motion Control	R/W	0x40
0x42	BURST_READ_FIRST	Burst Read Starting Register	R/W	0x03
0x43	AUTO_LED_CTRL	AUTO LED Control	R/W	0x08
0x45	REST_MODE_CONFIG	Rest Mode Configuration	R/W	0x00
0x63	MOTION_BURST	Burst Read	R	0x00

PROD_ID Address: 0x00

Product ID Register

Access: Read Reset Value: 0x29

Bit	7	6	5	4	3	2	1	0
Field	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0

Data Type: 8-Bit unsigned integer

USAGE: This register contains a unique identification assigned to the ADNS-5095. The value in this register does not change; it can be used to verify that the serial communications link is functional. If using this register to verify serial communications link during rest modes, please read following registers in this sequence: 0x00, 0x02, 0x03, 0x04, 0x00 (regardless of register 0x02's status). If both or either one of the read 0x00 value is correct, no additional action is required as the serial communication link is good. Only if both read 0x00 value attempts are wrong, perform a reset operation to the sensor to restore the serial communications link.

Note: Highly recommended to use Motion pin function during rest modes for motion detection.

REV_ID Address: 0x01

Revision ID Register

Access: Read Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0

Data Type: 8-Bit unsigned integer

USAGE: This register contains the IC revision. It is subject to change when new IC versions are released.

MOTION_ST Address: 0x02

Motion Status Register

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MOTION_ST	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Data Type: Bit field.

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOTION_ST bit is set, then the user should read registers 0x03 (DELTA_X) and 0x04 (DELTA_Y) to get the accumulated motion data. Read this register before reading the DELTA_X and DELTA_Y registers. Writing any data into this register clears MOTION_ST bit, DELTA_X and DELTA_Y registers. However the written data byte will not be saved.

Bit	Field Name	Description
7	MOTION_ST	Motion detected since last report **0 = No motion (default)** 1 = Motion occurred, data in DELTA_X and DELTA_Y registers ready to be read
6-0	RSVD	Reserved

DELTA_X Address: 0x03

X Displacement Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	X7	X6	X5	X4	X3	X2	X1	X0

Data Type: Eight bit 2's complement number.

USAGE: X-axis movement in counts since last report. Absolute value is determined by resolution. Reading this register clears the content of this register.

NOTE: Registers 0x03 and 0x04 MUST be read consecutively.

DELTA_Y Address: 0x04

Y Displacement Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Data Type: Eight bit 2's complement number.

USAGE: Y-axis movement in counts since last report. Absolute value is determined by resolution. Reading this register clears the content of this register.

NOTE: Avago RECOMMENDS that registers 0x03 and 0x04 be read consecutively.

SQUAL Address: 0x05

Squal Quality Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	SQ7	SQ6	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0

Data Type: Upper 8 bits of a 9-bit unsigned integer.

USAGE: SQUAL (Surface Quality) is a measure of the number of valid features visible by the sensor in the current frame.

The maximum SQUAL register value is 255. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 800 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero, if there is no surface below the sensor. SQUAL is typically maximized when the navigation surface is at the optimum distance from the imaging lens (the nominal Z-height).

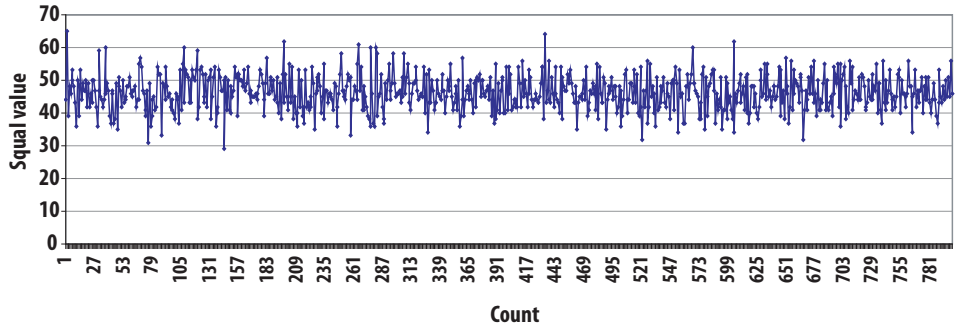


Figure 20. Squal values (white paper)

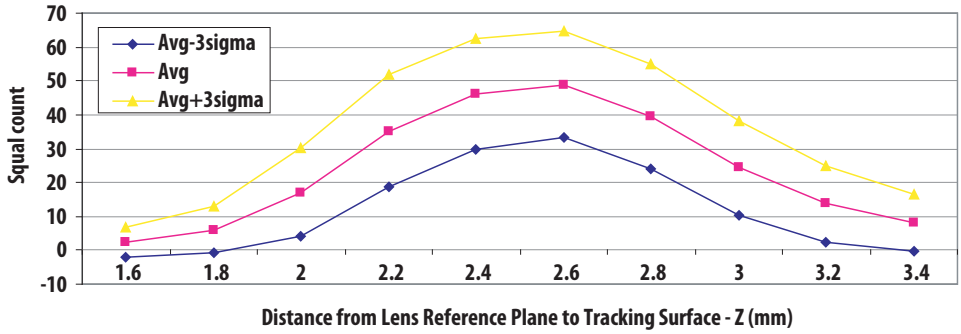


Figure 21. Mean squal vs. Z (White Paper)

SHUT_HI Address: 0x06

Shutter Open Time (Upper 8-bits) Register

Access: Read Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	S15	S14	S13	S12	S11	S10	S9	S8

SHUT_LO Address: 0x07

Shutter Open Time (Lower 8-bits) Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	S7	S6	S5	S4	S3	S2	S1	S0

Data Type: Sixteen bit unsigned integer.

USAGE: Units are in clock cycles. Read SHUT_HI first, then SHUT_LO. They should be read consecutively. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value is automatically adjusted.

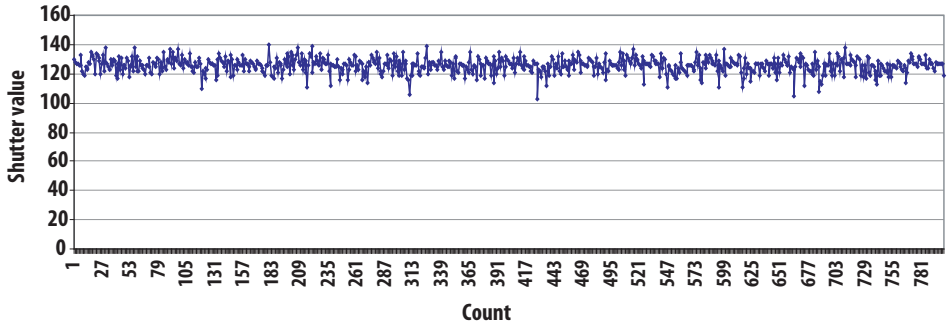


Figure 22. Shutter (white paper).

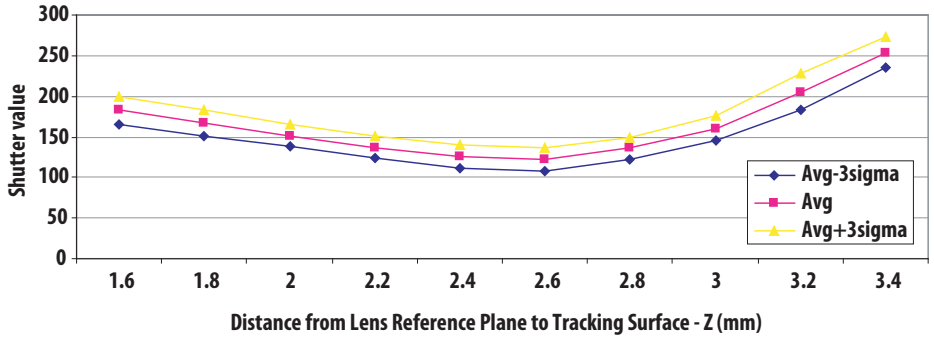


Figure 23. Mean shutter vs. Z (white paper).

PIX_MAX Address: 0x08

Maximum Pixel Value Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MP7	MP6	MP5	MP4	MP3	MP2	MP1	MP0

Data Type: Eight-bit number.

USAGE: Store the highest pixel value in current frame. Minimum value = 0, maximum value = 255. The highest pixel value may vary with different frame.

PIX_ACCUM Address: 0x09

Average Pixel Value Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	AP7	AP6	AP5	AP4	AP3	AP2	AP1	AP0

Data Type: High 8-bits of an unsigned 16-bit integer.

USAGE: This register stores the accumulated pixel value of the last image taken. This register can be used to find the average pixel value, where Average Pixel = (register value AP[7:0]) * 0.71

The maximum accumulated value is 45847 but only bits [15:8] are reported, therefore the maximum register value is 179. The minimum is 0. The PIX_ACCUM value may vary with different frame.

PIX_MIN Address: 0x0a

Minimum Pixel Value Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MP7	MP6	MP5	MP4	MP3	MP2	MP1	MP0

Data Type: Eight-bit number.

USAGE: Store the lowest pixel value in current frame. Minimum value = 0, maximum value = 127. The minimum pixel value may vary with different frame.

PIX_GRAB Address: 0x0b

Pixel Grabber Register

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	PG_VALID	PG6	PG5	PG4	PG3	PG2	PG1	PG0

Data Type: Eight bit word.

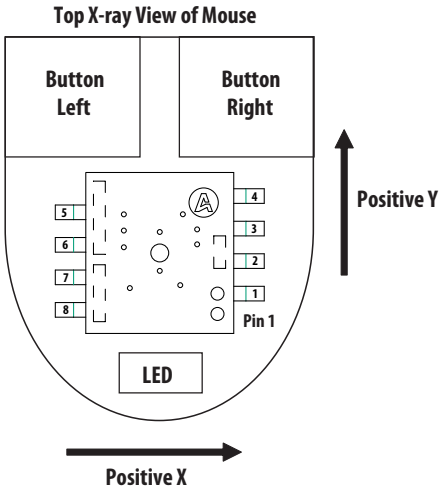
USAGE: The pixel grabber captures 1 pixel per frame. Bit-7 (MSB) of this register will be set to indicate that the 7-bit pixel data (PG[6:0]) is valid for grabbing. In a 19x19 pixel array, it will take 361 read operations to grab all the pixels to form the complete image.

Bit(s)	Field Name	Description
7	PG_VALID	Pixel Grabber Valid
6:0	PG[6:0]	Pixel Data

NOTE: Any write operation into this register will reset the grabber to origin (pixel 0 position). The sensor should not be moved before the 361 read operations are completed to ensure original data is grabbed to produce good (uncorrupted) image.

19x19 Pixel Array Address Map – (View from top of sensor)

	342	323	304	285	266	247	228	209	190	171	152	133	114	95	76	57	38	19	0 First
	343	324	305	286	267	248	229	210	191	172	153	134	115	96	77	58	39	20	1
	344	325	306	287	268	249	230	211	192	173	154	135	116	97	78	59	40	21	2
	345	326	307	288	269	250	231	212	193	174	155	136	117	98	79	60	41	22	3
	346	327	308	289	270	251	232	213	194	175	156	137	118	99	80	61	42	23	4
	347	328	309	290	271	252	233	214	195	176	157	138	119	100	81	62	43	24	5
	348	329	310	291	272	253	234	215	196	177	158	139	120	101	82	63	44	25	6
	349	330	311	292	273	254	235	216	197	178	159	140	121	102	83	64	45	26	7
	350	331	312	293	274	255	236	217	198	179	160	141	122	103	84	65	46	27	8
	351	332	313	294	275	256	237	218	199	180	161	142	123	104	85	66	47	28	9
	352	333	314	295	276	257	238	219	200	181	162	143	124	105	86	67	48	29	10
	353	334	315	296	277	258	239	220	201	182	163	144	125	106	87	68	49	30	11
	354	335	316	297	278	259	240	221	202	183	164	145	126	107	88	69	50	31	12
	355	336	317	298	279	260	241	222	203	184	165	146	127	108	89	70	51	32	13
	356	337	318	299	280	261	242	223	204	185	166	147	128	109	90	71	52	33	14
	357	338	319	300	281	262	243	224	205	186	167	148	129	110	91	72	53	34	15
	358	339	320	301	282	263	244	225	206	187	168	149	130	111	92	73	54	35	16
	359	340	321	302	283	264	245	226	207	188	169	150	131	112	93	74	55	36	17
Last	360	341	322	303	284	265	246	227	208	189	170	151	132	113	94	75	56	37	18



MOUSE_CTRL Address: 0x0d

Mouse Control Register

Access: Read/Write Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RES_EN	RES2	RES1	RES0	PD	RES_D

Data Type: Bit field

USAGE: Resolution and chip reset information can be accessed or to be edited by this register.

Bit(s)	Field Name	Description
7:6	RSVD	Reserved
5	RES_EN	Enable resolution settings set on MOUSE_CTRL [4:2]
4:2	RES [2:0]	Resolution **000: 1000 dpi (default)** 001: 250 dpi 010: 500 dpi 011: 1250 dpi 100: 1500 dpi 101: 1750 dpi
1	PD	Power Down
0	RES_D	0: 500 dpi **1: 1000 dpi (default)**

NOTE:
1. Setting MOUSE_CTRL [5] bit to '1' will supersede and ignore MOUSE_CTRL [0] setting.
2. Each read/write operation of this register should be followed by a write operation: write register 0x21 with 0x10

RUN_DOWNSHIFT Address: 0x0e

Run to Rest1 Time Register

Access: Read/Write Reset Value: 0x46

Bit	7	6	5	4	3	2	1	0
Field	RUD7	RUD6	RUD5	RUD4	RUD3	RUD2	RUD1	RUD0

Data Type: Eight bit number

USAGE: This register sets the Run to Rest1 mode downshift time. The time is the value of this register multiply by 16 frames. Min value for this register must be 1.

For example at typical frame rate of 2250fps, each frame period is about 444us. Therefore the run downshift time would be Register value (0x46) * 16 * frame period = 70 * 16 * 444us = 497.3ms

REST1_PERIOD Address: 0x0f

Rest1 Period Register

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	R1P7	R1P6	R1P5	R1P4	R1P3	R1P2	R1P1	R1P0

Data Type: Eight bit number

USAGE: This register sets the Rest1 period. Period = (register value R1P [7:0] +1) x 7ms (typical slow clock period). Min value for this register is 0. Max value is 0xFD.

NOTE: Writing into this register when the sensor itself is operating in this rest mode may result in unexpected behavior of the sensor. To avoid this from happening, below commands should be incorporated prior and after the write command into this register.

w 22 80 -> write 0x80H into register 0x22H prior to writing into this register

w 0f XX -> writing into this register

w 22 00 -> write 0x00H into register 0x22H after writing into this register

REST1_DOWNSHIFT Address: 0x10

Rest1 to Rest2 Downshift Time Register

Access: Read/Write Reset Value: 0x4f

Bit	7	6	5	4	3	2	1	0
Field	R1D7	R1D6	R1D5	R1D4	R1D3	R1D2	R1D1	R1D0

Data Type: Eight bit number

USAGE: This register sets the Rest1 to Rest2 mode downshift time. Time = (register value R1D [7:0]) x (Rest1 period) x 16. Min value for this register is 0.

REST2_PERIOD Address: 0x11

Rest2 Period Register

Access: Read/Write Reset Value: 0x09

Bit	7	6	5	4	3	2	1	0
Field	R2P7	R2P6	R2P5	R2P4	R2P3	R2P2	R2P1	R2P0

Data Type: Eight bit number

USAGE: This register sets the Rest2 period. Period = (register value R2P [7:0] +1) x 7ms (typical slow clock period). Min value for this register is 0. Max value is 0xFD.

NOTE: Writing into this register when the sensor itself is operating in this rest mode may result in unexpected behavior of the sensor. To avoid this from happening, below commands should be incorporated prior and after the write command into this register.

w 22 80 -> write 0x80H into register 0x22H prior to writing into this register

w 11 XX -> writing into this register

w 22 00 -> write 0x00H into register 0x22H after writing into this register

REST2_DOWNSHIFT Address: 0x12

Rest2 to Rest3 Downshift Time Register

Access: Read/Write Reset Value: 0x2f

Bit	7	6	5	4	3	2	1	0
Field	R2D7	R2D6	R2D5	R2D4	R2D3	R2D2	R2D1	R2D0

Data Type: Eight bit number

USAGE: This register sets the Rest1 to Rest2 mode downshift time. Time = (register value R2D [7:0]) x (Rest2 period) x 128. Min value for this register is 0.

REST3_PERIOD Address: 0x13

Rest3 Period Register

Access: Read/Write Reset Value: 0x31

Bit	7	6	5	4	3	2	1	0
Field	R3P7	R3P6	R3P5	R3P4	R3P3	R3P2	R3P1	R3P0

Data Type Eight bit number

USAGE: This register sets the Rest3 period. Period = (register value R3P [7:0] +1) x 7ms (typical slow clock period). Min value for this register is 0. Max value is 0xFD.

NOTE: Writing into this register when the sensor itself is operating in this rest mode may result in unexpected behavior of the sensor. To avoid this from happening, below commands should be incorporated prior and after the write command into this register.

w 22 80 -> write 0x80H into register 0x22H prior to writing into this register

w 13 XX -> writing into this register

w 22 00 -> write 0x00H into register 0x22H after writing into this register

MOUSE_CTRL_EN Address: 0x21

Mouse Control Enable Register

Access: Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MCE7	MCE6	MCE5	MCE4	MCE3	MCE2	MCE1	MCE0

Data Type: Eight bit unsigned integer.

USAGE: Write 0x10 to this register after accessing register 0x0d to complete read/write operations.

FRAME_IDLE Address: 0x35

Frame Idle Setting Register

Access: Read/Write Reset Value: 0xf0

Bit	7	6	5	4	3	2	1	0
Field	1	1	FR5	FR4	FR3	FR2	FR1	FR0

Data Type: Eight bit unsigned integer.

USAGE : This register is used to control the frame rate. The value in this register is used to add frame idling time, which effectively reduces the frame rate..

frame_idle_time (in clock counts) = (register value) * 32

Frame period (in clock counts) = shutter_time (reg 0x06 and reg 0x07) + (3400 clocks) + frame_idle_time

When this register is set to 0xf0, the typical frame rate is about 2250 fps @26MHz

RESET Address: 0x3a

Reset Register

Access: Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RST7	RST6	RST5	RST4	RST3	RST2	RST1	RST0

Data Type: Eight bit unsigned integer.

USAGE: This register is used as chip reset by writing 0x5a into this register.

NOT_REV_ID Address: 0x3f

Inverted Revision ID Register

Access: Read Reset Value: 0xfe

Bit	7	6	5	4	3	2	1	0
Field	RRID7	RRID6	RRID5	RRID4	RRID3	RRID2	RRID1	RRID0

Data Type: Eight bit unsigned integer

USAGE: This register contains the inverse of the revision ID which is located at register 0x01.

LED_CTRL Address: 0x40

LED Control Register

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	LCOF	RSVD	LSEL1	LSEL0

Data Type: Eight bit unsigned integer

USAGE: This register is used to control the LED operating mode and current to optimize/minimize the power consumption.

Bit	Field Name	Description
7:4	RSVD	Reserved
3	LCOF	**0 : Normal operation (default)** 1 : LED Continuous Off
2	RSVD	Reserved
1:0	LSEL[1:0]	**0x0: LED Current set to 20mA (default)** 0x1: LED Current set to 15mA 0x2: LED Current set to 36mA 0x3: LED Current set to 30mA

NOTE: If LED is operating in AUTO current switching mode (AUTO_LED_CONTROL [0] at address 0x43 is cleared, LED current setting (LED_CONTROL [1:0]) will be ignored. Only when AUTO current switching is disabled through setting AUTO_LED_CONTROL [0], the LED drive current is determined by LED_CONTROL [1:0]

MOTION_CTRL Address: 0x41

Motion Control Register

Access: Read/Write Reset Value: 0x40

Bit	7	6	5	4	3	2	1	0
Field	MOT_A	MOT_S	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Data Type: Eight bit unsigned integer

USAGE: This register is used to set the feature of MOTION interrupt output. If MOT_S bit is clear, the MOTION pin is level-sensitive. With active low (MOT_A bit is clear) level-sensitive configuration, the MOTION pin will be driven low when there is motion detected indicating there is motion data in DELTA_X and DELTA_Y registers. The mouse microcontroller can read MOTION_ST register, DELTA_X register, and then DELTA_Y register sequentially. After all the motion data has been read, DELTA_X and DELTA_Y registers will be zero, the MOTION pin will be driven high by the sensor.

If MOT_S is set, the MOTION pin is edge sensitive. If MOT_A is also set, it means active high or rising edge triggered. Whenever there is motion detected by the sensor, a pulse (~230us) will be sent out through this pin. This pulse can be used to trigger or wake the controller up from its sleep mode to read motion data from the sensor. The controller can then read MOTION_ST register, DELTA_X register, and then DELTA_Y register sequentially. (Refer to Motion Function for more information)

Bit	Field Name	Description
7	MOT_A	MOTION Active **0 : LOW (default)** 1 : HIGH
6	MOT_S	MOTION Sensitivity 0 : Level sensitive **1 : Edge sensitive (default)**
5:0	RSVD	Reserved

BURST_READ_FIRST Address: 0x42

Burst Read Starting Address Register

Access: Read/Write Reset Value: 0x03

Bit	7	6	5	4	3	2	1	0
Field	BM7	BM6	BM5	BM4	BM3	BM2	BM1	BM0

Data Type: Eight bit unsigned integer

USAGE: This register provides the starting register address the sensor will read during Burst Mode. For more information, refer to Burst Mode Operation.

Note: To change the burst mode starting address from default (DELTA_X or 0x03) pull the NCS low, set the BURST_READ_FIRST register with the burst mode starting address, read register 0x63 for burst reads, and terminate the burst reads by pulling NCS high. This must be repeated each time when performing burst reads with address other than default.

AUTO_LED_CTRL Address: 0x43

AUTO LED Control

Access: Read/Write Reset Value: 0x08

Bit	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	LED_HI [1]	LED_HI [0]	LED_LO	A_LED_DIS

Data Type: Eight bit unsigned integer

USAGE: This register enables AUTO LED current switching. This is a 'smart' LED feature whereby the LED current is self adjusting between the low and high current settings (bit 3:1) according to the brightness of the tracking surface if this feature is enabled (via clearing bit 0). The brighter the surface, the lower the LED current will be. If A_LED_DIS (bit 0) is set, this means AUTO LED mode is disabled, then the LED current is determined by LSEL[1:0] setting in LED_CTRL register (0x40).

Bit	Field Name	Description
7:4	RSVD	Reserved
3:2	LED_HI [1:0]	AUTO LED High Current 0x0: Auto LED high current is 15mA 0x1: Auto LED high current is 20mA **0x2: Auto LED high current is 30mA (default)** 0x3: Auto LED high current is 36mA
1	LED_LO	AUTO LED Low Current **0: Auto LED low current is 15mA (default)** 1: Auto LED low current is 20mA
0	A_LED_DIS	AUTO LED Disable **0: AUTO LED enabled (default)** 1: AUTO LED disabled

Note: When AUTO LED is enabled, the AUTO LED current will be switched between low and high current setting determined by LED_LO and LED_HI [1:0]. If LED_LO current setting is higher than the LED_HI, the current will be based on the higher setting. For example if LED_LO is 20mA and LED_HI is 15mA, the AUTO LED current will be fixed at 20mA.

REST_MODE_CONFIG Address: 0x45

Rest Mode Configuration Register

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RM1	RM0	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Data Type: Eight bit unsigned integer

USAGE: This register is used to set the operating mode of the ADNS-5095.

Bit	Field Name	Description
7:6	RM[1:0]	Sensor Operating Mode **0x00: Normal (default)** 0x01: Rest 1 0x02: Rest 2 0x03: Rest 3
5:0	RSVD	Reserved

Read operation to REST_MODE_CONFIG indicates which mode the sensor is in. Write operation into this register will force the sensor into rest modes (Rest 1, 2 or 3). Write the value 0x40 into 0x45 register to force sensor into Rest 1, 0x80 to Rest 2 or 0xC0 to Rest 3. To get out of any forced rest mode, write 0x00 into this register to set back to normal mode.

Note: Write 0x00 to register 0x22 during start up sensor initialization to enable configuration to this register.

MOTION_BURST Address: 0x63

Burst Read Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0

Data Type: Various.

USAGE: This register is used to enable burst mode. Burst is initiated by a read of this register, which will then return continuous data starting from the address stored in BURST_READ FIRST register through register 0x09. If burst operation is not terminated at this point, the internal address counter stops incrementing and register 0x09 value will be returned repeatedly. Burst operation is terminated when NCS is asserted high. For more information, refer to Burst Mode Operation.

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