Integrated Circuit Systems, Inc.

ICS8431-11

255MHz, Low Jitter, LVPECL Frequency Synthesizer

General Description

The ICS8431-11 is a general purpose clock frequency synthesizer for IA64/32 application and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The VCO operates at a frequency range of 190MHz to 510MHz providing an output frequency range of 95MHz to 255MHz. The output frequency can be programmed using the parallel interface, M0 thru M8, to the configuration logic. Spread spectrum clocking is programmed via the control inputs SSC_CTL0 and SSC_CTL1.

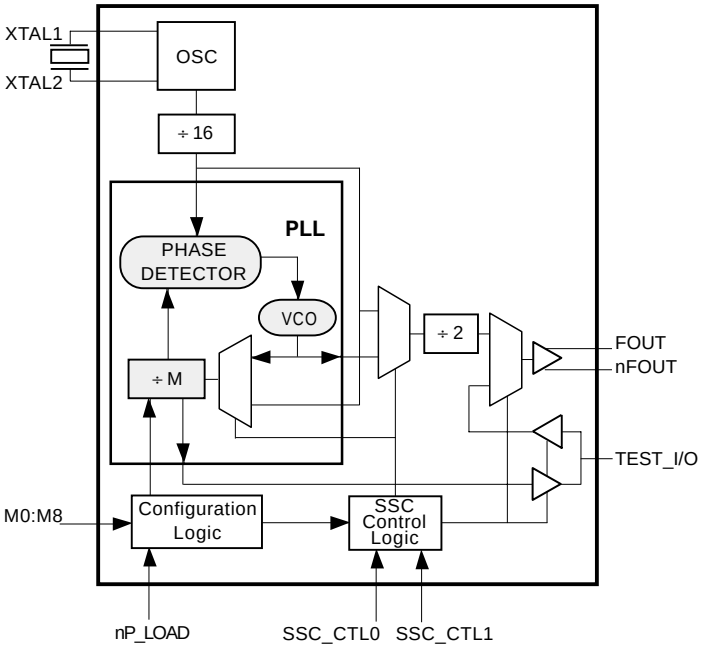
Programmable features of the ICS8431-11 support four operational modes. The four modes are spread spectrum clocking (SSC), non-spread spectrum clock and two test modes which are controlled by the SSC_CTL[1:0] pins. Unlike other synthesizers, the ICS8431-11 can immediately change spread-spectrum operation without having to reset the device.

In SSC mode, the output clock is modulated in order to achieve a reduction in EMI. In one of the PLL bypass test modes, the PLL is disconnected as the source to the differential output allowing an external source to be connnected to the TEST_I/O pin. This is useful for in-circuit testing and allows the differential output to be driven at a lower frequency throughout the system clock tree. In the other PLL bypass mode, the oscillator divider is used as the source to both the M and the Fout divide by 2. This is useful for characterizing the oscillator and internal dividers.

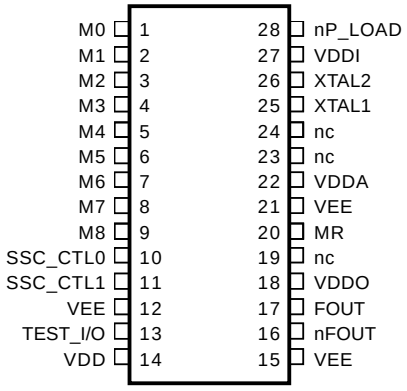
Features

- Fully integrated PLL
- Differential 3.3V LVPECL output
- Programmable PLL loop divider for generating a variety of output frequencies.
- Crystal oscillator interface
- Spread Spectrum Clocking (SSC) fixed at 1/2% modulation for environments requiring ultra low EMI
- Typical RMS cycle-to-cycle jitter 2.6 ps
- LVTTL / LVCMOS control inputs
- PLL bypass modes supporting in-circuit testing and on-chip functional block characterization
- 3.3V supply voltage
- 28 lead SOIC
- 0°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



ICS8431-11
28-Lead SOIC
M Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1 - 5	M0-M6	Input	Pulldown	M divider inputs. Data latched on LOW-to-HIGH transistion of nP_LOAD input. LVCMOS / LVTTL pins interface levels.
6 - 8	M7-M8	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transistion of nP_LOAD input. LVCMOS / LVTTL pins interface levels.
10, 11	SSC CTL0, SSC CTL1	Input	Pullup	SCC control pins. LVTTL / LVCMOS interface levels.
12	VEE	Power		Ground pin for core and test output.
13	TEST I/O	Input / Output		Programmed as input in PLL bypass mode.
14	VDD	Power		Power supply pin for core and test output.
15	VEE	Power		Ground pin for output.
16, 17	nFOUT, FOUT	Output		These differential outputs are main output drivers for the synthesizer. They are compatible with terminated positive referenced LVPECL logic.
18	VDDO	Power		Power supply pin for output.
19, 23, 24	nc	Unused		No connection.
20	MR	Input	Pulldown	Reset M counter. Forces FOUT low.
21	VEE	Power		Ground pin.
22	VDDA	Power		PLL power supply pin.
25, 26	XTAL1, XTAL2	Input		Crystal oscillator input.
27	VDDI	Power		Power supply pin for core.
28	nP_LOAD	Input	Pulldown	M divider latch enable input. LVTTL / LVCMOS interface levels.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Pin Capacitance				4	pF
RPULLUP	Input Pullup Resistor			51		KΩ
RPULLDOWN	Input Pulldown Resistor			51		KΩ

Table 3A. SSC Control Input Function Table

Inputs		TEST_I/O Source	SSC	Outputs		Operational Modes
SSC_CTL1	SSC_CTL0			FOUT, nFOUT	TEST_I/O	
0	0	Internal	Disabled	fXTAL ÷ 32	fXTAL ÷ 16 ÷ M	PLL bypass; Oscillator, oscillator, M and N dividers test mode. NOTE 1
0	1	PLL	Enabled	$\frac{fXTAL \times M}{32}$	Hi-Z	Default SSC; Modulation Factor = ½ Percent
1	0	External	Disabled	Test Clk	Input	PLL Bypass Mode, (1MHz≤ Test Clk ≤ 200MHz); NOTE 1
1	1	PLL	Disabled	$\frac{fXTAL \times M}{32}$	Hi-Z	No SSC Modulation

NOTE 1: Used for in house debug and characterization.

Table 3B. Programmable VCO Frequency Function Table (NOTE 1)

VCO Frequency (MHz)	M Count	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
190	190	0	1	0	1	1	1	1	1	0
191	191	0	1	0	1	1	1	1	1	1
192	192	0	1	1	0	0	0	0	0	0
193	193	0	1	1	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
508	508	1	1	1	1	1	1	1	0	0
509	509	1	1	1	1	1	1	1	0	1
510	510	1	1	1	1	1	1	1	1	0

NOTE 1: Assumes a 16MHz crystal.

Absolute Maximum Ratings

Supply Voltage	4.6V
Inputs	-0.5V to VDD + 0.5V
Outputs	-0.5V to VDDO + 0.5V
Ambient Operating Temperature	0°C to 85°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, VDD = VDDA = VDDI = VDDO = 3.3V±5%, T_A = 0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDD	Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		3.135	3.3	3.465	V
VDDA	Analog Power Supply Voltage		3.135	3.3	3.465	V
VDDI	Input Power Supply Voltage		3.135	3.3	3.465	V
IEE					140	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, VDD = VDDA = VDDI = VDDO = 3.3V±5%, T_A = 0°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	M0:M8, SSC_CTL0, SSC_CTL1, MR, TEST_I/O, nP_LOAD	3.135V ≤ VDD ≤ 3.465V	2		VDD + 0.3	V
VIL	Input Low Voltage	M0:M8, SSC_CTL0, SSC_CTL1, MR, TEST_I/O, nP_LOAD	3.135V ≤ VDD ≤ 3.465V	-0.3		0.8	V
IIH	Input High Current	M7, M8, SSC_CTL0, SSC_CTL1, TEST_IO	VDD = VIN = 3.465V			5	µA
		M0:M6, nP_LOAD, MR	VDD = VIN = 3.465V			150	µA
IIL	Input Low Current	M7, M8, SSC_CTL0, SSC_CTL1, TEST_IO	VDD = 3.465V, VIN = 0V	-150			µA
		M0:M6, nP_LOAD, MR	VDD = 3.465V, VIN = 0V	-5			µA

Table 4C. LVPECL DC Characteristics, VDD = VDDA = VDDI = VDDO = 3.3V±5%, T_A = 0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VOH	Output High Voltage; NOTE 1		VDDO - 1.28		VDDO - 0.98	V
VOL	Output Low Voltage; NOTE 1		VDDO - 2.0		VDDO - 1.7	V
VSWING	Peak-to-Peak Output Voltage Swing		600	700	850	mV

NOTE 1: Output terminated with 50Ω to VDDO - 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			16.0		MHz
Frequency Tolerance		-50		+50	ppm
Frequency Stability		-100		+100	ppm
Drive Level				100	µW
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance		3		7	pF
Load Capacitance		10	18	32	pF
Series Pin Inductance		3		7	nH
Operating Temperature Range		0		70	°C
Aging	Per year @25°C	-5		+5	ppm

Table 6. AC Characteristics, VDD = VDDA = VDDI = VDDO = 3.3V±5%, T_A = 0°C to 85°C, 16MHz Crystal

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Fave	Average Output Frequency; NOTE 4		-750		+750	ppm
$t_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 2	FOUT = 200 MHz		18	30	ps
					35	ps
odc	Output Duty Cycle; NOTE 2		47		53	%
tR	Output Rise Time; NOTE 1, 2	20% to 80%	300	450	600	ps
tF	Output Fall Time; NOTE 1, 2	20% to 80%	300	450	600	ps
Fxtal	Crystal Input Range; NOTE 3		14	16	20	MHz
Fm	SSC Modulation Frequency; NOTE 1, 2		30		33.33	KHz
Fmf	SSC Modulation Factor; NOTE 1, 2			0.4	0.6	%
SSCred	Spectral Reduction; NOTE 1, 2		7	10		dB
tSTABLE	Power-up to Stable Clock Output				10	ms

NOTE 1: Spread Spectrum clocking enabled.
NOTE 2: Outputs terminated with 50Ω to VDDO - 2V.
NOTE 3: Only valid within the VCO operating range.
NOTE 4: Without external crystal components.
$t_{jit(cc)}$, tR, tF, odc conform to JEDEC JESD65 definitions.

Parameter Measurement Information

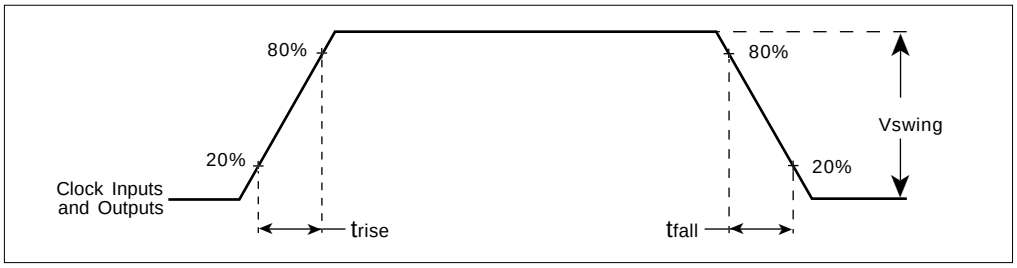


Figure 1 — Input and Output Slew Rates

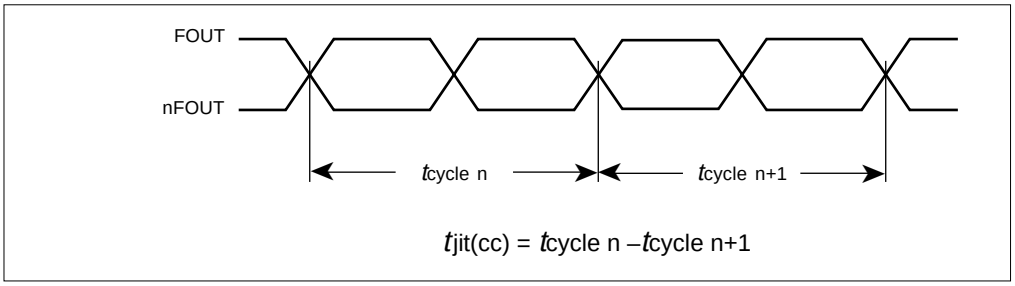


Figure 2 — Cycle-to-Cycle Jitter

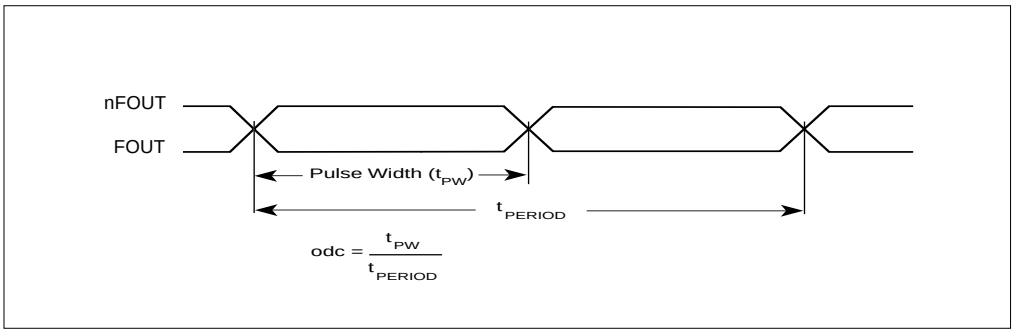


Figure 3 — odc & *t*PERIOD

Functional Description

The ICS8431-11 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A 16MHz series-resonant, fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector. With a 16MHz crystal this provides a 1MHz reference frequency. The VCO of the PLL operates over a range of 190 to 510MHz. The output of the loop divider is also applied to the phase detector.

The phase detector and the loop filter force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to the LVPECL output buffer. The divider provides a 50% output duty cycle.

The programmable features of the ICS8431-11 support four output operational modes and a programmable PLL loop divider. The four output operational modes are spread spectrum clocking (SSC), non-spread spectrum clock and two test modes and are controlled by the SSC_CTL[1:0] pins.

The PLL loop divider or M divider is programmed by using inputs M0 through M8. While the nP_LOAD input is held LOW, the data present at M0:M8 is transparent to the M-divider. On the LOW-to-HIGH transition of nP_LOAD, the M0:M8 data is latched into the M-divider and any further changes at the M0:M8 inputs will not be seen by the M-divider until the next LOW transition on nP_LOAD.

The relationship between the VCO frequency, the crystal frequency and the loop counter/divider is defined as follows:

$$fVCO = \frac{fxtal}{16} \times M$$

The M count and the required values of M0:M8 for programming the VCO are shown in *Table 3B*, Programmable VCO Frequency Function Table. The frequency out is defined as follows:

$$FOUT = \frac{fVCO}{2} = \frac{fxtal \times M}{32}$$

For the ICS8431-11, the output divider equals 2. Valid M values for which the PLL will achieve lock are defined as $190 \leq M \leq 510$.

Crystal Input and Oscillator Interface

The ICS8431-11 features an internal oscillator that uses an external quartz crystal as the source of its reference frequency. A 16MHz crystal divided by 16 before being sent to the phase detector provides the reference frequency. The oscillator is a series resonant, multi-vibrator type design. This design provides better stability and eliminates the need for large on chip capacitors. Though a series resonant crystal is preferred, a parallel resonant crystal can be used. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified. A few hundred ppm translates to KHz inaccuracy. In general computing applications this level of inaccuracy is irrelevant. If better ppm accuracy is required, an external capacitor can be added to a parallel resonant crystal in series to pin 25. *Figure 1A* shows how to interface with a crystal.

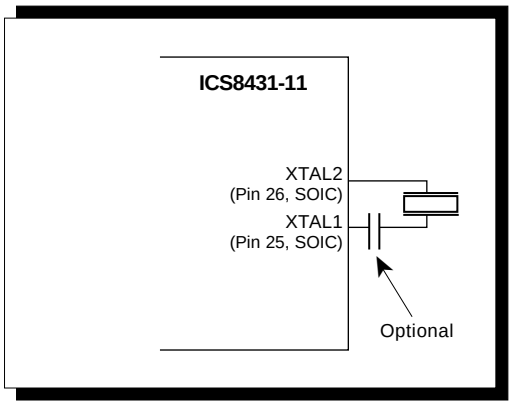


Figure 1A. Crystal Interface

Figures 1A, 1B, and 1C show various crystal parameters which are recommended only as guidelines. Figure 1A shows how to interface a capacitor with a parallel resonant crystal. *Figure 1B* shows the capacitor value needed for the optimum PPM performance over various parallel resonant crystals. *Figure 1C* shows the recommended tuning capacitance for a various parallel resonant crystal.

Figure 1B. Recommended tuning capacitance for various parallel resonant crystals.

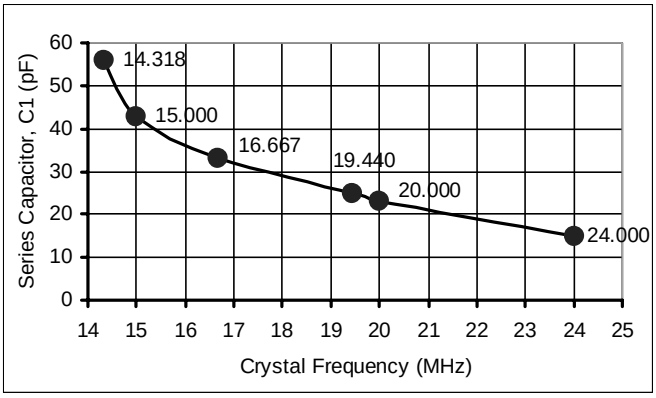
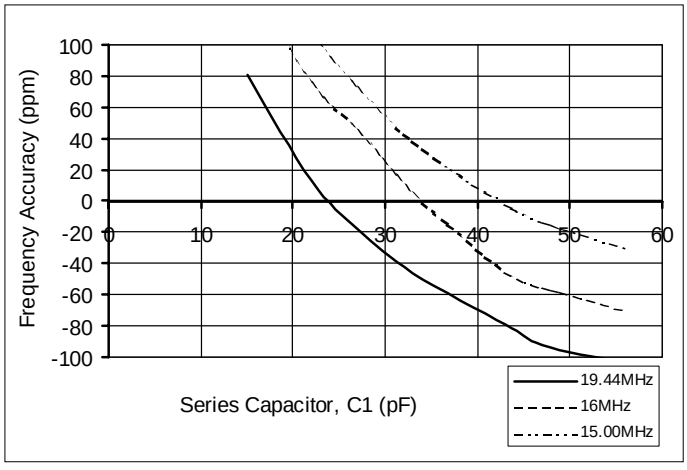


Figure 1C. Recommended tuning capacitance for various parallel resonant crystal.



Spread Spectrum

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 30KHz triangle waveform is used with 0.5% down-spread (+0.0% / -0.5%) from the nominal 200MHz clock frequency. An example of a triangle frequency modulation profile is shown in *Figure 2* below. The ramp profile can be expressed as:

- Fnom = Nominal Clock Frequency in Spread OFF mode (200MHz with 16MHz IN)
- Fm = Nominal Modulation Frequency (30KHz)
- δ = Modulation Factor (0.5% down spread)

$(1 - \delta)$ fnom + 2 fm x δ x fnom x t when $0 < t < \frac{1}{2\,fm}$,

$(1 - \delta)$ fnom - 2 fm x δ x fnom x t when $\frac{1}{2\,fm} < t < \frac{1}{fm}$

The ICS8431-11 triangle modulation frequency deviation will not exceed 0.6% down-spread from the nominal clock frequency (+0.0% / -0.5%). An example of the amount of down spread relative to the nominal clock frequency can be seen in the frequency domain, as shown in *Figure 3.* The ratio of this width to the fundamental frequency is typically 0.4%, and will not exceed 0.6%. The resulting spectral reduction will be greater than 7dB, as shown in Figure 3. It is important to note the ICS8431-11 7dB minimum spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

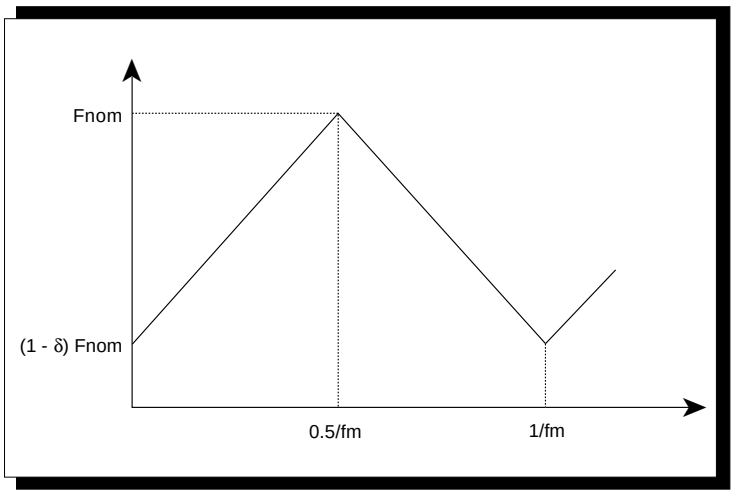


Figure 2. Triangle Frequency Modulation

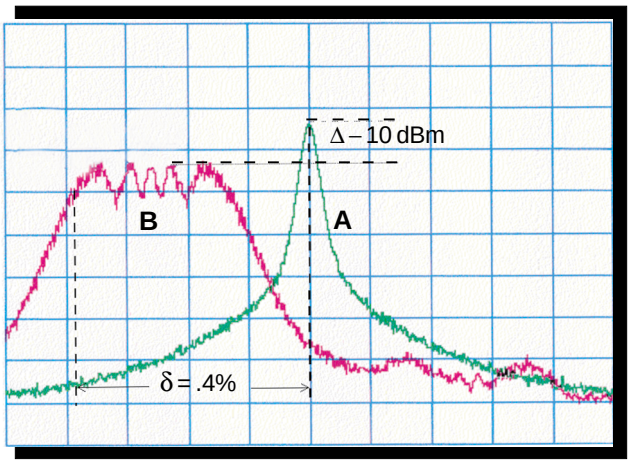


Figure 3. 200MHz Clock Output in Frequency Domain

(A) Spread-Spectrum OFF
(B) Spread-Spectrum ON

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8431-11 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. VDD, VDDI, VDDA, and VDDO should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, better power supply isolation is required. *Figure 4* illustrates how a 10Ω along with a 10µF and a .01µF bypass capacitor should be connected to each power supply pin.

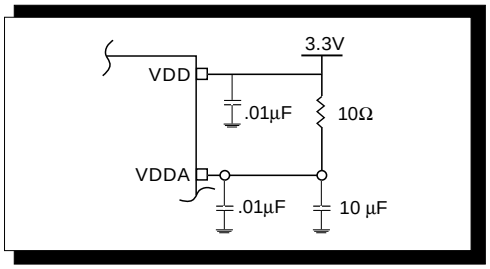


Figure 4. Power Supply Filtering

Termination for PECL Outputs

The clock layout topology shown below is typical for IA64/32 platforms. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/PECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. There are a few simple termination schemes. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

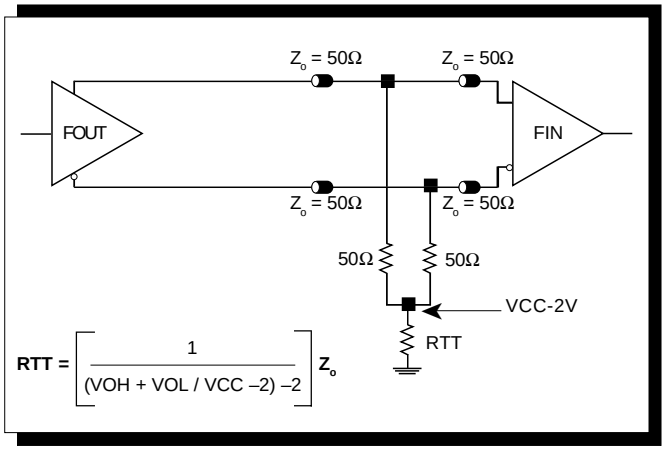


Figure 5A. LVPECL Output Termination

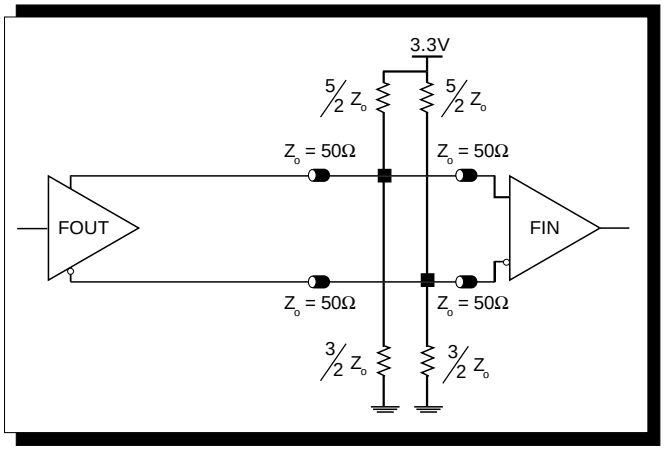


Figure 5B. LVPECL Output Termination

Layout Guideline

The schematic of the ICS8431-11 layout example used in this layout guideline is shown in *Figure 6A.* The ICS8431-11 recommended PCB board layout for this example is shown in *Figure 6B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stacking of the P.C. board.

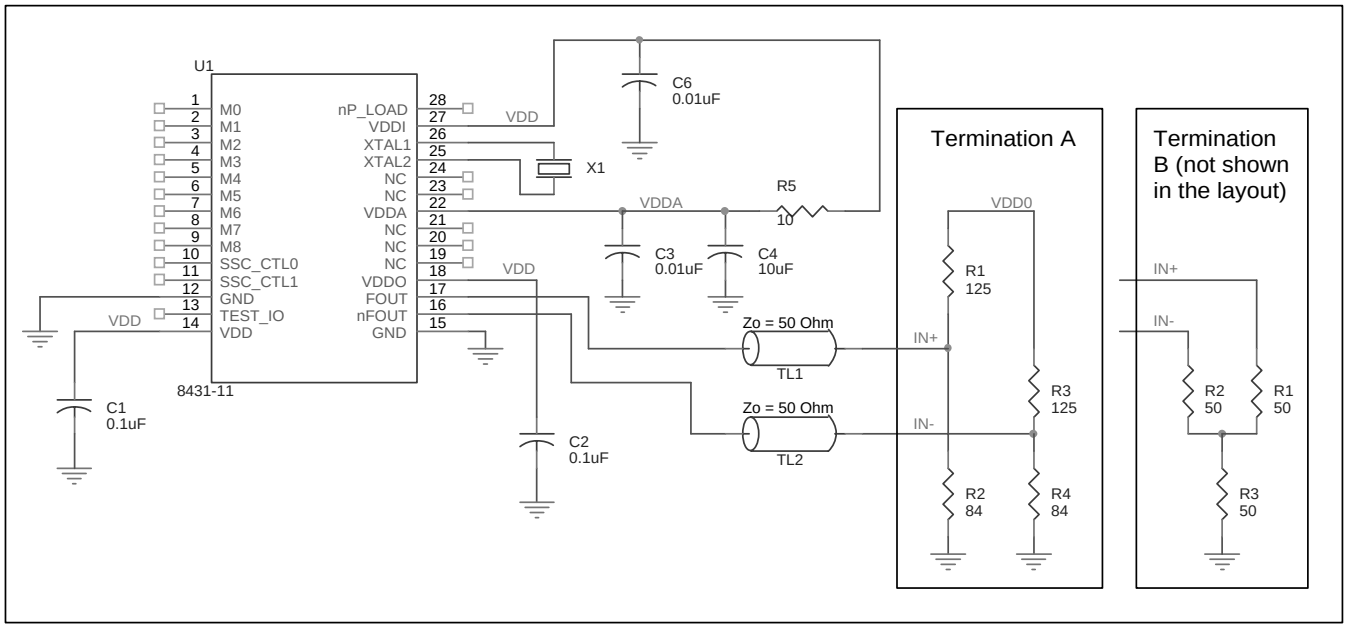


Figure 6A. Recommended Schematic Layout

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors C1, C2 and C3, C4, C5, C6 as close as possible to the power pins. If space allows, placing the decoupling capacitor at the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin generated by the via.

Maximize the pad size of the power (ground) at the decoupling capacitor. Maximize the number of vias between power (ground) and the pads. This can reduce the inductance between the power (ground) plane and the component power (ground) pins.

If VDDA shares the same power supply with VDD, insert the RC filter R5, C3, and C4 in between. Place this RC filter as close to the VDDA as possible.

Clock Traces and Termination

The component placements, locations and orientations should be arranged to achieve the best clock signal quality. Poor clock signal quality can degrade the system performance or cause system failure. In the synchronous high-speed digital system, the clock signal is less tolerable to poor signal quality than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The trace shape and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signals traces.

- The traces with 50Ω transmission lines TL1 and TL2 at FOUT and nFOUT should have equal delay and run adjacent to each other. Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock trace on same layer. Whenever possible, avoid any vias on the clock traces. Any via on the trace can affect the trace characteristic impedance and hence degrade signal quality.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow more space between the clock trace and the other signal trace.
- Make sure no other signal trace is routed between the clock trace pair.

The matching termination resistors R1, R2, R3 and R4 should be located as close to the receiver input pins as possible. Other termination scheme can also be used but is not shown in this example.

Crystal

The crystal X1 should be located as close as possible to the pins 26 (XTAL1) and 25 (XTAL2). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

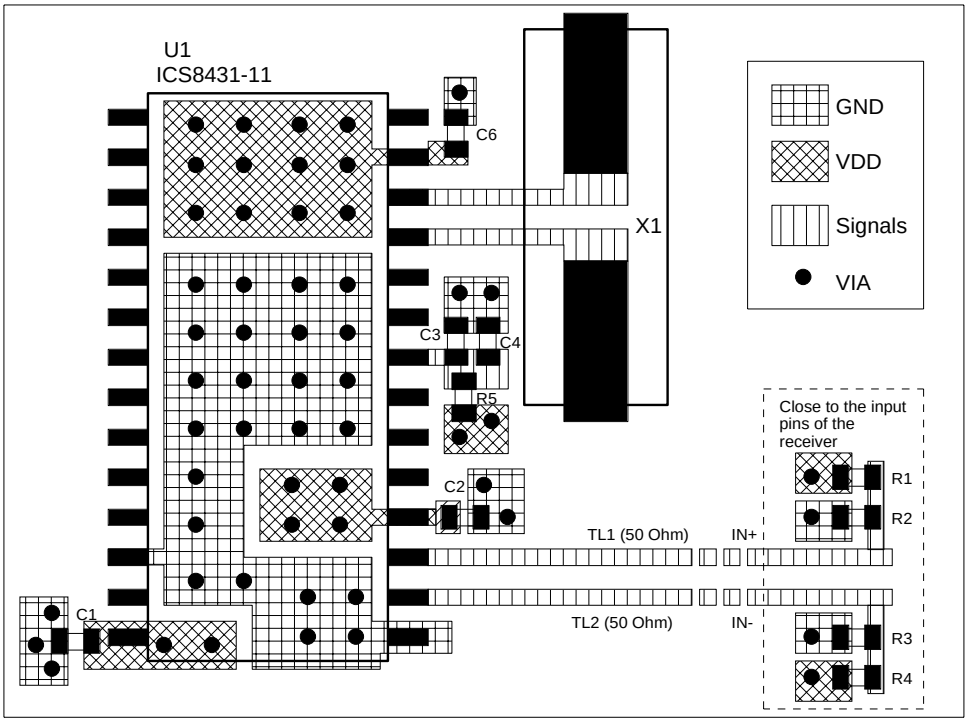


Figure 6B. PCB Board Layout For ICS8431-11

Package Outline - M Suffix

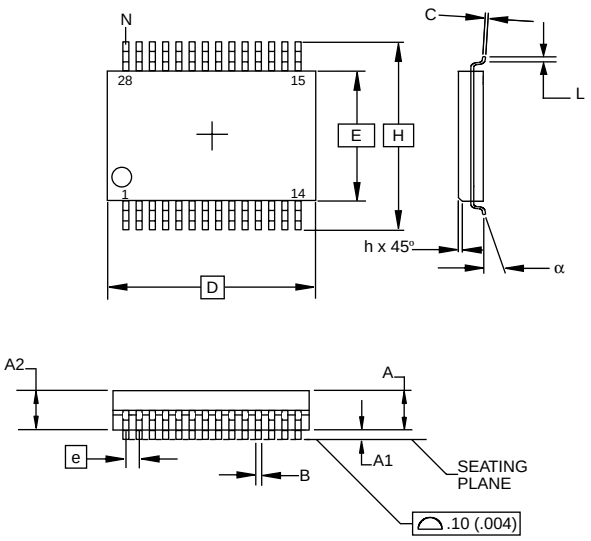


Table 7. Package Dimensions

SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
N	28			
A	--	2.65	--	0.104
A1	0.10	--	0.0040	--
A2	2.05	2.55	0.081	0.100
B	0.33	0.51	0.013	0.020
C	0.18	0.32	0.007	0.013
D	17.70	18.40	0.697	0.724
E	7.40	7.60	0.291	0.299
e	1.27 BASIC		0.050 BASIC	
H	10.00	10.65	0.394	0.419
h	0.25	0.75	0.010	0.029
L	0.40	1.27	0.016	0.050
α	0°	8°	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

Table 8. Ordering Information

Part/Order Number	Marking	Package	Count	Temperature
ICS8431CM-11	ICS8431CM-11	28 Lead SOIC	26 Per Tube	0°C to 70°C
ICS8431CM-11T	ICS8431CM-11	28 Lead SOIC on Tape and Reel	1000	0°C to 70°C