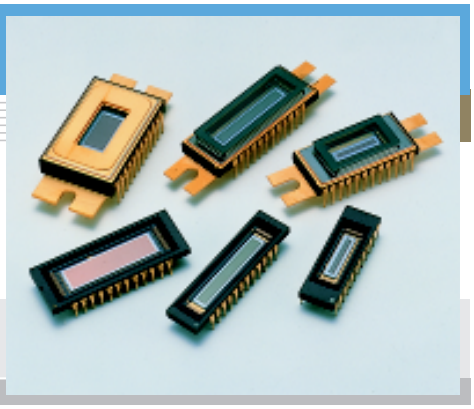

CCD area image sensor
S7010/S7011/S7015 series

Front-illuminated FFT-CCD

S7010/S7011/S7015 series are families of FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. By using the binning operation, S7010/S7011/S7015 series can be used as a linear image sensor having a long aperture in the direction of the device length. This makes S7010/S7011/S7015 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. S7010/S7011/S7015 series also feature low noise and low dark signal (MPP mode operation). This enables low-light-level detection and long integration time, thus achieving a wide dynamic range.
S7010/S7011/S7015 series have an effective pixel size of 24 × 24 µm and are available in image areas ranging from 12.288 (H) × 1.44 (V) mm^2 (512 × 60 pixels) up to a large image area of 24.576 (H) × 6.048 (V) mm^2 (1024 × 252 pixels).

Features

- 512 (H) × 60 (V) to 1024 (H) × 252 (V) pixel format
- Pixel size: 24 × 24 µm
- Line/pixel binning
- 100 % fill factor
- Wide dynamic range
- Low dark signal
- Low readout noise
- MPP operation

Applications

- Fluorescence spectrometer, ICP
- Raman spectrometer
- Industrial inspection requiring
- Semiconductor inspection
- DNA sequencer
- Low-light-level detection

■ Selection guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm(H) × mm(V)]	Suitable multichannel detector Head
S7010-0906	Non-cooled	532 × 64	512 × 60	12.288 × 1.440	C7020
S7010-0907		532 × 128	512 × 124	12.288 × 2.976	
S7010-0908		532 × 256	512 × 252	12.288 × 6.048	
S7010-1006		1044 × 64	1024 × 60	24.576 × 1.440	
S7010-1007		1044 × 128	1024 × 124	24.576 × 2.976	
S7010-1008		1044 × 256	1024 × 252	24.576 × 6.048	
S7011-0906	One-stage TE-cooled	532 × 64	512 × 60	12.288 × 1.440	C7021
S7011-0907		532 × 128	512 × 124	12.288 × 2.976	
S7011-1006		1044 × 64	1024 × 60	24.576 × 1.440	
S7011-1007		1044 × 128	1024 × 124	24.576 × 2.976	
S7015-0908		532 × 256	512 × 252	12.288 × 6.048	C7025
S7015-1008		1044 × 256	1024 × 252	24.576 × 6.048	

■ General ratings

Parameter	Specification
Pixel size	24 (H) × 24 (V) µm
Vertical clock phase	2 phase
Horizontal clock phase	2 phase
Output circuit	One-stage MOSFET source follower
Package	24 pin ceramic DIP (refer to dimensional outlines)
Window *1	S7010 series: quartz glass S7011 series: sapphire glass S7015 series: quartz glass *2

*1: Window-less is available upon request.
*2: Sapphire glass is available upon request.

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■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+30	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	V_{OD}	-0.5	-	+25	V
RD voltage	V_{RD}	-0.5	-	+18	V
ISV voltage	V_{ISV}	-0.5	-	+18	V
ISH voltage	V_{ISH}	-0.5	-	+18	V
IGV voltage	V_{IG1V}, V_{IG2V}	-10	-	+15	V
IGH voltage	V_{IG1H}, V_{IG2H}	-10	-	+15	V
SG voltage	V_{SG}	-10	-	+15	V
OG voltage	V_{OG}	-10	-	+15	V
RG voltage	V_{RG}	-10	-	+15	V
TG voltage	V_{TG}	-10	-	+15	V
Vertical clock voltage	V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal clock voltage	V_{P1H}, V_{P2H}	-10	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{OD}	18	20	22	V
Reset drain voltage		V_{RD}	11.5	12	12.5	V
Output gate voltage		V_{OG}	1	3	5	V
Substrate voltage		V_{SS}	-	0	-	V
Test point (vertical input source)		V_{ISV}	-	V_{RD}	-	V
Test point (horizontal input source)		V_{ISH}	-	V_{RD}	-	V
Test point (vertical input gate)		V_{IG1V}, V_{IG2V}	-8	0	-	V
Test point (horizontal input gate)		V_{IG1H}, V_{IG2H}	-8	0	-	V
Vertical shift register clock voltage	High	V_{P1VH}, V_{P2VH}	4	6	8	V
	Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage	High	V_{P1HH}, V_{P2HH}	4	6	8	V
	Low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Summing gate voltage	High	V_{SGH}	4	6	8	V
	Low	V_{SGL}	-9	-8	-7	
Reset gate voltage	High	V_{RGH}	4	6	8	V
	Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage	High	V_{TGH}	4	6	8	V
	Low	V_{TGL}	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	1	MHz
Vertical shift register capacitance *3	C_{P1V}, C_{P2V}	-	3,000	-	pF
Horizontal shift register capacitance *3	C_{P1H}, C_{P2H}	-	120	-	pF
Summing gate capacitance	C_{SG}	-	7	-	pF
Reset gate capacitance	C_{RG}	-	7	-	pF
Transfer gate capacitance	C_{TG}	-	120	-	pF
Charge transfer efficiency *4	CTE	0.99995	0.99999	-	-
DC output level *5	Vout	12	15	18	V
Output impedance *5	Zo	-	3	-	kΩ
Power consumption *5 *6	P	-	15	-	mW

*3: S7010/S7011-1007
*4: Charge transfer efficiency per pixel, measured at half of the full well.
*5: The values depend on the load resistance. (typical, VOD=20 V, load resistance=22 kΩ)
*6: Power consumption of the on-chip amplifier.

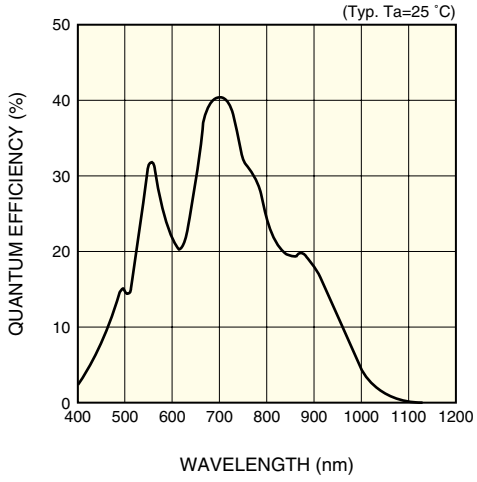
■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	150,000	300,000	-	e^-
	Horizontal *7		300,000	600,000	-	
CCD node sensitivity		Sv	1.8	2.2	-	μV/e^-
Dark current *8 MPP mode (tentative data)	25 °C	DS	-	400	3000	e^-/pixel/s
	0 °C		-	20	150	
Readout noise *9		Nr	-	8	12	e^- rms
Dynamic range *10	Line binnng	DR	25,000	75,000	-	-
	Area scanning		12,000	37,500	-	-
Photo response non-uniformity *11		PRNU	-	±3	±10	%
Spectral response range		λ	-	400 to 1,100	-	nm

*7: Large horizontal full well for vertical binning operation.
*8: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*9: -40 °C, operating frequency is 150 kHz.
*10: Dynamic range: DR = Full well/Readout noise.
*11: Measured at half of full well capacity.
Photo response non-uniformity:

$$\text{PRNU}\ (\%) = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

■ Spectral response (without window)



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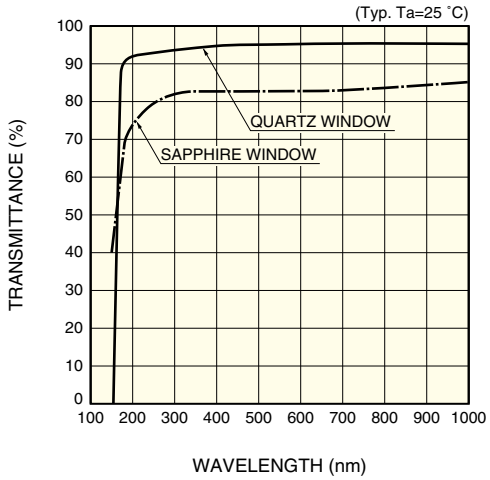
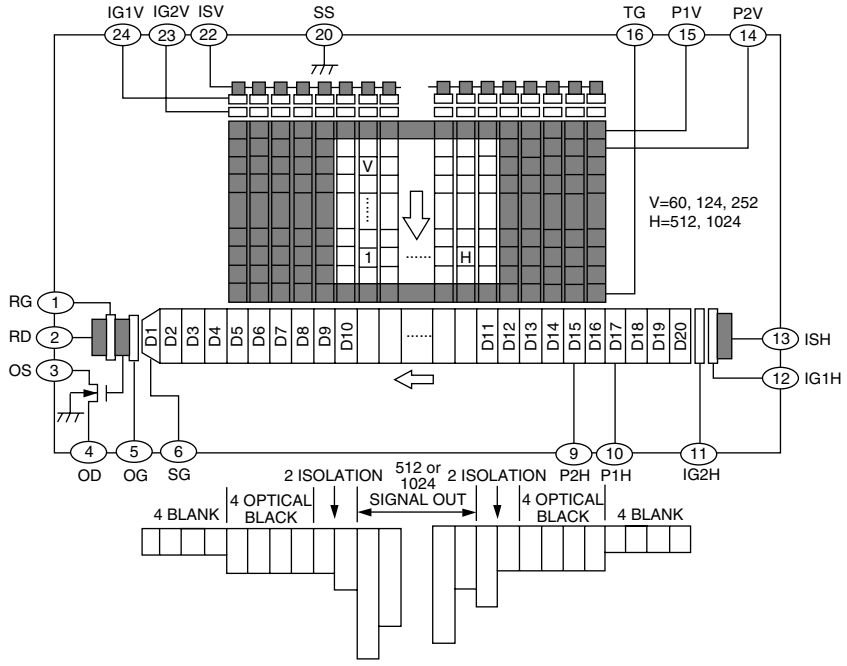
■ Spectral transmittance characteristics



KMPDB0101EA

■ Device structure, line output format



KMPDC0015EB

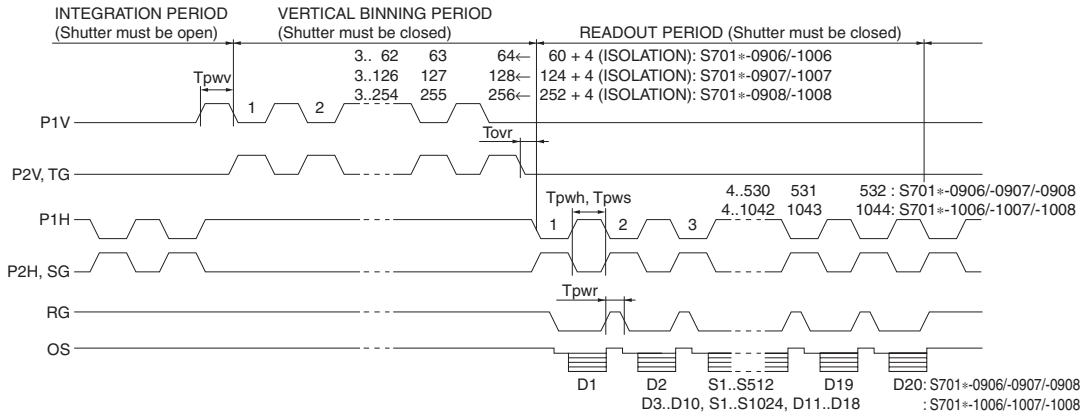
Pixel format

Left ← Horizontal Direction → Right						
Blank	Optical Black	Isolation	Effective	Isolation	Optical Black	Blank
4	4	2	512 or 1024	2	4	4

Top ← Vertical Direction → Bottom		
Isolation	Effective	Isolation
2	60, 124 or 252	2

■ Timing chart

Line binning

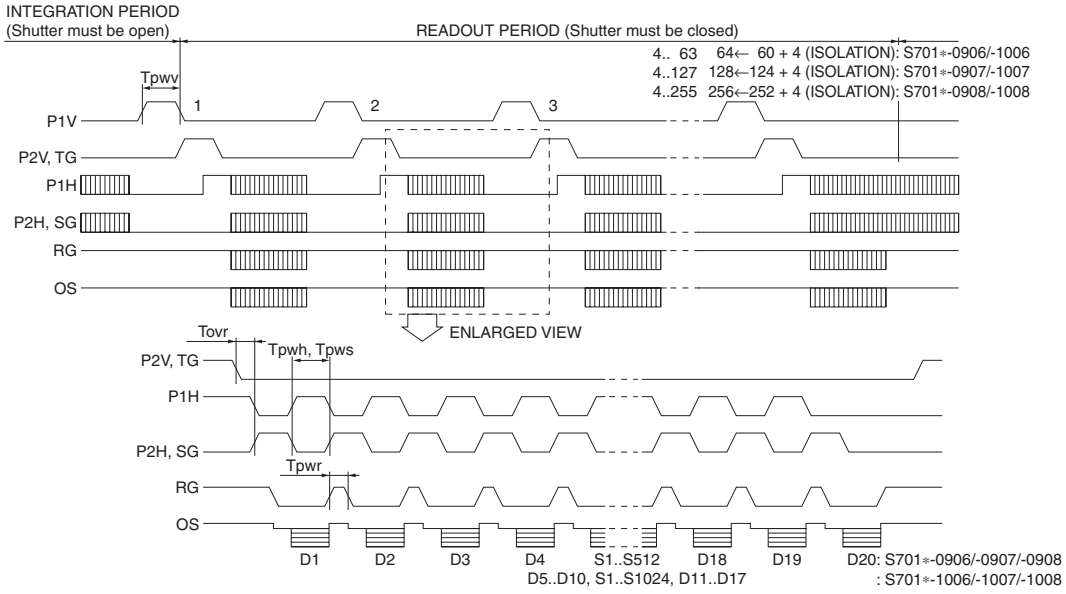


KMPDC0122EA

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*12	6 *13	-	-	µs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*12	500	-	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	-	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	Overlap time	Tovr	-	3	-	-	µs

*12: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.
*13: In case of S701∗-0908/-1007.

Area scanning 1: low dark current mode

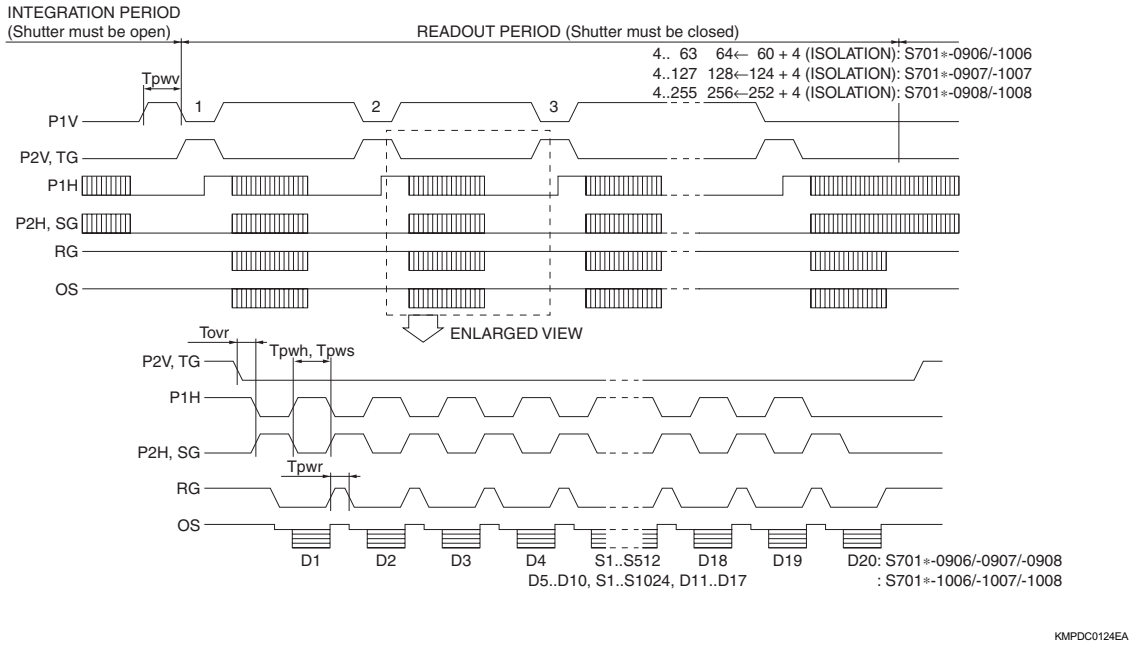


KMPDC0123EA

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*14	6 *15	-	-	µs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*14	500	-	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	-	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	Overlap time	Tovr	-	3	-	-	µs

*14: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.
*15: In case of S701∗-0908/-1007.

Area scanning 2: large full well mode



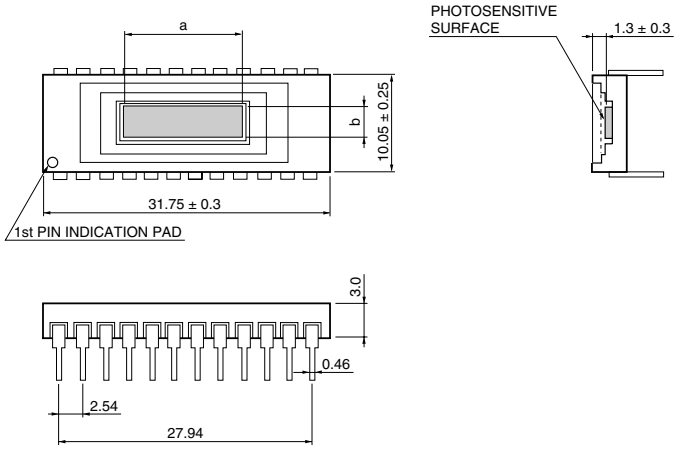
KMPDC0124EA

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*16	6 *17	-	-	µs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*16	500	-	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	-	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG - P1H	Overlap time	Tovr	-	3	-	-	µs

*16: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.
*17: In case of S701∗-0908/-1007.

■ Dimensional outlines (unit: mm)

S7010-0906/-0907



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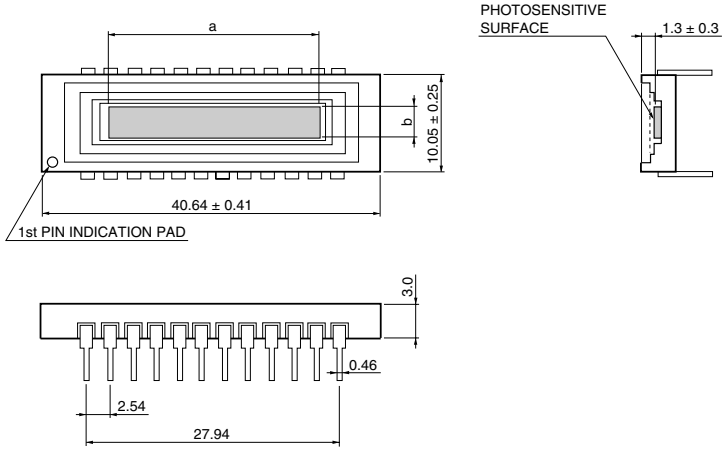
S7010-1006/-1007



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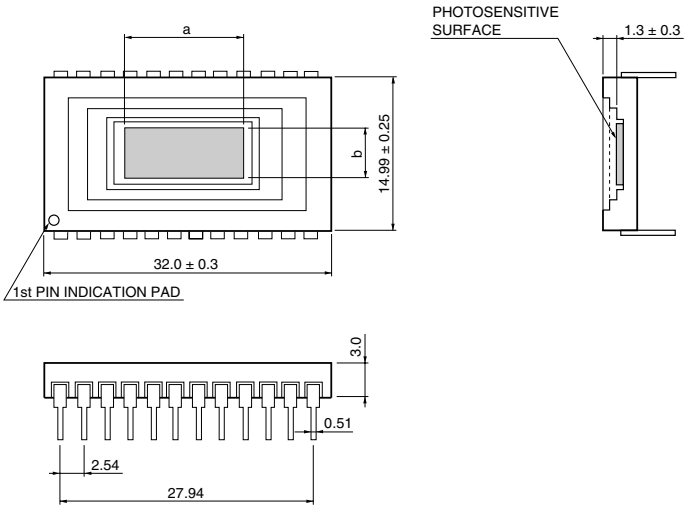
S7010-0908



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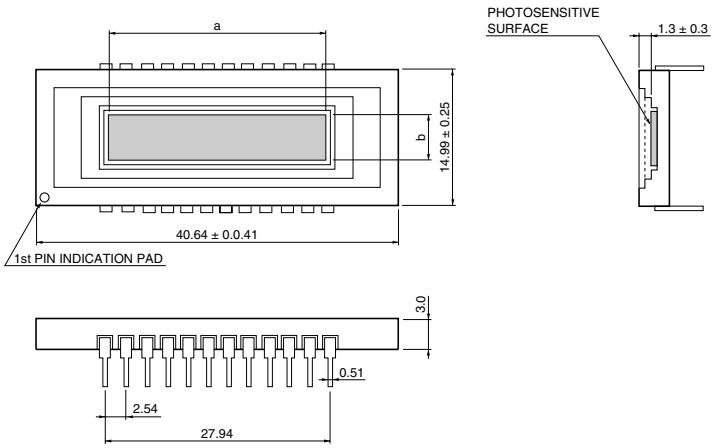
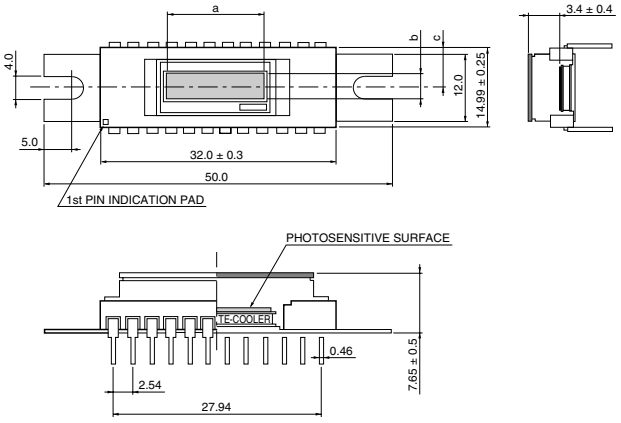
S7010-1008



KMPDA0056EA

Type No.	Active area	
	a	b
S7010-0906	12.288 (H)	1.440 (V)
S7010-0907	12.288 (H)	2.976 (V)
S7010-0908	12.288 (H)	6.048 (V)
S7010-1006	24.576 (H)	1.440 (V)
S7010-1007	24.576 (H)	2.976 (V)
S7010-1008	24.576 (H)	6.048 (V)

S7011-0906/-0907



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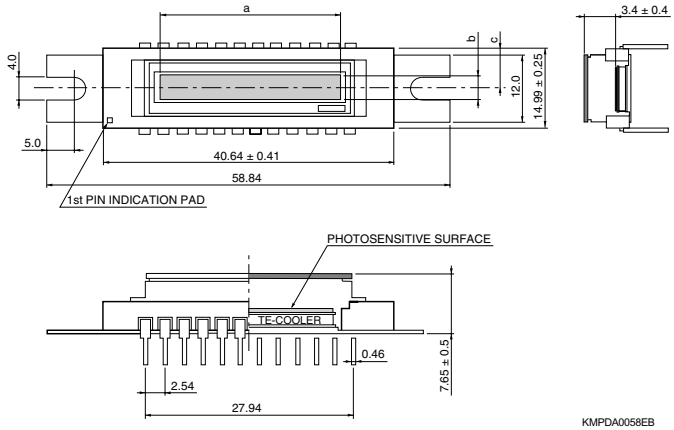
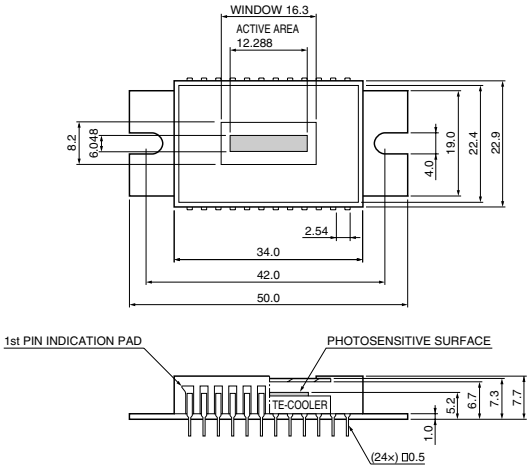
S7011-1006/-1007



KMPDA0058EB

Type No.	Active area		
	a	b	c
S7011-0906	12.288 (H)	1.440 (V)	7.5
S7011-0907	12.288 (H)	2.976 (V)	7.1
S7011-1006	24.576 (H)	1.440 (V)	7.5
S7011-1007	24.576 (H)	2.976 (V)	7.1

S7015-0908



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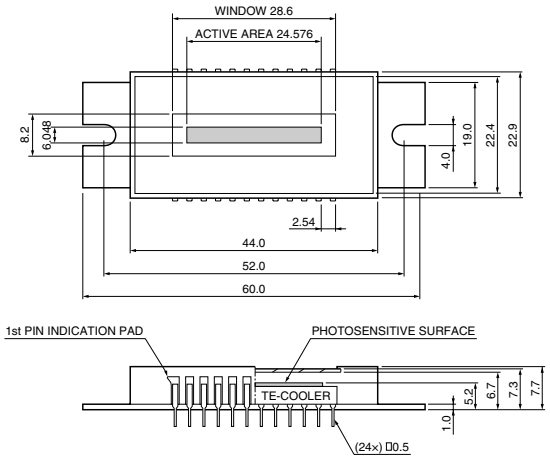
S7015-1008



KMPDA0045EB

■ Pin connections

Pin No.	S7010 series		S7011 series		S7015 series		Remark
	Symbol	Description	Symbol	Description	Symbol	Description	
1	RG	Reset gate	RG	Reset gate	RG	Reset gate	
2	RD	Reset drain	RD	Reset drain	RD	Reset drain	
3	OS	Output transistor source	OS	Output transistor source	OS	Output transistor source	
4	OD	Output transistor drain	OD	Output transistor drain	OD	Output transistor drain	
5	OG	Output gate	OG	Output gate	OG	Output gate	
6	SG	Summing gate	SG	Summing gate	SG	Summing gate	=P2H
7	NC		Th1	Thermistor	Th1	Thermistor	
8	NC		Th2	Thermistor	Th2	Thermistor	
9	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
11	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	0 V
12	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	0 V
13	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	=RD
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	TG *18	Transfer gate	TG *18	Transfer gate	TG *18	Transfer gate	=P2V
17	NC		NC		NC		
18	NC		P-	TE-cooler-	P-	TE-cooler-	
19	NC		P+	TE-cooler+	P+	TE-cooler+	
20	SS	Substrate (GND)	SS	Substrate (GND)	SS	Substrate (GND)	
21	NC		NC		NC		
22	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	=RD
23	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	0 V
24	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	0 V

*18 TG: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

■ Specifications of built-in TE-cooler (Typ.)

Parameter	Symbol	Condition	S7011-0906/ -0907	S7011-1006/ -1007	S7015-0908	S7015-1008	Unit
Internal resistance	Rint	Ta=25 °C	2.8	6.0	2.5	1.2	Ω
Maximum current *19	Imax	Tc *20=Th *21=25 °C	1.5	1.5	1.5	3.0	A
Maximum voltage	Vmax	Tc *20=Th *21=25 °C	4.4	8.8	3.8	3.6	V
Maximum heat absorption *22	Qmax		3.4	6.7	3.4	5.1	W
Maximum temperature of heat radiating side	-		70				°C

*19: Maximum current Imax:
If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.

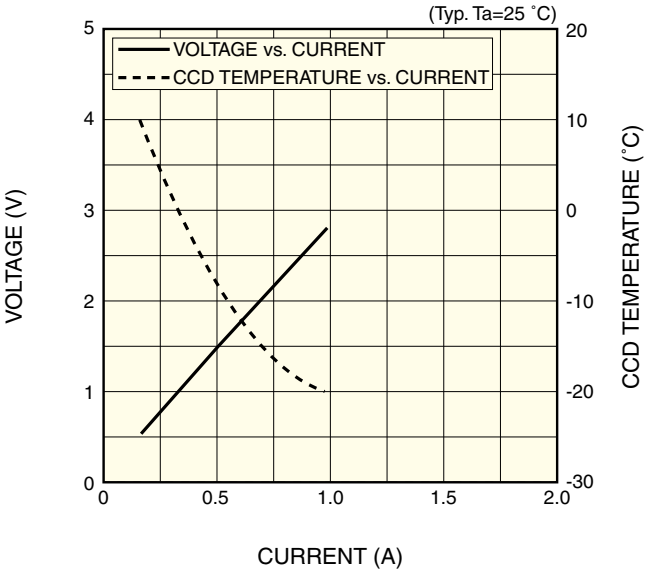
*20: Temperature of the cooling side of thermoelectric cooler.

*21: Temperature of the heat radiating side of thermoelectric cooler.

*22: Maximum heat absorption Qmax.
This is a heat absorption when the maximum current is supplied to the TE-cooler.

■ TE-cooler characteristics

S7011-0906/-0907



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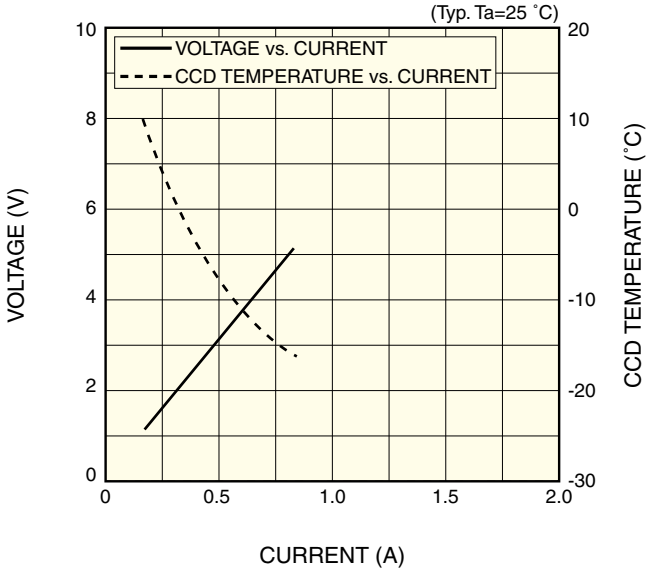
S7011-1006/-1007



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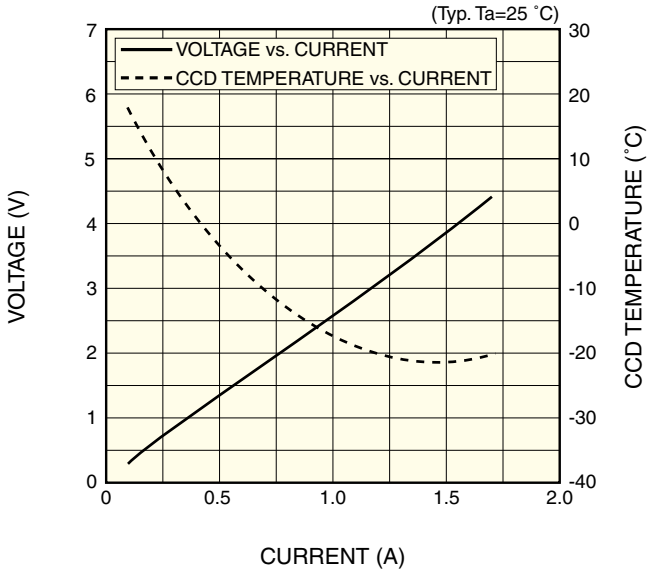
S7015-0908



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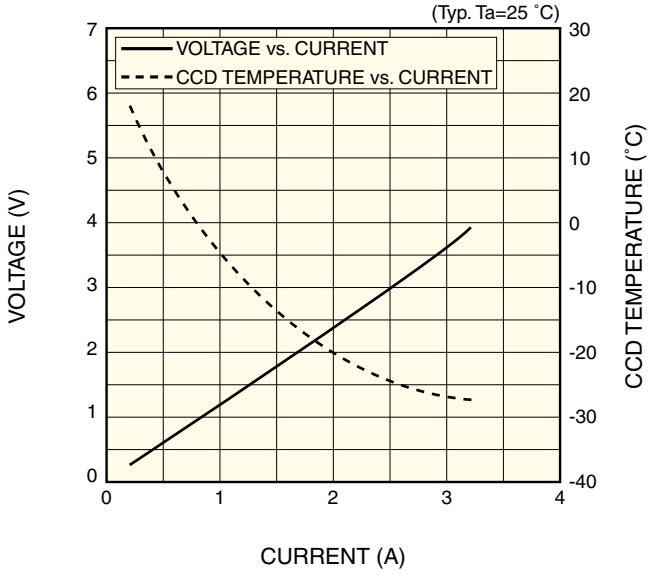
S7015-1008



KMPDB0179EA

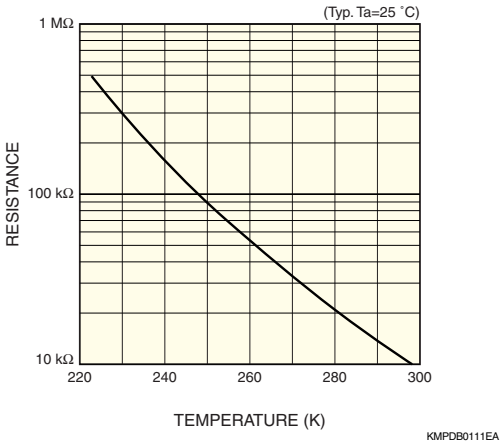
■ Specifications of built-in temperature sensor

A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$$R1 = R2 \times \exp B\left(\frac{1}{T1} - \frac{1}{T2}\right)$$

where R1 is the resistance at absolute temperature T1 (K)
R2 is the resistance at absolute temperature T2 (K)
B is so-called the B constant (K)

The characteristics of the thermistor used are as follows.
R (298K) = 10 kΩ
B (298K / 323K) = 3450 K



■ Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature incline rate

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

Multichannel detector head (C7020, C7021, C7025)

Features

- C7020: for S7010 series
  C7021: for S7011 series
  C7025: for S7015 series
- Area scanning or full line-binnng operation
- Readout frequency: 250 kHz
- Readout noise: 20 e⁻rms
- ΔT=50 °C (ΔT changes by radiation method.)

Input	Symbol	Value
Supply voltage	V_{D1}	+5 Vdc, 200 mA
	V_{A1+}	+15 Vdc, +100 mA
	V_{A1-}	-15 Vdc, -100 mA
	V_{A2}	+24 Vdc, 30 mA
	V_{D2}	+5 Vdc, 30 mA (C7021, C7025)
	Vp	+5 Vdc, 2.5 A (C7021, C7025)
	V_F	+12 Vdc, 100 mA (C7021, C7025)
Master start	ϕms	HCMOS logic compatible
Master clock	ϕmc	HCMOS logic compatible, 1 MHz

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