

- Frequency range 38MHz to 640MHz
- LVPECL Output
- Supply Voltage 3.3 VDC
- Phase jitter 0.4ps typical
- Pull range from $\pm 30\text{ppm}$ to $\pm 150\text{ppm}$

DESCRIPTION

GPF64 VCXOs are packaged in a 6 pad 11.4 x 9.6mm SMD package. Typical phase jitter for GPF series VCXOs is 0.4 ps. Output is LVPECL. Applications include phase lock loop, SONET/ATM, set-top boxes, MPEG, audio/video modulation, video game consoles and HDTV.

SPECIFICATION

Frequency Range:	38.0MHz to 640.0MHz
Supply Voltage:	3.3 VDC $\pm 5\%$
Output Logic:	LVPECL
RMS Period Jitter:	3.0ps typical
Peak to Peak Jitter:	20.0ps typical, 30.0ps maximum
Phase Jitter:	0.4ps typical, 5.0ps maximum
Initial Frequency Accuracy:	Tune to the nominal frequency with $V_c = 1.65 \pm 0.2\text{VDC}$
Output Voltage HIGH (1):	Vdd-1.025V minimum Vdd-0.880V maximum
Output Voltage LOW (0):	Vdd-1.810V minimum Vdd-1.620V maximum ($R_L = 50\Omega$ to Vdd-2V)
Pulling Range:	From $\pm 30\text{ppm}$ to $\pm 150\text{ppm}$
Control Voltage Range:	1.65 ± 0.35 Volts
Temperature Stability:	See table
Output Load:	50Ω into Vdd or Thevenin equiv.
Rise/Fall Times:	0.5ns typ., 0.7ns max. 20% Vdd to 80% Vdd
Duty Cycle:	50% $\pm 5\%$ (Measured at Vdd-1.3V)
Start-up Time:	10ms maximum, 5ms typical
Current Consumption:	75mA maximum at 212.5MHz 80mA maximum at 622.08MHz
Static Discharge Protection:	2kV maximum
Storage Temperature:	-55° to $+150^\circ\text{C}$
Ageing:	$\pm 2\text{ppm}$ per year maximum
Enable/Disable:	See table
RoHS Status:	Fully compliant or non-compliant

FREQUENCY STABILITY

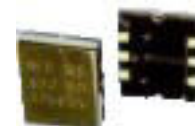
Stability Code	Stability $\pm\text{ppm}$	Temp. Range
A	25	$0^\circ \sim +70^\circ\text{C}$
B	50	$0^\circ \sim +70^\circ\text{C}$
C	100	$0^\circ \sim +70^\circ\text{C}$
D	25	$-40^\circ \sim +85^\circ\text{C}$
E	50	$-40^\circ \sim +85^\circ\text{C}$
F	100	$-40^\circ \sim +85^\circ\text{C}$

If non-standard frequency stability is required
Use 'I' followed by stability, i.e. I20 for $\pm 20\text{ppm}$

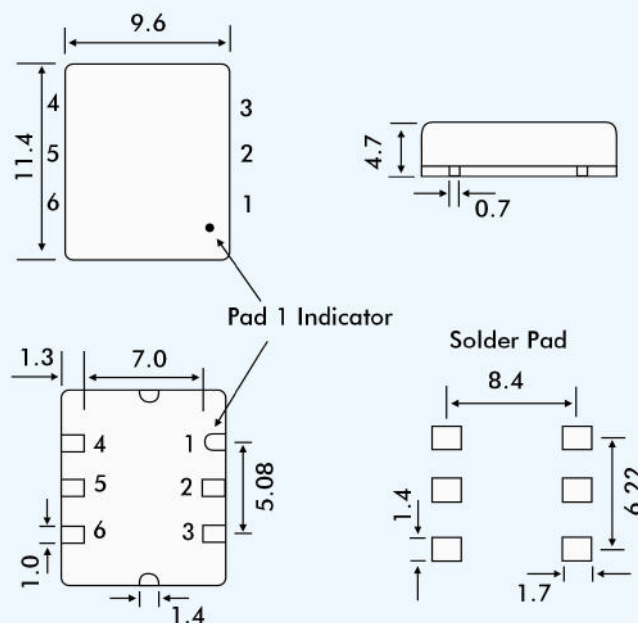
ENABLE/DISABLE FUNCTION

Tristate Pad Status	Output Status
Not connected Below 0.3Vdd (Ref. to ground)	LVPECL and Complimentary LVPECL enabled Both outputs are disabled (high impedance)
Above 0.7Vdd (Ref. to ground)	Both outputs are enabled

11.4 x 9.6 x 2.5mm SMD VCXO



OUTLINE & DIMENSIONS



Pad Connections

- 1 Voltage Control (rounded pad)
- 2 Enable/Disable (Tristate)
- 3 Ground
- 4 Output
- 5 Complimentary Output
- 6 Supply Voltage

PART NUMBERING

Example: **3GPF64GB-80N-60.000**

