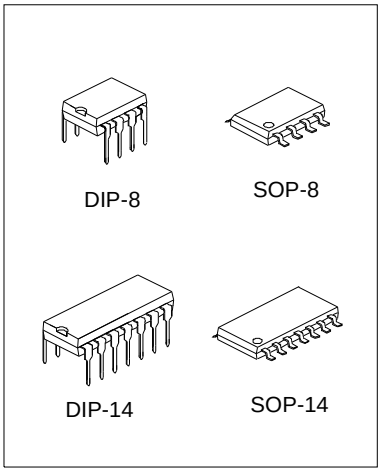
DTMF GENERATOR WITH MICRO-PROCESSOR INTERFACE

DESCRIPTION

The SC9200 tone generators are designed for μC interfaces. They can be instructed by a μC to generate 16 dual tones and 8 single tones from the DTMF pin. The SC9200A/AS provides a serial mode whereas the SC9200B/BS contains a selectable serial/parallel mode interface for various applications



FEATURES

* Operating voltage: 2.0V~5.5V
* Serial mode for the SC9200A/AS
* Serial/parallel mode for the SC9200B/BS
* Low standby current
* Low total harmonic distortion
* 3.58MHz crystal or ceramic resonator

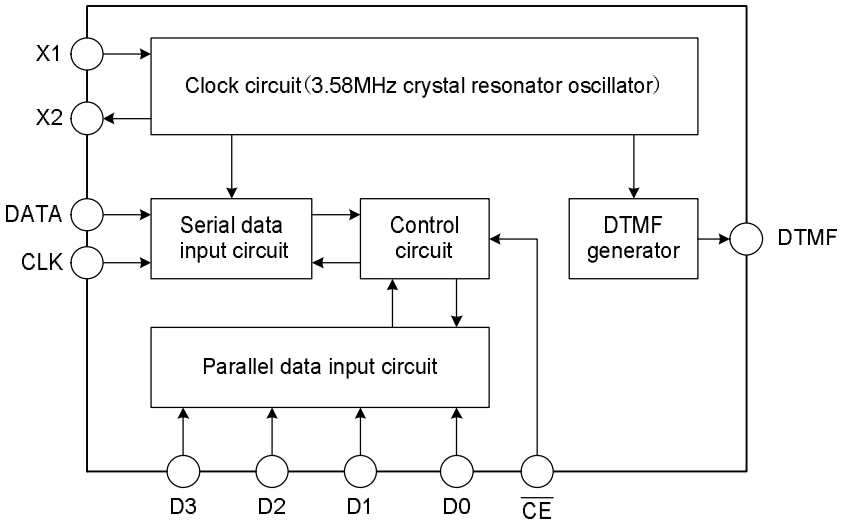
APPLICATIONS

* Security systems
* Home automation
* Remote control through telephone lines
* Communication system, etc.

ORDERING INFORMATION

Part No.	Package
SC9200A	DIP-8-300-2.54
SC9200B	DIP-14-300-2.54
SC9200AS	SOP-8-225-1.27
SC9200BS	SOP-14-225-1.27

BLOCK DIAGRAM



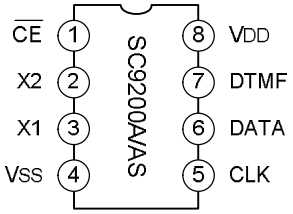
ABSOLUTE MAXIMUM RATING

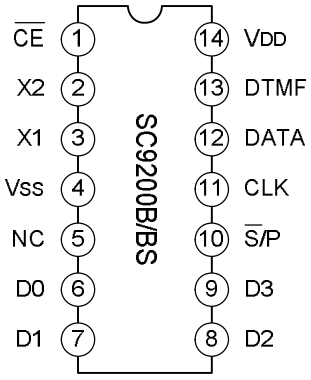
Characteristic	Symbol	Ratings	Unit
Supply Voltage	V_{SS}	-0.3~6	V
Input Voltage	V_{IN}	V_{SS}-0.3~V_{DD}+0.3	V
Storage Temperature	T_{stg}	-50~125	°C
Operating Temperature	T_{opr}	-20~75	°C

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Operating Voltage	V_{DD}	--	Serial	1.8	--	5.5	V
			Parallel	2.0			
Operating Current	I_{DD}	2.5V	$\overline{S/P}$ =V_{DD}, D0~D3=V_{SS}, $\overline{CE}$ =V_{SS}, No load	--	240	2500	μA
		5.0V		--	950	3000	
Low Input Voltage	V_{IL}	--	--	V_{SS}	--	0.2V_{DD}	V
High Input Voltage	V_{IH}	--	--	0.8V_{DD}	--	V_{DD}	V
Standby Current	I_{STB}	2.5V	$\overline{S/P}$, $\overline{CE}$ =V_{DD}, No load	--	--	1	μA
		5.0V		--	--	2	
Pull-high Resistance	R_P	2.5V	V_{OL}=0V	120	180	270	kΩ
		5.0V		45	68	100	
DTMF Output Delay Time (Parallel Mode)	t_{DE}	5V	--	--	t_{UP}+6	t_{UP}+8	ms
DTMF Output DC Level	V_{TDC}	2V~5.5V	DTMF Output	0.45V_{DD}	--	0.75V_{DD}	V
DTMF Sink Current	I_{TOL}	2.5V	V_{DTMF}=0.5V	-0.1	--	--	mA
DTMF Output AC Level	V_{TAC}	2.5V	Row group, R_L=5kΩ	0.12	0.15	0.18	V_{rms}
Column Pre-emphasis	ACR	2.5V	Row group=0dB	1	2	3	dB
DTMF Output Load	R_L	2.5V	t_{HD}≤-23dB	5	--	--	kΩ
Tone Signal Distortion	tHD	2.5V	R_L=5kΩ	--	-30	-23	dB
Clock Input Rate (Serial Mode)	f_{CLK}	--	--	--	100	500	kHz
Oscillator Starting Time (When $\overline{CE}$ is low)	t_{UP}	5.0V	The time from $\overline{CE}$ falling edge to normal oscillator operation	--	--	10	ms
System Frequency	f_{OSC}	--	Crystal=3.5795MHz	3.5759	3.5759	3.5831	MHz

PIN CONFIGURATION





PIN DESCRIPTION

Pin NO.		Pin Name	Description
DIP-8 SOP-8	DIP-14 SOP-14		
1	1	$\overline{CE}$	Chip enable, active low.
2	2	X2	The system oscillator consists of an inverter, a bias resistor, and the required load capacitor on chip. The oscillator function can be implemented by Connect a standard 3.579545MHz crystal to the X1 and X2 terminals.
3	3	X1	
4	4	VSS	Negative power supply.
	5	NC	No connection.
	6~9	D0~D3	Data inputs for the parallel mode. When the IC is operating in the serial mode, the data input terminals (D0~D3) are included with a pull-high resistor. When the IC is operating in the parallel mode, these pins become floating.
	10	$\overline{S/P}$	Operation mode selection input $\overline{S/P}$ ="H": Parallel mode $\overline{S/P}$ ="L": Serial mode
5	11	CLK	Data synchronous clock input for the serial mode. When the IC is operating in the parallel mode, the input terminal (CLK) is included with a pull-high resistor. When the IC is operating in the serial mode, this pin becomes floating.
6	12	DATA	Data input terminal for the serial mode. When the IC is operating in the parallel mode, the input terminal (DATA) is included with a pull-high resistor. When the IC is operating in the serial mode, this pin becomes floating.
7	13	DTMF	Output terminal of the DTMF signal.
8	14	VDD	Positive power supply, 2.0V~5.5V for normal operation.

FUNCTIONAL DESCRIPTION

The SC9200 are DTMF generators for μC interfaces. They are controlled by a μC in the serial mode.

1. Serial mode (SC9200)

The SC9200 employ a data input, a 5-bit code, and a synchronous clock to transmit a DTMF signal. The relationship between the digital codes and the tone output frequency is shown in Table 1 as for the control timing diagram, refer to *Figure 1.*

Table 1: Digits vs. input data vs. tone output frequency (serial mode)

Digit	D4	D3	D2	D1	D0	Tone Output Frequency (Hz)
1	0	0	0	0	1	697+1209
2	0	0	0	1	0	697+1336
3	0	0	0	1	1	697+1477
4	0	0	1	0	0	770+1209
5	0	0	1	0	1	770+1336
6	0	0	1	1	0	770+1477
7	0	0	1	1	1	852+1209
8	0	1	0	0	0	852+1336
9	0	1	0	0	1	852+1477
0	0	1	0	1	0	941+1336
*	0	1	0	1	1	941+1209
#	0	1	1	0	0	941+1477
A	0	1	1	0	1	697+1633
B	0	1	1	1	0	770+1633
C	0	1	1	1	1	852+1633
D	0	0	0	0	0	941+1633
--	1	0	0	0	0	697
--	1	0	0	0	1	770
--	1	0	0	1	0	852
--	1	0	0	1	1	941
--	1	0	1	0	0	1209
--	1	0	1	0	1	1336
--	1	0	1	1	0	1477
--	1	0	1	1	1	1633
DTMF OFF	1	1	1	1	1	--

*Notes: The codes not listed in Table 1 are not used D4 is MSB.

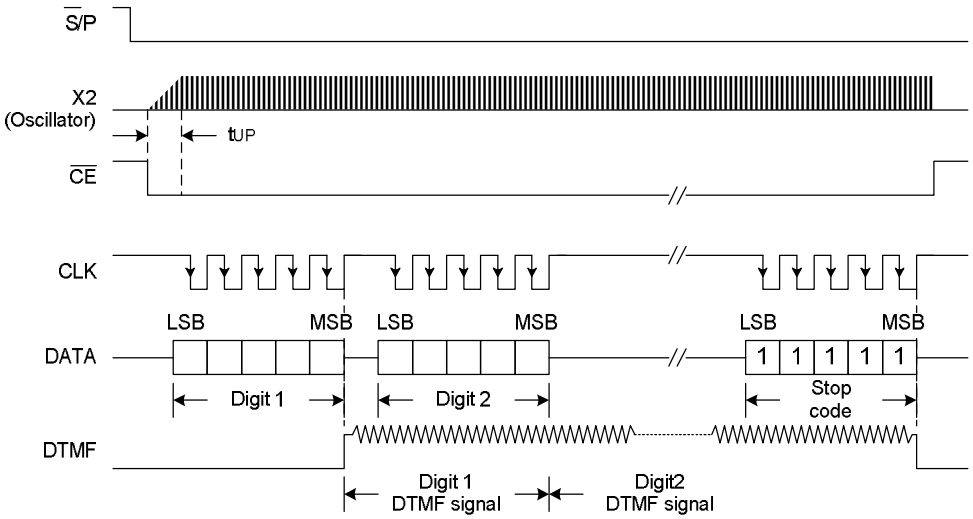


Figure 1

2. Parallel mode (SC9200B/BS)

The SC9200B/BS provides four data inputs D0~D3 to generate their corresponding DTMF signals. The $\overline{S/P}$ has to be connected high to select the parallel operation mode. Then the input data codes should be determined. Finally, the $\overline{CE}$ is connected low to transmit the DTMF signal from the DTMF pin.

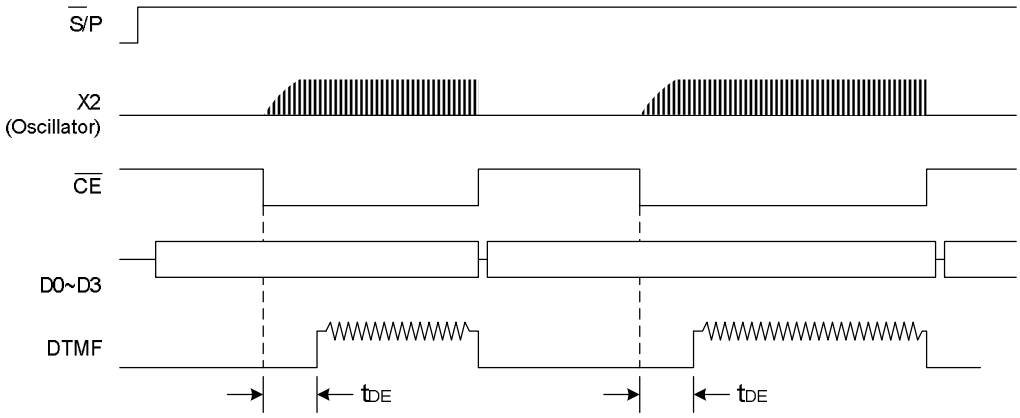
The TDE time (about 6ms) will be delayed from the $\overline{CE}$ falling edge to the DTMF signal output.

The relationship between the digital codes and the tone output frequency is illustrated in Table 2. As for the control timing diagram, see *Fiigure 2*.

When the system is operating in the parallel mode, D0~D3 are all in the floating state. Thus, these data input pins should not float.

Table 2: Digits vs. input data vs. tone output frequency (parallel mode)

Digit	D3	D2	D1	D0	Tone Output Frequency
1	0	0	0	1	697+1209
2	0	0	1	0	697+1336
3	0	0	1	1	697+1477
4	0	1	0	0	770+1209
5	0	1	0	1	770+1336
6	0	1	1	0	770+1477
7	0	1	1	1	852+1209
8	1	0	0	0	852+1336
9	1	0	0	1	852+1477
0	1	0	1	0	941+1336
*	1	0	1	1	941+1209
#	1	1	0	0	941+1477
A	1	1	0	1	697+1633
B	1	1	1	0	770+1633
C	1	1	1	1	852+1633
D	0	0	0	0	941+1633

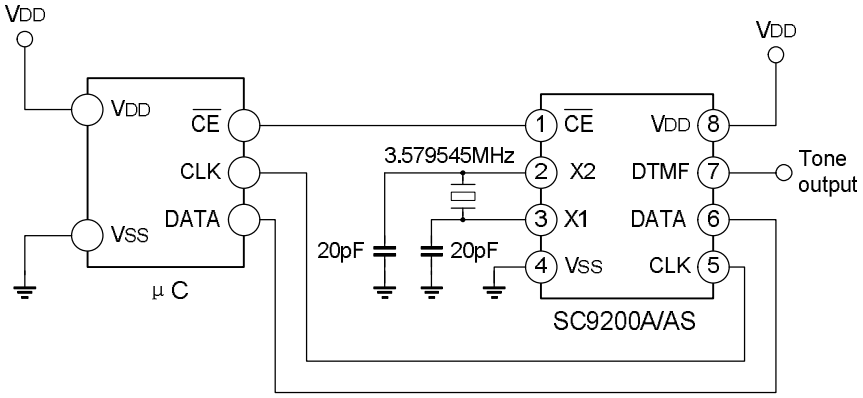


*Note: The data (D0~D3) should be ready before the $\overline{CE}$ becomes low.

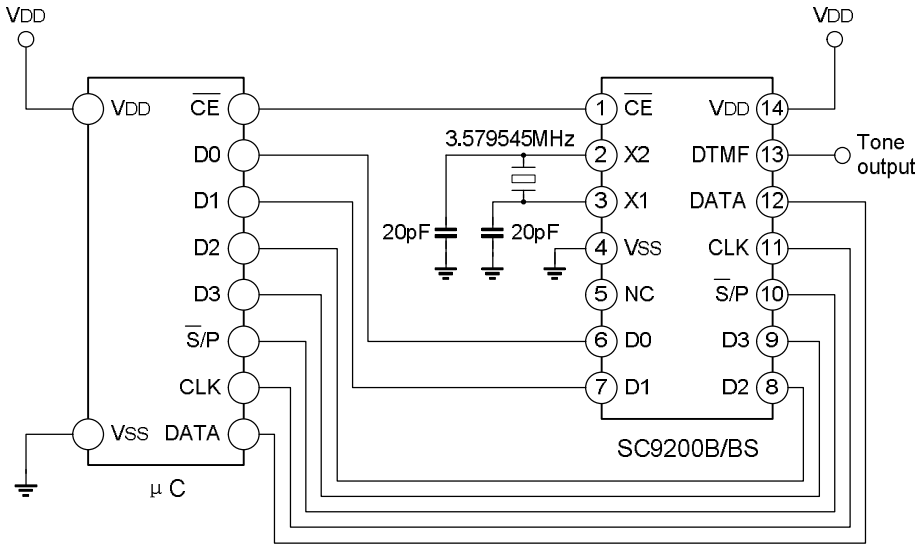
Figure 1

APPLICATION CIRCUIT

Serial mode

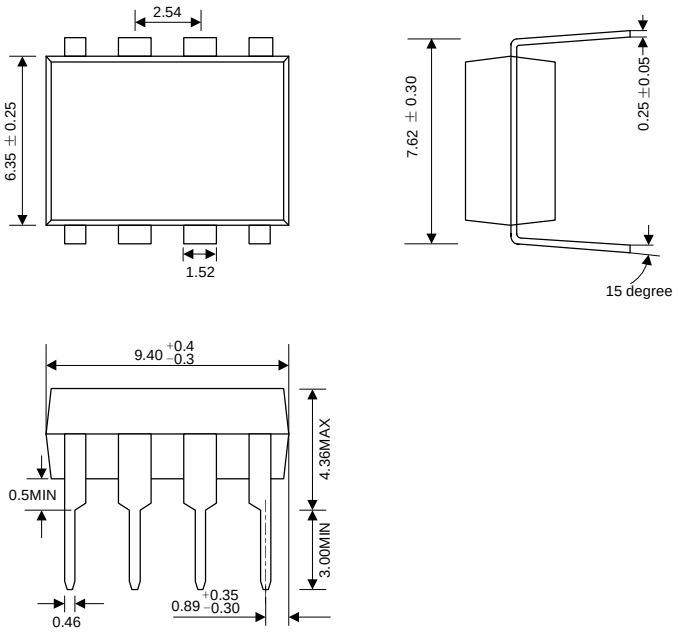


Serial/parallel mode

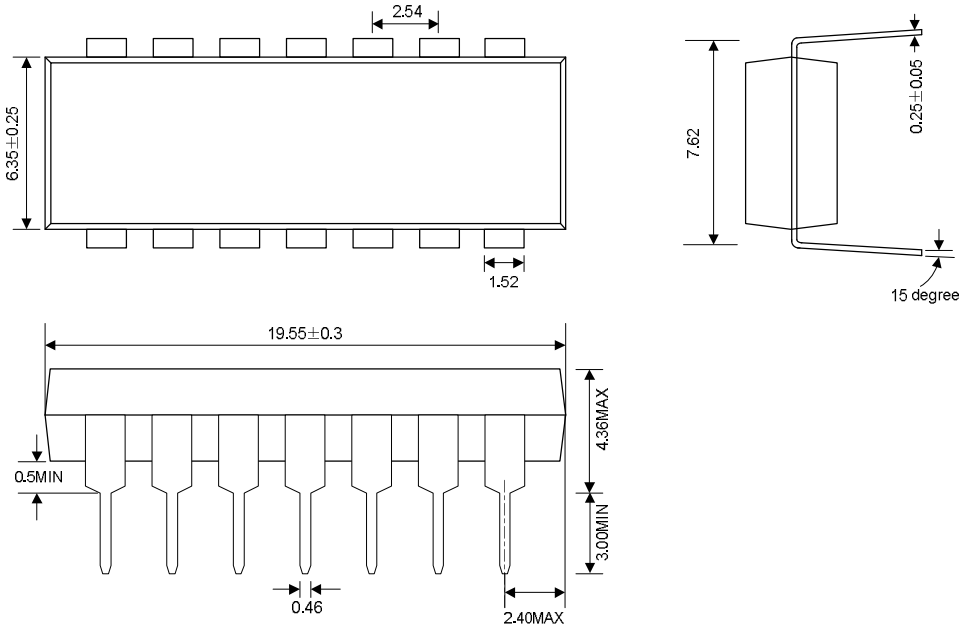


PACKAGE OUTLINE

DIP-8-300-2.54 UNIT: mm

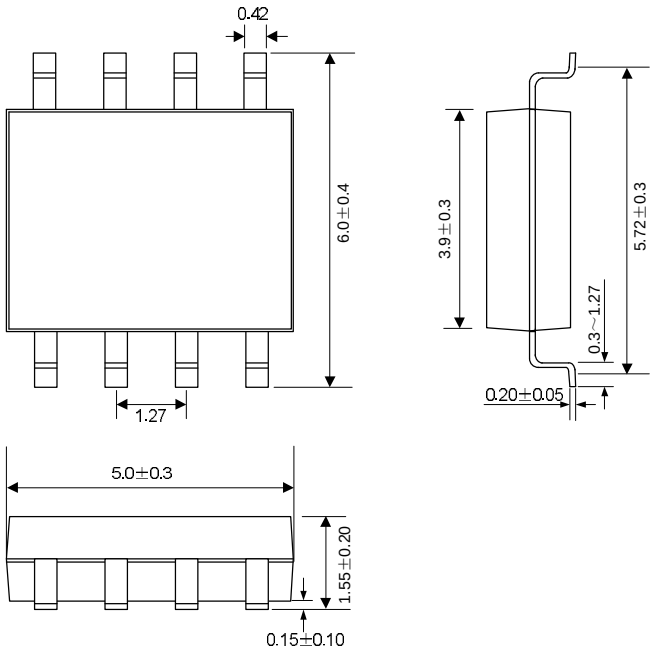


DIP-14-300-2.54 UNIT: mm

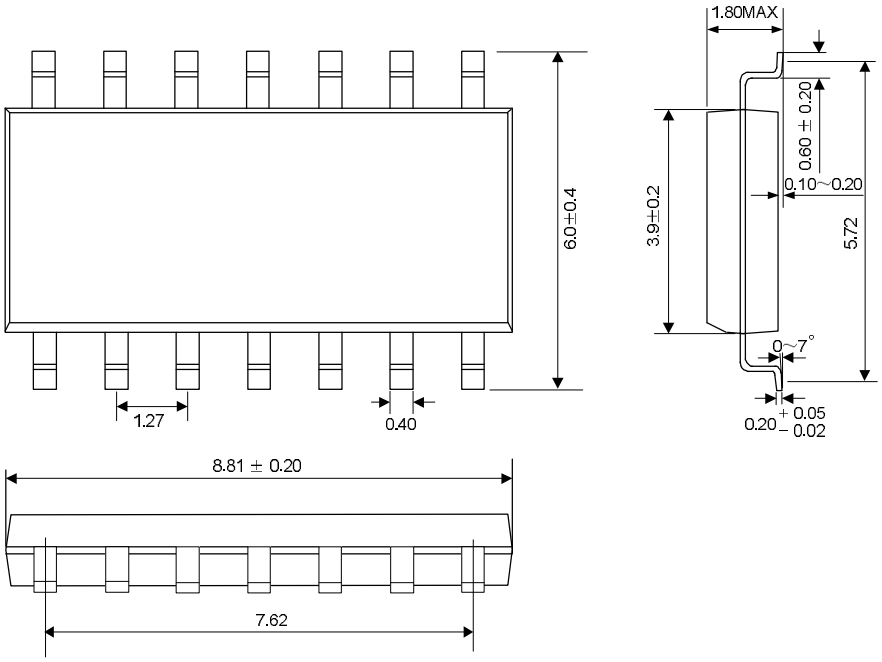


PACKAGE OUTLINE (Continued)

SOP-8-225-1.27 UNIT: mm



SOP-14-225-1.27 UNIT: mm





HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.