KS57C0002/0004
4-BIT CMOS Microcontroller

Product Specification

OVERVIEW

The KS57C0002/0004 single-chip CMOS microcontroller is designed for high-performance using Samsung's newest 4-bit CPU core. With a four-channel comparator, eight LED direct drive pins, serial I/O interface, and a versatile
8-bit timer/countkxcellent design solution for a variety of general-purpose applications.

Up to 24 pins of the 30-pin SDIP package can be dedicated to I/O. Five vectored interrupts provide fast response to internal and external events. In addition, the KS57C0002/0004's advanced CMOS technology ensures low power consumption and a wide operating voltage range.

FEATURES

Memory

- 256 × 4-bit data memory (KS57C0002)
  512 × 4-bit data memory (KS57C0004)
- 2048 × 8-bit program memory (KS57C0002)
  4096 × 8-bit program memory (KS57C0004)

24 I/O Pins

- I/O: 18 pins, including 8 high-current pins
- Input only: 6 pins

Comparator

- 4-channel mode with internal reference (4-bit resolution) and 16-step variable reference voltage
- 3-channel mode with external reference
- 150 mV resolution (minimum)

8-Bit Basic Timer

- Programmable interval timer

8-Bit Timer/Counter

- Programmable interval timer
- External event counter function
- Timer/counter clock output to TCLO0 pin

Watch Timer

- Interval generation: 0.5 s, 3.9ms at 32768 Hz
- Four frequency outputs to the BUZ pin

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive-only mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Bit Sequential Carrier

- Support for 16-bit serial data transfer in arbitrary format

Interrupts

- Two external interrupt vectors
- Three internal interrupt vectors
- Two quasi-interrupts

Memory-Mapped I/O Structure

- Data memory bank 15

Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (system clock stops)

Oscillation Sources

- Crystal, ceramic, or RC for system clock (RC is only for the KS57C0002)
- Crystal, ceramic: 4.19 MHz (typical)
- RC: 1 MHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 μs at 4.19 MHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 2.7 V to 6.0 V

Package Type

- 30 SDIP, 32 SOP

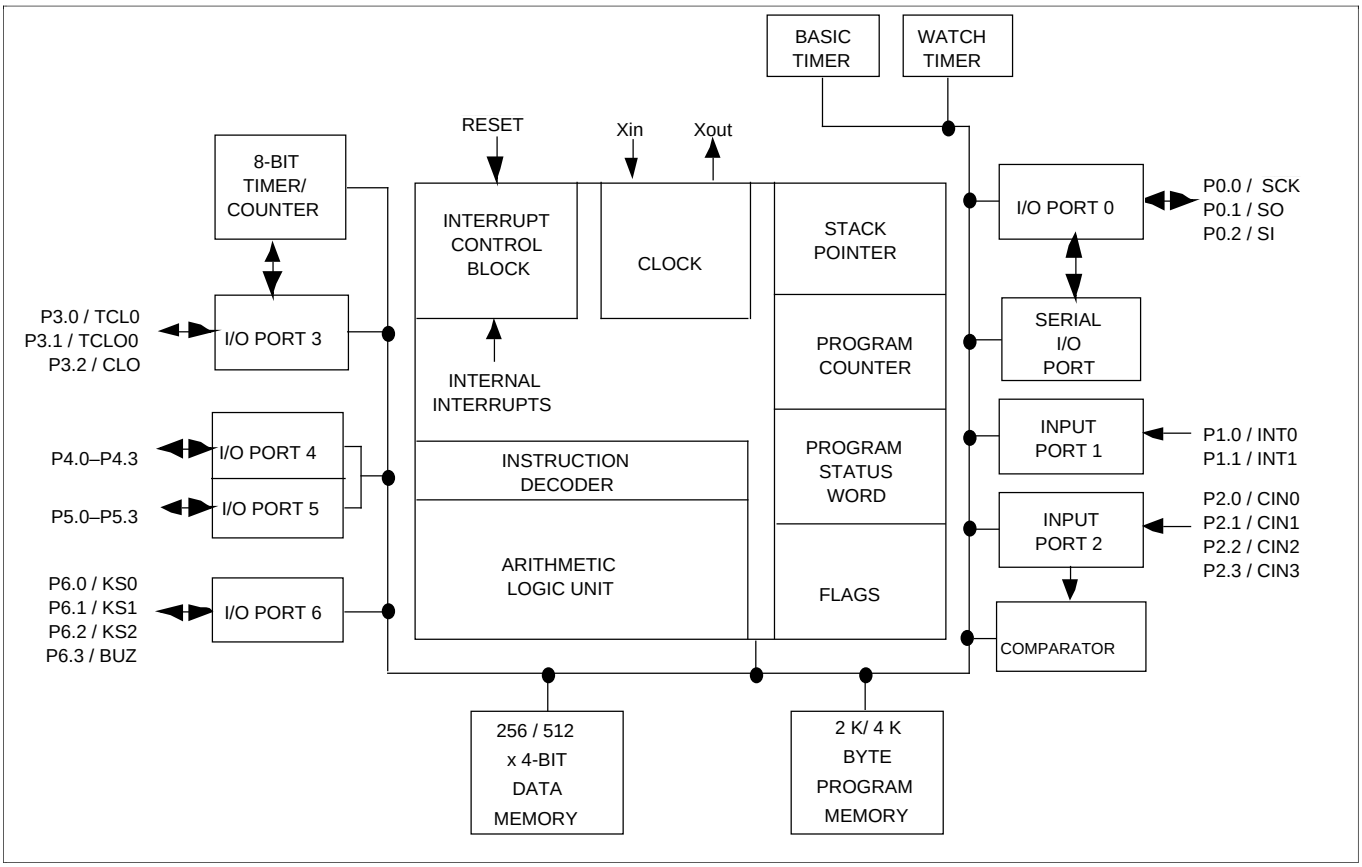


Figure 1. KS57C0002/0004 Block Diagram

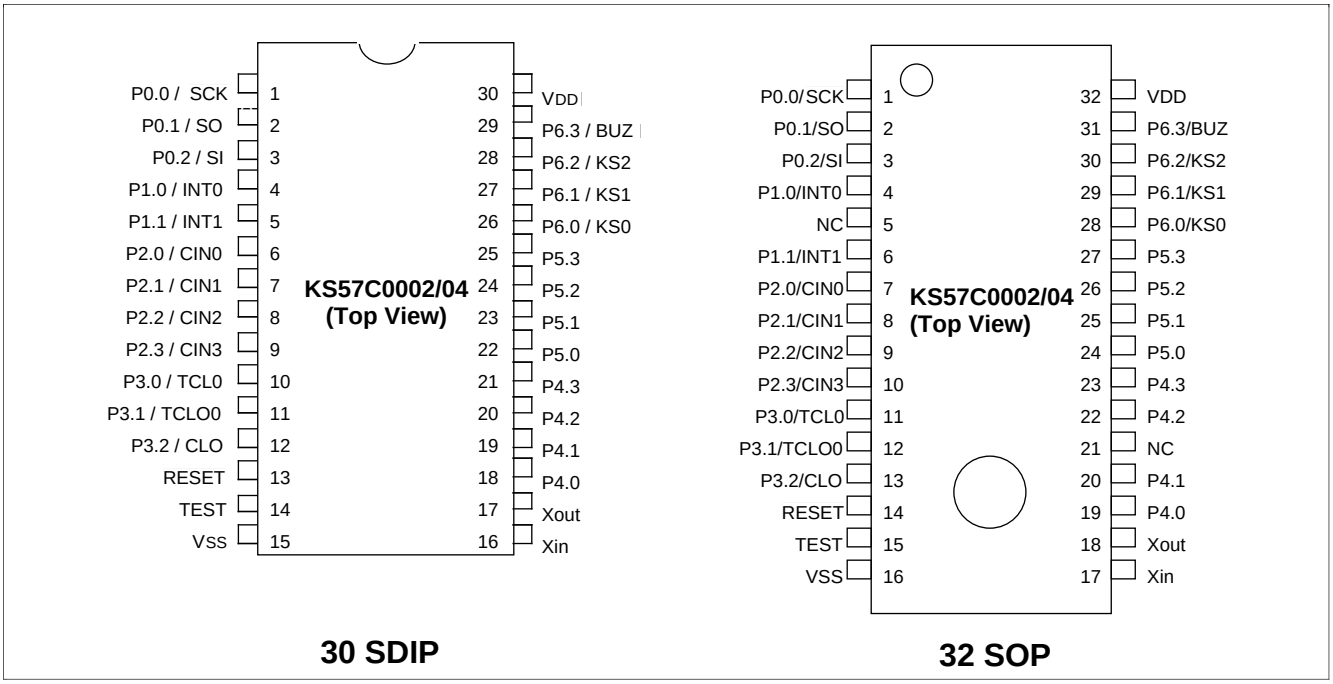


Figure 2. KS57C0002/0004 Pin Assignments (32 SOP, 30 SDIP)

Table 1. KS57C0002/0004 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2	I/O	3-bit I/O port. 1-bit or 3-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output.	1 2 3	SCK SO SI
P1.0 P1.1	I	2-bit input port. 1-bit or 2-bit read and test is possible. Pull-up resistors are assignable by software.	4 5	INT0 INT1
P2.0–P2.3	I	4-bit input port. 1-bit or 4-bit read and test is possible.	6–9	CIN0–CIN3
P3.0 P3.1 P3.2	I/O	Same as port 0	10 11 12	TCL0 TCLO0 CLO
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. 1-, 4-, or 8-bit read/write and test is possible. Pins are individually configurable as input or output. Ports can be configurable as n-channel open-drain by mask option (maximum 9V).	18–21 22–25	—
P6.0 P6.1 P6.2 P6.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins individually configurable as input or output.	26 27 28 29	KS0 KS1 KS2 BUZ
INT0	I	External interrupts with rising/falling edge detection	4	P1.0
INT1	I	External interrupts with rising/falling edge detection	5	P1.1
CIN0–CIN3	I	4-channel comparator input. CIN0–CIN2: comparator input only. CIN3: comparator input or external reference input	6–9	P2.0–P2.3
SCK	I/O	Serial interface clock signal	1	P0.0
SO	I/O	Serial data output	2	P0.1
SI	I/O	Serial data input	3	P0.2
TCL0	I/O	External clock input for timer/counter	10	P3.0
TCLO0	I/O	Timer/counter clock output	11	P3.1
CLO	I/O	CPU clock output	12	P3.2
BUZ	I/O	2 kHz, 4 kHz, 8 kHz, or 16 kHz frequency output at 4.19 MHz for buzzer sound	29	P6.3
KS0–KS2	I/O	Quasi-interrupt input with falling edge detection	26–28	P6.0–P6.2
V_{DD}	—	Main power supply	30	—
V_{SS}	—	Ground	15	—
RESET	I	Reset signal	13	—
TEST	I	Test signal input (must be connected to V_{SS})	14	—
X_{in}, X_{out}	—	Crystal, ceramic, or RC oscillator signal for system clock	16, 17	—

Table 2. Supplemental KS57C0002/0004 Pin Data

Pin Numbers	Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
1, 2, 3	P0.0–P0.2	SCK, SO, SI	I/O	Input	5
4, 5	P1.0, P1.1	INT0, INT1	I	Input	3
6–9	P2.0–P2.3	CIN0–CIN3	I	Input	6, 8 *
10–12	P3.0–P3.2	TCL0, TCLO0, CLO	I/O	Input	5
13	RESET	—	I	—	9
14	TEST	—	I	—	—
15	V_{SS}	—	—	—	—
16, 17	Xin, Xout	—	—	—	—
18–21	P4.0–P4.3	—	I/O	Input	7
22–25	P5.0–P5.3	—	I/O	Input	7
26–29	P6.0–P6.3	KS0, KS1, KS2, BUZ	I/O	Input	5
30	V_{DD}	—	—	—	—

* I/O circuit type 8 is for P2.3 only.

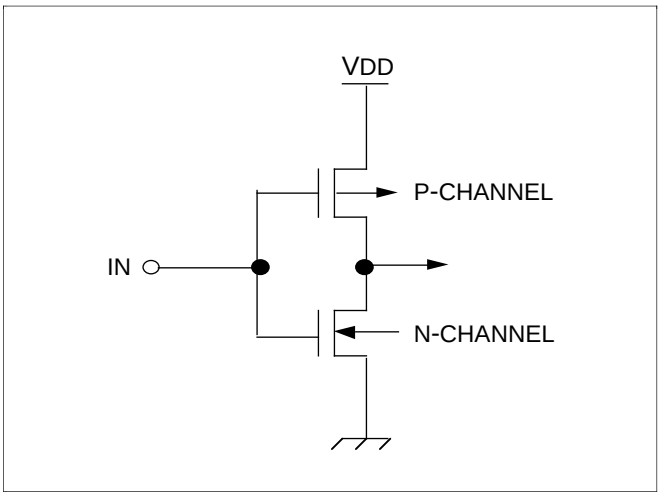


Figure 3. Pin Circuit Type 1

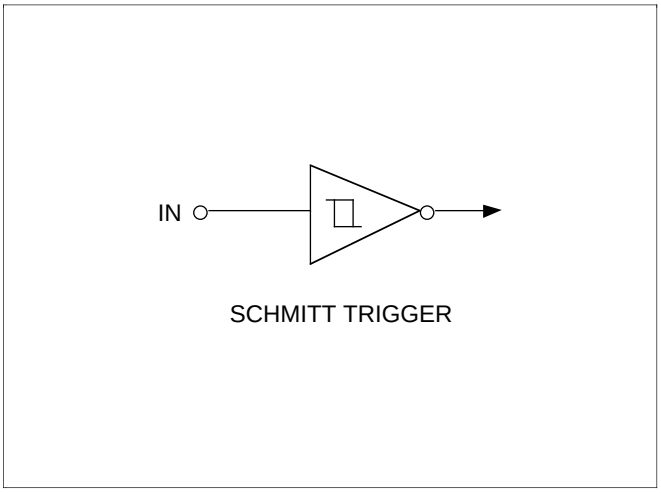


Figure 4. Pin Circuit Type 2

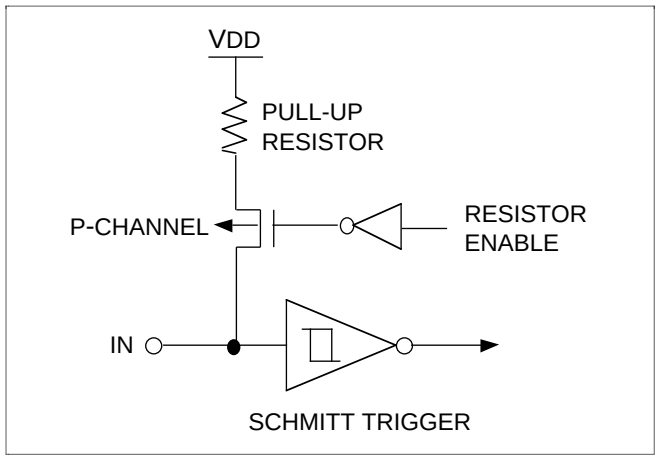


Figure 5. Pin Circuit Type 3

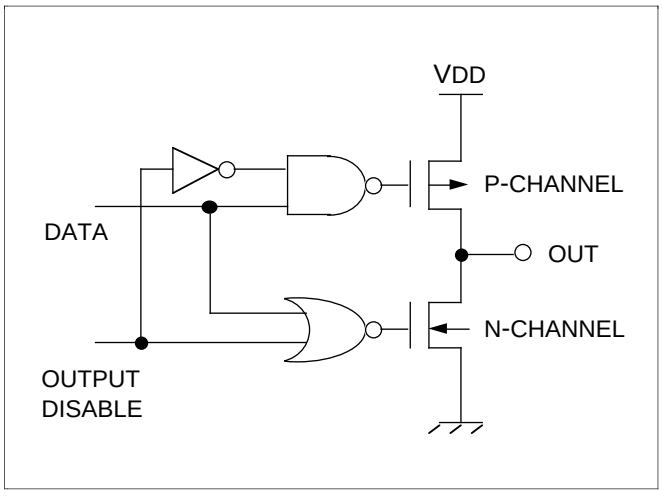


Figure 6. Pin Circuit Type 4

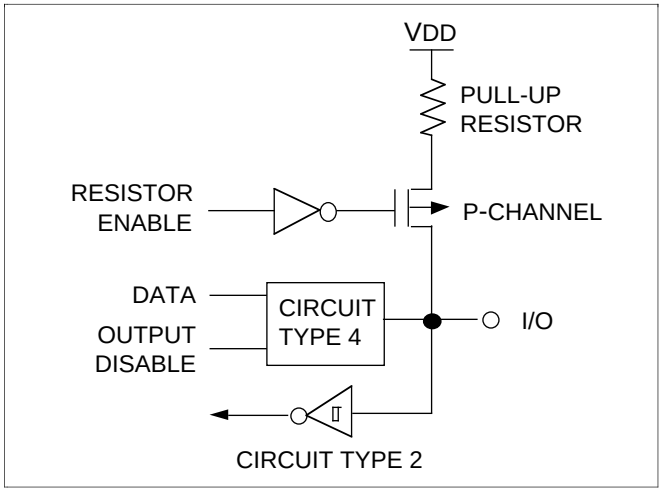


Figure 7. Pin Circuit Type 5

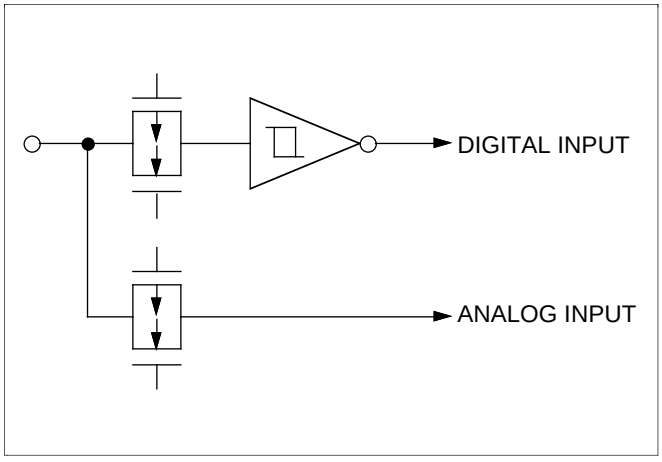


Figure 8. Pin Circuit Type 6

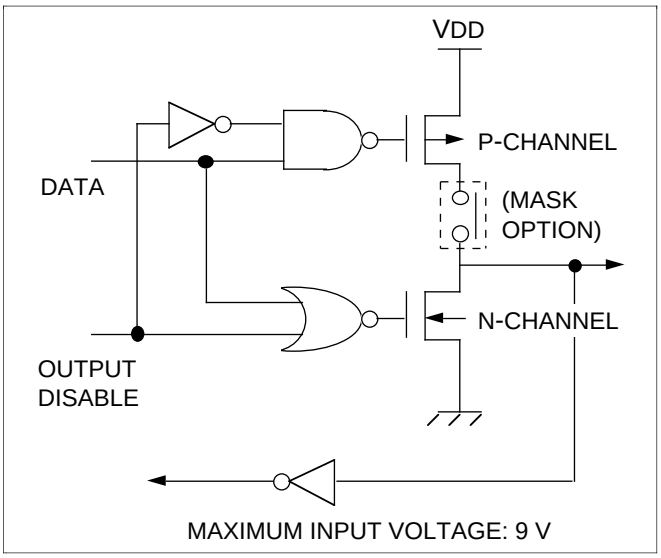


Figure 9. Pin Circuit Type 7

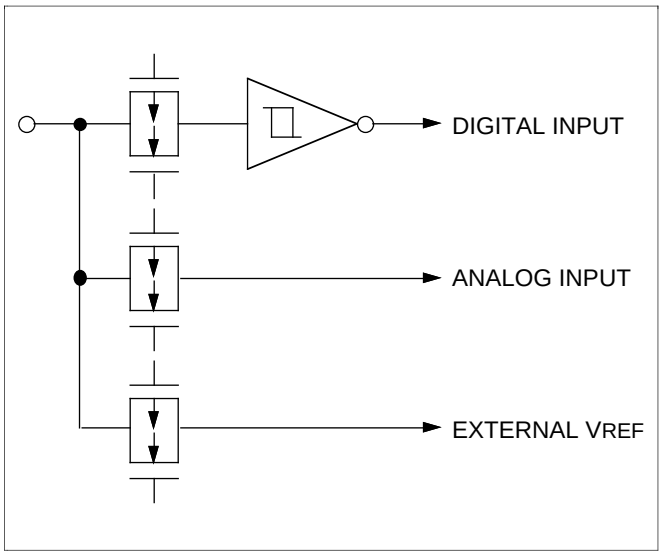


Figure 10. Pin Circuit Type 8

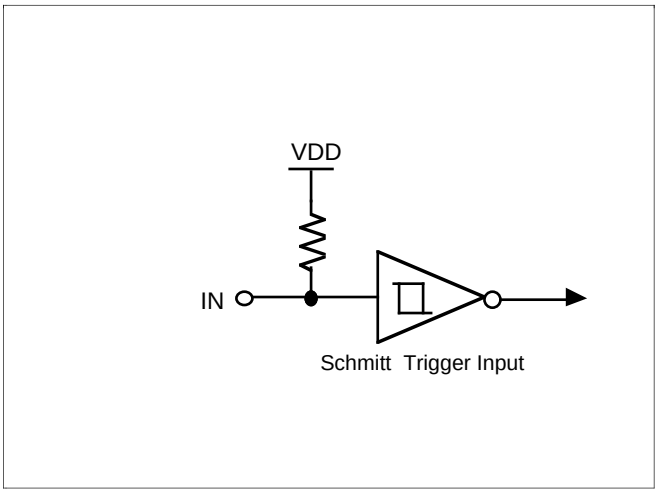


Figure 11. Pin Circuit Type 9

PROGRAM MEMORY (ROM)

ROM maps for KS57C0002/0004 devices are mask programmable at the factory. In their standard configuration, the device's 2048 × 8-bit (KS57C0002), or 4096 × 8-bit (KS57C0004) program memory has four areas that are directly addressable by the program counter (PC):

— 16-byte general-purpose area

— 16-byte area for vector addresses

— 96-byte instruction reference area

— 1920-byte (KS57C0002), 3968-byte (KS57C0004) general-purpose area

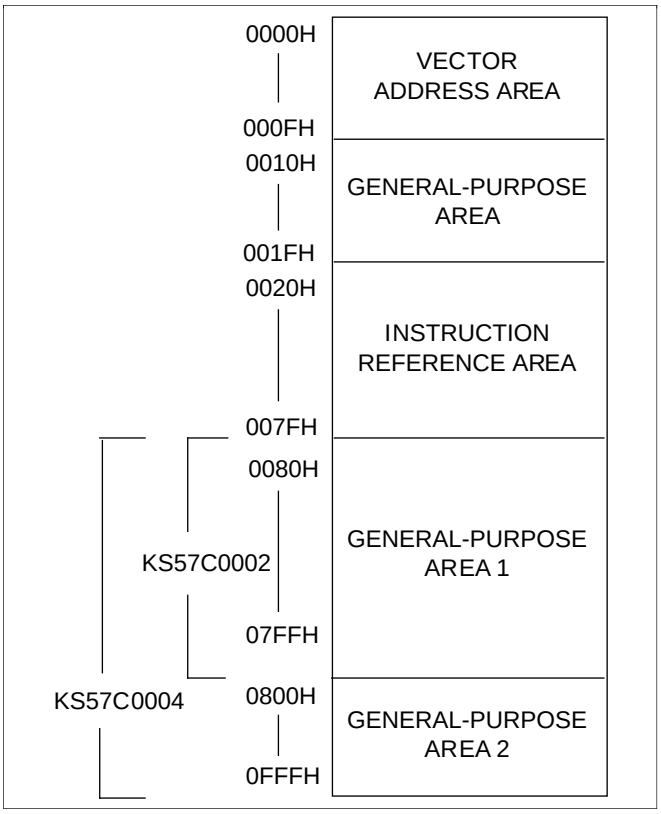


Figure 12. ROM Map

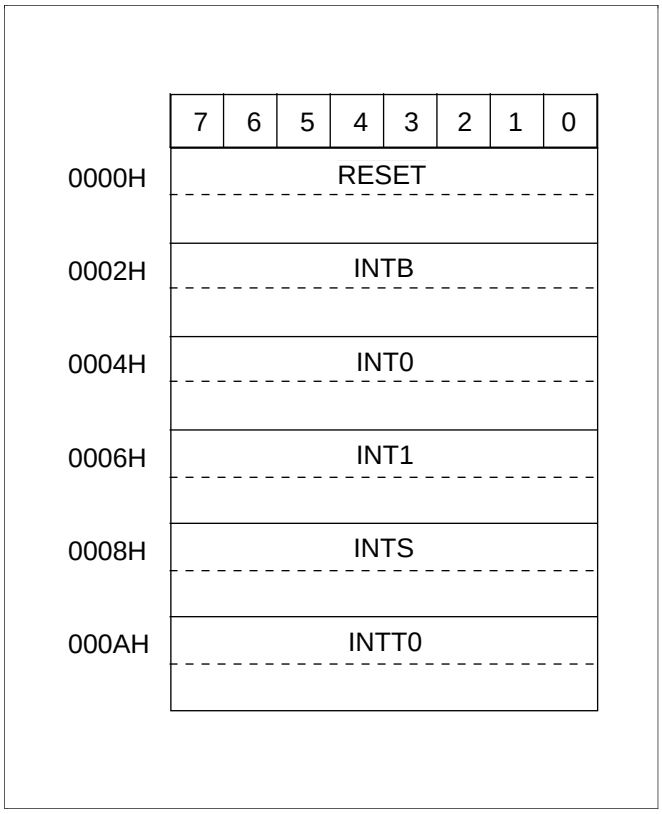


Figure 13. Vector Address Map

DATA MEMORY (RAM)

In its standard configuration, the 256× 4 -bit (KS57C0002), or the 512 ×4-bit (KS57C0004) data memory has four areas:

— 32 ×4-bit working registers

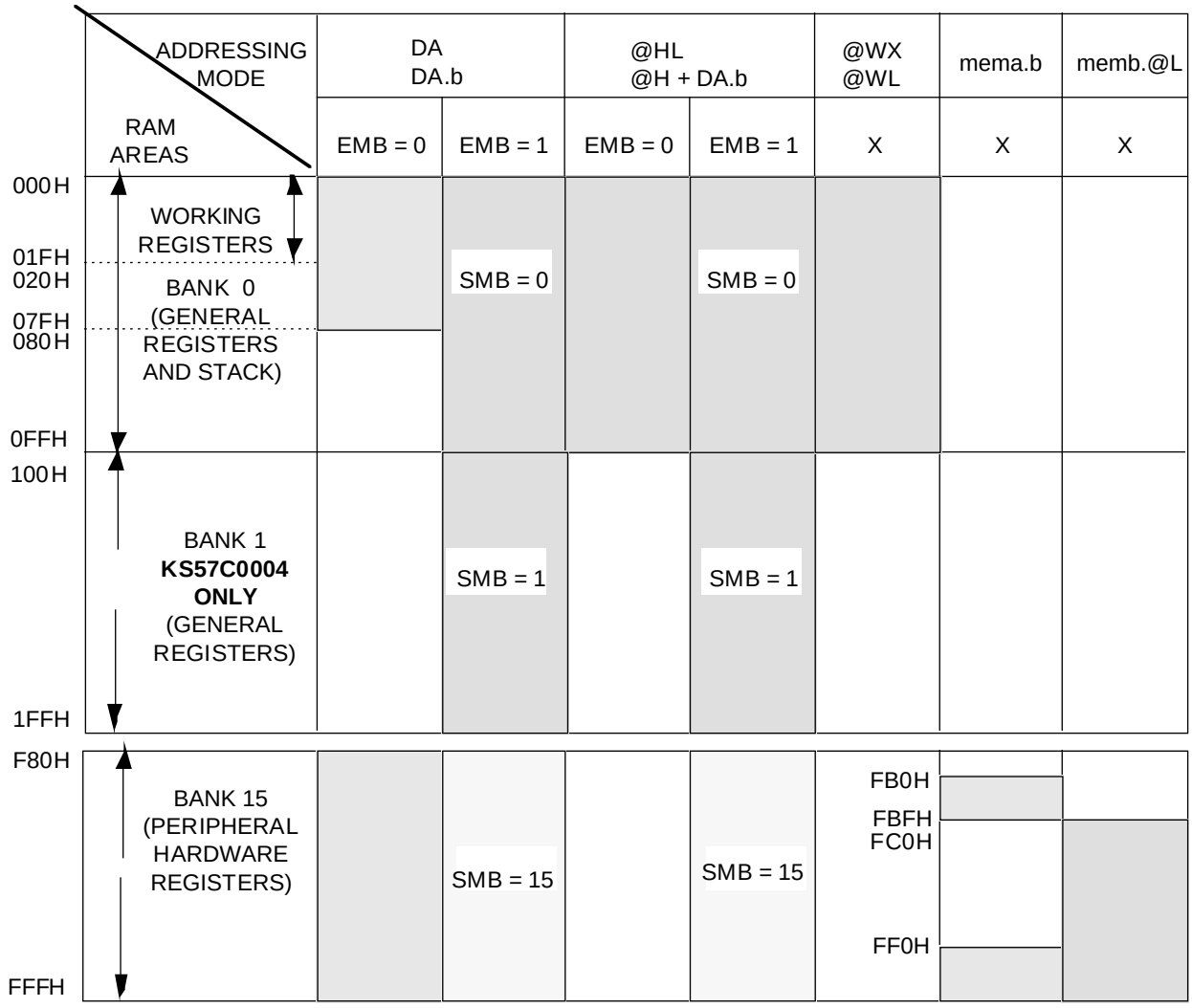
— 224× 4-bit general-purpose area in bank0 which is also used as the stack area

— 256×4 -bit general-purpose area in bank1 **(KS57C0004 only)**

— 128× 4-bit area in bank 15 for memory-mapped I/O addresses

I/O MAP FOR HARDWARE REGISTERS

Table 3 contains detailed information about I/O mapping for peripheral hardware in bank 15 (register locations F80H–FFFH).



NOTES: 1. 'X' means don't care.
2. Blank columns indicate RAM areas that are not addressable, given the addressing method and enable memory bank (EMB) flag setting shown in the column headers.

Figure 14. Data Memory (RAM) Address Structure

Table 3. I/O Map for Memory Bank 15

Memory Bank 15						Addressing Mode			
Address	**Register**	**Name**				**R/W**	**1-Bit**	**4-Bit**	**8-Bit**
F81H–F80H	SP	Stack Pointer				R/W	No	No	Yes
F85H	BMOD	Basic Timer Mode Register				W	.3	Yes	No
F87H–F86H	BCNT	Basic Timer Counter Register				R	No	No	Yes
F89H–F88H	WMOD	Watch Timer Mode Register				W	No	No	Yes
F91H–F90H	TMOD0	Timer/Counter 0 Mode Register				W	.3	No	Yes
F95H–F94H	TCNT0	Timer/Counter 0 Counter Register				R	No	No	Yes
F97H–F96H	TREF0	Timer/Counter 0 Reference Reg				W	No	No	Yes
FB0H	PSW	IS1	IS0	EMB	ERB	R/W	Yes	Yes	Yes
FB1H		C (2)	SC2	SC1	SC0	R	No	No	
FB2H	IPR	SIO Mode Register				W	IME	Yes	No
FB3H	PCON	Power Control Register				W	No	Yes	No
FB4H	IMOD0	External Interrupt 0 Mode Register				W	No	Yes	No
FB5H	IMOD1	External Interrupt 1 Mode Register				W	No	Yes	No
FB6H	IMODK	External Key Interrupt Mode Reg				W	No	Yes	No
FB8H		"0"	"0"	IEB	IRQB	R/W	Yes	Yes	No
FBAH		"0"	"0"	IEW	IRQW	R/W	Yes	Yes	No
FBCH		"0"	"0"	IET0	IRQT0	R/W	Yes	Yes	No
FBDH		"0"	"0"	IES	IRQS				
FBEH		IE1	IRQ1	IE0	IRQ0				
FBFH		"0"	"0"	IEK	IRQK				
FC0H	BSC0	Bit Sequential Carrier 0				R/W	Yes	Yes	Yes
FC1H	BSC1	Bit Sequential Carrier 1							
FC2H	BSC2	Bit Sequential Carrier 2							
FC3H	BSC3	Bit Sequential Carrier 3							
FD0H	CLMOD	Clock Mode Register				W	No	Yes	No
FD4H	CMPREG	Comparison Result Register				R	No	Yes	No
FD7H–FD6H	CMOD	Comparator Mode Register				R/W	No	No	Yes
FDDH–FDCH	PUMOD	Pull-up Mode Register				W	No	No	Yes
FE1H–FE0H	SMOD	SIO Mode Register				W	.3	No	Yes
FE2H	P2MOD	Port 2 Mode Register				W	No	Yes	No
FE5H–FE4H	SBUF	SIO Buffer Register				R/W	No	No	Yes
FE9H–FE8H	PMG1	Port Mode Group 1				W	No	No	Yes
FEBH–FEAH	PMG2	Port Mode Group 2							

Table 3. I/O Map for Memory Bank 15 (Concluded)

Memory Bank 15			Addressing Mode			
Address	**Register**	**Name**	**R/W**	**1-Bit**	**4-Bit**	**8-Bit**
FEDH–FECH	PMG3	Port Mode Group 3	W	No	No	Yes
FF0H	P0	Port 0	R/W	Yes	Yes	No
FF1H	P1	Port 1	R			No
FF2H	P2	Port 2	R			No
FF3H	P3	Port 3	R/W			No
FF4H	P4	Port 4	R/W			Yes
FF5H	P5	Port 5	R/W			
FF6H	P6	Port 6	R/W			No

NOTES:
1. Bit 0 in the WMOD register must be set to "0".
2. The carry flag can be read or written by specific bit manipulation instructions only.

BIT SEQUENTIAL CARRIER (BSC)

The bit sequential carrier (BSC) is a 16-bit general register that is mapped in data memory bank 15. Using the BSC, you can specify sequential addresses and bit locations using 1-bit indirect addressing (memb.@L).

BSC bit addressing is independent of the current EMB value. In this way, programs can process 16-bit data by moving the bit location sequentially and then incrementing or decrementing the value of the L register.

For 8-bit manipulations, the 4-bit register names BSC0 and BSC2 must be specified and the upper and lower 8 bits manipulated separately. If the values of the L register are 0H at BSC0.@L, the address and bit location assignment is FC0H.0. If the L register content is FH at BSC0.@L, the address and bit location assignment is FC3H.3.

Table 4. BSC Register Organization

Name	Address	Bit 3	Bit 2	Bit 1	Bit 0
BSC0	FC0H	BSC0.3	BSC0.2	BSC0.1	BSC0.0
BSC1	FC1H	BSC1.3	BSC1.2	BSC1.1	BSC1.0
BSC2	FC2H	BSC2.3	BSC2.2	BSC2.1	BSC2.0
BSC3	FC3H	BSC3.3	BSC3.2	BSC3.1	BSC3.0

☞ **PROGRAMMING TIP — Using the BSC Register to Output 16-Bit Data**

To use the bit sequential carrier (BSC) register to output 16-bit data (5937H) to the P3.0 pin:

```
        BITS    EMB
        SMB     15
        LD      EA,#37H         ;
        LD      BSC0,EA         ;   BSC0 ← A, BSC1 ← E
        LD      EA,#59H         ;
        LD      BSC2,EA         ;   BSC2 ← A, BSC3 ← E
        SMB     0
        LD      L,#0H           ;
AGN LDB C,BSC0.@L               ;
        LDB     P3.0,C          ;   P3.0 ← C
        INCS    L
        JR      AGN
        RET
```

INTERRUPTS

The KS57C0002/0004 microcontroller has two external interrupts, three internal interrupts, and two quasi-interrupts. Table 5 shows the conditions for each interrupt generation. The request flags that actually generate these interrupts are cleared by hardware when the service routine is vectored. However, the quasi-interrupt's request flags must be cleared by software.

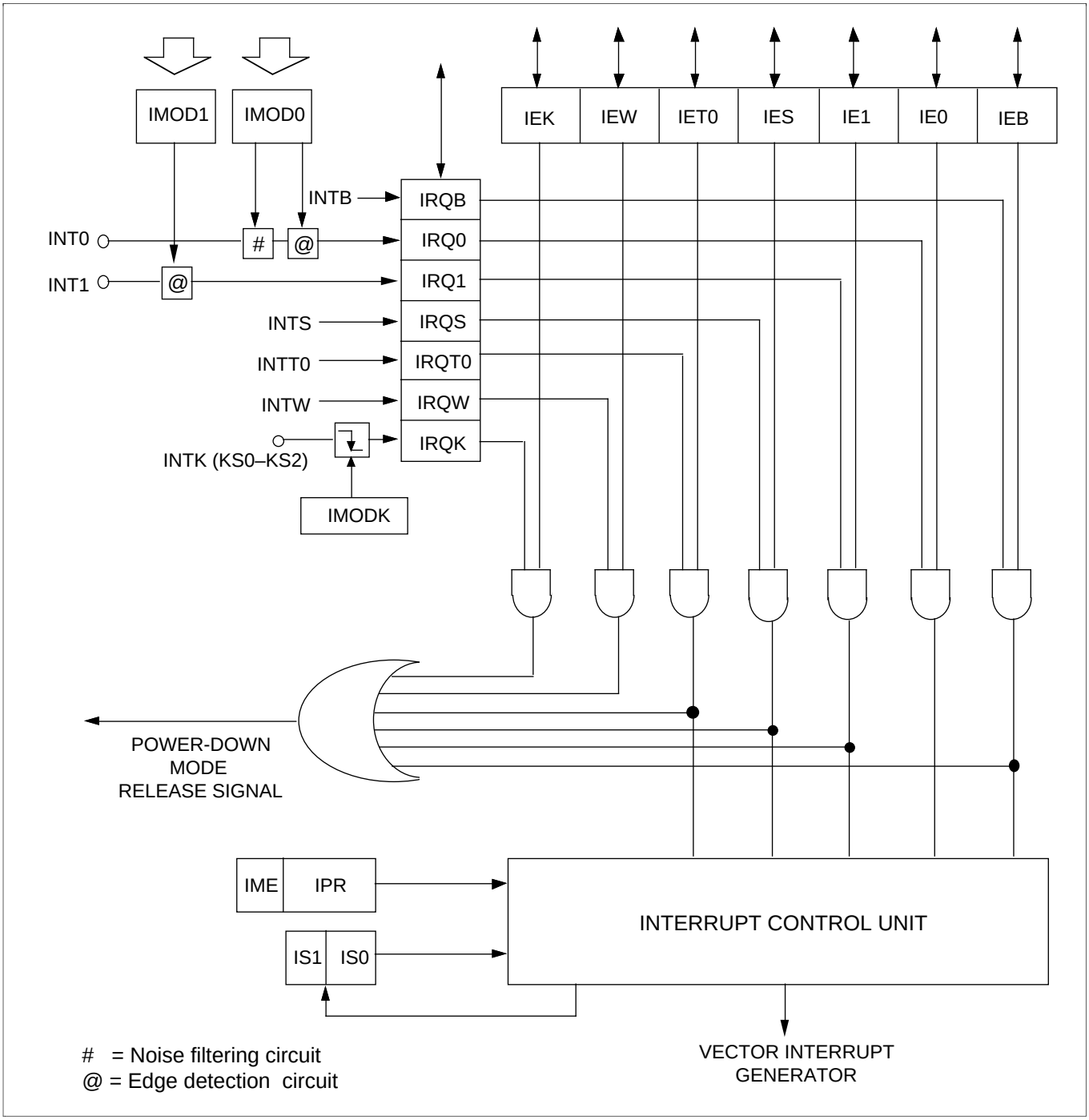


Figure 15. Interrupt Control Circuit Diagram

Table 5. Interrupt Request Flag Conditions and Priorities

Interrupt Source	Internal / External	Condition for IRQx Flag Setting	Interrupt Priority	Request Flag Name
INTB	I	Reference time interval signal from basic timer	1	IRQB
INT0	E	Rising or falling edge detected at INT0 pin	2	IRQ0
INT1	E	Rising or falling edge detected at INT1 pin	3	IRQ1
INTS	I	Completion signal for serial transmit-and-receive or receive-only operation	4	IRQS
INTT0	I	Signals for TCNT0 and TREF0 registers match	5	IRQT0
INTK *	E	Falling edge is detected at any of the KS0–KS2 pins	—	IRQK
INTW *	I	Time interval of 0.5 s or 3.19 ms	—	IRQW

* The INTK and INTW are quasi-interrupts and INTK are used only for testing incoming signals.

INTERRUPT ENABLE FLAGS (IEx)

IEx flags, when set to "1", enable specific interrupt requests to be serviced. When the interrupt request flag is set to "1", an interrupt will not be serviced until its corresponding IEx flag is also enabled. The IPR register contains a global disable bit, IME, which disables all interrupt at once.

Table 6. Interrupt Enable and Request Flag

Address	Bit 3	Bit 2	Bit 1	Bit 0
FB8H	0	0	IEB	IRQB
FBAH	0	0	IEW	IRQW
FBBH	0	0	0	0
FBCH	0	0	IET0	IRQT0
FBDH	0	0	IES	IRQS
FBEH	IE1	IRQ1	IE0	IRQ0
FBFH	0	0	IEK	IRQK

NOTES:
1. IEx refers to all interrupt enable flags.
2. IRQx refers to all interrupt request flags.
3. IEx = "0" is interrupt disable mode.
4. IEx = "1" is interrupt enable mode.

INTERRUPT PRIORITY

Each interrupt source can also be individually programmed to high levels by modifying the IPR register. When IS1 = 0 and IS0 = 1, a low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt.

If you clear the interrupt status flags (IS1 and IS0) to "0" in a interrupt service routine, a high-priority interrupt can be interrupted by low-priority interrupt (multi-level interrupt). Before the IPR can be modified by 4-bit write instructions, all interrupts must first be disabled by a DI instruction.

When all interrupts are low priority (the lower three bits of the IPR register are "0"), the interrupt requested first will have high priority. Therefore, the first-requested interrupt cannot be superseded by any other interrupt.

If two or more interrupt requests are received simultaneously, the priority level is determined according to the standard interrupt priorities, where the default priority is assigned by hardware when the lower three IPR bits = "0".

In this case, the higher-priority interrupt request is serviced and the other interrupt is inhibited. Then, when the high-priority interrupt is returned from its service routine by an IRET instruction, the inhibited service routine is started.

Table 7. Interrupt Priority Register Settings

IPR.2	IPR.1	IPR.0	Result of IPR Bit Setting
0	0	0	Process all interrupt requests at low priority.
0	0	1	INTB
0	1	0	INT0
0	1	1	INT1
1	0	0	INTS
1	0	1	INTT0

Table 8. Default Priorities

Source	Default Priority
INTB	1
INT0	2
INT1	3
INTS	4
INTT0	5

EXTERNAL INTERRUPTS

The external interrupt mode registers (IMOD0 and IMOD1) are used to control the triggering edge of the input signal at the INT0 and INT1 pins, respectively.

When a sampling clock rate of fx/64 is used for INT0, an interrupt request flag must be cleared before 16 machine cycles have elapsed. Since the INT0 pin has a clock-driven noise filtering circuit built into it, please take the following precautions when you use it:

— To trigger an interrupt, the input signal width at INT0 must be at least two times wider than the pulse width of the clock selected by IMOD0. This is true even when the INT0 pin is used for general-purpose input.

— Since the INT0 input sampling clock does not operate during Stop or Idle mode, you cannot use INT0 to release power-down mode.

When modifying the IMOD0 and IMOD1 registers, it is possible to accidentally set an interrupt request flag.

To avoid unwanted interrupts, take these precautions when writing your programs:

1. Disable all interrupts with a DI instruction.
2. Modify the IMOD0 or IMOD1 register.
3. Clear all relevant interrupt request flags.
4. Enable the interrupt by setting the appropriate IEx flag.
5. Enable all interrupts with an EI instructions.

Table 9. IMOD0 and IMOD1 Register Organization (4-Bit W)

IMOD0.3	0	IMOD0.1	IMOD0.0	Effect of IMOD0 Settings
0				Select CPU clock for sampling
1				Select fx/64 sampling clock
	0	0	0	Rising edge detection
	0	0	1	Falling edge detection
	0	1	0	Both rising and falling edge detection
	0	1	1	IRQ0 flag cannot be set to "1"

0	0	0	IMOD1.0	Effect of IMOD1 Settings
0	0	0	0	Rising edge detection
0	0	0	1	Falling edge detection

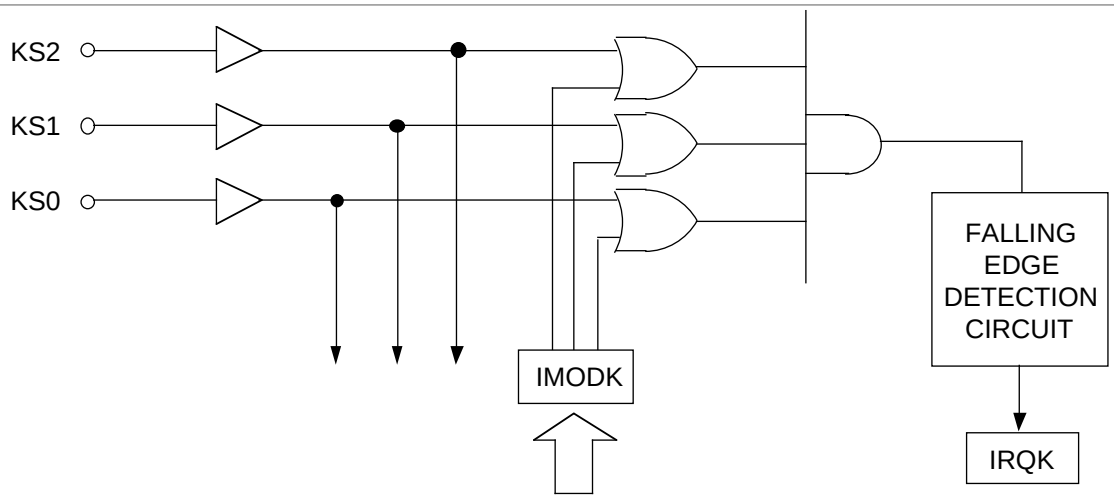
EXTERNAL KEY INTERRUPT MODE REGISTER

The external key interrupt (INTK) mode register, IMODK, is used to select KS pins as interrupt input pins. When a falling edge is detected at one of the KS0–KS2 pins, the IRQK flag is set to "1". This generates an interrupt request and a release signal for power-down mode. To generate a key interrupt on a falling signal edge at KS0–KS2, all of the KS0–KS2 pins must be configured to input mode.

If one or more of the pins which are configured as key Interrupt (KS0–KS2) are in Low input or Low output state, the key Interrupt can not be occurred.

Table 10. IMODK Register Bit Settings (4-Bit W)

0	IMODK.2	IMODK.1	IMODK.0	Effect of IMODK Settings
0	0	0	0	Disable key interrupt
0	0	0	1	Select falling edge at KS0
0	0	1	0	Select falling edge at KS1
0	0	1	1	Select falling edge at KS0–KS1
0	1	0	0	Select falling edge at KS2
0	1	0	1	Select falling edge at KS0, KS2
0	1	1	0	Select falling edge at KS1–KS2
0	1	1	1	Select falling edge at KS0–KS2



NOTE: To generate a key interrupt on a falling edge at KS0–KS2, all KS0–KS2 pins must be configured to input mode.

Figure 15-1. Circuit diagram for KS0-KS2 Pins

OSCILLATOR CIRCUITS

The KS57C0002/0004 system clock circuit is shown in Figure 16 below. By manipulating bits 1 and 0 of the PCON register, the system clock frequency can be divided by 4, 8, or 64.

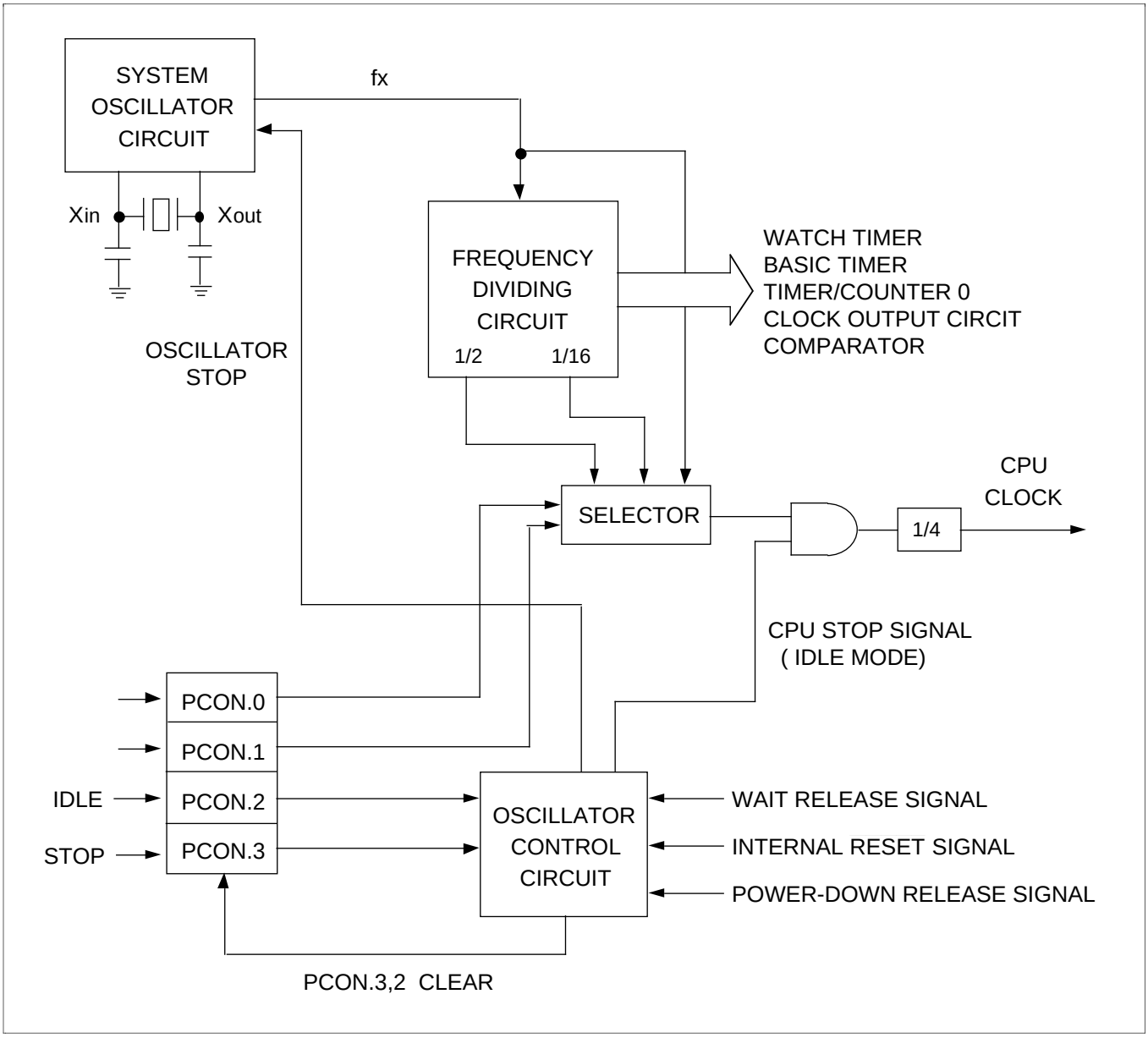


Figure 16. Clock Circuit Diagram

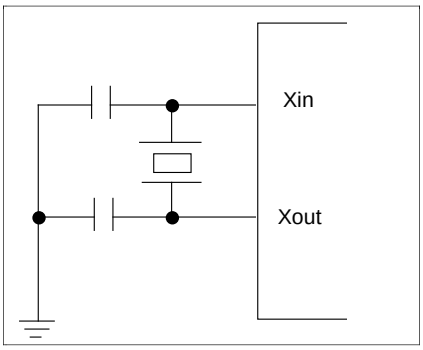


Figure 17. Crystal/Ceramic Oscillator

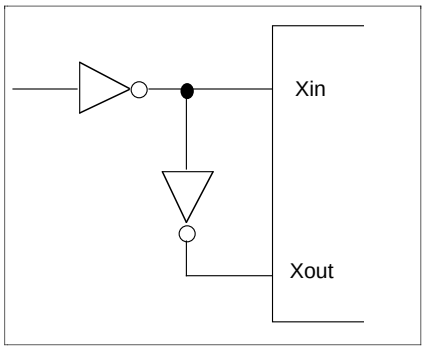


Figure 18. External Clock

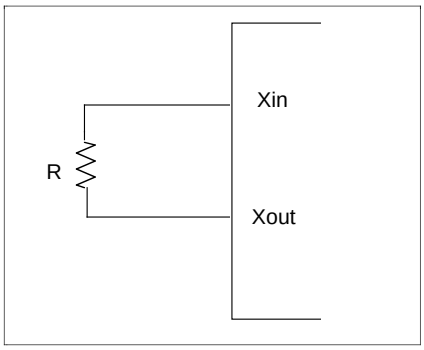


Figure 19. RC Oscillator (only for the KS57C0002)

POWER CONTROL REGISTER (PCON)

The power control register, PCON, is used to select the CPU clock frequency and to control CPU operating and power-down modes. PCON bits 3 and 2 are controlled by the STOP and IDLE instructions, which engage the Stop and Idle power-down modes, respectively. Using these instructions, you can initiate a power-down mode at any time, regardless of the current value of the enable memory bank flag (EMB).

Table 11. Power Control Register (PCON) Organization (4-Bit W)

PCON Bit Settings		Resulting CPU Operating Mode
PCON.3	PCON.2	
0	0	Normal CPU operating mode
0	1	Idle power-down mode
1	0	Stop power-down mode

PCON Bit Settings		Resulting CPU Clock Frequency
PCON.1	PCON.0	
0	0	fx/64
1	0	fx/8
1	1	fx/4

☞ **PROGRAMMING TIP — Setting the CPU Clock**

To set the CPU clock to 0.95 μs at 4.19 MHz:

```
BITS    EMB
SMB     15
LD      A,#3H
LD      PCON,A
```

INSTRUCTION CYCLE TIMES

The unit of time that equals one machine cycle varies depending on how the oscillator clock signal is divided.

Table 12. Instruction Cycle Times for CPU Clock Rates

Selected CPU Clock	Resulting Frequency	Oscillation Source	Cycle Time (μs)
fx/64	65.5 kHz	fx = 4.19 MHz	15.3
fx/8	524.0 kHz		1.91
fx/4	1.05 MHz		0.95

CLOCK OUTPUT CIRCUIT

The clock output circuit outputs clock pulses to the CLO pin. The clock output mode register, CLMOD, is used to enable or disable clock output to the CLO pin and to select the CPU clock source and frequency. To output a frequency, the clock output pin CLO/P3.2 must be set to output mode and the pin's latch must be cleared to "0". Bit 2 in the CLMOD register must always be "0".

Table 13. Clock Output Mode Register (CLMOD) Organization

CLMOD Bit Settings		Resulting Clock Output	
CLMOD.1	CLMOD.0	Clock Source	Frequency
0	0	CPU clock (fx/4, fx/8, fx/64)	1.05 MHz, 524 kHz, 65.5 kHz
0	1	fx/8	524 kHz
1	0	fx/16	262 kHz
1	1	fx/64	65.5 kHz

CLMOD.3	Result of CLMOD.3 Setting
0	Clock output is disabled
1	Clock output is enabled

NOTE: Frequencies assume that fx = 4.19 MHz.

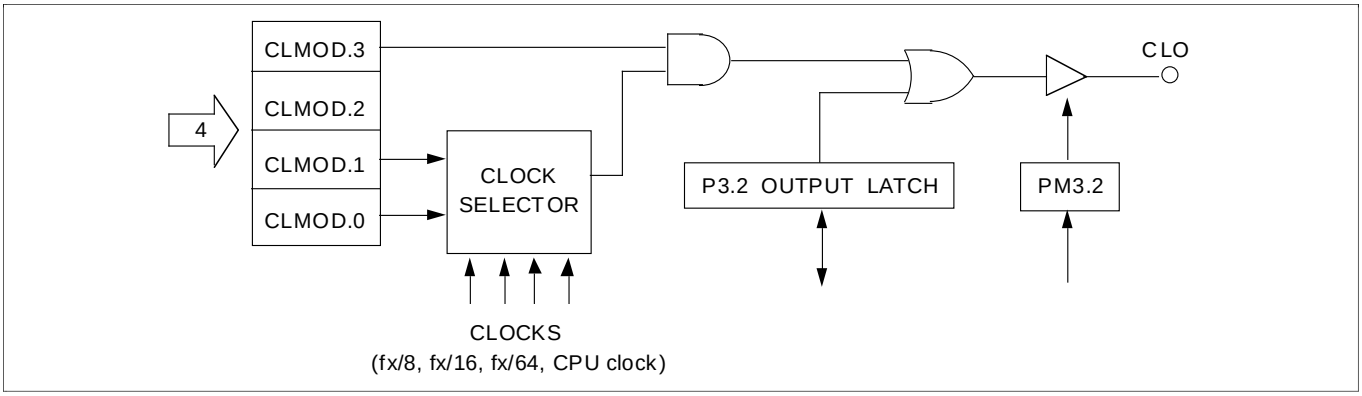


Figure 20. CLO Output Pin Circuit Diagram

☞ **PROGRAMMING TIP — CPU Clock Output to the CLO Pin**

To output the CPU clock to the CLO pin:

```
BITS    EMB                 ;   Or BITR EMB
SMB     15
LD      EA,#40H
LD      PMG1,EA             ;   P3.2 ← Output mode
BITR    P3.2                ;   Clear P3.2 output latch
LD      A,#9H
LD      CLMOD,A
```

POWER-DOWN

The KS57C0002/0004 microcontroller has two power-down modes to reduce power consumption: Idle and Stop. In Idle mode, the CPU clock stops while peripherals and the oscillator continue to operate normally.

In Stop mode, system clock oscillation is halted (assuming it is currently operating), and peripheral hardware components are powered-down. The effect of Stop mode on specific peripheral hardware components — CPU, basic timer, serial I/O, timer/counters 0, and watch timer — and on external interrupt requests, is detailed in Table 14.

Table 14. Hardware Operation During Power-Down Modes

Operation	Stop Mode (STOP)	Idle Mode (IDLE)
Clock oscillator	System clock oscillation stops	CPU clock oscillation stops (system clock oscillation continues)
Basic timer	Basic timer stops	Basic timer operates (with IRQB set at each reference interval)
Serial interface	Operates only if external SCK input is selected as the serial I/O clock	Operates if a clock other than the CPU clock is selected as the serial I/O clock
Timer/counter 0	Operates only if TCL0 is selected as the counter clock	Timer/counter 0 operates
Comparator	Comparator operation is stopped	Comparator operates
Watch timer	Watch timer operation is stopped	Watch timer operates
External interrupts	INT1 and INTK are acknowledged; INT0 is not serviced	INT1 and INTK are acknowledged; INT0 is not serviced
CPU	All CPU operations are disabled	All CPU operations are disabled
Power-down mode release signal	Interrupt request signals (except INT0) are enabled by an interrupt enable flag or by RESET input	Interrupt request signals (except INT0) are enabled by an interrupt enable flag or by RESET input

RECOMMENDED CONNECTIONS FOR UNUSED PINS

To reduce overall power consumption, please configure unused pins according to the guidelines described in Table 15.

Table 15. Unused Pin Connections for Reduced Power Consumption

Pin/Share Pin Names	Recommended Connection
P0.0 / SCK P0.1 / SO P0.2 / SI	Input mode: Connect to V_{DD} Output mode: Do not connect
P1.0 / INT0 – P1.1 / INT1	Connect to V_{DD}
P2.0 / CIN0 P2.1 / CIN1 P2.2 / CIN2 P2.3 / CIN3	Connect to V_{DD}
P3.0 / TCLO0 P3.1 / TCLO1 P3.2 / CLO P3.3 / BUZ P4.0–P4.3, P5.0–P5.3 P6.0 / KS0 – P6.3 / BUZ	Input mode: Connect to V_{DD} Output mode: Do not connect
TEST	Connect to V_{SS}

RESET

Table 16 provides detailed information about hardware register values after a RESET occurs during power-down mode or during normal operation.

Table 16. Hardware Register Values After RESET

Hardware Component or Subcomponent	If RESET Occurs During Power-Down Mode	If RESET Occurs During Normal Operation
Program counter (PC)	Lower three bits of address 0000H are transferred to PC10–8, and the contents of 0001H to PC7–0.	Lower three bits of address 0000H are transferred to PC10–8, and the contents of 0001H to PC7–0.
Program Status Word (PSW):		
Carry flag (C)	Retained	Undefined
Skip flag (SC0–SC2)	0	0
Interrupt status flags (IS0, IS1)	0	0
Bank enable flags (EMB, ERB)	Bit 6 of address 0000H in program memory is transferred to the ERB flag, and bit 7 of the address to the EMB flag.	Bit 6 of address 0000H in program memory is transferred to the ERB flag, and bit 7 of the address to the EMB flag.
Stack pointer (SP)	Undefined	Undefined

Table 16. Hardware Register Values After RESET (Continued)

Hardware Component or Subcomponent	If RESET Occurs During Power-Down Mode	If RESET Occurs During Normal Operation
Data Memory (RAM):		
General registers E, A, L, H, X, W, Z, Y	Values retained	Undefined
General-purpose registers	Values retained (Note 1)	Undefined
Bank selection registers (SMB, SRB)	0, 0	0, 0
BSC register (BSC0–BSC3)	0	0
Clocks:		
Power control register (PCON)	0	0
Clock output mode register (CLMOD)	0	0
Interrupts:		
Interrupt request flags (IRQx)	0	0
Interrupt enable flags (IEx)	0	0
Interrupt priority flag (IPR)	0	0
Interrupt master enable flag (IME)	0	0
INT0 mode register (IMOD0)	0	0
INT1 mode register (IMOD1)	0	0
INTK mode register (IMODK)	0	0
I/O Ports:		
Output buffers	Off	Off
Output latches	0	0
Port mode flags (PM)	0	0
Pull-up resistor mode reg (PUMOD)	0	0
Port 2 mode register (PWMOD)	0	0
Basic Timer:		
Count register (BCNT)	Undefined	Undefined
Mode register (BMOD)	0	0
Timer/Counter 0:		
Count registers (TCNT0)	0	0
Reference registers (TREF0)	FFH, FFFFH	FFH, FFFFH
Mode registers (TMOD0)	0	0
Output enable flags (TOE0)	0	0

Note1: The values of the 0F8H-0FDH are not retained when a RESET signal is input.

Table 16. Hardware Register Values After RESET (Continued)

Hardware Component or Subcomponent	If RESET Occurs During Power-Down Mode	If RESET Occurs During Normal Operation
Watch Timer:		
Watch timer mode register (WMOD)	0	0
Comparator		
Comparator mode register (CMOD)	0	0
Comparison result register	Undefined	Undefined
Serial I/O Interface:		
SIO mode register (SMOD)	0	0
SIO interface buffer (SBUF)	Values retained	Undefined

I/O PORTS

The KS57C0002/0004 has two input ports and five I/O ports. There are total of 6 input pins and 18 configurable I/O pins, including 8 high-current I/O pins. This gives a total number of 24 I/O pins.

PORT MODE FLAGS (PM FLAGS)

Port mode flags (PM) are used to configure I/O ports 0 and 3–6 to input or output mode. It does this by setting or clearing the corresponding I/O buffer. If a PM bit is "0", the corresponding I/O pin is set to input mode. If the PM bit is "1", the corresponding pin is set to output mode.

Table 17. Port Mode Flag Map

PM Group ID	Address	Bit 3	Bit 2	Bit 1	Bit 0
PMG1	FE8H	"0"	PM0.2	PM0.1	PM0.0
	FE9H	"0"	PM3.2	PM3.1	PM3.0
PMG2	FEAH	PM4.3	PM4.2	PM4.1	PM4.0
	FEBH	"0"	"0"	"0"	"0"
PMG3	FECH	PM5.3	PM5.2	PM5.1	PM5.0
	FEDH	PM6.3	PM6.2	PM6.1	PM6.0

☞ PROGRAMMING TIP — Configuring I/O Ports as Input or Output

Configure P0.0 and P3.0 as an output port and the other ports as input ports:

```
BITS    EMB
SMB     15
LD      EA,#11H
LD      PMG1,EA         ;   P0.0 and P3.0 ← Output
LD      EA,#00H
LD      PMG2,EA         ;   P4 ← Input
LD      EA,#00H
LD      PMG3,EA         ;   P5, P6 ← Input
```

PORT 2 MODE REGISTER (P2MOD)

P2MOD register settings determine if port 2 is used either for analog input or for digital input.

FE2H 4-Bit W

P2MOD.3	P2MOD.2	P2MOD.1	P2MOD.0

When a P2MOD bit is set to "1", the corresponding pin is configured as a digital input pin. When set to "0", configured as an analog input pin: P2MOD.0 for P2.0, P2MOD.1 for P2.1, P2MOD.2 for P2.2, and P2MOD.3 for P2.3.

PULL-UP RESISTOR MODE REGISTER (PUMOD)

The pull-up resistor mode register, PUMOD, is used to assign internal pull-up resistors to specific I/O ports. When a configurable I/O port pin is used as an output pin, its assigned pull-up resistor is automatically disabled, even though the pin's pull-up is enabled by a corresponding PUMOD bit setting.

When bit = "1", a pull-up resistor is assigned to the corresponding I/O port: PUMOD.3 for port 3, PUMOD.6 for port 6, and so on.

Table 18. Pull-Up Resistor Mode Register (PUMOD) Organization (8-Bit W)

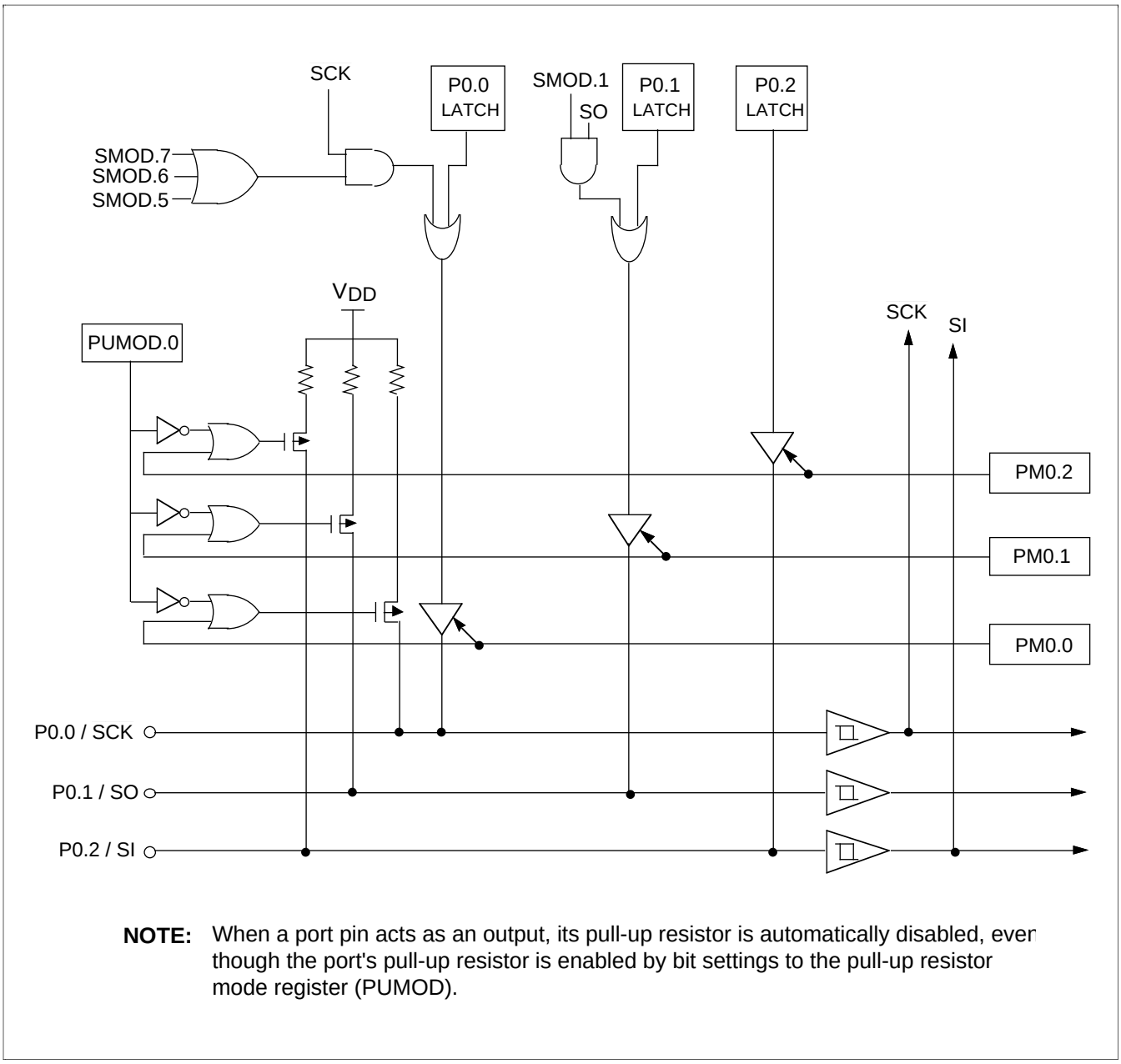
Address	Bit 3	Bit 2	Bit 1	Bit 0
FDCH	PUMOD.3	"0"	PUMOD.1	PUMOD.0
FDDH	"0"	PUMOD.6	"0"	"0"

☞ PROGRAMMING TIP — Enabling and Disabling I/O Port Pull-Up Resistors

P6 enable pull-up resistors, P0, P1, and P3 disable pull-up resistors.

```
BITS    EMB
SMB     15
LD      EA,#40H
LD      PUMOD,EA        ;   P6 enable
```

PORT 0 CIRCUIT DIAGRAM



NOTE: When a port pin acts as an output, its pull-up resistor is automatically disabled, even though the port's pull-up resistor is enabled by bit settings to the pull-up resistor mode register (PUMOD).

Figure 21. I/O Port 0 Circuit Diagram

PORT 1 CIRCUIT DIAGRAM

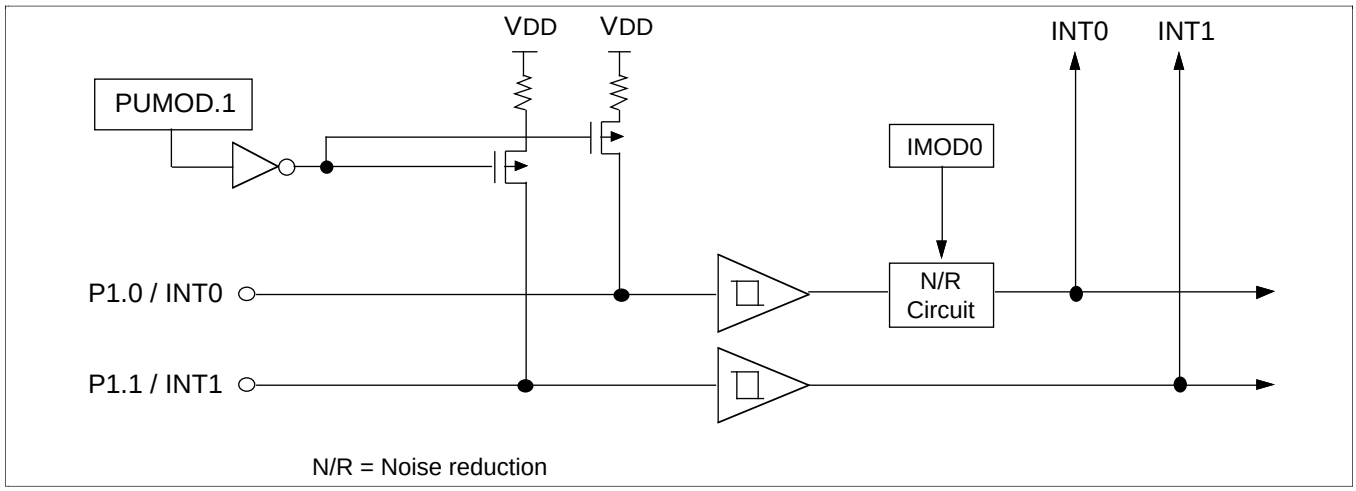


Figure 22. Input Port 1 Circuit Diagram

PORT 2 CIRCUIT DIAGRAM

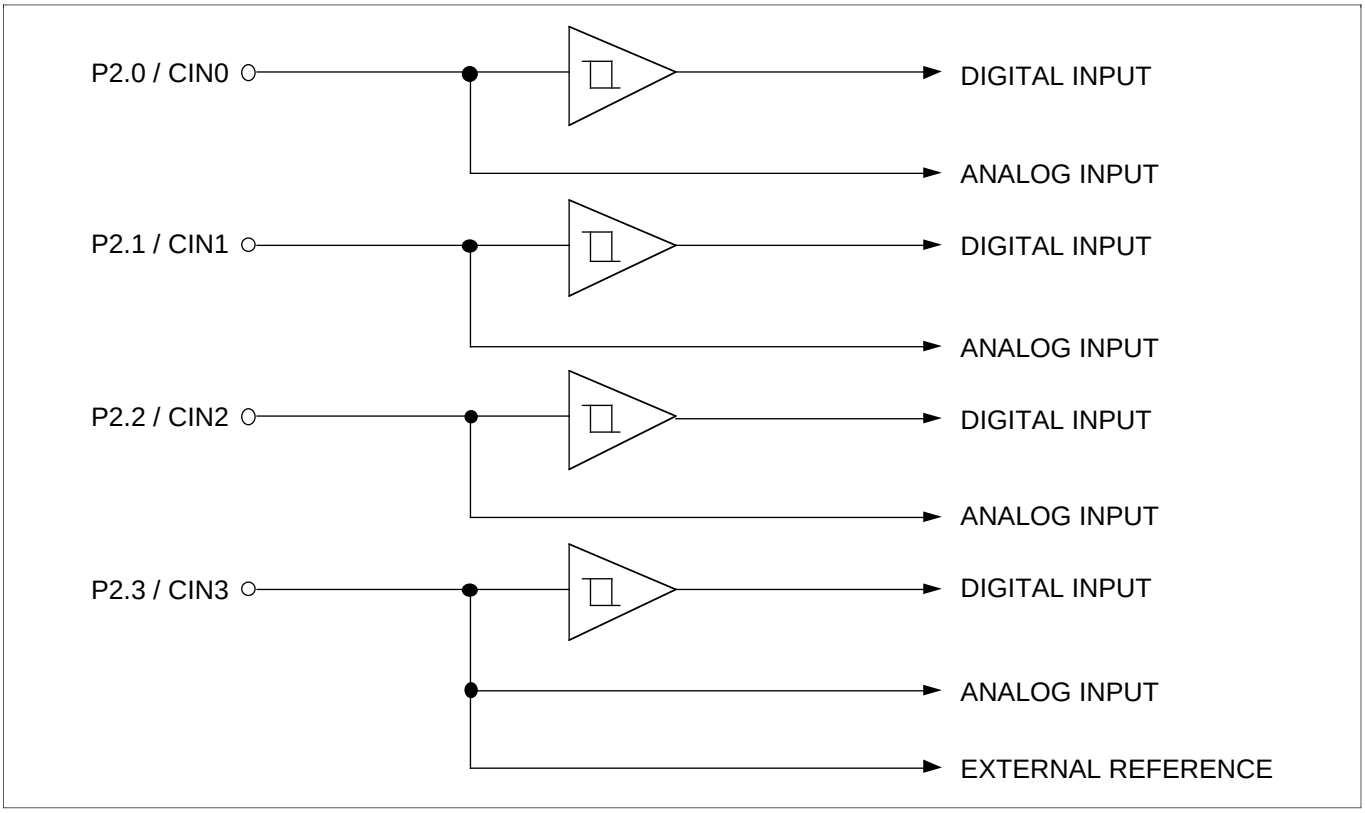
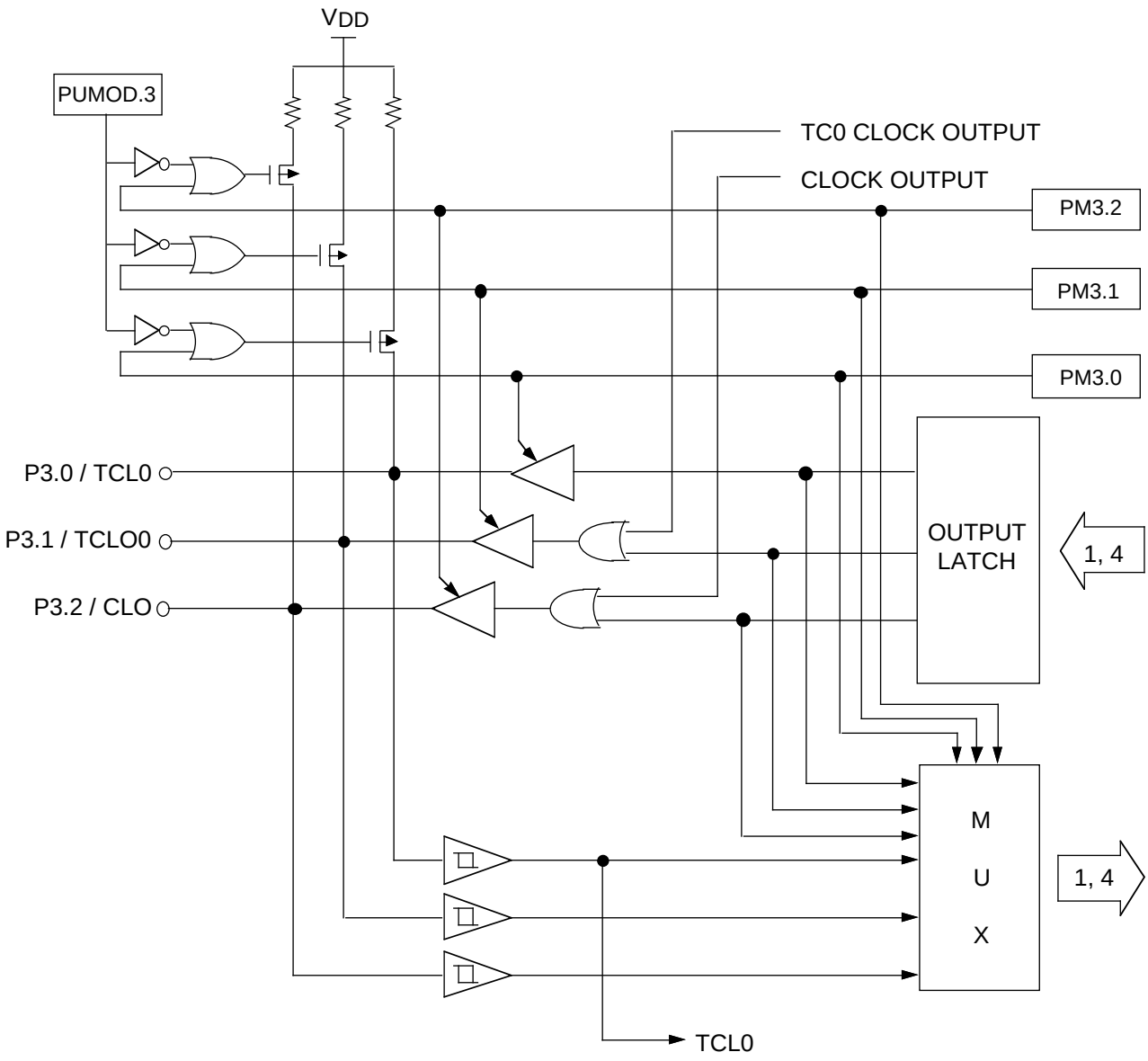


Figure 23. Port 2 Circuit Diagram

PORT 3 CIRCUIT DIAGRAM



NOTE: When a port pin acts as an output, its pull-up resistor is automatically disabled, even though the port's pull-up resistor is enabled by bit settings to the pull-up resistor mode register (PUMOD).

Figure 24. Port 3 Circuit Diagram

PORTS 4 AND 5 CIRCUIT DIAGRAM

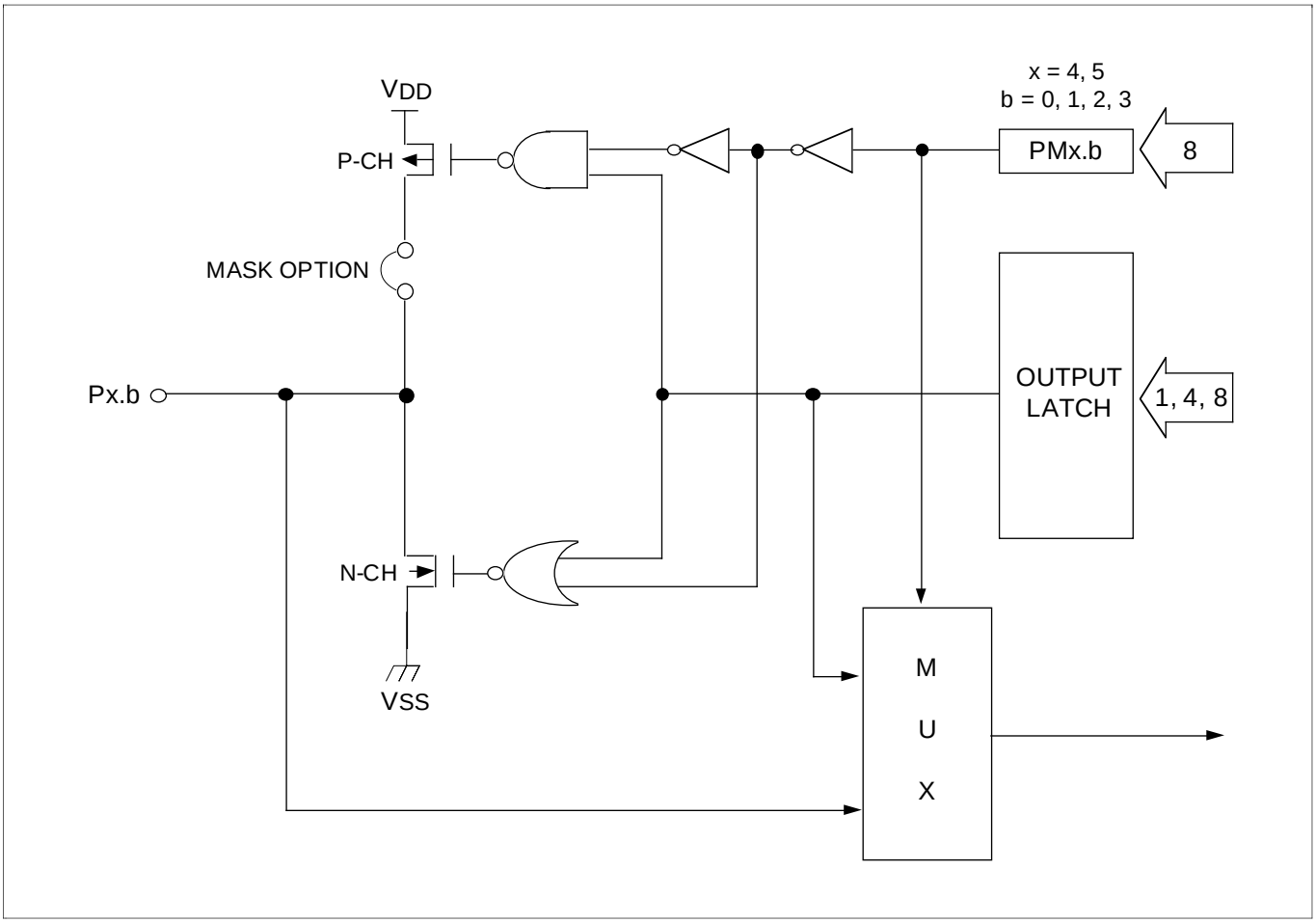
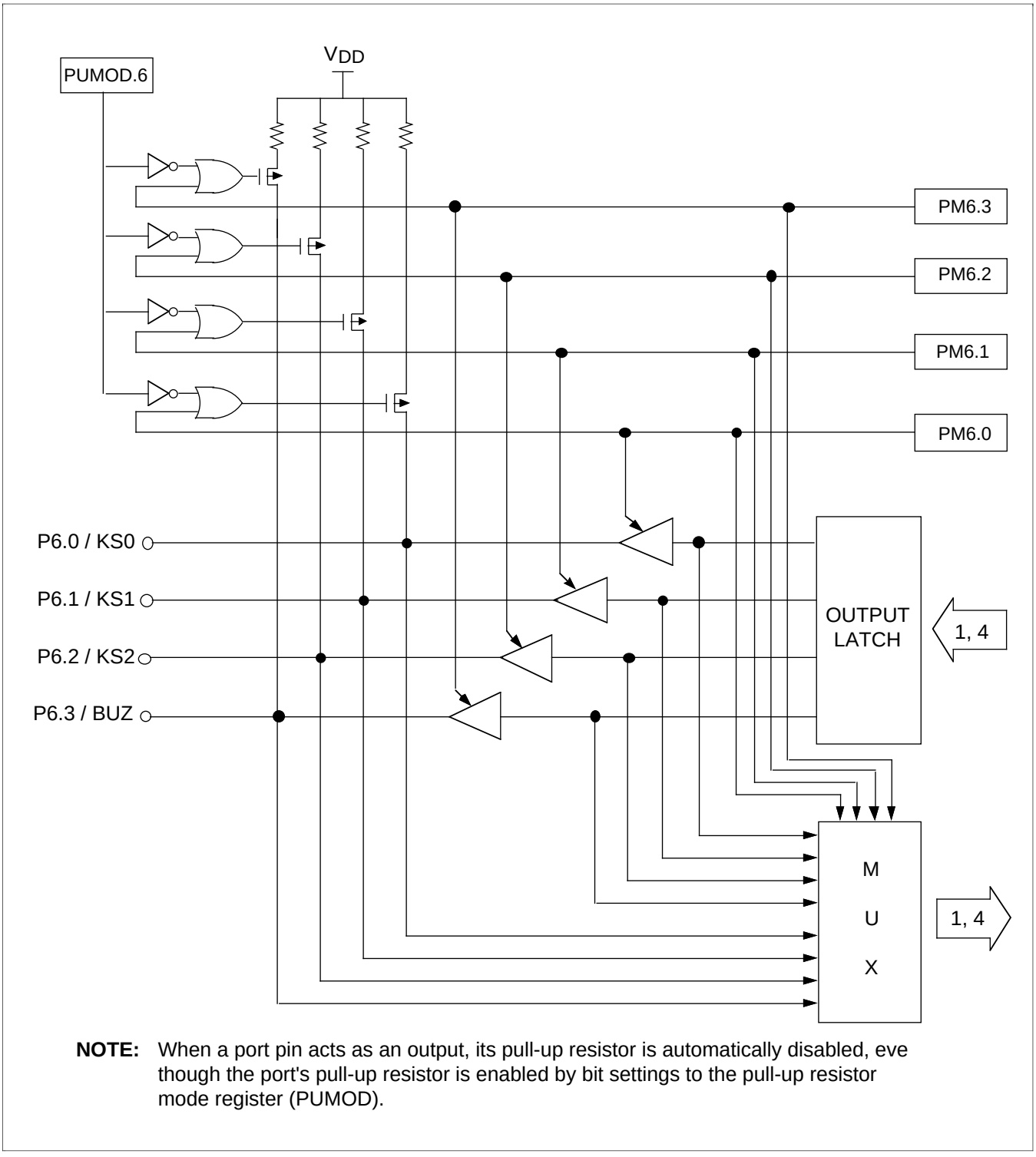


Figure 25. Circuit Diagram for Ports 4 and 5

PORT 6 CIRCUIT DIAGRAM



NOTE: When a port pin acts as an output, its pull-up resistor is automatically disabled, eve though the port's pull-up resistor is enabled by bit settings to the pull-up resistor mode register (PUMOD).

Figure 26. Port 6 Circuit Diagram

BASIC TIMER (BT)

The basic timer generates interrupt requests atprecise intervals. You can use the basic timer as a "watchdog" timer for monitoring system events or use BT output to stabilize clock oscillation when Stop mode is released by an interrupt and following RESET.

Interval Timer Function

The measurement of elapsed time intervals is the basic timer's primary function. The standard interval is 256 BT clock pulses. To restart the basic timer, set bit 3 of the mode register BMOD to "1". The 8-bit counter register, BCNT, is incremented each time a clock signal is detected that corresponds to the frequency selected by BMOD. BCNT continues incrementing as it counts BT clocks until an overflow occurs. An overflow causes the BT interrupt request flag (IRQB) to be set to "1" to signal that the designated time interval has elapsed. An interrupt request is then generated, BCNT is cleared to "0", and counting continues from 00H.

Oscillation Stabilization Interval Control

Setting bits 2–0 of the BMOD register determines the time interval (also referred to as 'wait time') required to stabilize clock signal oscillation when power-down mode is released by an interrupt. When a RESET signal is generated, the standard stabilization interval for system clock oscillation following a RESET is 31.3ms at 4.19 MHz.

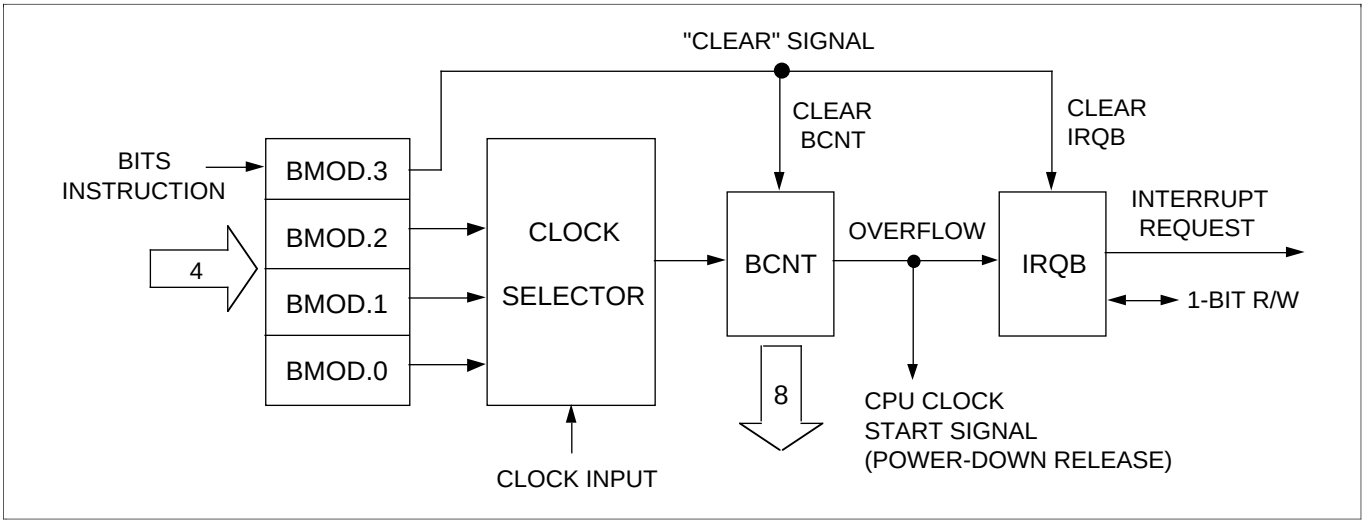


Figure 27. Basic Timer Circuit Diagram

BASIC TIMER MODE REGISTER (BMOD)

The basic timer mode register, BMOD, is used to select input frequency and oscillation stabilization time. The most significant bit of the BMOD register, BMOD.3, is used to restart the basic timer. When BMOD.3 is set to "1", the contents of the BT counter register (BCNT) and the BT interrupt request flag (IRQB) are both cleared to "0", and timer operation is restarted.

Table 19. Basic Timer Mode Register (BMOD) Organization (4-Bit W)

BMOD.3	Basic Timer Enable/Disable Control Bit
1	Start basic timer; clear IRQB, BCNT, and BMOD.3 to "0".

BMOD.2	BMOD.1	BMOD.0	Basic Timer Input Clock	Oscillation Stabilization
0	0	0	$fx/2^{12}$ (1.02 kHz)	$2^{20}/fx$ (250 ms)
0	1	1	$fx/2^{9}$ (8.18 kHz)	$2^{17}/fx$ (31.3 ms)
1	0	1	$fx/2^{7}$ (32.7 kHz)	$2^{15}/fx$ (7.82 ms)
1	1	1	$fx/2^{5}$ (131 kHz)	$2^{13}/fx$ (1.95 ms)

NOTES:
1. Clock frequencies and stabilization intervals assume a system oscillator clock frequency (fx) of 4.19 MHz.
2. fx = system clock frequency.
3. Oscillation stabilization time is the time required to stabilize clock signal oscillation after Stop mode is released.
4. The standard stabilization time for system clock oscillation following a RESET is 31.3 ms at 4.19 MHz.
5. BMOD.3 is bit addressable.

BASIC TIMER COUNTER (BCNT)

BCNT is an 8-bit counter register for the basic timer. When BCNT has incremented to hexadecimal 'FFH', it is cleared to '00H' and an overflow is generated. The overflow causes the interrupt request flag, IRQB, to be set to "1". When the interrupt request is generated, BCNT immediately resumes counting incoming clock signals.

NOTE

Always execute a BCNT read operation twice to eliminate the possibility of reading unstable data while the counter is incrementing. If, after two consecutive reads, the BCNT values match, you can select the latter value as valid data. Until the results of the consecutive reads match, however, the read operation must be repeated until the validation condition is met.

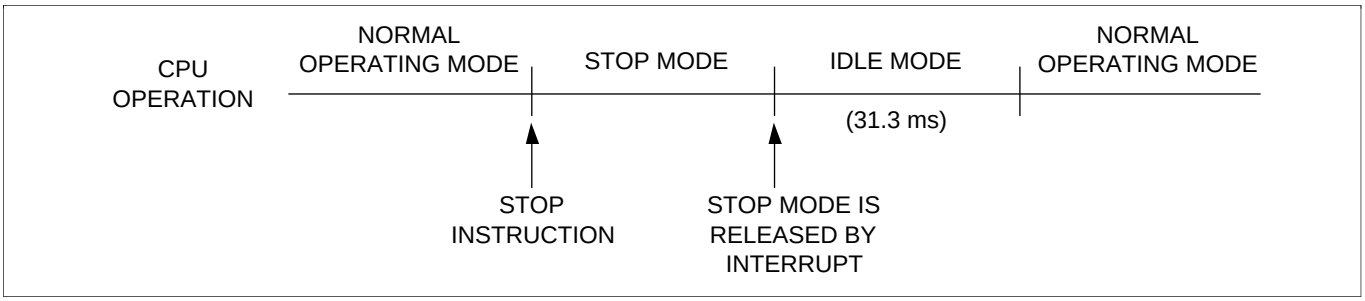
☞ PROGRAMMING TIP — Using the Basic Timer

1. To read the basic timer count register (BCNT):

```
        BITS    EMB
        SMB     15
BCNTR   LD      EA,BCNT
        LD      YZ,EA
        LD      EA,BCNT
        CPSE    EA,YZ
        JR      BCNTR
```

2. When Stop mode is released by an interrupt, set the oscillation stabilization interval to 31.3 ms:

```
        BITS    EMB
        SMB     15
        LD      A,#0BH
        LD      BMOD,A          ;   Wait time is 31.3 ms
        STOP                    ;   Set stop power-down mode
        NOP
        NOP
        NOP
```



3. To set the basic timer interrupt interval time to 1.95 ms (at 4.19 MHz):

```
        BITS    EMB
        SMB     15
        LD      A,#0FH
        LD      BMOD,A
        EI
        BITS    IEB             ;   Basic timer interrupt enable flag is set to "1"
```

4. Clear BCNT and the IRQB flag and restart the basic timer:

```
        BITS    EMB
        SMB     15
        BITS    BMOD.3
```

8-BIT TIMER/COUNTER 0 (TC0)

Timer/counter 0 (TC0) is used to count system 'events' by identifying the transition (high-to-low or low-to-high) of incoming square wave signals.

To indicate that an event has occurred, or that a specified time interval has elapsed, TC0 generates an interrupt request. By counting signal transitions and comparing the current counter value with the reference register value, TC0 can be used to measure specific time intervals.

Timer/counter 0 can supply a clock signal to the clock selector circuit of the serial I/O interface for data shifter and clock counter operations. (These internal SIO operations are controlled in turn by the SIO mode register, SMOD). This clock generation function lets you adjust data transmission rates across the serial interface.

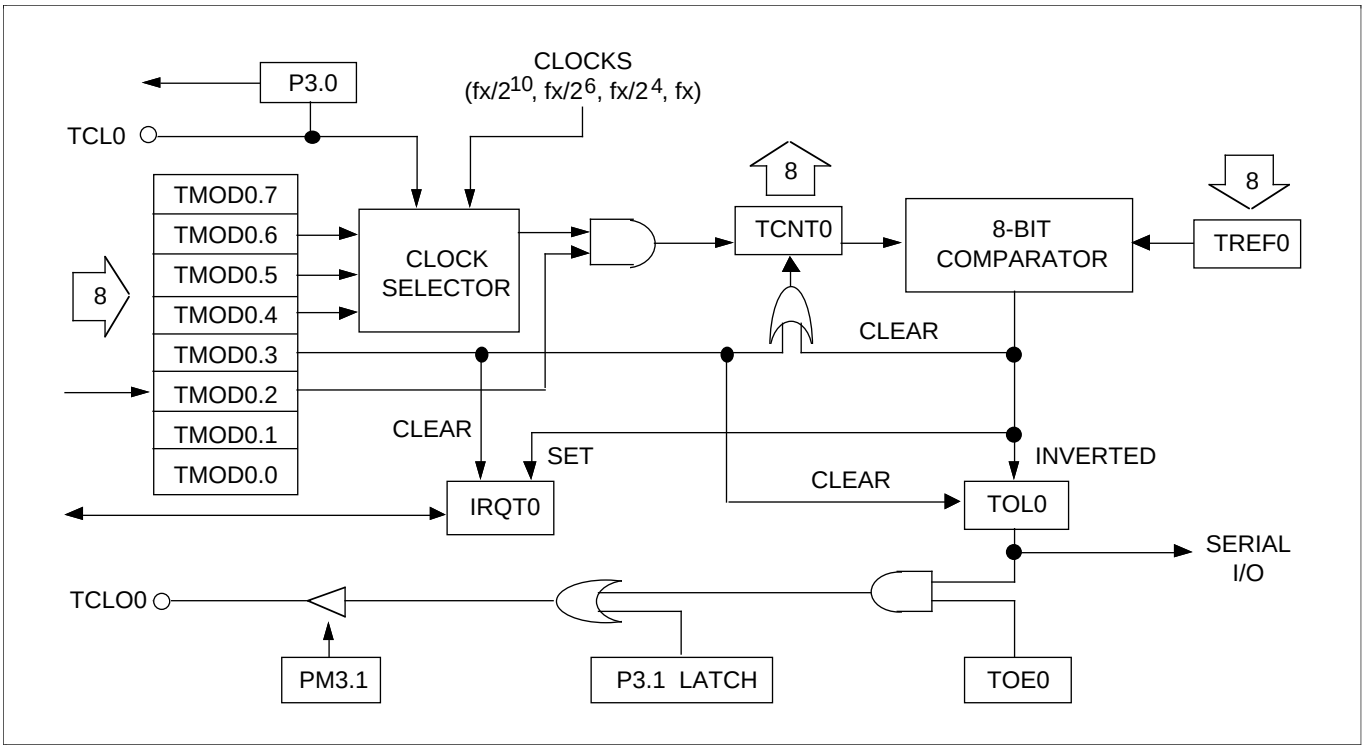


Figure 28. TC0 Circuit Diagram

PROGRAMMABLE TIMER/COUNTER FUNCTION

Timer/counter 0 can generate interrupt requests at various intervals, based on the selected system clock frequency. The reference register, TREF0, stores the value for the number of clock pulses to be generated between interrupt requests. The counter register, TCNT0, counts the incoming clock pulses, which are compared to the TREF0 value as TCNT0 is incremented. When TREF0 = TCNT0, the TC0 interrupt request flag (IRQT0) is set to "1", the status of TOL0 is inverted, and the interrupt is generated.

The content of TCNT0 is then cleared to 00H, and TC0 continues counting.

EVENT COUNTER FUNCTION

Timer/counter 0 can be used to monitor or detect system 'events' by using the external clock input at the TCL0 pin (I/O port 3.0) as the counter source. To activate the TC0 event counter function, P3.0/TCL0 must be set to input mode. With the exception of the different TMOD0.4–TMOD0.6 settings, the operation sequence for TC's event counter function is identical to its programmable timer/counter function.

TC0 CLOCK FREQUENCY OUTPUT

Using timer/counter, you can output a modifiable clock frequency to the TC0 clock output pin, TCLO0. To enable the output to the TCLO0/P3.1, the pin must be set to output mode when the timer output enable flag (TOE0) has been enabled.

☞ PROGRAMMING TIP — TC0 Signal Output to the TCLO0 Pin

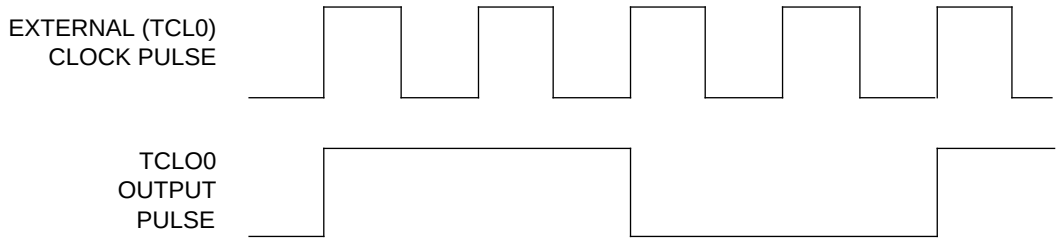
Output a 30 ms pulse width signal to the TCLO0 pin:

```
BITS    EMB
SMB     15
LD      EA,#79H
LD      TREF0,EA
LD      EA,#4CH
LD      TMOD0,EA
LD      EA,#20H
LD      PMG1,EA         ;   P3.1 ← Output mode
BITR    P3.1            ;   P3.1 clear
BITS    TOE0
```

By selecting an external clock source, you can divide the incoming clock signal by the TREF0 value and then output this modified clock frequency to the TCLO0 pin.

☞ PROGRAMMING TIP — External TCL0 Clock Output to the TCLO0 Pin

Output external TCL0 clock pulse to the TCLO0 pin (divide by four):




```
BITS    EMB
SMB     15
LD      EA,#01H
LD      TREF0,EA
LD      EA,#0CH
LD      TMOD0,EA
LD      EA,#20H
LD      PMG1,EA         ;   P3.1 ← Output mode
BITR    P3.1            ;   P3.1 clear
BITS    TOE0
```

TC0 MODE REGISTER (TMOD0)

TMOD0 is the 8-bit mode control register for timer/counter 0. When TMOD0.3 is set to "1", the contents of TCNT0, IRQT0, and TOL0 are cleared, counting starts from 00H, and TMOD0.3 is automatically reset to "0" for normal TC0 operation. When TC0 operation stops (TMOD0.2 = "0"), the contents of the TC0 counter register, TCNT0, are retained until TC0 is re-enabled.

Table 20. TC0 Mode Register (TMOD0) Organization (8-Bit W)

Bit Name	Setting	Resulting TC0 Function	Address
TMOD0.7	0	MSB value always logic zero	F91H
TMOD0.6 TMOD0.5 TMOD0.4	0,1	Specify input clock edge and internal frequency	
TMOD0.3	1	Clear TCNT0, IRQT0, and TOL0. Then immediately resume counting. (This bit is automatically cleared to "0" when counting resumes.)	F90H
TMOD0.2	0	Disable timer/counter; retain TCNT0 contents	
	1	Enable timer/counter	
TMOD0.1	0	Value always "0"	
TMOD0.0	0	LSB value always "0"	

Table 21. TMOD0.6, TMO0.5, and TMOD0.4 Bit Settings

TMOD0.6	TMOD0.5	TMOD0.4	Resulting Counter Source and Clock Frequency
0	0	0	External clock input (TCL0) on rising edges
0	0	1	External clock input (TCL0) on falling edges
1	0	0	$fx/2^{10}$ = 4.09 kHz
1	0	1	$fx/2^{6}$ = 65.5 kHz
1	1	0	$fx/2^{4}$ = 262 kHz
1	1	1	fx = 4.19 MHz

NOTE: 'fx' = system clock

☞ PROGRAMMING TIP — Restarting TC0 Counting Operation

1. Set TC0 timer interval to 4.09 kHz:

```
BITS    EMB
SMB     15
LD      EA,#4CH
LD      TMOD0,EA
EI
BITS    IET0
```

2. Clear TCNT0, IRQT0, and TOL0. Then, restart the TC0 counting operation:

```
BITS    EMB
SMB     15
BITS    TMOD0.3
```

TC0 REFERENCE REGISTER (TREF0)

TREF0 is used to store a reference value to be compared to the incrementing TCNT0 register in order to identify an elapsed time interval.

Use the following formula to calculate the correct value to load to the TREF0 reference register:

TC0 timer interval =

$$(\text{TREF0 value} + 1) \times \frac{1}{\text{TMOD0frequencysetting}}$$

(assuming a TREF0 value $\neq$ 0)

TC0 OUTPUT ENABLE FLAG (TOE0)

The 1-bit timer/counter 0 output enable flag TOE0 controls output from TC0 to the TCLO0 pin.

F92H 1-Bit R/W

0	**TOE0**	0	0

When you set the TOE0 flag to "1", the contents of TOL0 can be output to the TCLO0 pin.

☞ PROGRAMMING TIP — Setting a TC0 Timer Interval

To set a 30 ms timer interval for TC0, given fx = 4.19MHz, follow these steps.

1. Select the timer/counter mode register with a maximum setup time of 62.5 ms (assume that the TC0 counter clock = $fx/2^{10}$, and TREF0 is FFH):

2. Calculate the TREF0 value:

$$30\ \text{ms} = \frac{\text{TREF0value}+1}{4.09\text{kHz}}$$

$$\text{TREF0} + 1 = \frac{30\text{ms}}{244\mu\text{s}} = 122.9 = 7\text{AH}$$

$$\text{TREF0 value} = 7\text{AH} - 1 = 79\text{H}$$

3. Load the value 79H to the TREF0 register:

```
BITS    EMB
SMB     15
LD      EA,#79H
LD      TREF0,EA
LD      EA,#4CH
LD      TMOD0,EA
```

WATCH TIMER

Watch timer functions include real-time and watch-time measurement and interval timing for the system clock. It is also used as a clock source for generating buzzer output.

To start the watch timer, set bit 2 of the watch timer mode register, WMOD.2, to "1". The watch timer starts, the interrupt request flag IRQW is automatically set to "1", and interrupt requests commence in 0.5-second intervals. Because the watch timer functions as a quasi-interrupt instead of a vectored interrupt, the IRQW flag should be cleared to "0" by program software as soon as a requested interrupt service routine has been executed.

The watch timer can generate a steady 2 kHz, 4 kHz, 8 kHz, or 16 kHz signal to the BUZ pin. To generate a BUZ signal, clear the output latch for I/O port 6.3 to "0" and set the port 6.3 output mode flag (PM6.3) to output mode.

By setting WMOD.1 to "1", the watch timer functions in high-speed mode, generating an interrupt every 3.91 ms. High-speed mode is useful for timing events during program debugging sequences.

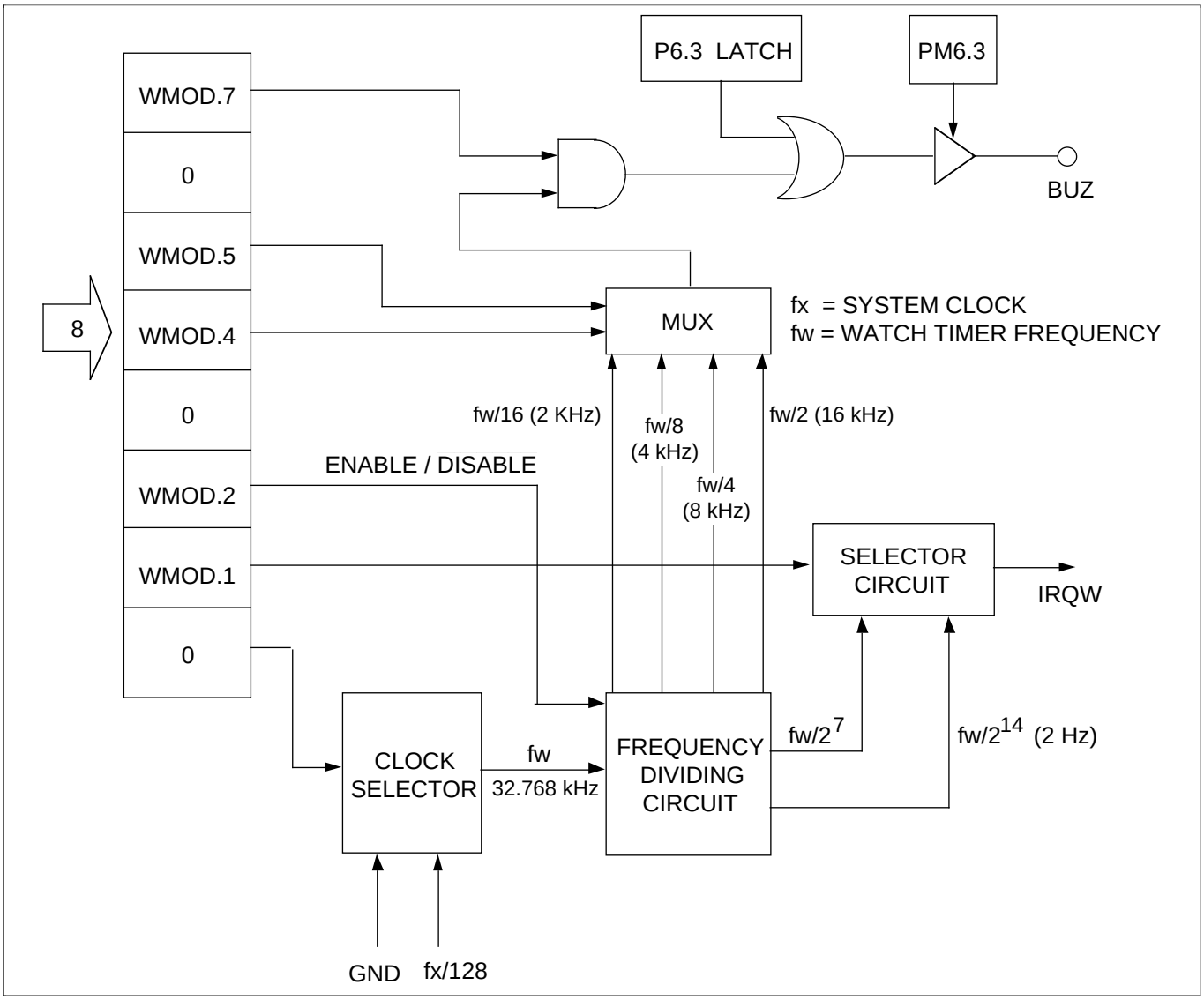


Figure 29. Watch Timer Circuit Diagram

WATCH TIMER MODE REGISTER (WMOD)

The watch timer mode register WMOD is used to select specific watch timer operations.

Table 22. Watch Timer Mode Register (WMOD) Organization (8-Bit W)

Bit Name	Values		Function	Address
WMOD.7	0		Disable buzzer (BUZ) signal output	F89H
	1		Enable buzzer (BUZ) signal output	
WMOD.6	"0"		Always "0"	
WMOD.5 – .4	0	0	2 kHz buzzer (BUZ) signal output	
	0	1	4 kHz buzzer (BUZ) signal output	
	1	0	8 kHz buzzer (BUZ) signal output	
	1	1	16 kHz buzzer (BUZ) signal output	
WMOD.3	"0"		Always "0"	F88H
WMOD.2	0		Disable watch timer; clear frequency dividing circuits	
	1		Enable watch timer	
WMOD.1	0		Normal mode; sets IRQW to 0.5 s	
	1		High-speed mode; sets IRQW to 3.91 ms	
WMOD.0	0		Always "0"	

NOTE: System clock frequency (fx) is assumed to be 4.19 MHz.

☞ PROGRAMMING TIP — Using the Watch Timer

1. Select a 0.5 second interrupt, and 2 kHz buzzer enable:

```
        BITS    EMB
        SMB     15
        LD      EA,#80H
        LD      PMG3,EA         ;   P6.3 ← Output mode
        BITR    P6.3            ;   Clear P6.3 output latch
        LD      EA,#84H
        LD      WMOD,EA
        BITS    IEW
```

2. Sample real-time clock processing method:

```
CLOCK   BTSTZ   IRQW            ;   0.5 second check
        RET                     ;   No, return
        •                       ;   Yes, 0.5 second interrupt generation
        •
        •                       ;   Increment HOUR, MINUTE, SECOND
```

COMPARATOR

Port 2 can be used as a analog input port for the 4-channel comparator block. The reference voltage for the comparator can be supplied either internally or externally at P2.3.

When internal reference voltage is used, four channels (P2.0–P2.3) are used for analog inputs and the internal reference voltage is varies at 16 levels. If an external reference voltage is input at P2.3, the other three pins (P2.0–P2.2) in port 2 are used for analog input. Unused port 2 pins must be connected to V_{DD}.

When a conversion is completed, the result is saved in the comparison result register CMPREG. The initial values of the CMPREG are undefined and the comparator operation is disabled by a RESET.

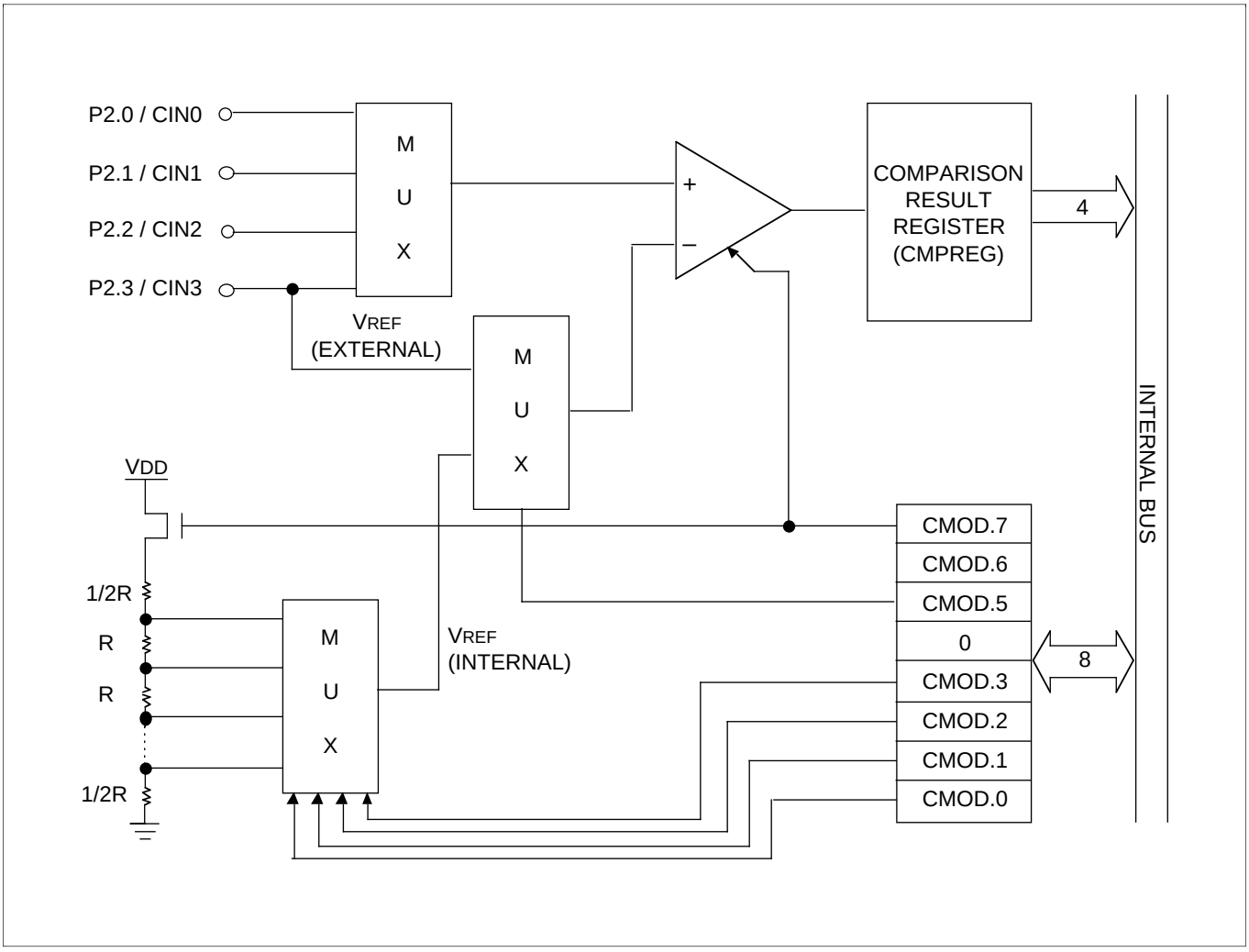


Figure 30 Comparator Circuit Diagram

COMPARATOR MODE REGISTER (CMOD)

The comparator mode register (CMOD) is used to set the operation mode of the comparator. Based on the CMOD.5 bit setting, an internal or an external reference voltage is input for the comparator, as follows:

When CMOD.5 is "0":

— A reference voltage is selected by the CMOD.0 to CMOD.3 bit settings.

— P2.0 to P2.3 are used as analog input pins.

— The internal digital-to-analog converter generates 16 reference voltages.

— The comparator can detect a 150 mV difference between the reference voltage and analog input voltages.

— Comparator results are written into 4-bit comparison result register (CMPREG).

When CMOD.5 is set to "1":

— External reference voltage is supplied from P2.3/CIN3.

— P2.0 to P2.2 are used as the analog input pins.

— The comparator can detect a 150 mV difference between the reference voltage and analog input voltages.

— Bits 0–2 in the CMPREG register contain the results (the content of bit 3 is not used).

Bit 6 in the CMOD register controls conversion time while bit 7 enables or disables comparator operation to reduce power consumption.

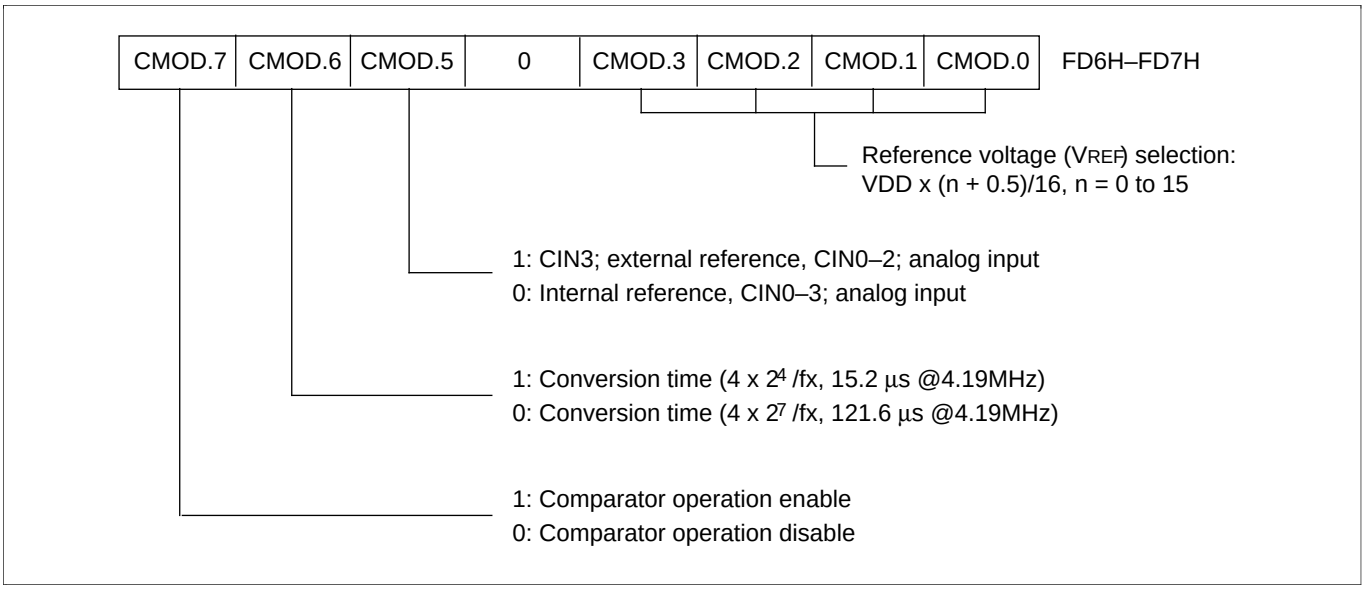


Figure 31. Comparator Mode Register Organization

PORT 2 MODE REGISTER (P2MOD)

P2MOD register settings determine if port 2 is used for analog or digital input.

FE2H 4-Bit W

P2MOD.3	P2MOD.2	P2MOD.1	P2MOD.0

When a P2MOD bit is set to "1", the corresponding pin is configured as a digital input pin. When it is "0", the corresponding pin is configured as an analog input: P2MOD.0 for P2.0, P2MOD.1 for P2.1, P2MOD.2 for P2.2, and P2MOD.3 for P2.3.

COMPARATOR OPERATION

The comparator compares analog voltage input at CIN0–CIN3 with an external or internal reference voltage (V_{REF}) that is selected by CMOD register. The result is written to the comparison result register CMPREG at address FD4H.

The comparison result is calculated as follows:

If "1" Analog input voltage ≥ V_{REF} + 150 mV

If "0" Analog input voltage ≤ V_{REF} – 150 mV

To obtain a comparison result, the data must be read out from the CMPREG register after V_{REF} is updated by changing the CMOD value after a conversion time has elapsed.

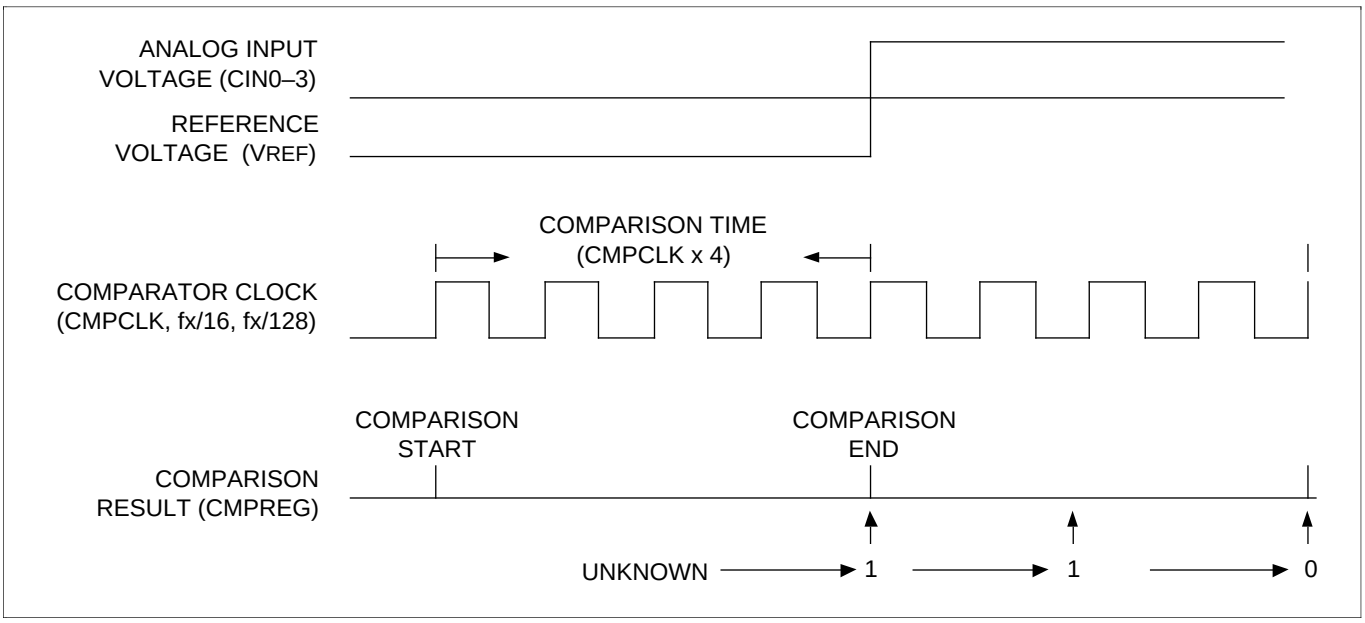


Figure 32. Conversion Characteristics

☞ PROGRAMMING TIP — Programming the Comparator

The following program example converts the analog voltage input at CIN0–CIN2 pins into 4-bit digital code.

```
        BITR    EMB
        LD      A,#0H
        LD      P2MOD,A     ;   Analog input selection (CIN0–CIN3)
        LD      EA,#8XH     ;   x = 0–F, comparator enable
                            ;   Internal reference, conversion time (121.6 μs)
        LD      CMOD,EA
WAIT LD A,#0H
        INCS    A
        JR      WAIT
        LD      A,CMPREG    ;   Read the result
        LD      P4,A        ;   Output the result from port 4
```

SERIAL I/O INTERFACE

Using the serial I/O interface, you can exchange 8-bit data with an external device. The serial interface can run off an internal or an external clock source, or the TOL0 signal that is generated by the 8-bit timer/counter 0, TC0. If you use the TOL0 clock signal, you can modify its frequency to adjust the serial data transmission rate.

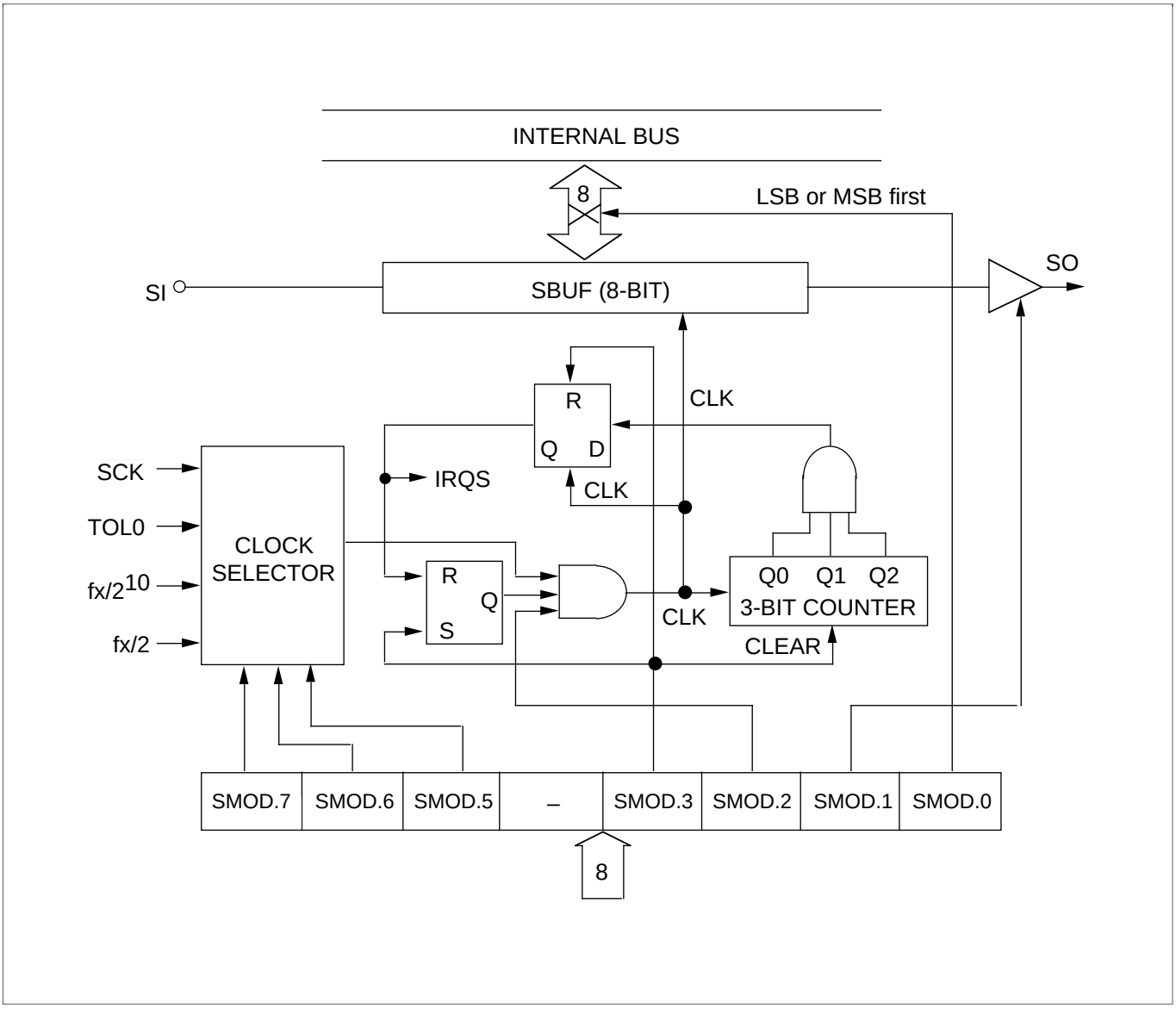


Figure 33. Serial I/O Interface Circuit Diagram

SERIAL I/O MODE REGISTER (SMOD)

The serial I/O mode register (SMOD) specifies the operation mode of the serial interface. SMOD register settings enable you to select either MSB-first or LSB-first serial transmission, and to operate in transmit-and-receive mode or receive-only mode. When SMOD.3 is set to "1", the contents of the serial interface interrupt request flag, IRQS, and the 3-bit serial clock counter are cleared, and SIO operations are initiated. When the SIO transmission starts, SMOD.3 is cleared to "0".

SERIAL I/O BUFFER REGISTER (SBUF)

When the serial interface operates in transmit-and-receive mode (SMOD.1 = "1"), transmit data in the SIO buffer register are output to the SO pin at the rate of one bit for each falling edge of the SIO clock. Receive data is simultaneously input from the SI pin to SBUF at the rate of one bit for each rising edge of the SIO clock.

When receive-only mode is used, incoming data is input to the SIO buffer at the rate of one bit for each rising edge of the SIO clock. SBUF can be read or written using 8-bit RAM control instructions.

Table 23. SIO Mode Register (SMOD) Organization (8-Bit W)

SMOD.0	0	Most significant bit (MSB) is transmitted first
	1	Least significant bit (LSB) is transmitted first
SMOD.1	0	Receive-only mode; output buffer is off
	1	Transmit-and-receive mode
SMOD.2	0	Disable the data shifter and clock counter; retain contents of IRQS flag when serial transmission is halted
	1	Enable the data shifter and clock counter; set IRQS flag to "1" when serial transmission is halted
SMOD.3	1	Clear IRQS flag and 3-bit clock counter to "0"; initiate transmission and then reset this bit to "0"; this bit is also bit-addressable.
SMOD.4	0	Bit not used; value is always "0"

SMOD.7	SMOD.6	SMOD.5	Clock Selection	R/W Status of SBUF
0	0	0	External clock at SCK pin	SBUF is enabled when SIO operation is halted or when SCK goes high.
0	0	1	Use TOL0 clock from TC0	
0	1	x	CPU clock: fx/4, fx/8, fx/64	Enable SBUF read/write
1	0	0	4.09 kHz clock: $fx/2^{10}$	SBUF is enabled when SIO operation is halted or when SCK goes high.
1	1	1	262 kHz clock: $fx/2^4$	

NOTES:
1. 'fx' = system clock; 'x' means 'don't care.'
2. kHz frequency ratings assume a system clock (fx) running at 4.19 MHz.
3. The SIO clock selector circuit cannot select a $fx/2^4$ clock if the CPU clock is fx/64.

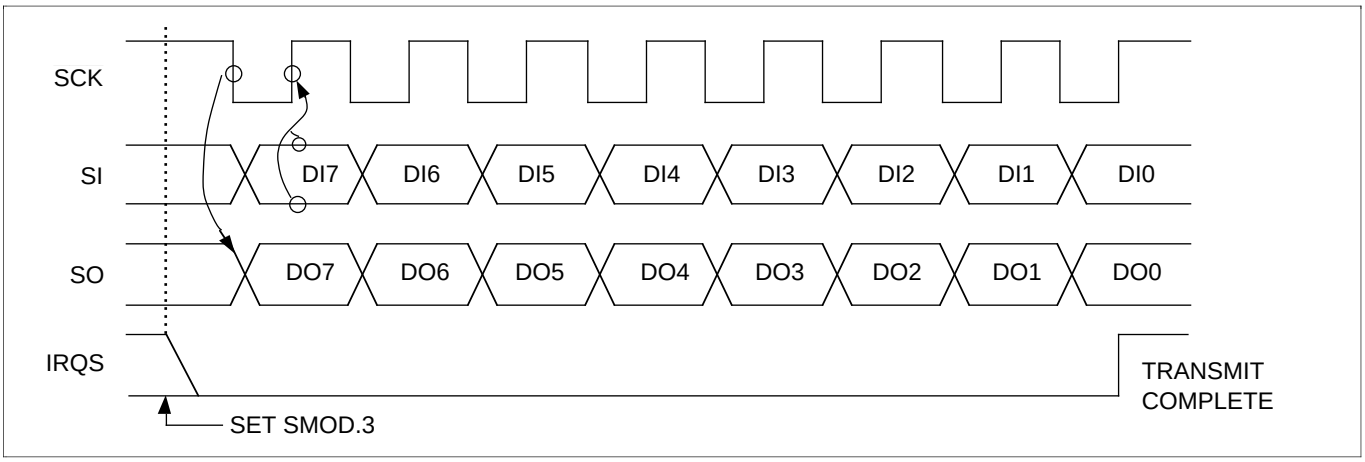


Figure 34. SIO Timing in Transmit/Receive Mode

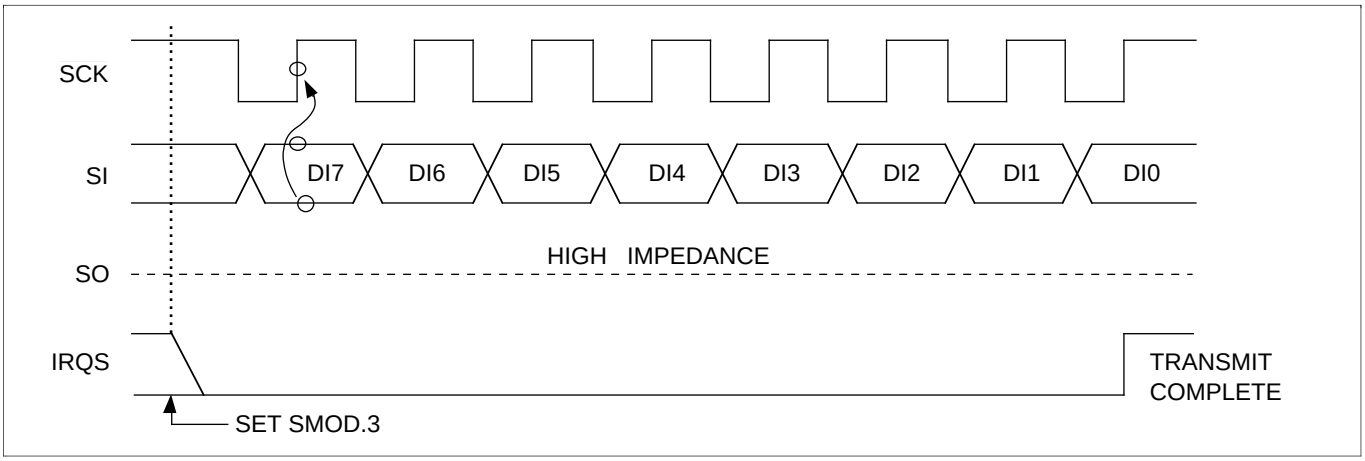


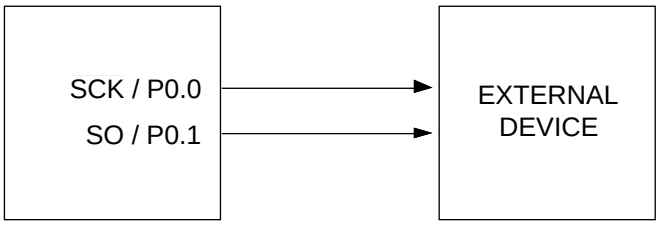
Figure 35. SIO Timing in Receive-Only Mode

☞ **PROGRAMMING TIP — Setting Transmit/Receive Modes for Serial I/O**

1. Transmit the data value 48H through the serial I/O interface using an internal clock frequency of fx/2^4 and in MSB-first mode:

```
        BITS    EMB
        SMB     15
        LD      EA,#03H
        LD      PMG1,EA         ;  P0.0 / SCK and P0.1 / SO ← Output
        LD      EA,#48H         ;
        LD      SBUF,EA         ;
        LD      EA,#0EEH
        LD      SMOD,EA         ;  SIO data transfer
```

☞ **PROGRAMMING TIP — Setting Transmit/Receive Modes for Serial I/O (Continued)**



KS57C0002

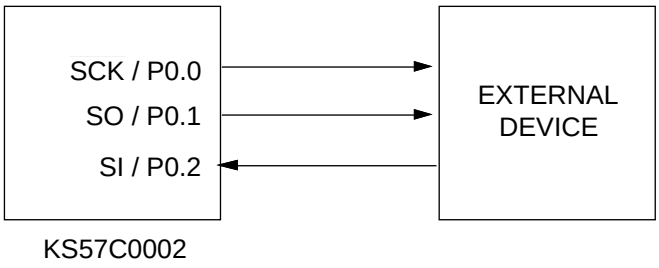
2. Use CPU clock to transfer and receive serial data at high speed:

```
        BITR    EMB
        LD      EA,#03H
        LD      PMG1,EA         ;  P0.0 / SCK and P0.1 / SO ← Output, P0.2 / SI ← Input
        LD      EA,TDATA        ;  TDATA address = Bank0(20H–7FH)
        LD      SBUF,EA
        LD      EA,#4FH
        LD      SMOD,EA         ;  SIO start
        BITR    IES             ;  SIO Interrupt Enable
STEST   BTSTZ   IRQS
        JR      STEST
        LD      EA,SBUF
        LD      RDATA,EA        ;  RDATA address = Bank0 (20H–7FH)
```

☞ **PROGRAMMING TIP — Setting Transmit/Receive Modes for Serial I/O (Continued)**

3. Transmit and receive an internal clock frequency of 4.09 kHz (at 4.19 MHz) in LSB-first mode:

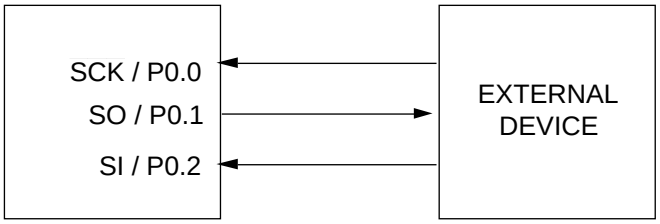
```
        BITR    EMB
        LD      EA,#03H
        LD      PMG1,EA         ; P0.0 / SCK and P0.1 / SO ← Output, P0.2 / SI ← Input
        LD      EA,TDATA        ; TDATA address = Bank0 (20H–7FH)
        LD      SBUF,EA
        LD      EA,#8FH
        LD      SMOD,EA         ; SIO start
        EI
        BITS    IES             ; SIO Interrupt Enable
        •
        •
        •
INTS    PUSH    SB              ; Store SMB, SRB
        PUSH    EA              ; Store EA
        BITR    EMB
        LD      EA,TDATA        ; EA ← Transmit data
                                ; TDATA address = Bank0 (20H–7FH)
        XCH     EA,SBUF         ; Transmit data ↔ Receive data
        LD      RDATA,EA        ; RDATA address = Bank0 (20H–7FH)
        BITS    SMOD.3          ; SIO start
        POP     EA
        POP     SB
        IRET
```



☞ **PROGRAMMING TIP — Setting Transmit/Receive Modes for Serial I/O (Continued)**

4. Transmit and receive an external clock in LSB-first mode:

```
        BITR    EMB
        LD      EA,#02H
        LD      PMG1,EA         ; P0.1 / SO ← Output, P0.0 / SCK and P0.2/SI← Input
        LD      EA,TDATA        ; TDATA address = Bank0 (20H–7FH)
        LD      SBUF,EA
        LD      EA,#0FH
        LD      SMOD,EA         ; SIO start
        EI
        BITS    IES             ; SIO Interrupt Enable
        •
        •
        •
INTS    PUSH    SB              ; Store SMB, SRB
        PUSH    EA              ; Store EA
        BITR    EMB
        LD      EA,TDATA        ; EA ← Transmit data
                                ; TDATA address = Bank0 (20H–7FH)
        XCH     EA,SBUF         ; Transmit data ↔ Receive data
        LD      RDATA,EA        ; RDATA address = Bank0 (20H–7FH)
        BITS    SMOD.3          ; SIO start
        POP     EA
        POP     SB
        IRET
```



KS57C0002

ELECTRICAL DATA

Table 24. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions		Rating	Units
Supply Voltage	V_{DD}	—		– 0.3 to + 7.0	V
Input Voltage	V_{I1}	Ports 4, 5	CMOS push-pull	– 0.3 to V_{DD} + 0.3	V
			Open-drain	– 0.3 to + 9	
	V_{I2}	All I/O ports except 4 and 5		– 0.3 to V_{DD} + 0.3	
Output Voltage	V_O	—		– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active		– 5	mA
		All I/O ports active		– 15	
Output Current Low	I_{OL}	Ports 0, 3, and 6		5	mA
		Ports 4 and 5		30	
		All ports, total		+ 100	
Operating Temperature	T_A	—		– 40 to + 85	°C
Storage Temperature	T_{stg}	—		– 65 to + 150	°C

Table 25. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	Ports 4 and 5	0.7V_{DD}	—	V_{DD}	V
	V_{IH2}	Ports 0, 1, 2, 3, 6, and RESET	0.8V_{DD}	—	V_{DD}	
	V_{IH3}	X_{in} and X_{out}	V_{DD} – 0.5	—	V_{DD}	
Input Low Voltage	V_{IL1}	Ports 4 and 5	—	—	0.3V_{DD}	V
	V_{IL2}	Ports 0, 1, 2, 3, 6, and RESET			0.2V_{DD}	
	V_{IL3}	X_{in} and X_{out}			*	
Output High Voltage	V_{OH}	V_{DD} = 4.5 V to 6.0 V I_{OH} = – 1 mA Ports 0, 3, 4, 5, 6	V_{DD} – 1.0	—	—	V
		V_{DD} = 4.5 V to 6.0 V I_{OH} = – 3.0 mA Ports 0, 3, 4, 5, 6	V_{DD} – 2.0			

* The value is 0.2V at KS57C0002 or 0.4V at KS57C0004.

Table 25. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Low Voltage	V_{OL}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 15 mA Ports 4 and 5 only	—	0.4	2	V
		V_{DD} = 4.5 V to 6.0 V I_{OL} = 1.6 mA Ports 0, 3, 6 only		—	0.4	
		V_{DD} = 4.5 V to 6.0 V I_{OL} = 4.0 mA Ports 0, 3, 6 only			2	
Input High Leakage Current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{in} and X_{out}	—	—	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{in} and X_{out}			20	
	I_{LIH3}	V_{IN} = 9 V Ports 4 and 5 are open-drain			10	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{in}, X_{out} and RESET	—	—	– 3	µA
	I_{LIL2}	V_{IN} = 0 V X_{in} and X_{out}			– 20	
Output High Leakage Current	I_{LOH1}	V_O = V_{DD} All output pins except for port 4 and port 5	—	—	3	µA
	I_{LOH2}	V_O = 9 V Ports 4 and 5 are open-drain			10	
Output Low Leakage Current	I_{LOL}	V_O = 0 V	—	—	– 3	µA
Pull-Up Resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% Port 0, 1, 3, 6	15	40	80	KΩ
		V_{IN} = 0 V; V_{DD} = 3 V ± 10% Port 0, 1, 3, 6	30		200	
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% RESET	100	230	400	KΩ
		V_{IN} = 0 V; V_{DD} = 3 V ± 10% RESET	200	490	800	

Table 25. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current (1)	I_{DD1}	V_{DD} = 5 V ± 10% (2) 4.19 MHz crystal oscillator C1 = C2 = 22 pF	—	2.5	8	mA
		V_{DD} = 3 V ± 10% (3) 4.19 MHz crystal oscillator C1 = C2 = 22 pF		0.62	1.2	
	I_{DD2}	Idle mode; V_{DD} = 5 V ± 10% 4.19 MHz crystal oscillator C1 = C2 = 22 pF	—	1.2	1.8	mA
		Idle mode; V_{DD} = 3 V ± 10% 4.19 MHz crystal oscillator C1 = C2 = 22 pF		0.58	1.0	
	I_{DD3}	Stop mode V_{DD} = 5 V ± 10%		0.5	5	µA
		Stop mode V_{DD} = 3 V ± 10%		0.3	3	

NOTES:
1. The currents in the following circuits are not included; on-chip pull-up resistors, output port drive currents and comparator.
2. For high-speed controller operation, set the PCON register to 0011B.
3. For low-speed controller operation, set the PCON register to 0000B.

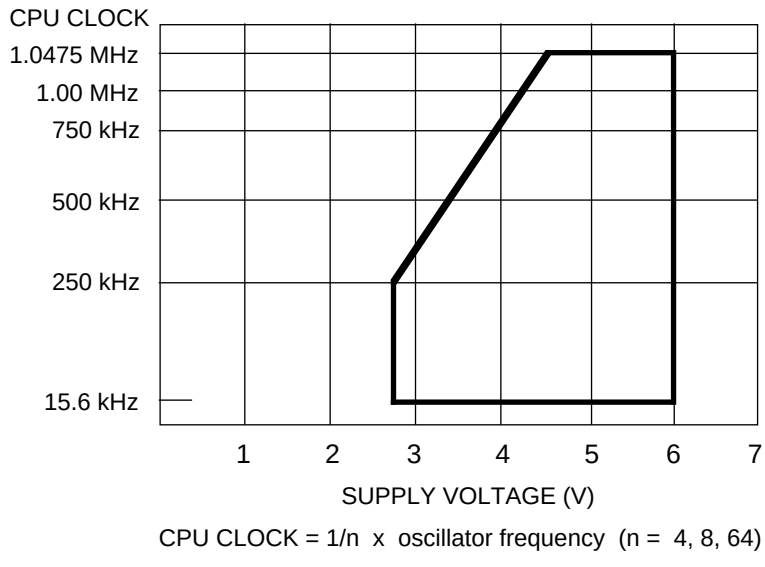
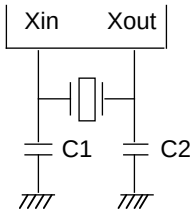
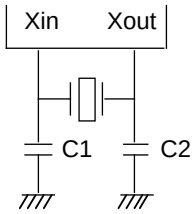
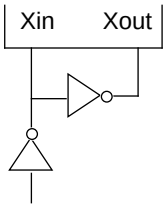
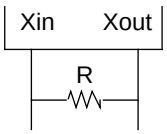


Figure 36. Standard Operating Voltage Range

Table 26. Oscillator Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	—	0.4	—	4.5	MHz
		Stabilization time (2)	After V_{DD} reaches the minimum level of its variable range	—	—	4	ms
Crystal Oscillator		Oscillation frequency (1)	—	0.4	4.19	4.5	MHz
		Stabilization time (2)	V_{DD} = 2.7 V to 4.5 V	—	—	30	ms
			V_{DD} = 4.5 V to 6.0 V	—	—	10	ms
External Clock		Xin input frequency (1)	—	0.4	—	4.5	MHz
		Xin input high and low level width (t_{XH}, t_{XL})	—	100	—	150	ns
RC Oscillator (3)		Oscillation frequency limitation	V_{DD} = 5 V	0.4	—	2	MHz

NOTES:
1. Oscillation frequency and X_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a reset or termination of Stop mode.
3. RC is only for the KS57C0002.

Table 27. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	—	—	15	pF
Output Capacitance	C_{OUT}		—	—	15	pF
I/O Capacitance	C_{IO}		—	—	15	pF

Table 28. Comparator Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.0 V to 6.0 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range	—	—	0	—	V_{DD}	V
Reference Voltage Range	V_{REF}	—	0	—	V_{DD}	V
Input Voltage Accuracy	V_{CIN}	—	—	—	±150	mV
Input Leakage Current	I_{CIN}, I_{REF}	—	– 3	—	3	µA

Table 29. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t_{CY}	V_{DD} = 4.5 V to 6.0 V	0.95	—	64	µs
		V_{DD} = 2.7 V to 4.5 V	3.8			
TCL0 Input Frequency	f_{TI}	V_{DD} = 4.5 V to 6.0 V	0	—	1	MHz
		V_{DD} = 2.7 V to 4.5 V			275	kHz
TCL0 Input High, Low Width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 V to 6.0 V	0.48	—	—	µs
		V_{DD} = 2.7 V to 4.5 V	1.8			
SCK Cycle Time	t_{KCY}	V_{DD} = 4.5 V to 6.0 V; Input	800	—	—	ns
		V_{DD} = 4.5 V to 6.0 V; Output	1600			
		V_{DD} = 2.7 V to 4.5 V; Input	3200			
		V_{DD} = 2.7 V to 4.5 V; Output	3800			

Table 29. A.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SCK High, Low Width	t_{KH}, t_{KL}	V_{DD} = 4.5 V to 6.0 V; Input	400	—	—	ns
		V_{DD} = 4.5 V to 6.0 V; Output	$t_{KCY}/2$ – 50			
		V_{DD} = 2.7 V to 4.5 V; Input	1600			
		V_{DD} = 2.7 V to 4.5 V; Output	$t_{KCY}/2$ – 150			
SI Setup Time to SCK High	t_{SIK}	Input	100	—	—	ns
		Output	150			
SI Hold Time to SCK High	t_{KSI}	Input	400	—	—	ns
		Output	400			
Output Delay for SCK to SO	t_{KSO}	V_{DD} = 4.5 V to 6.0 V; Input	—	—	300	ns
		V_{DD} = 4.5 V to 6.0 V; Output			250	
		V_{DD} = 2.7 V to 4.5 V; Input			1000	
		V_{DD} = 2.7 V to 4.5 V; Output			1000	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0	*	—	—	µs
		INT0, INT1, KS0–KS2	10			
RESET Input Low Width	t_{RSL}	Input	10	—	—	µs

* The minimum value for INT0 is based on a clock of $2t_{CY}$ or 128/fx as assigned by the IMOD0 register setting.

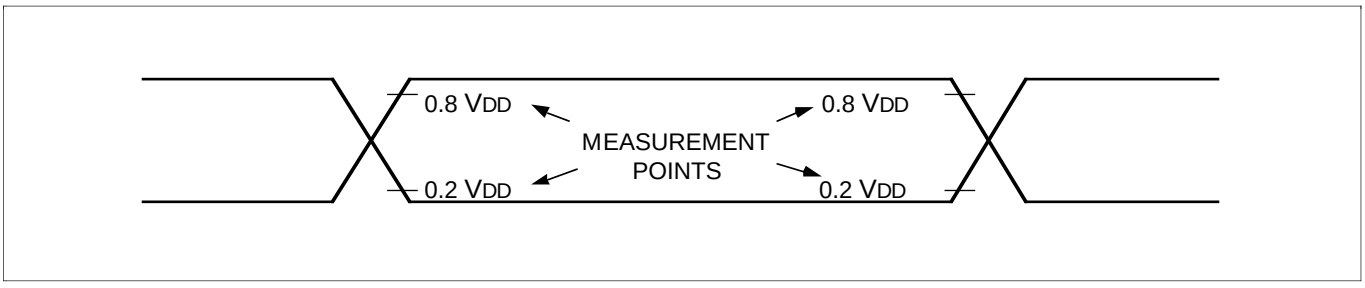


Figure 37. A.C. Timing Measurement Points (Except for X_{in})

Table 30. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Data Retention Supply Voltage	V_{DDDR}	—	2.0	—	6.0	V
Data Retention Supply Current	I_{DDDR}	—	—	0.1	10	µA
Release Signal Set Time	t_{SREL}	—	0	—	—	ms
Oscillation Stabilization Time (1)	t_{WAIT}	When released by RESET	—	2^{17}/fx	—	ms
		When released by interrupt	—	(2)	—	ms

NOTES:
1. During oscillation stabilization time, CPU operation must be stopped to avoid instability during oscillator startup.
2. The basic timer causes a delay of 2^{17}/fx after a reset.

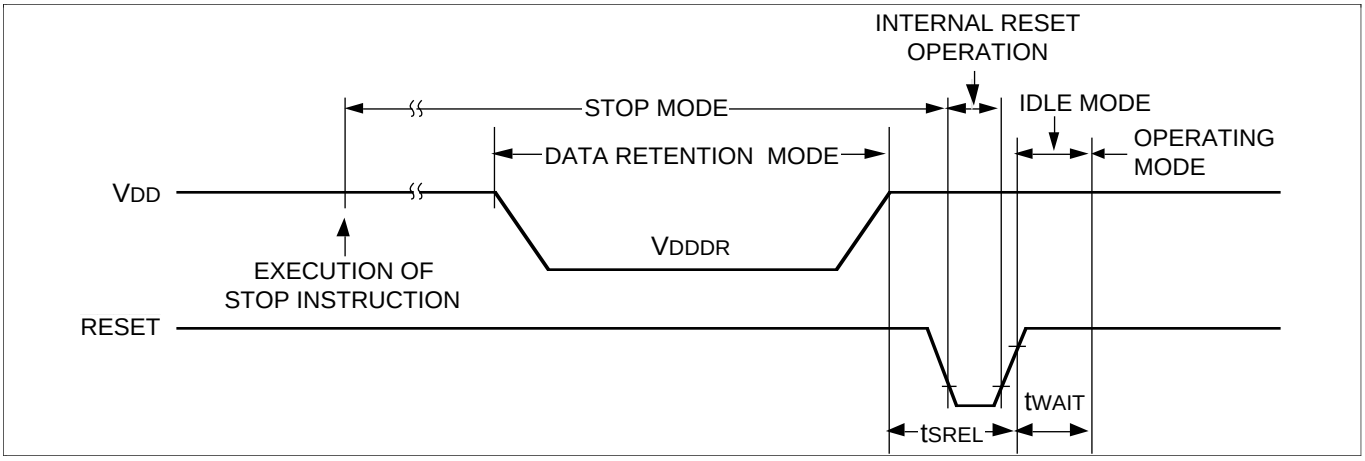


Figure 38. Stop Mode Release Timing When Initiated By RESET

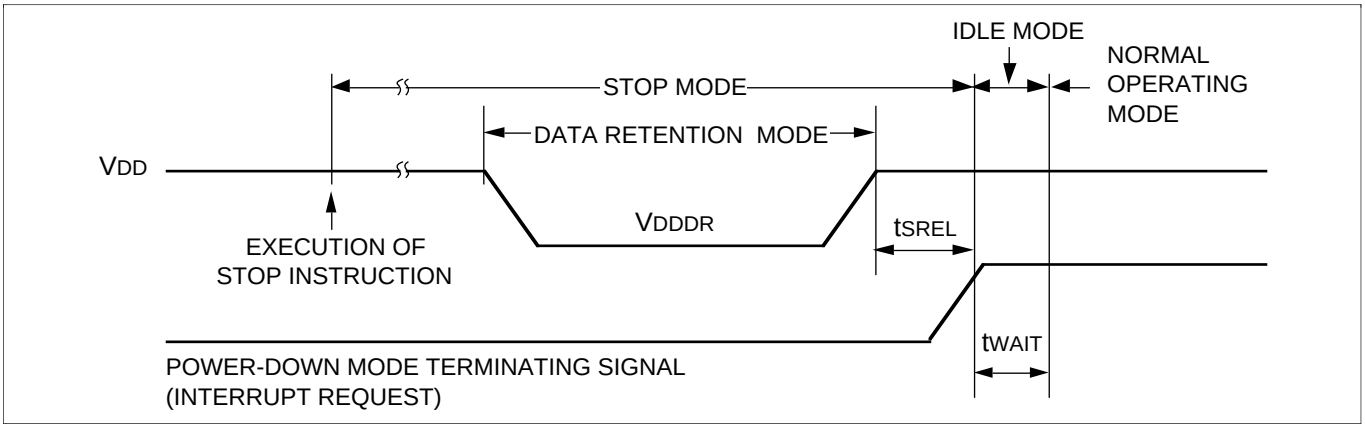


Figure 39. Stop Mode Release Timing When Initiated By Interrupt Request

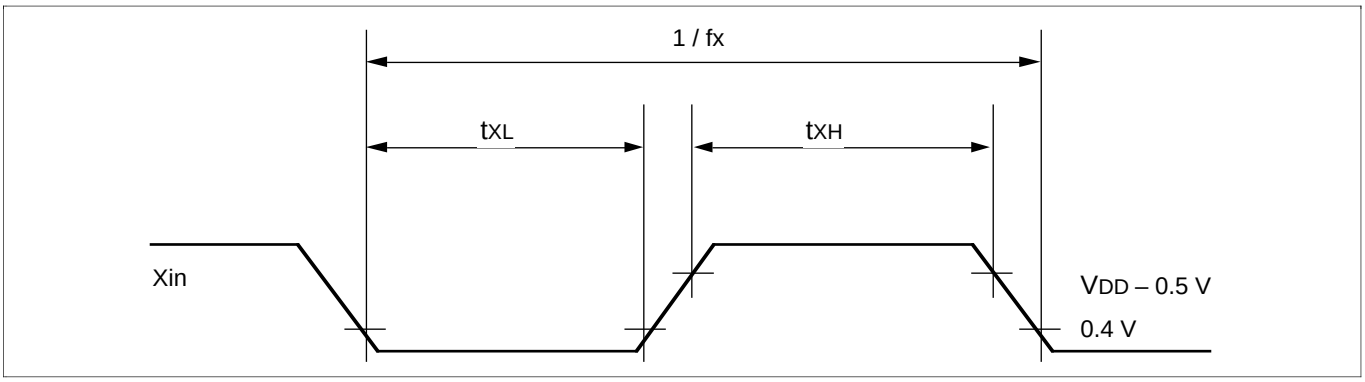


Figure 40 Clock Timing Measurement at X_{in}

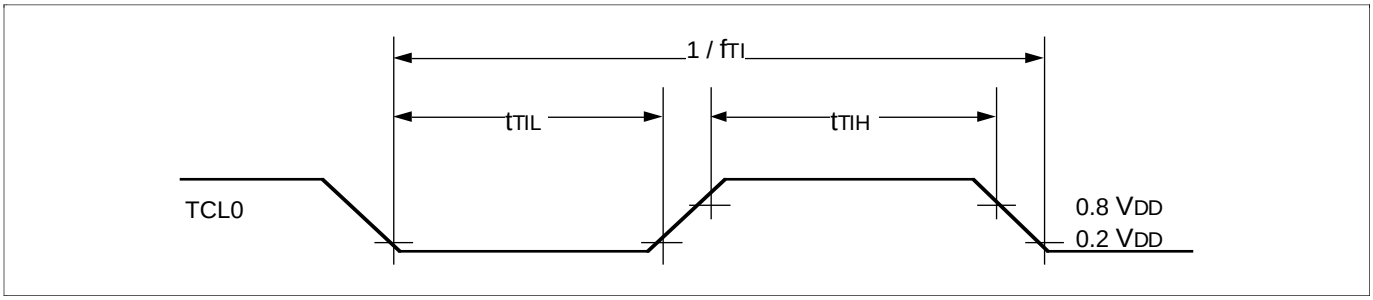


Figure 41. TCL0 Timing

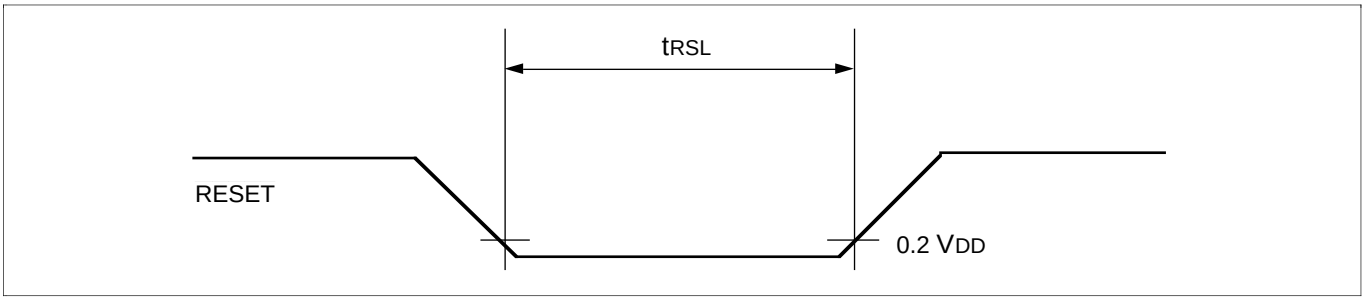


Figure 42. Input Timing for RESET Signal

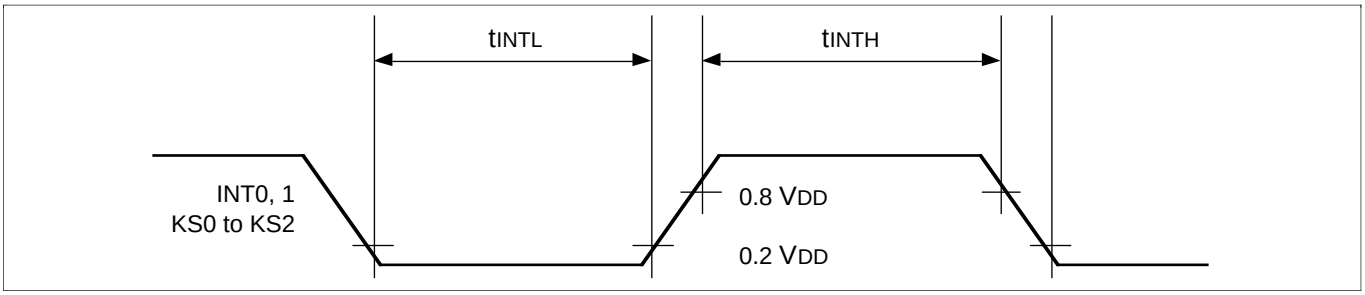


Figure 43. Input Timing for External Interrupts

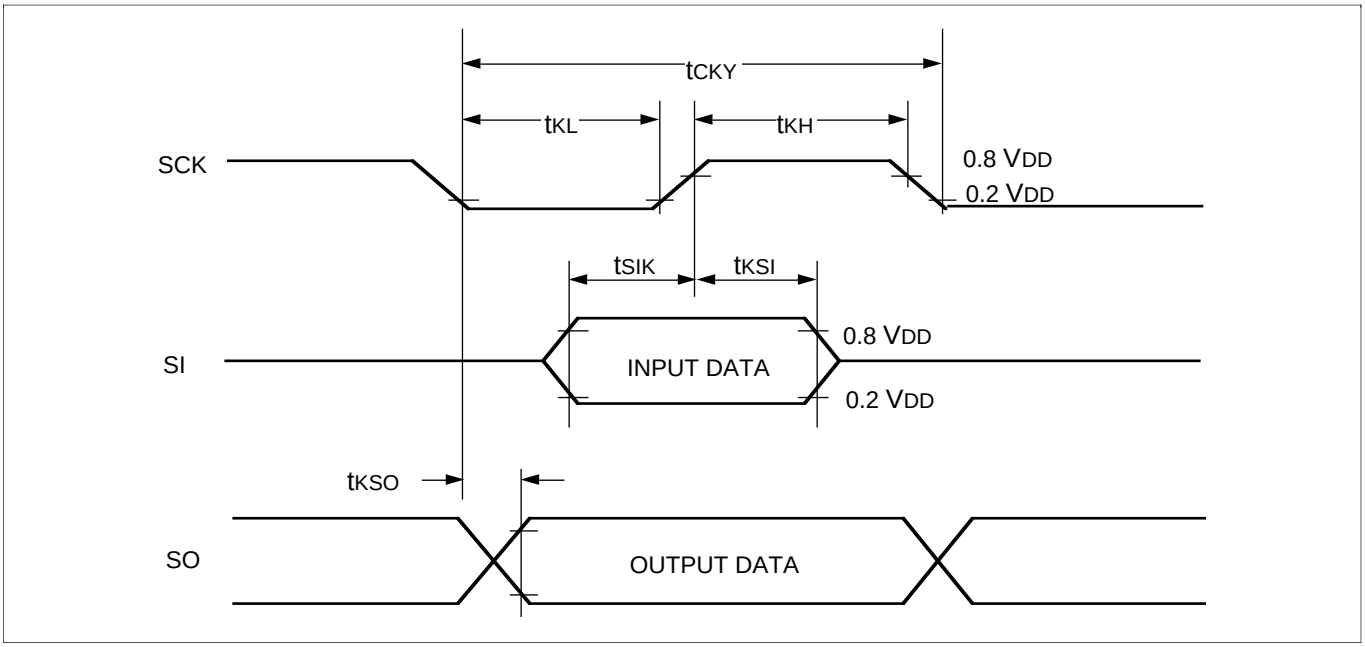


Figure 44. Serial Data Transfer Timing

CHARACTERISTIC CURVES

NOTE

The characteristic values shown in the following graphs are based on actual test measurements. They do not, however, represent guaranteed operating values.

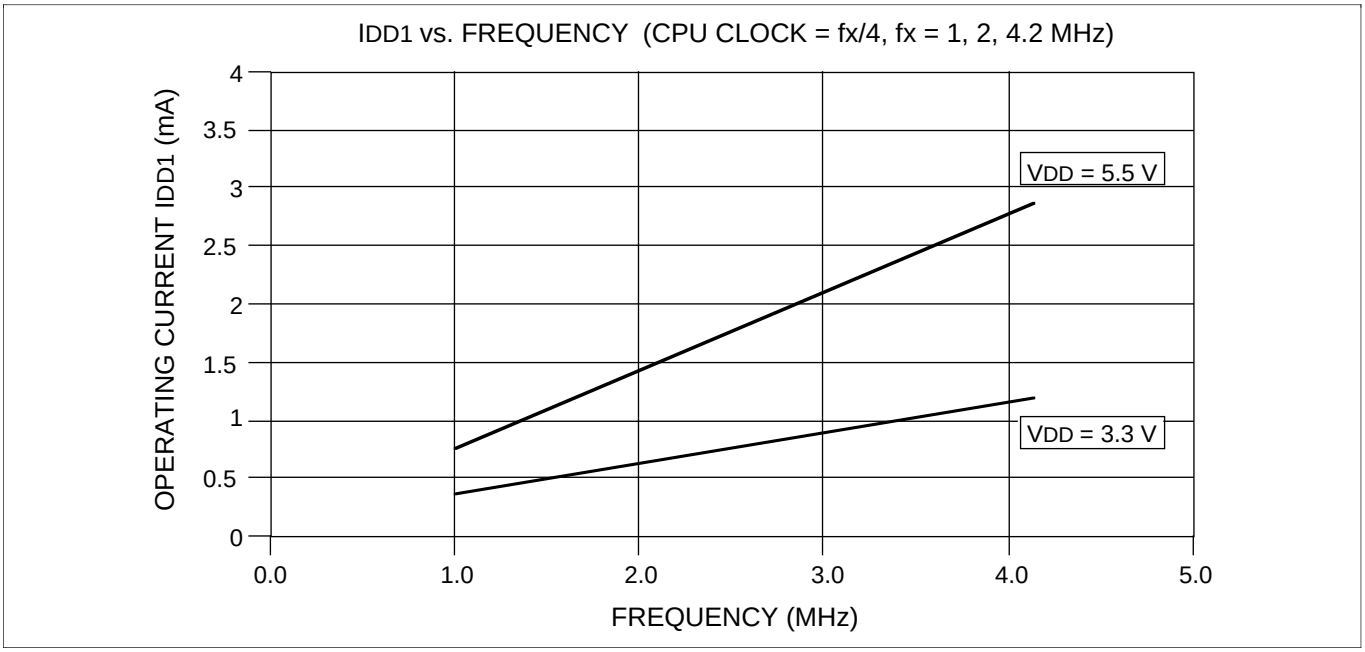


Figure 45. Frequency VS. I_{DD1}

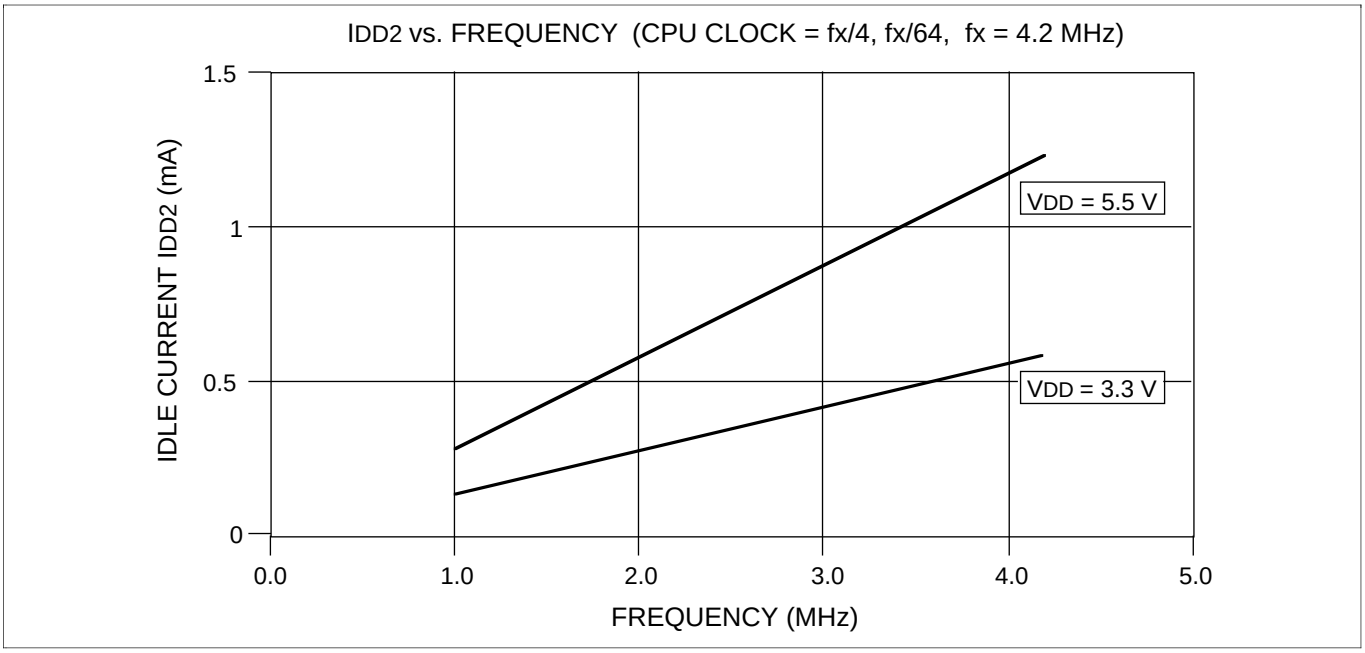


Figure 46. Frequency VS. I_{DD2}

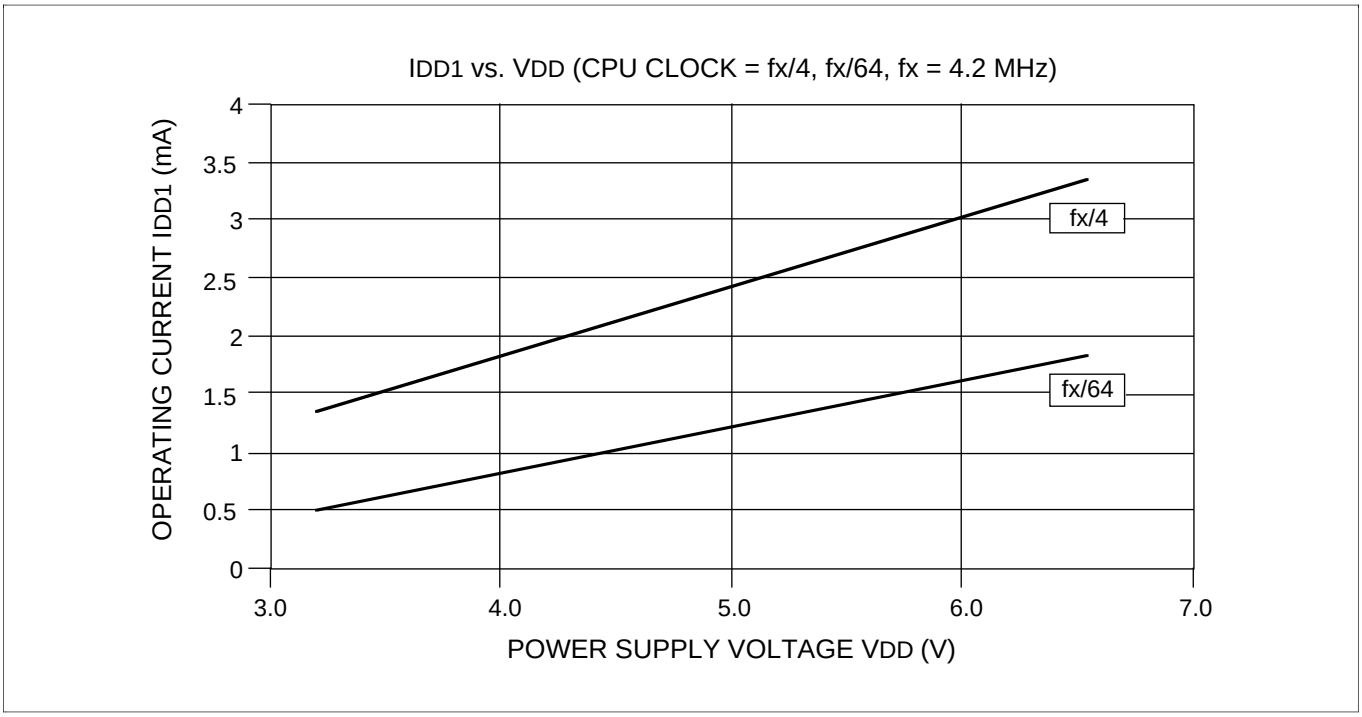


Figure 47. V_{DD} vs. I_{DD1}

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