MIC2127A

75V, Synchronous Buck Controller Featuring Adaptive On-Time Control

Features

- Hyper Speed Control® Architecture Enables:
  - High Input to Output Voltage Conversion Ratio Capability
  - Any Capacitor™ Stable
  - Ultra-Fast Load Transient Response
- Wide 4.5V-75V Input Voltage Range
- Adjustable Output Voltage from 0.6V to 30V
- 270 kHz-800 kHz Programmable Switching Frequency
- Built-In 5V Regulator for Single-Supply Operation
- Auxiliary Bootstrap LDO for Improving System Efficiency
- Internal Bootstrap Diode
- Selectable Light Load Operating Mode
- Enable Input and Power Good Output
- Programmable Current Limit
- Hiccup Mode Short-Circuit Protection
- Soft Start, Internal Compensation and Thermal Shutdown
- Supports Safe Start-Up into a Prebiased Output

Applications

- Networking/Telecom Equipment
- Base Station, Servers
- Distributed Power Systems
- Industrial Power Supplies

General Description

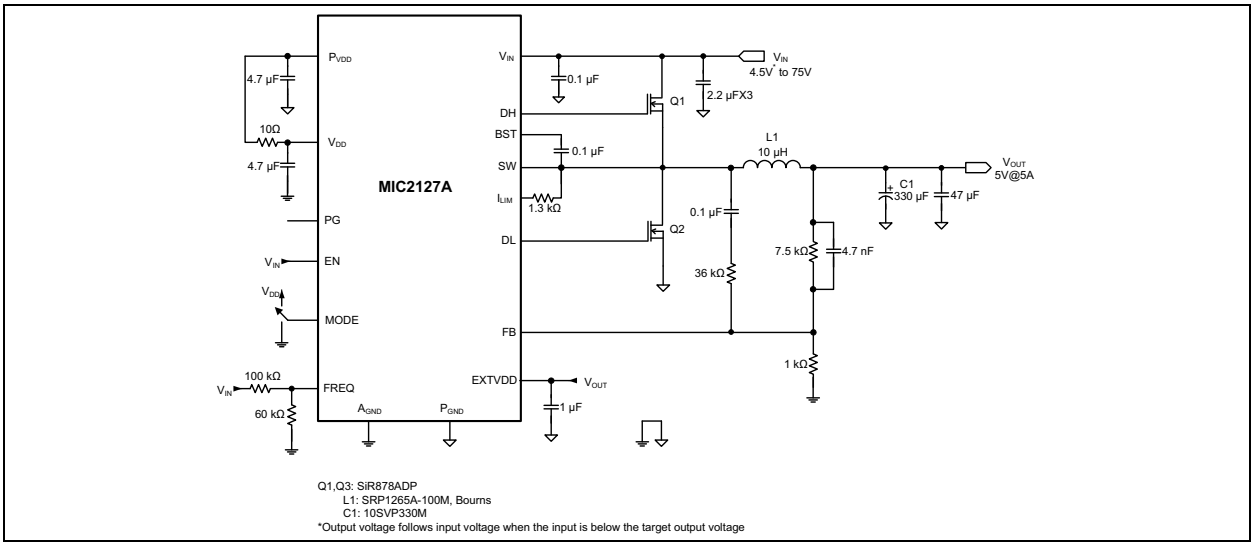
The MIC2127A is a constant-frequency synchronous buck controller featuring a unique adaptive on-time control architecture. The MIC2127A operates over an input voltage range from 4.5V-75V. The output voltage is adjustable down to 0.6V with an accuracy of ±1%. The device operates with programmable switching frequency from 270 kHz-800 kHz.

The MIC2127A features a MODE pin that allows the user to select either Continuous Conduction mode or Hyper Light Load (HLL) mode under light loads. An auxiliary bootstrap LDO improves the system efficiency by supplying the MIC2127A internal circuit bias power and gate drivers from the output of the converter. A logic level enable (EN) signal can be used to enable or disable the controller. The MIC2127A can start-up monotonically into a prebiased output. The MIC2127A features an open drain power good signal (PG) that signals when the output is in regulation and can be used for simple power supply sequencing.

The MIC2127A offers a full suite of protection features to ensure protection of the IC during Fault conditions. These include undervoltage lockout to ensure proper operation under power-sag conditions, “hiccup” mode short-circuit protection, internal soft start of 5 ms to reduce inrush current during start-up and thermal shutdown.

The MIC2127A is available in a 16-pin 3 mm x 3 mm VQFN package, with an operating junction temperature range from –40°C to +125°C.

Typical Application

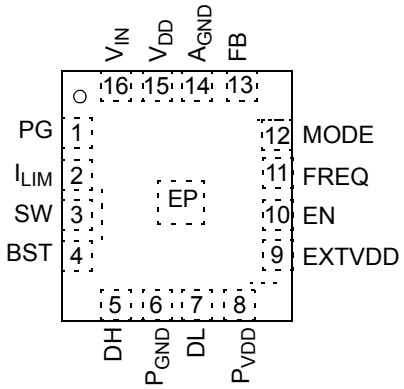


Q1,Q3: SiR878ADP
L1: SRP1265A-100M, Bourns
C1: 10SVP330M
*Output voltage follows input voltage when the input is below the target output voltage

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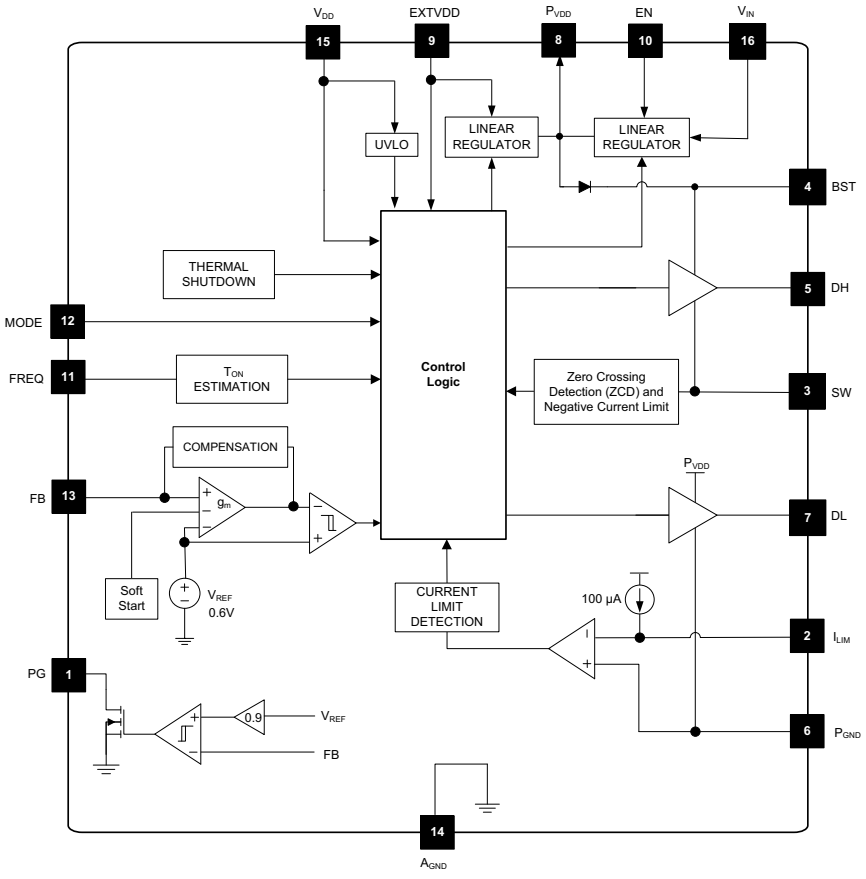
Package Types

MIC2127A
3 x 3 VQFN*
(Top View)



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN}, FREQ, I_{LIM}, SW to P_{GND} ..... –0.3V to +76V
V_{DD}, P_{VDD}, FB, PG, MODE to A_{GND} ..... –0.3V to +6V
EXTVDD to A_{GND} ..... –0.3V to +16V
BST to SW ..... –0.3V to +6V
BST to A_{GND} ..... –0.3V to +82V
EN to A_{GND} ..... –0.3V to (V_{IN} +0.3V)
DH, DL to A_{GND} ..... –0.3V to (V_{DD} +0.3V)
P_{GND} to A_{GND} ..... –0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10s) ..... 260°C
ESD Rating[1] 1000V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

Operating Ratings[1]

Supply Voltage (V_{IN}) ..... 4.5V to 75V
SW, FREQ, I_{LIM}, EN ..... 0V to V_{IN}
Junction Temperature (T_J) ..... –40°C to +125°C
Package Thermal Resistance (3 mm × 3 mm VQFN 16LD)
Junction to Ambient (θ_{JA}) ..... 50.8°C/W
Junction to Case (θ_{JC}) ..... 25.3°C/W

Note 1: The device is not ensured to function outside the operating range.

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ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Specifications: unless otherwise specified, V_{IN} = 12V, V_{OUT} = 1.2V; $V_{BST} - V_{SW}$ = 5V, T_A = +25°C. **Boldface** values indicate –40°C ≤ T_J ≤ +125°C (Note 2).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Power Supply Input						
Input Voltage Range	V_{VIN}	**4.5**	—	**5.5**	V	P_{VDD} and V_{DD} shorted to V_{IN} (V_{PVDD} = V_{VIN} = V_{VDD})
		5.5	—	**75**		
Quiescent Supply Current	I_Q	—	1.4	1.8	mA	V_{FB} = 1.5V, MODE = V_{DD}, no switching
		—	300	600	µA	V_{FB} = 1.5V, MODE = A_{GND}, no switching
Shutdown Supply Current	$I_{VIN(SHDN)}$	—	0.1	**5**	µA	EN = Low
		—	30	**60**	µA	EN = Low, V_{IN} = V_{DD} = 5.5V
P_{VDD},V_{DD} and EXTVDD						
P_{VDD} Output Voltage	V_{PVDD}	**4.8**	5.1	**5.4**	V	V_{VIN} = 7V to 75V, I_{PVDD} = 10 mA
V_{DD} UVLO Threshold	$V_{VDD_UVLO_Rise}$	**3.7**	4.2	**4.5**	V	V_{DD} rising
V_{DD} UVLO Hysteresis	$V_{VDD_UVLO_Hys}$	—	600	—	mV	V_{DD} falling
EXTVDD Bypass Threshold	V_{EXTVDD_Rise}	**4.4**	4.6	**4.85**	V	EXTVDD rising
EXTVDD Bypass Hysteresis	V_{EXTVDD_Hys}	—	200	—	mV	
EXTVDD Dropout Voltage		—	250	—	mV	V_{EXTVDD} = 5V, I_{PVDD} = 25 mA
Reference						
Feedback Reference Voltage	V_{REF}	0.597	0.6	0.603	V	T_J = 25°C
		0.594	0.6	**0.606**	V	–40°C ≤ T_J ≤ 125°C
FB Bias Current (Note 3)	I_{FB}	—	50	**500**	nA	V_{FB} = 0.6V
Enable Control						
EN Logic Level High	V_{EN_H}	**1.6**	—	—	V	
EN Logic Level Low	V_{EN_L}	—	—	**0.6**	V	
EN Hysteresis	V_{EN_Hys}	—	100	—	mV	
EN Bias Current	I_{EN}	—	6	**30**	µA	V_{EN} = 12V
ON Timer						
Switching Frequency	f_0	—	800	—	kHz	V_{FREQ} = V_{VIN}, V_{VIN} = 12V
		230	270	**300**		V_{FREQ} = 33% of V_{VIN}, V_{VIN} = 12V
Maximum Duty Cycle	D_{MAX}	—	85	—	%	V_{FREQ} = V_{VIN} = 12V
Minimum Duty Cycle	D_{MIN}	—	0	—	%	V_{FB} > 0.6V
Minimum ON Time	$t_{ON(MIN)}$	—	80	—	ns	
Minimum OFF Time	$t_{OFF(MIN)}$	**150**	230	**350**	ns	
MODE						
MODE Logic High Level	V_{MODE_H}	**1.6**	—	—	V	
MODE Logic Low Level	V_{MODE_L}	—	—	**0.6**	V	
MODE Hysteresis	V_{MODE_Hys}	—	70	—	mV	

Note 1: Specification for packaged product only.

2: The application is fully functional at low V_{DD} (supply of the control section) if the external MOSFETs have low voltage V_{TH}.

3: Design specification.

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ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Specifications: unless otherwise specified, V_{IN} = 12V, V_{OUT} = 1.2V; $V_{BST} – V_{SW}$ = 5V, T_A = +25°C. **Boldface** values indicate –40°C ≤ T_J ≤ +125°C (Note 2).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Current Limit						
Current-Limit Comparator Offset	V_{OFFSET}	**–15**	0	**15**	mV	V_{FB} = 0.59V
I_{LIM} Source Current	I_{CL}	90	100	110	µA	V_{FB} = 0.59V
I_{LIM} Source Current Tempco		—	0.3	—	µA/°C	
Negative Current Limit Comparator Threshold	—	—	48	—	mV	
Zero Crossing Detection Comparator						
Zero Crossing Detection Comparator Threshold		**–24**	–8	**8**	mV	
FET Drivers						
DH On-Resistance, High State	$R_{DH(PULL-UP)}$	—	2	**3**	Ω	
DH On-Resistance, Low State	$RDH_{(PULL_DOWN)}$	—	2	**4**	Ω	
DL On-Resistance, High State	$R_{DL(PULL-UP)}$	—	2	**4**	Ω	
DL On-Resistance, Low State	$R_{DL(PULL_DOWN)}$	—	0.36	**0.8**	Ω	
SW, VIN and BST Leakage						
BST Leakage	—	—	—	**30**	µA	
V_{IN} Leakage	—	—	—	**50**	µA	
SW Leakage	—	—	—	**50**	µA	
Power Good (PG)						
PG Threshold Voltage	V_{PG_Rise}	**85**	—	**95**	$\%V_{OUT}$	V_{FB} rising
PG Hysteresis	V_{PG_Hys}	—	6	—	$\%V_{OUT}$	V_{FB} falling
PG Delay Time	PG_R_DLY	—	150	—	µs	V_{FB} rising
PG Low Voltage	V_{OL_PG}	—	140	**200**	mV	V_{FB} < 90% × V_{NOM}, I_{PG} = 1 mA
Thermal Protection						
Overtemperature Shutdown	T_{SHDN}	—	150	—	°C	Junction temperature rising
Overtemperature Shutdown Hysteresis	T_{SHDN_Hys}	—	15	—	°C	

Note 1: Specification for packaged product only.

2: The application is fully functional at low V_{DD} (supply of the control section) if the external MOSFETs have low voltage V_{TH}.

3: Design specification.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: unless otherwise specified, V_{IN} = 12V, V_{OUT} = 1.2V; $V_{BST} – V_{SW}$ = 5V, T_A = +25°C.

Parameters		Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges							
Storage Temperature		T_S	–65	—	+150	°C	
Junction Temperature		T_J	–40	—	+150	°C	
Package Thermal Resistances							
Thermal Resistance, 16 Lead, 3 x 3 mm VQFN	Junction to Ambient	θ_{JA}	—	50.8	—	°C/W	
	Junction to Case	θ_{JC}		25.3		°C/W	

2.0 TYPICAL CHARACTERISTIC CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{VIN} = 12V, f_{SW} = 300 kHz, R_{ILIM} = 1.3 kΩ, L = 10 µH, V_{EXTVDD} = V_{OUT}, T_A = +25°C (refer to the Typical Application circuit).

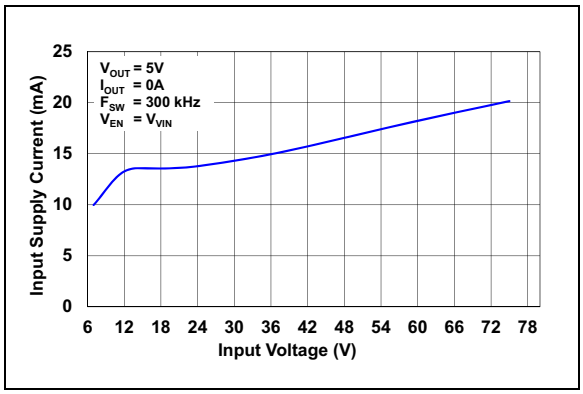


FIGURE 2-1: *Input Supply Current vs. Input Voltage.*

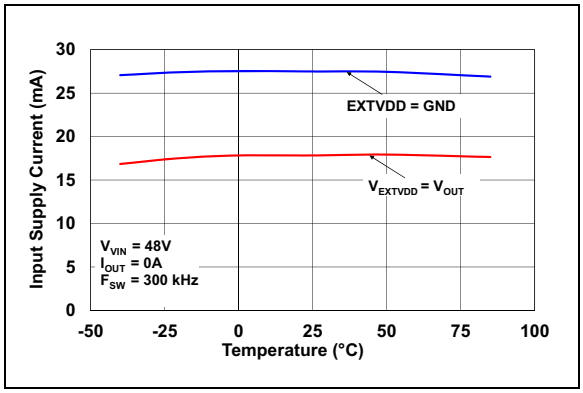


FIGURE 2-2: *Input Supply Current vs. Temperature.*

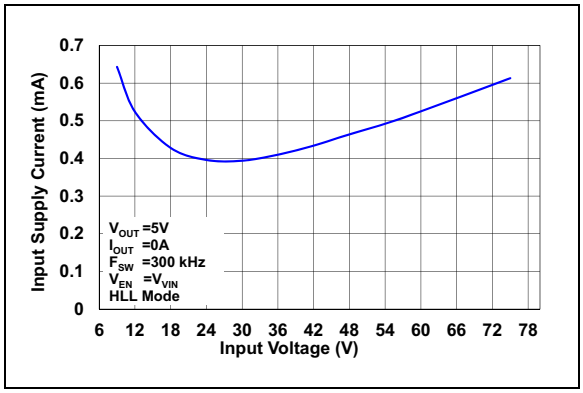


FIGURE 2-3: *Input Supply Current vs. Input Voltage (HLL Mode).*

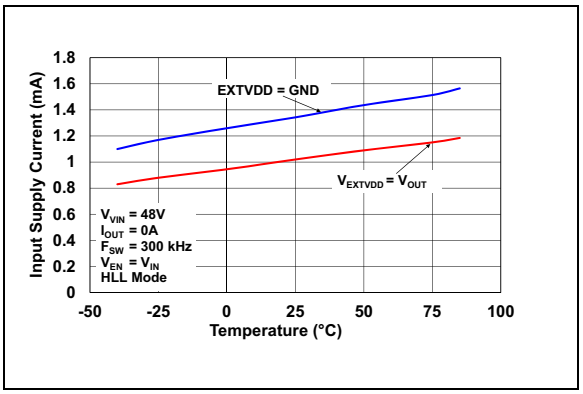


FIGURE 2-4: *Input Supply Current vs. Temperature (HLL Mode).*

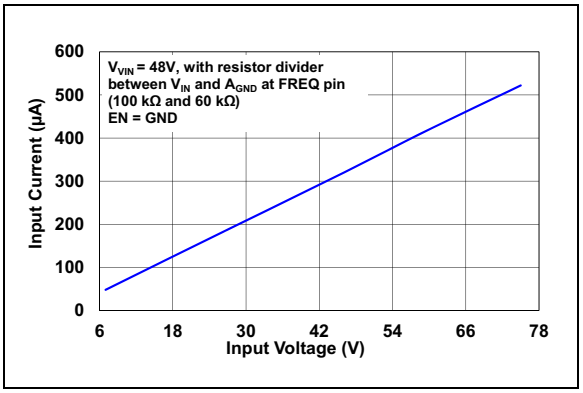


FIGURE 2-5: *Input Shutdown Current vs. Input Voltage.*

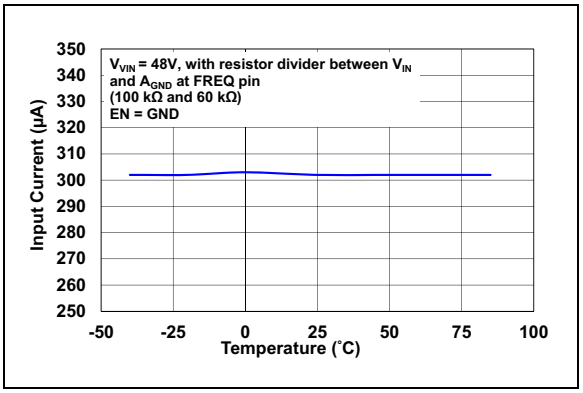


FIGURE 2-6: *Input Shutdown Current vs. Temperature.*

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Note: Unless otherwise indicated, V_{VIN} = 12V, f_{SW} = 300 kHz, R_{ILIM} = 1.3 kΩ, L = 10 µH, V_{EXTVDD} = V_{OUT}, T_A = +25°C (refer to the Typical Application circuit).

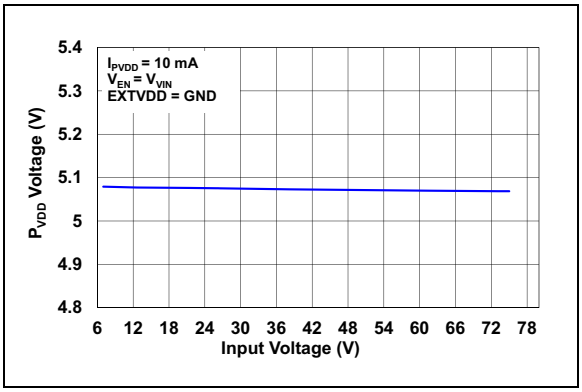


FIGURE 2-7: *P_{VDD} Line Regulation.*

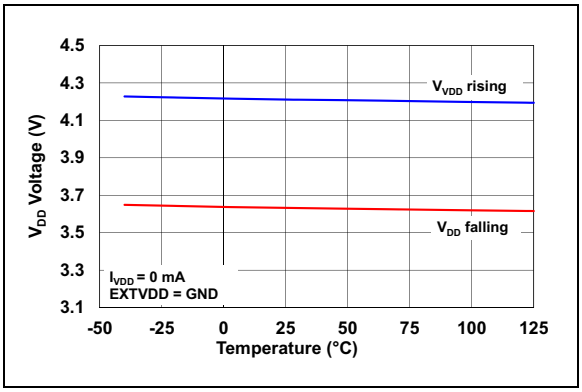


FIGURE 2-10: *V_{DD} UVLO Threshold vs. Temperature.*

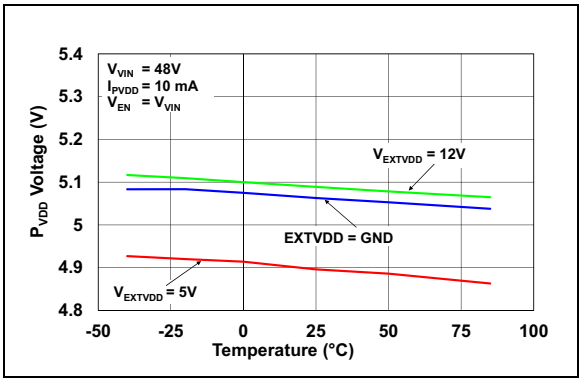


FIGURE 2-8: *P_{VDD} Voltage vs. Temperature.*

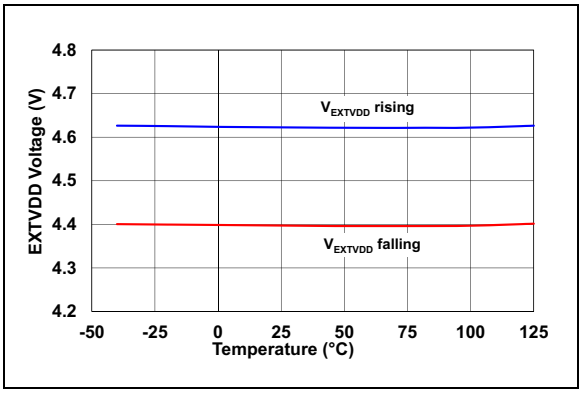


FIGURE 2-11: *EXTVDD Threshold vs. Temperature.*

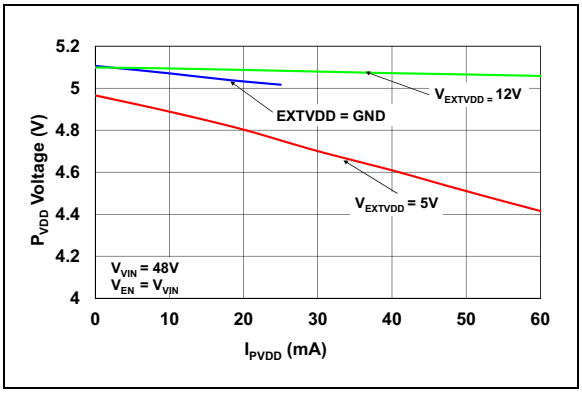


FIGURE 2-9: *P_{VDD} Load Regulation.*

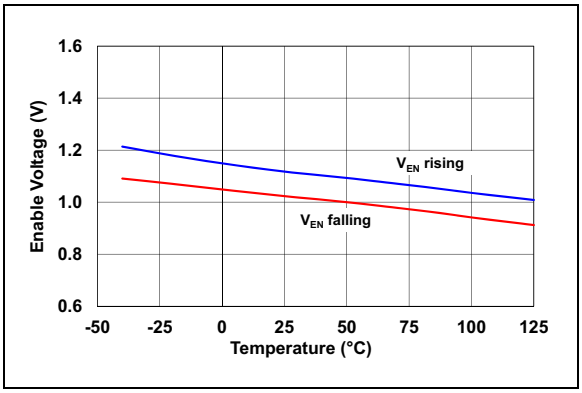


FIGURE 2-12: *Enable Threshold vs. Temperature.*

Note: Unless otherwise indicated, V_{VIN} = 12V, f_{SW} = 300 kHz, R_{ILIM} = 1.3 kΩ, L = 10 µH, V_{EXTVDD} = V_{OUT}, T_A = +25°C (refer to the Typical Application circuit).

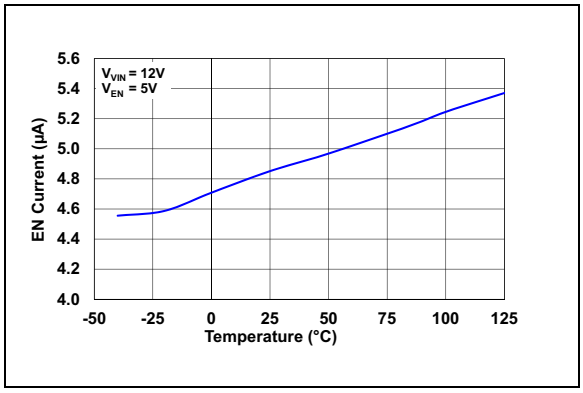


FIGURE 2-13: *Enable Bias Current vs. Temperature.*

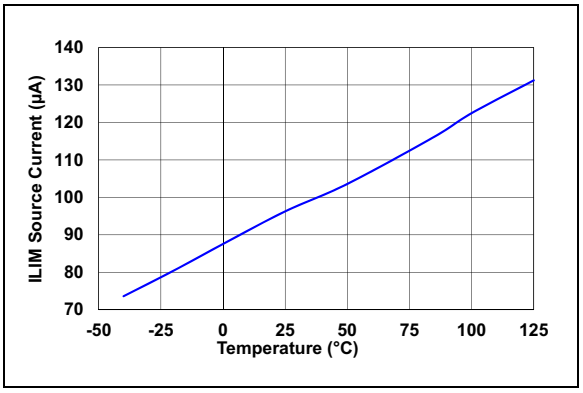


FIGURE 2-16: *I_{LIM} Source Current vs. Temperature.*

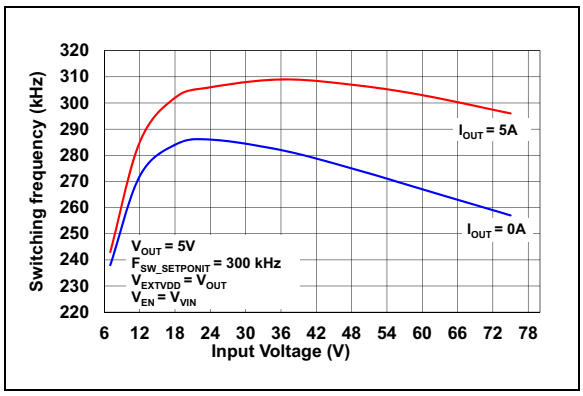


FIGURE 2-14: *Switching Frequency vs. Input Voltage.*

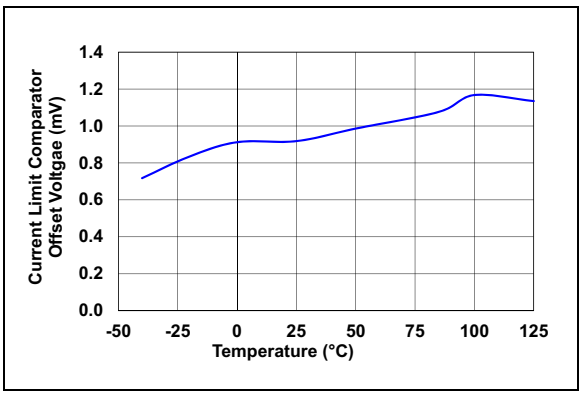


FIGURE 2-17: *Current Limit Comparator Offset vs Temperature.*

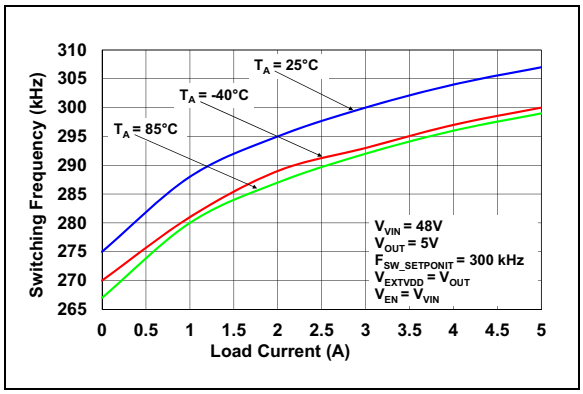


FIGURE 2-15: *Switching Frequency vs. Load Current.*

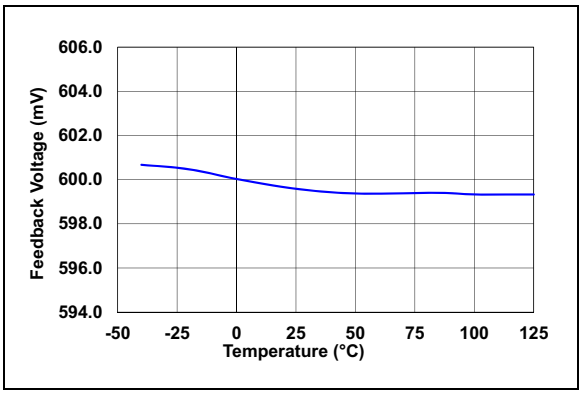


FIGURE 2-18: *Feedback Voltage vs. Temperature.*

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Note: Unless otherwise indicated, V_{VIN} = 12V, f_{SW} = 300 kHz, R_{ILIM} = 1.3 kΩ, L = 10 µH, V_{EXTVDD} = V_{OUT}, T_A = +25°C (refer to the Typical Application circuit).

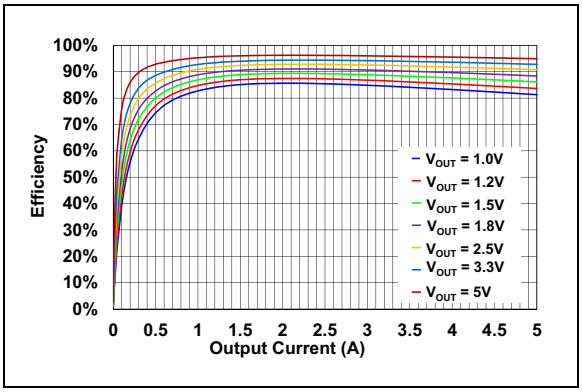


FIGURE 2-19: *Efficiency vs. Output Current (Input Voltage = 12V, CCM Mode).*

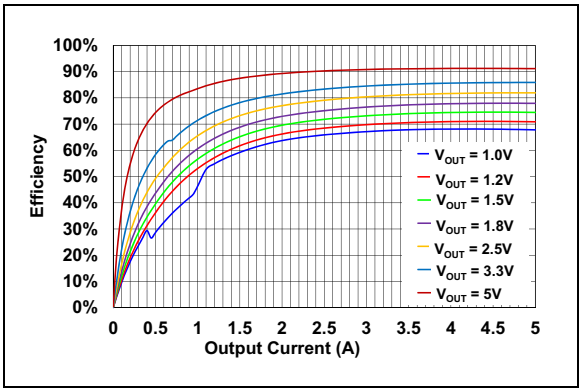


FIGURE 2-22: *Efficiency vs. Output Current (Input Voltage = 48V, CCM Mode).*

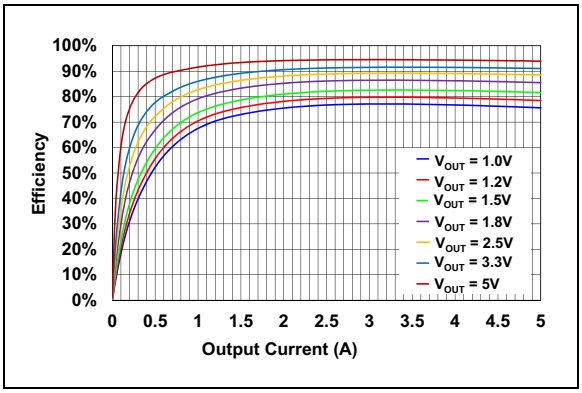


FIGURE 2-20: *Efficiency vs. Output Current (Input Voltage = 24V, CCM Mode).*

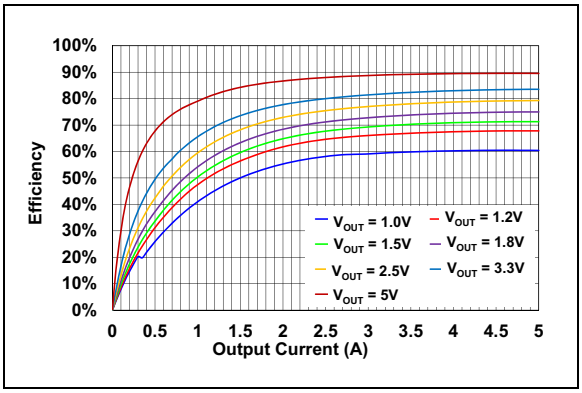


FIGURE 2-23: *Efficiency vs. Output Current (Input Voltage = 60V, CCM Mode).*

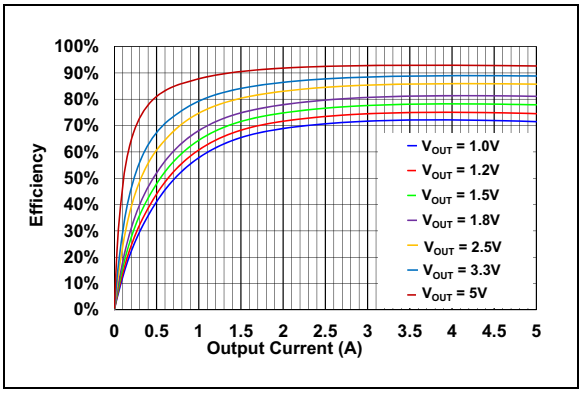


FIGURE 2-21: *Efficiency vs. Output Current (Input Voltage = 36V, CCM Mode).*

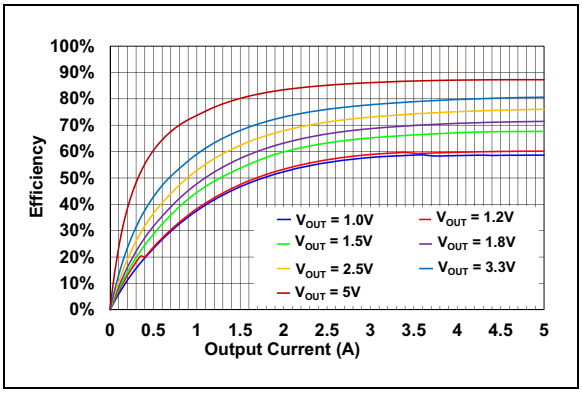


FIGURE 2-24: *Efficiency vs. Output Current (Input Voltage = 75V, CCM Mode).*

Note: Unless otherwise indicated, V_{VIN} = 12V, f_{SW} = 300 kHz, R_{ILIM} = 1.3 kΩ, L = 10 µH, V_{EXTVDD} = V_{OUT}, T_A = +25°C (refer to the Typical Application circuit).

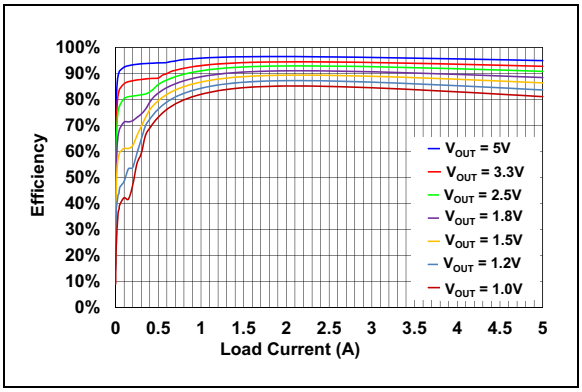


FIGURE 2-25: *Efficiency vs. Output Current (Input Voltage = 12V, HLL Mode).*

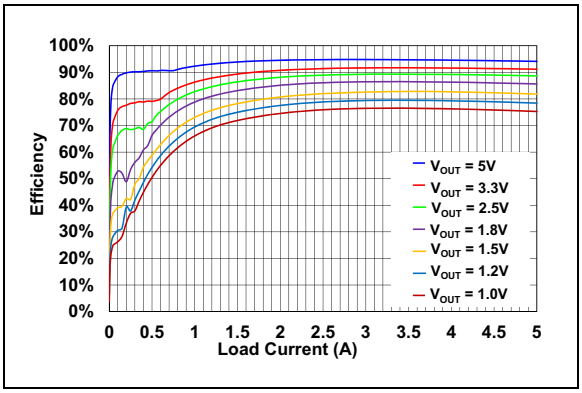


FIGURE 2-26: *Efficiency vs. Output Current (Input Voltage = 24V, HLL Mode).*

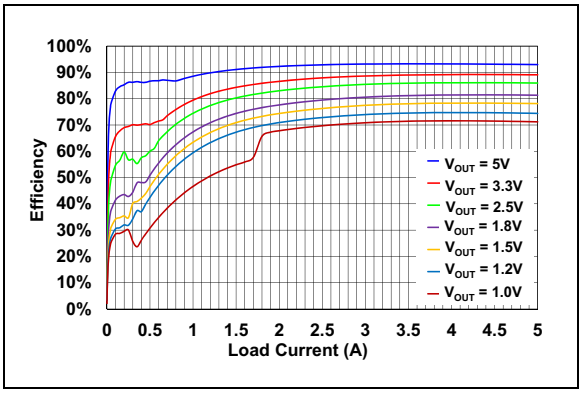


FIGURE 2-27: *Efficiency vs. Output Current (Input Voltage = 36V, HLL Mode).*

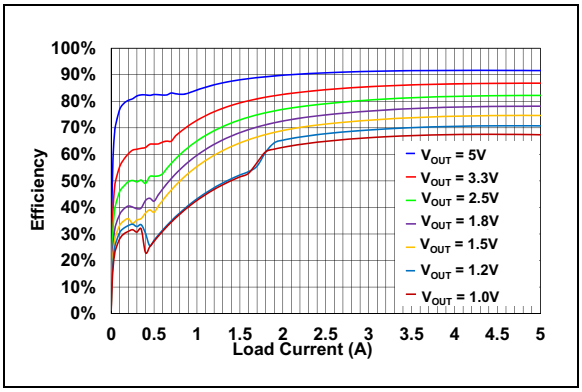


FIGURE 2-28: *Efficiency vs. Output Current (Input Voltage = 48V, HLL Mode).*

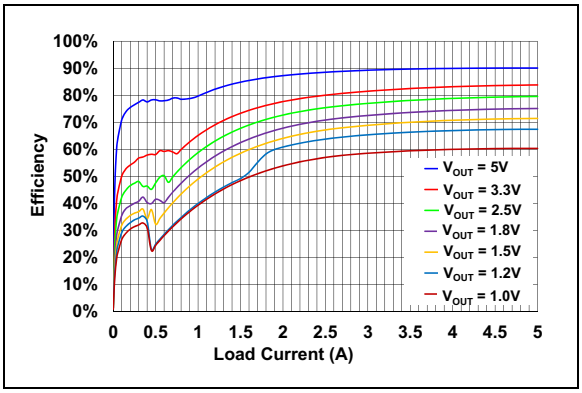


FIGURE 2-29: *Efficiency vs. Output Current (Input Voltage = 60V, HLL Mode).*

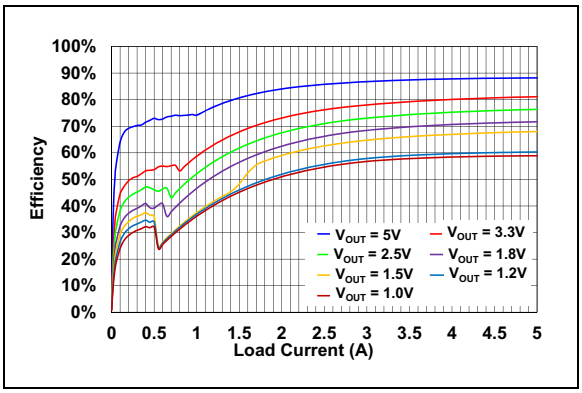


FIGURE 2-30: *Efficiency vs. Output Current (Input Voltage = 75V, HLL Mode).*

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Note: Unless otherwise indicated, V_{VIN} = 12V, f_{SW} = 300 kHz, R_{ILIM} = 1.3 kΩ, L = 10 µH, V_{EXTVDD} = V_{OUT}, T_A = +25°C (refer to the Typical Application circuit).

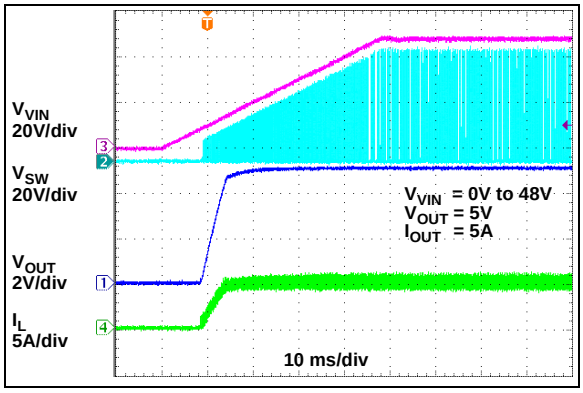


FIGURE 2-31: *Power-Up.*

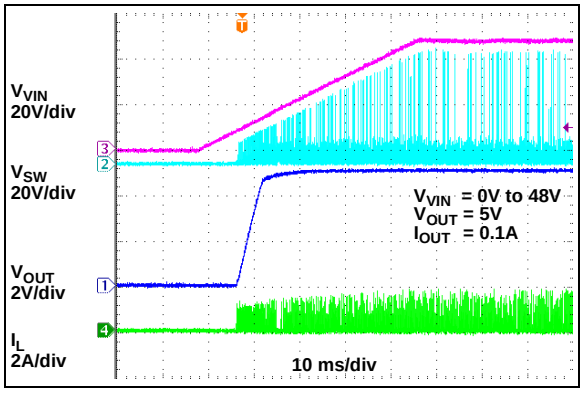


FIGURE 2-34: *Power-Up at Light Load in HLL Mode (I_{OUT} = 0.1A).*

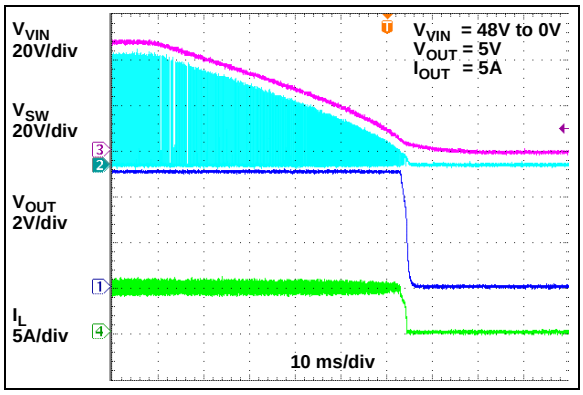


FIGURE 2-32: *Power-Down.*

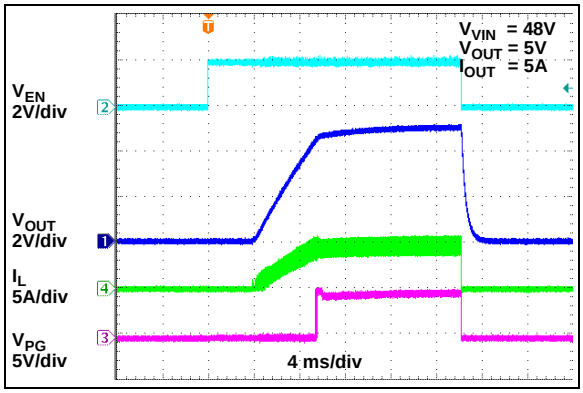


FIGURE 2-35: *Enable Turn-On/Turn-Off.*

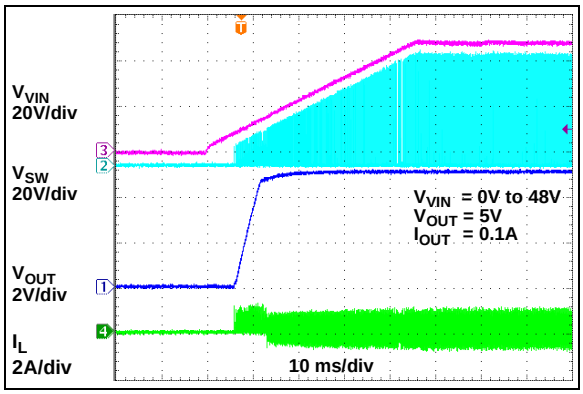


FIGURE 2-33: *Power-Up at Light Load in CCM Mode (I_{OUT} = 0.1A).*

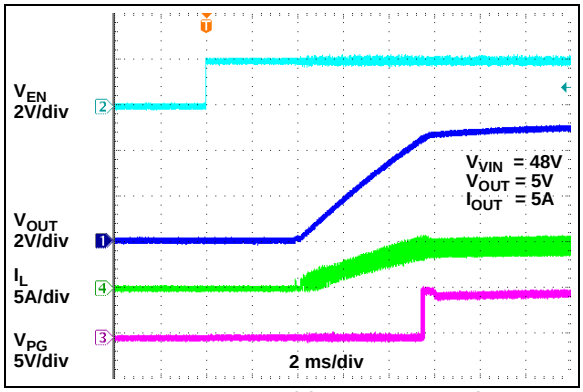


FIGURE 2-36: *Enable Turn-On Delay.*

Note: Unless otherwise indicated, V_{VIN} = 12V, f_{SW} = 300 kHz, R_{ILIM} = 1.3 kΩ, L = 10 µH, V_{EXTVDD} = V_{OUT}, T_A = +25°C (refer to the Typical Application circuit).

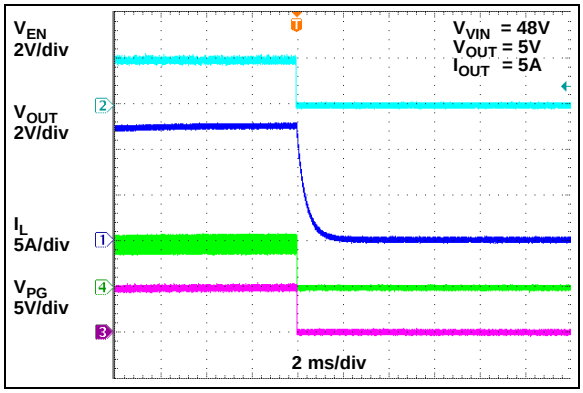


FIGURE 2-37: *Enable Turn-Off Delay.*

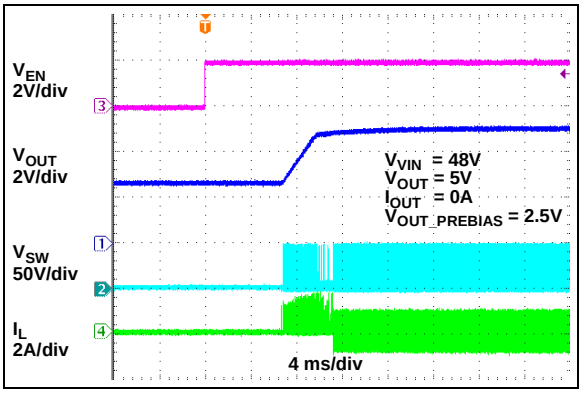


FIGURE 2-40: *Enable Turn-On with Prebiased Output (CCM Mode).*

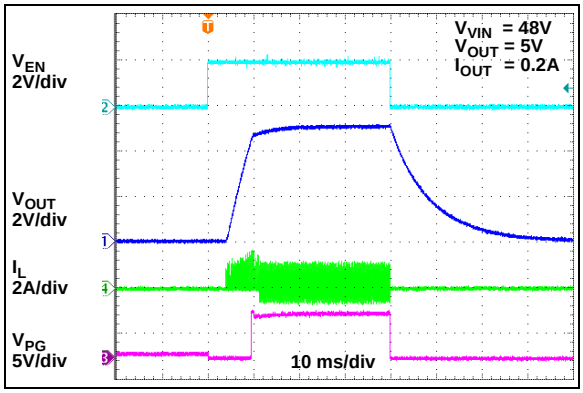


FIGURE 2-38: *Enable Turn-On/Turn-Off at Light Load in CCM Mode.*

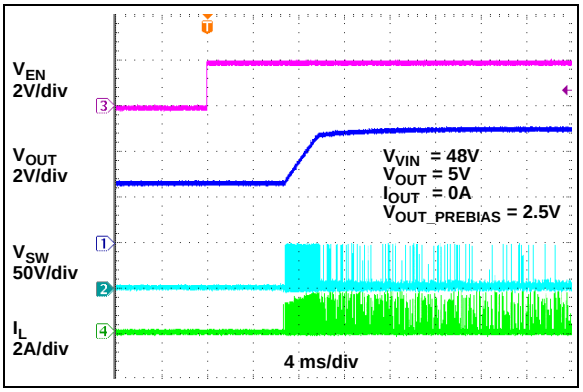


FIGURE 2-41: *Enable Turn-On with Prebiased Output (HLL Mode).*

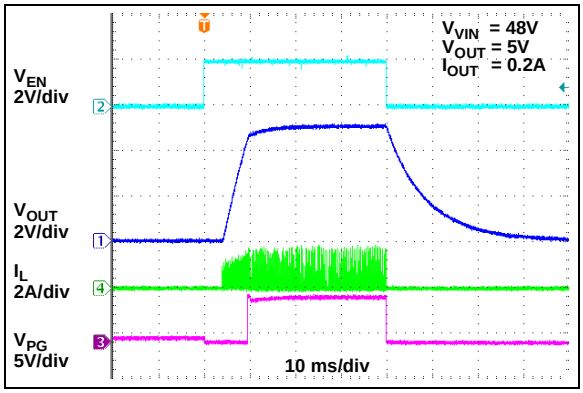


FIGURE 2-39: *Enable Turn-On/Turn-Off at Light Load in HLL Mode.*

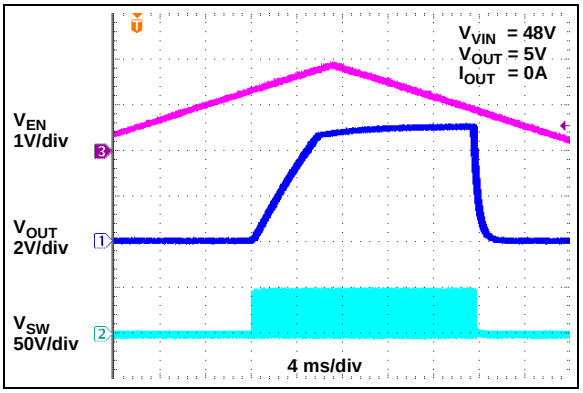


FIGURE 2-42: *Enable Thresholds.*

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Note: Unless otherwise indicated, V_{VIN} = 12V, f_{SW} = 300 kHz, R_{ILIM} = 1.3 kΩ, L = 10 µH, V_{EXTVDD} = V_{OUT}, T_A = +25°C (refer to the Typical Application circuit).

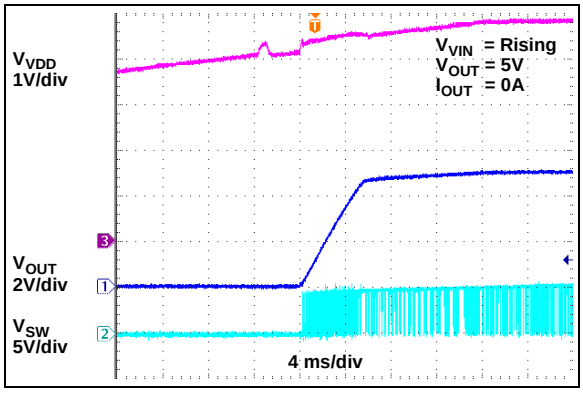


FIGURE 2-43: *V_{DD} UVLO Threshold-Rising.*

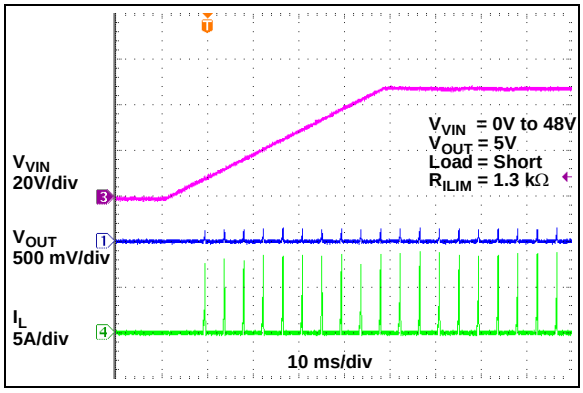


FIGURE 2-46: *Power-Up into Output Short.*

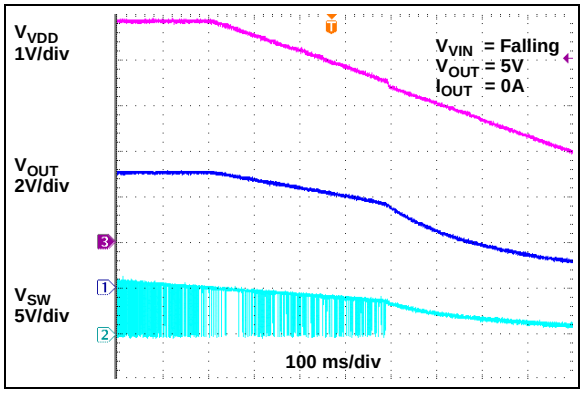


FIGURE 2-44: *V_{DD} UVLO Threshold-Falling.*

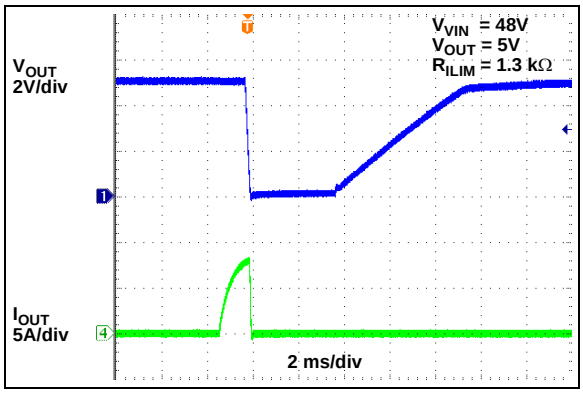


FIGURE 2-47: *Output Current Limit Threshold.*

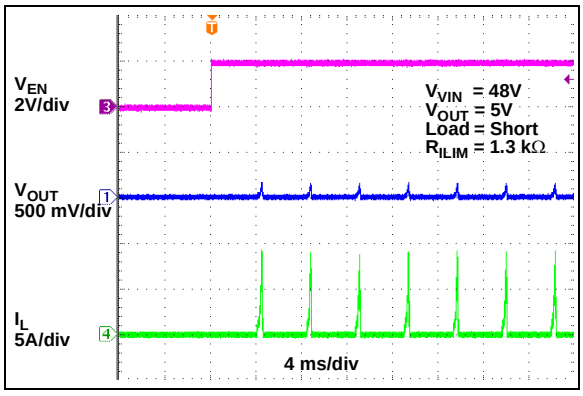


FIGURE 2-45: *Enable into Output Short.*

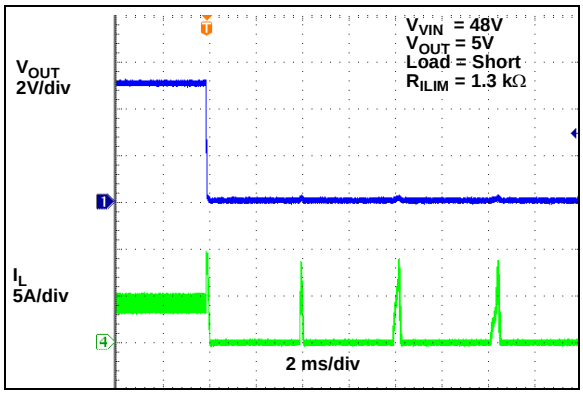


FIGURE 2-48: *Output Short Circuit.*

Note: Unless otherwise indicated, V_{VIN} = 12V, f_{SW} = 300 kHz, R_{ILIM} = 1.3 kΩ, L = 10 µH, V_{EXTVDD} = V_{OUT}, T_A = +25°C (refer to the Typical Application circuit).

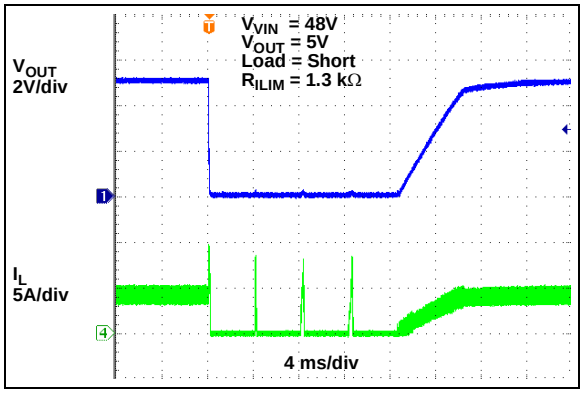


FIGURE 2-49: *Recovery from Output Short Circuit.*

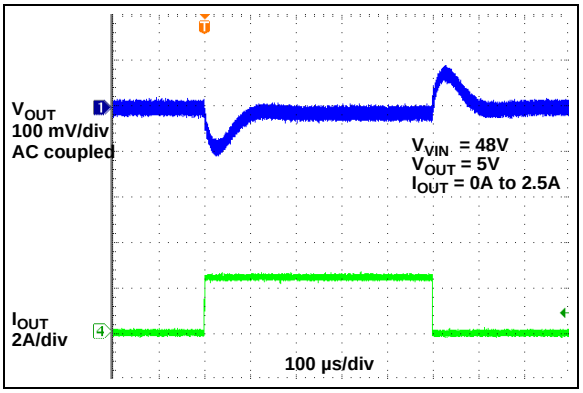


FIGURE 2-52: *Load Transient Response (CCM Mode).*

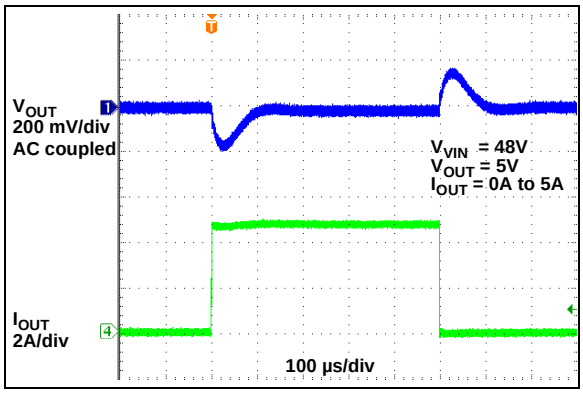


FIGURE 2-50: *Load Transient Response (CCM Mode).*

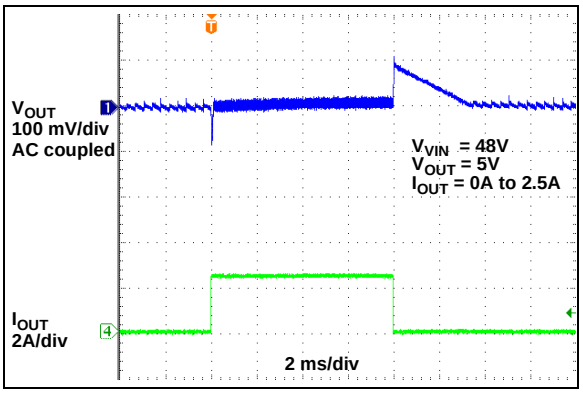


FIGURE 2-53: *Load Transient Response (HLL Mode).*

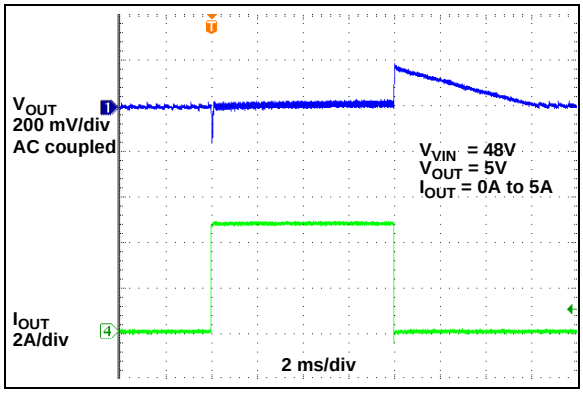


FIGURE 2-51: *Load Transient Response (HLL Mode).*

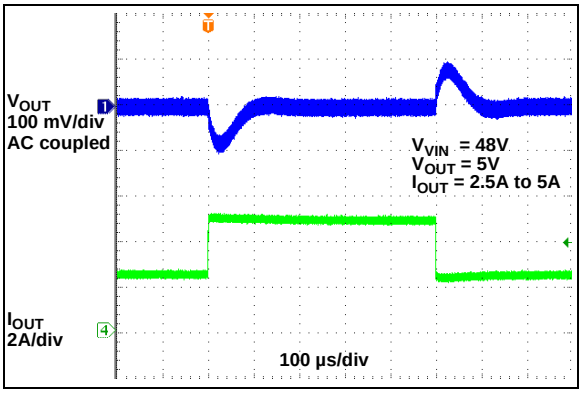


FIGURE 2-54: *Load Transient Response (HLL Mode).*

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Note: Unless otherwise indicated, V_{VIN} = 12V, f_{SW} = 300 kHz, R_{ILIM} = 1.3 kΩ, L = 10 µH, V_{EXTVDD} = V_{OUT}, T_A = +25°C (refer to the Typical Application circuit).

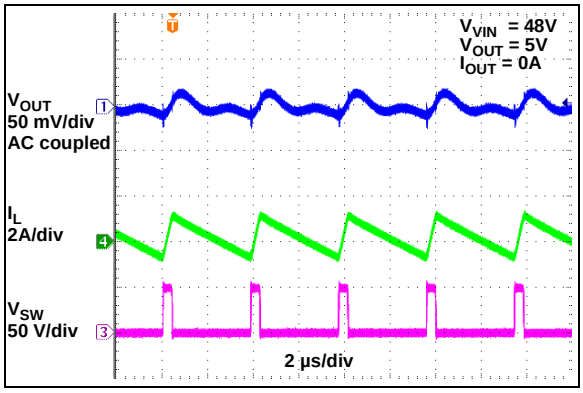


FIGURE 2-55: *Switching Waveform at No Load (CCM Mode).*

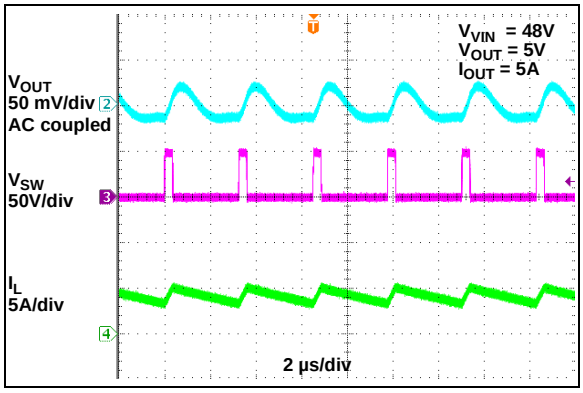


FIGURE 2-57: *Switching Waveform at Full Load.*

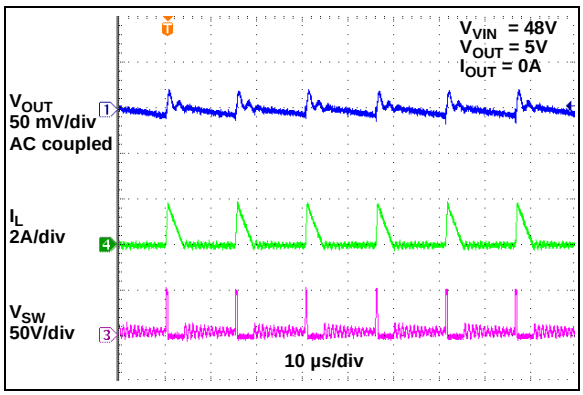


FIGURE 2-56: *Switching Waveform at No Load (HLL Mode).*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MIC2127A	Symbol	Pin Function
1	PG	Open-drain Power Good Output Pin
2	I_{LIM}	Current Limit Setting Resistor Connection Pin
3	SW	Switch Pin and Current Sense Input for negative current limit
4	BST	Bootstrap Capacitor Connection Pin
5	DH	High-side N-MOSFET Gate Driver Output
6	P_{GND}	Power Ground
7	DL	Low-side N-MOSFET Gate Driver Output
8	P_{VDD}	Internal Low Dropout Regulators Output of the MIC2127A
9	EXTVDD	Supply Input for the internal low voltage LDO
10	EN	Enable Input
11	FREQ	Switching Frequency Programming Input
12	MODE	Light Load Mode Selection Input
13	FB	Feedback Input
14	A_{GND}	Analog Ground
15	V_{DD}	Supply Input for the MIC2127A internal analog circuits
16	V_{IN}	Supply Input for the internal high-voltage LDO
17	EP	Exposed Pad

3.1 Power Good Output Pin (PG)

Connect PG to V_{DD} through a pull-up resistor. PG is low when the FB voltage is 10% below the 0.6V reference voltage.

3.2 Current Limit Pin (I_{LIM})

Connect a resistor from I_{LIM} to SW to set the current limit. Refer to **Section 4.3 "Current Limit (ILIM)"** for more details.

3.3 Switch Pin (SW)

The SW pin provides the return path for the high-side N-MOSFET gate driver when High-Side MOSFET Gate Drive (DH) is low and is also used to sense low-side MOSFET current by monitoring the SW node voltage for negative current limit function.

Connect SW to the pin where the high-side MOSFET source and the low-side MOSFET drain terminal are connected together.

3.4 Bootstrap Capacitor Pin (BST)

BST capacitor acts as supply for the high-side N-MOSFET driver. Connect a minimum of 0.1 µF low ESR ceramic capacitor between BST and SW. Refer to **Section 4.5 "High-Side MOSFET Gate Drive (DH)"** for more details.

3.5 High-Side N-MOSFET Gate Driver Output Pin (DH)

High-side N-MOSFET gate driver Output. Connect DH to the gate of external high-side N-MOSFET.

3.6 Power Ground Pin (P_{GND})

P_{GND} provides the return path for the internal low-side N-MOSFET gate driver output and also acts as reference for the current limit comparator. Connect P_{GND} to the external low-side N-MOSFET source terminal and to the return terminal of P_{VDD} bypass capacitor.

3.7 Low-Side N-MOSFET Gate Driver Output Pin (DL)

Low-side N-MOSFET gate driver output. Connect to the gate terminal of the external low-side N-MOSFET.

3.8 Internal Low Dropout Regulators Output Pin (P_{VDD})

Combined output of the two internal LDOs (one LDO powered by V_{IN} and the other LDO powered by EXTVDD). P_{VDD} is the supply for the low-side MOSFET driver and for the floating high-side MOSFET driver. Connect a minimum of 4.7 µF low ESR ceramic capacitor from P_{VDD} to P_{GND}.

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3.9 EXTVDD

Supply to the internal low voltage LDO. Connect EXTVDD to the output of the buck converter if it is between 4.7V to 14V to improve system efficiency. Bypass EXTVDD with a minimum of 1 µF low ESR ceramic capacitor.

3.10 Enable Input Pin (EN)

EN is a logic input. Connect to logic high to enable the converter, and connect to logic low to disable the converter.

3.11 Switching Frequency Programming Input Pin (FREQ)

Switching Frequency Programming Input. Connect to mid-point of the resistor divider formed between V_{IN} and A_{GND} to set the switching frequency of the converter. Tie FREQ to V_{IN} to set the switching frequency to 800 kHz. Refer to **Section 5.1 "Setting the Switching Frequency"** for more details.

3.12 Light Load Mode Selection Input Pin (MODE)

Light Load Mode Selection Input. Connect MODE pin to V_{DD} to select Continuous Conduction mode under light loads, or connect to A_{GND} to select Hyper Light Load (HLL) mode of operation under light loads. Refer to **Section 4.2 "Light Load Operating Mode (MODE)"** for further details.

3.13 Feedback Input Pin (FB)

FB is input to the transconductance amplifier of the control loop. The control loop regulates the FB voltage to 0.6V. Connect the FB node to the mid-point of the resistor divider between output and A_{GND}.

3.14 Analog Ground Pin (A_{GND})

A_{GND} is the reference to the analog control circuits inside the MIC2127A. Connect A_{GND} to P_{GND} at one point on the PCB.

3.15 Bias Voltage Pin (V_{DD})

Supply for the MIC2127A internal analog circuits. Connect V_{DD} to P_{VDD} of the MIC2127A through a low-pass filter. Connect a minimum of 4.7 µF low ESR ceramic capacitor from V_{DD} to A_{GND} for decoupling.

3.16 Input Voltage Pin (V_{IN})

Supply Input to the internal high-voltage LDO. Connect to the main power source and bypass to P_{GND} with a minimum of 0.1 µF low ESR ceramic capacitor.

3.17 Exposed Pad (EP)

Connect to the A_{GND} copper plane to improve thermal performance of the MIC2127A.

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4.0 FUNCTIONAL DESCRIPTION

The MIC2127A is an adaptive on-time synchronous buck controller, designed to cover a wide range of input voltage applications ranging from 4.5V-5V. An adaptive on-time control scheme is employed to get a fast transient response and to obtain high-voltage conversion ratios at constant switching frequency. Overcurrent protection is implemented by sensing low-side MOSFET's $R_{DS(ON)}$, which eliminates lossy current sense resistor. The device features internal soft-start, enable input, UVLO, power good output (PG), secondary bootstrap LDO and thermal shutdown.

4.1 Theory of Operation

The MIC2127A is an adaptive on-time synchronous buck controller that operates based on ripple at the feedback node. The output voltage is sensed by the MIC2127A feedback pin (FB) and is compared to a 0.6V reference voltage (V_{REF}) at the low-gain transconductance error amplifier (g_M), as shown in the Functional Block Diagram. Figure 4-1 shows the MIC2127A control loop timing during steady-state operation.

The error amplifier behaves as the short circuit for the ripple voltage frequency on the FB pin, which causes the error amplifier output voltage ripple to follow the feedback voltage ripple. When the transconductance error amplifier output (V_{gM}) is below the reference voltage of the comparator, which is same as the error amplifier reference (V_{REF}), the comparator triggers and generates an on-time event. The on-time period is predetermined by the fixed t_{ON} estimator circuitry, which is given by Equation 4-1:

EQUATION 4-1:

$$t_{ON(ESTIMATED)} = \frac{V_{OUT}}{V_{VIN} \times f_{SW}}$$

Where:

- V_{OUT} = Output voltage
- V_{VIN} = Power stage input voltage
- f_{SW} = Switching frequency

At the end of the ON time, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF time of the high-side MOSFET depends on the feedback voltage. When the feedback voltage decreases, the output of the g_M amplifier (V_{gM}) also decreases. When the output of the g_M amplifier (V_{gM}) is below the reference voltage of the comparator (which is same as the error amplifier reference (V_{REF})), the OFF time ends and ON time is triggered. If the OFF time determined by the feedback voltage is less than the minimum OFF time ($t_{OFF(MIN)}$) of the MIC2127A, which is about 230 ns (typical), the MIC2127A control logic applies the $t_{OFF(MIN)}$, instead.

The maximum duty cycle can be calculated using Equation 4-2:

EQUATION 4-2:

$$D_{MAX} = \frac{t_{SW} - t_{OFF(MIN)}}{t_{SW}} = 1 - \frac{230\ ns}{t_{SW}}$$

Where:

- t_{SW} = Switching period, equal to $1/f_{SW}$

It is not recommended to use the MIC2127A with an OFF time close to $t_{OFF(MIN)}$ during steady-state operation.

The adaptive on-time control scheme results in a constant switching frequency over the wide range of input voltage and load current. The actual ON time and resulting switching frequency varies with the different rising and falling times of the external MOSFETs. The minimum controllable ON time ($t_{ON(MIN)}$) results in a lower switching frequency than the target switching frequency in high V_{IN} to V_{OUT} ratio applications.

Equation 4-3 shows the output-to-input voltage ratio, below which the MIC2127A lowers the switching frequency in order to regulate the output to set value.

EQUATION 4-3:

$$\frac{V_{OUT}}{V_{IN}} \geq t_{ON(MIN)} \times f_{SW}$$

Where:

- V_{OUT} = Output voltage
- V_{IN} = Input voltage
- f_{SW} = Switching frequency
- $t_{ON(MIN)}$ = Minimum controllable ON time (80 ns typ.)

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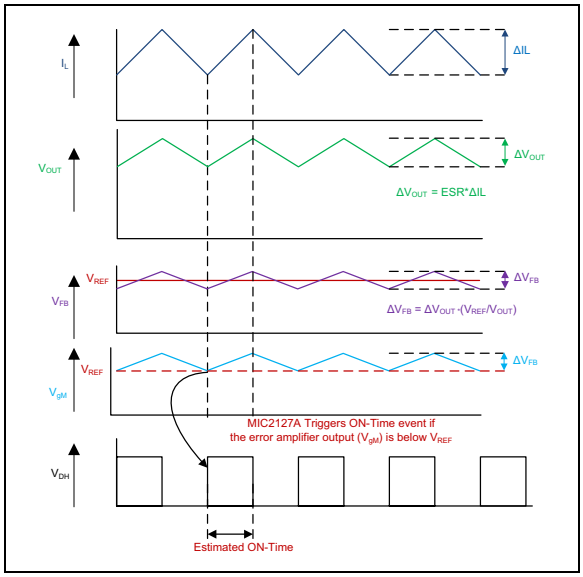


FIGURE 4-1: *MIC2127A Control Loop Timing.*

Figure 4-2 shows operation of the MIC2127A during load transient. The output voltage drops due to a sudden increase in load, which results in the error amplifier output (V_{gM}) falling below V_{REF}. This causes the comparator to trigger an on-time event. At the end of the ON time, a minimum OFF time $t_{OFF(MIN)}$ is generated to charge the bootstrap capacitor. The next ON time is triggered immediately after the $t_{OFF(MIN)}$ if the error amplifier output voltage (V_{gM}) is still below V_{REF} due to the low feedback voltage. This operation results in higher switching frequency during load transients. The switching frequency returns to the nominal set frequency once the output stabilizes at new load current level. The output recovery time is fast and the output voltage deviation is small in the MIC2127A converter due to the varying duty cycle and switching frequency.

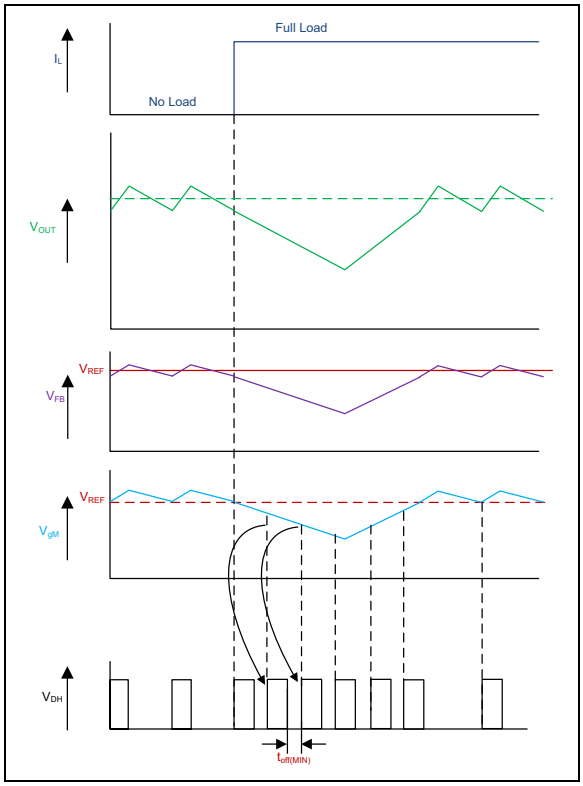


FIGURE 4-2: *MIC2127A Load Transient Response.*

Unlike true current-mode control, the MIC2127A uses the output voltage ripple to trigger an on-time event. In order to meet the stability requirements, the MIC2127A feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the internal error amplifier. The recommended feedback voltage ripple is approximately 20 mV-100 mV over the full input voltage range. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the internal error amplifier. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. For these applications, ripple injection is required to ensure proper operation. Refer to **Section 5.7 "Ripple Injection"** for details about the ripple injection technique.

4.2 Light Load Operating Mode (MODE)

MIC2127A features a MODE pin that allows the user to select either Continuous Conduction mode or Hyper Light Load (HLL) mode under light loads. HLL mode increases the system efficiency at light loads by reducing the switching frequency. Continuous Conduction mode keeps the switching frequency almost constant over the load current range.

Figure 4-3 shows the control loop timing in HLL mode. The MIC2127A has a zero crossing comparator (ZC Detection) that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON time. The zero crossing comparator triggers whenever the low-side MOSFET current goes negative and turns off the low-side MOSFET. The switching instant of the high-side MOSFET depends on the error amplifier output, which is same as the comparator inverting input (see the Functional Block Diagram). If the error amplifier output is higher than the comparator reference, then the MIC2127A enters into Sleep mode. During Sleep mode, both the high-side and low-side MOSFETs are kept off and the efficiency is optimized by shutting down all the nonessential circuits inside the MIC2127A. The load current is supplied by the output capacitor during Sleep mode. The control circuitry wakes up when the error amplifier output falls below the comparator reference and a t_{ON} pulse is triggered.

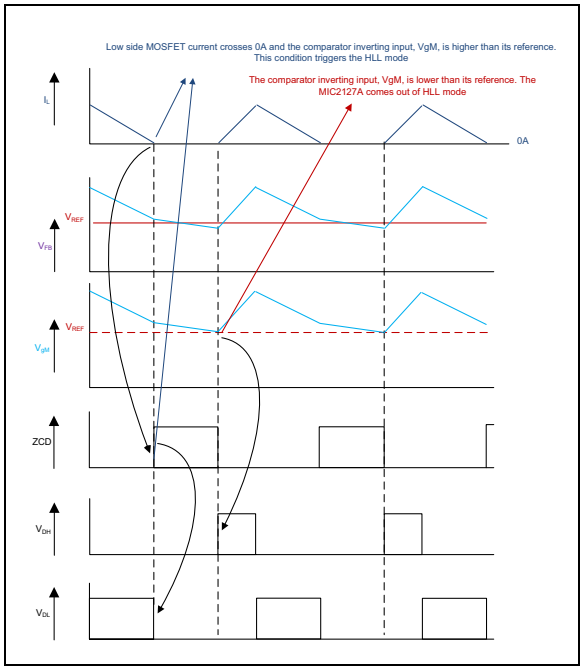


FIGURE 4-3: *MIC2127A Control Loop Timing (HLL Mode).*

The typical no-load supply current during HLL mode is only about 300 µA, allowing the MIC2127A to achieve high efficiency at light load operation.

4.3 Current Limit (I_{LIM})

The MIC2127A uses the low-side MOSFET $R_{DS(ON)}$ to sense inductor current. In each switching cycle of the MIC2127A converter, the inductor current is sensed by monitoring the voltage across the low-side MOSFET during the OFF period of the switching cycle, during which low-side MOSFET is ON. An internal current source of 100 µA generates a voltage across the external current limit, setting resistor R_{CL} as shown in Figure 4-4.

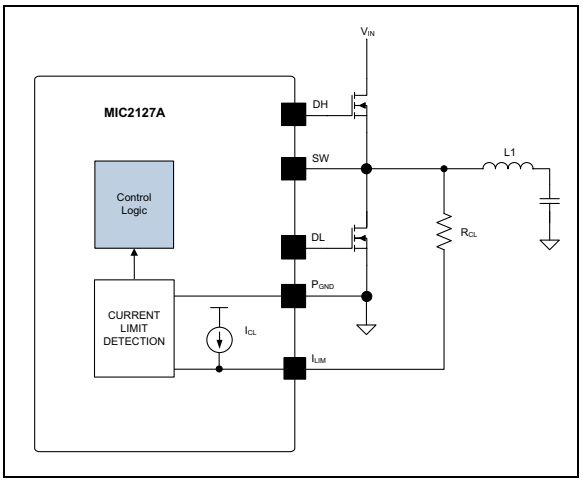


FIGURE 4-4: *MIC2127A Current Limiting Circuit.*

The I_{LIM} pin voltage (V_{ILIM}) is the difference of the voltage across the low-side MOSFET and the voltage across the resistor (V_{CL}). The sensed voltage V_{ILIM} is compared with the power ground (P_{GND}) after a blanking time of 150 ns.

If the absolute value of the voltage drop across the low-side MOSFET is greater than the absolute value of the voltage across the current setting resistor (V_{CL}), the MIC2127A triggers the current limit event. Consecutive eight-current limit events trigger the Hiccup mode. Once the controller enters into Hiccup mode, it initiates a soft-start sequence after a hiccup timeout of 4 ms (typical). Both the high-side and low-side MOSFETs are turned off during hiccup timeout. The hiccup sequence, including the soft start, reduces the stress on the switching FETs and protects the load and supply from severe short conditions.

The current limit can be programmed by using the following Equation 4-4.

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EQUATION 4-4:

$$R_{CL} = \frac{\left(I_{CLIM} + \frac{\Delta IL_{PP}}{2}\right) \times R_{DS(ON)} + V_{OFFSET}}{I_{CL}}$$

Where:

I_{CLIM}	=	Load current limit
$R_{DS\ (ON)}$	=	On-resistance of low-side power MOSFET
ΔIL_{PP}	=	Inductor peak-to-peak ripple current
V_{OFFSET}	=	Current-limit comparator offset (15 mV max.)
I_{CL}	=	Current-limit source current (100 µA typ)

Since MOSFET $R_{DS(ON)}$ varies from 30%-40% with temperature, it is recommended to consider the $R_{DS(ON)}$ variation while calculating R_{CL} in the above equation, to avoid false current limiting due to increased MOSFET junction temperature rise. Also connect the SW pin directly to the drain of the low-side MOSFET to accurately sense the MOSFETs $R_{DS(ON)}$.

To improve the current limit variation, the MIC2127A adjusts the internal source current of the current limit (I_{CL}) at a rate of 0.3 µA/°C when the MIC2127A junction temperature changes to compensate the $R_{DS(ON)}$ variation of external low-side MOSFET. The effectiveness of this method depends on the thermal gradient between the MIC2127A and the external low-side MOSFET. The lower the thermal gradient, the better the current limit variation.

A small capacitor (C_{CL}) can be connected from the I_{LIM} pin to P_{GND} to filter the switch node ringing during the OFF time, allowing a better current sensing. The time constant of R_{CL} and C_{CL} should be less than the minimum OFF time.

4.4 Negative Current Limit

The MIC2127A implements negative current limit by sensing the SW voltage when the low-side FET is ON. If the SW node voltage exceeds 48 mV typical, the device turns off the low-side FET for 500 ns. Negative current limit value is shown in Equation 4-5.

EQUATION 4-5:

$$I_{NLIM} = \frac{48mV}{R_{DS(ON)}}$$

Where:

I_{NLIM}	=	Negative current limit
$R_{DS\ (ON)}$	=	On-resistance of low-side power MOSFET

4.5 High-Side MOSFET Gate Drive (DH)

The MIC2127A's high-side drive circuit is designed to switch an N-Channel external MOSFET. The MIC2127A Functional Block diagram shows a bootstrap diode between the P_{VDD} and BST pins. This circuit supplies energy to the high-side drive circuit. A low ESR ceramic capacitor should be connected between BST and SW pins (refer to the Typical Application circuit).The capacitor between BST and SW pins, C_{BST}, is charged while the low-side MOSFET is on. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. A minimum of 0.1 µF low ESR ceramic capacitor is recommended between BST and SW pins. The required value of C_{BST} can be calculated using the following Equation 4-6:

EQUATION 4-6:

$$C_{BST} = \frac{Q_{G_HS}}{\Delta V_{BST}}$$

Where:

Q_{G_HS}	=	High-side MOSFET total gate charge
ΔV_{BST}	=	Drop across the C_{BST}, generally 50 mV to 100 mV

A small resistor in series with C_{BST} can be used to slow down the turn-on time of the high-side N-channel MOSFET.

4.6 Low-Side MOSFET Gate Drive (DL)

The MIC2127A's low-side drive circuit is designed to switch an N-Channel external MOSFET. The internal low-side MOSFET driver is powered by P_{VDD}. Connect a minimum of 4.7 µF low-ESR ceramic capacitor to supply the transient gate current of the external MOSFET.

4.7 Auxiliary Bootstrap LDO (EXTVDD)

The MIC2127A features an auxiliary bootstrap LDO that improves the system efficiency by supplying the MIC2127A internal circuit bias power and gate drivers from the converter output voltage. This LDO is enabled when the voltage on the EXTVDD pin is above 4.6V (typical) and, at the same time, the main LDO that operates from V_{IN} is disabled to reduce power consumption.

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5.0 APPLICATIONS INFORMATION

5.1 Setting the Switching Frequency

The MIC2127A is an adjustable-frequency, synchronous buck controller, featuring a unique adaptive on-time control architecture. The switching frequency can be adjusted between 270 kHz-800 kHz by changing the resistor divider network between V_{IN} and A_{GND} pins consisting of R_1 and R_2, as shown in Figure 5-1.

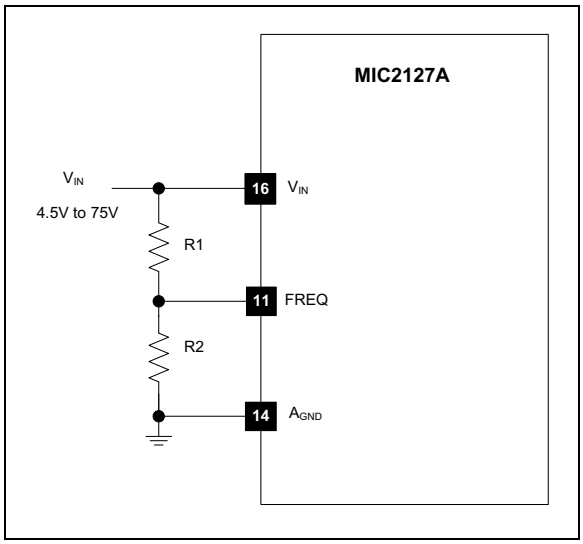


FIGURE 5-1: *Switching Frequency Adjustment.*

Equation 5-1 shows the estimated switching frequency.

EQUATION 5-1:

$$f_{SW_ADJ} = f_O \times \frac{R_2}{R_1 + R_2}$$

f_O is the switching frequency when R_1 is 100 kΩ and R_2 being open; f_O is typically 800 kHz. For more precise setting, it is recommended to use Figure 5-2.

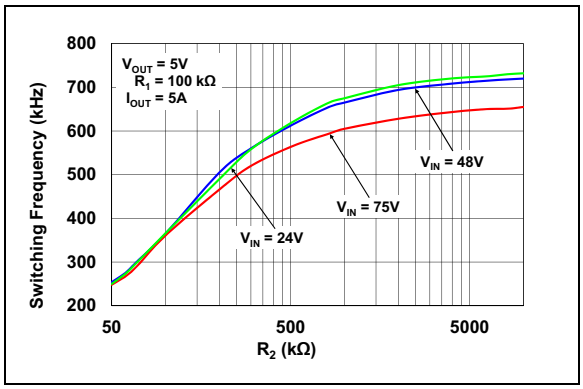


FIGURE 5-2: *Switching Frequency vs. R_2.*

5.2 Output Voltage Setting

The output voltage can be adjusted using a resistor divider from output to A_{GND} whose mid-point is connected to the FB pin, as shown the Figure 5-3.

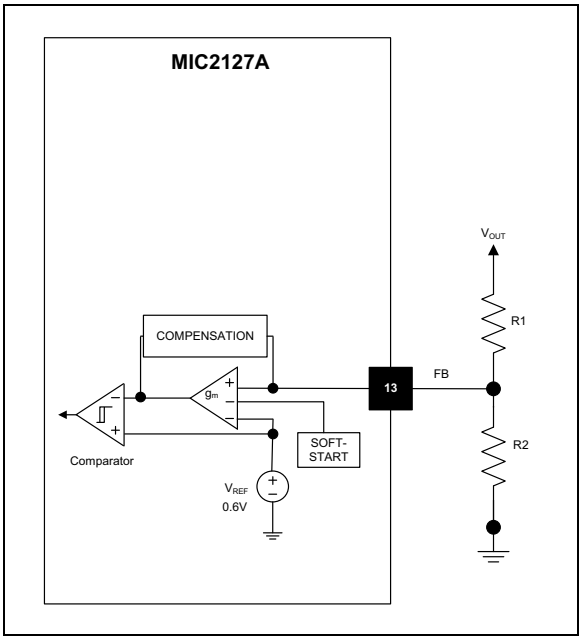


FIGURE 5-3: *Output Voltage Adjustment.*

The output voltage can be calculated using Equation 5-2.

EQUATION 5-2:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

Where:

V_{REF} = 0.6V

The maximum output voltage that can be programmed using the MIC2127A is limited to 30V, if not limited by the maximum duty cycle (see Equation 4-2).

A typical value of R_1 is less than 30 kΩ. If R_1 is too large, it may allow noise to be introduced into the voltage feedback loop. It also increases the offset between the set output voltage and actual output voltage because of the error amplifier bias current. If R_1 is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R_1 is selected, R_2 can be calculated using Equation 5-3.

EQUATION 5-3:

$$R_2 = \frac{R_1}{\frac{V_{OUT}}{V_{REF}} - 1}$$

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5.3 MOSFET Selection

Important parameters for MOSFET selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage rating for the high-side and low-side MOSFETs is essentially equal to the power stage input voltage V_{IN}. A safety factor of 30% should be added to the $V_{IN(MAX)}$ while selecting the voltage rating of the MOSFETs to account for voltage spikes due to circuit parasitic elements.

5.3.1 HIGH-SIDE MOSFET POWER LOSSES

The total power loss in the high-side MOSFET (P_{HSFET}) is the sum of the power losses because of conduction ($P_{CONDUCTION}$), switching (P_{SW}), reverse recovery charge of low-side MOSFET body diode (P_{Qrr}) and MOSFET's output capacitance discharge, as calculated in the Equation 5-4.

EQUATION 5-4:

$$P_{HSFET} = P_{CONDUCTION(HS)} + P_{SW(HS)} + P_{Qrr} + P_{COSS}$$

$$P_{CONDUCTION(HS)} = (I_{RMS(HS)})^2 \times R_{DS(ON_HS)}$$

$$P_{SW(HS)} = 0.5 \times V_{IN} \times I_{LOAD} \times (t_R + t_F) \times f_{SW}$$

$$P_{Qrr} = V_{IN} \times Q_{rr} \times f_{SW}$$

$$P_{COSS} = \frac{1}{2} \times (C_{OSS(HS)} + C_{OSS(HS)}) \times (V_{IN})^2 \times f_{SW}$$

Where:

$R_{DS(ON_HS)}$	=	On-resistance of the high-side MOSFET
V_{IN}	=	Operating input voltage
I_{LOAD}	=	Load current
f_{SW}	=	Operating switching frequency
Q_{rr}	=	Reverse recovery charge of low-side MOSFET body diode or of external diode across low-side MOSFET
$C_{OSS(HS)}$	=	Effective high-side MOSFET output capacitance
$C_{OSS(LS)}$	=	Effective low-side MOSFET output capacitance
$I_{RMS(HS)}$	=	RMS current of the high-side MOSFET which can be calculated using Equation 5-5.
t_R, t_F	=	The high-side MOSFET turn-on and turn-off transition times which can be approximated by Equation 5-7 and Equation 5-8

EQUATION 5-5:

$$I_{RMS(HS)} = I_{LOAD} \times \sqrt{D}$$

I_{LOAD} is the load current and D is the operating duty cycle, given by Equation 5-6.

EQUATION 5-6:

$$D = \frac{V_{OUT}}{V_{IN}}$$

EQUATION 5-7:

$$t_R = \frac{Q_{SW(HS)} \times [R_{DH(PULL_UP)} + R_{HS(GATE)}]}{V_{DD} - V_{TH}}$$

EQUATION 5-8:

$$t_F = \frac{Q_{SW(HS)} \times [R_{DH(PULL_DOWN)} + R_{HS(GATE)}]}{V_{TH}}$$

Where:

$R_{DH(PULL-UP)}$	=	High-side gate driver pull-up resistance
$R_{DH(PULL-DOWN)}$	=	High-side gate driver pull-down resistance
$R_{HS(GATE)}$	=	High-side MOSFET gate resistance
V_{TH}	=	Gate to Source threshold voltage of the high-side MOSFET
$Q_{SW(HS)}$	=	Switching gate charge of the high-side MOSFET which can be approximated by Equation 5-9.

EQUATION 5-9:

$$Q_{SW(HS)} = \frac{Q_{GS(HS)}}{2} + Q_{GD(HS)}$$

Where:

$Q_{GS(HS)}$	=	High-side MOSFET gate to source charge
$Q_{GD(HS)}$	=	High-side MOSFET gate to drain charge

5.3.2 LOW-SIDE MOSFET POWER LOSSES

The total power loss in the low-side MOSFET (P_{LSFET}) is the sum of the power losses because of conduction ($P_{CONDUCTION(LS)}$) and body diode conduction during the dead time (P_{DT}), as calculated in Equation 5-10.

EQUATION 5-10:

$$P_{LSFET} = P_{CONDUCTION(LS)} + P_{DT}$$

$$P_{CONDUCTION(LS)} = (I_{RMS(LS)})^2 \times R_{DS(ON_LS)}$$

$$P_{DT} = 2 \times V_F \times I_{LOAD} \times t_{DT} \times f_{SW}$$

Where:

$R_{DS(ON_LS)}$	=	On-resistance of the low-side MOSFET
V_F	=	Low-side MOSFET body diode forward voltage drop
t_{DT}	=	Dead time which is approximately 20 ns
f_{SW}	=	Switching Frequency
$I_{RMS(LS)}$	=	RMS current of the low-side MOSFET which can be calculated using Equation 5-11

EQUATION 5-11:

$$I_{RMS(LS)} = I_{LOAD} \times \sqrt{1 - D}$$

Where:

I_{LOAD}	= load current
D	= operating duty cycle

5.4 Inductor Selection

Inductance value, saturation and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current.

The lower the inductance value, the higher the peak-to-peak ripple current through the inductor, which increases the core losses in the inductor. Higher inductor ripple current also requires more output capacitance to smooth out the ripple current. The greater the inductance value, the lower the peak-to-peak ripple current, which results in a larger and more expensive inductor.

A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 30% of the maximum output current.

The inductance value is calculated by Equation 5-12.

EQUATION 5-12:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times 0.3 \times I_{FL}}$$

Where:

V_{IN}	=	Input voltage
f_{SW}	=	Switching frequency
I_{FL}	=	Full load current
V_{OUT}	=	Output voltage

For a selected Inductor, the peak-to-peak inductor current ripple can be calculated using Equation 5-13.

EQUATION 5-13:

$$\Delta I_{L_PP} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The peak inductor current is equal to the load current plus one half of the peak-to-peak inductor current ripple which is shown in Equation 5-14.

EQUATION 5-14:

$$I_{L_PK} = I_{LOAD} + \frac{\Delta I_{L_PP}}{2}$$

The RMS and saturation current ratings of the selected inductor should be at least equal to the RMS current and saturation current calculated in Equation 5-15 and Equation 5-16.

EQUATION 5-15:

$$I_{L_RMS} = \sqrt{(I_{LOAD(MAX)})^2 + \frac{(\Delta I_{L_PP})^2}{12}}$$

Where:

$I_{LOAD(MAX)}$	=	Maximum load current

EQUATION 5-16:

$$I_{L_SAT} = \frac{(R_{CL} \times I_{CL}) + 15mV}{R_{DS(ON)}}$$

Where:

R_{CL}	=	Current limit resistor
I_{CL}	=	Current-Limit Source Current (100 µA typical)
$R_{DS\ (ON)}$	=	On-resistance of low-side power MOSFET

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Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. Use of ferrite materials is recommended in the higher switching frequency applications. Lower-cost iron powder cores may be used, but the increase in core loss reduces the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized, although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetic's vendor.

The amount of copper loss in the inductor is calculated by Equation 5-17.

EQUATION 5-17:

$$P_{INDUCTOR(CU)} = (I_{L_RMS})^2 \times R_{DCR}$$

5.5 Output Capacitor Selection

The main parameters for selecting the output capacitor are capacitance value, voltage rating and RMS current rating. The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Recommended capacitor types are ceramic, tantalum, low-ESR aluminum electrolytic, OS-CON and POSCAP. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR can be calculated using Equation 5-18.

EQUATION 5-18:

$$ESR \leq \frac{\Delta V_{OUT_PP}}{\Delta I_{L_PP}}$$

Where:

ΔV_{OUT_PP}	=	Peak-to-peak output voltage ripple
ΔI_{L_PP}	=	Peak-to-peak inductor current ripple

The required output capacitance to meet steady state output voltage ripple can be calculated using Equation 5-19.

EQUATION 5-19:

$$C_{OUT} = \frac{\Delta I_{L_PP}}{8 \times f_{SW} \times \Delta V_{OUT_PP}}$$

Where:

C_{OUT}	=	Output capacitance value
f_{SW}	=	Switching frequency
ΔV_{OUT_PP}	=	Steady state output voltage ripple

As described in **Section 4.1 "Theory of Operation"**, the MIC2127A requires at least 20 mV peak-to-peak ripple at the FB pin to ensure that the g_M amplifier and the comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitor's value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection circuit should be used to provide enough feedback-voltage ripple. Refer to the **Section 5.7 "Ripple Injection"** for details.

The voltage rating of the capacitor should be twice the output voltage for tantalum and 20% greater for aluminum electrolytic, ceramic or OS-CON. The output capacitor RMS current is calculated in Equation 5-20.

EQUATION 5-20:

$$I_{C_OUT(RMS)} = \frac{\Delta I_{L_PP}}{\sqrt{12}}$$

The power dissipated in the output capacitor is shown in Equation 5-21.

EQUATION 5-21:

$$P_{DIS(C_OUT)} = (I_{C_OUT(RMS)})^2 \times ESR_{C_OUT}$$

5.6 Input Capacitor Selection

The input capacitor reduces peak current drawn from the power supply and reduces noise and voltage ripple on the input. The input voltage ripple depends on the input capacitance and ESR. The input capacitance and ESR values can be calculated using Equation 5-22.

EQUATION 5-22:

$$C_{IN} = \frac{I_{LOAD} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN_C}}$$

$$ESR_{C_IN} = \frac{\Delta V_{IN_ESR}}{I_{L_PK}}$$

Where:

I_{LOAD}	=	Load Current
I_{L_PK}	=	Peak Inductor Current
ΔV_{INC}	=	Input ripple due to capacitance
ΔV_{INESR}	=	Input ripple due to input capacitor ESR
η	=	Power conversion efficiency

The input capacitor should be rated for ripple current rating and voltage rating. The RMS value of input capacitor current is determined at the maximum output current. The RMS current rating of the input capacitor should be greater than or equal to the input capacitor RMS current calculated using Equation 5-23.

EQUATION 5-23:

$$I_{C_IN(RMS)} = I_{LOAD(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is calculated using Equation 5-24.

EQUATION 5-24:

$$P_{DISS(C_IN)} = (I_{C_IN(RMS)})^2 \times ESR_{C_IN}$$

5.7 Ripple Injection

The minimum recommended ripple at the FB pin for proper operation of the MIC2127A error amplifier and comparator is 20 mV. However, the output voltage ripple is generally designed as 1%-2% of the output voltage. For low output voltages, such as a 1V, the output voltage ripple is only 10 mV-20 mV, and the feedback voltage ripple is less than 20 mV. If the feedback voltage ripple is so small that the g_M amplifier and comparator cannot sense it, then the MIC2127A loses control and the output voltage is not regulated. In order to have sufficient V_{FB} ripple, the ripple injection method should be applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

1. Enough ripple at the feedback due to the large ESR of the output capacitor (Figure 5-4). The converter is stable without any additional ripple injection at the FB node. The feedback voltage ripple is given by Equation 5-25.

EQUATION 5-25:

$$\Delta V_{FB(PP)} = \frac{R_2}{R_2 + R_1} \times ESR \times \Delta I_{L_PP}$$

ΔI_{L_PP} is the peak-to-peak value of the inductor current ripple.

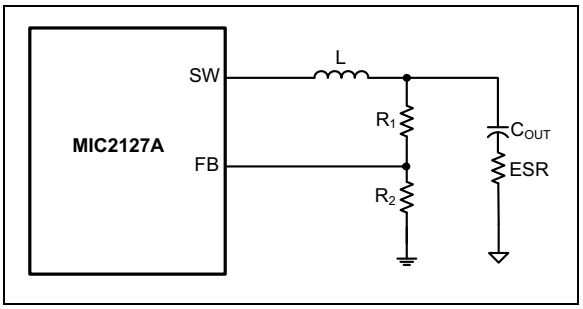


FIGURE 5-4: *Enough Ripple at FB.*

2. Inadequate ripple at the feedback voltage due to the small ESR of the output capacitor.

The output voltage ripple can be fed into the FB pin through a feed forward capacitor, C_{FF} in this case, as shown in Figure 5-5. The typical C_{FF} value is between 1 nF-100 nF. With the feed forward capacitor, the feedback voltage ripple is very close to the output voltage ripple, which is shown in Equation 5-26.

EQUATION 5-26:

$$\Delta V_{FB(PP)} = ESR \times \Delta I_{L_PP}$$

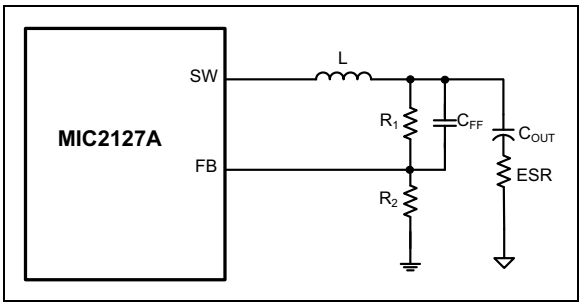


FIGURE 5-5: *Inadequate Ripple at FB.*

3. Virtually no ripple at the FB pin voltage due to the very-low ESR of the output capacitors.

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In this case, additional ripple can be injected into the FB pin from the switching node SW, via a resistor R_{INJ} and a capacitor C_{INJ}, as shown in Figure 5-6.

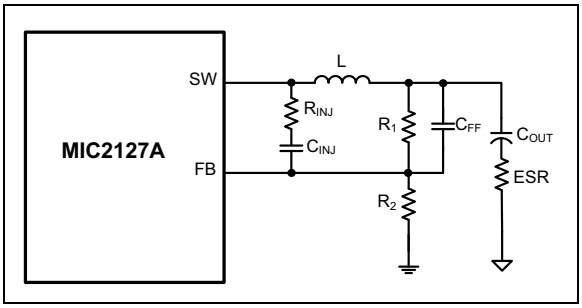


FIGURE 5-6: *Invisible Ripple at FB.*

The injected ripple at the FB pin in this case is given by the Equation 5-27.

EQUATION 5-27:

$$\Delta V_{FB(PP)} = \frac{V_{OUT} \times (1 - D)}{C_{FF} \times R_{INJ} \times f_{SW}}$$

In Equation 5-27, it is assumed that the time constant associated with the C_{FF} meets the criterion shown in Equation 5-28.

EQUATION 5-28:

$$\tau \geq T_{SW}$$

$$\tau = C_{FF} \times (R_1 \| R_2 \| R_{INJ})$$

The process of sizing the ripple injection resistor and capacitors is:

1. Select C_{INJ} in the range of 47 nF-100 nF, which can be considered as short for a wide range of the frequencies.
2. Select C_{FF} in the range of 0.47 nF-10 nF, if R_1 and R_2 are in kΩ range.
3. Select R_{INJ} according to Equation 5-29.

EQUATION 5-29:

$$R_{INJ} = \frac{V_{OUT} \times (1 - D)}{C_{FF} \times f_{SW} \times \Delta V_{FB(PP)}}$$

Where:

V_{OUT}	=	Output voltage
D	=	Duty cycle
f_{SW}	=	Switching frequency
$\Delta V_{FB}(pp)$	=	Feedback Ripple

Once all the ripple injection component values are calculated, ensure that the criterion shown in Equation 5-28 is met.

5.8 Power Dissipation in MIC2127A

The MIC2127A features two Low Dropout Regulators (LDOs) to supply power at the P_{VDD} pin from either V_{IN} or EXTVDD depending on the voltage at the EXTVDD pin. P_{VDD} powers MOSFET drivers and V_{DD} pin, which is recommended to connect to P_{VDD} through a low pass filter, powers the internal circuitry. In the applications where the output voltage is 5V and above (up to 14V), it is recommended to connect EXTVDD to the output to reduce the power dissipation in the MIC2127A, to reduce the MIC2127A junction temperature and to improve the system efficiency.

The power dissipation in the MIC2127A depends on the internal LDO being in use, on the gate charge of the external MOSFETs and on the switching frequency. The power dissipation and the junction temperature of the MIC2127A can be estimated using Equations 5-30, 5-31 and 5-32.

Power dissipation in the MIC2127A when EXTVDD is not used.

EQUATION 5-30:

$$P_{IC} = V_{IN} \times (I_{SW} + I_Q)$$

Power dissipation in the MIC2127A when EXTVDD is used.

EQUATION 5-31:

$$P_{IC} = V_{EXTVDD} \times (I_{SW} + I_Q)$$

$$I_{SW} = Q_G \times f_{SW}$$

$$Q_G = Q_{G_HS} + Q_{G_LS}$$

Where:

I_{SW}	=	Switching current into the V_{IN} pin
I_Q	=	Quiescent current
Q_G	=	Total gate charge of the external MOSFETs which is sum of the gate charge of high-side MOSFET (Q_{G_HS}) and the low-side MOSFET (Q_{G_LS}) at 5V gate to source voltage. Gate charge information can be obtained from the MOSFETs datasheet.
V_{EXTVDD}	=	Voltage at the EXTVDD pin ($4.6 \leq V_{EXTVDD} \leq 14$ V typ.)

The junction temperature of the MIC2127A can be estimated using Equation 5-32.

EQUATION 5-32:

$$T_J = (P_{IC} \times \theta_{JA}) + T_A$$

Where:

T_J	=	Junction temperature
P_{IC}	=	Power dissipation
θ_{JA}	=	Junction Ambient Thermal resistance (50.8°C/W)

The maximum recommended operating junction temperature for the MIC2127A is +125°C.

Using the output voltage of the same switching regulator, when it is between 4.6V (typ.) to 14V, as the voltage at the EXTVDD pin significantly reduces the power dissipation inside the MIC2127A. This reduces the junction temperature rise as illustrated in Equation 5-34.

For the typical case of V_{VIN} = 48V, V_{OUT} = 5V, maximum ambient temperature of +85°C and 10 mA of I_{SW}, the MIC2127A junction temperature when the EXTVDD is not used is given by Equation 5-33.

EQUATION 5-33:

$$P_{IC} = 48V \times (10\,mA + 1.5mA)$$
$$P_{IC} = 0.552W$$
$$T_J = (0.552W \times 50.8℃/W) + 85℃$$
$$T_J = 113℃$$

When the 5V output is used as the input to the EXTVDD pin, the MIC2127A junction temperature reduces from +113°C to +88°C, as calculated in Equation 5-34.

EQUATION 5-34:

$$P_{IC} = 5V \times (10\,mA + 1.5\,mA)$$
$$P_{IC} = 0.058W$$
$$T_J = (0.058W \times 50.8\,℃/W) + 85\,℃$$
$$T_J = 88\,℃$$

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6.0 PCB LAYOUT GUIDELINES

PCB layout is critical to achieve reliable, stable and efficient performance. The following guidelines should be followed to ensure proper operation of the MIC2127A converter.

6.1 IC

- The ceramic bypass capacitors, which are connected to the V_{DD} and P_{VDD} pins, must be located right at the IC. Use wide traces to connect to the V_{DD}, P_{VDD} and A_{GND}, and P_{GND} pins respectively.
- The signal ground pin (A_{GND}) must be connected directly to the ground planes.
- Place the IC close to the point-of-load (POL).
- Signal and power grounds should be kept separate and connected at only one location.

6.2 Input Capacitor

- Place the input ceramic capacitors as closely as possible to the MOSFETs.
- Place several vias to the ground plane closely to the input capacitor ground terminal.

6.3 Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- The SW pin should be connected directly to the drain of the low-side MOSFET to accurately sense the voltage across the low-side MOSFET.

6.4 Output Capacitor

- Use a copper plane to connect the output capacitor ground terminal to the input capacitor ground terminal.
- The feedback trace should be separate from the power trace and connected as closely as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

6.5 MOSFETs

- MOSFET gate drive traces must be short and wide. The ground plane should be the connection between the MOSFET source and P_{GND}.
- Chose a low-side MOSFET with a high CGS/CGD ratio and a low internal gate resistance to minimize the effect of d_V/d_t inducted turn-on.
- Use a 4.5V V_{GS} rated MOSFET. Its higher gate threshold voltage is more immune to glitches than a 2.5V or 3.3V rated MOSFET.

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

16-Pin QFN (3 x 3 mm)



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

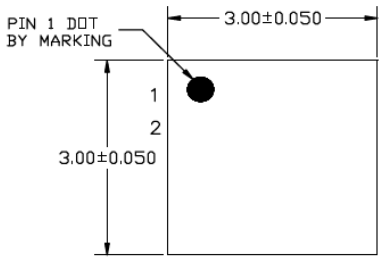
Underbar (_) and/or Overbar (¯) symbol may not be to scale.

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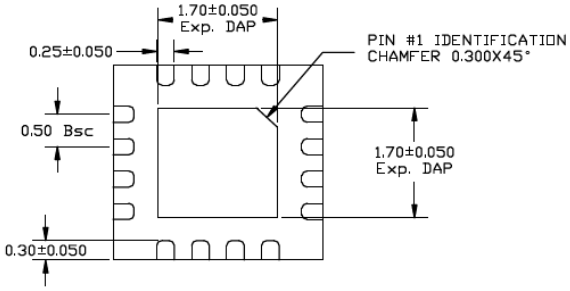
TITLE

16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

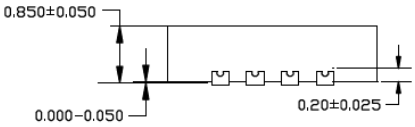
DRAWING #	QFN33-16LD-PL-3	UNIT	MM
Lead Frame	NiPdAu	Lead Finish	NiPdAu



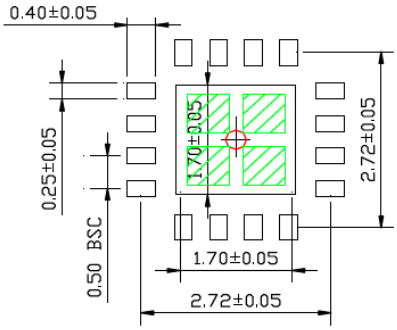
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60mm IN SIZE, 0.20mm SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

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APPENDIX A: REVISION HISTORY

Revision B (December 2016)

- Minor editorial corrections.
- Updated Product Identification System page.

Revision A (December 2016)

- Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XX
Device	Temperature	Package Code	Media Type

Device:	MIC2127A: 75V, Synchronous Buck Controller Featuring Adaptive On-Time Control
Temperature:	Y = Industrial Temperature Grade (-40°C to +125°C)
Package:	ML = 16 Lead, 3x3 mm VQFN
Media Type:	TR = 5000/reel T5 = 500/reel

Examples:

a) MIC2127AYML-TR: 75V, Synchronous Buck Controller Featuring Adaptive On-Time Control, –40°C to +125°C junction temperature range, 16-LD VQFN package, 5000/reel

b) MIC2127AYML-T5: 75V, Synchronous Buck Controller Featuring Adaptive On-Time Control, –40°C to +125°C junction temperature range, 16-LD VQFN package, 500/reel

NOTES:

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