Precision, Unity-Gain Differential Amplifier

AMP03

FEATURES

High CMRR: 100 dB Typ
Low Nonlinearity: 0.001% Max
Low Distortion: 0.001% Typ
Wide Bandwidth: 3 MHz Typ
Fast Slew Rate: 9.5 V/μs Typ
Fast Settling (0.01%): 1 μs Typ
Low Cost

APPLICATIONS

Summing Amplifiers
Instrumentation Amplifiers
Balanced Line Receivers
Current-Voltage Conversion
Absolute Value Amplifier
4 to 20 mA Current Transmitter
Precision Voltage Reference Applications
Lower Cost and Higher Speed Version of INA105

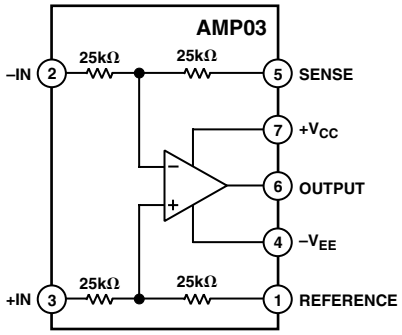
GENERAL DESCRIPTION

The AMP03 is a monolithic unity-gain, high speed differential amplifier. Incorporating a matched thin film resistor network, the AMP03 features stable operation over temperature without requiring expensive external matched components. The AMP03 is a basic analog building block for differential amplifier and instrumentation applications.

The differential amplifier topology of the AMP03 both amplifies the difference between two signals and provides extremely high rejection of the common-mode input voltage. By providing common-mode rejection (CMR) of 100 dB typical, the AMP03 solves common problems encountered in instrumentation design. As an example, the AMP03 is ideal for performing either addition or subtraction of two signals without using expensive externally matched precision resistors. The large common-mode rejection is made possible by matching the internal resistors to better than 0.002% and maintaining a thermally symmetric layout. Additionally, due to high CMR over frequency, the AMP03 is an ideal general amplifier for buffering signals in a noisy environment into data acquisition systems.

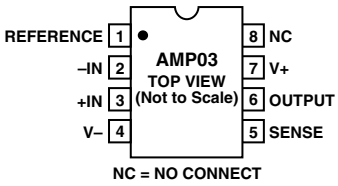
The AMP03 is a higher speed alternative to the INA105. Featuring slew rates of 9.5 V/μs and a bandwidth of 3 MHz, the AMP03 offers superior performance to the INA105 for high speed current sources, absolute value amplifiers, and summing amplifiers.

FUNCTIONAL BLOCK DIAGRAM

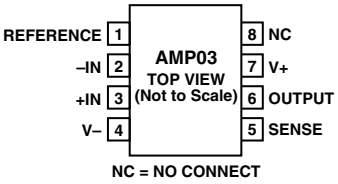


PIN CONNECTIONS

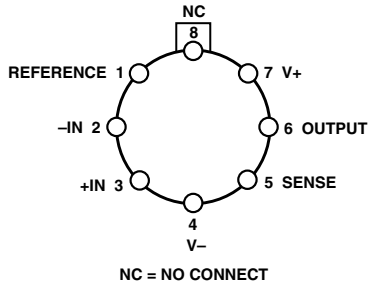
8-Lead PDIP
(P Suffix)



8-Lead SOIC
(S Suffix)



Header
(J Suffix)



REV. F

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AMP03–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	AMP03F			AMP03B			AMP03G			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Offset Voltage	V_{OS}	V_{CM} = 0 V	–400	+10	+400	–700	+20	+700	–750	+25	+750	µV
Gain Error		No Load, V_{IN} = ±10 V, R_S = 0 Ω		0.00004	0.008		0.00004	0.008		0.001	0.008	%
Input Voltage Range	IVR	(Note 1)	±20			±20			±20			V
Common-Mode Rejection	CMR	V_{CM} = ±10 V	85	100		80	95		80	95		dB
Power Supply Rejection Ratio	PSRR	V_S = ±6 V to ±18 V		0.6	10		0.6	10		0.7	10	µV/V
Output Swing	V_O	R_L = 2 kΩ	±12	±13.7		±12	±13.7		±12	±13.7		V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	+45/–15			+45/–15			+45/–15			mA
Small-Signal Bandwidth (–3 dB)	BW	R_L = 2 kΩ		3			3			3		MHz
Slew Rate	SR	R_L = 2 kΩ	6	9.5		6	9.5		6	9.5		V/µs
Capacitive Load Drive Capability	C_L	No Oscillation		300			300			300		pF
Supply Current	I_{SY}	No Load		2.5	3.5		2.5	3.5		2.5	3.5	mA

NOTES
[1]Input voltage range guaranteed by CMR test.
Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, –55°C ≤ T_A ≤ +125°C for B Grade)

Parameter	Symbol	Conditions	AMP03B			Unit
			Min	Typ	Max	
Offset Voltage	V_{OS}	V_{CM} = 0 V	–1500	+150	+1500	µV
Gain Error		No Load, V_{IN} = ±10 V, R_S = 0 Ω		0.0014	0.02	%
Input Voltage Range	IVR		±20			V
Common-Mode Rejection	CMR	V_{CM} = ±10 V	75	95		dB
Power Supply Rejection Ratio	PSRR	V_S = ±6 V to ±18 V		0.7	20	µV/V
Output Swing	V_O	R_L = 2 kΩ	±12	±13.7		V
Slew Rate	SR	R_L = 2 kΩ		9.5		V/µs
Supply Current	I_{SY}	No Load		3.0	4.0	mA

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, –40°C ≤ T_A ≤ +85°C for F and G Grades)

Parameter	Symbol	Conditions	AMP03F			AMP03G			Unit
			Min	Typ	Max	Min	Typ	Max	
Offset Voltage	V_{OS}	V_{CM} = 0 V	–1000	+100	+1000	–2000	+200	+2000	µV
Gain Error		No Load, V_{IN} = ±10 V, R_S = 0 Ω		0.0008	0.015		0.002	0.02	%
Input Voltage Range	IVR		±20			±20			V
Common-Mode Rejection	CMR	V_{CM} = ±10 V	80	95		75	90		dB
Power Supply Rejection Ratio	PSRR	V_S = ±6 V to ±18 V		0.7	15		1.0	15	µV/V
Output Swing	V_O	R_L = 2 kΩ	±12	±13.7		±12	±13.7		V
Slew Rate	SR	R_L = 2 kΩ		9.5			9.5		V/µs
Supply Current	I_{SY}	No Load		2.6	4.0		2.6	4.0	mA

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = ±15 V, T_A = 25°C, unless otherwise noted.)*

Parameter	Symbol	Conditions	AMP03GBC Limit	Unit
Offset Voltage	V_{OS}	V_S = ±18 V	0.5	mV max
Gain Error		No Load, V_{IN} = ±10 V, R_S = 0 Ω	0.008	% max
Input Voltage Range	IVR		±10	V min
Common-Mode Rejection	CMR	V_{CM} = ±10 V	80	dB min
Power Supply Rejection Ratio	PSRR	V_S = ±6 V to ±18 V	8	µV/V max
Output Swing	V_O	R_L = 2 kΩ	±12	V max
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	+45/–15	mA min
Supply Current	I_{SY}	No Load	3.5	mA max

*Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage[2] . . . . . Supply Voltage
Output Short-Circuit Duration . . . . . Continuous
Storage Temperature Range
P, J Package . . . . . –65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . 300°C
Junction Temperature . . . . . 150°C
Operating Temperature Range
AMP03B . . . . . –55°C to +125°C
AMP03F, AMP03G . . . . . –40°C to +85°C

Package Type	θ_{JA}[3]	θ_{JC}	Unit
Header (J)	150	18	°C/W
8-Lead PDIP (P)	103	43	°C/W
8-Lead SOIC (S)	155	40	°C/W

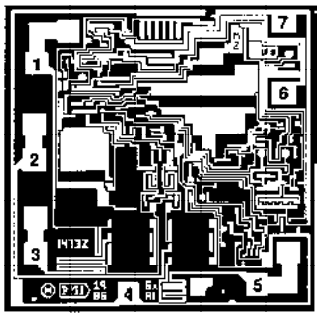
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for header and PDIP packages and for device soldered to printed circuit board for SOIC package.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AMP03GP	–40°C to +85°C	8-Lead PDIP	P-8
AMP03BJ	–40°C to +85°C	Header	H-08B
AMP03FJ	–40°C to +85°C	Header	H-08B
AMP03BJ/883C	–55°C to +125°C	Header	H-08B
AMP03GS	–40°C to +85°C	8-Lead SOIC	S-8
AMP03GS-REEL	–40°C to +85°C	8-Lead SOIC	S-8
5962-9563901MGA	–55°C to +125°C	Header	H-08B
AMP03GBC		Die	

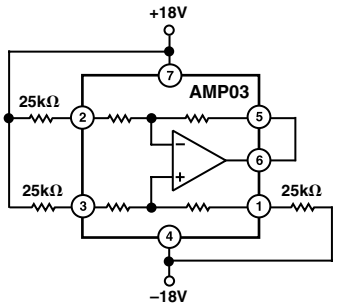
NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in PDIP and header packages.
[2]Consult factory for /883 data sheet.

DICE CHARACTERISTICS

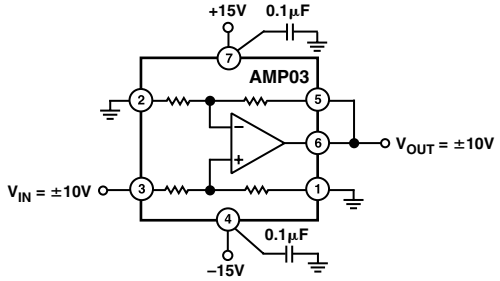


DIE SIZE 0.076 inch × 0.076 inch, 5,776 sq. mm
(1.93 mm × 1.93 mm, 3.73 sq. mm)

BURN-IN CIRCUIT



SLEW RATE TEST CIRCUIT

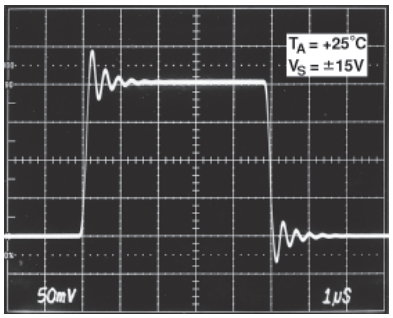


CAUTION

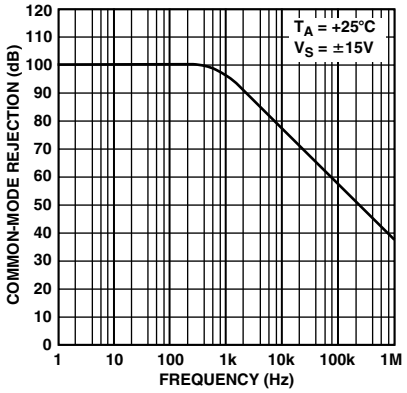
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AMP03 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



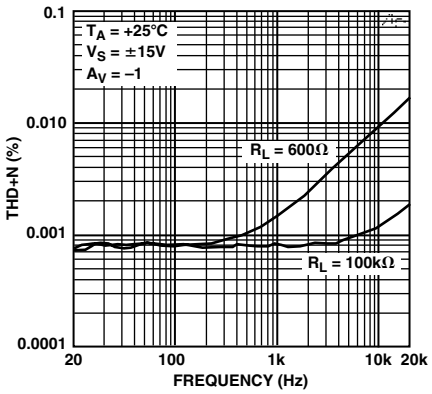
AMP03–Typical Performance Characteristics



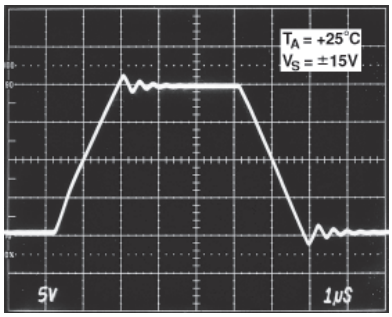
TPC 1. Small Signal Transient Response



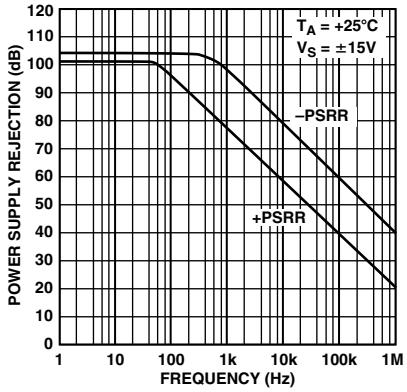
TPC 2. Common-Mode Rejection vs. Frequency



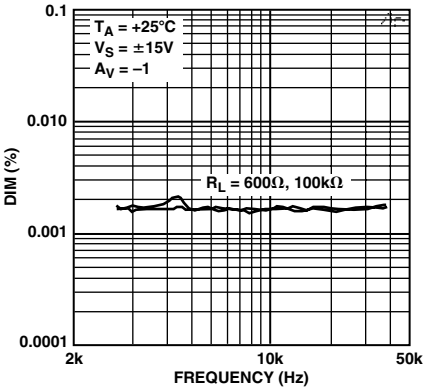
TPC 3. Total Harmonic Distortion vs. Frequency



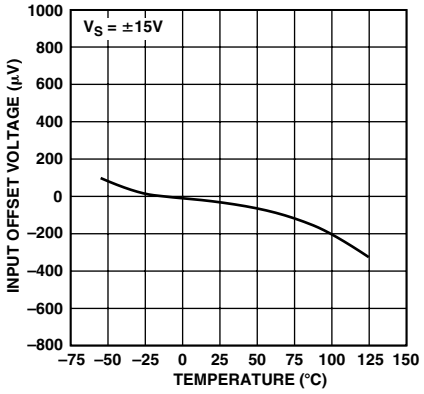
TPC 4. Large Signal Transient Response



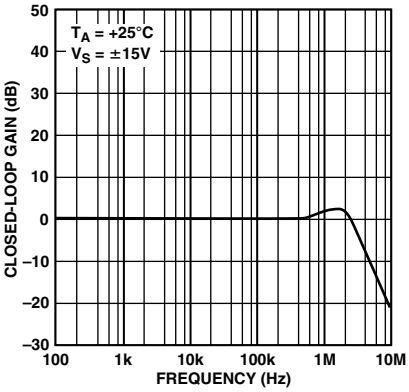
TPC 5. Power Supply Rejection vs. Frequency



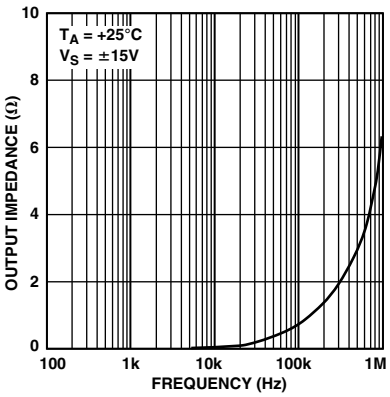
TPC 6. Dynamic Intermodulation Distortion vs. Frequency



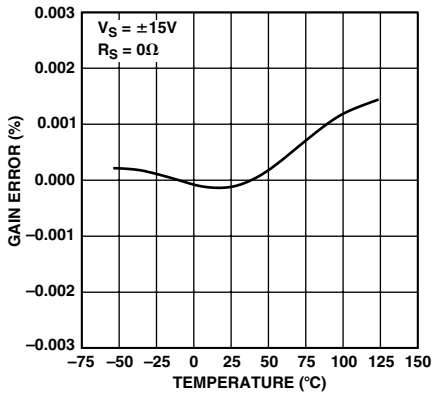
TPC 7. Input Offset Voltage vs. Temperature



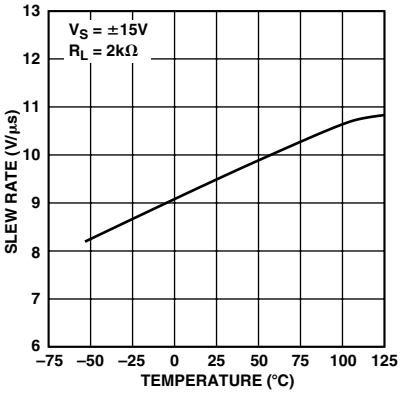
TPC 8. Closed-Loop Gain vs. Frequency



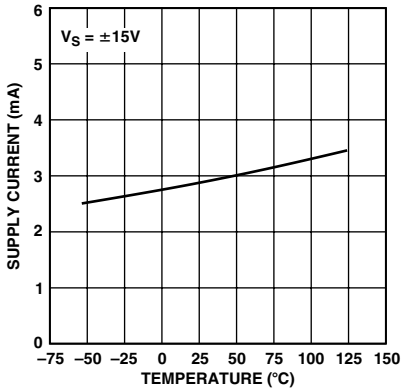
TPC 9. Closed-Loop Output Impedance vs. Frequency



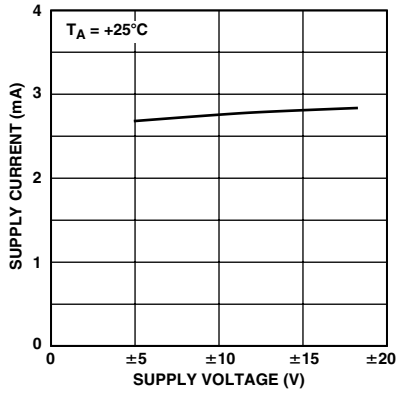
TPC 10. Gain Error vs. Temperature



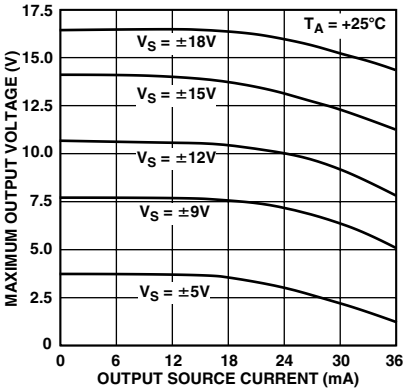
TPC 11. Slew Rate vs. Temperature



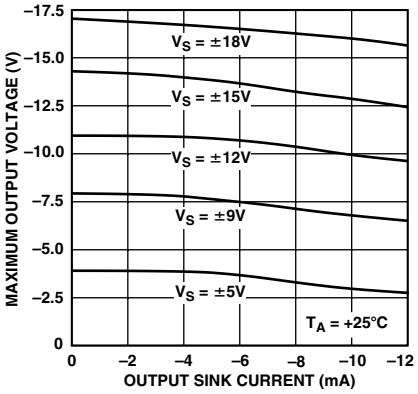
TPC 12. Supply Current vs. Temperature



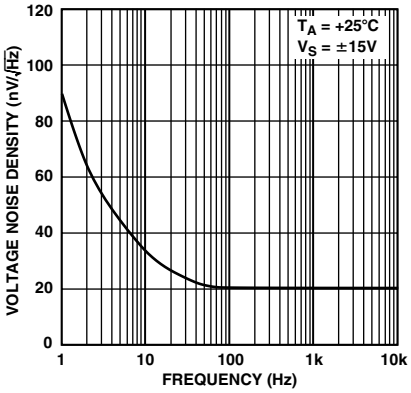
TPC 13. Supply Current vs. Supply Voltage



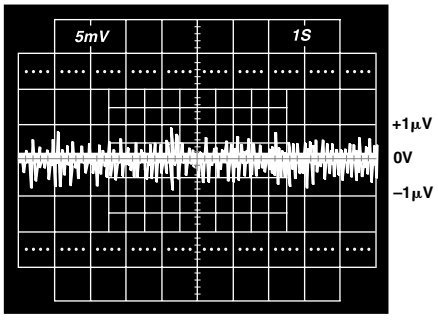
TPC 14. Maximum Output Voltage vs. Output Current (Source)



TPC 15. Maximum Output Voltage vs. Output Current (Sink)

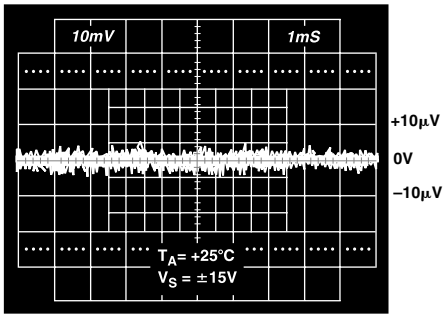


TPC 16. Voltage Noise Density vs. Frequency



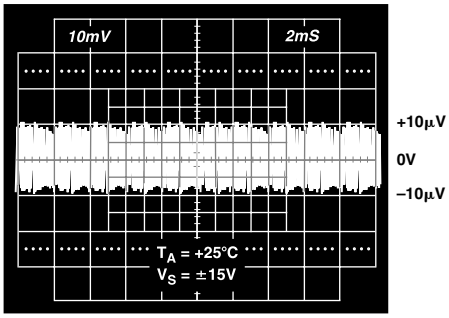
0.1 TO 10Hz PEAK-TO-PEAK NOISE

TPC 17. Low Frequency Voltage Noise



NOTE: EXTERNAL AMPLIFIER GAIN = 1000; THEREFORE, VERTICAL SCALE = 10µV/DIV.

TPC 18. Voltage Noise from 0 kHz to 1 kHz



NOTE: EXTERNAL AMPLIFIER GAIN = 1000; THEREFORE, VERTICAL SCALE = 10µV/DIV.

TPC 19. Voltage Noise from 0 kHz to 10 kHz

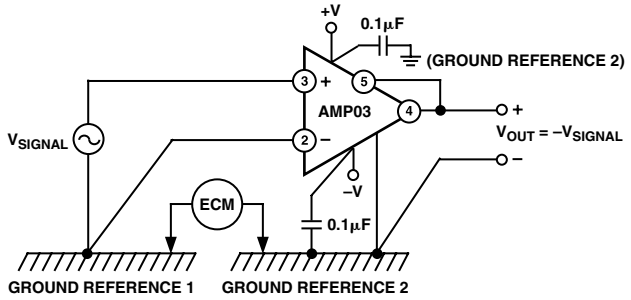


Figure 1. AMP03 Serves to Reject Common-Mode Voltages in Instrumentation Systems. Common-Mode Voltages Occur Due to Ground Current Returns. V_{SIGNAL} and E_{CM} Must Be within the Common-Mode Range of AMP03.

APPLICATIONS INFORMATION

The AMP03 represents a versatile analog building block. In order to capitalize on the fast settling time, high slew rate, and high CMR, proper decoupling and grounding techniques must be employed. Figure 1 illustrates the use of 0.1 μF decoupling capacitors and proper ground connections.

MAINTAINING COMMON-MODE REJECTION

In order to achieve the full common-mode rejection capability of the AMP03, the source impedance must be carefully controlled. Slight imbalances of the source resistance will result in a degradation of dc CMR—even a 5 Ω imbalance will degrade CMR by 20 dB. Also, the matching of the reactive source impedance must be matched in order to preserve the CMRR over frequency.

APPLICATION CIRCUITS

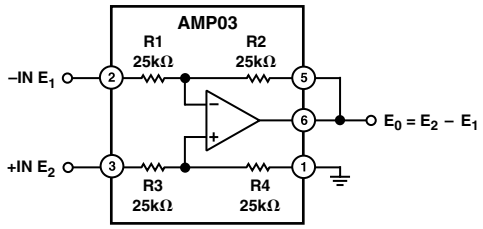


Figure 2. Precision Difference Amplifier. Rejects Common-Mode Signal = $(E_1 + E_2)/2$ by 100 dB

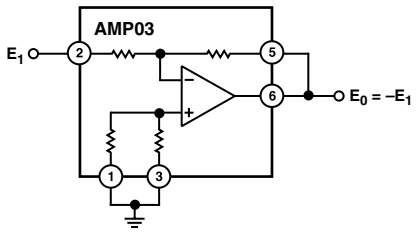


Figure 3. Precision Unity-Gain Inverting Amplifier

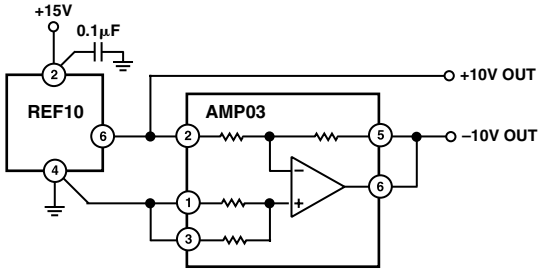


Figure 4. ±10 V Precision Voltage Reference

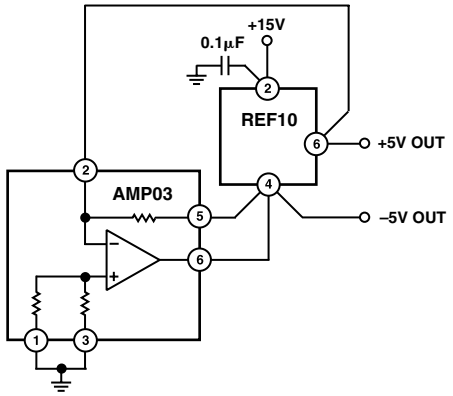


Figure 5. ±5 V Precision Voltage Reference

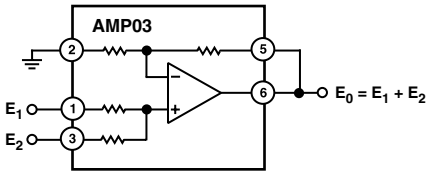


Figure 6. Precision Summing Amplifier

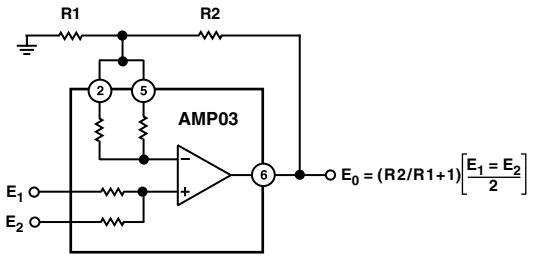


Figure 7. Precision Summing Amplifier with Gain

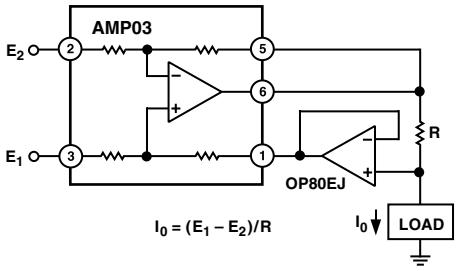


Figure 8. Differential Input Voltage-to-Current Converter for Low I_{OUT}. OP80EJ maintains 250 fA max input current, allowing I_O to be less than 1 pA.

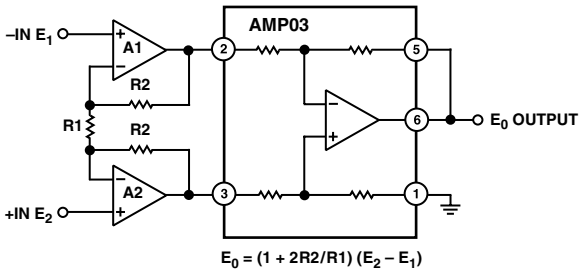


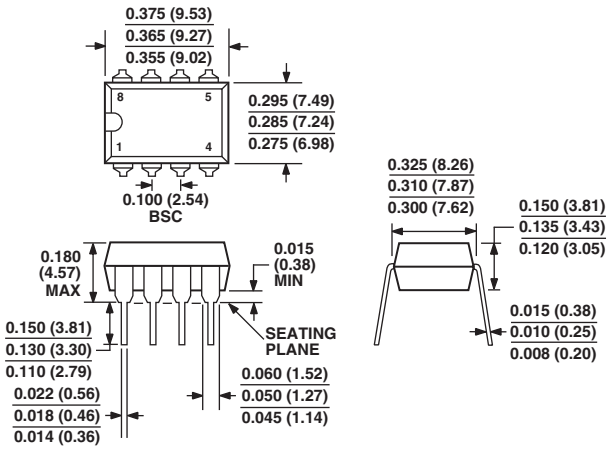
Figure 9. Suitable Instrumentation Amplifier Requirements Can Be Addressed by Using an Input Stage Consisting of A1, A2, R1, and R2. The following matrix suggests a suitable amplifier.

System Design Requirement	**Suggested Op Amp For A1 and A2**
Source Impedance Low, Need Low Voltage Noise Performance	OP27, OP37 OP227 (Dual Matched) OP270 (Dual) OP271 OP470 OP471
Source Impedance High ($R_S \geq 15$ kΩ). Need Low Current Noise	OP80 OP41 OP43 OP249 OP97
Require Ultrahigh Input Impedance	OP80 OP97 OP41 OP43
Need Wider Bandwidth and High Speed	OP42 OP43 OP249

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]
[P Suffix]
(N-8)

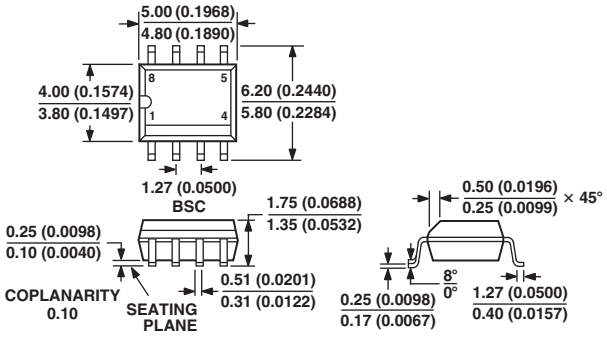
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Small Outline Package [SOIC]
[S Suffix]
(R-8)

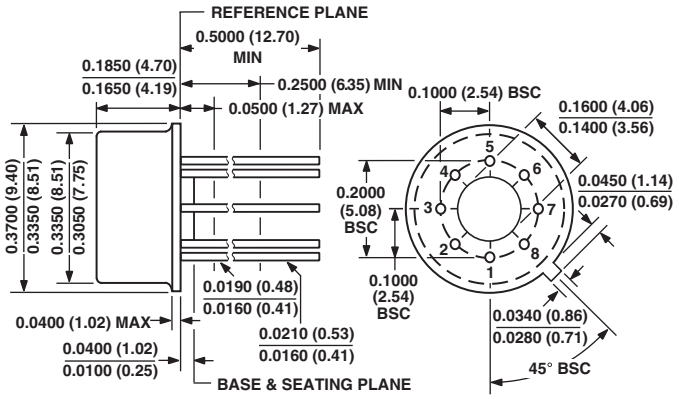
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Metal Can [TO-99]
[J Suffix]
(H-08B)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-002AK
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
12/03—Data Sheet changed from REV. E to REV. F.	
Changes to ELECTRICAL CHARACTERISTICS	2
Changes to ORDERING GUIDE	3
Updated OUTLINE DIMENSIONS	7

C00249–0–12/03(F)