FemtoClock® Crystal-to-LVDS Frequency Synthesizer w/Integrated Fanout Buffer

ICS844256D

DATA SHEET

General Description

The ICS844256D is a Crystal-to-LVDS Clock Synthesizer/Fanout Buffer designed for SONET and Gigabit Ethernet applications. The output frequency can be set using the frequency select pins and a 25MHz crystal for Ethernet frequencies, or a 19.44MHz crystal for SONET. The low phase noise characteristics of the ICS844256D make it an ideal clock for these demanding applications.

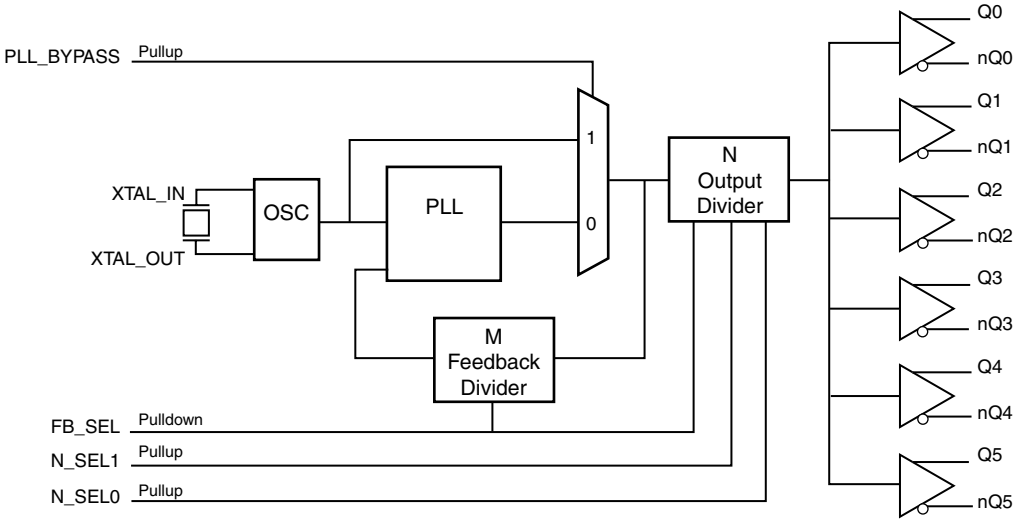
Features

- Six differential LVDS output pairs
- Crystal oscillator interface
- Output frequency range: 62.5MHz - 625MHz
- Crystal input frequency range:15.625MHz - 25.5MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.43ps (typical)
- Full 3.3V or mixed 3.3V core, 2.5V output supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

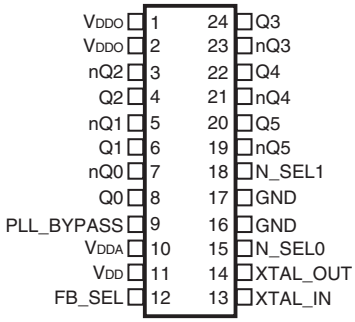
Divider Function Table

Inputs			Function		
FB_SEL	N_SEL1	N_SEL0	M Divider Value	N Divider Value	M/N Divider Value
0	0	0	25	1	25
0	0	1	25	2	12.5
0	1	0	25	4	6.25
0	1	1	25 (default)	5	5
1	0	0	32	1	32
1	0	1	32	2	16
1	1	0	32	4	8
1	1	1	32	8	4

Block Diagram



Pin Assignment



ICS844256D

24-Lead TSSOP, E-Pad
4.40mm x 7.8mm x 0.925mm
package body
G Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	V_{DDO}	Power		Output supply pins.
3, 4	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
5, 6	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
7, 8	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
9	PLL_BYPASS	Input	Pullup	PLL Bypass. When LOW, the output is driven from the VCO output. When HIGH, the PLL is bypassed and the output frequency = crystal frequency ÷ N output divider. LVCMOS / LVTTL interface levels.
10	V_{DDA}	Power		Analog supply pin.
11	V_{DD}	Power		Core supply pin.
12	FB_SEL	Input	Pulldown	Feedback and output frequency select pin. LVCMOS/LVTTL interface levels. See Table 3.
13, 14	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
15, 18	N_SEL0, N_SEL1	Input	Pullup	Feedback and output frequency select pins. LVCMOS/LVTTL interface levels. See Table 3.
16, 17	GND	Power		Power supply ground.
19, 20	nQ5, Q5	Output		Differential output pair. LVDS interface levels.
21, 22	nQ4, Q4	Output		Differential output pair. LVDS interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

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Function Tables

Table 3. Example Frequency Function Table

Inputs				Function			
XTAL (MHz)	FB_SEL	N_SEL1	N_SEL0	M Divider Value	VCO (MHz)	N Divider Value	Output (MHz)
20	0	0	0	25	500	1	500
20	0	0	1	25	500	2	250
20	0	1	0	25	500	4	125
20	0	1	1	25	500	5	100
21.25	0	1	1	25	531.25	5	106.25
24	0	0	0	25	600	1	600
24	0	0	1	25	600	2	300
24	0	1	0	25	600	4	150
24	0	1	1	25	600	5	120
25	0	0	0	25	625	1	625
25	0	0	1	25	625	2	312.5
25	0	1	0	25	625	4	156.25
25	0	1	1	25	625	5	125
25.5	0	1	0	25	637.5	4	159.375
15.625	1	1	1	32	500	8	62.5
18.5625	1	1	1	32	594	8	74.25
18.75	1	0	0	32	600	1	600
18.75	1	0	1	32	600	2	300
18.75	1	1	0	32	600	4	150
18.75	1	1	1	32	600	8	75
19.44	1	0	0	32	622.08	1	622.08
19.44	1	0	1	32	622.08	2	311.04
19.44	1	1	0	32	622.08	4	155.52
19.44	1	1	1	32	622.08	8	77.76
19.53125	1	0	0	32	625	1	625
19.53125	1	0	1	32	625	2	312.5
19.53125	1	1	0	32	625	4	156.25
19.53125	1	1	1	32	625	8	78.125
20	1	1	1	32	640	8	80

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	32.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.11	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				172	mA
I_{DDA}	Analog Supply Current				11	mA
I_{DDO}	Output Supply Current				72	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.11	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				172	mA
I_{DDA}	Analog Supply Current				11	mA
I_{DDO}	Output Supply Current				70	mA

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Table 4C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 3.3V ± 5% or 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	FB_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
		PLL_BYPASS, N_SEL0, N_SEL1	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	FB_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		PLL_BYPASS, N_SEL0, N_SEL1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4D. LVDS DC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	350	454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125	1.25	1.45	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4E. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	350	454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125	1.25	1.45	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		15.625		25.5	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

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AC Electrical Characteristics

Table 6A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		62.5		625	MHz
*t*sk(o)	Output Skew; NOTE 1, 2				65	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	125MHz (1.875MHz – 20MHz)		0.43		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		565	ps
odc	Output Duty Cycle	≤ 312.5MHz	47		53	%
		> 312.5MHz	45		55	%
t_{LOCK}	PLL Lock Time				25	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Refer to the Phase Noise Plot.

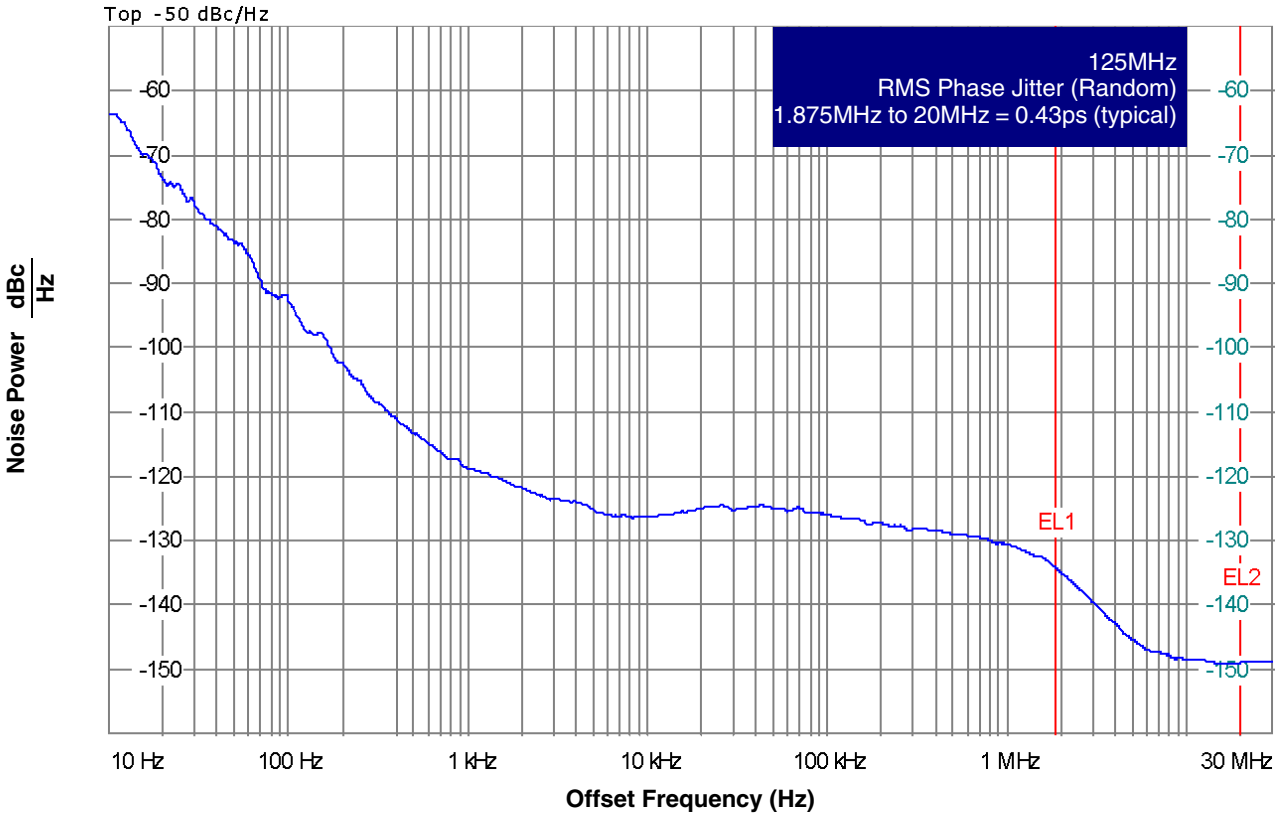
Table 6B. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		62.5		625	MHz
*t*sk(o)	Output Skew; NOTE 1, 2				65	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	125MHz (1.875MHz – 20MHz)		0.43		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		550	ps
odc	Output Duty Cycle	≤ 312.5MHz	47		53	%
		> 312.5MHz	44		56	%
t_{LOCK}	PLL Lock Time				25	ms

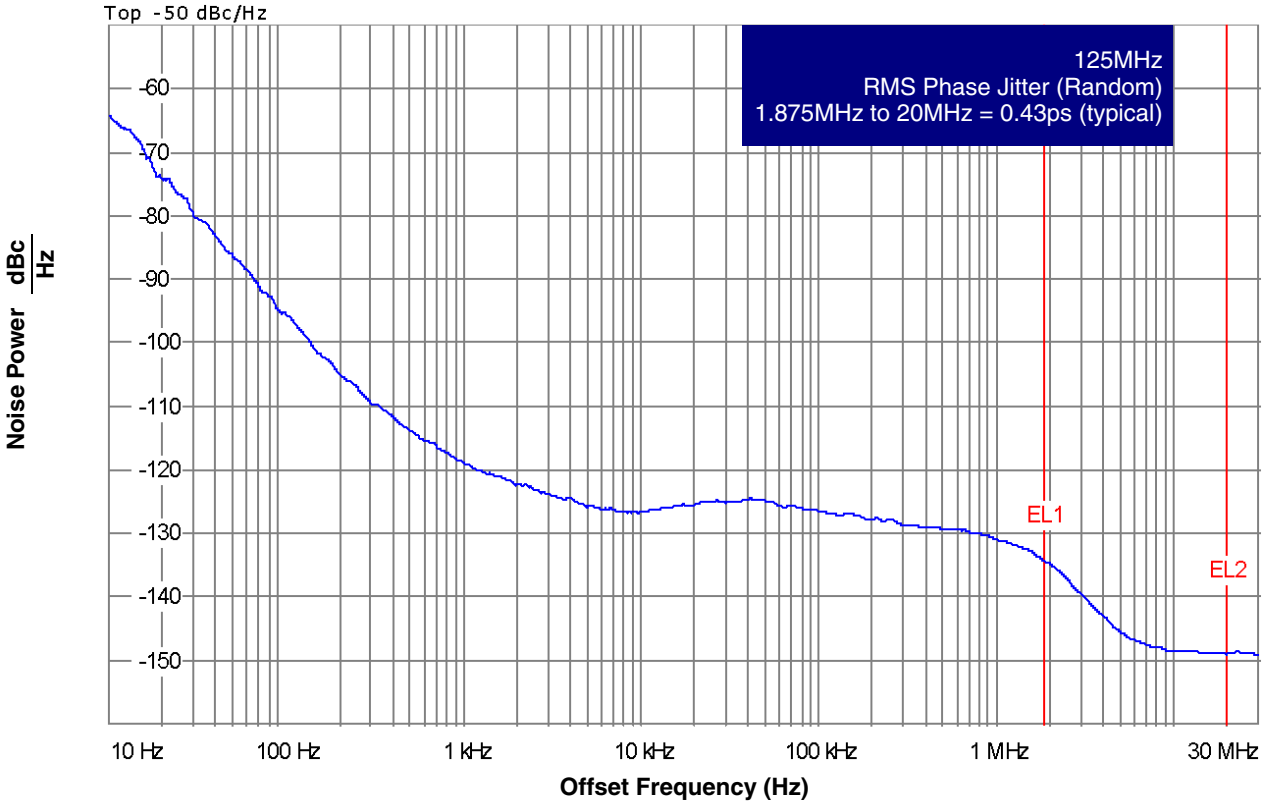
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
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NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Refer to the Phase Noise Plot.

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Typical Phase Noise at 125MHz (3.3V core/3.3V output)

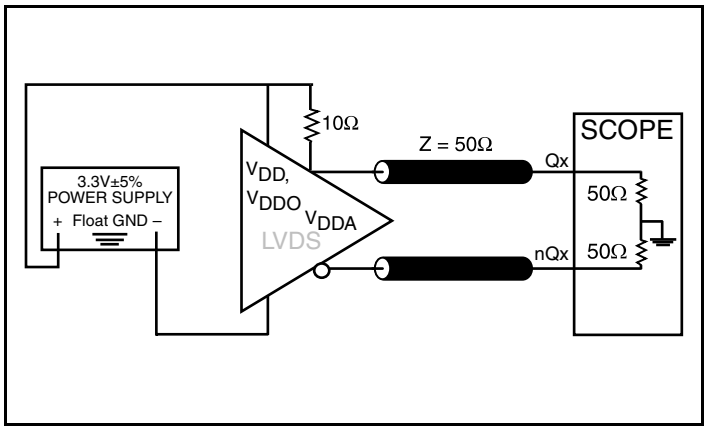


Typical Phase Noise at 125MHz (3.3V core/2.5V output)

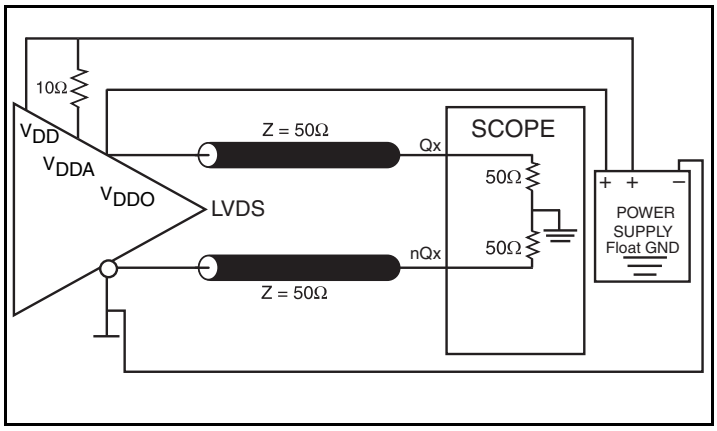


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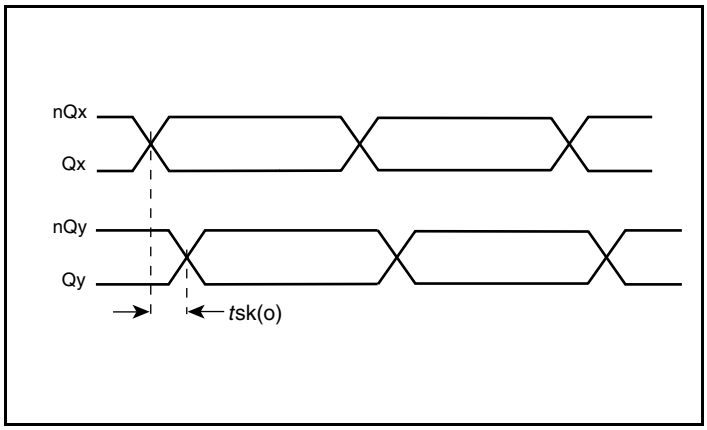
Parameter Measurement Information



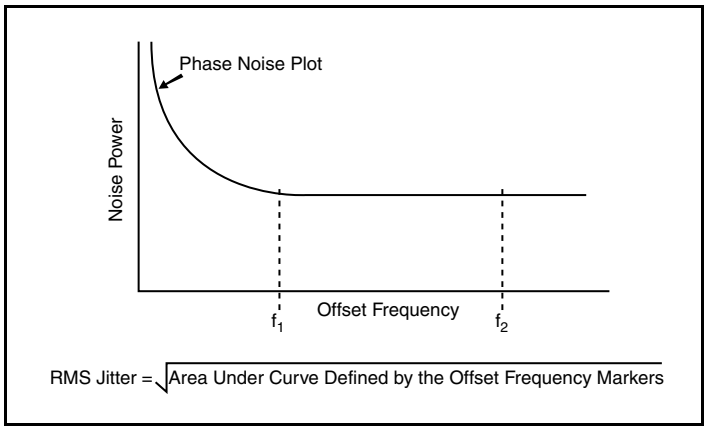
3.3V Core/3.3V Output Load AC Test Circuit



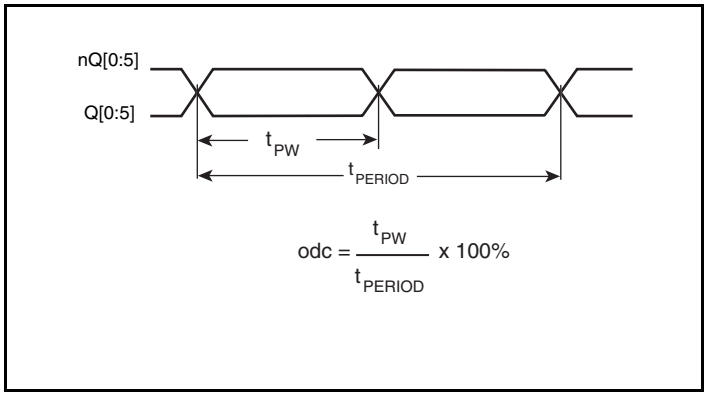
3.3V Core/2.5V Output Load AC Test Circuit



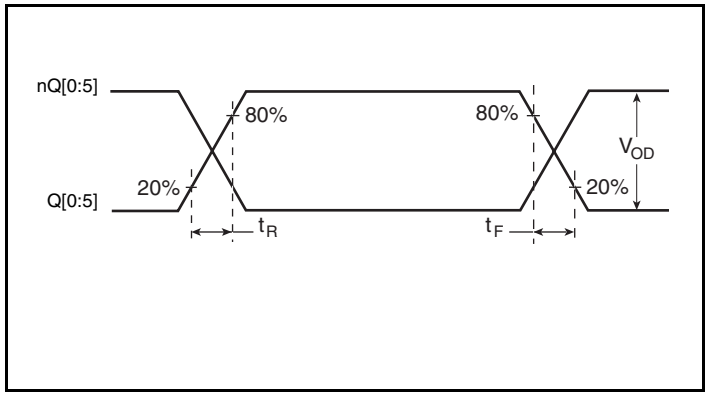
Output Skew



RMS Phase Jitter



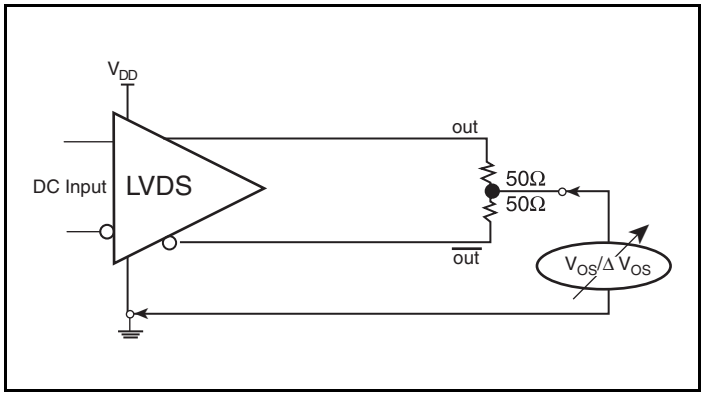
Output Duty Cycle/Pulse Width/Period



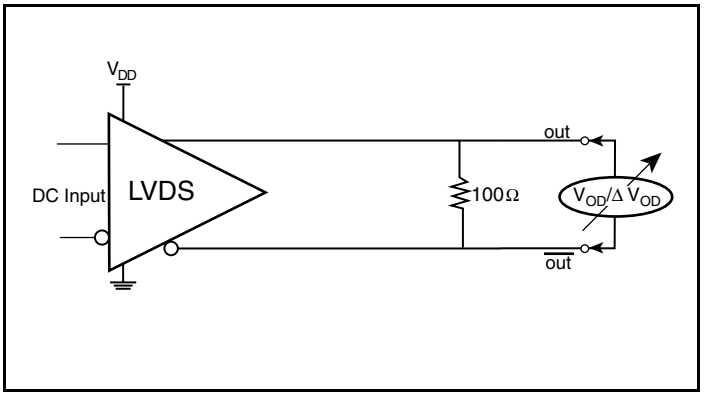
Output Rise/Fall Time

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Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844256D provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

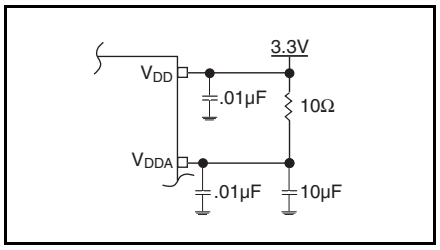


Figure 1. Power Supply Filtering

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Crystal Input Interface

The ICS844256D has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

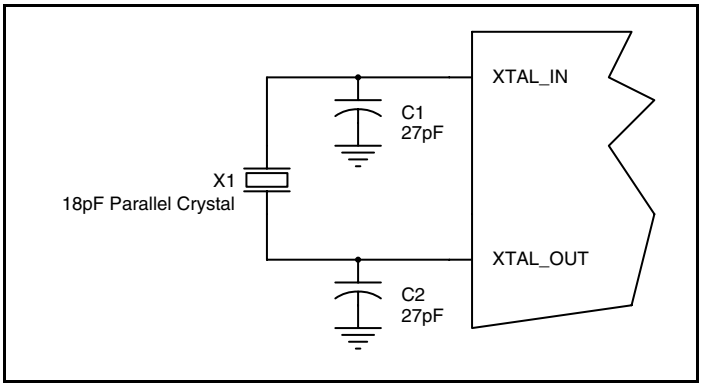


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

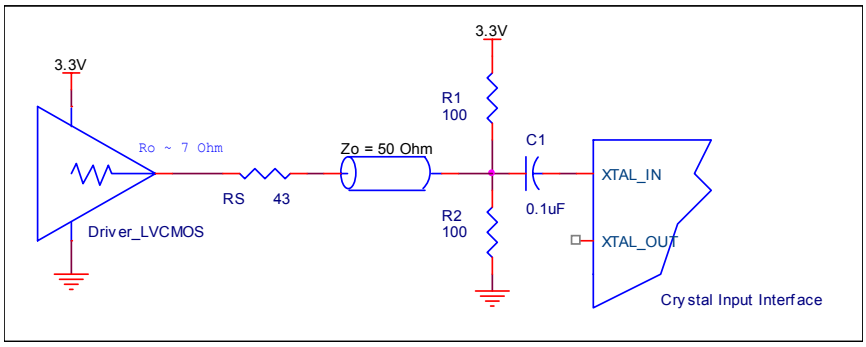


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

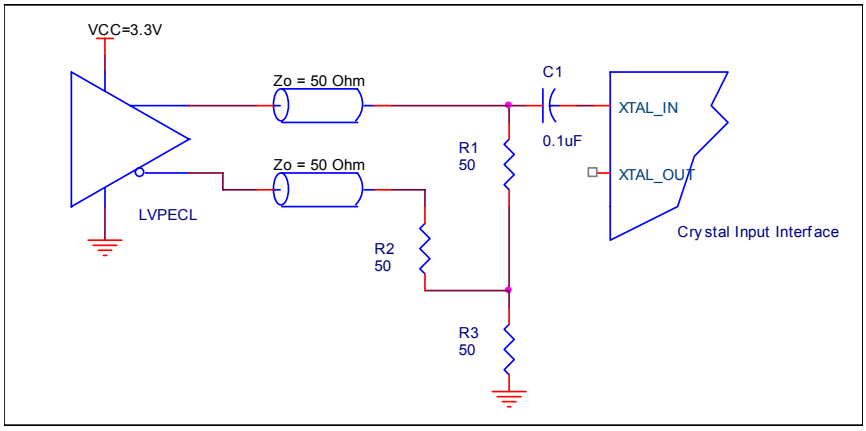


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

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Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 4 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the input receivers amplitude and common mode input range should be verified for compatibility with the output.

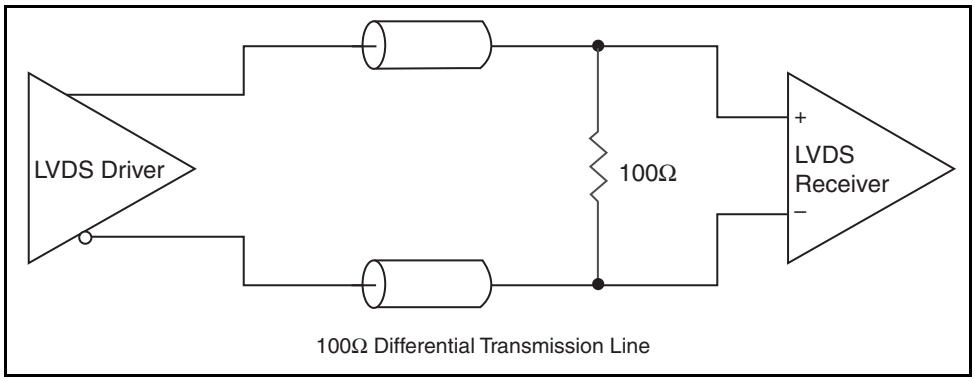


Figure 4. Typical LVDS Driver Termination

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EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

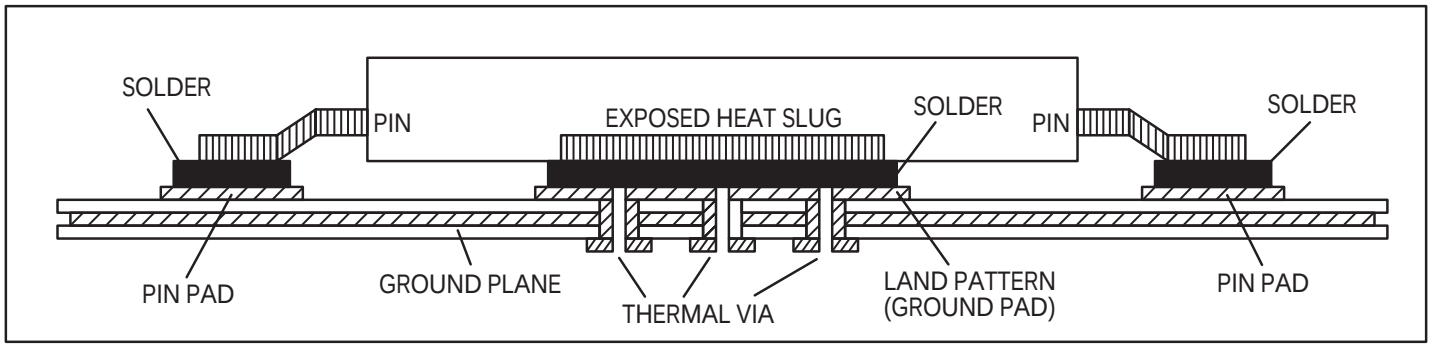


Figure 5. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

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Schematic Example

Figure 6 shows an example of ICS844256D application schematic. In this example, the device is operated at $V_{DD} = V_{DDO} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The C1 and C2 = 27pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVDS for receiver without built-in termination are shown in this schematic.

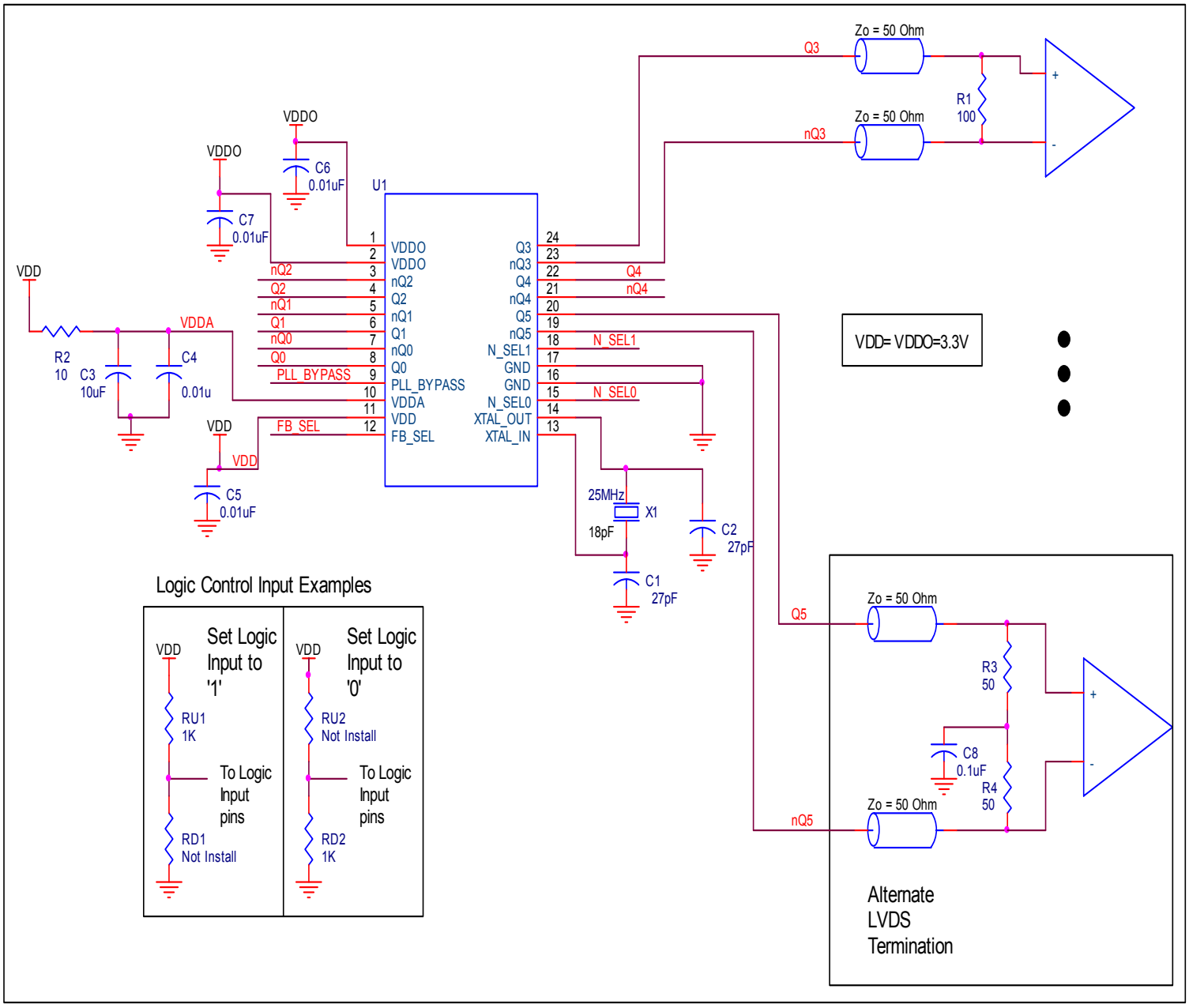


Figure 6. ICS844256D Schematic Layout

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Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844256D.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844256D is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (172mA + 11mA) = **634.1mW**
- Power (outputs)$_{MAX}$ = V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 72mA = **249.48mW**

Total Power$_{_MAX}$ = 634.1mW + 249.48mW = **883.58mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming air flow and a multi-layer board, the appropriate value is 32.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.884W * 32.1°C/W = 98.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board.

Table 7. Thermal Resistance θ_{JA} for 24 Lead TSSOP, E-Pad, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.1°C/W	25.5°C/W	24.0°C/W

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Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP, E-Pad

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.1°C/W	25.5°C/W	24.0°C/W

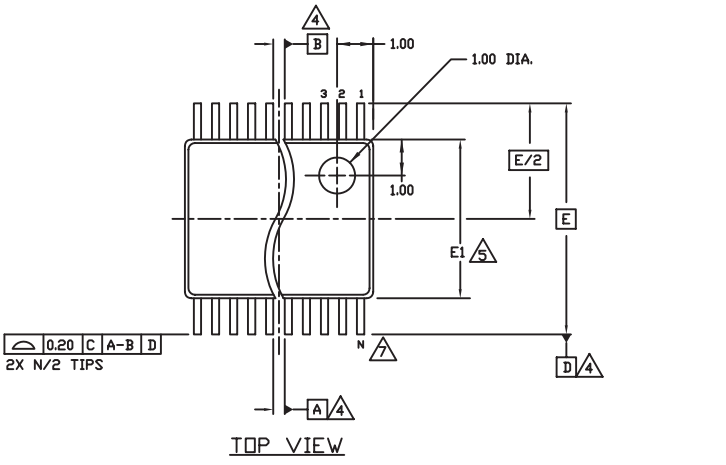
Transistor Count

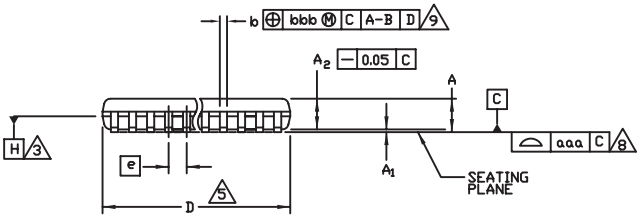
The transistor count for ICS844256D is: 4011

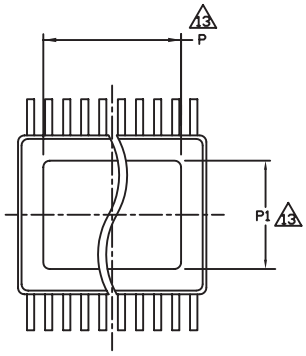
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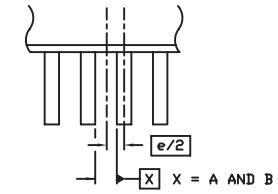
Package Outline and Package Dimensions

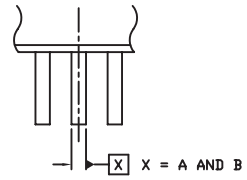
Package Outline - G Suffix for 24 Lead TSSOP, E-Pad

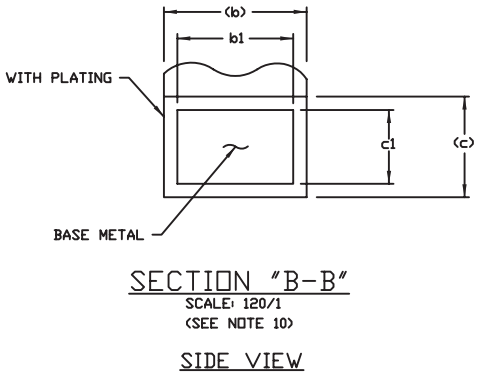


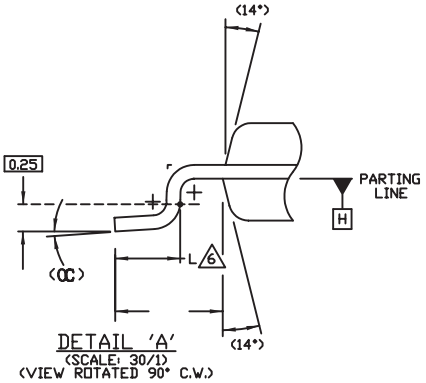












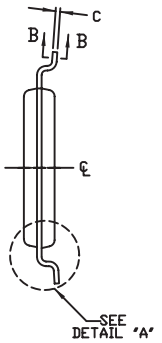


Table 9. Package Dimensions

All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		24	
A			1.10
A1	0.05		0.15
A2	0.85	0.90	0.95
b	0.19		0.30
b1	0.19	0.22	0.25
c	0.09		0.20
c1	0.09	0.127	0.16
D	7.70		7.90
E		6.40 Basic	
E1	4.30	4.40	4.50
e		0.65 Basic	
L	0.50	0.60	0.70
P	5.0		5.5
P1	3.0		3.2
α	0°		8°
ααα		0.076	
bbb		0.10	

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Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844256DGLF	ICS844256DGLF	“Lead-Free” 24 Lead TSSOP, E-Pad	Tube	0°C to 70°C
844256DGLFT	ICS844256DGLF	“Lead-Free” 24 Lead TSSOP, E-Pad	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056

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