19-4596; Rev 4; 5/09

DEMO KIT AVAILABLE

# DS3101
# Stratum 2/3E/3 Timing Card IC

www.maxim-ic.com

## GENERAL DESCRIPTION

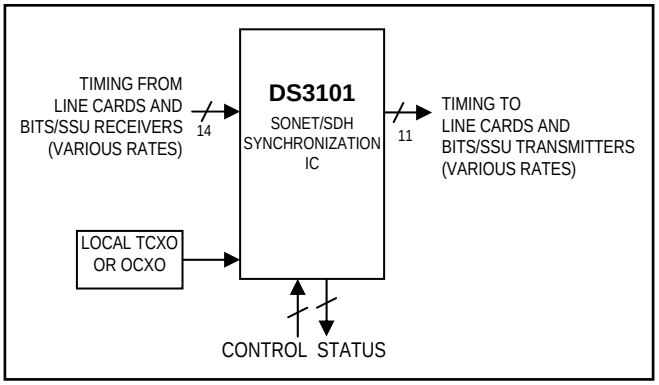
When paired with an external TCXO or OCXO, the DS3101 is a highly integrated central timing and synchronization solution for SONET/SDH network elements. With 14 input clocks, the device directly accepts both line timing from a large number of line cards and external timing from external DS1/E1 BITS transceivers. All input clocks are continuously monitored for frequency accuracy and activity. Any two of the input clocks can be selected as the references for the two core DPLLs. The T0 DPLL complies with the Stratum 2, 3E, 3 4E and 4 requirements of GR-1244, GR-253, G.812 Types I - IV, G.813 and G.8262. From the output of the core DPLLs, a wide variety of output clock frequencies and frame pulses can be produced simultaneously on the 11 output clock pins. Two DS3101 devices can be configured in a master/slave arrangement for timing card equipment protection.

The DS3101 registers and I/O pins are backward compatible with Semtech's ACS8520 and ACS8530 timing card ICs. The DS3101 is functionally equivalent to a DS3100 without integrated BITS transceivers.

## APPLICATIONS

SONET/SDH ADMs, MSPPs, and MSSPs
Digital Cross-Connects
DSLAMs
Service Provider Routers

## FUNCTIONAL DIAGRAM




## FEATURES

- **Synchronization Subsystem for Stratum 2, 3E, 3, 4E, and 4, SMC, SEC and EEC**
  - Meets Requirements of GR-1244 Stratum 2 - 4, GR-253, G.812 Types I - IV, G.813 and G.8262
  - Stratum 2, 3E or 3 Holdover Accuracy with Suitable External Oscillator
  - Programmable Bandwidth, 0.5mHz to 70Hz
  - Hitless Reference Switching on Loss of Input
  - Phase Build-Out and Transient Absorption
  - Locks To and Generates 125MHz for Gigabit Synchronous Ethernet per ITU-T G.8261
- **14 Input Clocks**
  - 10 CMOS/TTL Inputs Accept 2kHz, 4kHz, and Any Multiple of 8kHz Up to 125MHz
  - Two LVDS/LVPECL/CMOS/TTL Inputs Accept Nx8kHz Up to 125MHz Plus 155.52MHz
  - Two 64kHz Composite Clock Receivers
  - Continuous Input Clock Quality Monitoring
  - Separate 2/4/8kHz Frame Sync Input
- **11 Output Clocks**
  - Five CMOS/TTL Outputs Drive Any Internally Produced Clock Up to 77.76MHz
  - Two LVDS Outputs Each Drive Any Internally Produced Clock Up to 311.04MHz
  - One 64kHz Composite Clock Transmitter
  - One 1.544MHz/2.048MHz Output Clock
  - Two Sync Pulses: 8kHz and 2kHz
  - Output Clock Rates Include 2kHz, 8kHz, NxDS1, NxDS2, DS3, NxE1, E3, 6.48MHz, 19.44MHz, 38.88 MHz, 51.84MHz, 62.5MHz, 77.76MHz, 125MHz, 155.52MHz, 311.04MHz
- **Internal Compensation for Master Clock Oscillator Frequency Accuracy**
- **Processor Interface: 8-Bit Parallel or SPI Serial**
- **1.8V Operation with 3.3V I/O (5V Tolerant)**

## ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| DS3101GN | -40°C to +85°C | 256 CSBGA (17mm)$^2$ |
| DS3101GN+ | -40°C to +85°C | 256 CSBGA (17mm)$^2$ |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

***Note:*** *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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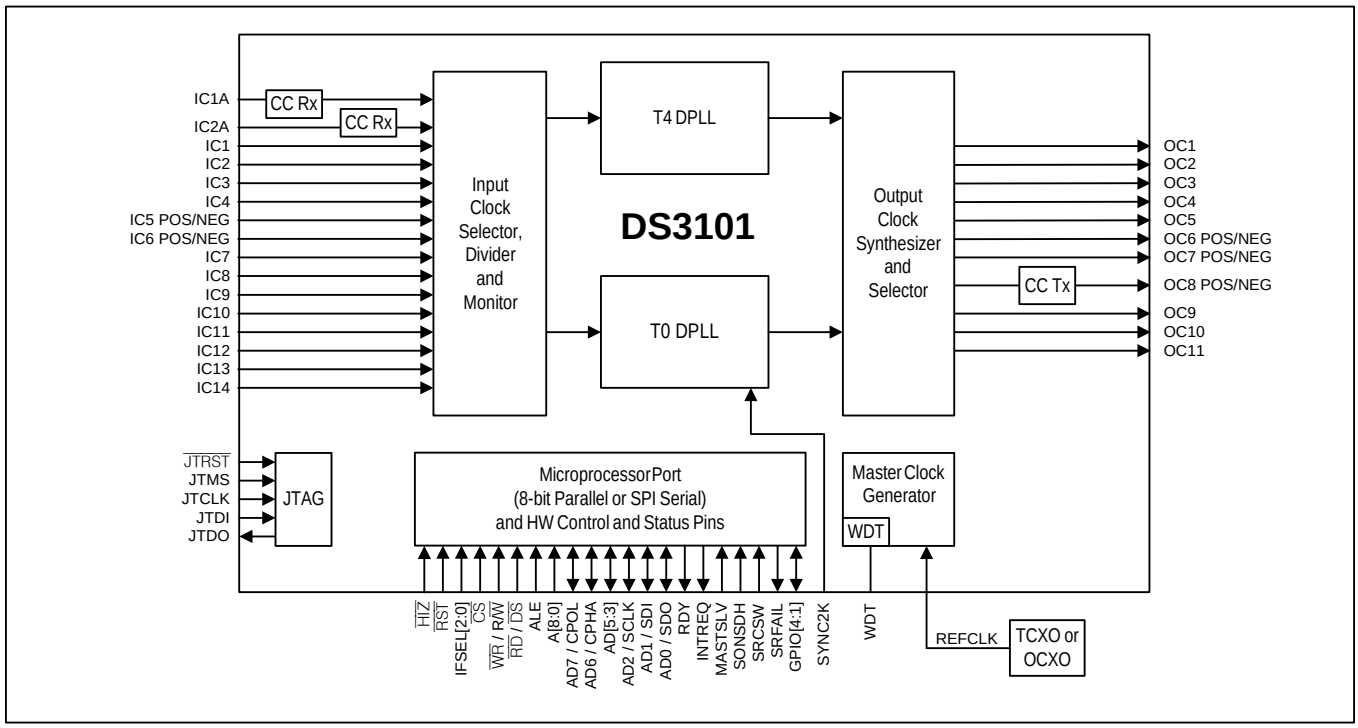
# 1. STANDARDS COMPLIANCE

## Table 1-1. Applicable Telecom Standards

| SPECIFICATION | SPECIFICATION TITLE |
|---|---|
| **ANSI** | |
| T1.101 | *Synchronization Interface Standard*, 1999 |
| T1.102 | *Digital Hierarchy—Electrical Interfaces*, 1993 |
| TIA/EIA-644-A | *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits,* 2001 |
| **ETSI** | |
| EN 300 417-6-1 | *Transmission and Multiplexing (TM); Generic Requirements of Transport Functionality of Equipment; Part 6-1: Synchronization Layer Functions*, v1.1.3 (1999-05) |
| EN 300 462-3-1 | *Transmission and Multiplexing (TM); Generic Requirements for Synchronization Networks; Part 3-1: The Control of Jitter and Wander within Synchronization Networks*, v1.1.1 (1998-05) |
| EN 300 462-5-1 | *Transmission and Multiplexing (TM); Generic Requirements for Synchronization Networks; Part 5-1: Timing Characteristics of Slave Clocks Suitable for Operation in Synchronous Digital Hierarchy (SDH) Equipment*, v1.1.1 (1998-05) |
| **IEEE** | |
| IEEE 1149.1 | *Standard Test Access Port and Boundary-Scan Architecture*, 1990 |
| **ITU-T** | |
| G.781 | *Synchronization Layer Functions* (06/1999) |
| G.783 | *ITU G.783 Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks* (10/2000 plus Amendment 1 06/2002 and Corrigendum 2 03/2003) |
| G.812 | *Timing Requirements of Slave Clocks Suitable for Use as Node Clocks in Synchronization Networks* (06/1998) |
| G.813 | *Timing characteristics of SDH equipment slave clocks (SEC)* (03/2003) |
| G.823 | *The Control of Jitter and Wander within Digital Networks which are Based on the 2048kbps Hierarchy* (03/2000) |
| G.824 | *The Control of Jitter and Wander within Digital Networks which are Based on the 1544kbps Hierarchy* (03/2000) |
| G.825 | *The Control of Jitter and Wander within Digital Networks which are Based on the Synchronous Digital Hierarchy (SDH)* (03/2000) |
| G.8262 | *Timing characteristics of synchronous Ethernet equipment slave clock (EEC)* (08/2007) |
| **TELCORDIA** | |
| GR-253-CORE | *SONET Transport Systems: Common Generic Criteria*, Issue 3, September 2000 |
| GR-378-CORE | *Generic Requirements for Timing Signal Generators*, Issue 2, February 1999 |
| GR-1244-CORE | *Clocks for the Synchronized Network: Common Generic Criteria,* Issue 2, December 2000 |

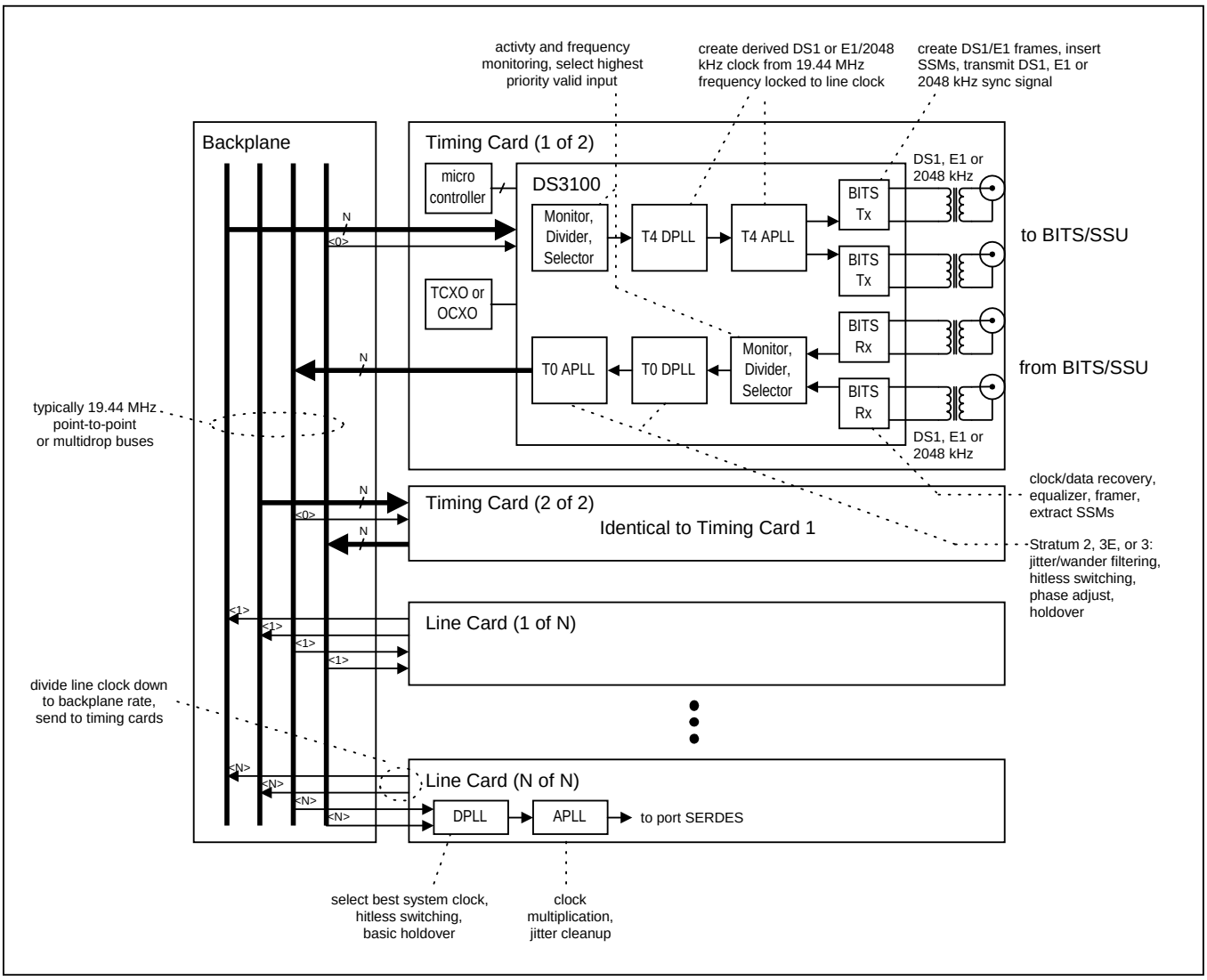
# 2. BLOCK DIAGRAM

## Figure 2-1. DS3101 Block Diagram



# 3. APPLICATION EXAMPLE

## Figure 3-1. Typical Application Example




# 4. DETAILED DESCRIPTION

Figure 2-1 illustrates the blocks described in this section and how they relate to one another. Section 5 provides a detailed feature list.

The DS3101 is a highly integrated timing card IC for systems with SONET/SDH ports. At the core of this device are two digital phase-locked loops (DPLLs) labeled T0 and T4[1]. DPLL technology makes uses of digital-signal processing (DSP) and digital-frequency synthesis (DFS) techniques to implement PLLs that are precise, flexible, and have consistent performance over voltage, temperature, and manufacturing process variations. The DS3101's DPLLs are digitally configurable for input and output frequencies, loop bandwidth, damping factor, pull-in/hold-in range, and a variety of other factors. Both DPLLs can directly lock to many common telecom frequencies and also can lock at 8kHz to any multiple of 8kHz up to 155.52MHz. The DPLLs can also tolerate and filter significant amounts of jitter and wander.

[1] These names are adapted from output ports of the SETS function specified in ITU and ETSI standards such as ETSI EN 300 462-2-1.

The T0 DPLL is responsible for generating the system clocks used to time the outgoing traffic interfaces of the system (SONET/SDH, synchronous Ethernet, etc.). To perform this role in a variety of systems with diverse performance requirements, the T0 DPLL has a sophisticated feature set and is highly configurable. T0 can automatically transition among free-run, locked and holdover states all without software intervention. In free-run, T0 generates a stable, low-noise clock with the same frequency accuracy as the external oscillator connected to the REFCLK pin. With software calibration the DS3101 can even improve the accuracy to within ±0.02 ppm. When an input reference has been validated, T0 transitions to the locked state in which its output clock accuracy is equal to the accuracy of the input reference. While in the locked state, T0 acquires a high-accuracylong-term average frequency value to use as the holdover frequency. When its selected reference fails, T0 can very quickly detect the failure and enter the holdover state to avoid affecting its output clock. From holdover it can automatically switch to the next highest priority input reference, again without affecting its output clock (hitless switching). Switching among input references can be either revertive or nonrevertive. When all input references are lost, T0 stays in holdover in which it generates a stable low-noise clock with initial frequency accuracy equal to its stored holdover value and drift performance determined by the quality of the external oscillator. With a suitable local oscillator the T0 DPLL provides holdover performance suitable for all applications up to and including Stratum 2. T0 can also perform phase build-outs and fine-granularity output clock phase adjustments.

The T4 DPLL has a much less demanding role to play and therefore is much simpler than T0. Often T4 is used as a frequency converter to create a derived DS1- or E1-rate clock (frequency locked to an incoming SONET/SDH port) to be sent to a nearby BITS Timing Signal Generator (TSG, Telcordia terminology) or Synchronization Supply Unit (SSU, ITU-T terminology). In other cases T4 is phase-locked to T0 and used as a frequency converter to produce additional output clock rates for use within the system, such as NxDS1, NxE1, NxDS2, DS3, E3, or 125MHz for synchronous Ethernet. T4 can also be configured as a measuring tool to measure the frequency of an input reference or the phase difference between two input references.

At the front end of both the T0 and T4 DPLLs is the Input Clock Selector, Divider, and Monitor (ICSDM) block. This block continuously monitors as many as 14 different input clocks of various frequencies for activity and frequency accuracy. In addition, ICSDM maintains separate input clock priority tables for the T0 and T4 DPLLs and can automatically select and provide the highest priority valid clock to each DPLL without any software intervention. The ICSDM block can also divide the selected clock down to 8kHz if required by the DPLL.

In addition to digital clock signals from system line cards, the DS3101 can also directly receive up to two 64kHz composite clock signals on its IC1A and IC2A pins. These signals typically come from a nearby BITS Timing Signal Generator or SSU to provide external timing to the system.

The Output Clock Synthesizer and Selector (OCSS) block shown in Figure 2-1 contains the T0 output APLL, the T4 output APLL, clock divider logic, and additional output DFS blocks. The T0 and T4 APLLs multiply the clock rates from the DPLLs by four and simulataneously attenuate jitter. Using the different settings of the T0 and T4 DPLLs and the output divider logic, the DS3101 can produce more than 60 different output frequencies including common SONET/SDH, PDH and synchronous Ethernet rates plus 2kHz and 8kHz frame pulses.

In addition to creating digital clock signals for use within the system, the DS3101 can also directly transmit one composite clock signal on its OC8 pin. This signal typically conveys the recovered timing from one SONET/SDH port to a nearby BITS timing-signal generator or SSU which in turn distributes timing to the whole central office.

The entire chip is clocked from the external oscillator connected to the REFCLK pin. Thus the free-run and holdover stability of the DS3101-based timing card is entirely a function of the stability of the external oscillator, the performance of which can be selected to match the application: TCXO, OCXO, double-oven OCXO, etc. The 12.8MHz clock from the external oscillator is multiplied by sixteen by the Master Clock Generator block to create the 204.8MHz master clock used by the rest of the device. Since every block on the device depends on the master clock and therefore the local oscillator clock for proper operation, the master clock generator has a watchdog timer (WDT) function that can be used to signal a local microprocessor in the event of a local oscillator clock failure.

The DS3101 also has several features to support master/slave timing card redundancy and protection. Two DS3101 devices on redundant cards can be configured to maintain the same priority tables, choose the same input references, and generate output clocks and frame syncs with the same frequency and phase.

# 5. DETAILED FEATURES

## 5.1 T0 DPLL Features

- High-resolution DPLL plus low-jitter output APLL
- Sophisticated state machine automatically transitions between free-run, locked, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth in 18 steps from 0.5mHz to 70Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10, or 20
- Multiple phase detectors: phase/frequency, early/late, and multicycle
- Phase/frequency locking (±360° capture) or nearest-edge phase locking (±180° capture)
- Multicycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- Phase build-out in response to input phase transients (1 to 3.5µs)
- Phase build-out in response to reference switching
- Less than 5ns output clock phase transient during phase build-out
- Output phase adjustment up to ±200ns in 6ps steps with respect to selected input reference
- High-resolution frequency and phase measurement
- Holdover frequency averaging with 8- or 110-minute intervals
- APLL frequency options suitable for N x 19.44MHz, N x DS1, and N x E1
- Low-jitter frame sync (8kHz) and multiframe sync (2kHz) outputs on OC10 and OC11
- 2kHz and 8kHz clocks available on OC1 through OC7 with programmable polarity and pulse width

## 5.2 T4 DPLL Features

- High-resolution DPLL plus low-jitter output APLL
- Programmable bandwidth: 18Hz, 35Hz, or 70Hz
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10, or 20
- Multiple phase detectors: phase/frequency, early/late, and multicycle
- Phase/frequency locking (±360° capture) or nearest-edge phase locking (±180° capture)
- Multicycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- APLL frequency options suitable for N x 19.44MHz, N x DS1, N x E1, DS3, E3, 6312kHz, and N x 62.5MHz (for Gigabit Ethernet)
- 2kHz and 8kHz clocks available on OC1 through OC7 with programmable polarity and pulse width
- Can operate independently or locked to T0 DPLL
- Phase detector can be used to measure phase difference between two input clocks

## 5.3 Input Clock Features

- 14 input clocks
- 10 programmable-frequency CMOS/TTL input clocks accept any multiple of 8kHz up to 125MHz
- Two LVDS/LVPECL/CMOS/TTL input clocks accept any multiple of 8kHz up to 125MHz plus 155.52MHz
- Two 64kHz composite clock receivers (AMI format) that can also be configured as programmable-frequency CMOS/TTL input clocks if needed
- All 14 input clocks are constantly monitored by programmable frequency monitors and activity monitors
- Fast activity monitor can disqualify the selected reference after two missing clock cycles
- Separate 2/4/8kHz sync input

## 5.4 Output Clock Features

- 11 output clocks
- Five programmable-frequency CMOS/TTL output clocks drive any internally produced clock up 77.76MHz
- Two programmable-frequency LVDS output clocks drive any internally produced clock up to 311.04MHz
- Two sync pulses, 2kHz and 8kHz, can be disciplined by a 2kHz or 8kHz sync input
- One 1.544MHz/2.048MHz output clock
- One 64kHz composite clock output (AMI format)
- Output clock rates include 2kHz, 8kHz, NxDS1, NxDS2, DS3, NxE1, E3, 19.44MHz, 38.88MHz, 51.84MHz, 62.5MHz, 77.76MHz, 125.0MHz, 155.52MHz, and 311.04MHz
- Outputs at even divisors of 311.04MHz have less than 0.5ns peak-to-peak output jitter

## 5.5 Redundancy Features

- Devices on redundant timing cards can be configured for master/slave operation
- Clocks and frame syncs can be cross-wired between devices to ensure that slave always tracks master
- Master/slave mode pin can auto-configure slave to track master with no phase build-out and wider bandwidth
- Input clock priority tables can easily be kept synchronized between master and slave

## 5.6 Composite Clock I/O Features

- Two composite clock receivers and one composite clock transmitter (all AMI format)
- Compliant with Telcordia GR-378 composite clock, G.703 centralized clock, and G.703 Appendix II.1 Japanese synchronization interfaces
- Configurable for 50% or 5/8 duty cycle, 1V or 3V pulse amplitude, and 110Ω/120Ω/133Ω termination
- Received signals are monitored for LOS, AMI violations, presence/absence of the 8 kHz component, and presence/absence of the 400Hz component (for G.703 Appendix II.1 option b)
- Transmitter can generate or suppress the 8kHz component and/or the 400 Hz component (for G.703 Appendix II.1 option b)
- Composite clock receiver inputs can be configured as programmable-frequency CMOS/TTL inputs if composite clock support is not needed

## 5.7 General Features

- Operates from a single external 12.800MHz local oscillator (TCXO or OCXO)
- On-chip local oscillator watchdog circuit
- Microprocessor interface can be 8-bit parallel (Intel or Motorola, multiplexed or nonmultiplexed) or SPI serial
- Register set can be write-protected

# 6. PIN DESCRIPTIONS

## Table 6-1. Input Clock Pin Descriptions

| PIN | NAME[1] | TYPE[2] | FUNCTION |
|---|---|---|---|
| H1 | REFCLK | I | **Reference Clock.** Connect to a 12.800MHz, high-accuracy, high-stability, low-noise local oscillator (TCXO or OCXO). See Section 7.3. |
| P6 | IC1A | I | **Input Clock 1 AMI.** AMI 64kHz composite clock. Enabled when MCR5:IC1SF = 0. See Section 7.10.1, Table 10-6, and Figure 10-3. |
| A10 | IC1 | $I_{PD}$ | **Input Clock 1.** CMOS/TTL. Programmable frequency (default 8kHz). Enabled when MCR5:IC1SF = 1. See Section 7.10.1. |
| P7 | IC2A | I | **Input Clock 2 AMI.** AMI 64kHz composite clock. Enabled when MCR5:IC2SF = 0. See Section 7.10.1, Table 10-6, and Figure 10-3. |
| B10 | IC2 | $I_{PD}$ | **Input Clock 2.** CMOS/TTL. Programmable frequency (default 8kHz). Enabled when MCR5:IC2SF = 1. See Section 7.10.1. |
| C10 | IC3 | $I_{PD}$ | **Input Clock 3.** CMOS/TTL. Programmable frequency (default 8kHz). |
| A11 | IC4 | $I_{PD}$ | **Input Clock 4.** CMOS/TTL. Programmable frequency (default 8kHz). |
| B5 | IC5POS | $I_A$, $I_A$ | **Input Clock 5.** LVDS/LVPECL. Programmable frequency (default 19.44MHz LVDS).<br>*LVDS*: See Table 10-4 and Figure 10-1.<br>*LVPECL*: See Table 10-5 and Figure 10-2.<br>*CMOS/TTL:* Bias IC5NEG to 1.4V and connect the single-ended signal to IC5POS. |
| A5 | IC5NEG | | |
| B4 | IC6POS | $I_A$, $I_A$ | **Input Clock 6.** LVDS/LVPECL. Programmable frequency (default 19.44MHz LVPECL).<br>*LVDS*: See Table 10-4 and Figure 10-1.<br>*LVPECL*: See Table 10-5 and Figure 10-2.<br>*CMOS/TTL:* Bias IC6NEG to 1.4V and connect the single-ended signal to IC6POS. |
| A4 | IC6NEG | | |
| B11 | IC7 | $I_{PD}$ | **Input Clock 7.** CMOS/TTL. Programmable frequency (default 19.44MHz). |
| C11 | IC8 | $I_{PD}$ | **Input Clock 8.** CMOS/TTL. Programmable frequency (default 19.44MHz). |
| A12 | IC9 | $I_{PD}$ | **Input Clock 9.** CMOS/TTL. Programmable frequency (default 19.44MHz). |
| B12 | IC10 | $I_{PD}$ | **Input Clock 10.** CMOS/TTL. Programmable frequency (default 19.44MHz). |
| A13 | IC11 | $I_{PD}$ | **Input Clock 11.** CMOS/TTL. Programmable frequency (default 19.44MHz in master mode, 6.48MHz in slave mode). |
| C12 | IC12 | $I_{PD}$ | **Input Clock 12.** CMOS/TTL. Programmable frequency (default 1.544/2.048MHz). |
| B13 | IC13 | $I_{PD}$ | **Input Clock 13.** CMOS/TTL. Programmable frequency (default 1.544/2.048MHz). |
| A14 | IC14 | $I_{PD}$ | **Input Clock 14.** CMOS/TTL. Programmable frequency (default 1.544/2.048MHz). |
| B14 | SYNC2K | $I_{PD}$ | **Frame Sync Input.** 2kHz, 4kHz, or 8kHz. |

## Table 6-2. Output Clock Pin Descriptions

| PIN | NAME[1] | TYPE[2] | FUNCTION |
|---|---|---|---|
| C6 | OC1 | $O_3$ | **Output Clock 1.** CMOS/TTL. Programmable frequency (default 6.48MHz). |
| A7 | OC2 | $O_3$ | **Output Clock 2.** CMOS/TTL. Programmable frequency (default 38.88MHz). |
| B7 | OC3 | $O_3$ | **Output Clock 3.** CMOS/TTL. Programmable frequency (default 19.44MHz). |
| C7 | OC4 | $O_3$ | **Output Clock 4.** CMOS/TTL. Programmable frequency (default 38.88MHz). |
| A8 | OC5 | $O_3$ | **Output Clock 5.** CMOS/TTL. Programmable frequency (default 77.76MHz). |
| B3 | OC6POS | $O_3$ | **Output Clock 6.** LVDS. Programmable frequency (default 38.88MHz LVDS). See Table 10-4 and Figure 10-1. |
| A3 | OC6NEG | | |
| C2 | OC7POS | $O_3$ | **Output Clock 7.** LVDS. Programmable frequency (default 19.44MHz LVDS). See Table 10-4 and Figure 10-1. |
| C1 | OC7NEG | | |
| C8 | OC8POS | $O_3$ | **Output Clock 8.** AMI. 64kHz composite clock. See Section 7.10.2, Table 10-6, and Figure 10-3. |
| B8 | OC8NEG | | |
| A9 | OC9 | $O_3$ | **Output Clock 9.** CMOS/TTL. 1.544/2.048MHz. |
| B9 | OC10 | $O_3$ | **Output Clock 10.** CMOS/TTL. 8kHz frame sync or clock. |
| C9 | OC11 | $O_3$ | **Output Clock 11.** CMOS/TTL. 2kHz multiframe sync or clock. |

## Table 6-3. Global Pin Descriptions

| PIN | NAME[1] | TYPE[2] | FUNCTION |
|---|---|---|---|
| B6 | $\overline{RST}$ | $I_{PU}$ | **Active-Low Reset.** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as $\overline{RST}$ is low. $\overline{RST}$ should be held low for at least two REFCLK cycles. |
| R14 | $\overline{HIZ}$ | $I_{PU}$ | **Acitve-Low High-Z Enable Input.** The $\overline{JTRST}$ pin must be low to activate this function.<br>0 = Put all output pins in a high-impedance state<br>1 = Normal operation |
| N1 | IFSEL0 | $I_{PD}$ | **Microprocessor Interface Select.** During reset, the value on these pins is latched into the IFSEL field of the IFCR register. See Section 7.11.<br>010 = Intel bus mode (multiplexed)<br>011 = Intel bus mode (nonmultiplexed)<br>100 = Motorola mode (nonmultiplexed)<br>101 = SPI mode (address and data transmitted LSB first)<br>110 = Motorola mode (multiplexed)<br>111 = SPI mode (address and data transmitted MSB first)<br>000, 001 = {unused value} |
| N2 | IFSEL1 | | |
| P1 | IFSEL2 | | |
| R11 | MASTSLV | $I_{PU}$ | **Master/Slave Select Input.** Sets the state of the MASTSLV bit in the MCR3 register.<br>0 = slave mode<br>1 = master mode |
| M3 | SONSDH | $I_{PD}$ | **SONET/SDH Frequency Select Input.** Sets the reset-default state of the SONSDH bit in MCR3, the DIG1SS and DIG2SS bits in MCR6, and the OC9SON bit in T4CR1.<br>0 = SDH rates (N x 2.048MHz)<br>1 = SONET rates (N x 1.544MHz) |
| M2 | SRCSW | $I_{PD}$ | **Source Switching.** Fast source switching control input. See Section 7.6.5. |
| J2 | SRFAIL | $O_3$ | **SRFAIL Status.** When MCR10:SRFPIN = 1, this pin follows the state of the SRFAIL status bit in the MSR2 register. This gives the system a very fast indication of the failure of the current reference. When MCR10:SRFPIN = 0, SRFAIL is disabled (low). |
| C5 | WDT | $I_A$ | **Watchdog Timer.** Analog node for the REFCLK watchdog timer. Connect to a resistor (R) to $V_{DDIO}$ and a capacitor (C) to ground. Suggested values are R = 20kΩ and C = 0.01µF. See Section 7.3. |

## Table 6-4. Parallel Interface Pin Descriptions

***Note:*** *These pins are active in Intel and Motorola bus modes. See Section 7.11.1 for functional description and Section 10.4 for timing specifications.*

| PIN | NAME[1] | TYPE[2] | FUNCTION |
|---|---|---|---|
| K14 | ALE | $I_{PD}$ | **Address Latch Enable.** This signal controls the address latch. In nonmultiplexed bus modes, the address is latched from A[8:0]. In these modes, ALE is typically wired high to make the latch transparent. In multiplexed bus modes, the address is latched from A[8] and AD[7:0]. |
| J16 | $\overline{CS}$ | $I_{PU}$ | **Active-Low Chip Select.** This pin must be asserted (low) to read or write internal registers. |
| J15 | $\overline{WR}$/R/$\overline{W}$ | $I_{PU}$ | **Active-Low Write Enable or Read/Active-Low Write Select.** For Intel bus modes, $\overline{WR}$ is asserted to write internal registers. For Motorola bus modes, R/$\overline{W}$ = 1 indicates a read and R/$\overline{W}$ = 0 indicates a write. |
| J14 | $\overline{RD}$/$\overline{DS}$ | $I_{PU}$ | **Active-Low Read Enable or Active-Low Data Strobe.** For the Intel-style interface modes, $\overline{RD}$ is asserted (low) to read internal registers. For the Motorola-style interface modes, the falling edge of $\overline{DS}$ enables data output on AD[7:0] during reads while the rising edge of $\overline{DS}$ latches data from AD[7:0] during writes. |
| E16 | A[8] | $I_{PD}$ | **Address Bus.** In nonmultiplexed bus modes, these inputs specify the address of the internal register to be accessed. In multiplexed bus modes, the address is specified on A[8] and AD[7:0], while A[7:0] are not used and should be wired high or low. |
| F15 | A[7] | | |
| G14 | A[6] | | |
| F16 | A[5] | | |
| G15 | A[4] | | |
| H14 | A[3] | | |
| G16 | A[2] | | |
| H15 | A[1] | | |
| H16 | A[0] | | |
| C14 | AD[7] | I/O | **Address/Data Bus.** In both multiplexed and nonmultiplexed bus modes, these pins are an 8-bit data bus. In multiplexed bus modes, these pins also convey the lower 8 bits of the register address. |
| D14 | AD[6] | | |
| E14 | AD[5] | | |
| C15 | AD[4] | | |
| D15 | AD[3] | | |
| C16 | AD[2] | | |
| D16 | AD[1] | | |
| E15 | AD[0] | | |
| B15 | $\overline{RDY}$ | O | **Active-Low Ready/Data Acknowledge.** This pin is asserted when the device has completed a read or write operation. |
| A15 | INTREQ | O | **Interrupt Request.** The behavior of this pin is configured in the INTCR register. Polarity can be active high or active low. Drive action can be push-pull or open drain. The pin can also be configured as a general-purpose output if the interrupt request function is not needed. |

## Table 6-5. SPI Bus Mode Pin Descriptions

***Note:*** *These pins are active in SPI interface modes. See Section 7.11.2 for functional description and Section 10.5 for timing specifications.*

| PIN | NAME[1] | TYPE[2] | FUNCTION |
|---|---|---|---|
| J16 | $\overline{CS}$ | $I_{PU}$ | **Active-Low Chip Select.** This pin must be asserted to read or write internal registers. |
| C16 | SCLK | I | **Serial Clock.** SCLK is always driven by the SPI bus master. |
| D16 | SDI | I | **Serial Data Input.** The SPI bus master transmits data to the device on this pin. |
| E15 | SDO | O | **Serial Data Output.** The device transmits data to the SPI bus master on this pin. |
| D14 | CPHA | I | **Clock Phase.** See Section Figure 7-8.<br>0 = data is latched on the leading edge of the SCLK pulse<br>1 = data is latched on the trailing edge of the SCLK pulse |
| C14 | CPOL | I | **Clock Polarity.** See Section Figure 7-8.<br>0 = SCLK is normally low and pulses high during bus transactions<br>1 = SCLK is normally high and pulses low during bus transactions |
| A15 | INTREQ | O | **Interrupt Request.** The behavior of this pin is configured in the INTCR register. Polarity can be active high or active low. Drive action can be push-pull or open drain. The pin can also be configured as a general-purpose output if the interrupt request function is not needed. |

## Table 6-6. JTAG Interface Pin Descriptions

***Note:*** *See Section 9 for functional description and Section 10.6 for timing specifications.*

| PIN | NAME[1] | TYPE[2] | FUNCTION |
|---|---|---|---|
| T8 | $\overline{JTRST}$ | $I_{PU}$ | **Active-Low JTAG Test Reset.** Asynchronously resets the test access port (TAP) controller. If not used, $\overline{JTRST}$ can be held low or high. |
| R8 | JTCLK | I | **JTAG Clock.** Shifts data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, JTCLK can be held low or high. |
| R9 | JTDI | $I_{PU}$ | **JTAG Test Data Input.** Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, JTDI can be held low or high. |
| P9 | JTDO | O | **JTAG Test Data Output.** Test instructions and data are clocked out on this pin on the falling edge of JTCLK. If not used, leave floating. |
| T9 | JTMS | $I_{PU}$ | **JTAG Test Mode Select.** Sampled on the rising edge of JTCLK and is used to place the port into the various defined IEEE 1149.1 states. If not used, connect to $V_{DDIO}$ or leave floating. |

## Table 6-7. General-Purpose I/O Pin Descriptions

| PIN | NAME[1] | TYPE[2] | FUNCTION |
|---|---|---|---|
| E2 | GPIO1 | I/O | **General-Purpose I/O Pin 1.** GPCR:GPIO1D configures this pin as an input or an output. GPCR:GPIO1O specifies the output value. GPSR:GPIO1 indicates the state of the pin. |
| F3 | GPIO2 | I/O | **General-Purpose I/O Pin 2.** GPCR:GPIO2D configures this pin as an input or an output. GPCR:GPIO2O specifies the output value. GPSR:GPIO2 indicates the state of the pin. |
| H2 | GPIO3 | I/O | **General-Purpose I/O Pin 3.** GPCR:GPIO3D configures this pin as an input or an output. GPCR:GPIO3O specifies the output value. GPSR:GPIO3 indicates the state of the pin. |
| J1 | GPIO4 | I/O | **General-Purpose I/O Pin 4.** GPCR:GPIO4D configures this pin as an input or an output. GPCR:GPIO4O specifies the output value. GPSR:GPIO4 indicates the state of the pin. |

## Table 6-8. Power-Supply Pin Descriptions

| PIN | NAME[1] | TYPE[2] | FUNCTION |
|---|---|---|---|
| D6, D8, D9, D11, E6, E11, F4, F5, F12, F13, H4, H13, J4, J13, L4, L5, L12, L13, M6, M11, N6, N8, N9, N11 | $V_{DD}$ | P | **Core Power Supply.** 1.8V ±10% |
| B1, B16, D7, D10, E7–E10, G4, G5, G12, G13, H5, H12, J5, J12, K4, K5, K12, K13, M7–M10, N7, N10, R1, R16 | $V_{DDIO}$ | P | **I/O Power Supply.** 3.3V ±10% |
| A1, A16, D4, D5, D12, D13, E4, E5, E12, E13, F6–F11, G6–G11, H6–H11, J6–J11, K6–K11, L6–L11, M4, M5, M12, M13, N4, N5, N12, N13, T1, T16 | $V_{SS}$ | P | **Ground Reference** |
| A6 | VDD_ICDIFF | P | **Power Supply for LVDS Inputs (IC5 and IC6).** 3.3V ±10% |
| C4 | VSS_ICDIFF | P | **Return for LVDS Inputs (IC5 and IC6)** |
| B2 | VDD_OC6 | P | **Power Supply for LVDS Output OC6.** 1.8V ±10% |
| A2 | VSS_OC6 | P | **Return for LVDS Output OC6** |
| C3 | VDD_OC7 | P | **Power Supply for LVDS Output OC7.** 1.8V ±10% |
| D3 | VSS_OC7 | P | **Return for LVDS Output OC7** |
| D1 | AVDD_PLL1 | P | **Power Supply for T0 Output APLL.** 1.8V ±10% |
| D2 | AVSS_PLL1 | P | **Return for T0 Output APLL** |
| E1 | AVDD_PLL2 | P | **Power Supply for T4 Output APLL.** 1.8V ±10% |
| E3 | AVSS_PLL2 | P | **Return for T4 Output APLL.** |
| F1 | AVDD_PLL3 | P | **Power Supply for T0 Feedback APLL.** 1.8V ±10% |
| G2 | AVSS_PLL3 | P | **Return for T0 Feedback APLL** |
| G1 | AVDD_PLL4 | P | **Power Supply for Master Clock Generator APLL.** 1.8V ±10% |
| G3 | AVSS_PLL4 | P | **Return for Master Clock Generator APLL** |
| TM1 | R13 | — | **Connect to $V_{SS}$** |
| TM2 | T15 | | |
| C13, F2, F14, H3, J3, K1, K2, K3, K15, K16, L1, L2, L3, L14, L15, L16, M1, M14, M15, M16, N3, N14, N15, N16, P2–P5, P8, P10–P16, R2–R7, R10, R12, R15, T2–T7, T10–T14 | N.C. | — | **No Connection** |

**Note 1:** All pin names with an overbar (e.g., $\overline{CS}$) are active low.

**Note 2:** All pins, except power and analog pins, are CMOS/TTL, unless otherwise specified in the pin description.

I = input pin

O = output pin

$I_A$ = analog input pin

$O_A$ = analog output pin (can be placed in a high-impedance state)

$I_{PD}$ = input pin with internal 50kΩ pulldown

$O_3$ = output pin that can tri-stated (i.e., placed in a high-impedance state)

$I_{PU}$ = input pin with internal 50kΩ pullup to approx. 2.2V

P = power-supply pin

I/O = input/output pin

**Note 3:** All digital pins are I/O pins in JTAG mode.

**Note 4:** When ramping power supplies up or down, the voltage on any 1.8V power supply pin must not exceed the voltage on any 3.3V power-supply pin.

# 7. FUNCTIONAL DESCRIPTION

## 7.1 Overview

The DS3101 has 14 input clocks and 11 output clocks,. There are two separate DPLL paths in the device: the high-performance T0 path and the simpler T4 path. See Figure 2-1.

Two of the 14 input clocks are 64kHz composite clock receivers (by default), two are LVDS/LVPECL, and 10 are CMOS/TTL (5V tolerant). The composite clock receivers can be converted to CMOS/TTL inputs as needed. The CMOS/TTL inputs can accept signals from 2kHz to 125MHz. The LVDS/LVPECL pins can accept clock signals up to 155.52MHz.

Each input clock can be monitored continually for activity and/or frequency. Frequency can be compared to both a hard limit and a soft limit. Inputs outside the hard limit are declared invalid, while inputs inside the hard limit but outside the soft limit are merely flagged. Each input can be marked unavailable or given a priority number. Separate input priority numbers are maintained for the T0 DPLL and the T4 DPLL. Except in special modes, the highest priority valid input is automatically selected as the reference for each path.

Both the T0 and T4 DPLLs can directly lock to many common telecom frequencies, including, but not limited to 8kHz, DS1, E1, 19.44MHz, and 38.88MHz. The DPLLs can also lock to any multiple of 8kHz up to 125MHz.

The T0 DPLL is the high-performance path with all the features for node timing synchronization. The T4 DPLL is a simpler auxiliary path typically used to provide derived DS1s, E1s, or other synchronization signals to an external BITS/SSU. The two paths can be operated independently or locked together.

Both DPLLs have these features:

- Automatic reference selection based on input quality and priority
- Optional manual reference selection/forcing
- Configurable quality thresholds for each input
- Adjustable PLL characteristics, including bandwidth, pull-in range, and damping factor
- Ability to lock to several common telecom frequencies plus multiples of 8kHz up to 155.52MHz
- Frequency conversion between input and output using digital frequency synthesis
- Combined performance of a stable, consistent digital PLL and a low-jitter analog output PLL

The T0 DPLL has these additional features not available in the T4 DPLL:

- A full state machine for automatic transitions among free-run, locked, and holdover states
- Nonrevertive reference switching mode
- Phase build-out for reference switching (“hitless”) and for phase hits on the selected reference
- Output vs. input phase offset control
- 18 bandwidth selections from 0.5mHz to 70Hz (vs. three selections for the T4 path)
- Noise rejection circuitry for low-frequency references
- Optional software control over holdover frequency
- Output phase alignment to input frame sync signal
- Several frequency averaging methods for acquiring the holdover frequency

The T4 DPLL has these additional features not available in the T0 DPLL:

- Optional mode to lock to the T0 DPLL
- Optional mode to measure the phase difference between two input clocks
- Ability to generate DS3, E3, 6312kHz, and N x 62.5MHz (Gigabit Ethernet) frequencies

Typically the internal state machine controls the T0 DPLL, but manual control by system software is also available. The T4 DPLL has a simpler state machine that software cannot directly control. In either DPLL, however, software can override the DPLL logic using manual reference selection.

The T0 DPLL always operates at 77.76MHz, regardless of the output frequencies selected for the output clock pins. The T4 DPLL can operate at any of several frequencies in order to support generation of frequencies such as

44.736MHz (DS3) and 34.368MHz (E3). When the T4 DPLL is locked to the T0 DPLL, it locks to an 8kHz signal from T0 to ensure synchronization of all possible T4 frequencies, which are always multiples of 8kHz.

The outputs of the T0 and T4 DPLLs are connected to high-speed APLLs that multiply the DPLL clock rate and filter DPLL output jitter. The outputs of the APLLs are divided down to make a wide variety of possible frequencies available at the output clock pins. All or some of the output frequencies of the T0 DPLL can be synchronized to an input 2kHz, 4kHz, or 8kHz sync signal (SYNC2K pin). This synchronization to a low-frequency input enables, among other things, two redundant timing cards to maintain output phase alignment with one another.

Seven of the output clocks can be configured for a variety of different frequencies from either the T0 DPLL or the T4 DPLL. One output clock is a 64kHz composite clock transmitter (AMI format), one is 1544kHz or 2048kHz, one is 8kHz, and one is 2kHz. Of the seven multifrequency outputs, five are CMOS/TTL and two are LVDS. Altogether more than 60 output frequencies are possible, ranging from 2kHz to 311.04MHz.

## 7.2 Device Identification and Protection

The 16-bit read-only ID field in the ID1 and ID2 registers is set to 0C1Dh = 3101 decimal. The device revision can be read from the REV register. Contact the factory to interpret this value and determine the latest revision. The register set can be protected from inadvertent writes using the PROT register.

## 7.3 Local Oscillator and Master Clock Configuration

The T0 and T4 DPLL paths operate from a 204.8MHz master clock. The master clock is synthesized from a 12.800MHz clock originating from a local oscillator attached to the REFCLK pin. The stability of the T0 DPLL in holdover is equivalent to the stability of the local oscillator. Selection of an appropriate local oscillator is, therefore, of crucial importance if the telecom standards listed in Table 1-1 are to be met. TCXOs can be used in less stringent cases, but OCXOs are required in the most demanding applications. Even OCXOs may need to be shielded to avoid slow frequency changes due to ambient temperature fluctuations and drift. Careful evaluation of the local oscillator component is necessary to ensure proper performance. Contact Maxim at www.maxim-ic.com/support for recommended oscillators. For reference, the Telcordia GR-1244-CORE stability requirements for Stratum 2, Stratum 3E and Stratum 3 are listed in Table 7-1.

### Table 7-1. GR-1244 Stratum 2/3E/3 Stability Requirements

| PARAMETER | STRATUM 2 | STRATUM 3E | STRATUM 3 |
|---|---|---|---|
| Temperature | n/a | $\pm 10 \times 10^{-9}$ | $\pm 280 \times 10^{-9}$ |
| Drift (non-temp) | $\pm 1 \times 10^{-10}$/day | $\pm 1.16 \times 10^{-14}$/sec ($\pm 1 \times 10^{-9}$/day) | $\pm 4.63 \times 10^{-13}$/sec ($\pm 40 \times 10^{-9}$/day) |

***Note:*** *Refer to GR-1244-CORE for additional details.*

The stability of the local oscillator is very important, but its absolute frequency accuracy is less important because the DS3101 can compensate for frequency inaccuracies when synthesizing the 204.8MHz master clock from the local oscillator clock. The MCLKFREQ field in registers MCLK1 and MCLK2 specifies the frequency adjustment to be applied. The adjust can be from -771ppm to +514ppm in 0.0196229ppm (i.e., ~0.02ppm) steps.

The DS3101 implements a stand-alone watchdog circuit that causes an interrupt on the INTREQ pin when the local oscillator attached to the REFCLK pin is significantly off frequency. The watchdog interrupt is not maskable, but *is* subject to the INTCR register settings. When the watchdog circuit activates, reads of any and all registers in the device will return 00h to indicate the failure. In response to the activation of the INTREQ pin or during periodic polling, if system software ever reads 00h from the ID registers (which are hard-coded to 0C1Dh = 3101 decimal) then it can conclude that the local oscillator attached to that DS3101 has failed. For proper operation of the watchdog timer, connect the WDT pin to a resistor (R) to $V_{DDIO}$ and a capacitor (C) to ground. Suggested values are R = 20kΩ and C = 0.01µF.

## 7.4 Input Clock Configuration

The DS3101 has 14 input clocks: IC1 to IC14. Table 7-2 provides summary information about each clock, including signal format and available frequencies. The device tolerates a wide range of duty cycles on input clocks, out to a minimum high time or minimum low time of 3ns or 30% of the clock period, whichever is smaller.

### 7.4.1 Signal Format Configuration

Inputs with CMOS/TTL signal format accept both TTL and 3.3V CMOS levels. One key configuration bit that affects the available frequencies is the SONSDH bit in MCR3. When SONSDH = 1 (SONET mode), the 1.544MHz frequency is available. When SONSDH = 0 (SDH mode), the 2.048MHz frequency is available. During reset, the default value of this bit is latched from the SONSDH pin.

Input clocks IC5 and IC6 can be configured to accept LVDS, LVPECL, or CMOS/TTL signals by using the proper set of external components. The recommended LVDS termination is shown in Figure 10-1, and the LVDS electrical specifications are listed in Table 10-4. The recommended LVPECL termination is shown in Figure 10-2, and the LVPECL electrical specifications are listed in Table 10-5. To configure these differential inputs to accept single-ended CMOS/TTL signals, use a voltage-divider to bias the ICxNEG pin to approximately 1.4V and connect the single-ended signal to the ICxPOS pin. If IC5 or IC6 is not used it should be configured for LVDS and left floating (one input is internally pulled high and the other internally pulled low). (See also MCR5:IC5SF and IC6SF.)

By default, input clocks IC1 and IC2 are 64kHz composite clock receivers (see Section 7.10). The composite clock signal is a 64kHz AMI clock with an embedded 8kHz clock indicated by deliberate bipolar violations (BPVs) every 8 clock cycles. The 8kHz component is the clock that is forwarded to the DPLLs. The AMI composite clock electrical specifications are shown in Table 10-6, and the recommended external components are shown in Figure 10-3. IC1 and IC2 can be configured as standard CMOS/TTL inputs (identical to IC3) by setting MCR5:IC1SF = 1 or MCR5:IC2SF = 1, respectively.

## Table 7-2. Input Clock Capabilities

| INPUT CLOCK | SIGNAL FORMATS | FREQUENCIES | DEFAULT FREQUENCY |
|---|---|---|---|
| IC1 | AMI or CMOS/TTL(3) | 64kHz composite clock or up to 125MHz | 8kHz |
| IC2 | AMI or CMOS/TTL(3) | 64kHz composite clock or up to 125MHz | 8kHz |
| IC3 | CMOS/TTL | Up to 125MHz(1) | 8kHz |
| IC4 | CMOS/TTL | Up to 125MHz | 8kHz |
| IC5 | LVDS/LVPECL or CMOS/TTL | Up to 155.52MHz(2) | 19.44MHz |
| IC6 | LVDS/LVPECL or CMOS/TTL | Up to 155.52MHz | 19.44MHz |
| IC7 | CMOS/TTL | Up to 125MHz | 19.44MHz |
| IC8 | CMOS/TTL | Up to 125MHz | 19.44MHz |
| IC9 | CMOS/TTL | Up to 125MHz | 19.44MHz |
| IC10 | CMOS/TTL | Up to 125MHz | 19.44MHz |
| IC11 | CMOS/TTL | Up to 125MHz | Master mode (MASTSLV = 1): 19.44MHz<br>Slave mode (MASTSLV = 0): 6.48MHz |
| IC12 | CMOS/TTL | Up to 125MHz | SONET mode (SONSDH = 1): 1.544MHz<br>SDH mode (SONSDH = 0): 2.048MHz |
| IC13 | CMOS/TTL | Up to 125MHz | SONET mode (SONSDH = 1): 1.544MHz<br>SDH mode (SONSDH = 0): 2.048MHz |
| IC14 | CMOS/TTL | Up to 125MHz | SONET mode (SONSDH = 1): 1.544MHz<br>SDH mode (SONSDH = 0): 2.048MHz |

**Note 1:** Available frequencies for CMOS/TTL input clocks are 2kHz, 4kHz, 8kHz, 1.544MHz (SONET mode), 2.048MHz (SDH mode), 6.312MHz, 6.48MHz, 19.44MHz, 25.92MHz, 38.88MHz, 51.84MHz, 77.76MHz, and N x 8kHz for $2 \le N \le 15{,}625$.

**Note 2:** Available frequencies for LVDS/LVPECL input clocks include all CMOS/TTL frequencies in Note 1 plus 155.52MHz.

**Note 3:** Signal formats for IC1 and IC2 are controlled by MCR5:IC1SF and IC2SF, respectively.

### 7.4.2 Frequency Configuration

Input clock frequencies are configured in the FREQ field of the ICR registers. The DIVN and LOCK8K bits of these same registers specify the locking frequency mode, as shown in Table 7-3.

## Table 7-3. Locking Frequency Modes

| DIVN | LOCK8K | LOCKING FREQUENCY MODE |
|---|---|---|
| 0 | 0 | Direct lock mode |
| 0 | 1 | LOCK8K mode |
| 1 | X | DIVN mode |

#### 7.4.2.1 Direct Lock Mode

In direct lock mode, the DPLLs lock to the selected reference at the frequency specified in the corresponding ICR register. Direct lock mode can only be used for input clocks with these specific frequencies: 2kHz, 4kHz, 8kHz, 1.544MHz, 2.048MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.92MHz, 38.88MHz, 51.84MHz, 77.76MHz, and 155.52MHz. For the 155.52MHz case, the input clock is internally divided by two, and the DPLL direct-locks at 77.76 MHz.

The T0 DPLL can direct-lock to all the specific input frequencies listed above, and so can the T4 DPLL when configured for 77.76MHz operation (see Section 7.8.2.2). When configured for *non*-77.76MHz operation, the T4 DPLL can direct-lock to any of the specific frequencies listed above from 2kHz to 6.48MHz, but for the specific frequencies of 19.44MHz and higher, the input must be configured for LOCK8K or DIVN mode.

MTIE may be somewhat lower in direct lock mode because the higher frequencies allow more frequent phase updates.

#### 7.4.2.2 LOCK8K Mode

In LOCK8K mode, an internal divider is configured to divide the selected reference down to 8kHz. The DPLLs lock to the 8kHz output of the divider. LOCK8K mode can only be used for input clocks with these frequencies: 8kHz, 1.544MHz, 2.048MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.92MHz, 38.88MHz, 51.84MHz, 77.76MHz, and 155.52MHz. LOCK8K mode is enabled for a particular input clock by setting the LOCK8K bit in the corresponding ICR register. LOCK8K mode gives a greater tolerance to input jitter because it uses lower frequencies for phase comparisons. The clock edge to lock to on the selected reference can be configured using the 8KPOL bit in the TEST1 register. For 2kHz and 4kHz clocks, the LOCK8K bit is ignored and direct-lock mode is used.

#### 7.4.2.3 DIVN Mode

In DIVN mode, the internal divider is configured from the value stored in the DIVN registers. The DIVN value must be chosen so that when the selected reference is divided by DIVN+1 the output clock is 8kHz. The DPLLs lock to the 8kHz output of the divider. DIVN mode can only be used for input clocks whose frequency is an integer multiple of 8 kHz and less than or equal to 155.52MHz. The DIVN register field can range from 1 to 19,439 inclusive. The same DIVN+1 factor is used for all input clocks configured for DIVN mode. When DIVN = 1 in an ICR register, the FREQ field of that register is ignored. Note that although DIVN divider is able to divide down clock rates has as high as 155.52MHz (DIVN = 19,439), the CMOS/TTL inputs are only rated for a maximum clock rate of 125MHz (DIVN = 15,624).

## 7.5 Input Clock Quality Monitoring

Each input clock is continuously monitored for frequency accuracy and activity. Frequency monitoring is described in Section 7.5.1, while activity monitoring is described in Sections 7.5.2 and 7.5.3. Any input clock that has a frequency out-of-band alarm or activity alarm is automatically declared invalid. The valid/invalid state of each input clock is reported in the corresponding real-time status bit in register VALSR1 or VALSR2. When the valid/invalid state of a clock changes, the corresponding latched status bit is set in register MSR1 or MSR2, and an interrupt request occurs if the corresponding interrupt enable bit is set in registers IER1 or IER2. Input clocks marked invalid cannot be selected as the reference for either DPLL. If the T4 DPLL does not have any valid input clocks available, the T4NOIN status bit is set to 1 in MSR3.

### 7.5.1 Frequency Monitoring

The DS3101 monitors the frequency of each input clock and invalidates any clock whose frequency is outside of specified limits. Two frequency limits can be specified: a soft limit and a hard limit. For all input clocks except the T0 DPLL's selected reference, these limits are specified in the ILIMIT register. For the T0 DPLL's selected reference the limits are specified in the SRLIMIT register. When the frequency of an input clock is greater than or equal to the soft limit, the corresponding SOFT alarm bit is set to 1 in the ISR registers. The soft limit is only for monitoring; triggering it does not invalidate the clock. When the frequency of an input clock is greater than or equal to the hard limit, the corresponding HARD alarm bit is set to 1 in the ISR registers, and the clock is marked invalid in the VALSR registers. Monitoring according to the hard and soft limits is enabled/disabled using the HARDEN and SOFTEN bits in the MCR10 register. Both the ILIMIT and SRLIMIT registers have a default soft limit of ±11.43ppm and a default hard limit of ±15.24ppm. Limits can be set from ±3.81ppm to ±60.96ppm in 3.81ppm steps. Both the SOFT and HARD alarm limits have hysteresis as required by GR-1244. Frequency monitoring is only done on an input clock when the clock does not have an activity alarm.

Frequency measurement can be done with respect to the internal 204.8MHz master clock or the 77.76MHz T0 DPLL output, as specified by the FMONCLK bit in MCR10. Measured frequency can be read from any frequency monitor by specifying the input clock in the FMEASIN field of MCR11 and reading the frequency from the FMEAS register.

### 7.5.2 Activity Monitoring

Each input clock is monitored for activity and proper behavior using a leaky bucket accumulator. A leaky bucket accumulator is similar to an analog integrator: the output amplitude increases in the presence of input events and gradually decays in the absence of events. When events occur infrequently, the accumulator value decays fully between events and no alarm is declared. When events occur close enough together, the accumulator increments faster than it can decay and eventually reaches the alarm threshold. After an alarm has been declared, if events occur infrequently enough, the accumulator can decay faster than it is incremented and eventually reaches the alarm clear threshold.

The leaky bucket accumulator for each input clock can be assigned one of four configurations (0 through 3) in the BUCKET field of the ICR registers. Each leaky bucket configuration has programmable size, alarm declare threshold, alarm clear threshold, and decay rate, all of which are specified in the LBxy registers at addresses 50h through 5Fh.

Activity monitoring is divided into 128ms intervals. The accumulator is incremented once for each 128ms interval in which the input clock is inactive for more than two cycles (more than four cycles for 155.52MHz input clocks). Thus the "fill" rate of the bucket is at most 1 unit per 128ms, or approximately 8 units/second. During each period of 1, 2, 4 or 8 intervals (programmable), the accumulator decrements if no irregularities occur. Thus the "leak" rate of the bucket is approximately 8, 4, 2, or 1 units/second. A leak is prevented when a fill event occurs in the same interval.

When the value of an accumulator reaches the alarm threshold (LBxU register), the corresponding ACT alarm bit is set to 1 in the ISR registers, and the clock is marked invalid in the VALSR registers. When the value of an accumulator reaches the alarm clear threshold (LBxL register), the activity alarm is cleared by clearing the clock's ACT bit. The accumulator cannot increment past the size of the bucket specified in the LBxS register. The decay rate of the accumulator is specified in the LBxD register. The values stored in the leaky bucket configuration registers must have the following relationship at all times: LBxS ≥ LBxU > LBxL.

When the leaky bucket is empty, the minimum time to declare an activity alarm in seconds is LBxU / 8 (where the "x" in "LbxU" is the leaky bucket configuration number, 0 to 3). The minimum time to clear an activity alarm in seconds is [$2^{LBxD}$ x (LBxS - LBxL) / 8]. For example, assume LBxU = 8, LBxL = 1, LBxS = 10, and LBxD = 0. The minimum time to declare an activity alarm would be 8 / 8 = 1 second. The minimum time to clear the activity alarm would be [$2^0$ x (10 - 1) / 8 = 1.125 seconds].

For input clocks IC1 and IC2 configured in composite clock mode, if MCR5:BITERR = 1, then the accumulator is also incremented whenever a violation of the one-BPV-in-eight pattern is detected.

### 7.5.3 Selected Reference Activity Monitoring

The input clock that each DPLL is currently locked to is called the selected reference. The quality of a DPLL's selected reference is exceedingly important, since missing cycles and other anomalies on the selected reference can cause unwanted jitter, wander or frequency offset on the output clocks. When anomalies occur on the selected reference they must be detected as soon as possible to give the DPLL opportunity to temporarily disconnect from the reference until the reference is available again. By design, the regular input clock activity monitor (Section 7.5.2) is too slow to be suitable for monitoring the selected reference. Instead, each DPLL has its own fast activity monitor that detects inactivity within approximately two missing reference clock cycles (within approximately four missing cycles for 155.52MHz references).

When the T0 DPLL detects a no-activity event, it immediately enters mini-holdover mode to isolate itself from the selected reference and sets the SRFAIL bit in MSR2. The setting of the SRFAIL bit can cause an interrupt request on the INTREQ pin if the corresponding enable bit is set in IER2. If MCR10:SRFPIN = 1, the SRFAIL output pin follows the state of the SRFAIL status bit. Optionally, a no-activity event can also cause an ultra-fast reference switch (see Section 7.6.4). When PHLIM1:NALOL = 0 (default), the T0 DPLL does not declare loss-of-lock during no-activity events. If the selected reference becomes available again before any alarms are declared by the activity monitor or frequency monitor, then the T0 DPLL continues to track the selected reference using nearest-edge locking (±180°) to avoid cycle slips. When NALOL = 1, the T0 DPLL declares loss-of-lock during no-activity events. This causes the T0 state machine to transition to the loss-of-lock state, which sets the MSR2:STATE bit and causes an interrupt request if enabled. If the selected reference becomes available again before any alarms are declared by the activity monitor or frequency monitor, then the T0 DPLL tracks the selected reference using phase/frequency locking (±360°) until phase lock is reestablished.

When the T4 DPLL detects a no-activity event, its behavior is similar to the T0 DPLL with respect to the PHLIM1:NALOL control bit. Unlike the T0 DPLL, however, the T4 DPLL does not set the SRFAIL status bit. If NALOL = 1, the T4 DPLL clears the OPSTATE:T4LOCK status bit, which sets MSR3:T4LOCK and causes an interrupt request if enabled.

### 7.5.4 Composite Clock Inputs

When input clocks IC1 and IC2 are configured for composite clock mode (MCR5:IC1SF = 0 and MCR5:IC2SF = 0), they are also monitored for various defects (AMI error, LOS, etc.) See Section 7.10.1 for further details.

## 7.6 Input Clock Priority, Selection, and Switching

### 7.6.1 Priority Configuration

During normal operation, the selected reference for the T0 DPLL and the selected reference for the T4 DPLL are chosen automatically based on the priority rankings assigned to the input clocks in the input priority registers (IPR1 to IPR7). Each of these seven registers has priority fields for two input clocks. When T4T0 = 0 in the MCR11 register, the IPR registers specify the input clock priorities for the T0 DPLL. When T4T0 = 1, the IPR registers specify the input clock priorities for the T4 DPLL. The default input clock priorities, for both PLLs, are shown in Table 7-4.

Any unused input clock should be given the priority value 0, which disables the clock and marks it as unavailable for selection. Priority 1 is highest while priority 15 is lowest. The same priority can be given to two or more clocks.

**Table 7-4. Default Input Clock Priorities**

| INPUT CLOCK | DEFAULT PRIORITY |
|---|---|
| IC1 | 2 |
| IC2 | 3 |
| IC3 | 4 |
| IC4 | 5 |
| IC5 | 6 |
| IC6 | 7 |
| IC7 | 8 |

| INPUT CLOCK | DEFAULT PRIORITY |
|---|---|
| IC8 | 9 |
| IC9 | 10 |
| IC10 | 11 |
| IC11 | 12 or 1 (1) |
| IC12 | 13 |
| IC13 | 14 |
| IC14 | 15 |

**Note 1:** During reset, the default priority for IC11 is set to 12 in the master device and set to 1 in the slave device. Devices are configured as master and slave by the value of the MASTSLV pin. (The state of the MASTSLV pin is mirrored in the MASTSLV bit of the MCR3 register.) See Section 7.9.

### 7.6.2 Automatic Selection Algorithm

The real-time valid/invalid state of each input clock is maintained in the VALSR1 and VALSR2 registers. The selected reference can be marked invalid for phase, frequency or activity. Other input clocks can be invalidated for frequency or activity.

The reference selection algorithm for each DPLL chooses the highest-priority valid input clock to be the selected reference. To select the proper input clock based on these criteria, the selection algorithm maintains a priority table of valid inputs. The top three entries in this table and the selected reference are displayed in the PTAB1 and PTAB2 registers. When T4T0 = 0 in the MCR11 register, these registers indicate the highest priority input clocks for the T0 DPLL. When T4T0 = 1, they indicate the highest priority input clocks for the T4 path.

If two or more input clocks are given the same priority number then those inputs are prioritized among themselves using a fixed circular list. If one equal-priority clock is the selected reference but becomes invalid then the next equal-priority clock in the list becomes the selected reference. If an equal-priority clock that is not the selected reference becomes invalid, it is simply skipped over in the circular list. The selection among equal-priority inputs is inherently nonrevertive, and revertive switching mode (see next paragraph) has no effect in the case where multiple equal-priority inputs have the highest priority.

An important input to the selection algorithm for T0 DPLL is the REVERT bit in the MCR3 register. In revertive mode (REVERT = 1), if an input clock with a higher priority than the selected reference becomes valid, the higher-priority reference immediately becomes the selected reference. In nonrevertive mode (REVERT = 0), the higher-priority reference does not immediately become the selected reference but does become the highest-priority reference in the priority table (REF1 field in the PTAB1 register). (The selection algorithm always switches to the highest-priority valid input when the selected reference goes invalid, regardless of the state of the REVERT bit.) For many applications, nonrevertive mode is preferred for the T0 DPLL because it minimizes disturbances on the output clocks due to reference switching. The T4 DPLL always operates in revertive mode.

In nonrevertive mode, planned switchover to a newly valid higher priority input clock can be done manually under software control. The validation of the new higher priority clock sets the corresponding status bit in the MSR1 or

MSR2 register, which can drive an interrupt request on the INTREQ pin if needed. System software can then respond to this change of state by briefly enabling revertive mode (toggling REVERT high then back low) to drive the switchover to the higher priority clock.

In most systems redundant timing cards are required, with one functioning as the master and the other as the slave. In such systems the priority tables of the master and slave must match. The DS3101's register set makes it easy for the slave's priority table to track the master's table. At system start-up, the same priorities must be assigned to the input clocks, for both DPLLs, in the master and slave devices. During operation, if an input clock becomes valid or invalid in one device (master or slave), the change is flagged in that device's MSR1 or MSR2 register, which can drive an interrupt request on the INTREQ pin if needed. The real-time valid/invalid state of the input clocks can then be read from that device's VALSR1 and VALSR2 registers. Once the nature of the state change is understood, the control bits of the other device's VALCR1 and VALCR2 registers can be manipulated to mark clocks invalid in the other device as well.

### 7.6.3 Forced Selection

The T0FORCE field in the MCR2 register and the T4FORCE field in the MCR4 register provide a way to force a specified input clock to be the selected reference for the T0 and T4 DPLLs, respectively. In both T0FORCE and T4FORCE, values of 0 and 15 specify normal operation with automatic reference selection. Values from 1 to 14 specify the input clock to be the forced selection. Internally forcing is accomplished by giving the specified clock the highest priority (as specified in PTAB1:REF1). In revertive mode (MCR3:REVERT = 1) the forced clock automatically becomes the selected reference (as specified in PTAB1:SELREF) as well. In nonrevertive mode (T0 DPLL only) the forced clock only becomes the selected reference when the existing selected reference is invalidated or made unavailable for selection. In both revertive and nonrevertive modes when an input is forced to be the highest priority, the normal highest priority input (when no input is forced) is listed as the second-highest priority (PTAB2:REF2) and the normal second-highest priority input is listed as the third-highest priority (PTAB2:REF3).

### 7.6.4 Ultra-Fast Reference Switching

By default, disqualification of the selected reference and switchover to another reference occurs when the activity monitor's inactivity alarm threshold has been crossed, a process that takes on the order of hundreds of milliseconds or seconds. For the T0 DPLL, an option for extremely fast disqualification and switchover is also available. When ultra-fast switching is enabled (MCR10:UFSW = 1), if the fast activity monitor detects approximately two missing clock cycles it declares the reference failed by forcing the leaky bucket accumulator to its upper threshold (see Section 7.5.2) and initiates reference switching. This is in addition to setting the SRFAIL bit in MSR2 and optionally generating an interrupt request, as described in Section 7.5.3. When ultra-fast switching occurs, the T0 DPLL transitions to the prelocked 2 state, which allows switching to occur faster by bypassing the Loss-of-Lock state. The device should be in non-revertive mode when ultra-fast switching is enabled. If the device is in revertive mode, ultra-fast switching could cause excessive reference switching when the highest priority input is intermittent.

### 7.6.5 External Reference Switching Mode

In the external reference switching mode, the SRCSW input pin controls reference switching between two clock inputs. This mode is enabled by setting the EXTSW bit to 1 in the MCR10 register. In this mode, if the SRCSW pin is high, the device is forced to lock to input IC3 (if the priority of IC3 is nonzero in IPR2) or IC5 (if the priority of IC3 is zero) whether or not the selected input has a valid reference signal. If the SRCSW pin is low the device is forced to lock to input IC4 (if the priority of IC4 is non-zero in IPR2) or IC6 (if the priority of IC4 is zero) whether or not the selected input has a valid reference signal. During reset the default value of the EXTSW bit is latched from the SRCSW pin. If external reference switching mode is enabled during reset, the default frequency tolerance (DLIMIT registers) is configured to ±80ppm rather than the normal default of ±9.2ppm.

In external reference switching mode the device is simply a clock switch, and the DPLL is forced to lock onto the selected reference whether it is valid or not. Unlike forced reference selection (Section 7.6.3) this mode controls the PTAB1:SELREF field directly and is therefore not affected by the state of the MCR3:REVERT bit. During external reference switching mode, only PTAB1:SELREF is affected; the REF1, REF2 and REF3 fields in the PTAB registers continue to indicate the highest, second-highest, and third-highest priority valid inputs chosen by the automatic selection logic. External reference switching mode only affects the T0 DPLL.

### 7.6.6 Output Clock Phase Continuity During Reference Switching

If phase build out is enabled (PBOEN = 1 in MCR10) or the DPLL frequency limit (DLIMIT) is set to less than ±30ppm then the device always complies with the GR-1244-CORE requirement that the rate of phase change must be less than 81ns per 1.326ms during reference switching.

## 7.7 DPLL Architecture and Configuration

Both the T0 and T4 paths of the device are digital PLLs (DPLLs) with analog PLLs (APLLs) at the output stage. This architecture combines the benefits of both PLL types.

Digital PLLs have two key benefits: (1) stable, repeatable performance that is insensitive to process variations, temperature and voltage, and (2) flexible behavior that is easily programmed via configuration registers. DPLLs use digital frequency synthesis (DFS) to generate various clocks. In DFS, a high-speed master clock (204.8MHz) is multiplied up from the 12.800MHz local oscillator clock applied to the REFCLK pin. This master clock is then digitally divided down to the desired output frequency. Since the resolution of the DFS process is one master clock cycle or 4.88ns, the DFS output clock has jitter of up to 1 master clock UI (4.88ns) pk-pk.

The analog PLLs filter the jitter from the DPLLs, reducing the 4.88ns pk-pk jitter to 0.5ns pk-pk and 60ps RMS, typical, measured broadband (10Hz to 1GHz).

The DPLLs in the device are configurable for many PLL parameters including bandwidth, damping factor, input frequency, pull-in/hold-in range, loop frequency, output frequency, input-to-output phase offset, phase build-out, and more. No knowledge of loop equations or gain parameters is required to configure and operate the device. No external components are required for the DPLLs or the APLLs except the high-quality local oscillator connected to the REFCLK pin.

The T0 path is the main path through the device, and the T0 DPLL has a full free-run/locked/holdover state machine and full programmability. The T4 path is a simpler frequency converter/synthesis path, lacking the low bandwidth settings, phase build-out, phase adjustment controls, and holdover state found in the T0 DPLL.

### 7.7.1 T0 DPLL State Machine

The T0 DPLL has three main timing modes: locked, holdover, and free-run. The control state machine for the T0 DPLL has states for each timing mode as well as three temporary states: prelocked, prelocked 2, and loss-of-lock. The state transition diagram is shown in Figure 7-1. Descriptions of each state are given in the paragraphs below. During normal operation the state machine controls state transitions. When necessary, however, the state can be forced using the T0STATE field of the MCR1 register.

Whenever the T0 DPLL changes state, the STATE bit in MSR2 is set, which can cause an interrupt request if enabled. The current T0 DPLL state can be read from the T0STATE field of the OPSTATE register.

#### 7.7.1.1 Free-Run State

Free-run mode is the reset default state. In free-run, all output clocks are derived from the 12.800MHz local oscillator attached to the REFCLK pin. The frequency of each output clock is a specific multiple of the local oscillator. The frequency accuracy of each output clock is equal to the frequency accuracy of the master clock (see Section 7.3). The state machine transitions from free-run to the prelocked state when at least one input clock is valid.

#### 7.7.1.2 Prelocked State

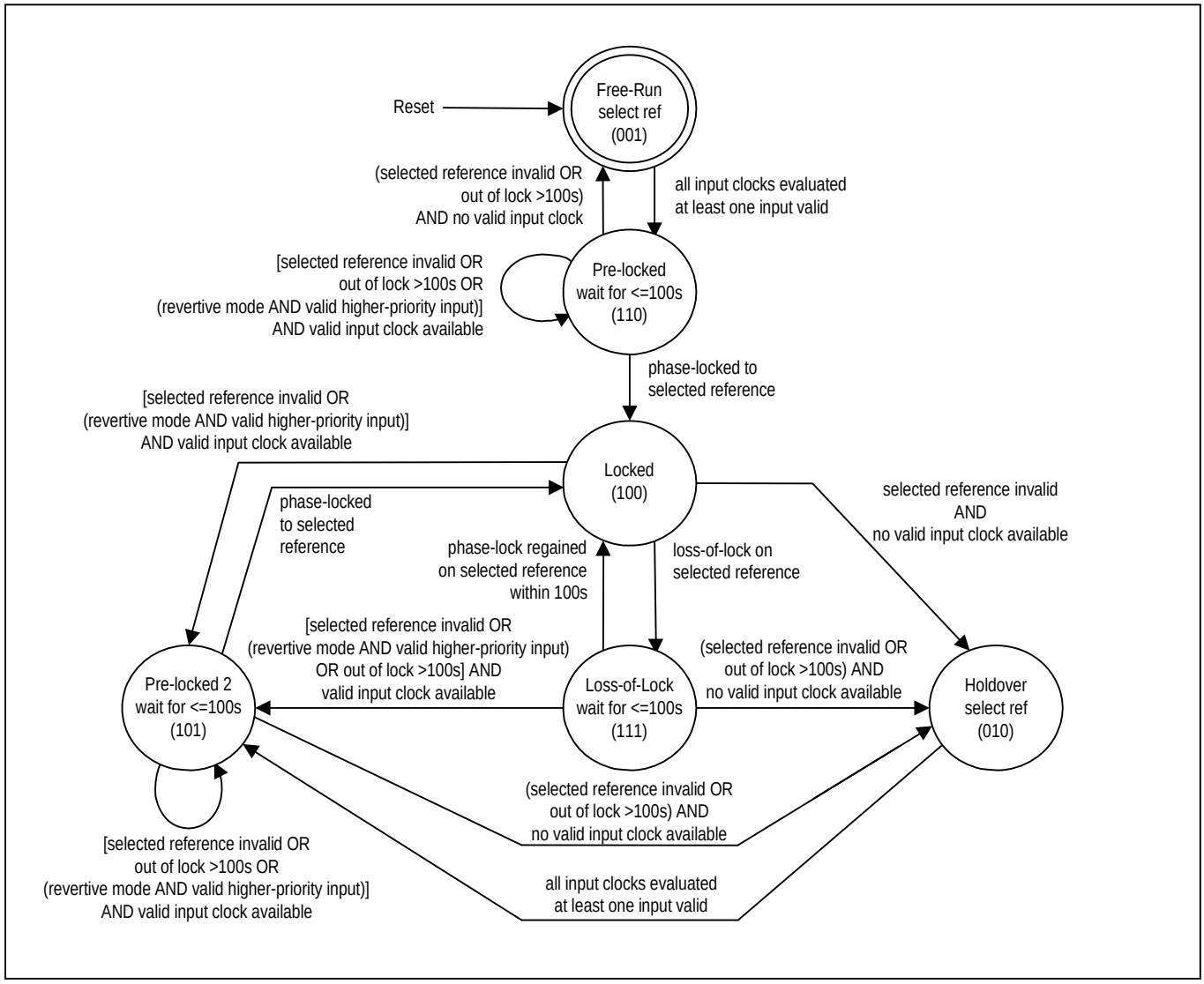
The prelocked state provides a 100-second period (default value of PHLKTO register) for the DPLL to lock to the selected reference. If phase lock is achieved during this period then the state machine transitions to locked mode.

If the DPLL fails to lock to the selected reference within the phase-lock time-out period specified by PHLKTO then a phase lock alarm is raised (corresponding LOCK bit set in the ISR register), invalidating the input (ICn bit goes low in VALSR registers). If another input clock is valid then the state machine re-enters the prelocked state and tries to lock to the alternate input clock. If no other input clocks are valid then the state machine transitions back to the free-run state.

In revertive mode (REVERT = 1 in MCR3), if a higher priority input clock becomes valid during the phase-lock timeout period, then the state machine re-enters the prelocked state and tries to lock the higher priority input. If a

phase-lock timeout period longer than 100 seconds is required for locking (such as 700 seconds for Stratum 3E or 1000 seconds for Stratum 2 applications), the PHLKTO register must be configured accordingly.

## Figure 7-1. T0 DPLL State Transition Diagram




**Note 1:** An input clock is valid when it has no activity alarm, no hard frequency limit alarm, and no phase lock alarm (see the VALSR registers and the ISR registers).

**Note 2:** All input clocks are continuously monitored for activity and frequency.

**Note 3:** Only the selected reference is monitored for loss of lock.

**Note 4:** Phase lock is declared internally when the DPLL has maintained phase lock continuously for approximately 1 to 2 seconds.

**Note 5:** To simply the diagram, the phase-lock timeout period is always shown as 100s, which is the default value of the PHLKTO register. Longer or shorter timeout periods can be specified as needed by writing the appropriate value to the PHLKTO register.

#### 7.7.1.3 Locked State

The T0 DPLL state machine can reach the locked state from the prelocked, prelocked 2, or loss-of-lock states when the DPLL has locked to the selected reference for at least one second (see Section 7.7.6). In the locked state, the output clocks track the phase and frequency of the selected reference.

While in the locked state, if the selected reference is so impaired that an activity alarm or a hard frequency limit alarm is raised (corresponding ACT or HARD bit set in the ISR register), then the selected reference is invalidated (ICn bit goes low in VALSR registers), and the state machine immediately transitions to either the prelocked 2 state (if another valid input clock is available) or the holdover state (if no other input clock is valid).

If loss-of-lock is declared while in the locked state, the state machine transitions to the loss-of-lock state.

#### 7.7.1.4 Loss-of-Lock State

When the loss-of-lock detectors (see Section 7.7.6) indicate loss-of-phase lock, the state machine immediately transitions from the locked state to the loss-of-lock state. In the loss-of-lock state the DPLL tries for 100 seconds (default value of PHLKTO register) to regain phase lock. If phase lock is regained during that period, the state machine transitions back to the locked state.

If, during the phase-lock timeout period specified by PHLKTO, the selected reference is so impaired that an activity alarm or a hard frequency limit alarm is raised (corresponding ACT or HARD bit set in the ISR registers), then the selected reference is invalidated (ICn bit goes low in VALSR registers), and the state machine immediately transitions to either the prelocked 2 state (if another valid input clock is available) or the holdover state (if no other input clock is valid).

If phase lock cannot be regained by the end of the phase-lock timeout period, then a phase lock alarm is raised (corresponding LOCK bit set in the ISR registers), the selected reference is invalidated (ICn bit goes low in VALSR registers), and the state machine transitions to either the prelocked 2 state (if another valid input clock is available) or the holdover state (if no other input clock is valid).

#### 7.7.1.5 Prelocked 2 State

The prelocked and prelocked 2 states are similar. The prelocked 2 state provides a 100-second period (default value of PHLKTO register) for the DPLL to lock to the new selected reference. If phase lock is achieved during this period, then the state machine transitions to locked mode.

If the DPLL fails to lock to the new selected reference within the phase-lock timeout period specified by PHLKTO, then a phase lock alarm is raised (corresponding LOCK bit set in the ISR registers), invalidating the input (ICn bit goes low in VALSR registers). If another input clock is valid, the state machine re-enters the prelocked 2 state and tries to lock to the alternate input clock. If no other input clocks are valid, the state machine transitions to the holdover state.

In revertive mode (REVERT = 1 in MCR3), if a higher priority input clock becomes valid during the phase-lock timeout period, the state machine re-enters the prelocked 2 state and tries to lock to the higher priority input.

If a phase-lock timeout period longer than 100 seconds is required for locking (such as 700 seconds for Stratum 3E or 1000 seconds for Stratum 2 applications), then the PHLKTO register must be configured accordingly.

#### 7.7.1.6 Holdover State

The device reaches the holdover state when it declares its selected reference invalid and has no other valid input clocks available. During holdover the T0 DPLL is not phase locked to any input clock but instead generates its output frequency from stored frequency information, typically the averaged frequency of the DPLL when it was in the locked state. The device can be configured for manual or automatic holdover as described in the following subsections. When at least one input clock has been declared valid the state machine immediately transitions from holdover to the prelocked 2 state and tries to lock to the highest priority valid clock.

##### 7.7.1.6.1 Automatic Holdover

For automatic holdover (MANHO = 0 in MCR3), the device can be further configured for instantaneous mode or averaged mode. In *instantaneous mode* (AVG = 0 in HOCR3), the holdover frequency is set to the DPLL's current frequency at the moment of entry into holdover (i.e., the value of the FREQ field in the FREQ1, FREQ2 and FREQ3 registers when MCR11:T4T0 = 0). The FREQ field is the DPLL's integral path and therefore is an average

frequency with a rate of change inversely proportional to the DPLL bandwidth. The DPLL's proportional path is not used to minimize the effect of recent phase disturbances on the holdover frequency.

In *averaged mode* (AVG = 1 in HOCR3), the holdover frequency is set to an internally averaged value. During locked operation the frequency indicated in the FREQ field is internally averaged. The FAST bit in HOCR3 determines the period of this averaging. When FAST = 1 the frequency is averaged for a period of approximately 8 minutes. When FAST = 0 (slow), the frequency is averaged for a period of approximately 110 minutes. The T0 DPLL indicates that it has acquired valid holdover values by setting the FHORDY and SHORDY status bits in VALSR2 (real-time status) and MSR4 (latched status). If FAST = 0 and the T0 DPLL must enter holdover before the 110-minute average is available, then the 8-minute average is used, if available. Otherwise the instantaneous value from the integral path is used. If FAST = 1 and the T0 DPLL must enter holdover before the 8-minute average is available, then the instantaneous value is used.

#### 7.7.1.6.2 Manual Holdover

For *manual holdover* (MANHO = 1 in MCR3), the holdover frequency is set by the HOFREQ field in the HOCR1, HOCR2 and HOCR3 registers. The HOFREQ field has the same size and format as the current frequency field (FREQ[18:0] in the FREQ1, FREQ2, and FREQ3 registers). If desired, software can, during locked operation, read the current frequency from FREQ, filter or average it over time, and then write the resulting holdover frequency to HOFREQ. The FREQ field is derived from the DPLL's integral path, and thus can be considered an average frequency with a rate of change inversely proportional to the DPLL bandwidth.

To combine internal averaging with additional software filtering, the HOFREQ field can be configured to read out the internally averaged frequency when RDAVG = 1 in the HOCR3 register. This averaged value can be read from HOFREQ regardless of the current holdover mode. The FAST bit in HOCR3 specifies whether the value read is from the fast averager or the slow averager.

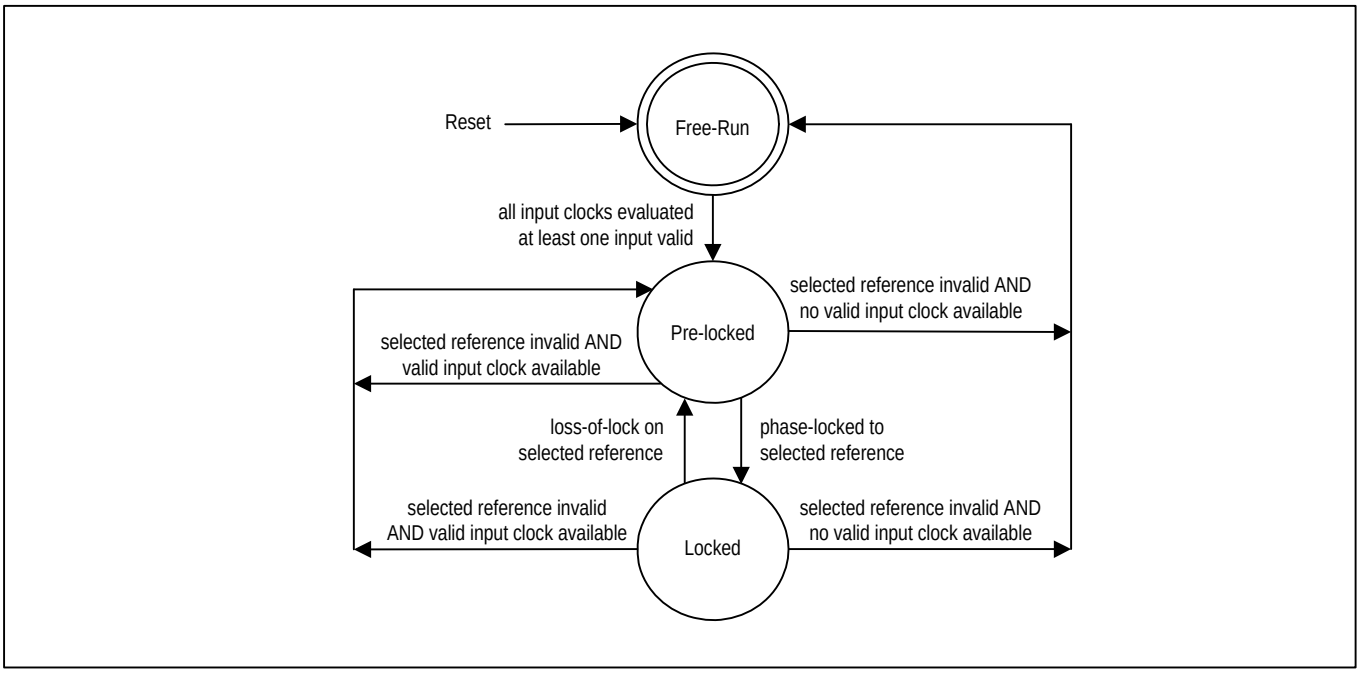
#### 7.7.1.7 Mini-Holdover

When the selected reference fails, the fast activity monitor (Section 7.5.3) isolates the T0 DPLL from the reference within one or two clock cycles to avoid adverse effects on the DPLL frequency. When this fast isolation occurs, the DPLL enters mini-holdover mode, with a mini-holdover frequency as specified by the MINIHO field of HOCR3. Mini-holdover lasts until the selected reference returns or a new input clock has been chosen as the selected reference or the state machine enters the holdover state. Note that when the T0 DPLL is configured for manual holdover (MCR3:MANHO = 1), mini-holdover is also configured for manual holdover and HOCR3:MINIHO is ignored.

### 7.7.2 T4 DPLL State Machine

The T4 DPLL has a simpler state machine than the T0 DPLL, as shown in Figure 7-2. The T4 DPLL states are similar to the equivalent states of the T0 DPLL. Note that the T4 DPLL only operates in revertive switching mode.

**Figure 7-2. T4 DPLL State Transition Diagram**




### 7.7.3 Bandwidth

The bandwidth of the T4 DPLL is configured in the T4BW register to be 18Hz, 35Hz, or 70Hz. This bandwidth value is used for both acquisition and locked mode.

The bandwidth of the T0 DPLL is configured in the T0ABW and T0LBW registers for various values from 0.5mHz to 70Hz. The AUTOBW bit in the MCR9 register controls automatic bandwidth selection. When AUTOBW = 1, the T0 DPLL uses the T0ABW bandwidth during acquisition (not phase locked) and the T0LBW bandwidth when phase locked. When AUTOBW = 0 the T0 DPLL uses the T0LBW bandwidth all the time, both during acquisition and when phase locked.

When LIMINT = 1 in the MCR9 register, the DPLL's integral path is limited (i.e., frozen) when the DPLL reaches minimum or maximum frequency. Setting LIMINT = 1 minimizes overshoot when the DPLL is pulling in.

### 7.7.4 Damping Factor

The damping factor for the T0 DPLL is configured in the DAMP field of the T0CR2 register, while the damping factor the T4 DPLL is configured in the DAMP field of the T4CR2 register. The reset default damping factors for both DPLLs are chosen to give a maximum wander gain peak of approximately 0.1dB. Available settings are a function of DPLL bandwidth (configured in the T4BW, T0ABW, and T0LBW registers). See Table 7-5.

## Table 7-5. Damping Factors and Peak Jitter/Wander Gain

| BANDWIDTH | DAMP[2:0] VALUE | DAMPING FACTOR | GAIN PEAK (dB) |
|---|---|---|---|
| 0.5mHz to 4Hz | 1, 2, 3, 4, 5 | 5 | 0.1 |
| 8Hz | 1 | 2.5 | 0.2 |
| | 2, 3, 4, 5 | 5 | 0.1 |
| 18 Hz | 1 | 1.2 | 0.4 |
| | 2 | 2.5 | 0.2 |
| | 3, 4, 5 | 5 | 0.1 |
| 35 Hz | 1 | 1.2 | 0.4 |
| | 2 | 2.5 | 0.2 |
| | 3 | 5 | 0.1 |
| | 4, 5 | 10 | 0.06 |
| 70 Hz | 1 | 1.2 | 0.4 |
| | 2 | 2.5 | 0.2 |
| | 3 | 5 | 0.1 |
| | 4 | 10 | 0.06 |
| | 5 | 20 | 0.03 |

### 7.7.5 Phase Detectors

Phase detectors are used to compare a PLL's feedback clock with its input clock. Several phase detectors are available in both the T0 and T4 DPLLs:

- Phase/frequency detector (PFD)
- Early/late phase detector (PD2) for fine resolution
- Multicycle phase detector (MCPD) for large input jitter tolerance

These detectors can be used in combination to give fine phase resolution combined with large jitter tolerance. As with the rest of the DPLL logic, the phase detectors operate at input frequencies up to 77.76MHz. The multicycle phase detector detects and remembers phase differences of many cycles (up to 8191UI).

The phase detectors can be configured for normal phase/frequency locking (±360° capture) or nearest-edge phase locking (±180° capture). With nearest-edge detection the phase detectors are immune to occasional missing clock cycles. The DPLL automatically switches to nearest-edge locking when the multicycle phase detector is disabled and the other phase detectors determine that phase lock has been achieved. Setting D180 = 1 in the TEST1 register disables nearest-edge locking and forces the DPLL to use phase/frequency locking.

The early/late phase detector, also known as phase detector 2, is enabled and configured in the PD2* fields of registers T0CR2 and T0CR3 for the T0 DPLL and registers T4CR2 and T4CR3 for the T4 DPLL. The reset default settings of these registers are appropriate for all operating modes. Adjustments only affect small signal overshoot and bandwidth.

The multicycle phase detector is enabled by setting MCPDEN = 1 in the PHLIM2 register. The range of the MCPD—from ±1UI up to ±8191UI—is configured in the COARSELIM field of PHLIM2. The MCPD tracks phase position over many clock cycles, giving high jitter tolerance. Thus the use of the MCPD is an alternative to the use of LOCK8K mode for jitter tolerance.

When USEMCPD = 1 in PHLIM2, the MCPD is used in the DPLL loop, giving faster pull-in but more overshoot. In this mode the loop has similar behavior to LOCK8K mode. In both cases large phase differences contribute to the dynamics of the loop. When enabled by MCPDEN = 1, the MCPD tracks the phase position whether or not it is used in the DPLL loop.

### 7.7.6 Loss of Phase Lock Detection

Loss of phase lock is triggered by any of the following in both the T0 and T4 DPLLs:

- The fine phase lock detector (measures phase between input and feedback clocks)
- The coarse phase lock detector (measures whole cycle slips)
- Hard frequency limit detector
- Inactivity detector

The fine phase lock detector is enabled by setting FLEN = 1 in the PHLIM1 register. The fine phase limit is configured in the FINELIM field of PHLIM1.

The coarse phase lock detector is enabled by setting CLEN = 1 in the PHLIM2 register. The coarse phase limit is configured in the COARSELIM field of PHLIM2. This coarse phase lock detector is part of the multicycle phase detector (MCPD) described in Section 7.7.5. the COARSELIM fields sets both the MCPD range and the coarse phase limit, since the two are equivalent. If loss of phase lock should not be declared for multiple-UI input jitter then the fine phase lock detector should be disabled and the coarse phase lock detector should be used instead.

The hard frequency limit detector is enabled by setting FLLOL = 1 in the DLIMIT3 register. The hard limit for the T0 DPLL is configured in registers DLIMIT1 and DLIMIT2. The T4 DPLL hard limit is fixed at ±80ppm. When the DPLL frequency reaches the hard limit, loss-of-lock is declared. The DLIMIT3 register also has the SOFTLIM field to specify a soft frequency limit. Exceeding the soft frequency limit does not cause loss-of-lock to be declared. When the T0 DPLL frequency exceeds the soft limit the T0SOFT status bit is set in the OPSTATE register. When the T4 DPLL frequency exceeds the soft limit the T4SOFT status bit is set in OPSTATE. Both the SOFT and HARD alarm limits have hysteresis as required by GR-1244.

The inactivity detector is enabled by setting NALOL = 1 in the PHLIM1 register. When this detector is enabled the DPLL declares loss-of-lock after one or two missing clock cycles on the selected reference. See Section 7.5.3.

When the T0 DPLL declares loss of phase lock, the state machine immediately transitions to the loss-of-lock state, which sets the STATE bit in the MSR2 register and requests an interrupt if enabled.

When the T4 DPLL declares loss of phase lock, the T4LOCK bit is cleared in the OPSTATE register, which sets the T4LOCK bit in the MSR3 register and requests an interrupt if enabled.

### 7.7.7 Phase Monitor and Phase Build-Out

#### 7.7.7.1 Phase Monitor

The T0 DPLL has a phase monitor that measures the phase error between the input clock reference and the DPLL output. The phase monitor is enabled by setting PHMON:PMEN = 1. When the T0 DPLL is set for low bandwidth, a phase transient on the input causes an immediate phase error that is gradually reduced as the DPLL tracks the input. When the measured phase error exceeds the limit set in the PHMON:PMLIM field, the phase monitor declares a phase monitor alarm by setting the MSR3:PHMON bit. The PMLIM field can be configured for a limit ranging from about 1µs to about 3.5µs.

#### 7.7.7.2 Phase Build-Out in Response to Input Phase Transients

See Telcordia GR-1244-CORE Section 5.7 for an explanation of phase build-out (PBO) and the requirement for stratum 2 and 3E clocks to perform PBO in response to input phase transients.

When the phase monitor is enabled (as described in Section 7.7.7.1) and PHMON:PMPBEN = 1, the T0 DPLL automatically triggers PBO events in response to input transients greater than the limit set in PHMON:PMLIM. The range of limits available in the PMLIM field allows the T0 DPLL to be configured to build out input transients greater than 3.5µs, greater than 1µs, or any threshold in between.

To determine when to perform PBO, the phase monitor watches for phase changes greater than 100ns in a 10ms interval on the selected reference. When such a phase change occurs, an internal 0.1 second timer is started. If during this interval the phase change is greater than the PMLIM threshold then a PBO event occurs. During a PBO event the device enters a temporary holdover state in which the phase difference between the selected reference and the output is measured and fed into the DPLL loop to absorb the input transient. After a PBO event, regardless of the input phase transient, the output phase transient is less than or equal to 5ns. Phase build-out can be frozen at the current phase offset by setting MCR10:PBOFRZ = 1. When PBO is frozen the T0 DPLL ignores subsequent phase build-out events and maintains the current phase offset between input and outputs.

#### 7.7.7.3 Phase Build-Out in Response to Reference Switching

When MCR10:PBOEN = 0, phase build-out is not performed during reference switching, and the T0 DPLL always locks to the selected reference at zero degrees of phase. With PBO disabled, transitions from a failed reference to the next highest priority reference and transitions from holdover or free-run to locked mode cause phase transients on output clocks as the T0 DPLL jumps from its previous phase to the phase of the new selected reference.

When MCR10:PBOEN = 1, phase build-out is performed during reference switching. With PBO enabled, if the selected reference fails and another valid reference is available then the device enters a temporary holdover state in which the phase difference between the new reference and the output is measured and fed into the DPLL loop to absorb the input phase difference. Similarly, during transitions from holdover or free-run to locked mode, the phase difference between the new reference and the output is measured and fed into the DPLL loop to absorb the input phase difference. After a PBO event, regardless of the input phase difference, the output phase transient is less than or equal to 5ns.

Any time that PBO is enabled it can also be frozen at the current phase offset by setting MCR10:PBOFRZ = 1. When PBO is frozen the T0 DPLL ignores subsequent phase build-out events and maintains the current phase offset between inputs and outputs.

Disabling PBO while the T0 DPLL is in the locked state causes a phase change on the output clocks while the DPLL switches to tracking the selected reference with 0 degrees of phase error. The rate of phase change on the output clocks depends on the DPLL bandwidth. Enabling PBO in the locked state also causes a PBO event.

#### 7.7.7.4 Manual Phase Build-Out Control

Software can have manual control over phase build-out, if required. Initial configuration for manual PBO involves locking to an input clock with frequency ≥ 6.48MHz, setting MCR10:PBOEN = 0 and PHMON:PMPBEN = 0 to disable automatic phase build-out, and setting PHMON:PMEN = 1 and the proper phase limit in PHMON:PMLIM to enable monitoring for a phase transient.

During operation, software can monitor for either a phase transient (MSR3:PHMON = 1) or a T0 DPLL state change (MSR2:STATE = 1). When either event occurs, software can perform the following procedure to execute a manual phase build-out (PBO) event:

1) Read the phase offset from the PHASE registers to decide whether or not to initiate a PBO event.
2) If a PBO event is desired then save the phase offset and set MCR10:PBOEN to cause a PBO event.
3) When the PBO event is complete (wait for a timeout and/or PHASE = 0), write the manual phase offset registers (OFFSET) with the phase offset read earlier. (**Note:** the PHASE register is in degrees, the OFFSET register is in picoseconds)
4) Clear MCR10:PBOEN and wait for the next event that may need a manual PBO.

#### 7.7.7.5 PBO Phase Offset

An uncertainty of up to 5ns is introduced each time a phase build-out event occurs. This uncertainty results in a phase hit on the output. Over a large number of phase build-out events the mean error should be zero. The PBOFF register specifies a small fixed offset for each phase build-out event to skew the average error toward zero and eliminate accumulation of phase shifts in one direction.

### 7.7.8 Input to Output Phase Adjustment

When phase build-out is disabled (PBOEN = 0 in MCR10 and PMPBEN = 0 in PHMON), the OFFSET registers can be used to adjust the phase of the T0 DPLL output clocks with respect to the selected reference. Output phase offset can be adjusted over a ±200ns range in 6ps increments. This phase adjustment occurs in the feedback clock so that the output clocks are adjusted to compensate. The rate of change is therefore a function of DPLL bandwidth. To quickly track large changes in phase, either LOCK8K mode (Section 7.4.2.2) or the coarse phase detector (Section 7.7.5) should be used. Simply writing to the OFFSET registers with phase build-out disabled causes a change in the input to output phase which can be considered to be a delay adjustment.

### 7.7.9 Phase Recalibration

When a phase build-out occurs, either automatic or manual, the feedback frequency synthesizer does not get an internal alignment signal to keep it aligned with the output dividers, and therefore the phase difference between input and output may become incorrect. This could occur if there is a power supply glitch or EMI event that affects the sequential logic state machines. Setting the FSCR3:RECAL bit periodically causes a recalibration process to be executed, which corrects any phase error that may have occurred.

During the recalibration process the device puts the DPLL into mini holdover, internally ramps the phase offset to zero, resets all clock dividers, ramps the phase offset to the value stored in the OFFSET registers, and then switches the DPLL out of mini holdover. If the OFFSET registers are written during the recalibration process, the process will ramp the phase offset to the new offset value.

### 7.7.10 Frequency and Phase Measurement

Standard input clock frequency monitoring is described in Section 7.5.1. The input clock monitors report measured frequency with 3.8ppm resolution. More accurate measurement of frequency and phase can be accomplished using the DPLLs. The T0 DPLL is always monitoring its selected reference, but if the T4 DPLL is not otherwise used then it can be configured as a high-resolution frequency and phase monitor. Software can then connect the T4 DPLL to various input clocks on a rotating basis to measure frequency and phase. See MCR4:T4FORCE.

DPLL frequency measurements can be read from the FREQ field spanning registers FREQ1, FREQ2 and FREQ3. This field indicates the frequency of the selected reference for either the T0 DPLL or the T4 DPLL, depending on the setting of the T4T0 bit in MCR11. This frequency measurement has a resolution of 0.0003068ppm over a ±80ppm range. The value read from the FREQ field is the DPLL's integral path value, which is an averaged measurement with an averaging time inversely proportional to DPLL bandwidth.

DPLL phase measurements can be read from the PHASE field spanning registers PHASE1 and PHASE2. This field indicates the phase difference seen by the phase detector for either the T0 DPLL or the T4 DPLL, depending

on the setting of the T4T0 bit in MCR11. This phase measurement has a resolution of approximately 0.7 degrees and is internally averaged with a -3dB attenuation point of approximately 100Hz. Thus, for low DPLL bandwidths the PHASE field gives input phase wander in the frequency band from the DPLL corner frequency up to 100Hz. This information could be used by software to compute a crude MTIE measurement up to an observation time of approximately 1000 seconds.

For the T0 DPLL, the PHASE field always indicates the phase difference between the selected reference and the internal feedback clock. The T4 DPLL, however, can be configured to measure the phase difference between two input clocks. When T0CR1:T4MT0 = 1, the T4 path is disabled and the T4 phase detector is configured to compare the T0 DPLL selected reference with the T4 DPLL selected reference. Any input clock can then be forced to be the T4 DPLL selected reference using the T4FORCE field of MCR4. This feature can be used, for example, to measure the phase difference between the T0 DPLL's selected reference and its next highest priority reference. Software could compute MTIE and TDEV with respect to the selected reference for any or all of the other input clocks.

When comparing the phase of the T0 and T4 selected references by setting T0CR1:T4MT0 = 1, several details must be kept in mind. In this mode, the T4 path receives a copy of the T0 selected reference, either directly or through a divider to 8kHz. If the T4 selected reference is divided down to 8kHz using LOCK8K or DIVN modes (see Section 7.4.2), then the copy of the T0 selected reference is also divided down to 8kHz. If the T4 selected reference is configured for direct-lock mode, then the copy of the T0 selected reference is not divided down and must be the same frequency as the T4 selected reference. See Table 7-6 for more details. (While T0CR1:T4MT0 = 1 the T0 path continues to lock to the T0 selected reference in the manner specified in the corresponding ICR register.)

## Table 7-6. T0 Adaptation for T4 Phase Measurement Mode

| LOCKING MODE FOR T4 SELECTED REFERENCE | LOCKING MODE FOR T0 SELECTED REFERENCE | LOCKING MODE FOR COPY OF T0 SELECTED REF | FREQUENCY OF THE T4 SELECTED REF FOR T4/T0 PHASE MEASUREMENT | FREQUENCY OF THE T0 SELECTED REF FOR T4/T0 PHASE MEASUREMENT |
|---|---|---|---|---|
| DIVN or LOCK8K | DIRECT | LOCK8K | 8kHz | 8kHz |
| DIVN or LOCK8K | LOCK8K | LOCK8K | 8kHz | 8kHz |
| DIVN or LOCK8K | DIVN | DIVN | 8kHz | 8kHz |
| DIRECT | Any | DIRECT | Same as the T4 selected ref input frequency | Same as the T0 selected ref input frequency(1) |

**Note 1:** In this case, the T0 select reference must be the same frequency as the T4 selected reference.

**Note 2:** If the T4 selected reference frequency is 8kHz and the T0 selected reference is a different frequency, the two references can be compared by configuring the T4 selected reference for 8 kHz and LOCK8K mode. This forces the copy of the T0 selected reference to be divided down to 8kHz using either LOCK8K or DIVN mode.

### 7.7.11 Input Wander and Jitter Tolerance

The device is compliant with the jitter and wander tolerance requirements of the standards listed in Table 1-1. Wander is tolerated up to the point where wander causes an apparent long-term frequency offset larger than the limits specified in the ILIMIT and/or SRLIMIT registers. In such a situation the input clock would be declared invalid. Jitter is tolerated up to the point of eye closure. Either LOCK8K mode (see Section 7.4.2.2) or the multicycle phase detector (see Section 7.7.5) should be used for high jitter tolerance.

### 7.7.12 Jitter and Wander Transfer

In the DS3101, the transfer of jitter and wander from the selected reference to the output clocks has a programmable transfer function that is determined by the DPLL bandwidth. (See Section 7.7.3.) In the T0 DPLL, the 3dB corner frequency of the jitter transfer function can be set to any of 18 positions from 0.5mHz to 70Hz. In the T4 DPLL, the 3dB corner frequency of the jitter transfer function can be set to 18Hz, 35Hz, or 70Hz.

During locked mode, the transfer of wander from the local oscillator clock (connected to the REFCLK pin) to the output clocks is not significant as long as the DPLL bandwidth is set high enough to allow the DPLL to quickly compensate for oscillator frequency changes. During free-run and holdover modes, local oscillator wander has a much more significant effect. See Section 7.3.

### 7.7.13 Output Jitter and Wander

Several factors contribute to jitter and wander on the output clocks, including:

- Jitter and wander amplitude on the selected reference (while in the locked state)
- The jitter/wander transfer characteristic of the device (while in the locked state)
- The jitter and wander on the local oscillator clock signal (especially wander while in the holdover state)

The DPLL in the device has programmable bandwidth (see Section 7.7.3). With respect to jitter and wander, the DPLL behaves as a low-pass filter with a programmable pole. The bandwidth of the DPLL is normally set low enough to strongly attenuate jitter. The wander attenuation depends on the DPLL bandwidth chosen.

Over time frequency changes in the local oscillator can cause a phase difference between the selected reference and the output clocks. This is especially true at DPLL bandwidths of 0.1Hz and below because the DPLL's rate of change may be slower than the oscillator's rate of change. Oscillators with better stability will minimize this effect. In some applications an OCXO may be required rather than a TCXO. In the most demand applications, the OCXO may need to be shielded to further reduce the rate of temperature change and thus the rate of frequency change.

Typical MTIE and TDEV measurements for the DS3101 in locked mode are shown in Figure 7-3 and Figure 7-4, respectively.

## Figure 7-3. Typical MTIE for T0 DPLL Output

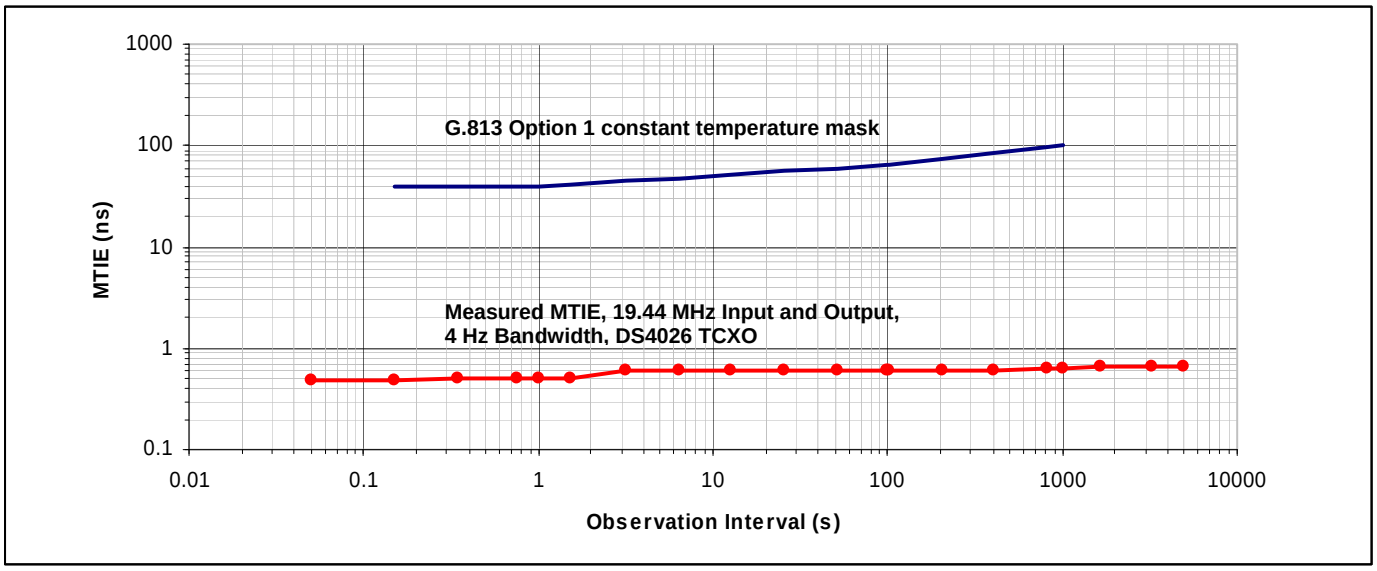
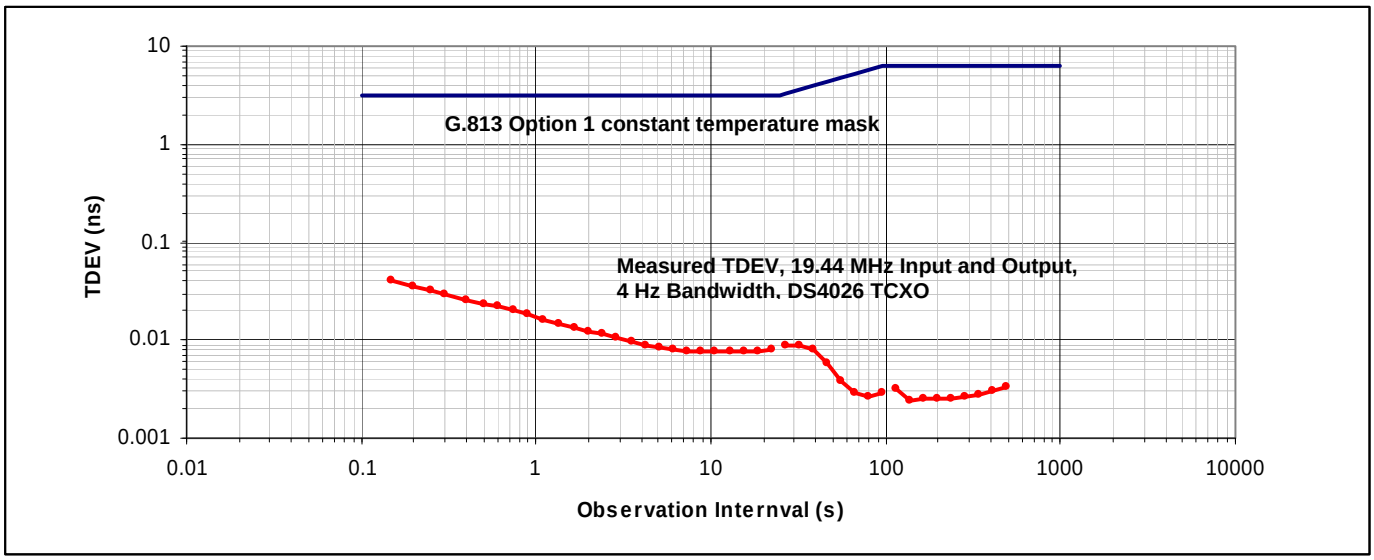


**Figure 7-4. Typical TDEV for T0 DPLL Output**




## 7.8 Output Clock Configuration

A total of 11 output clock pins, OC1 to OC11, are available on the device. Output clocks OC1 to OC7 are individually configurable for a variety of frequencies derived from either the T0 DPLL path or the T4 DPLL path. Output clocks OC8 to OC11 are more specialized, serving as a dedicated composite clock transmitter (OC8), a 1544/2.048kHz clock (OC9), an 8kHz frame sync (OC10), and a 2kHz multiframe sync (OC11). Table 7-7 provides more detail on the capabilities of the output clocks.

**Table 7-7. Output Clock Capabilities**

| OUTPUT CLOCK | SIGNAL FORMAT | FREQUENCIES SUPPORTED |
|---|---|---|
| OC1 | CMOS/TTL | Frequency selection per Section 7.8.2.3 and Table 7-9 through Table 7-12 |
| OC2 | CMOS/TTL | |
| OC3 | CMOS/TTL | |
| OC4 | CMOS/TTL | |
| OC5 | CMOS/TTL | |
| OC6 | LVDS | |
| OC7 | LVDS | |
| OC8 | AMI | 64kHz composite clock |
| OC9 | CMOS/TTL | 1.544MHz or 2.048MHz |
| OC10 | CMOS/TTL | 8kHz frame sync with programmable pulse width and polarity |
| OC11 | CMOS/TTL | 2kHz multiframe sync with programmable pulse width and polarity |

### 7.8.1 Signal Format Configuration

Output clocks OC6 and OC7 are enabled and disabled via the OC6SF and OC7SF configuration bits in the MCR8 register. The LVDS electrical specifications are listed in Table 10-4, and the recommended LVDS termination is shown in Figure 10-1. These outputs can be easily interfaced to LVPECL and CML inputs on neighboring ICs using a few external passive components. Refer to Maxim App Note HFAN-1.0: Introduction to LVDS, PECL, and CML for details.

Output clock OC8 is a dedicated composite clock (CC) transmitter. The composite clock signal is a 64kHz AMI clock with an embedded 8kHz clock indicated by deliberate bipolar violations (BPVs) every 8 clock cycles. See Section 7.10.2 for OC8 configuration details. The AMI CC electrical specifications are shown in Table 10-6, and the recommended external components are shown in Figure 10-3.

Output clocks OC1 to OC5 and OC9 to OC11 are always CMOS/TTL signal format.

### 7.8.2 Frequency Configuration

The frequency of most of the output clocks is a function of the settings used to configure the components of the T0 and T4 PLL paths. These components are shown in the detailed block diagram of Figure 7-5.

The T0 and T4 PLLs use digital frequency synthesis (DFS) to generate various clocks. In DFS, a high-speed master clock (204.8MHz) is divided down to the desired output frequency. The edges of the output clock, however, are not ideally located in time but rather are aligned with the edges of the master clock resulting in jitter with an amplitude equal to 1 period of the master clock (i.e., 4.88ns).

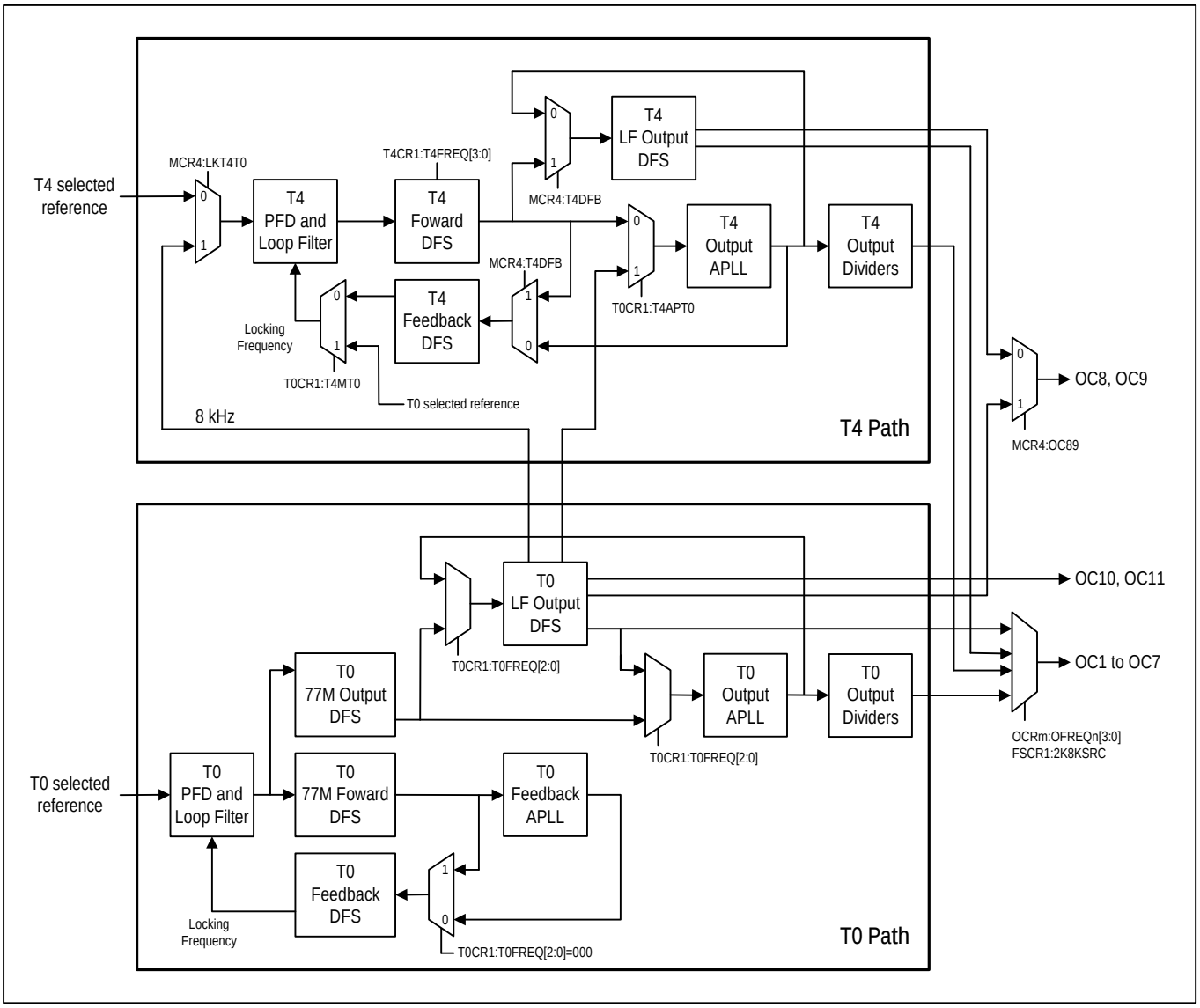
#### 7.8.2.1 T0 DPLL and APLL Details

The 77M forward DFS block (see Figure 7-5) uses the 204.8MHz master clock and DFS to synthesize a 77.76MHz clock with 4.88ns inherent peak-to-peak jitter. This clock can be fed directly to the feedback DFS block or it can be passed through the feedback APLL to reduce jitter to less than 1ns. The 77M forward DFS block handles phase build-out and any phase offset configured in the OFFSET registers. Thus, the 77M output DFS block and the 77M forward DFS block are frequency locked but may have a phase offset.

The feedback DFS block takes as its input clock either the output from the 77M forward DFS or the jitter-filtered output from the T0 feedback APLL. The feedback DFS block synthesizes the appropriate locking frequency for use in the phase-frequency detector (PFD).

The 77M output DFS block also uses the 204.8MHz master clock and DFS to synthesize a 77.76MHz clock with 4.88ns peak-to-peak jitter. This clock goes to both the output APLL and the low frequency (LF) output DFS block.

## Figure 7-5. DPLL Block Diagram




The LF output DFS block takes as its input clock either the output from the 77M output DFS or the jitter-filtered output of the output APLL. The LF output DFS block synthesizes three frequencies: Digital1, Digital2, and a third frequency for producing multiple N x DS1/E1 rates via the output APLLs. When the output APLL uses the output from the LF output DFS, the LF output DFS uses the output from the 77M output DFS block to avoid a loop. The LF output DFS also synthesizes frequencies for use by output clocks OC8, OC9, OC10, and OC11.

The frequency of the Digital1 clock is configured by the DIG1SS bit in MCR6 and the DIG1F[1:0] field in MCR7. The frequency of the Digital2 clock is configured by the DIG2AF and DIG2SS bits in MCR6 and the DIG2F[1:0] field in MCR7. Digital1 and Digital2 can be independently configured for any of the frequencies shown in Table 7-8. Because they are generated by DFS and cannot be filtered by an APLL, Digital1 and Digital2 have relatively high-amplitude jitter. The minimum jitter is approximately 12ns (one period of the input clock to the LF output DFS) when the T0 path is in analog feedback mode. The maximum jitter is approximately 17ns when T0 is in digital feedback mode. Both the Digital1 and Digital2 rates are available to output clocks OC1 to OC7.

The output APLL takes as its input clock either the output of the 77M output DFS or one of the frequencies from the LF output DFS (77.76MHz, 16 x DS1, 24 x DS1, 12 x E1, or 16 x E1). The output frequency of the output APLL is four times the input frequency (e.g., 311.04MHz for 77.76MHz input). The output clock is then divided by 1, 2, 4, 6, 8, 12, 16, and 48. These clock rates are available to the OC1 to OC7 output clocks.

## Table 7-8. Digital1 and Digital2 Frequencies

| DIGxF[1:0] SETTING IN MCR7 | DIGxSS SETTING IN MCR6 | FREQUENCY (MHz) |
|---|---|---|
| 00 | 0 | 2.048 |
| 01 | 0 | 4.096 |
| 10 | 0 | 8.192 |
| 11 | 0 | 16.384 |
| 00 | 1 | 1.544 |
| 01 | 1 | 3.088 |
| 10 | 1 | 6.176 |
| 11 | 1 | 12.352 |

***Note:*** *When MCR6:DIG2AF = 1, Digital2 generates 6312kHz (must set MCR6:DIG2SS = 0 and MCR7:DIG2F = 00).*

#### 7.8.2.2 T4 DPLL and APLL Details

The T4 path is simpler than the T0 path and does not support phase build-out or phase offset. The T4 path can be locked to an input clock or to the T0 path (by setting LKT4T0 = 1 in MCR4). Using the 204.8MHz master clock and DFS, the T4 forward DFS block generates a clock with 4.88 ns inherent peak-to-peak jitter at any of the following frequencies: 16 x DS1, 24 x DS1, 12 x E1, 16 x E1, DS3, 2 x E3, 62.5MHz, or 77.76MHz. This clock can be fed directly to the T4 feedback DFS block (T4DFB = 1 in MCR4), or it can be passed through the T4 output APLL to reduce jitter to less than 1ns (T4DFB = 0).

The T4 feedback DFS block takes as its input clock either the output from the T4 forward DFS or the jitter-filtered output from the T4 output APLL, depending on the setting of MCR4:T4DFB. The T4 feedback DFS block synthesizes the appropriate locking frequency for use in the T4 phase-frequency detector (PFD).

The T4 output APLL filters jitter to less than 1 ns and takes as its input clock either the output of the T4 forward DFS block or one of the frequencies from the T0 LF output DFS (16xDS1, 24xDS1, 12xE1, 16xE1 or 4x6312kHz, as specified by T0CR1:T0FT4[2:0]). The output frequency of the output APLL is four times the input frequency (e.g., 311.04MHz for 77.76MHz input). The output clock is then divided by 2, 4, 8, 16, 48, and 64. These clock rates are available to the OC1 to OC7 output clocks.

The T4 LF output DFS block normally takes as its input clock the jitter-filtered output of the T4 output APLL. When the T4 output APLL is connected to the T0 LF output DFS (T0CR1:T4APT0 = 1), the T4 output APLL must be disconnected from the T4 DPLL loop by configuring the loop for digital feedback (MCR4:T4DFB = 1). In this situation the T4 LF output DFS takes its input from the T4 forward DFS block. The T4 LF output DFS block generates 2kHz and 8kHz frequencies for use by output clocks OC1 to OC7 (when FSCR1:2K8KSRC = 1) and synthesizes frequencies for use by output clocks OC8 and OC9 (when MCR4:OC89 = 1).

#### 7.8.2.3 OC1 to OC7 Configuration

The following is a step-by-step procedure for configuring the frequencies of output clocks OC1 to OC7:

1) Determine whether the T4 path must be independent of the T0 path or not. If the T4 path must be independent, set T4APT0 = 0 in register T0CR1. If the T4 path can be locked to the T0 path then set T4APT0 = 1.
2) Use Table 7-9 to select a set of output frequencies for each path, T0 and T4. Each path can only generate one set of output frequencies. (In SONET/SDH equipment the T0 path is typically configured for an APLL frequency of 311.04MHz in order to get 19.44MHz and/or 38.88MHz output clocks to distribute to system line cards.)
3) Determine from Table 7-9 the T0 and T4 APLL frequencies required for the frequency sets chosen in step 2.
4) Configure the T0FREQ field in register T0CR1 as shown in Table 7-10 for the T0 APLL frequency determined in step 3. Configure the T4FREQ field in register T4CR1 as shown in Table 7-11 for the T4 APLL frequency determined in step 3. If the T4 APLL is locked to the T0 DPLL then the T0FT4 field in T0CR1 must also be configured as shown in Table 7-11.
5) Using Table 7-9 and Table 7-12, configure the frequencies of output clocks OC1 through OC7 in the OFREQn fields of registers OCR1 to OCR4.
6) If any of OC1 to OC7 are configured for 2kHz or 8kHz frequency, set 2K8KSRC = 0 in FSCR1 to source these frequencies from the T0 path or 2K8KSRC = 1 to source these frequencies from the T4 path.

Table 7-13 lists all possible frequencies for output clocks OC1 to OC7 and specifies how to configure the T0 path and/or the T4 path to obtain each frequency. Table 7-13 also indicates the expected jitter amplitude for each frequency.

### Table 7-9. APLL Frequency to Output Frequencies (T0 and T4)

| APLL FREQUENCY | APLL/2 | APLL/4 | APLL/6 | APLL/8 | APLL/12 | APLL/16 | APLL/48 | APLL/64 |
|---|---|---|---|---|---|---|---|---|
| 311.04 | 155.52 | **77.76** | **51.84** | **38.88** | 25.92 | **19.44** | 6.48 | 4.86 |
| 274.944 | 137.472 | 68.376 | — | **34.368** | — | 17.184 | 5.728 | 4.296 |
| 250.000 | 125.000 | 62.500 | — | 31.250 | — | 15.625 | 5.2083 | 3.90625 |
| 178.944 | 89.472 | **44.736** | — | 22.368 | — | 11.184 | 3.728 | 2.796 |
| 148.224 | 74.112 | 37.056 | **24.704** | 18.528 | **12.352** | 9.264 | **3.088** | 2.316 |
| 131.072 | 65.536 | **32.768** | 21.84533 | **16.384** | 10.92267 | **8.192** | 2.73067 | **2.048** |
| 100.992 | 50.496 | 25.248 | 16.832 | 12.624 | 8.416 | **6.312** | 2.104 | 1.578 |
| 98.816 | 49.408 | **24.704** | 16.46933 | **12.352** | 8.23467 | **6.176** | 2.05867 | **1.544** |
| 98.304 | 49.152 | 24.576 | **16.384** | 12.288 | **8.192** | 6.144 | **2.048** | 1.536 |

*Note: All frequencies in MHz. Common telecom frequencies are in **bold** type.*

### Table 7-10. T0 APLL Frequency to T0 Path Configuration

| T0 APLL FREQUENCY (MHz) | T0 FREQUENCY MODE | T0FREQ[2:0] SETTING IN T0CR1 | OUTPUT JITTER (pk-pk, ns) |
|---|---|---|---|
| 311.04 | 77.76MHz, digital feedback | 000 | < 0.5 |
| 311.04 | 77.7MHz, analog feedback | 001 | < 0.5 |
| 98.304 | 12 x E1 (digital feedback) | 010 | < 2 |
| 131.072 | 16 x E1 (digital feedback) | 011 | < 2 |
| 148.224 | 24 x DS1 (digital feedback) | 100 | < 2 |
| 98.816 | 16 x DS1 (digital feedback) | 101 | < 2 |
| 100.992 | 4 x 6312kHz (digital feedback) | 110 | < 2 |

## Table 7-11. T4 APLL Frequency to T4 Path Configuration

| T4 APLL FREQUENCY (MHz) | T4 FREQUENCY MODE | T4 FORWARD DFS FREQ (MHz) | T4APT0 SETTING IN T0CR1 | T4FREQ[3:0] SETTING IN T4CR1 | T0FT4[2:0] SETTING IN T0CR1 | OUTPUT JITTER (pk-pk, ns) |
|---|---|---|---|---|---|---|
| 311.04 | Squelched | 77.76 | 0 | 0000 | XXX | < 0.5 |
| 311.04 | Normal | 77.76 | 0 | 0001 | XXX | < 0.5 |
| 98.304 | 12 x E1 | 24.576 | 0 | 0010 | XXX | < 0.5 |
| 131.072 | 16 x E1 | 32.768 | 0 | 0011 | XXX | < 0.5 |
| 148.224 | 24 x DS1 | 37.056 | 0 | 0100 | XXX | < 0.5 |
| 98.816 | 16 x DS1 | 24.704 | 0 | 0101 | XXX | < 0.5 |
| 274.944 | 2 x E3 | 68.736 | 0 | 0110 | XXX | < 0.5 |
| 178.944 | DS3 | 44.736 | 0 | 0111 | XXX | < 0.5 |
| 100.992 | 4 x 6312 kHz | 25.248 | 0 | 1000 | XXX | < 0.5 |
| 250.000 | GbE ÷ 16 | 62.500 | 0 | 1001 | XXX | < 0.5 |
| 98.304 | T0 12 x E1 | — | 1 | XXXX | 000 | < 2 |
| 131.072 | T0 16 x E1 | — | 1 | XXXX | 010 | < 2 |
| 148.224 | T0 24 x DS1 | — | 1 | XXXX | 100 | < 2 |
| 98.816 | T0 16 x DS1 | — | 1 | XXXX | 110 | < 2 |
| 100.992 | 4 x 6312kHz | — | 1 | XXXX | 111 | < 2 |

## Table 7-12. OC1 to OC7 Output Frequency Selection

| REGISTER VALUE[1] | FREQUENCY | | | | | | |
|---|---|---|---|---|---|---|---|
| | OC1 | OC2 | OC3 | OC4 | OC5 | OC6 | OC7 |
| 0000 | Disabled | Disabled | Disabled | Disabled | Disabled | Disabled | Disabled |
| 0001 | 2kHz | 2kHz | 2kHz | 2kHz | 2kHz | 2kHz | 2kHz |
| 0010 | 8kHz | 8kHz | 8kHz | 8kHz | 8kHz | 8kHz | 8kHz |
| 0011 | Digital2 | Digital2 | Digital2 | Digital2 | Digital2 | T0 APLL/2 | Digital2 |
| 0100 | Digital1 | Digital1 | Digital1 | Digital1 | Digital1 | Digital1 | T0 APLL/2 |
| 0101 | T0 APLL/48 | T0 APLL/48 | T0 APLL/48 | T0 APLL/48 | T0 APLL/48 | T0 APLL/1 | T0 APLL/48 |
| 0110 | T0 APLL/16 | T0 APLL/16 | T0 APLL/16 | T0 APLL/16 | T0 APLL/16 | T0 APLL/16 | T0 APLL/16 |
| 0111 | T0 APLL/12 | T0 APLL/12 | T0 APLL/12 | T0 APLL/12 | T0 APLL/12 | T0 APLL/12 | T0 APLL/12 |
| 1000 | T0 APLL/8 | T0 APLL/8 | T0 APLL/8 | T0 APLL/8 | T0 APLL/8 | T0 APLL/8 | T0 APLL/8 |
| 1001 | T0 APLL/6 | T0 APLL/6 | T0 APLL/6 | T0 APLL/6 | T0 APLL/6 | T0 APLL/6 | T0 APLL/6 |
| 1010 | T0 APLL/4 | T0 APLL/4 | T0 APLL/4 | T0 APLL/4 | T0 APLL/4 | T0 APLL/4 | T0 APLL/4 |
| 1011 | T4 APLL/64 | T4 APLL/64 | T4 APLL/64 | T4 APLL/2 | T4 APLL/2 | T4 APLL/64 | T4 APLL/64 |
| 1100 | T4 APLL/48 | T4 APLL/48 | T4 APLL/48 | T4 APLL/48 | T4 APLL/48 | T4 APLL/48 | T4 APLL/48 |
| 1101 | T4 APLL/16 | T4 APLL/16 | T4 APLL/16 | T4 APLL/16 | T4 APLL/16 | T4 APLL/16 | T4 APLL/16 |
| 1110 | T4 APLL/8 | T4 APLL/8 | T4 APLL/8 | T4 APLL/8 | T4 APLL/8 | T4 APLL/8 | T4 APLL/8 |
| 1111 | T4 APLL/4 | T4 APLL/4 | T4 APLL/4 | T4 APLL/4 | T4 APLL/4 | T4 APLL/4 | T4 APLL/4 |

***Note 1:*** *The value of the OFREQn field (in the OCR1 through OCR4 registers) corresponding to output clock OCn.*

## Table 7-13. Possible Frequencies for OC1 to OC7

| FREQUENCY (MHz) | | T0 DPLL MODE | T4 DPLL MODE | T4 APLL SOURCE | OFREQN SETTING | JITTER (TYP) | |
|---|---|---|---|---|---|---|---|
| | | | | | | RMS (ps) | pk-pk (ns) |
| 2kHz | | 77.76MHz, analog | — | — | 0001 | 60 | 0.6 |
| 2kHz | | Any digital feedback | | | 0001 | 1400 | 5.0 |
| 8kHz | | 77.76MHz, analog | | | 0010 | 60 | 0.6 |
| 8kHz | | Any digital feedback | | | 0010 | 1400 | 5.0 |
| 1.536 | Not OC4 or OC5 | | 12 x E1 | T4 DPLL | **1011** | 55 | 0.6 |
| 1.536 | Not OC4 or OC5 | | | T0 12 x E1 | **1011** | 250 | 1.5 |
| 1.544 | Via Digital1, not OC7 | 77.76MHz, analog | | | 0100 | 3800 | 13 |
| 1.544 | Via Digital2, not OC6 | 77.76MHz, analog | | | 0011 | 3800 | 13 |
| 1.544 | Via Digital1, not OC7 | Any digital feedback | | | 0100 | 3800 | 18 |
| 1.544 | Via Digital2, not OC6 | Any digital feedback | | | 0011 | 3800 | 18 |
| 1.544 | Not OC4 or OC5 | | 16 x DS1 | T4 DPLL | 1011 | 140 | 1.2 |
| 1.544 | Not OC4 or OC5 | | | T0 16 x DS1 | 1011 | 275 | 1.9 |
| 1.578 | Not OC4 or OC5 | | 4 x 6312kHz | T4 DPLL | 1011 | 240 | 1.5 |
| 1.578 | Not OC4 or OC5 | | | T0 4x6312kHz | 1011 | 260 | 1.8 |
| 2.048 | Not OC6 | 12 x E1 mode | | | 0101 | 425 | 2.6 |
| 2.048 | Via Digital1, not OC7 | 77.76MHz, analog | | | 0100 | 3800 | 13 |
| 2.048 | Via Digital2, not OC6 | 77.76MHz, analog | | | 0011 | 3800 | 13 |
| 2.048 | Via Digital1, not OC7 | Any digital feedback | | | 0100 | 3800 | 18 |
| 2.048 | Via Digital2, not OC6 | Any digital feedback | | | 0011 | 3800 | 18 |
| 2.048 | | | 12 x E1 | T4 DPLL | 1100 | 55 | 0.6 |
| 2.048 | | | | T0 12 x E1 | 1100 | 250 | 1.5 |
| 2.048 | Not OC4 or OC5 | | 16 x E1 | T4 DPLL | 1011 | 50 | 0.5 |
| 2.048 | Not OC4 or OC5 | | | T0 16 x E1 | 1011 | 350 | 2.4 |
| 2.059 | Not OC6 | 16 x DS1 | | | 0101 | 435 | 2.8 |
| 2.059 | | | 16 x DS1 | T4 DPLL | 1100 | 140 | 1.2 |
| 2.059 | | | | T0 16 x DS1 | 1100 | 275 | 1.9 |
| 2.104 | Not OC6 | 4 x 6312 kHz | | | 0101 | 340 | 2.3 |
| 2.104 | | | 4 x 6312kHz | T4 DPLL | 1100 | 240 | 1.8 |
| 2.104 | | | | T0 4x6312kHz | 1100 | 260 | 1.8 |
| 2.316 | Not OC4 or OC5 | | 24 x DS1 | T4 DPLL | 1011 | 150 | 1.0 |
| 2.316 | Not OC4 or OC5 | | | T0 24 x DS1 | 1011 | 400 | 2.8 |
| 2.731 | Not OC6 | 16 x E1 | | | 0101 | 380 | 2.6 |
| 2.731 | | | 16 x E1 | T4 DPLL | 1100 | 50 | 0.5 |
| 2.731 | | | | T0 16 x E1 | 1100 | 350 | 2.4 |

| FREQUENCY (MHz) | | T0 DPLL MODE | T4 DPLL MODE | T4 APLL SOURCE | OFREQN SETTING | JITTER (TYP) | |
|---|---|---|---|---|---|---|---|
| | | | | | | RMS (ps) | pk-pk (ns) |
| 2.796 | Not OC4 or OC5 | | DS3 | T4 DPLL | 1011 | 80 | 0.7 |
| 3.088 | Not OC6 | 24 x DS1 | | | 0101 | 400 | 2.8 |
| 3.088 | Via Digital1, not OC7 | 77.76MHz, analog | | | 0100 | 3800 | 13 |
| 3.088 | Via Digital2, not OC6 | 77.76MHz, analog | | | 0011 | 3800 | 13 |
| 3.088 | Via Digital1, not OC7 | Any digital feedback | | | 0100 | 3800 | 18 |
| 3.088 | Via Digital2, not OC6 | Any digital feedback | | | 0011 | 3800 | 18 |
| 3.088 | | | 24 x DS1 | T4 DPLL | 1100 | 150 | 1.0 |
| 3.088 | | | | T0 24 x DS1 | 1100 | 400 | 2.8 |
| 3.728 | | | DS3 | T4 DPLL | 1100 | 80 | 0.7 |
| 3.90625 | Not OC4 or OC5 | | GbE ÷ 16 | T4 DPLL | 1011 | 70 | 0.6 |
| 4.096 | Via Digital1, not OC7 | 77.76 MHz, analog | | | 0100 | 3800 | 13 |
| 4.096 | Via Digital2, not OC6 | 77.76 MHz, analog | | | 0011 | 3800 | 13 |
| 4.096 | Via Digital1, not OC7 | Any digital feedback | | | 0100 | 3800 | 18 |
| 4.096 | Via Digital2, not OC6 | Any digital feedback | | | 0011 | 3800 | 18 |
| 4.296 | Not OC4 or OC5 | | 2 x E3 | T4 DPLL | 1011 | 350 | 2.0 |
| 4.86 | Not OC4 or OC5 | | 77.76MHz | T4 DPLL | 1011 | 60 | 0.6 |
| 5.2083 | | | GbE ÷ 16 | T4 DPLL | 1100 | 70 | 0.6 |
| 5.728 | | | 2 x E3 | T4 DPLL | 1100 | 350 | 2.0 |
| 6.144 | | 12 x E1 | | | 0110 | 425 | 2.6 |
| 6.144 | | | 12 x E1 | T4 DPLL | 1101 | 55 | 0.6 |
| 6.144 | | | | T0 12 x E1 | 1101 | 250 | 1.5 |
| 6.176 | | 16 x DS1 | | | 0110 | 435 | 2.8 |
| 6.176 | Via Digital1, not OC7 | 77.76MHz, analog | | | 0100 | 3800 | 13 |
| 6.176 | Via Digital2, not OC6 | 77.76MHz, analog | | | 0011 | 3800 | 13 |
| 6.176 | Via Digital1, not OC7 | Any digital feedback | | | 0100 | 3800 | 18 |
| 6.176 | Via Digital2, not OC6 | Any digital feedback | | | 0011 | 3800 | 18 |
| 6.176 | | | 16 x DS1 | T4 DPLL | 1101 | 140 | 1.2 |
| 6.176 | | | | T0 16 x DS1 | 1101 | 275 | 1.9 |
| 6.312 | | 4 x 6312kHz | | | 0110 | 340 | 2.3 |
| 6.312 | Via Digital 2, not OC6 | 77.76MHz, analog | | | 0011 | 3800 | 13 |
| 6.312 | Via Digital 2, not OC6 | Any digital feedback | | | 0011 | 3800 | 18 |
| 6.312 | | | 4 x 6312kHz | T4 DPLL | 1101 | 240 | 1.8 |
| 6.312 | | | | T0 4 x 6312kHz | 1101 | 260 | 1.8 |
| 6.48 | Not OC6 | 77.76MHz, analog | | | 0101 | 60 | 0.6 |
| 6.48 | Not OC6 | 77.76MHz, digital | | | 0101 | 60 | 0.6 |
| 6.48 | | | 77.76 MHz | T4 DPLL | 1100 | 60 | 0.6 |
| 8.192 | | 12 x E1 | | | 0111 | 425 | 2.6 |
| 8.192 | | 16 x E1 | | | 0110 | 380 | 2.6 |
| 8.192 | Via Digital1, not OC7 | 77.76 MHz, analog | | | 0100 | 3800 | 13 |
| 8.192 | Via Digital2, not OC6 | 77.76 MHz, analog | | | 0011 | 3800 | 13 |
| 8.192 | Via Digital1, not OC7 | Any digital feedback | | | 0100 | 3800 | 18 |
| 8.192 | Via Digital2, not OC6 | Any digital feedback | | | 0011 | 3800 | 18 |
| 8.192 | | | 16 x E1 | T4 DPLL | 1101 | 50 | 0.5 |
| 8.192 | | | | T0 16 x E1 | 1101 | 350 | 2.4 |
| 8.235 | | 16 x DS1 | | | 0111 | 435 | 2.8 |
| 8.416 | | 4 x 6312kHz | | | 0111 | 340 | 2.3 |
| 9.264 | | 24 x DS1 | | | 0110 | 400 | 2.8 |
| 9.264 | | | 24 x DS1 | T4 DPLL | 1101 | 150 | 1.0 |
| 9.264 | | | | T0 24 x DS1 | 1101 | 400 | 2.8 |
| 10.923 | | 16 x E1 | | | 0111 | 380 | 2.6 |
| 11.184 | | | DS3 | T4 DPLL | 1101 | 80 | 0.7 |
| 12.288 | | 12 x E1 | | | 1000 | 425 | 2.6 |
| 12.288 | | | 12 x E1 | T4 DPLL | 1110 | 55 | 0.6 |
| 12.288 | | | | T0 12 x E1 | 1110 | 250 | 1.5 |
| 12.352 | | 24 x DS1 | | | 0111 | 400 | 2.8 |
| 12.352 | | 16 x DS1 | | | 1000 | 435 | 2.8 |
| 12.352 | | | 16 x DS1 | T4 DPLL | 1110 | 140 | 1.2 |
| 12.352 | | | | T0 16 x DS1 | 1110 | 275 | 1.9 |
| 12.352 | Via Digital1, Not OC7 | 77.76MHz, analog | | | 0100 | 3800 | 13 |

| FREQUENCY (MHz) | | T0 DPLL MODE | T4 DPLL MODE | T4 APLL SOURCE | OFREQN SETTING | JITTER (TYP) | |
|---|---|---|---|---|---|---|---|
| | | | | | | RMS (ps) | pk-pk (ns) |
| 12.352 | Via Digital2, Not OC6 | 77.76MHz, analog | | | 0011 | 3800 | 13 |
| 12.352 | Via Digital1, Not OC7 | Any digital feedback | | | 0100 | 3800 | 18 |
| 12.352 | Via Digital2, Not OC6 | Any digital feedback | | | 0011 | 3800 | 18 |
| 12.624 | | 4 x 6312kHz | | | 1000 | 340 | 2.3 |
| 12.624 | | | 4 x 6312kHz | T4 DPLL | 1110 | 240 | 1.8 |
| 12.624 | | | | T0 4x6312kHz | 1110 | 260 | 1.8 |
| 15.625 | | | GbE ÷ 16 | T4 DPLL | 1101 | 70 | 0.6 |
| 16.384 | | 12 x E1 | | | 1001 | 425 | 2.6 |
| 16.384 | | 16 x E1 | | | 1000 | 380 | 2.6 |
| 16.384 | | | 16 x E1 | T4 DPLL | 1110 | 50 | 0.5 |
| 16.384 | | | | T0 16 x DS1 | 1110 | 275 | 1.9 |
| 16.384 | Via Digital1, Not OC7 | 77.76MHz, analog | | | 0100 | 3800 | 13 |
| 16.384 | Via Digital2, Not OC6 | 77.76MHz, analog | | | 0011 | 3800 | 13 |
| 16.384 | Via Digital1, Not OC7 | Any digital feedback | | | 0100 | 3800 | 18 |
| 16.384 | Via Digital2, Not OC6 | Any digital feedback | | | 0011 | 3800 | 18 |
| 16.469 | | 16 x DS1 | | | 1001 | 435 | 2.8 |
| 16.832 | | 4 x 6312kHz | | | 1001 | 340 | 2.3 |
| 17.184 | | | 2 x E3 | T4 DPLL | 1101 | 350 | 2.0 |
| 18.528 | | 24 x DS1 | | | 1000 | 400 | 2.8 |
| 18.528 | | | 24 x DS1 | T4 DPLL | 1110 | 150 | 1.0 |
| 18.528 | | | | T0 24 x DS1 | 1110 | 400 | 2.8 |
| 19.44 | | 77.76MHz, analog | | | 0110 | 60 | 0.6 |
| 19.44 | | 77.76MHz, digital | | | 0110 | 60 | 0.6 |
| 19.44 | | | 77.76 MHz | T4 DPLL | 1101 | 60 | 0.6 |
| 21.845 | | 16 x E1 | | | 1001 | 380 | 2.6 |
| 22.368 | | | DS3 | T4 DPLL | 1110 | 80 | 0.7 |
| 24.576 | | 12 x E1 | | | 1010 | 425 | 2.6 |
| 24.576 | | | 12 x E1 | T4 DPLL | 1111 | 55 | 0.6 |
| 24.576 | | | | T0 12 x E1 | 1111 | 250 | 1.5 |
| 24.704 | | 24 x DS1 | | | 1001 | 400 | 2.8 |
| 24.704 | | 16 x DS1 | | | 1010 | 435 | 2.8 |
| 24.704 | | | 16 x DS1 | T4 DPLL | 1111 | 140 | 1.2 |
| 24.704 | | | | T0 16 x DS1 | 1111 | 275 | 1.9 |
| 25.000 | | | GbE ÷ 16 | T4 DPLL | 1100 | 70 | 0.6 |
| 25.248 | | 4 x 6312kHz | | | 1010 | 340 | 2.3 |
| 25.248 | | | 4 x 6312kHz | T4 DPLL | 1111 | 240 | 1.8 |
| 25.248 | | | | T0 4x6312kHz | 1111 | 260 | 1.8 |
| 25.92 | | 77.76MHz, analog | | | 0111 | 60 | 0.6 |
| 25.92 | | 77.76MHz, digital | | | 0111 | 60 | 0.6 |
| 31.25 | | | GbE ÷ 16 | T4 DPLL | 1110 | 70 | 0.6 |
| 32.768 | | 16 x E1 | | | 1010 | 380 | 2.6 |
| 32.768 | | | 16 x E1 | T4 DPLL | 1111 | 50 | 0.5 |
| 32.768 | | | | T0 16 x E1 | 1111 | 350 | 2.4 |
| 34.368 | | | 2 x E3 | T4 DPLL | 1110 | 350 | 2.0 |
| 37.056 | | 24 x DS1 | | | 1010 | 400 | 2.8 |
| 37.056 | | | 24 x DS1 | T4 DPLL | 1111 | 150 | 1.0 |
| 37.056 | | | | T0 24 x DS1 | 1111 | 400 | 2.8 |
| 38.88 | | 77.76MHz, analog | | | 1000 | 60 | 0.6 |
| 38.88 | | 77.76MHz, digital | | | 1000 | 60 | 0.6 |
| 38.88 | | | 77.76MHz | T4 DPLL | 1110 | 60 | 0.6 |
| 44.736 | | | DS3 | T4 DPLL | 1111 | 80 | 0.7 |
| 49.152 | OC6 and OC7 Only | 12 x E1 | | | 0011/0100 | 425 | 2.6 |
| 49.152 | OC4 and OC5 Only | | 12 x E1 | T4 DPLL | 1011 | 55 | 0.6 |
| 49.152 | OC4 and OC5 Only | | | T0 12 x E1 | 1011 | 250 | 1.5 |
| 49.408 | OC6 and OC7 Only | 16 x DS1 | | | 0011/0100 | 435 | 2.8 |
| 49.408 | OC4 and OC5 Only | | 16 x DS1 | T4 DPLL | 1011 | 140 | 1.2 |
| 49.408 | OC4 and OC5 Only | | | T0 16 x DS1 | 1011 | 275 | 1.9 |
| 50.496 | OC6 and OC7 Only | 4 x 6312kHz | | | 0011/0100 | 340 | 2.3 |
| 50.496 | OC4 and OC5 Only | | 4 x 6312kHz | T4 DPLL | 1011 | 240 | 1.8 |

| FREQUENCY (MHz) | | T0 DPLL MODE | T4 DPLL MODE | T4 APLL SOURCE | OFREQN SETTING | JITTER (TYP) | |
|---|---|---|---|---|---|---|---|
| | | | | | | RMS (ps) | pk-pk (ns) |
| 50.496 | OC4 and OC5 Only | | | T0 4 x 6312kHz | 1011 | 260 | 1.8 |
| 51.84 | | 77.76MHz, analog | | | 1001 | 60 | 0.6 |
| 51.84 | | 77.76MHz, digital | | | 1001 | 60 | 0.6 |
| 62.50 | | | GbE ÷ 16 | T4 DPLL | 1111 | 70 | 0.6 |
| 65.536 | OC6 and OC7 Only | 16 x E1 | | | 0011/0100 | 380 | 2.6 |
| 65.536 | OC4 and OC5 Only | | 16 x E1 | T4 DPLL | 1011 | 50 | 0.5 |
| 65.536 | OC4 and OC5 Only | | | T0 16 x E1 | 1011 | 350 | 2.4 |
| 68.736 | | | 2 x E3 | T4 DPLL | 1111 | 350 | 2.0 |
| 74.112 | OC6 and OC7 Only | 24 x DS1 | | | 0011/0100 | 400 | 2.8 |
| 74.112 | OC4 and OC5 Only | | 24 x DS1 | T4 DPLL | 1011 | 150 | 1.0 |
| 74.112 | OC4 and OC5 Only | | | T0 24 x DS1 | 1011 | 400 | 2.8 |
| 77.76 | | 77.76MHz, analog | | | 1010 | 60 | 0.6 |
| 77.76 | | 77.76MHz, digital | | | 1010 | 60 | 0.6 |
| 77.76 | | | 77.76MHz | | 1111 | 60 | 0.6 |
| 89.472 | OC4 and OC5 Only | | DS3 | T4 DPLL | 1011 | 80 | 0.7 |
| 98.304 | OC6 Only | 12 x E1 | | | 0101 | 425 | 2.6 |
| 98.816 | OC6 Only | 16 x DS1 | | | 0101 | 435 | 2.8 |
| 100.992 | OC6 Only | 4 x 6312kHz | | | 0101 | 340 | 2.8 |
| 125.000 | OC5 Only | | GbE ÷ 16 | T4 DPLL | 1011 | 70 | 0.6 |
| 131.072 | OC6 Only | 16 x E1 | | | 0101 | 380 | 2.6 |
| 137.472 | OC4 and OC5 Only | | 2 x E3 | T4 DPLL | 1011 | 350 | 2.0 |
| 148.224 | OC6 Only | 24 x DS1 | | | 0101 | 400 | 2.8 |
| 155.52 | OC6 and OC7 Only | 77.76MHz, analog | | | 0011/0100 | 60 | 0.6 |
| 155.52 | OC6 and OC7 Only | 77.76MHz, digital | | | 0011/0100 | 60 | 0.6 |
| 155.52 | OC4 and OC5 Only | | 77.76MHz | T4 DPLL | 1011 | 60 | 0.6 |
| 311.04 | OC6 Only | 77.76MHz, analog | | | 0101 | 60 | 0.6 |
| 311.04 | OC6 Only | 77.76MHz, digital | | | 0101 | 60 | 0.6 |

#### 7.8.2.4 OC8 and OC9 Configuration

Output clocks OC8 and OC9 are generated by digital frequency synthesis (DFS) from either the T0 path or the T4 path, depending on the setting of the OC89 bit in MCR4. When generated from the T4 path (OC89 = 0), if ASQUEL = 1 in T4CR1 then OC8 and OC9 are automatically squelched when T4 has no valid input references.

OC8 is always a 64kHz composite clock transmitter and therefore does not require any frequency configuration. Being 64kHz, OC8 can be divided down directly from the source DFS block's input clock. The jitter on OC8 can range from 13ns to 17ns, depending on whether the DPLL is in analog or digital feedback mode. See Section 7.10.2 for additional OC8 configuration details.

OC9 is always a DS1 or E1 clock. OC9 is enabled by setting OC9EN = 1 in the OCR4 register, and it is configured for DS1 or E1 with the OC9SON bit in T4CR1 (when OC89 = 0) or with the SONSDH bit in MCR3 (when OC89 = 1). OC9 must synthesized, rather than directly divided down, from the source DFS block's input clock. The jitter on OC9 is therefore a function of the jitter on the input clock and the jitter generated during synthesis. OC9 jitter can range from 11ns to 20ns.

#### 7.8.2.5 OC10 and OC11 Configuration

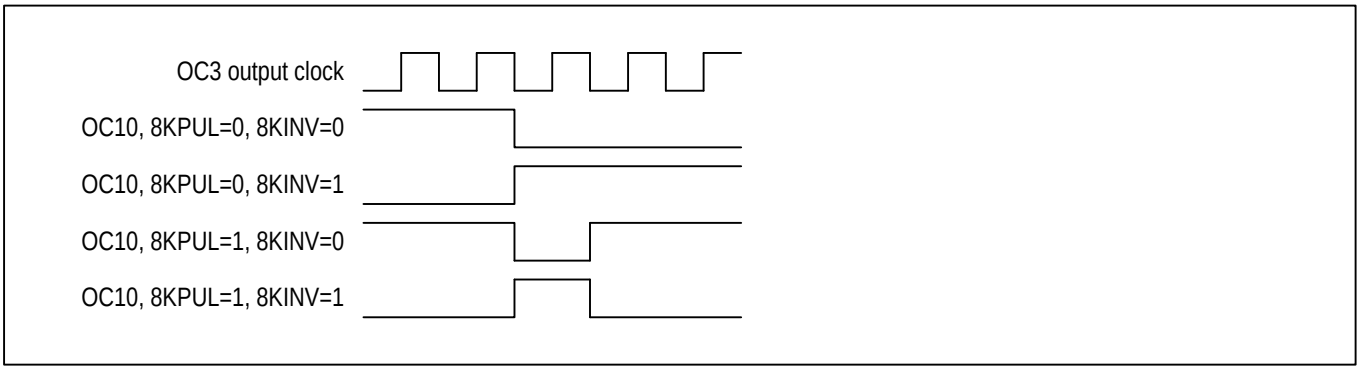
Output clocks OC10 and OC11 are always generated from the T0 path. OC10 is enabled by setting OC10EN = 1 in the OCR4 register, while OC11 is enabled by setting OC11EN = 1 in OCR4.

When 8KPUL = 0 in FSCR1, OC10 is configured as an 8kHz clock with 50% duty cycle. When 8KPUL = 1, OC10 is an 8kHz frame sync that pulses low once every 125µs with pulse width equal to one cycle of output clock OC3. When 8KINV = 1 in FSCR1, the clock or pulse polarity of OC10 is inverted.

When 2KPUL = 0 in FSCR1, OC11 is configured as an 2kHz clock with 50% duty cycle. When 2KPUL = 1, OC11 is a 2kHz frame sync that pulses low once every 500µs with pulse width equal to one cycle of output clock OC3. When 2KINV = 1 in FSCR1, the clock or pulse polarity of OC11 is inverted.

If either 8KPUL = 1 or 2KPUL = 1, then output clock OC3 must be generated from the T0 DPLL and must be configured for a frequency of 1.544MHz or higher or the OC10/OC11 pulses may not be generated correctly. Figure 7-6 shows how the 8KPUL and 8KINV control bits affect the OC10 output. The 2KPUL and 2KINV bits have an identical effect on OC11.

### Figure 7-6. OC10 8kHz Options




## 7.9 Equipment Redundancy Configuration

Most high-reliability SONET/SDH systems require two identical timing cards for equipment redundancy. The DS3101 directly supports this requirement. In such a system one timing cards is designated the master while the other is designated the slave. The rest of the system, outside the timing cards, is set up to take timing from the master normally, but to automatically switch to taking timing from the slave if the master fails. To avoid excessive phase transients when switching between master timing and slave timing, the clocks from the master and the slave must be frequency locked and usually phase locked as well. To accomplish this requires a method involving both static configuration and ongoing oversight by system software. The elements of this methodology are listed in Table 7-14.

### Table 7-14. Equipment Redundancy Methodology

| | |
|---|---|
| 1. | The various clock sources available in the system should be wired to the same pins on the slave as on the master, except:<br>A. One output clock from the master device should be wired to an input clock on the slave.<br>B. One output clock from the slave device should be wired to an input clock on the master. |
| 2. | The input clock priorities (IPR registers) on master and slave should be identical, for both T0 and T4 paths, except:<br>A. The master output clock is the highest priority input on the slave(1)<br>B. The slave output clock is disabled (priority 0) on the master<br>This ensures that the frequency of the slave matches the frequency of the master. |
| 3. | Any input declared invalid in one device (VALSR registers) must be marked invalid by software in the other device (VALCR registers). This and item 2 together ensure that when the master is performing properly, the slave locks to the master, and when the master fails, the slave locks to the input clock the master was previously locked to. |
| 4. | The slave's T0 DPLL bandwidth should be set higher than the master's (T0LBW, T0ABW registers) to ensure that the slave follows any transients coming from the master. (70Hz is recommended.) |
| 5. | Phase build-out should be disabled (MCR10:PBOEN = 0 and PHMON:PMPBEN = 0) on the slave when it is locked to the master to ensure that the slave maintains phase lock with the master. This also allows the use of phase offset (OFFSET registers) to compensate for delays between master and slave. |
| 6. | Revertive mode should be enabled on the slave (REVERT = 1 in MCR3) to ensure the slave switches from any other reference to the master as soon as the master's clock is valid. |

**Note 1:** This must be done for the slave's T0 path, but is not necessary for the slave's T4 path. In the slave's T4 path the input clock priorities should match those of the master except the input connected to the master's output clock should be disabled. This causes the slave's T4 path to only lock to external references.

### 7.9.1 Master-Slave Pin Feature

Some of the elements of redundancy configuration listed in Table 7-14 are automatically handled in the device when the master-slave pin feature is used (MASTSLV). When this feature is supported in a system, one output clock of the master device must be wired to input clock IC11 on the slave device, and one output clock of the slave device should be wired to IC11 on the master device. This cross-wiring allows the system to dynamically configure either device as master and the other as slave.

When the MASTSLV pin is wired low on one device, that device is configured as the slave. The other device must be configured as the master by wiring its MASTSLV pin high. In each device the state of the MASTSLV pin is always indicated in the read-only MASTSLV bit in register MCR3.

The slave device (MASTSLV = 0) is automatically configured as follows:

- The priority of input clock IC11 is set to 1 (highest) (IPR6:PRI11[3:0] = 0001).
- Phase build-out is disabled (MCR10:PBOEN = 0).
- Revertive mode is enabled (MCR3:REVERT = 1).
- T0 DPLL bandwidth is forced to the acquisition setting (i.e., to the setting in the T0ABW register, which should be set to a high bandwidth by software).

In the master device (MASTSLV = 1), none of these settings are forced to specific values. Rather, each setting is configured as needed for normal operation of the system. During configuration, software should configure the master to disable (priority 0) input clock IC11 and should configure the remaining input clock priorities identically in master and slave. During operation, software must maintain matching input clock priorities, as described in item 3 of Table 7-14.

The master-slave pin feature is optional and can be disabled by wiring the MASTSLV pin high on both devices. If this feature is disabled, all the elements of equipment redundancy listed in Table 7-14 must be configured and maintained by software.

### 7.9.2 Master-Slave Output Clock Phase Alignment

When the T0 DPLL is locked to a selected reference with frequency f, any output clocks derived from T0 with frequency f are phase aligned with the selected reference (if phase build-out is disabled). Any output clocks derived from T0 with frequency greater than f are “falling edge aligned” with the frequency-f output clock. Any output clocks derived from T0 with frequency less than f may or may not be aligned, depending on whether or not their frequencies are integer sub-multiples of f. These statements also apply to output clocks derived from the T4 DPLL.

Given this information, if master and slave devices are cross-wired with 19.44MHz clocks, for example, the output clocks at N x 19.44MHz (N = 1, 2, 4, 8, or 16) from the two devices are phase-aligned with one another. Output clocks at lower frequencies (6.48MHz, 1.544MHz, 2.048MHz, 2kHz, 8kHz, etc.) from the two devices would not necessarily be phase aligned. In many systems, lack of phase alignment between the two devices at these clock rates is not an issue. In some systems, however, the 2kHz and/or 8kHz clocks of the two devices must be aligned to avoid framing errors during switchover between master and slave.

One way to align the 2kHz and/or 8kHz clocks of the master and slave devices is to configure the slave to lock to a 2kHz or 8kHz output of the master. Another way is to use the SYNC2K input as described in Section 7.9.3.

### 7.9.3 Master-Slave Frame and Multiframe Alignment with the SYNC2K Pin

With this method of aligning the 2kHz and 8kHz clocks of the master and slave devices, both a higher-speed clock (such as 6.48MHz or 19.44MHz) and a frame-sync signal (normally 2kHz) from the master are passed to the slave (and vice versa when their roles are reversed). The higher-speed clock from the master is connected to a regular input clock pin on the slave, such as IC11, while the frame-sync signal from the master is connected to the SYNC2K pin on the slave. The slave locks to the higher-speed clock and samples the frame-sync signal on SYNC2K. The slave then uses the SYNC2K signal to falling-edge align some or all of the output clocks. Only the falling edge of SYNC2K has significance. A 4kHz or 8kHz clock can also be used on SYNC2K without any changes to the register configuration, but only output clocks of 8kHz and above are aligned in this case. Phase build-out should be disabled on the slave (PBOEN = 0 in MCR10), and the higher-speed input clock on the slave must be configured for direct-lock mode (ICR:DIVN = 0 and LOCK8K = 0).

**Sampling.** By default the SYNC2K signal is first sampled on the rising edge of the selected reference. This gives the most margin, given that the SYNC2K signal is falling-edge aligned with the selected reference since both come from the master device. The expected timing of SYNC2K with respect to the sampling clock can be adjusted from 0.5 cycles early to 1 cycle late using the FSCR2:PHASE[1:0] field.

**Resampling.** The SYNC2K signal is then resampled by an internal clock derived from the T0 DPLL. The resampling resolution is a function of the frequency of the selected reference and FSCR2:OCN. When OCN = 0, the resampling resolution is 6.48MHz, which gives the highest sampling margin and also aligns clocks at 6.48MHz and multiples thereof. When OCN = 1, if the selected reference is 19.44MHz then the resampling resolution is 19.44MHz. If the selected reference is 38.88MHz then the resampling resolution is 38.88MHz. The selected reference must be either 19.44MHz or 38.88MHz.

**SYNC2K Enable.** The SYNC2K signal is only allowed to align output clocks if the T0 DPLL is locked and SYNC2K is enabled and qualified. SYNC2K can be enabled automatically or manually. When MCR3:AEFSEN = 1, SYNC2K is enabled automatically when EFSEN = 1 and the T0 DPLL is locked to the input clock specified by FSCR3:SOURCE[3:0]. When AEFSEN = 0, SYNC2K is enabled manually when MCR3:EFSEN = 1 and disabled when EFSEN = 0. In manual mode when EFSEN = 1, FSCR3:SOURCE[3:0] is ignored and SYNC2K is always enabled regardless of which input clock is the selected reference.

**SYNC2K Qualification.** SYNC2K is qualified when it has consistent phase and correct frequency. Specifically, SYNC2K is qualified when its significant edge has been found at exact 2kHz boundaries (when resampled as described above) for 64 SYNC2K cycles in a row. SYNC2K is disqualified when one significant edge is not found at the 2kHz boundary.

**Output Clock Alignment.** When T0 is locked and SYNC2K is enabled and qualified, SYNC2K can be used to falling-edge align the T0-derived output clocks. Output clocks OC10 and OC11 share a 2kHz alignment generator, while the rest of the T0-derived output clocks share a second 2kHz alignment generator. When SYNC2K is not enabled or is not qualified, these 2Hz alignment generators free-run with their existing 2kHz alignments. When SYNC2K is enabled and qualified, the OC10/OC11 2kHz alignment generator is always synchronized by SYNC2K, and therefore OC10 and OC11 are always falling-edge aligned with SYNC2K. When FSCR2:INDEP = 0, the T0 2kHz alignment generator is also synchronized with the OC10/OC11 2kHz alignment generator to falling-edge align all T0-derived output clocks with SYNC2K. When INDEP = 1, the T0 2kHz alignment generator is not synchronized with the OC10/OC11 2kHz alignment generator and continues to free-run with its existing 2kHz alignment. This avoids any disturbance on the T0-derived output clocks when SYNC2K has a change of phase position.

**Frame Sync Monitor.** The frame sync monitor signal OPSTATE:FSMON operates in two modes, depending on the setting of the enable bit (MCR3:EFSEN).

When EFSEN = 1 (SYNC2K enabled) the FSMON bit is set when SYNC2K is not qualified and cleared when SYNC2K is qualified. If SYNC2K is disqualified then both 2kHz alignment generators are immediately disconnected from SYNC2K to avoid phase movement on the T0-derived outputs clocks. When OPSTATE:FSMON is set, the latched status bit MSR3:FSMON is also set, which can cause an interrupt if enabled. If SYNC2K immediately stabilizes at a new phase and proper frequency, then it is requalified after 64 2kHz cycles (nominally 32ms). Unless system software intervenes, after SYNC2K is requalified the 2kHz alignment generators will synchronize with SYNC2K's new phase alignment, causing a sudden phase movement on the output clocks. System software can

avoid this sudden phase movement on the output clocks by responding to the FSMON interrupt within the 32ms window with appropriate action, which might include disabling SYNC2K (MCR3:EFSEN = 0) to prevent the resynchronization of the 2kHz alignment generators with SYNC2K, forcing the slave into holdover (MCR1:T0STATE = 010) to avoid affecting the output clocks with any other phase hits, and possibly even disabling the master and promoting the slave to master (see Section 7.9.1) since the 2kHz signal from the master should not have such phase movements.

When EFSEN = 0 (SYNC2K disabled) OPSTATE:FSMON is set when the negative edge of the re-sampled SYNC2K signal is outside of the window determined by FSCR3:MONLIM relative to the OC11 negative edge (or positive edge if OC11 is inverted) and clear when within the window. When OPSTATE:FSMON is set, the latched status bit MSR3:FSMON is also set, which can cause an interrupt if enabled.

**Other Frame Sync Configuration Options.** OC10 and OC11 are always produced from the T0 path. Output clocks OC1 to OC7 can also be configured as 2kHz or 8kHz outputs, derived from either the T0 path or the T4 path (as specified by the 2K8KSRC bit in FSCR1). If needed, the T4 DPLL can be used as a separate DPLL for the frame sync path by configuring it for a 2kHz input and 2kHz and/or 8 kHz frame sync outputs.

## 7.10 Composite Clock Receivers and Transmitter

By default, input clocks IC1 and IC2 are configured as composite clock receivers. Output clock OC8 is a dedicated composite clock transmitter. These I/Os support the following key composite clock variations:

- GR-378 composite clock (**Note 1**)
- G.703 centralized clock (**Note 2**)
- G.703 Japanese synchronization interface (**Note 3**)

**Note 1:** Complies with Telcordia GR-378 composite clock and G.703 section 4.2.2 centralized clock option b).

**Note 2:** Complies with ITU_T G.703 section 4.2.2 centralized clock options a) and G.703 Section 4.2.3 contradirectional interface clock.

**Note 3:** Complies with ITU_T G.703 Appendix II.1 options a) and option b) Japanese synchronization interfaces.

Composite clock (CC) signals provide both bit and byte synchronization for equipment with DS0 connections. In all CC variations, the signal is a 64kHz AMI signal with an embedded 8kHz clock indicated by a deliberate bipolar violation (BPV) every 8 clock cycles. The option b) Japanese synchronization interface in G.703 Appendix II.1 also has an embedded 400Hz clock indicated by a BPV *removed* every 400Hz. Details about the several composite clock variations are described in the following paragraphs and summarized in Table 7-15.

**GR-378 Composite Clock.** As shown in Table 7-16 and Figure 7-7, the GR-378 composite clock signal has a 5/8 duty-cycle square pulse and a 133Ω line impedance. The G.703 Section 4.2.2 option b) centralized clock specifications are nearly identical to the GR-378 composite clock, with the exception of line termination impedance (110Ω for G.703 vs. 133Ω for GR-378).

**G.703 Centralized Clock and other 64kHz + 8kHz Timing Signals.** G.703 Section 4.2.2 defines two centralized clock types, option a) and option b). Option b) is discussed in the GR-378 paragraph above. As shown in Table 7-17, the option a) centralized clock has a 50% duty cycle and a 110Ω line impedance. G.703 also specifies three other timing signals that have characteristics and specifications that are nearly identical to those of centralized clock option a). These other signals are (1) the timing signal in the 64kbps contradirectional interface defined in G.703 Section 4.2.3, (2) the 64kHz + 8kHz Japanese timing signal defined in G.703 Appendix II.1, and (3) the 64kHz + 8kHz + 400Hz Japanese timing signal defined in G.703 Appendix II.1 (which has the 8kHz BPV removed every 400Hz). Table 7-17 tabulates the requirements for each of these signals.

### Table 7-15. Composite Clock Variations

| VARIATION | LINE IMPEDANCE (Ω0) | PULSE AMPLITUDE (V) | NOMINAL DUTY CYCLE | BPVs |
|---|---|---|---|---|
| Composite Clock, GR-378 | 133 | 2.7 to 5.5 | 5/8 | 8kHz |
| Centralized Clock, G.703 4.2.2 option b) | 110 | 3.0 ± 0.5 | 5/8 | 8kHz |
| Centralized Clock, G.703 4.2.2 option a) | 110 | 1.0 ± 0.1V | 50% | 8kHz |
| Japanese Sync Interface, G.703 Appendix II.1 option a) | 110 | ≤ 1 ± 0.1 | 50% | 8kHz |
| Japanese Sync Interface, G.703 Appendix II.1 option b) | 110 | ≤ 1 ± 0.1 | 50% | 8kHz, but removed at 400Hz |
| Contradirectional Interface Clock, G.703 4.2.3 | 120 | 1.0 ± 0.1 | 50% | 8kHz |

### 7.10.1 IC1 and IC2 Receivers

Input clocks IC1 and IC2 can be either composite clock receivers (via the IC1A and IC2A pins) or standard CMOS/TTL inputs (via the IC1 and IC2 pins). Configuration bits MCR5:IC1SF and IC2SF specify the signal format for IC1 and IC2, respectively. When these inputs are configured as composite clock (CC) receivers, they can directly receive incoming AMI-coded 64kHz CC signals, including those with the pre-emphasis described in GR-378 Section 4.2. See the electrical specifications in Table 10-6, and the recommended external components in Figure 10-3.

Each CC receiver derives an 8kHz clock from the 8kHz component of the incoming CC signal. It is this 8kHz clock that is forwarded to the input clock monitoring and selection circuitry. The falling edge of this 8kHz clock can be configured to coincide with the leading edge of the 8kHz BPV or the leading edge of the pulse following the BPV, as specified by the CCEDGE field in the MCR5 register.

Incoming composite clock signals are monitored for loss-of-signal and AMI violations. When either of these signal conditions occurs, a corresponding latched status bit is set in register MSR3. When set, these status bits can cause an interrupt request on the INTREQ pin if enabled by the corresponding bits in IER3. Loss of signal is declared when no pulses are detected in the incoming signal in a 32µs period (i.e., after two missing pulses, voltage threshold $V_{LOS}$ = 0.2V typical). The amplitude threshold for detecting a pulse is 0.2V. An AMI violation is declared when a deviation from the expected pattern of seven ones followed by a BPV occurs in each of two consecutive 8-bit periods. When MCR5:BITERR = 1, single-bit violations of the one-BPV-in-eight pattern are considered irregularities by the corresponding activity monitor and increment the leaky bucket accumulator. When MCR5:AMI = 1, the detection of an AMI violation automatically invalidates the offending clock. When MCR5:LOS = 1, the detection of loss-of-signal automatically invalidates the offending clock.

In addition, register MSR4 has latched status bits that indicate the absence of the 8kHz component and the 400Hz component. In some networks the 8kHz component is removed to signal an alarm condition. If the BPVs that indicate the 8kHz component cannot be found in the incoming signal in a 500µs period (four 8kHz cycles), then MSR4:ICxNO8 is set to indicate the fact. This can cause an interrupt on the INTREQ pin if enabled by the corresponding bit in IER4. This logic is always active. If the lack of the 8kHz component is not an alarm signal in the synchronization network, then IER4:ICxNO8 can be set to 0 to disable the interrupt, and MSR4:ICxNO8 can be ignored. If the 8kHz component is not present in the signal, then the CC receiver does not forward an 8kHz clock to the input monitoring logic. The input monitoring logic then declares that input clock invalid.

If the missing BPVs that indicate the 400Hz component cannot be found in a 5ms period (two 400Hz cycles), then MSR4:ICxNO4 is set. This can cause an interrupt on the INTREQ pin if enabled by the corresponding bit in IER4. This logic is always active. If the 400Hz component is not expected to be present in the signal, then IER4:ICxNO4 can be set to 0 to disable the interrupt, and MSR4:ICxNO4 can be ignored.

When the 8kHz component is entirely missing from the incoming signal, the AMI status bit in MSR3 is continually set, and can cause repeated interrupts if enabled. Therefore, in networks where the lack of the 8kHz component is used as an alarm signal, after MSR4:ICxNO8 is set to indicate that the 8kHz component is missing, the interrupt for MSR3:AMIx should be disabled until ICxNO8 goes low, indicating the 8kHz component is present again. Also, since the 8kHz component is the clock that is forwarded to the input clock monitor, if the 8kHz component is missing in the incoming signal, the input clock monitor automatically invalidates the clock. If the 400Hz component is missing, however, the AMI status bit is not set and the clock is not invalidated.

### 7.10.2 OC8 Transmitter

Output clock OC8 is a dedicated composite clock transmitter. See the electrical specifications in Table 10-6, and the recommended external components in Figure 10-3. OC8 is a differential output consisting of pins OC8POS and OC8NEG. These pins are enabled/disabled by OCR4:OC8EN. Either 50% or 5/8 duty cycle can be selected by setting T4CR1:OC8DUTY appropriately. In some networks the 8kHz component (i.e., the one BPV every eight cycles) is removed to signal an alarm condition; the 8kHz component of the OC8 signal can be removed as needed by setting MCR8:OC8NO8 = 1.

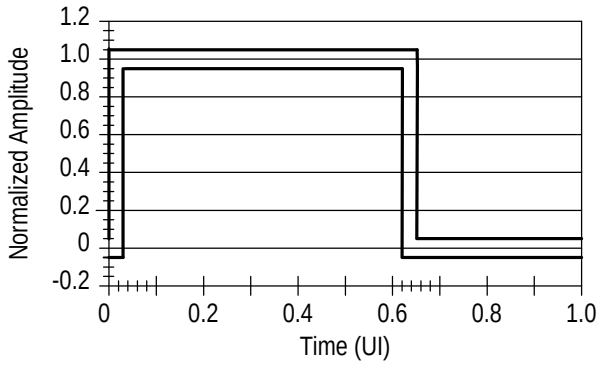
When the selected reference is either IC1 or IC2 and that input is configured in AMI/CC mode (MCR5:IcxSF = 0), and the signal on that input has an 8kHz component (MSR4:ICxNO8 = 0), then the output BPVs on OC8 (the 8kHz component) is closely aligned (within a few µs) to the input BPVs but may be of opposite polarity.

To support the G.703 Appendix II.1 option b) Japanese synchronization interface, the 400Hz component (i.e., the removed BPV every 160 cycles) can be enabled by setting MCR8:OC8400 = 1. If the selected reference is either IC1 or IC2 and that input is configured in AMI/CC mode (MCR5:IcxSF = 0) and the signal on that input has a 400 Hz component (MSR4:ICxNO4 = 0), then OC8's 400Hz component is aligned with the input 400 Hz component but may be the opposite polarity. Otherwise, the 400Hz component for OC8 is divided down from OC8's 8kHz component. Setting OC8400 = 1 has no effect if OC8NO8 = 1. See Section 7.8.2.4 for additional OC8 configuration details.

## Table 7-16. GR-378 Composite Clock Interface Specification

| PARAMETER | SPECIFICATION |
|---|---|
| Nominal Line Rate | 64kHz with 8kHz bipolar violation. |
| Line-Rate Accuracy | Accuracy of the network clock. |
| Line Code | Bipolar (AMI), return-to-zero, with 5/8 duty cycle. |
| Medium | A shielded, balanced twisted pair. |
| Test Load Impedance | The resistive test load of 133Ω (±5%) shall be used at the interface for evaluation of the pulse shape and the electrical parameters. |
| Pulse Amplitude | The amplitude of an isolated pulse shall be between 2.7V and 5.5V. |
| Pulse Shape | The shape of an isolated pulse shall be rectangular with rise and fall times less than 0.5µs such that the pulse fits the shape of the mask in Figure 7-7. |
| Pulse Imbalance | The ratio of the amplitudes of the positive and negative pulses shall be from 0.95 to 1.05.<br>The ratio of the widths of the positive and negative pulses shall be from 0.95 to 1.05. |
| DC Power | No DC power shall be applied to the interface. |

## Figure 7-7. GR-378 Composite Clock Pulse Mask




| Time (UI) | Minimum Normalized Amplitude | Minimum Normalized Amplitude |
|---|---|---|
| 0 | -0.05 | 1.05 |
| 0.032 | 0.95 | 1.05 |
| 0.625 | -0.05 | 1.05 |
| 0.657 | -0.05 | 0.05 |
| 1 | -0.05 | 0.05 |

## Table 7-17. G.703 Synchronization Interfaces Specification

| PARAMETER | SPECIFICATION |
|---|---|
| Pulse Shape | Nominally rectangular, with rise and fall times less than 1µs. |
| Transmission Media | Symmetric pair cable. |
| Nominal Test Load Impedance | 110Ω resistive (centralized clock and appendix II Japanese signals).<br>120Ω resistive (contradirectional interface). |
| Peak Voltage of a Mark (Pulse) | 1.0V ± 0.1V |
| Peak Voltage of a Space (No Pulse) | 0V ± 0.1V |
| Nominal Pulse Width | 7.8µs ± 0.78µs |
| Pulse Imbalance | The ratio of the amplitudes of the positive and negative pulses shall be from 0.95 to 1.05.<br>The ratio of the widths of the positive and negative pulses shall be from 0.95 to 1.05. |
| Alarm Condition for Received Signal Amplitude | No alarm for pulse amplitudes between $0.63V_{0-P.}$ and $1.1V_{0-P}$. |

## 7.11 Microprocessor Interfaces

The DS3101 microprocessor interface can be configured for 8-bit parallel or SPI serial operation. During reset, the device determines its interface mode by latching the state of the IFSEL[2:0] pins into the IFSEL field of the IFCR register. Table 7-18 shows possible values of IFSEL.

### Table 7-18. Microprocessor Interface Modes

| IFSEL[2:0] | MODE |
|---|---|
| 010 | Intel bus mode (multiplexed) |
| 011 | Intel bus mode (nonmultiplexed) |
| 100 | Motorola mode (nonmultiplexed) |
| 101 | SPI mode (LSB first) |
| 110 | Motorola mode (multiplexed) |
| 111 | SPI mode (MSB first) |
| 000, 001 | {unused value} |

### 7.11.1 Parallel Interface Modes

In the Motorola interface modes, the interface is Motorola-style with $\overline{CS}$, R/$\overline{W}$, and $\overline{DS}$ control lines. In the Intel modes, the interface is Intel-style with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control lines. For multiplexed bus modes, the A[8], AD[7:0], and ALE pins are wired to the corresponding pins on the microprocessor, and the falling edge of ALE latches the address on A[8] and AD[7:0]. For nonmultiplexed bus modes, the A[8:0] and AD[7:0] pins are wired to the corresponding pins on the micro, and the falling edge of ALE latches the address on A[8:0]. In nonmultiplexed bus modes, ALE is typically wired high to make the latch transparent. See Section 10.4 for AC timing details.

### 7.11.2 SPI Interface Mode

In the SPI modes, the device presents an SPI interface on the $\overline{CS}$, SCLK, SDI, and SDO pins. SPI is a widely used master/slave bus protocol that allows a master device and one or more slave devices to communicate over a serial bus. The DS3101 is always a slave device. Masters are typically microprocessors, ASICs, or FPGAs. Data transfers are always initiated by the master device, which also generates the SCLK signal. The DS3101 receives serial data on the SDI pin and transmits serial data on the SDO pin. SDO is high impedance except when the DS3101 is transmitting data to the bus master.

**Bit Order.** When IFCR:IFSEL = 101, the register address and all data bytes are transmitted LSB first on both SDI and SDO. When IFSEL = 111, the register address and all data bytes are transmitted MSB first on both SDI and SDO. The Motorola SPI convention is MSB first.

**Clock Polarity and Phase.** The CPOL pin defines the polarity of SCLK. When CPOL = 0, SCLK is normally low and pulses high during bus transactions. When CPOL = 1, SCLK is normally high and pulses low during bus transactions. The CPHA pin sets the phase (active edge) of SCLK. When CPHA = 0, data is latched in on SDI on the leading edge of the SCLK pulse and updated on SDO on the trailing edge. When CPHA = 1, data is latched in on SDI on the trailing edge of the SCLK pulse and updated on SDO on the following leading edge. SCLK does not have to toggle between access, i.e., when $\overline{CS}$ is high. See Figure 7-8.

**Device Selection.** Each SPI device has its own chip-select line. To select the DS3101, pull its $\overline{CS}$ pin low.

**Control Word.** After $\overline{CS}$ is pulled low, the bus master transmits the control word during the first 16 SCLK cycles. In MSB-first mode, the control word has the form:

R/$\overline{W}$ A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 BURST

where A[13:0] is the register address, R/$\overline{W}$ is the data direction bit (1 = read, 0 = write), and BURST is the burst bit (1 = burst access, 0 = single-byte access). In LSB-first mode, the order of the 14 address bits is reversed. In the discussion that follows, a control word with R/$\overline{W}$ = 1 is a read control word, while a control word with R/$\overline{W}$ = 0 is a write control word.

**Single-Byte Writes.** See Figure 7-9. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 0 followed by the data byte to be written. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

**Single-Byte Reads.** See Figure 7-9. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 0. The DS3101 then responds with the requested data byte. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

**Burst Writes.** See Figure 7-9. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 1 followed by the first data byte to be written. The DS3101 receives the first data byte on SDI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the DS3101 continues to write the data received and increment its address counter. After the address counter reaches 3FFFh, it rolls over to address 0000h and continues to increment.

**Burst Reads.** See Figure 7-9. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 1. The DS3101 then responds with the requested data byte on SDO, increments its address counter, and prefetches the next data byte. If the bus master continues to demand data, the DS3101 continues to provide the data on SDO, increment its address counter, and prefetch the following byte. After the address counter reaches 3FFFh, it rolls over to address 0000h and continues to increment.

**Early Termination of Bus Transactions.** The bus master can terminate SPI bus transactions at any time by pulling $\overline{CS}$ high. In response to early terminations, the DS3101 resets its SPI interface logic and waits for the start of the next transaction. If a write transaction is terminated prior to the SCLK edge that latches the LSB of a data byte, the data byte is not written.

**Design Option: Wiring SDI and SDO Together.** Because communication between the bus master and the DS3101 is half-duplex, the SDI and SDO pins can be wired together externally to reduce wire count. To support this option, the bus master must not drive the SDI/SDO line when the DS3101 is transmitting.

**AC Timing.** See Table 10-12 and Figure 10-6 for AC timing specifications for the SPI interface.

## Figure 7-8. SPI Clock Polarity and Phase Options

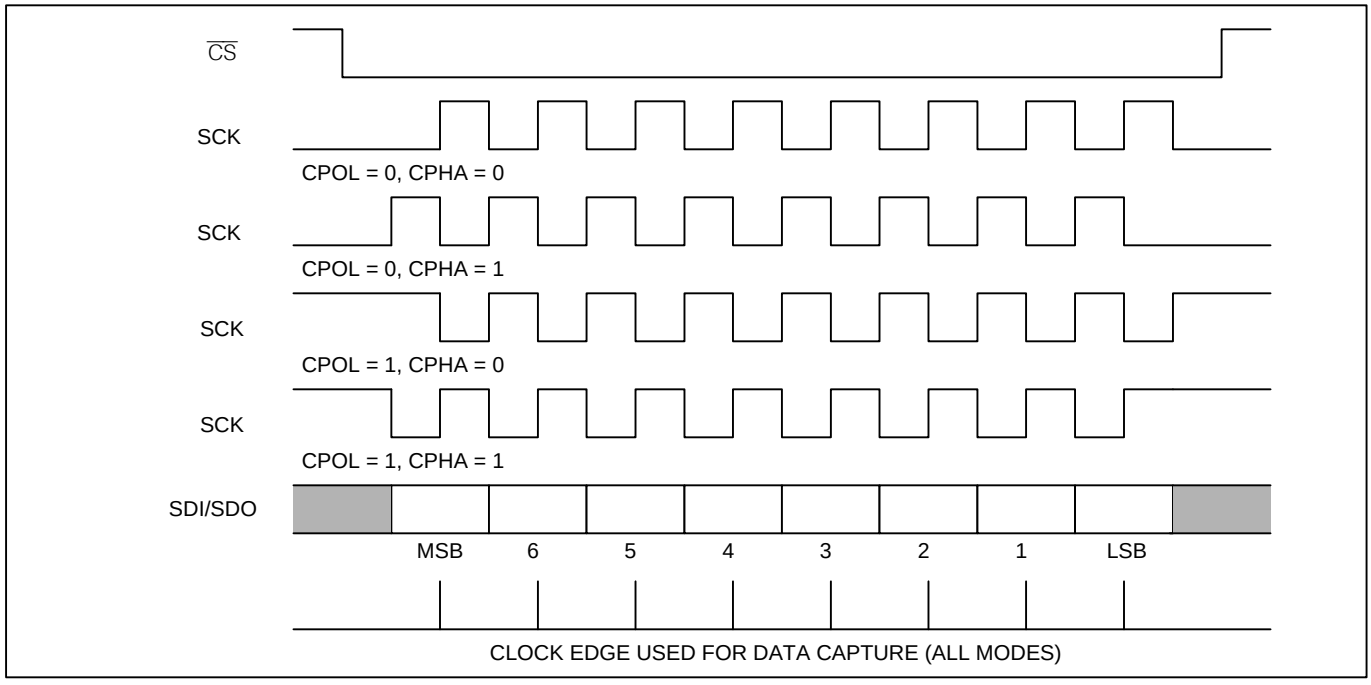
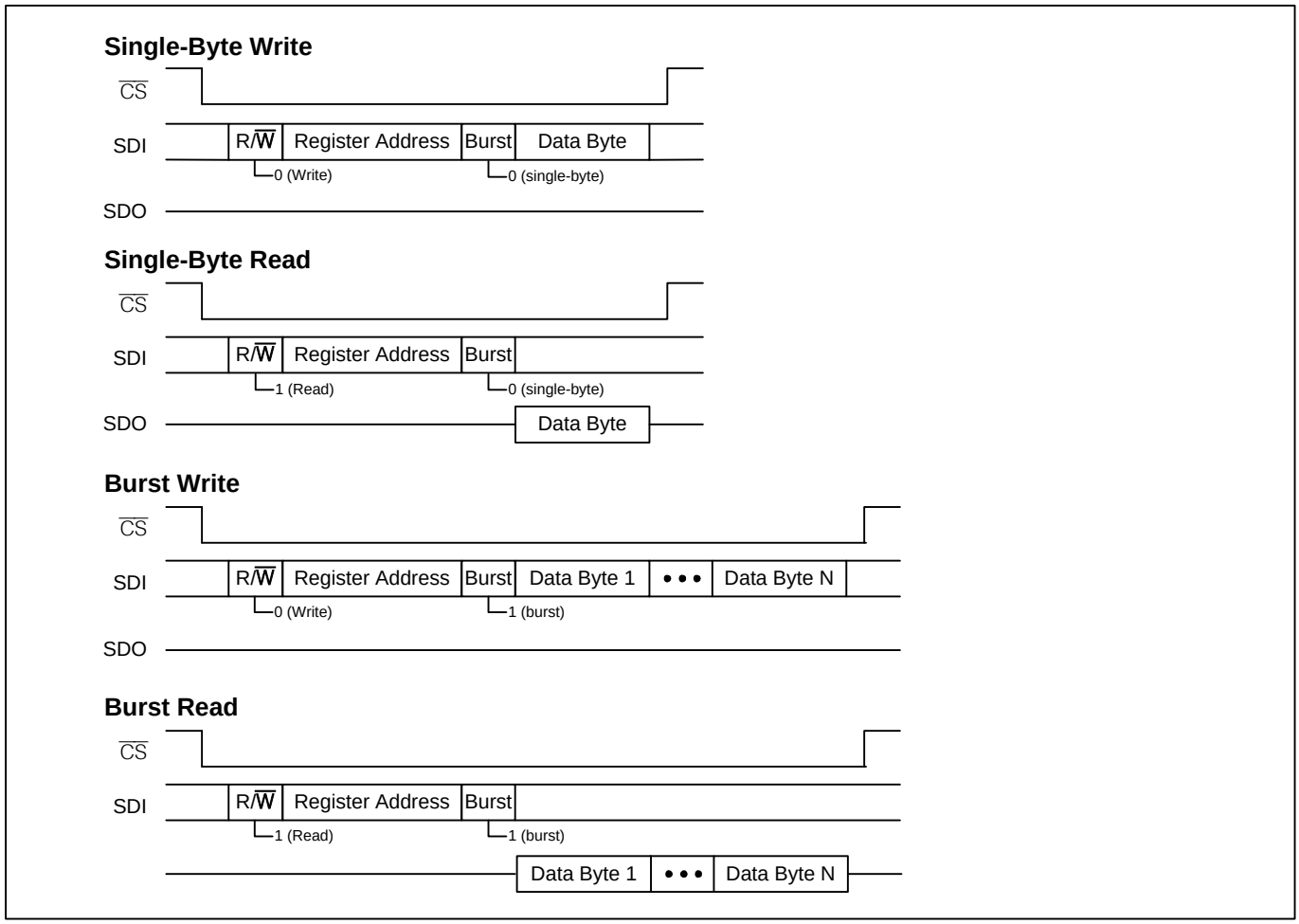


**Figure 7-9. SPI Bus Transactions**




## 7.12 Reset Logic

The device has three reset controls: the $\overline{RST}$ pin, the RST bit in MCR1, and the JTAG reset pin, $\overline{JTRST}$. The $\overline{RST}$ pin asynchronously resets the entire device, except for the JTAG logic. When the $\overline{RST}$ pin is low, all internal registers are reset to their default values, including those fields that latch their default values from, or based on, the states of input pins when the $\overline{RST}$ pin goes high (such as IFCR:IFSEL[2:0]). The $\overline{RST}$ pin must be asserted once after power-up while the external oscillator is stabilizing.

The MCR1:RST bit resets the entire device (except for the microprocessor interface, the JTAG logic, and the RST bit itself), but when RST is active, the register fields with pin-programmed defaults do not latch their values from, or based on, the corresponding input pins. Instead, these fields are reset to the default values that were latched when the $\overline{RST}$ pin was last active.

Maxim recommends holding $\overline{RST}$ low while the external oscillator starts up and stabilizes. Some OCXOs take 250ms or more to start up and stabilize their output signals to valid logic levels and pulse widths. An incorrect reset condition could result if $\overline{RST}$ is released before the oscillator has started up completely.

**Important:** System software must wait at least 100µs after reset ($\overline{RST}$ pin or RST bit) is deasserted before initializing the device as described in Section 7.14.

## 7.13 Power-Supply Considerations

Due to the dual-power-supply nature of the DS3101, some I/Os have parasitic diodes between a 1.8V supply and a 3.3V supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the 1.8V supply and the 3.3V supply to force the 3.3V supply to be less than one parasitic diode drop below the 1.8V supply. The second method is to ramp up the 3.3V supply first and then ramp up the 1.8V supply.

## 7.14 Initialization

After power-up or reset, a series of writes must be done to the DS3101 to tune it for optimal performance. This series of writes is called the initialization script. Each die revision of the DS3101 has a different initialization script. Download the latest initialization scripts from the DS3101 website, www.maxim-ic.com/DS3101.

# 8. REGISTER DESCRIPTIONS

### Table 8-1. Top-Level Memory Map

| ADDRESS RANGE | FUNCTIONAL BLOCK |
|---|---|
| 0000–007Fh | PLL Register Space |
| 0080–01FFh | Reserved |

Note: Systems must be able to access the entire address range from 0 to 01FFh. Proper device initialization requires a sequence of writes to addresses in the range 0180-01FFh.

As shown in Table 8-1 the DS3101 occupies an address range from 0000h to 01FFh. Addresses 0000h to 007Fh contain the user-accessible registers shown in Table 8-2. Addresses 0080h to 01FFh are reserved and should not be written. In each register, bit 7 is the MSB and bit 0 is the LSB. Register addresses not listed and bits marked with the symbol "—" are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode, resulting in undefined operation. Bits labeled "0" or "1" must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow Table 8-2.

## 8.1 Status Bits

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bits are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. Writing a 0 has no effect. When set, some latched status bits can cause an interrupt request on the INTREQ pin if enabled to do so by corresponding interrupt enable bits.

## 8.2 Configuration Fields

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked "—" are reserved and must be written with 0.

## 8.3 Multiregister Fields

Multiregister fields—such as FREQ[18:0] in registers FREQ1, FREQ2, and FREQ3—must be handled carefully to ensure that the bytes of the field remain consistent. A write access to a multiregister field is accomplished by writing all the registers of the field in any order, with no other accesses to the device in between. If the write sequence is interrupted by another access, none of the bytes are written and the MSR4:MRAA bit is set to indicate the write was aborted. A read access from a multiregister field is accomplished by reading the registers of the field in any order, with no other accesses to the device in between. When one register of a multiregister field is read, the other register(s) in the field are frozen until after they are all read. If the read sequence is interrupted by another access, the registers of the multibyte field are unfrozen and the MSR4:MRAA bit is set to indicate the read was aborted. For best results, interrupt servicing should be disabled in the microprocessor before a multiregister access and then enabled again after the access is complete. The multiregister fields are:

| FIELD | REGISTERS | ADDRESSES | TYPE |
|---|---|---|---|
| FREQ[18:0] | FREQ1, FREQ2, FREQ3 | 07, 0C, 0D | read-only |
| MCLKFREQ[15:0] | MCLK1, MCLK2 | 3C, 3D | read/write |
| HOFREQ[18:0] | HOCR1, HOCR2, HOCR3* | 3E, 3F, 40 | read/write |
| HARDLIM[9:0] | DLIMIT1, DLIMIT2 | 41, 42 | read/write |
| DIVN[14:0] | DIVN1, DIVN2 | 46, 47 | read/write |
| OFFSET[15:0] | OFFSET1, OFFSET2 | 70, 71 | read/write |
| PHASE[15:0] | PHASE1, PHASE2 | 77, 78 | read-only |

**HOCR3* *is a special case because its upper 5 bits are not part of a multiregister field, but its lower 3 bits are part of the HOFREQ[18:0] multiregister field. Writes to HOCR3 immediately update the upper 5 bits without any requirement to also write HOCR1 and HOCR2. The lower 3 bits of HOCR3 (HOFREQ[18:16]), however, can only be written as part of a proper write sequence for a multiregister field, as described above. A write to HOCR3 continugous with writes to HOCR1 and HOCR2 can simultaneously write the upper 5 bits immediately and start/continue/complete a multiregister write of HOFREQ[18:0].*

## 8.4 Register Definitions

### Table 8-2. Register Map

***Note:*** *Register names are hyperlinks to register definitions. Underlined fields are read-only.*

| ADDR | REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|
| 00h | ID1 | ID[7:0] | | | | | | | |
| 01 | ID2 | ID[15:8] | | | | | | | |
| 02 | REV | REV[7:0] | | | | | | | |
| 03 | TEST1 | PALARM | D180 | — | RA | 0 | 8KPOL | 0 | 0 |
| 05 | MSR1 | IC8 | IC7 | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| 06 | MSR2 | STATE | SRFAIL | IC14 | IC13 | IC12 | IC11 | IC10 | IC9 |
| 07 | FREQ3 | — | — | — | — | — | FREQ[18:16] | | |
| 08 | MSR3 | FSMON | T4LOCK | PHMON | T4NOIN | AMI2 | LOS2 | AMI1 | LOS1 |
| 09 | OPSTATE | FSMON | T4LOCK | T0SOFT | T4SOFT | — | T0STATE[2:0] | | |
| 0A | PTAB1 | REF1[3:0] | | | | SELREF[3:0] | | | |
| 0B | PTAB2 | REF3[3:0] | | | | REF2[3:0] | | | |
| 0C | FREQ1 | FREQ[7:0] | | | | | | | |
| 0D | FREQ2 | FREQ[15:8] | | | | | | | |
| 0E | VALSR1 | IC8 | IC7 | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| 0F | VALSR2 | FHORDY | SHORDY | IC14 | IC13 | IC12 | IC11 | IC10 | IC9 |
| 10 | ISR1 | SOFT2 | HARD2 | ACT2 | LOCK2 | SOFT1 | HARD1 | ACT1 | LOCK1 |
| 11 | ISR2 | SOFT4 | HARD4 | ACT4 | LOCK4 | SOFT3 | HARD3 | ACT3 | LOCK3 |
| 12 | ISR3 | SOFT6 | HARD6 | ACT6 | LOCK6 | SOFT5 | HARD5 | ACT5 | LOCK5 |
| 13 | ISR4 | SOFT8 | HARD8 | ACT8 | LOCK8 | SOFT7 | HARD7 | ACT7 | LOCK7 |
| 14 | ISR5 | SOFT10 | HARD10 | ACT10 | LOCK10 | SOFT9 | HARD9 | ACT9 | LOCK9 |
| 15 | ISR6 | SOFT12 | HARD12 | ACT12 | LOCK12 | SOFT11 | HARD11 | ACT11 | LOCK11 |
| 16 | ISR7 | SOFT14 | HARD14 | ACT14 | LOCK14 | SOFT13 | HARD13 | ACT13 | LOCK13 |
| 17 | MSR4 | FHORDY | SHORDY | MRAA | — | IC2NO4 | IC1NO4 | IC2NO8 | IC1NO8 |
| 18 | IPR1 | PRI2[3:0] | | | | PRI1[3:0] | | | |
| 19 | IPR2 | PRI4[3:0] | | | | PRI3[3:0] | | | |
| 1A | IPR3 | PRI6[3:0] | | | | PRI5[3:0] | | | |
| 1B | IPR4 | PRI8[3:0] | | | | PRI7[3:0] | | | |
| 1C | IPR5 | PRI10[3:0] | | | | PRI9[3:0] | | | |
| 1D | IPR6 | PRI12[3:0] | | | | PRI11[3:0] | | | |
| 1E | IPR7 | PRI14[3:0] | | | | PRI13[3:0] | | | |
| 20 | ICR1 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 21 | ICR2 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 22 | ICR3 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 23 | ICR4 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 24 | ICR5 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 25 | ICR6 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 26 | ICR7 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 27 | ICR8 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 28 | ICR9 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 29 | ICR10 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 2A | ICR11 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 2B | ICR12 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 2C | ICR13 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 2D | ICR14 | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| 30 | VALCR1 | IC8 | IC7 | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| 31 | VALCR2 | — | — | IC14 | IC13 | IC12 | IC11 | IC10 | IC9 |
| 32 | MCR1 | RST | — | — | — | — | T0STATE[2:0] | | |
| 33 | MCR2 | — | — | — | — | T0FORCE[3:0] | | | |

| ADDR | REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|
| 34 | MCR3 | AEFSEN | LKATO | XOEDGE | MANHO | EFSEN | SONSDH | MASTSLV | REVERT |
| 35 | MCR4 | LKT4T0 | T4DFB | — | OC89 | T4FORCE[3:0] | | | |
| 36 | MCR5 | CCEDGE | BITERR | AMI | LOS | IC2SF | IC1SF | IC6SF | IC5SF |
| 37 | IFSR | — | — | — | — | — | IFSEL[2:0] | | |
| 38 | MCR6 | DIG2AF | DIG2SS | DIG1SS | — | — | — | — | — |
| 39 | MCR7 | DIG2F[1:0] | | DIG1F[1:0] | | — | — | — | — |
| 3A | MCR8 | — | — | OC8400 | OC8NO8 | OC7SF | | OC6SF | |
| 3B | MCR9 | AUTOBW | — | — | — | LIMINT | PFD180 | — | — |
| 3C | MCLK1 | MCLKFREQ[7:0] | | | | | | | |
| 3D | MCLK2 | MCLKFREQ[15:8] | | | | | | | |
| 3E | HOCR1 | HOFREQ[7:0] | | | | | | | |
| 3F | HOCR2 | HOFREQ[15:8] | | | | | | | |
| 40 | HOCR3 | AVG | FAST | RDAVG | MINIHO[1:0] | | HOFREQ[18:16] | | |
| 41 | DLIMIT1 | HARDLIM[7:0] | | | | | | | |
| 42 | DLIMIT2 | — | — | — | — | — | — | HARDLIM[9:8] | |
| 43 | IER1 | IC8 | IC7 | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| 44 | IER2 | STATE | SRFAIL | IC14 | IC13 | IC12 | IC11 | IC10 | IC9 |
| 45 | IER3 | FSMON | T4LOCK | PHMON | T4NOIN | AMI2 | LOS2 | AMI1 | LOS1 |
| 46 | DIVN1 | DIVN[7:0] | | | | | | | |
| 47 | DIVN2 | — | DIVN[14:8] | | | | | | |
| 48 | MCR10 | FMONCLK | SRFPIN | UFSW | EXTSW | PBOFRZ | PBOEN | SOFTEN | HARDEN |
| 49 | ILIMIT | SOFT[3:0] | | | | HARD[3:0] | | | |
| 4A | SRLIMIT | SOFT[3:0] | | | | HARD[3:0] | | | |
| 4B | MCR11 | — | — | — | T4T0 | FMEASIN[3:0] | | | |
| 4C | FMEAS | FMEAS[7:0] | | | | | | | |
| 4D | DLIMIT3 | FLLOL | SOFTLIM[6:0] | | | | | | |
| 4E | IER4 | FHORDY | SHORDY | — | — | IC2NO4 | IC1NO4 | IC2NO8 | IC1NO8 |
| 50 | LB0U | LB0U[7:0] | | | | | | | |
| 51 | LB0L | LB0L[7:0] | | | | | | | |
| 52 | LB0S | LB0S[7:0] | | | | | | | |
| 53 | LB0D | — | — | — | — | — | — | LB0D[1:0] | |
| 54 | LB1U | LB1U[7:0] | | | | | | | |
| 55 | LB1L | LB1L[7:0] | | | | | | | |
| 56 | LB1S | LB1S[7:0] | | | | | | | |
| 57 | LB1D | — | — | — | — | — | — | LB1D[1:0] | |
| 58 | LB2U | LB2U[7:0] | | | | | | | |
| 59 | LB2L | LB2L[7:0] | | | | | | | |
| 5A | LB2S | LB2S[7:0] | | | | | | | |
| 5B | LB2D | — | — | — | — | — | — | LB2D[1:0] | |
| 5C | LB3U | LB3U[7:0] | | | | | | | |
| 5D | LB3L | LB3L[7:0] | | | | | | | |
| 5E | LB3S | LB3S[7:0] | | | | | | | |
| 5F | LB3D | — | — | — | — | — | — | LB3D[1:0] | |
| 60 | OCR1 | OFREQ2[3:0] | | | | OFREQ1[3:0] | | | |
| 61 | OCR2 | OFREQ4[3:0] | | | | OFREQ3[3:0] | | | |
| 62 | OCR3 | OFREQ6[3:0] | | | | OFREQ5[3:0] | | | |
| 63 | OCR4 | OC11EN | OC10EN | OC9EN | OC8EN | OFREQ7[3:0] | | | |
| 64 | T4CR1 | — | ASQUEL | OC8DUTY | OC9SON | T4FREQ[3:0] | | | |
| 65 | T0CR1 | T4MT0 | T4APT0 | T0FT4[2:0] | | | T0FREQ[2:0] | | |
| 66 | T4BW | — | — | — | — | — | — | T4BW[1:0] | |
| 67 | T0LBW | — | — | — | T0LBW[4:0] | | | | |
| 69 | T0ABW | — | — | — | T0ABW[4:0] | | | | |
| 6A | T4CR2 | — | PD2GA8K[2:0] | | | — | DAMP[2:0] | | |
| 6B | T0CR2 | — | PD2GA8K[2:0] | | | — | DAMP[2:0] | | |
| 6C | T4CR3 | PD2EN | PD2GA[2:0] | | | — | PD2GD[2:0] | | |

| ADDR | REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|
| 6D | T0CR3 | PD2EN | PD2GA[2:0] | | | — | PD2GD[2:0] | | |
| 6E | GPCR | GPIO4D | GPIO3D | GPIO2D | GPIO1D | GPIO4O | GPIO3O | GPIO2O | GPIO1O |
| 6F | GPSR | — | — | — | — | GPIO4 | GPIO3 | GPIO2 | GPIO1 |
| 70 | OFFSET1 | OFFSET[7:0] | | | | | | | |
| 71 | OFFSET2 | OFFSET[15:8] | | | | | | | |
| 72 | PBOFF | — | — | PBOFF[5:0] | | | | | |
| 73 | PHLIM1 | FLEN | NALOL | 1 | — | — | FINELIM[2:0] | | |
| 74 | PHLIM2 | CLEN | MCPDEN | USEMCPD | — | COARSELIM[3:0] | | | |
| 76 | PHMON | NW | — | PMEN | PMPBEN | PMLIM[3:0] | | | |
| 77 | PHASE1 | PHASE[7:0] | | | | | | | |
| 78 | PHASE2 | PHASE[15:8] | | | | | | | |
| 79 | PHLKTO | PHLKTOM[1:0] | | PHLKTO[5:0] | | | | | |
| 7A | FSCR1 | 2K8KSRC | — | — | — | 8KINV | 8KPUL | 2KINV | 2KPUL |
| 7B | FSCR2 | INDEP | OCN | — | — | — | — | PHASE[1:0] | |
| 7C | FSCR3 | RECAL | MONLIM[2:0] | | | SOURCE[3:0] | | | |
| 7D | INTCR | — | — | — | — | — | GPO | OD | POL |
| 7E | PROT | PROT[7:0] | | | | | | | |
| 7F | IFCR | — | — | — | — | — | IFSEL[2:0] | | |

**Register Map Color Coding**

| | |
|---|---|
| | Device Identification and Protection |
| | Local Oscillator and Master Clock Configuration |
| | Input Clock Configuration |
| | Input Clock Monitoring |
| | Input Clock Selection |
| | DPLL Configuration |
| | DPLL State |
| | Output Clock Configuration |
| | SYNC2K Configuration |
| | Microprocessor Interface Configuration |

**Unused Register Addresses**

04h, 1Fh, 2Eh, 2Fh, 4Fh, 68h, 75h

**Register Name:** ID1
**Register Description:** Device Identification Register, LSB
**Register Address:** 00h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | ID[7:0] | | | | | | | |
| **Default** | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |

**Bits 7 to 0: Device ID (ID[7:0]).** ID[15:0] = 0C1Dh = 3101 decimal.

**Register Name:** ID2
**Register Description:** Device Identification Register, MSB
**Register Address:** 01h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | ID[15:8] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

**Bits 7 to 0: Device ID (ID[15:8]).** See the ID1 register description.

**Register Name:** REV
**Register Description:** Device Revision Register
**Register Address:** 02h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | REV[7:0] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Device Revision (REV[7:0]).** Contact the factory to interpret this value and determine the latest revision.

**Register Name:** TEST1
**Register Description:** Test Register 1 (Not Normally Used)
**Register Address:** 03h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | PALARM | D180 | — | RA | 0 | 8KPOL | 0 | 0 |
| **Default** | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |

**Bit 7: Phase Alarm (PALARM).** This real-time status bit indicates the state of T0 DPLL phase lock.
0 = T0 phase-locked to input reference
1 = T0 loss of phase lock

**Bit 6: Disable 180 (D180).** When locking to a new reference, the T0 DPLL first tries nearest-edge locking (±180°) for the first two seconds. If unsuccessful it then tries full phase/frequency locking (±360°). Disabling the nearest-edge locking can reduce lock time by up to two seconds but may cause an unnecessary phase shift (up to 360°) when the new reference is close in frequency/phase to the old reference. See Section 7.7.5.
0 = normal operation: try nearest-edge locking then phase/frequency locking
1 = phase/frequency locking only

**Bit 4: Resync Analog Dividers (RA).** When this bit is set the T0 APLL output dividers are always synchronized to ensure that low-frequency outputs are in sync with the higher-frequency clock from the T0 DPLL.
0 = not synchronized
1 = always synchronized

**Bit 3:** Leave set to zero (test control).

**Bit 2: 8kHz Edge Polarity (8KPOL).** Specifies the input clock edge to lock to on the selected reference when it is configured for LOCK8K mode. See Section 7.4.2.
0 = Falling edge
1 = Rising edge

**Bit 1:** Leave set to zero (test control).

**Bit 0:** Leave set to zero (test control).

**Register Name:** MSR1
**Register Description:** Master Status Register 1
**Register Address:** 05h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | IC8 | IC7 | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| **Default** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Bits 7 to 0: Input Clock Status Change (IC8 to IC1).** Each of these latched status bits is set to 1 when the corresponding VALSR1 status bit changes state (set or cleared). If soft frequency limit alarms are enabled (MCR10:SOFTEN = 1), then each of these latched status bits is also set to 1 when the corresponding SOFT bit in the ISR registers changes state (set or cleared). Each bit is cleared when written with a 1 and not set again until either the VALSR1 bit or the SOFT bit changes state again. When one of these latched status bits is set it can cause an interrupt request on the INTREQ pin if the corresponding interrupt enable bit is set in the IER1 register. See Section 7.5 for input clock validation/invalidation criteria.

**Register Name:** MSR2
**Register Description:** Master Status Register 2
**Register Address:** 06h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | STATE | SRFAIL | IC14 | IC13 | IC12 | IC11 | IC10 | IC9 |
| **Default** | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

**Bit 7: T0 DPLL State Change (STATE).** This latched status bit is set to 1 when the operating state of the T0 DPLL changes. STATE is cleared when written with a 1 and not set again until the operating state changes again. When STATE is set it can cause an interrupt request on the INTREQ pin if the STATE interrupt enable bit is set in the IER2 register. The current operating state can be read from the T0STATE field of the OPSTATE register. See Section 7.7.1.

**Bit 6: Selected Reference Failed (SRFAIL).** This latched status bit is set to 1 when the selected reference to the T0 DPLL fails (i.e., no clock edges in two UI). SRFAIL is cleared when written with a 1. When SRFAIL is set it can cause an interrupt request on the INTREQ pin if the SRFAIL interrupt enable bit is set in the IER2 register. SRFAIL is not set in free-run mode or holdover mode. See Section 7.5.3.

**Bits 5 to 0: Input Clock Status Change (IC14 to IC9).** Each of these latched status bits is set to 1 when the corresponding VALSR status bit changes state (set or cleared). If soft frequency limit alarms are enabled (MCR10:SOFTEN = 1), then each of these latched status bits is also set to 1 when the corresponding SOFT bit in the ISR registers changes state (set or cleared). Each bit is cleared when written with a 1 and not set again until either the VALSR2 bit or the SOFT bit changes state again. When one of these latched status bits is set it can cause an interrupt request on the INTREQ pin if the corresponding interrupt enable bit is set in the IER2 register. See Section 7.5 for input clock validation/invalidation criteria.

**Register Name:** FREQ3
**Register Description:** Frequency Register 3
**Register Address:** 07h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | — | — | — | FREQ[18:16] | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 2 to 0: Current DPLL Frequency (FREQ[18:16]).** See the FREQ1 register description.

**Register Name:** MSR3
**Register Description:** Master Status Register 3
**Register Address:** 08h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | FSMON | T4LOCK | PHMON | T4NOIN | AMI2 | LOS2 | AMI1 | LOS1 |
| **Default** | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

**Bit 7: Frame Sync Input Monitor Alarm (FSMON).** This latched status bit is set to 1 when OPSTATE:FSMON transitions from 0 to 1. FSMON is cleared when written with a 1. When FSMON is set it can cause an interrupt request on the INTREQ pin if the FSMON interrupt enable bit is set in the IER3 register. See Section 7.9.3.

**Bit 6: T4 DPLL Lock Status Change (T4LOCK).** This latched status bit is set to 1 when the lock status of the T4 DPLL (OPSTATE:T4LOCK) changes (becomes locked when previously unlocked or becomes unlocked when previously locked). T4LOCK is cleared when written with a 1 and not set again until the T4 lock status changes again. When T4LOCK is set it can cause an interrupt request on the INTREQ pin if the T4LOCK interrupt enable bit is set in the IER3 register. See Section 7.7.6.

**Bit 5: Phase Monitor Alarm (PHMON).** This latched status bit is set to 1 when the phase monitor alarm limit has been exceeded (PMLIM field of the PHMON register). PHMON is cleared when written with a 1 and not set again until the threshold is exceeded again. When PHMON is set it can cause an interrupt request on the INTREQ pin if the PHMON interrupt enable bit is set in the IER3 register. See Section 7.7.7.

**Bit 4: T4 No Valid Inputs Alarm (T4NOIN).** This latched status bit is set to 1 when the T4 DPLL has no valid inputs available. T4NOIN is cleared when written with a 1 unless the T4 DPLL still has no valid inputs available. When T4NOIN is set it can cause an interrupt request on the INTREQ pin if the T4NOIN interrupt enable bit is set in the IER3 register. See Section 7.5.

**Bit 3: AMI Violation on IC2 (AMI2).** This latched status bit is set to 1 when a deviation from the expected pattern of seven ones followed by a BPV occurs on the IC2 input in each of two consecutive 8-bit periods. However, if the composite clock receiver can detect the presence of the 400 Hz component required by G.703 Appendix II.1 option b), then the missing BPVs that indicate the 400 Hz component are not considered AMI violations. AMI2 is cleared when written with a 1 and not set again until another AMI violation occurs. When AMI2 is set it can cause an interrupt request on the INTREQ pin if the AMI2 interrupt enable bit is set in the IER3 register. This status bit is only enabled when IC2 is configured as a composite clock receiver (MCR5:IC2SF = 0). See Section 7.10.1.

**Bit 2: LOS Error on IC2 (LOS2).** This latched status bit is set to 1 when no pulses are detected on the IC2 input in a 32µs period (i.e., after two missing pulses). LOS2 is cleared when written with a 1 and is not set again until IC2 transitions from valid signal to loss-of-signal again. When LOS2 is set it can cause an interrupt request on the INTREQ pin if the LOS2 interrupt enable bit is set in the IER3 register. This status bit is only enabled when IC2 is configured as a composite clock receiver (MCR5:IC2SF = 0). See Section 7.10.1.

**Bit 1: AMI Violation on IC1 (AMI1).** This latched status bit is set to 1 when a deviation from the expected pattern of seven ones followed by a BPV occurs on the IC1 input in each of two consecutive 8-bit periods. However, if the composite clock receiver can detect the presence of the 400Hz component required by G.703 Appendix II.1 option b), then the missing BPVs that indicate the 400Hz component are not considered AMI violations. AMI1 is cleared when written with a 1 and not set again until another AMI violation occurs. When AMI1 is set it can cause an interrupt request on the INTREQ pin if the AMI1 interrupt enable bit is set in the IER3 register. This status bit is only enabled when IC1 is configured as a composite clock receiver (MCR5:IC1SF = 0). See Section 7.10.1.

**Bit 0: LOS Error on IC1 (LOS1).** This latched status bit is set to 1 when no pulses are detected on the IC1 input in a 32 µs period (i.e., after two missing pulses). LOS1 is cleared when written with a 1 and is not set again until IC1 transitions from valid signal to loss-of-signal again. When LOS1 is set it can cause an interrupt request on the INTREQ pin if the LOS1 interrupt enable bit is set in the IER3 register. This status bit is only enabled when IC1 is configured as a composite clock receiver (MCR5:IC1SF = 0). See Section 7.10.1.

**Register Name:** OPSTATE
**Register Description:** Operating State Register
**Register Address:** 09h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | FSMON | T4LOCK | T0SOFT | T4SOFT | — | T0STATE[2:0] | | |
| **Default** | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

**Bit 7: Frame Sync Input Monitor Alarm (FSMON).** This real-time status bit indicates the current status of the frame sync input monitor. See Section 7.9.3.

0 = no alarm
1 = alarm

**Bit 6: T4 DPLL Lock Status (T4LOCK).** This real-time status bit indicates the current phase lock status of the T4 DPLL. See Sections 7.5.3 and 7.7.6.

0 = not locked to selected reference
1 = locked to selected reference

**Bit 5: T0 DPLL Frequency Soft Alarm (T0SOFT).** This real-time status bit indicates whether or not the T0 DPLL is tracking its reference within the soft alarm limits specified in the SOFT[6:0] field of the DLIMIT3 register. See Section 7.7.6.

0 = No alarm; frequency is within the soft alarm limits
1 = Soft alarm; frequency is outside the soft alarm limits

**Bit 4: T4 DPLL Frequency Soft Alarm (T4SOFT).** This real-time status bit indicates whether or not the T4 DPLL is tracking its reference within the soft alarm limits specified in the SOFT[6:0] field of the DLIMIT3 register. See Section 7.7.6.

0 = No alarm; frequency is within the soft alarm limits
1 = Soft alarm; frequency is outside the soft alarm limits

**Bits 2 to 0: T0 DPLL Operating State (T0STATE[2:0]).** This real-time status field indicates the current state of the T0 DPLL state machine. Values not listed below correspond to invalid (unused) states. See Section 7.7.1.

001 = Free-run
010 = Holdover
100 = Locked
101 = Prelocked 2
110 = Prelocked
111 = Loss-of-lock

**Register Name:** PTAB1
**Register Description:** Priority Table Register 1
**Register Address:** 0Ah

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | REF1[3:0] | | | | SELREF[3:0] | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 4: Highest Priority Valid Reference (REF1[3:0]).** This real-time status field indicates the highest-priority valid input reference. When T4T0 = 0 in the MCR11 register, this field indicates the highest priority reference for the T0 DPLL. When T4T0 = 1, it indicates the highest priority reference for the T4 DPLL. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 or VALCR2 register. When the T0 DPLL is in non-revertive mode (REVERT = 0 in the MCR3 register) this field may not have the same value as the SELREF[3:0] field. See Section 7.6.2.

0000 = No valid input reference available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 = Input IC5
0110 = Input IC6
0111 = Input IC7
1000 = Input IC8
1001 = Input IC9
1010 = Input IC10
1011 = Input IC11
1100 = Input IC12
1101 = Input IC13
1110 = Input IC14
1111 = {unused value}

**Bits 3 to 0: Selected Reference (SELREF[3:0]).** This real-time status field indicates the current selected reference. When T4T0 = 0 in the MCR11 register, this field indicates the selected reference for the T0 DPLL. When T4T0 = 1, it indicates the selected reference for the T4 DPLL. Note that an input clock cannot be indicated in this field if it has been marked invalid in the VALCR1 or VALCR2 register. When the T0 DPLL is in nonrevertive mode (REVERT = 0 in the MCR3 register) this field may not have the same value as the REF1[3:0] field. See Section 7.6.2.

0000 = No source currently selected
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 = Input IC5
0110 = Input IC6
0111 = Input IC7
1000 = Input IC8
1001 = Input IC9
1010 = Input IC10
1011 = Input IC11
1100 = Input IC12
1101 = Input IC13
1110 = Input IC14
1111 = {unused value}

**Register Name:** PTAB2
**Register Description:** Priority Table Register 2
**Register Address:** 0Bh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | REF3[3:0] | | | | REF2[3:0] | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 4: Third Highest Priority Valid Reference (REF3[3:0]).** This real-time status field indicates the third highest priority validated input reference. When T4T0 = 0 in the MCR11 register, this field indicates the third highest priority reference for the T0 DPLL. When T4T0 = 1, it indicates the third highest reference for the T4 DPLL. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 or VALCR2 register. See Section 7.6.2.

0000 = Less than three valid sources available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 = Input IC5
0110 = Input IC6
0111 = Input IC7
1000 = Input IC8
1001 = Input IC9
1010 = Input IC10
1011 = Input IC11
1100 = Input IC12
1101 = Input IC13
1110 = Input IC14
1111 = {unused value}

**Bits 3 to 0: Second Highest Priority Valid Reference (REF2[3:0]).** This real-time status field indicates the second highest priority validated input reference. When T4T0 = 0 in the MCR11 register, this field indicates the second highest priority reference for the T0 DPLL. When T4T0 = 1, it indicates the second highest reference for the T4 DPLL. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 or VALCR2 register. See Section 7.6.2.

0000 = Less than two valid sources available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 = Input IC5
0110 = Input IC6
0111 = Input IC7
1000 = Input IC8
1001 = Input IC9
1010 = Input IC10
1011 = Input IC11
1100 = Input IC12
1101 = Input IC13
1110 = Input IC14
1111 = {unused value}

**Register Name:** FREQ1
**Register Description:** Frequency Register 1
**Register Address:** 0Ch

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | FREQ[7:0] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The FREQ1, FREQ2, and FREQ3 registers must be read consecutively. See Section 8.3.

**Bits 7 to 0: Current DPLL Frequency (FREQ[7:0]).** The full 19-bit FREQ[18:0] field spans this register, FREQ2 and FREQ3. FREQ is a two's-complement signed integer that expresses the current frequency as an offset with respect to the master clock frequency (see Section 7.3). When T4T0 = 0 in the MCR11 register, FREQ indicates the current frequency offset of the T0 DPLL. When T4T0 = 1, FREQ indicates the current frequency offset of the T4 path. Because the value in this register field is derived from the DPLL integral path, it can be considered an average frequency with a rate of change inversely proportional to the DPLL bandwidth. If LIMINT = 1 in the MCR9 register, the value of FREQ freezes when the DPLL reaches its minimum or maximum frequency. The frequency offset in ppm is equal to FREQ[18:0] x 0.0003068. See Section 7.7.1.6.

Application Note: Frequency measurements are relative, i.e., they measure the frequency of the selected reference with respect to the local oscillator. As such, when a frequency difference exists, it is difficult to distinguish whether the selected reference is off frequency or the local oscillator is off frequency. In systems with timing card redundancy, the use of two timing cards, master and slave, can address this difficulty. Both master and slave have separate local oscillators, and each measures the selected reference. These two measurements provide the necessary information to distinguish which reference is off frequency, if we make the simple assumption that at most one reference has a significant frequency deviation at any given time (i.e., a single point of failure). If both master and slave indicate a significant frequency offset, then the selected reference must be off frequency. If the master indicates a frequency offset but the slave does not, then the master's local oscillator must be off frequency. Likewise, if the slave indicates a frequency offset but the master does not, then slave's local oscillator must be off frequency.

**Register Name:** FREQ2
**Register Description:** Frequency Register 2
**Register Address:** 0Dh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | FREQ[15:8] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Current DPLL Frequency (FREQ[15:8]).** See the FREQ1 register description.

**Register Name:** VALSR1
**Register Description:** Input Clock Valid Status Register 1
**Register Address:** 0Eh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | IC8 | IC7 | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Input Clock Valid Status (IC8 to IC1).** Each of these real-time status bits is set to 1 when the corresponding input clock is valid. An input is valid if it has no active alarms (HARD = 0, ACT = 0, LOCK = 0 in the corresponding ISR register). See also the MSR1 register and Section 7.5.

0 = Invalid
1 = Valid

**Register Name:** VALSR2
**Register Description:** Input Clock Valid Status Register 2
**Register Address:** 0Fh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | FHORDY | SHORDY | IC14 | IC13 | IC12 | IC11 | IC10 | IC9 |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Fast Holdover Frequency Ready (FHORDY).** This real-time status bit is set to 1 when the T0 DPLL has a holdover value that has been averaged over the 8-minute holdover averaging period. See the related latched status bit in MSR4 and Section 7.7.1.6.

**Bit 6: Slow Holdover Frequency Ready (SHORDY).** This real-time status bit is set to 1 when the T0 DPLL has a holdover value that has been averaged over the 110-minute holdover averaging period. See the related latched status bit in MSR4 and Section 7.7.1.6.

**Bits 5 to 0: Input Clock Valid Status (IC14 to IC9).** These bits have the same behavior as the bits in VALSR1 but for the IC9 through IC14 input clocks.

**Register Name:** ISR1
**Register Description:** Input Status Register 1
**Register Address:** 10h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | SOFT2 | HARD2 | ACT2 | LOCK2 | SOFT1 | HARD1 | ACT1 | LOCK1 |
| **Default** | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

**Bit 7: Soft Frequency Limit Alarm for Input Clock 2 (SOFT2).** This real-time status bit indicates a soft frequency limit alarm for input clock 2. If IC2 is the selected reference then SOFT2 is set to 1 when the frequency of IC2 is greater than or equal to the soft limit set in the SRLIMIT register. IF IC2 is not the selected reference then SOFT2 is set to 1 when the frequency of IC2 is greater than or equal to the soft limit set in the ILIMIT register. Soft alarms are disabled by default but can be enabled by setting SOFTEN = 1 in the MCR10 register. A soft alarm does not invalidate an input clock. See Section 7.5.1.

**Bit 6: Hard Frequency Limit Alarm for Input Clock 2 (HARD2).** This real-time status bit indicates a hard frequency limit alarm for input clock 2. If IC2 is the selected reference then HARD2 is set to 1 when the frequency of IC2 is greater than or equal to the hard limit set in the SRLIMIT register. If IC2 is not the selected reference then HARD2 is set to 1 when the frequency of IC2 is greater than or equal to the hard limit set in the ILIMIT register. Hard alarms are enabled by default but can be disabled by setting HARDEN = 0 in the MCR10 register. A hard alarm clears the IC2 status bit in the VALSR1 register, invalidating the IC2 clock. See Section 7.5.1.

**Bit 5: Activity Alarm for Input Clock 2 (ACT2).** This real-time status bit is set to 1 when the leaky bucket accumulator for IC2 reaches the alarm threshold specified in the LBxU register (where ‘x’ in ‘LBxU’ is specified in the BUCKET field of ICR2). An activity alarm clears the IC2 status bit in the VALSR1 register, invalidating the IC2 clock. See Section 7.5.2.

**Bit 4: Phase Lock Alarm for Input Clock 2 (LOCK2).** This status bit is set to 1 if IC2 is the selected reference and the T0 DPLL cannot phase lock to IC2 within the duration specified in the PHLKTO register (default = 100 seconds). A phase lock alarm clears the IC2 status bit in VALSR1, invalidating the IC2 clock. If LKATO = 1 in MCR3 then LOCK2 is automatically cleared after a timeout period of 128 seconds. LOCK2 is a read/write bit. System software can clear LOCK2 by writing 0 to it, but writing 1 is ignored. See Section 7.7.1.

**Bit 3: Soft Frequency Limit Alarm for Input Clock 1 (SOFT1).** This bit has the same behavior as the SOFT2 bit but for the IC1 input clock.

**Bit 2: Hard Frequency Limit Alarm for Input Clock 1 (HARD1).** This bit has the same behavior as the HARD2 bit but for the IC1 input clock.

**Bit 1: Activity Alarm for Input Clock 1 (ACT1).** This bit has the same behavior as the ACT2 bit but for the IC1 input clock.

**Bit 0: Phase Lock Alarm for Input Clock 1 (LOCK1).** This bit has the same behavior as the LOCK2 bit but for the IC1 input clock.

**Register Name:** ISR2, ISR3, ISR4, ISR5, ISR6, ISR7
**Register Description:** Input Status Register 2, 3, 4, 5, 6, 7
**Register Address:** 11h, 12h, 13h, 14h, 15h, 16h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | SOFTn | HARDn | ACTn | LOCKn | SOFTm | HARDm | ACTm | LOCKm |
| **Default** | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

These registers have the same behavior as ISR1 but for the other input clocks, as follows:

| INPUT CLOCKS | REGISTER |
|---|---|
| IC4 and IC3 | ISR2 |
| IC6 and IC5 | ISR3 |
| IC8 and IC7 | ISR4 |
| IC10 and IC9 | ISR5 |
| IC12 and IC11 | ISR6 |
| IC14 and IC13 | ISR7 |

**Register Name:** MSR4
**Register Description:** Master Status Register 4
**Register Address:** 17h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | FHORDY | SHORDY | MRAA | — | IC2NO4 | IC1NO4 | IC2NO8 | IC1NO8 |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Fast Holdover Frequency Ready (FHORDY).** This latched status bit is set to 1 when the T0 DPLL has a holdover value that has been averaged over the 8-minute holdover averaging period. FHORDY is cleared when written with a 1. When FHORDY is set it can cause an interrupt request on the INTREQ pin if the FHORDY interrupt enable bit is set in the IER4 register. See Section 7.7.1.6.

**Bit 6: Slow Holdover Frequency Ready (SHORDY).** This latched status bit is set to 1 when the T0 DPLL has a holdover value that has been averaged over the 110-minute holdover averaging period. SHORDY is cleared when written with a 1. When SHORDY is set it can cause an interrupt request on the INTREQ pin if the SHORDY interrupt enable bit is set in the IER4 register. See Section 7.7.1.6.

**Bit 5: Multiregister Access Aborted (MRAA).** This latched status bit is set to 1 when a multibyte access (read or write) is interrupted by another access to the device. MRAA is cleared when written with a 1. MRAA cannot cause an interrupt to occur. See Section 8.3.

**Bit 3: Input Clock 2 Has No 400Hz Component (IC2NO4).** This latched status bit is set to 1 when the missing BPVs that indicate the 400Hz component cannot be found in a 5ms period (two 400Hz cycles). IC2NO4 is cleared when written with a 1 unless the 400Hz component is still not present. When IC2NO4 is set it can cause an interrupt request on the INTREQ pin if the IC2NO4 interrupt enable bit is set in the IER4 register. This status bit is only enabled when IC2 is configured as a composite clock receiver (MCR5:IC2SF = 0). See Section 7.10.1.

**Bit 2: Input Clock 1 Has No 400Hz Component (IC1NO4).** This latched status bit is set to 1 when the missing BPVs that indicate the 400Hz component cannot be found in a 5ms period (two 400Hz cycles). IC1NO4 is cleared when written with a 1 unless the 400Hz component is still not present. When IC1NO4 is set it can cause an interrupt request on the INTREQ pin if the IC1NO4 interrupt enable bit is set in the IER4 register. This status bit is only enabled when IC1 is configured as a composite clock receiver (MCR5:IC1SF = 0). See Section 7.10.1.

**Bit 1: Input Clock 2 Has No 8kHz Component (IC2NO8).** This latched status bit is set to 1 when the BPVs that indicate the 8kHz component cannot be found in the incoming signal in a 500µs period (four 8kHz cycles). IC2NO8 is cleared when written with a 1 unless the 8kHz component is still not present. When IC2NO8 is set it can cause an interrupt request on the INTREQ pin if the IC2NO8 interrupt enable bit is set in the IER4 register. This status bit is only enabled when IC2 is configured as a composite clock receiver (MCR5:IC2SF = 0). See Section 7.10.1.

**Bit 0: Input Clock 1 Has No 8kHz Component (IC1NO8).** This latched status bit is set to 1 when the BPVs that indicate the 8kHz component cannot be found in the incoming signal in a 500µs period (four 8kHz cycles). IC1NO8 is cleared when written with a 1 unless the 8kHz component is still not present. When IC1NO8 is set it can cause an interrupt request on the INTREQ pin if the IC1NO8 interrupt enable bit is set in the IER4 register. This status bit is only enabled when IC1 is configured as a composite clock receiver (MCR5:IC1SF = 0). See Section 7.10.1.

**Register Name:** IPR1
**Register Description:** Input Priority Register 1
**Register Address:** 18h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | PRI2[3:0] | | | | PRI1[3:0] | | | |
| **Default (T0)** | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| **Default (T4)** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 4: Priority for Input Clock 2 (PRI2).** Priority 0001 is highest; priority 1111 is lowest. When MCR11:T4T0 = 0, PRI2 configures IC2's priority for the T0 DPLL. When T4T0 = 1, PRI2 configures IC2's priority for the T4 path. See Section 7.6.1.

0000 = IC2 unavailable for selection.
0001–1111= IC2 relative priority

**Bits 3 to 0: Priority for Input Clock 1 (PRI1).** Priority 0001 is highest; priority 1111 is lowest. When MCR11:T4T0 = 0, PRI1 configures IC1's priority for the T0 DPLL. When T4T0 = 1, PRI1 configures IC1's priority for the T4 path. See Section 7.6.1.

0000 = IC1 unavailable for selection.
0001–1111 = IC1 relative priority

**Register Name:** IPR2, IPR3, IPR4, IPR5, IPR6, IPR7
**Register Description:** Input Priority Register 2, 3, 4, 5, 6, 7
**Register Address:** 19h, 1Ah, 1Bh, 1Ch, 1Dh, 1Eh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | PRIn[3:0] | | | | PRIm[3:0] | | | |
| **Default** | see table | | | | | | | |

These registers have the same behavior as IPR1 but for the other input clocks, as follows:

| INPUT CLOCKS | REGISTER | DEFAULT (T0) | DEFAULT (T4) |
|---|---|---|---|
| IC4 and IC3 | IPR2 | 0101 0100 | 0000 0000 |
| IC6 and IC5 | IPR3 | 0111 0110 | 0111 0110 |
| IC8 and IC7 | IPR4 | 1001 1000 | 1001 1000 |
| IC10 and IC9 | IPR5 | 1011 1010 | 1011 1010 |
| IC12 and IC11 | IPR6 | 1101 1100 or 1101 0001* | 0000 0000 |
| IC14 and IC13 | IPR7 | 1111 1110 | 0000 0000 |

**In register IPR6, for the T0 path, if the MASTSLV pin is high (master mode) when $\overline{RST}$ = 0 then the default priority of input IC11 (PRI11) is 12. If the MASTSLV pin is low (slave mode) when $\overline{RST}$ = 0, then the default priority of IC11 is 1. When the device is in slave mode values written to PRI11[3:0] are latched, but the value read is always 0001 to indicate that input 11 is forced to have priority 1. See Section 7.9.1.*

**Register Name:** ICR1, ICR2, ICR3, ICR4, ICR5, ICR6, ICR7, ICR8, ICR9, ICR10, ICR11, ICR12, ICR13, ICR14
**Register Description:** Input Configuration Register 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14
**Register Address:** 20h, 21h, 22h, 23h, 24h, 25h, 26h, 27h, 28h, 29h, 2Ah, 2Bh, 2Ch, 2Dh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | DIVN | LOCK8K | BUCKET[1:0] | | FREQ[3:0] | | | |
| **Default** | 0 | 0 | 0 | 0 | See below | | | |

These registers are identical in function. ICRx is the control register for input clock ICx.

**Bit 7: DIVN Mode (DIVN).** When DIVN is set to 1, the input clock is divided down by a programmable pre-divider. The resulting output clock is then passed to the DPLL and frequency monitor. All input clocks for which DIVN = 1 are divided by the factor specified in DIVN1 and DIVN2. When DIVN = 1 in an ICR register, the FREQ field of that register must be set to 8kHz. See Section 7.4.2.3.

0 = Disabled
1 = Enabled

**Bit 6: LOCK8K Mode (LOCK8K).** When LOCK8K is set to 1, the input clock is divided down by a preset predivider. The resulting output clock, which is always 8kHz, is then passed to the DPLL. LOCK8K is ignored when DIVN = 1. LOCK8K is also ignored when DIVN = 0 and FREQ[3:0] = 1001 (2kHz) or 1010 (4kHz). See Section 7.4.2.2.

0 = Disabled
1 = Enabled

**Bits 5 to 4: Leaky Bucket Configuration (BUCKET[1:0]).** Each input clock has leaky bucket accumulator logic in its activity monitor. The LBxy registers at addresses 50h to 5Fh specify four different leaky bucket configurations. Any of the four configurations can be specified for the input clock. See Section 7.5.2.

00 = leaky bucket configuration 0
01 = leaky bucket configuration 1
10 = leaky bucket configuration 2
11 = leaky bucket configuration 3

**Bits 3 to 0: Input Clock Nominal Frequency (FREQ[3:0]).** This field specifies the input clock's nominal frequency. FREQ must be set to 0000 if DIVN = 1. See Section 7.4.2.

0000 = 8kHz
0001 = 1544kHz or 2048kHz (as determined by SONSDH bit in the MCR3 register)
0010 = 6.48MHz
0011 = 19.44MHz
0100 = 25.92MHz
0101 = 38.88MHz
0110 = 51.84MHz
0111 = 77.76MHz
1000 = 155.52MHz (only valid for IC5 and IC6)
1001 = 2kHz
1010 = 4kHz
1011 = 6312kHz
1100–1111 {unused values}

**FREQ[3:0] Default Values:**

| | |
|---|---|
| ICR1–ICR4: | 0000b |
| ICR5–ICR10: | 0011b |
| ICR11: | 0010b if MASTSLV = 0<br>0011b if MASTSLV = 1 |
| ICR12–ICR14: | 0001b |

Note that the ICR11 default value is set based on the state of the MASTSLV pin when the $\overline{RST}$ pin is asserted. See Section 7.12.

**Register Name:** VALCR1
**Register Description:** Input Clock Valid Control Register 1
**Register Address:** 30h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | IC8 | IC7 | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| **Default** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Bits 7 to 0: Input Clock Valid Control (IC8 to IC1).** These control bits can be used to force input clocks to be considered invalid. If a clock is invalidated by one of these control bits it will not appear in the priority table in the PTAB1 and PTAB2 registers, even if the clock is otherwise valid. One key application for these control bits is to force clocks invalid that are declared invalid in the other DS3101 device of a redundant pair. Note that setting a VALCR bit low has no effect on the corresponding bit in the VALSR registers. See Sections 7.6.2 and 7.9.1.

0 = Force invalid
1 = Do not force invalid; determine validity normally

**Register Name:** VALCR2
**Register Description:** Input Clock Valid Control Register 2
**Register Address:** 31h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | IC14 | IC13 | IC12 | IC11 | IC10 | IC9 |
| **Default** | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

**Bits 5 to 0: Input Clock Valid Control (IC14 to IC9).** These bits have the same behavior as the bits in VALCR1 but for the IC9 through IC14 input clocks.

**Register Name:** MCR1
**Register Description:** Master Configuration Register 1
**Register Address:** 32h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | RST | — | — | — | — | T0STATE[2:0] | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Device Reset (RST).** When this bit is high the entire device is held in reset, and all register fields, except the RST bit itself, are reset to their default states. When RST is active, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. Instead these fields are reset to the default values that were latched from the pins when the $\overline{RST}$ pin was last active. See Section 7.12.

0 = Normal operation
1 = Reset

**Bits 2 to 0: T0 DPLL State Control (T0STATE).** This field allows the T0 DPLL state machine to be forced to a specified state. The state machine will remain in the forced state, and therefore cannot react to alarms and other events, as long as T0STATE is not equal to 000. See Section 7.7.1.

000 = Automatic (normal state machine operation)
001 = Free-run
010 = Holdover
011 = {unused value}
100 = Locked
101 = Prelocked 2
110 = Prelocked
111 = Loss-of-lock

**Register Name:** MCR2
**Register Description:** Master Configuration Register 2
**Register Address:** 33h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | — | — | T0FORCE[3:0] | | | |
| **Default** | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**Bits 3 to 0: T0 DPLL Force Selected Reference (T0FORCE[3:0]).** This field provides a way to force a specified input clock to be the selected reference for the T0 DPLL. Internally this is accomplished by forcing the clock to have the highest priority (as specified in PTAB1:REF1). In revertive mode (MCR3:REVERT = 1) the forced clock automatically becomes the selected reference (as specified in PTAB1:SELREF) as well. In nonrevertive mode, the forced clock only becomes the selected reference when the existing selected reference is invalidated or made unavailable for selection.

When a reference is forced, the activity monitor and frequency monitor for that input and the T0 DPLL's loss-of-lock timeout logic all continue to operate and affect the relevant ISR, VALSR and MSR register bits. However, when the reference is declared invalid the T0 DPLL is not allowed to switch to another input clock. The T0 DPLL continues to respond to the fast activity monitor and the invalidate-on-event logic in the CC receivers (register MCR5), transitioning to miniholdover in response to short-term events and to full holdover in response to longer events. See Section 7.6.3.

0000 = Automatic source selection (normal operation)
0001 = Force to IC1
0010 = Force to IC2
0011 = Force to IC3
0100 = Force to IC4
0101 = Force to IC5
0110 = Force to IC6
0111 = Force to IC7
1000 = Force to IC8
1001 = Force to IC9
1010 = Force to IC10
1011 = Force to IC11
1100 = Force to IC12
1101 = Force to IC13
1110 = Force to IC14
1111 = Automatic source selection (normal operation)

**Register Name:** MCR3
**Register Description:** Master Configuration Register 3
**Register Address:** 34h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | AEFSEN | LKATO | XOEDGE | MANHO | EFSEN | SONSDH | MASTSLV | REVERT |
| **Default** | 1 | 1 | 0 | 0 | 0 | see below | see below | 0 |

**Bit 7: Auto External Frame Sync Enable (AEFSEN).** See Section 7.9.3.
0 = EFSEN bit (bit 3 below) enables and disables the external frame sync on the SYNC2K pin
1 = The external frame sync is enabled when EFSEN = 1 and the T0 DPLL is locked to the input clock specified in the SOURCE field of FSCR3.

**Bit 6: Phase Lock Alarm Timeout (LKATO).** This bit controls how phase alarms on input clocks can be terminated. Phase alarms are indicated by the LOCK bits in ISR registers
0 = Phase alarms on input clocks can only be cancelled by software
1 = Phase alarms are automatically cancelled after a timeout period of 128 seconds

**Bit 5: Local Oscillator Edge (XOEDGE).** This bit specifies the significant clock edge of the local oscillator clock signal on the REFCLK input pin. The faster edge should be selected for best jitter performance. See Section 7.3.
0 = Rising edge
1 = Falling edge

**Bit 4: Manual Holdover (MANHO).** When this bit is set to 1 the T0 DPLL holdover frequency is set by the HOFREQ field in the HOCR1, HOCR2 and HOCR3 registers. When MANHO = 1 it has priority over any other holdover control fields. See Section 7.7.1.6.
0 = Standard holdover: holdover frequency is learned by the T0 DPLL from the selected reference
1 = Manual holdover: holdover frequency is taken from the HOFREQ field

**Bit 3: External Frame Sync Enable (EFSEN).** When this bit is set to 1 the T0 DPLL looks for a reference frame sync pulse on the SYNC2K pin. See the AEFSEN bit description above for more information. See Section 7.9.3.
0 = Disable external frame sync; ignore SYNC2K pin
1 = Enable external frame sync on SYNC2K pin

**Bit 2: SONET or SDH Frequencies (SONSDH).** This bit specifies the clock rate for input clocks with FREQ=0001 in the ICR registers (20h to 2Dh). During reset the default value of this bit is latched from the SONSDH pin. See Section 7.4.2.
0 = 2048kHz
1 = 1544 Hz

**Bit 1: Master or Slave Configuration (MASTSLV).** This read-only bit indicates the state of the MASTSLV pin. This bit therefore does not have a fixed default value. To disable the master-slave pin feature and give software the ability to configure devices as either master or slave, wire the MASTSLV pin high (master mode) on both devices. See Section 7.9.
0 = Slave Mode. In this mode input clock IC11 is set to priority 1 (highest), the T0 DPLL is set to acquisition bandwidth, revertive mode is enabled, and phase build-out is disabled.
1 = Master Mode. In this mode all setting are configured by configuration registers.

**Bit 0: Revertive Mode (REVERT).** This bit configures the T0 DPLL for revertive or non-revertive operation. (The T4 DPLL is always revertive). In revertive mode, if an input clock with a higher priority than the selected reference becomes valid, the higher-priority reference immediately becomes the selected reference. In nonrevertive mode, the higher priority reference does not immediately become the selected reference but does become the highest-priority reference in the priority table (REF1 field in the PTAB1 register). See Section 7.6.2.

When the device is in slave mode (MASTSLV pin = 0) values written to this field are latched, but the value read is always 1 to indicate that the device is forced into revertive mode. See Section 7.9.1.
0 = Nonrevertive mode
1 = Revertive mode

**Register Name:** MCR4
**Register Description:** Master Configuration Register 4
**Register Address:** 35h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | LKT4T0 | T4DFB | — | OC89 | T4FORCE[3:0] | | | |
| **Default** | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Lock T4 to T0 (LKT4T0).** When this bit is set to 0 the T4 path operates independently from the T0 path. When it is set to 1 the T4 path locks to the output of the T0 DPLL, which allows the T4 path to be used to synthesize additional clock frequencies that are locked to the T0 reference. See Section 7.8.2.2.

0 = T4 path operates independently from T0 path
1 = T4 DPLL locks to the output of the T0 DPLL

**Bit 6: T4 Digital Feedback Mode (T4DFB).** See Section 7.8.2.2.

0 = Analog feedback mode
1 = Digital feedback mode

**Bit 4: Source Control for Clock Outputs 8 and 9 (OC89).** See Section 7.8.2.4.

0 = OC8 and OC9 generated from T4 DPLL
1 = OC8 and OC9 generated from T0 DPLL

**Bits 3 to 0: T4 DPLL Force Selected Reference (T4FORCE[3:0]).** This field provides a way to force a specified input clock to be the selected reference for the T4 DPLL. Internally this is accomplished by forcing the clock to have the highest priority (as specified in PTAB1:REF1). Since the T4 DPLL always operates in revertive mode, the forced clock automatically becomes the selected reference (as specified in PTAB1:SELREF) as well.

When a reference is forced, the activity monitor and frequency monitor for that input continue to operate and affect the relevant ISR, VALSR and MSR register bits. However, when the reference is declared invalid, the T4 DPLL is not allowed to switch to another input clock. See Section 7.6.3.

0000 = Automatic (normal operation)
0001 = Force to IC1
0010 = Force to IC2
0011 = Force to IC3
0100 = Force to IC4
0101 = Force to IC5
0110 = Force to IC6
0111 = Force to IC7
1000 = Force to IC8
1001 = Force to IC9
1010 = Force to IC10
1011 = Force to IC11
1100 = Force to IC12
1101 = Force to IC13
1110 = Force to IC14
1111 = Automatic (normal operation)

**Register Name:** MCR5
**Register Description:** Master Configuration Register 5
**Register Address:** 36h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | CCEDGE | BITERR | AMI | LOS | IC2SF | IC1SF | IC6SF | IC5SF |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**Bit 7: Composite Clock 8kHz Edge (CCEDGE).** This bit specifies the 8kHz clock edge in the incoming composite clock signals on inputs IC1 and IC2. See Section 7.10.1.
0 = The leading edge of the pulse following the BPV
1 = The leading edge of the BPV

**Bit 6: Increment the Activity Monitor on Bit Errors (BITERR).** If this bit is set to 1, then the detection of a deviation from the one-BPV-in-eight pattern on IC1 or IC2 (in composite clock mode) is considered an irregularity by the corresponding activity monitor. The activity monitors increment their leaky bucket accumulators once for each 128ms interval in which irregularities occur. See Section 7.10.1.
0 = Bit errors do not increment the input clock activity monitors
1 = Bit errors do increment the input clock activity monitors

**Bit 5: Invalidate on AMI Violation (AMI).** If this bit is set to 1, then the detection of a deviation from the one-BPV-in-eight pattern in each of two consecutive 8-bit periods on IC1 or IC2 (in composite clock mode) automatically invalidates the offending clock. See Section 7.10.1.
0 = Do not invalidate on AMI violation
1 = Invalidate on incorrect AMI violation

**Bit 4: Invalidate on Loss of Signal (LOS).** If this bit is set to 1, then the detection of two consecutive zeros on IC1 or IC2 (in composite clock mode) automatically invalidates the offending clock. See Section 7.10.1.
0 = Do not invalidate on LOS
1 = Invalidate on LOS

**Bit 3: Input Clock 2 Signal Format (IC2SF).** See Section 7.10.1.
0 = AMI 64kHz composite clock on the IC2A pin
1 = CMOS/TTL on the IC2 pin

**Bit 2: Input Clock 1 Signal Format (IC1SF).** See Section 7.10.1.
0 = AMI 64 kHz composite clock on the IC1A pin
1 = CMOS/TTL on the IC1 pin

**Bit 1: Input Clock 6 Signal Format (IC6SF).** For backward compatibility this bit can be written to and read back, but it does not affect the IC6POS/NEG inputs pins. See Section 7.4.1.
0 = LVDS compatible
1 = LVPECL compatible (default)

**Bit 0: Input Clock 5 Signal Format (IC5SF).** For backward compatibility this bit can be written to and read back, but it does not affect the IC6POS/NEG inputs pins. See Section 7.4.1.
0 = LVDS compatible (default)
1 = LVPECL compatible

**Register Name:** IFSR
**Register Description:** Microprocessor Interface Selection Status Register
**Register Address:** 37h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | — | — | — | IFSEL[2:0] | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | set by IFSEL[2:0] pins when $\overline{RST}$ = 0 | | |

**Bits 2 to 0: Microprocessor Interface Selection (IFSEL[2:0]).** This read-only field shows the current state of the IFSEL[2:0] pins. When $\overline{RST}$ = 0 the state of the IFSEL pins is latched into the microprocessor interface control register (IFCR). After $\overline{RST}$ is brought high, the IFSEL pins are ignored by the interface control logic and can be used as general purpose inputs whose values are shown in this register field. See Section 7.10.

**Register Name:** MCR6
**Register Description:** Master Configuration Register 6
**Register Address:** 38h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | DIG2AF | DIG2SS | DIG1SS | — | — | — | — | — |
| **Default** | 0 | see below | see below | 1 | 1 | 1 | 1 | 1 |

**Bit 7: Digital2 Alternate Frequency (DIG2AF).** See Section 7.8.2.1.
0 = Digital2 frequency specified by DIG2SS and MCR7:DIG2F.
1 = Digital2 frequency is 6312kHz (must set DIG2SS = 0 and MCR7:DIG2F = 00)

**Bit 6: Digital2 SONET or SDH Frequencies (DIG2SS).** This bit specifies whether the clock rates generated by the Digital2 clock synthesizer are multiples of 1.544MHz (SONET compatible) or multiples of 2.048MHz (SDH compatible). The specific multiple is set in the DIG2F field of the MCR7 register. When $\overline{RST}$ = 0 the default value of this bit is latched from the SONSDH pin. See Section 7.8.2.1.
0 = Multiples of 2048kHz
1 = Multiples of 1544kHz

**Bit 5: Digital1 SONET or SDH Frequencies (DIG1SS).** This bit specifies whether the clock rates generated by the Digital1 clock synthesizer are multiples of 1544kHz (SONET compatible) or multiples of 2048kHz (SDH compatible). The specific multiple is set in the DIG1F field of the MCR7 register. When $\overline{RST}$ = 0 the default value of this bit is latched from the SONSDH pin. See Section 7.8.2.1.
0 = Multiples of 2048kHz
1 = Multiples of 1544kHz

**Register Name:** MCR7
**Register Description:** Master Configuration Register 7
**Register Address:** 39h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | DIG2F[1:0] | | DIG1F[1:0] | | — | — | — | — |
| **Default** | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Bits 7 to 6: Digital2 Frequency (DIG2F[1:0]).** This field and DIG2SS of MCR6 configure the frequency of the Digital2 clock synthesizer. See Section 7.8.2.1.

| DIG2SS = 1 | DIG2SS = 0 |
|---|---|
| 00 = 1544kHz | 00 = 2048kHz |
| 01 = 3088kHz | 01 = 4096kHz |
| 10 = 6176kHz | 10 = 8192kHz |
| 11 = 12352kHz | 11 = 16384kHz |

**Bits 5 to 4: Digital1 Frequency (DIG1F[1:0]).** This field and DIG1SS of MCR6 configure the frequency of the Digital1 clock synthesizer. See Section 7.8.2.1.

| DIG1SS = 1 | DIG1SS = 0 |
|---|---|
| 00 = 1544kHz | 00 = 2048kHz |
| 01 = 3088kHz | 01 = 4096kHz |
| 10 = 6176kHz | 10 = 8192kHz |
| 11 = 12352kHz | 11 = 16384kHz |

**Register Name:** MCR8
**Register Description:** Master Configuration Register 8
**Register Address:** 3Ah

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | OC8400 | OC8NO8 | OC7SF | | OC6SF | |
| **Default** | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

**Bit 5: Output Clock 8, 400Hz Component Enable (OC8400).** See Section 7.10.2.
0 = 400 Hz component disabled
1 = 400 Hz component enabled

**Bit 4: Output Clock 8, 8kHz Component Disable (OC8NO8).** See Section 7.10.2.
0 = 8 kHz component enabled
1 = 8 kHz component disabled

**Bits 3 to 2: Output Clock 7 Control (OC7SF[1:0]).** See Section 7.8.1.
00 = Output disabled
01 = 3V LVDS compatible (default)
10 = 3V LVDS compatible
11 = 3V LVDS compatible

**Bits 1 to 0: Clock Output 6 Control (OC6SF[1:0]).** See Section 7.8.1.
00 = Output disabled
01 = 3V LVDS compatible
10 = 3V LVDS compatible (default)
11 = 3V LVDS compatible

**Register Name:** MCR9
**Register Description:** Master Configuration Register 9
**Register Address:** 3Bh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | AUTOBW | — | — | — | LIMINT | PFD180 | — | — |
| **Default** | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

**Bit 7: Automatic Bandwidth Selection (AUTOBW).** When the device is in slave mode (MASTSLV pin = 0), this field is ignored and the T0 DPLL is forced to use acquisition bandwidth. See Section 7.7.3.

0 = Always selects locked bandwidth from the T0LBW register
1 = Automatically selects either locked bandwidth (T0LBW register) or acquisition bandwidth (T0ABW register) as appropriate

**Bit 3: Limit Integral Path (LIMINT).** When this bit is set to 1, the T0 DPLL's integral path is limited (i.e., frozen) when the DPLL reaches minimum or maximum frequency, as set by the HARDLIM field in DLIMIT1 and DLIMIT2. When the integral path is frozen, the current DPLL frequency in registers FREQ1, FREQ2 and FREQ3 is also frozen. Setting LIMINT = 1 minimizes overshoot when the DPLL is pulling in. See Section 7.7.3.

0 = Do not freeze integral path at min/max frequency
1 = Freeze integral path at min/max frequency

**Bit 2: 180° PFD Enable (PFD180).** If TEST1:D180 = 1, then PFD180 has no effect.

0 = Use 180° phase detector (nearest edge locking mode)
1 = Use 180° phase-frequency detector

**Register Name:** MCLK1
**Register Description:** Master Clock Frequency Adjustment Register 1
**Register Address:** 3Ch

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | MCLKFREQ[7:0] | | | | | | | |
| **Default** | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

The MCLK1 and MCLK2 registers must be read consecutively and written consecutively. See Section 8.3.

**Bits 7 to 0: Master Clock Frequency Adjustment (MCLKFREQ[7:0]).** The full 16-bit MCLKFREQ[15:0] field spans this register and MCLK2. MCLKFREQ is an unsigned integer that adjusts the frequency of the internal 204.8MHz master clock with respect to the frequency of the local oscillator clock on the REFCLK pin by up to +514ppm and -771ppm. The master clock adjustment has the effect of speeding up the master clock with a positive adjustment and slowing it down with a negative adjustment. For example, if the oscillator connected to REFCLK has an offset of +1ppm then the adjustment should be -1ppm to correct the offset.

The formulas below translate adjustments to register values and vice versa. The default register value of 39,321 corresponds to 0ppm. See Section 7.3.

MCLKFREQ[15:0] = adjustment_in_ppm / 0.0196229 + 39,321

adjustment_in_ppm = ( MCLKFREQ[15:0] - 39,321 ) x 0.0196229

**Register Name:** MCLK2
**Register Description:** Master Clock Frequency Adjustment Register 2
**Register Address:** 3Dh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | MLCKFREQ[15:8] | | | | | | | |
| **Default** | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

**Bits 7 to 0: Master Clock Frequency Adjustment (MCLKFREQ[15:8]).** See the MCLK1 register description.

**Register Name:** HOCR1
**Register Description:** Holdover Configuration Register 1
**Register Address:** 3Eh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | HOFREQ[7:0] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Holdover Frequency (HOFREQ[7:0]).** The full 19-bit HOFREQ[18:0] field spans this register, HOCR2 and HOCR3. HOFREQ is a two's-complement signed integer, and it expresses the holdover frequency as an offset with respect to the master clock frequency (see Section 7.3). Writing this field sets the T0 DPLL's manual holdover frequency, which is used when MANHO = 1 in the MCR3 register. When HOCR3:RDAVG = 0, reading the HOFREQ field returns the manual holdover value previously written. When RDAVG = 1, reading the HOFREQ field returns the T0 DPLL's averaged frequency, either the fast average (if HOCR3:FAST = 1) or the slow average (if FAST = 0). The HOFREQ field has the same size and format as the FREQ[18:0] field (FREQ1, FREQ2 and FREQ3 registers) to allow software to read FREQ, filter the value, and then write to HOFREQ. Holdover frequency offset in ppm is equal to HOFREQ[18:0] x 0.0003068. See Section 7.7.1.6.

Note: After either HOCR3:RDAVG or HOCR3:FAST is changed, system software must wait at least 50µs before reading the corresponding holdover value from the HOFREQ[18:0] field.

**Register Name:** HOCR2
**Register Description:** Holdover Configuration Register 2
**Register Address:** 3Fh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | HOFREQ[15:8] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Holdover Frequency (HOFREQ[15:8]).** See the HOCR1 register description.

**Register Name:** HOCR3
**Register Description:** Holdover Configuration Register 3
**Register Address:** 40h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | AVG | FAST | RDAVG | MINIHO[1:0] | | HOFREQ[18:16] | | |
| **Default** | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

See Section 8.3 for important information about writing and reading this register.

**Bit 7: Averaging (AVG).** When this bit is set to 1 the T0 DPLL uses the averaged frequency value during holdover mode. When MANHO = 1 in the MCR3 register, this bit is ignored. See Section 7.7.1.6.
0 = Not averaged frequency; holdover frequency is either manual (MANHO = 1) or instantaneously frozen
1 = Averaged frequency (averaging rate set by the FAST bit below)

**Bit 6: Fast Averaging (FAST).** This bit controls the averaging rate used in the T0 DPLL's frequency averager. Fast averaging has a -3dB response point of approximately 8 minutes. Slow averaging has a -3dB response point of approximately 110 minutes. See Section 7.7.1.6.
0 = Slow frequency averaging
1 = Fast frequency averaging

**Bit 5: Read Average (RDAVG).** This bit controls which value is accessed when reading the HOFREQ field: the manual holdover frequency or the T0 DPLL's averaged frequency. This allows control software, optionally, to make use of the averager and manual holdover mode in a software-controlled holdover algorithm. See Section 7.7.1.6.
0 = Read the manual holdover frequency value previously written
1 = Read the averaged frequency

**Bits 4 to 3: Miniholdover Mode (MINIHO).** Miniholdover is the state of the T0 DPLL where it is in the locked state but has temporarily lost its input. In miniholdover the DPLL behaves exactly the same as in holdover but with holdover frequency selected as specified by this field. See Section 7.7.1.7.
00 = frequency determined in the same way as holdover mode
01 = frequency instantaneously frozen (i.e., as if AVG = 0)
10 = frequency taken from fast averager (i.e., as if AVG = 1 and FAST = 1)
11 = frequency taken from slow averager (i.e., as if AVG = 1 and FAST = 0)

**Bits 2 to 0: Holdover Frequency (HOFREQ[18:16]).** See the HOCR1 register description.

**Register Name:** DLIMIT1
**Register Description:** DPLL Frequency Limit Register 1
**Register Address:** 41h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | HARDLIM[7:0] | | | | | | | |
| **Default** | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

The DLIMIT1 and DLIMIT2 registers must be read consecutively and written consecutively. See Section 8.3.

**Bits 7 to 0: DPLL Hard Frequency Limit (HARDLIM[7:0]).** The full 10-bit HARDLIM[9:0] field spans this register and DLIMIT2. HARDLIM is an unsigned integer that specifies the hard frequency limit or pull-in/hold-in range of the T0 DPLL. When frequency limit detection is enabled by setting FLLOL = 1 in the DLIMIT3 register, if the DPLL frequency exceeds the hard limit then the DPLL declares loss-of-lock. The hard frequency limit in ppm is ±HARDLIM[9:0] x 0.078. The default value is normally ±9.2ppm. If external reference switching mode is enabled during reset (see Section 7.6.5), the default value is configured to ±79.794ppm (3FFh). See Section 7.7.6.

**Register Name:** DLIMIT2
**Register Description:** DPLL Frequency Limit Register 2
**Register Address:** 42h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | — | — | — | — | HARDLIM[9:8] | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 1 to 0: DPLL Hard Frequency Limit (HARDLIM[9:8]).** See the DLIMIT1 register description.

**Register Name:** IER1
**Register Description:** Interrupt Enable Register 1
**Register Address:** 43h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | IC8 | IC7 | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Interrupt Enable for Input Clock Status Change (IC8 to IC1).** Each of these bits is an interrupt enable control for the corresponding bit in the MSR1 register.

0 = Mask the interrupt
1 = Enable the interrupt

**Register Name:** IER2
**Register Description:** Interrupt Enable Register 2
**Register Address:** 44h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | STATE | SRFAIL | IC14 | IC13 | IC12 | IC11 | IC10 | IC9 |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Interrupt Enable for T0 DPLL State Change (STATE).** This bit is an interrupt enable for the STATE bit in the MSR2 register.

0 = Mask the interrupt
1 = Enable the interrupt

**Bit 6: Interrupt Enable for Selected Reference Failed (SRFAIL).** This bit is an interrupt enable for the SRFAIL bit in the MSR2 register.

0 = Mask the interrupt
1 = Enable the interrupt

**Bits 5 to 0: Interrupt Enable for Input Clock Status Change (IC14 to IC9).** Each of these bits is an interrupt enable control for the corresponding bit in the MSR2 register.

0 = Mask the interrupt
1 = Enable the interrupt

**Register Name:** IER3
**Register Description:** Interrupt Enable Register 3
**Register Address:** 45h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | FSMON | T4LOCK | PHMON | T4NOIN | AMI2 | LOS2 | AMI1 | LOS1 |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Interrupt Enable for Frame Sync Input Monitor Alarm (FSMON).** This bit is an interrupt enable for the FSMON bit in the MSR3 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Bit 6: Interrupt Enable for T4 DPLL Lock Status Change (T4LOCK).** This bit is an interrupt enable for the T4LOCK bit in the MSR3 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Bit 5: Interrupt Enable for Phase Monitor Alarm (PHMON).** This bit is an interrupt enable for the PHMON bit in the MSR3 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Bit 4: Interrupt Enable for T4 No Valid Inputs Alarm (T4NOIN).** This bit is an interrupt enable for the T4NOIN bit in the MSR3 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Bit 3: Interrupt Enable for AMI Violation on IC2 (AMI2).** This bit is an interrupt enable for the AMI2 bit in the MSR3 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Bit 2: Interrupt Enable for LOS Error on IC2 (LOS2).** This bit is an interrupt enable for the LOS2 bit in the MSR3 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Bit 1: Interrupt Enable for AMI Violation on IC1 (AMI1).** This bit is an interrupt enable for the AMI1 bit in the MSR3 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Bit 0: Interrupt Enable for LOS Error on IC1 (LOS1).** This bit is an interrupt enable for the LOS1 bit in the MSR3 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Register Name:** DIVN1
**Register Description:** DIVN Register 1
**Register Address:** 46h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | DIVN[7:0] | | | | | | | |
| **Default** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The DIVN1 and DIVN2 registers must be read consecutively and written consecutively. See Section 8.3.

**Bits 7 to 0: DIVN Factor (DIVN[7:0]).** The full 15-bit DIVN[14:0] field spans this register and DIVN2. This field contains the integer value used to divide the frequency of input clocks that are configured for DIVN mode (DIVN = 1 in registers ICR1 through ICR14). The frequency is divided by DIVN[14:0] + 1.

DIVN mode supports a maximum input frequency of 155.52MHz; therefore, the maximum value of DIVN[14:0] is 19,439 (i.e., 155.52MHz / 8kHz - 1). Performance with DIVN values greater than 19,439 is undefined. See Section 7.4.2.3.

**Register Name:** DIVN2
**Register Description:** DIVN Register 2
**Register Address:** 47h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | DIVN[14:8] | | | | | | |
| **Default** | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

**Bits 5 to 0: DIVN Factor (DIVN [14:8]).** See the DIVN1 register description.

**Register Name:** MCR10
**Register Description:** Master Configuration Register 10
**Register Address:** 48h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | FMONCLK | SRFPIN | UFSW | EXTSW | PBOFRZ | PBOEN | SOFTEN | HARDEN |
| **Default** | 0 | 0 | 0 | see below | 0 | 1 | 0 | 1 |

**Bit 7: Frequency Monitor Clock Source (FMONCLK).** This bit specifies the clock source for the input clock frequency monitors.
0 = T0 DPLL output
1 = Internal master clock

**Bit 6: SRFAIL Pin Enable (SRFPIN).** When this bit is set to 1, the SRFAIL pin is enabled. When enabled the SRFAIL pin follows the state of the SRFAIL status bit in the MSR2 register. This gives the system a very fast indication of the failure of the current reference. See Section 7.5.3.
0 = SRFAIL pin disabled (low)
1 = SRFAIL pin enabled

**Bit 5: Ultra-Fast Switching Mode (UFSW).** See Section 7.6.4.
0 = Disabled
1 = Enabled. The current reference source is disqualified after less than three missing clock cycles.

**Bit 4: External Reference Switching Mode (EXTSW).** This bit enables external reference switching mode. In this mode, if the SRCSW pin is high the T0 DPLL is forced to lock to input IC3 (if the priority of IC3 is nonzero) or IC5 (if the priority of IC3 is zero) whether or not the selected input has a valid reference signal. If the SRCSW pin is low the device is forced to lock to input IC4 (if the priority of IC4 is nonzero) or IC6 (if the priority of IC4 is zero) whether or not the selected input has a valid reference signal. During reset the default value of this bit is latched from the SRCSW pin. This mode only controls the T0 DPLL. The T4 DPLL is not affected. See Section 7.6.5.
0 = Normal operation
1 = External switching mode

**Bit 3: Phase Build-Out Freeze (PBOFRZ).** This bit freezes the current input-output phase relationship and does not allow further phase build-out events to occur. This bit affects phase build-out in response to input transients (Section 7.7.7.2) and phase build-out during reference switching (Section 7.7.7.3).
0 = Not frozen
1 = Frozen

**Bit 2: Phase Build-Out Enable (PBOEN).** When this bit is set to 1 a phase build-out event occurs every time the T0 DPLL changes to a new reference, including exiting the holdover and free-run states. When this bit is set to 0, the T0 DPLL locks to the new source with zero degrees of phase difference. See Section 7.7.7.

When the device is in slave mode (MASTSLV pin = 0) values written to this field are latched, but the value read is always 0 to indicate that the device is forced to have phase build-out disabled. See Section 7.9.1.
0 = Disabled
1 = Enabled

**Bit 1: Soft Frequency Alarm Enable (SOFTEN).** This bit enables input clock frequency monitoring with the soft alarm limits set in the ILIMIT and SRLIMIT registers. Soft alarms are reported in the SOFT status bits of the ISR registers. See Section 7.5.1.
0 = Disabled
1 = Enabled

**Bit 0: Hard Frequency Limit Enable (HARDEN).** This bit enables input clock frequency monitoring with the hard alarm limits set in the ILIMIT and SRLIMIT registers. Hard alarms are reported in the HARD status bits of the ISR registers. See Section 7.5.1.
0 = Disabled
1 = Enabled

**Register Name:** ILIMIT
**Register Description:** Input Clock Frequency Limit Register
**Register Address:** 49h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | SOFT[3:0] | | | | HARD[3:0] | | | |
| **Default** | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

**Bits 7 to 4: Soft Frequency Alarm Limit (SOFT[3:0]).** This field is an unsigned integer that specifies the soft frequency alarm limit for all input clocks except the T0 DPLL's selected reference. The soft limit for the selected reference is specified by SRLIMIT:SOFT[3:0]. The soft alarm limit is only used for monitoring; soft alarms do not invalidate input clocks. The limit in ppm is ±(SOFT[3:0] + 1) x 3.81. The default limit is ±11.43ppm. Soft alarms are reported in the SOFT status bits of the ISR registers. See Section 7.5.1.

**Bits 3 to 0: Hard Frequency Alarm Limit (HARD[3:0]).** This field is an unsigned integer that specifies the hard frequency alarm limit for all input clocks except the T0 DPLL's selected reference. The hard limit for the selected reference is specified by SRLIMIT:HARD[3:0]. Hard alarms invalidate input clocks. The limit in ppm is ±(HARD[3:0] + 1) x 3.81. The default limit is ±15.24ppm. Hard alarms are reported in the HARD status bits of the ISR registers. See Section 7.5.1.

**Register Name:** SRLIMIT
**Register Description:** Selected Reference Frequency Limit Register
**Register Address:** 4Ah

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | SOFT[3:0] | | | | HARD[3:0] | | | |
| **Default** | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

**Bits 7 to 4: Soft Frequency Alarm Limit (SOFT[3:0]).** This field is an unsigned integer that specifies the soft frequency alarm limit for the T0 DPLL's selected reference. The soft limit for all other input clocks is specified by ILIMIT:SOFT[3:0]. The soft alarm limit is only used for monitoring; soft alarms do not invalidate input clocks. The limit in ppm is ±(SOFT[3:0] + 1) x 3.81. The default limit is ±11.43ppm. Soft alarms are reported in the SOFT status bits of the ISR registers. See Section 7.5.1.

**Bits 3 to 0: Hard Frequency Alarm Limit (HARD[3:0]).** This field is an unsigned integer that specifies the hard frequency alarm limit for the T0 DPLL's selected reference. The hard limit for all other input clocks is specified by ILIMIT:HARD[3:0]. Hard alarms invalidate input clocks. The limit in ppm is ±(HARD[3:0] + 1) x 3.81. The default limit is ±15.24ppm. Hard alarms are reported in the HARD status bits of the ISR registers. See Section 7.5.1.

**Register Name:** MCR11
**Register Description:** Master Configuration Register 11
**Register Address:** 4Bh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | — | T4T0 | FMEASIN[3:0] | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 4: T4 or T0 Path Select (T4T0).** This bit specifies which path is being accessed when reads or writes are made to the following registers: PTAB1, PTAB2, FREQ1, FREQ2, FREQ3, IPR1 to IPR7, PHASE1, and PHASE2.

0 = T0 path
1 = T4 path

**Bits 3 to 0: Frequency Measurement Input Select (FMEASIN[3:0]).** This field specifies the input clock for the frequency measurement reported in the FMEAS register. See Section 7.5.1.

0000 = {unused value}
0001 = IC1
0010 = IC2
0011 = IC3
0100 = IC4
0101 = IC5
0110 = IC6
0111 = IC7
1000 = IC8
1001 = IC9
1010 = IC10
1011 = IC11
1100 = IC12
1101 = IC13
1110 = IC14
1111 = {unused value}

**Register Name:** FMEAS
**Register Description:** Frequency Measurement Register
**Register Address:** 4Ch

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | FMEAS[7:0] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Measured Frequency (FMEAS[7:0]).** This read-only field indicates the measured frequency of the input clock specified in the FMEASIN field of the MCR11 register. FMEAS is a two's-complement signed integer that expresses the frequency as an offset with respect to the frequency monitor clock (either the internal master clock or the output of the T0 DPLL, depending on the setting of the FMONCLK bit in the MCR10 register). The measured frequency is FMEAS[7:0] x 3.81ppm. See Section 7.5.1.

**Register Name:** DLIMIT3
**Register Description:** DPLL Frequency Limit Register 3
**Register Address:** 4Dh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | FLLOL | SOFTLIM[6:0] | | | | | | |
| **Default** | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |

**Bit 7: Frequency Limit Loss of Lock (FLLOL).** When this bit is set to 1, the T0 and T4 DPLLs internally declare loss-of-lock when their hard limits are reached. The T0 DPLL hard frequency limit is set in the HARDLIM[9:0] field in the DLIMIT1 and DLIMIT2 registers. The T4 DPLL hard frequency limit is fixed at ±80ppm.See Section 7.7.6.

0 = DPLL declares loss-of-lock normally
1 = DPLL also declares loss-of-lock when the hard frequency limit is reached

**Bits 6 to 0: DPLL Soft Frequency Limit (SOFTLIM6:0]).** This field is an unsigned integer that specifies the soft frequency limit for the T0 and T4 DPLLs. The soft limit is only used for monitoring; exceeding this limit does not cause loss-of-lock. The limit in ppm is ±SOFTLIM[6:0] x 0.628. The default value is ±8.79ppm. When the T0 DPLL frequency exceeds the soft limit the T0SOFT status bit is set in the OPSTATE register. When the T4 DPLL frequency exceeds the soft limit the T4SOFT status bit is set in OPSTATE. See Section 7.7.6.

**Register Name:** IER4
**Register Description:** Interrupt Enable Register 4
**Register Address:** 4Eh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | FHORDY | SHORDY | — | — | IC2NO4 | IC1NO4 | IC2NO8 | IC1NO8 |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Interrupt Enable for Fast Holdover Frequency Ready (FHORDY).** This bit is an interrupt enable for the FHORDY bit in the MSR4 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Bit 6: Interrupt Enable for Slow Holdover Frequency Ready (SHORDY).** This bit is an interrupt enable for the SHORDY bit in the MSR4 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Bit 3: Interrupt Enable for Input Clock 2 Has No 400Hz Component (IC2NO4).** This bit is an interrupt enable for the IC2NO4 bit in the MSR4 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Bit 2: Interrupt Enable for Input Clock 1 Has No 400Hz Component (IC1NO4).** This bit is an interrupt enable for the IC1NO4 bit in the MSR4 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Bit 1: Interrupt Enable for Input Clock 2 Has No 8kHz Component (IC2NO8).** This bit is an interrupt enable for the IC2NO8 bit in the MSR4 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Bit 0: Interrupt Enable for Input Clock 1 Has No 8kHz Component (IC1NO8).** This bit is an interrupt enable for the IC1NO8 bit in the MSR4 register.
0 = Mask the interrupt
1 = Enable the interrupt

**Register Name:** LB0U
**Register Description:** Leaky Bucket 0 Upper Threshold Register
**Register Address:** 50h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | LB0U[7:0] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**Bits 7 to 0: Leaky Bucket 0 Upper Threshold (LB0U[7:0]).** When the leaky bucket accumulator is equal to the value stored in this field, the activity monitor declares an activity alarm by setting the input clock's ACT bit in the appropriate ISR register. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

**Register Name:** LB0L
**Register Description:** Leaky Bucket 0 Lower Threshold Register
**Register Address:** 51h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | LB0L[7:0] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

**Bits 7 to 0: Leaky Bucket 0 Lower Threshold (LB0L[7:0]).** When the leaky bucket accumulator is equal to the value stored in this field, the activity monitoring logic clears the activity alarm (if previously declared) by clearing the input clock's ACT bit in the appropriate ISR register. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

**Register Name:** LB0S
**Register Description:** Leaky Bucket 0 Size Register
**Register Address:** 52h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | LB0S[7:0] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Bits 7 to 0: Leaky Bucket 0 Size (LB0S[7:0]).** This field specifies the maximum value of the leaky bucket. The accumulator cannot increment past this value. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

**Register Name:** LB0D
**Register Description:** Leaky Bucket 0 Decay Rate Register
**Register Address:** 53h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | — | — | — | — | LB0D[1:0] | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Bits 1 to 0: Leaky Bucket 0 Decay Rate (LB0D[1:0]).** This field specifies the decay or “leak” rate of the leaky bucket accumulator. For each period of 1, 2, 4, or 8 128ms intervals in which no irregularities are detected on the input clock, the accumulator decrements by 1. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

00 = decrement every 128ms (8 units/second)
01 = decrement every 256ms (4 units/second)
10 = decrement every 512ms (2 units/second)
11 = decrement every 1024ms (1 unit/second)

**Register Name:** LB1U, LB2U, LB3U
**Register Description:** Leaky Bucket 1/2/3 Upper Threshold Register
**Register Address:** 54h, 58h, 5Ch

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | LBxU[7:0] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**Bits 7 to 0: Leaky Bucket ‘x’ Upper Threshold (LBxU[7:0]).** See the LB0U register description.
Registers LB1U, LB1L, LB1S, and LB1D together specify leaky bucket configuration 1.
Registers LB2U, LB2L, LB2S, and LB2D together specify leaky bucket configuration 2.
Registers LB3U, LB3L, LB3S, and LB3D together specify leaky bucket configuration 3.

**Register Name:** LB1L, LB2L, LB3L
**Register Description:** Leaky Bucket 1/2/3 Lower Threshold Register
**Register Address:** 55h, 59h, 5Dh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | LBxL[7:0] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

**Bits 7 to 0: Leaky Bucket ‘x’ Lower Threshold (LBxL[7:0]).** See the LB0L register description.
Registers LB1U, LB1L, LB1S, and LB1D together specify leaky bucket configuration 1.
Registers LB2U, LB2L, LB2S, and LB2D together specify leaky bucket configuration 2.
Registers LB3U, LB3L, LB3S, and LB3D together specify leaky bucket configuration 3.

**Register Name:** LB1S, LB2S, LB3S
**Register Description:** Leaky Bucket 1/2/3 Size Register
**Register Address:** 56h, 5Ah, 5Eh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | LBxS[7:0] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Bits 7 to 0: Leaky Bucket ‘x’ Size (LBxS[7:0]).** See the LB0S register description.
Registers LB1U, LB1L, LB1S, and LB1D together specify leaky bucket configuration 1.
Registers LB2U, LB2L, LB2S, and LB2D together specify leaky bucket configuration 2.
Registers LB3U, LB3L, LB3S, and LB3D together specify leaky bucket configuration 3.

**Register Name:** LB1D, LB2D, LB3D
**Register Description:** Leaky Bucket 1/2/3 Decay Rate Register
**Register Address:** 57h, 5Bh, 5Fh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | — | — | — | — | LBxD[1:0] | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Bits 1 to 0: Leaky Bucket ‘x’ Decay Rate (LBxD[1:0]).** See the LB0D register description.
Registers LB1U, LB1L, LB1S, and LB1D together configure leaky bucket algorithm 1.
Registers LB2U, LB2L, LB2S, and LB2D together configure leaky bucket algorithm 2.
Registers LB3U, LB3L, LB3S, and LB3D together configure leaky bucket algorithm 3.

**Register Name:** OCR1
**Register Description:** Output Configuration Register 1
**Register Address:** 60h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | OFREQ2[3:0] | | | | OFREQ1[3:0] | | | |
| **Default** | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**Bits 7 to 4: Output Frequency of OC2 (OFREQ2[3:0]).** This field specifies the frequency of output clock OC2. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. Note that if the T4 DPLL is configured for 62.5MHz (T4CR1:T4FREQ = 1001) and the T4 APLL is configured to lock to the T4 DPLL (T0CR1:T4APT0 = 0), then OFREQ2 = 1100 specifies T4 APLL frequency divided by 10 to give an output frequency of 25MHz.

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-8)
0100 = Digital1 (see Table 7-8)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48 (or by 10, see note above)
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

**Bits 3 to 0: Output Frequency of OC1 (OFREQ1[3:0]).** This field specifies the frequency of output clock OC1. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. Note that if the T4 DPLL is configured for 62.5MHz (T4CR1:T4FREQ = 1001) and the T4 APLL is configured to lock to the T4 DPLL (T0CR1:T4APT0 = 0), then OFREQ1 = 1100 specifies T4 APLL frequency divided by 10 to give an output frequency of 25MHz.

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-8)
0100 = Digital1 (see Table 7-8)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48 (or by 10, see note above)
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

**Register Name:** OCR2
**Register Description:** Output Configuration Register 2
**Register Address:** 61h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | OFREQ4[3:0] | | | | OFREQ3[3:0] | | | |
| **Default** | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**Bits 7 to 4: Output Frequency of OC4 (OFREQ4[3:0]).** This field specifies the frequency of output clock OC4. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. Note that if the T4 DPLL is configured for 62.5MHz (T4CR1:T4FREQ = 1001) and the T4 APLL is configured to lock to the T4 DPLL (T0CR1:T4APT0 = 0), then OFREQ4 = 1100 specifies T4 APLL frequency divided by 10 to give an output frequency of 25MHz.

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-8)
0100 = Digital1 (see Table 7-8)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 2
1100 = T4 APLL frequency divided by 48 (or by 10, see note above)
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

**Bits 3 to 0: Output Frequency of OC3 (OFREQ3[3:0]).** This field specifies the frequency of output clock OC3. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. Note that if the T4 DPLL is configured for 62.5MHz (T4CR1:T4FREQ = 1001) and the T4 APLL is configured to lock to the T4 DPLL (T0CR1:T4APT0 = 0), then OFREQ3 = 1100 specifies T4 APLL frequency divided by 10 to give an output frequency of 25MHz.

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-8)
0100 = Digital1 (see Table 7-8)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48 (or by 10, see note above)
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

**Register Name:** OCR3
**Register Description:** Output Configuration Register 3
**Register Address:** 62h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | OFREQ6[3:0] | | | | OFREQ5[3:0] | | | |
| **Default** | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

**Bits 7 to 4: Output Frequency of OC6 (OFREQ6[3:0]).** This field specifies the frequency of output clock output OC6. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. Note that if the T4 DPLL is configured for 62.5MHz (T4CR1:T4FREQ = 1001) and the T4 APLL is configured to lock to the T4 DPLL (T0CR1:T4APT0 = 0), then OFREQ6 = 1100 specifies T4 APLL frequency divided by 10 to give an output frequency of 25MHz.

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = T0 APLL frequency divided by 2
0100 = Digital1 (see Table 7-8)
0101 = T0 APLL frequency
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48 (or by 10, see note above)
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

**Bits 3 to 0: Output Frequency of OC5 (OFREQ5[3:0]).** This field specifies the frequency of output clock OC5. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. Note that if the T4 DPLL is configured for 62.5MHz (T4CR1:T4FREQ = 1001) and the T4 APLL is configured to lock to the T4 DPLL (T0CR1:T4APT0 = 0), then OFREQ5 = 1100 specifies T4 APLL frequency divided by 10 to give an output frequency of 25MHz.

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-8)
0100 = Digital1 (see Table 7-8)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 2
1100 = T4 APLL frequency divided by 48 (or by 10, see note above)
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

**Register Name:** OCR4
**Register Description:** Output Configuration Register 4
**Register Address:** 63h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | OC11EN | OC10EN | OC9EN | OC8EN | OFREQ7[3:0] | | | |
| **Default** | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

**Bit 7: OC11 Enable (OC11EN).** This configuration bit enables the 2kHz output on OC11. See Section 7.8.2.5.
0 = Disabled (low)
1 = Enabled

**Bit 6: OC10 Enable (OC10EN).** This configuration bit enables the 8kHz output on OC10. See Section 7.8.2.5.
0 = Disabled (low)
1 = Enabled

**Bit 5: OC9 Enable (OC9EN).** This configuration bit enables the 1.544/2.048MHz output on OC9. See Section 7.8.2.4.
0 = Disabled (low)
1 = Enabled

**Bit 4: OC8 Enable (OC8EN).** This configuration bit enables OC8 to transmit a 64kHz composite clock signal. See Sections 7.8.2.4 and 7.10.2.
0 = Disabled (high impedance)
1 = Enabled

**Bits 3 to 0: Output Frequency of OC7 (OFREQ7[3:0]).** This field specifies the frequency of output clock output OC7. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. Note that if the T4 DPLL is configured for 62.5MHz (T4CR1:T4FREQ = 1001) and the T4 APLL is configured to lock to the T4 DPLL (T0CR1:T4APT0 = 0), then OFREQ7 = 1100 specifies T4 APLL frequency divided by 10 to give an output frequency of 25MHz.
0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-8)
0100 = T0 APLL frequency divided by 2
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48 (or by 10, see note above)
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

**Register Name:** T4CR1
**Register Description:** T4 DPLL Configuration Register 1
**Register Address:** 64h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | ASQUEL | OC8DUTY | OC9SON | T4FREQ[3:0] | | | |
| **Default** | 0 | 0 | 0 | see below | 0 | 0 | 0 | 1 |

**Bit 6: Auto-Squelch (ASQUEL).** When outputs OC8 and OC9 are sourced from the T4 DPLL (MCR4:OC89 = 0), this configuration bit enables automatic squelching of OC8 and OC9 whenever T4 has no valid input references. When an output is squelched it is forced low. See Section 7.8.2.4.

0 = Disable automatic squelching
1 = Enable automatic squelching of OC8 and OC9 when T4 has no valid input references

**Bit 5: OC8 Duty Cycle (OC8DUTY).** See Section 7.10.2.

0 = 50% duty cycle
1 = 5/8 duty cycle

**Bit 4: OC9 SONET/SDH (OC9SON).** When MCR4:OC89 = 0, this bit controls the frequency of clock output OC9. When OC89 = 1, this bit ignored and the frequency of OC9 is controlled by the SONSDH bit in MCR3. During reset the default value of this bit is latched from the SONSDH pin. See Section 7.8.2.4.

0 = 2048kHz (SDH)
1 = 1544kHz (SONET)

**Bits 3 to 0: T4 DPLL Frequency (T4FREQ[3:0]).** This field configures the T4 DPLL frequency. The T4 DPLL frequency can affect the frequency of the T4 APLL, which in turn affects the available output frequencies on clock outputs OC1 to OC7 (see registers OCR1 to OCR4). Optionally the T4 DPLL can be disabled and the T4 APLL can be locked to the T0 DPLL (see the T4APT0 bit in the T0CR1 register). See Section 7.8.2.

| | T4 DPLL FREQUENCY | T4 APLL FREQUENCY |
|---|---|---|
| 0000 = | Disabled | Depends on state of T4APT0 in T0CR1 register |
| 0001 = | 77.76MHz | 311.04MHz (4 x T4 DPLL) |
| 0010 = | 24.576MHz (12 x E1) | 98.304MHz (4 x T4 DPLL) |
| 0011 = | 32.768MHz (16 x E1) | 131.072MHz (4 x T4 DPLL) |
| 0100 = | 37.056MHz (24 x DS1) | 148.224MHz (4 x T4 DPLL) |
| 0101 = | 24.704MHz (16 x DS1) | 98.816MHz (4 x T4 DPLL) |
| 0110 = | 68.736MHz (2 x E3) | 274.944MHz (4 x T4 DPLL) |
| 0111 = | 44.736MHz (DS3) | 178.944MHz (4 x T4 DPLL) |
| 1000 = | 25.248MHz (4 x 6312 kHz) | 100.992MHz (4 x T4 DPLL) |
| 1001 = | 62.500MHz (GbE ÷ 16) | 250.000MHz (4 x T4 DPLL) |
| 1010–1111 = | {unused values} | {unused values} |

**Register Name:** T0CR1
**Register Description:** T0 DPLL Configuration Register 1
**Register Address:** 65h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | T4MT0 | T4APT0 | T0FT4[2:0] | | | T0FREQ[2:0] | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Bit 7: T4 Measure T0 Phase (T4MT0).** When this bit is set to 1 the T4 path is disabled, and the T4 phase detector is configured to measure the phase difference between the selected T0 DPLL input clock and the selected T4 DPLL input clock. See Section 7.7.10.

0 = Normal operation for the T4 path
1 = Enable T4-measure-T0-phase mode

**Bit 6: T4 APLL Source from T0 (T4APT0).** When this bit is set to 1 the T4 output APLL locks to the T0 LF output DFS rather than the T4 forward DFS. The T0FT4[1:0] field (below) specifies the T0 DPLL frequency. See Section 7.8.2.

0 = T4 APLL locks to T4 DPLL
1 = T4 APLL locks to T0 DPLL

**Bits 5 to 3: T0 Frequency to T4 APLL (T0FT4[2:0]).** This field specifies the frequency provided from the T0 LF output DFS to the T4 output APLL when the T4APT0 bit is set to 1. This frequency can be different than the frequency specified by T0CR1:T0FREQ. Values not listed below are unused. See Section 7.8.2.

| | T0 DPLL FREQUENCY | T4 APLL FREQUENCY |
|---|---|---|
| 000 = | 24.576MHz (12 x E1) | 98.304MHz (4 x T0 DPLL) |
| 010 = | 32.768MHz (16 x E1) | 131.072MHz (4 x T0 DPLL) |
| 100 = | 37.056MHz (24 x DS1) | 148.224MHz (4 x T0 DPLL) |
| 110 = | 24.704MHz (16 x DS1) | 98.816MHz (4 x T0 DPLL) |
| 111 = | 25.248MHz (4 x 6312 kHz) | 100.992MHz (4 x T0 DPLL) |

**Bits 2 to 0: T0 DPLL Frequency (T0FREQ[2:0]).** This field configures the T0 DPLL output frequency that is passed to the T0 Output APLL. The T0 DPLL output frequency affects the frequency of the T0 Output APLL, which in turn affects the available output frequencies on clock outputs OC1 to OC7 (see registers OCR1 to OCR4). See Section 7.8.2.

| | T0 DPLL FREQUENCY | T0 APLL FREQUENCY |
|---|---|---|
| 000 = | 77.76MHz, digital feedback | 311.04MHz (4 x T0 DPLL) |
| 001 = | 77.76MHz, analog feedback | 311.04MHz (4 x T0 DPLL) |
| 010 = | 24.576MHz (12 x E1) | 98.304MHz (4 x T0 DPLL) |
| 011 = | 32.768MHz (16 x E1) | 131.072MHz (4 x T0 DPLL) |
| 100 = | 37.056MHz (24 x DS1) | 148.224MHz (4 x T0 DPLL) |
| 101 = | 24.704MHz (16 x DS1) | 98.816MHz (4 x T0 DPLL) |
| 110 = | 25.248MHz (4 x 6312 kHz) | 100.992MHz (4 x T0 DPLL) |
| 111 = | {unused value} | {unused value} |

**Register Name:** T4BW
**Register Description:** T4 Bandwidth Register
**Register Address:** 66h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | — | — | — | — | T4BW[1:0] | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 1 to 0: T4 DPLL Bandwidth (T4BW[1:0]).** See Section 7.7.3.
00 = 18Hz
01 = 35Hz
10 = 70Hz
11 = {unused value}

**Register Name:** T0LBW
**Register Description:** T0 Locked Bandwidth Register
**Register Address:** 67h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | — | T0LBW[4:0] | | | | |
| **Default** | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |

**Bits 4 to 0: T0 DPLL Locked Bandwidth (T0LBW[4:0]).** This field configures the bandwidth of the T0 DPLL when locked to an input clock. When AUTOBW = 0 in the MCR9 register, the T0LBW bandwidth is used for acquisition and for locked operation. When AUTOBW = 1, T0ABW bandwidth is used for acquisition while T0LBW bandwidth is used for locked operation. See Section 7.7.3.
00000 = 0.5mHz
00001 = 1mHz
00010 = 2mHz
00011 = 4mHz
00100 = 8mHz
00101 = 15mHz
00110 = 30mHz
00111 = 60mHz
01000 = 0.1Hz
01001 = 0.3Hz
01010 = 0.6Hz
01011 = 1.2Hz
01100 = 2.5Hz
01101 = 4Hz
01110 = 8Hz
01111 = 18Hz
10000 = 35Hz
10001 = 70Hz
10010 to 11111 = {unused values}

**Register Name:** T0ABW
**Register Description:** T0 Acquisition Bandwidth Register
**Register Address:** 69h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | — | T0ABW[4:0] | | | | |
| **Default** | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**Bits 4 to 0: T0 DPLL Acquisition Bandwidth (T0ABW[4:0]).** This field configures the bandwidth of the T0 DPLL when acquiring lock. When AUTOBW = 0 in the MCR9 register, the T0LBW bandwidth is used for is used for acquisition and for locked operation. When AUTOBW = 1, T0ABW bandwidth is used for acquisition while T0LBW bandwidth is used for locked operation. See Section 7.7.3.

00000 = 0.5mHz
00001 = 1mHz
00010 = 2mHz
00011 = 4mHz
00100 = 8mHz
00101 = 15mHz
00110 = 30mHz
00111 = 60mHz
01000 = 0.1Hz
01001 = 0.3Hz
01010 = 0.6Hz
01011 = 1.2Hz
01100 = 2.5Hz
01101 = 4Hz
01110 = 8Hz
01111 = 18Hz
10000 = 35Hz
10001 = 70Hz
10010 to 11111 = {unused values}

**Register Name:** T4CR2
**Register Description:** T4 Configuration Register 2
**Register Address:** 6Ah

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | PD2GA8K[2:0] | | | — | DAMP[2:0] | | |
| **Default** | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

**Bits 6 to 4: Phase Detector 2 Gain, Analog Feedback, 8kHz (PD2GA8K[2:0]).** This field specifies the gain of the T4 phase detector 2 in analog feedback mode with an input clock of 8 kHz or less. This value is only used if automatic gain selection is enabled by setting PD2EN = 1 in the T4CR3 register. Analog vs. digital feedback mode is specified in MCR4:T4DFB. See Section 7.7.5.

**Bits 2 to 0: Damping Factor (DAMP[2:0]).** This field configures the damping factor of the T4 DPLL. Damping factor is a function of both DAMP[2:0] and the T4 DPLL bandwidth (T4BW register). The default value corresponds to a damping factor of 5. See Section 7.7.4.

| | 18Hz | 35Hz | 70Hz |
|---|---|---|---|
| 001 = | 1.2 | 1.2 | 1.2 |
| 010 = | 2.5 | 2.5 | 2.5 |
| 011 = | 5 | 5 | 5 |
| 100 = | 5 | 10 | 10 |
| 101 = | 5 | 10 | 20 |

000, 110, and 111 = {unused values}

The gain peak for each damping factor is shown below:

| DAMPING FACTOR | GAIN PEAK (dB) |
|---|---|
| 1.2 | 0.4 |
| 2.5 | 0.2 |
| 5 | 0.1 |
| 10 | 0.06 |
| 20 | 0.03 |

**Register Name:** T0CR2
**Register Description:** T0 Configuration Register 2
**Register Address:** 6Bh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | PD2GA8K[2:0] | | | — | DAMP[2:0] | | |
| **Default** | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

**Bits 6 to 4: Phase Detector 2 Gain, Analog Feedback, 8kHz (PD2GA8K[2:0]).** This field specifies the gain of the T0 phase detector 2 in analog feedback mode with an input clock of 8kHz or less. This value is only used if automatic gain selection is enabled by setting PD2EN = 1 in the T0CR3 register. Analog vs. digital feedback mode is specified in T0CR1:T0FREQ[2:0]. See Section 7.7.5.

**Bits 2 to 0: Damping Factor (DAMP[2:0]).** This field configures the damping factor of the T0 DPLL. Damping factor is a function of both DAMP[2:0] and the T0 DPLL bandwidth (T0ABW and T0LBW). The default value corresponds to a damping factor of 5. See Section 7.7.4.

| | ≤ 4Hz | 8Hz | 18Hz | 35Hz | 70Hz |
|---|---|---|---|---|---|
| 001 = | 5 | 2.5 | 1.2 | 1.2 | 1.2 |
| 010 = | 5 | 5 | 2.5 | 2.5 | 2.5 |
| 011 = | 5 | 5 | 5 | 5 | 5 |
| 100 = | 5 | 5 | 5 | 10 | 10 |
| 101 = | 5 | 5 | 5 | 10 | 20 |

000, 110, and 111 = {unused values}

The gain peak for each damping factor is shown below:

| DAMPING FACTOR | GAIN PEAK (dB) |
|---|---|
| 1.2 | 0.4 |
| 2.5 | 0.2 |
| 5 | 0.1 |
| 10 | 0.06 |
| 20 | 0.03 |

**Register Name:** T4CR3
**Register Description:** T4 Configuration Register 3
**Register Address:** 6Ch

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | PD2EN | PD2GA[2:0] | | | — | PD2GD[2:0] | | |
| **Default** | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

**Bit 7: Phase Detector 2 Gain Enable (PD2EN).** When this bit is set to 1, the T4 phase detector 2 is enabled and the gain is determined by the feedback mode. In digital feedback mode, the gain is set by the PD2GD field. In analog feedback mode the gain is set by the PD2GA field if the input clock frequency is greater than 8kHz or by the PD2GA8K field in the T4CR2 register is the input clock frequency is less than or equal to 8kHz. Analog vs. digital feedback mode is specified in MCR4:T4DFB. See Section 7.7.5.

0 = Disable
1 = Enable

**Bits 6 to 4: Phase Detector 2 Gain, Analog Feedback (PD2GA[2:0]).** This field specifies the gain of the T4 phase detector 2 in analog feedback mode with an input clock frequency greater than 8kHz. This value is only used if automatic gain selection is enabled by setting PD2EN = 1. Analog vs. digital feedback mode is specified in MCR4:T4DFB. See Section 7.7.5.

**Bits 2 to 0: Phase Detector 2 Gain, Digital Feedback (PD2GD[2:0]).** This field specifies the gain of the T4 phase detector 2 in digital feedback mode. This value is only used if automatic gain selection is enabled by setting PD2EN = 1. Analog vs. digital feedback mode is specified in MCR4:T4DFB. See Section 7.7.5.

**Register Name:** T0CR3
**Register Description:** T0 Configuration Register 3
**Register Address:** 6Dh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | PD2EN | PD2GA[2:0] | | | — | PD2GD[2:0] | | |
| **Default** | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

**Bit 7: Phase Detector 2 Gain Enable (PD2EN).** When this bit is set to 1, the T0 phase detector 2 is enabled and the gain is determined by the feedback mode. In digital feedback mode, the gain is set by the PD2GD field. In analog feedback mode the gain is set by the PD2GA field if the input clock is greater than 8kHz or by the PD2GA8K field in the T0CR2 register if the input clock frequency is less than or equal to 8kHz. Analog vs. digital feedback mode is specified in T0CR1:T0FREQ[2:0]. See Section 7.7.5.

0 = Disable
1 = Enable

**Bits 6 to 4: Phase Detector 2 Gain, Analog Feedback (PD2GA[2:0]).** This field specifies the gain of the T0 phase detector 2 in analog feedback mode with an input clock frequency greater than 8kHz. This value is only used if automatic gain selection is enabled by setting PD2EN = 1. Analog vs. digital feedback mode is specified in T0CR1:T0FREQ[2:0]. See Section 7.7.5.

**Bits 2 to 0: Phase Detector 2 Gain, Digital Feedback (PD2GD[2:0]).** This field specifies the gain of the T0 phase detector 2 in digital feedback mode. This value is only used if automatic gain selection is enabled by setting PD2EN = 1. Analog vs. digital feedback mode is specified in T0CR1:T0FREQ[2:0]. See Section 7.7.5.

**Register Name:** GPCR
**Register Description:** GPIO Configuration Register
**Register Address:** 6Eh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | GPIO4D | GPIO3D | GPIO2D | GPIO1D | GPIO4O | GPIO3O | GPIO2O | GPIO1O |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: GPIO4 Direction (GPIO4D).** This bit configures the data direction for the GPIO4 pin. When GPIO4 is an input its current state can be read from GPSR:GPIO4. When GPIO4 is an output, its value is controlled by the GPIO4O configuration bit.
0 = Input
1 = Output

**Bit 6: GPIO3 Direction (GPIO3D).** This bit configures the data direction for the GPIO3 pin. When GPIO3 is an input its current state can be read from GPSR:GPIO3. When GPIO3 is an output, its value is controlled by the GPIO3O configuration bit.
0 = Input
1 = Output

**Bit 5: GPIO2 Direction (GPIO2D).** This bit configures the data direction for the GPIO2 pin. When GPIO2 is an input its current state can be read from GPSR:GPIO2. When GPIO2 is an output, its value is controlled by the GPIO2O configuration bit.
0 = Input
1 = Output

**Bit 4: GPIO1 Direction (GPIO1D).** This bit configures the data direction for the GPIO1 pin. When GPIO1 is an input its current state can be read from GPSR:GPIO1. When GPI13 is an output, its value is controlled by the GPIO1O configuration bit.
0 = Input
1 = Output

**Bit 3: GPIO4 Output Value (GPIO4O).** When GPIO4 is configured as an output (GPIO4D = 1) this bit specifies the output value.
0 = Low
1 = High

**Bit 2: GPIO3 Output Value (GPIO3O).** When GPIO3 is configured as an output (GPIO3D = 1) this bit specifies the output value.
0 = Low
1 = High

**Bit 1: GPIO2 Output Value (GPIO2O).** When GPIO2 is configured as an output (GPIO2D = 1) this bit specifies the output value.
0 = Low
1 = High

**Bit 0: GPIO1 Output Value (GPIO1O).** When GPIO1 is configured as an output (GPIO1D = 1) this bit specifies the output value.
0 = Low
1 = High

**Register Name:** GPSR
**Register Description:** GPIO Status Register
**Register Address:** 6Fh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | — | — | GPIO4 | GPIO3 | GPIO2 | GPIO1 |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 3: GPIO4 State (GPIO4).** This bit indicates the current state of the GPIO4 pin.
0 = Low
1 = High

**Bit 2: GPIO3 State (GPIO3).** This bit indicates the current state of the GPIO3 pin.
0 = Low
1 = High

**Bit 2: GPIO2 State (GPIO2).** This bit indicates the current state of the GPIO2 pin.
0 = Low
1 = High

**Bit 1: GPIO1 State (GPIO1).** This bit indicates the current state of the GPIO1 pin.
0 = Low
1 = High

**Register Name:** OFFSET1
**Register Description:** Phase Offset Register 1
**Register Address:** 70h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | OFFSET[7:0] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The OFFSET1 and OFFSET2 registers must be read consecutively and written consecutively. See Section 8.3.

**Bits 7 to 0: Phase Offset (OFFSET[7:0]).** The full 16-bit OFFSET[15:0] field spans this register and the OFFSET2 register. OFFSET is a two's-complement signed integer that specifies the desired phase offset between the output clocks and the selected reference. The phase offset in picoseconds is equal to OFFSET[15:0] x actual_internal_clock_period / $2^{11}$. If the internal clock is at its nominal frequency of 77.76MHz, the phase offset equation simplifies to OFFSET[15:0] x 6.279ps. If, however, the DPLL is locked to a reference whose frequency is +1ppm from ideal, for example, then the actual internal clock period is 1 ppm shorter and the phase offset is 1ppm smaller. When the OFFSET field is written, the phase of the output clocks is automatically ramped to the new offset value to avoid loss of synchronization. To adjust the phase offset without changing the phase of the output clocks, use the recalibration process enabled by FSCR3:RECAL. The OFFSET field is ignored when phase build-out is enabled (PBOEN = 1 in the MCR10 register or PMPBEN = 1 in the PHMON register) and when the DPLL is not locked. See Section 7.7.8.

**Register Name:** OFFSET2
**Register Description:** Phase Offset Register 2
**Register Address:** 71h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | OFFSET[15:8] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Phase Offset (OFFSET[15:8]).** See the OFFSET1 register description.

**Register Name:** PBOFF
**Register Description:** Phase Build-Out Offset Register
**Register Address:** 72h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | PBOFF[5:0] | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 5 to 0: Phase Build-Out Offset Register (PBOFF[5:0]).** An uncertainty of up to 5ns is introduced each time a phase build-out event occurs. This uncertainty results in a phase hit on the output. Over a large number of phase build-out events the mean error should be zero. The PBOFF field specifies a fixed offset for each phase build-out event to skew the average error toward zero. This field is a two's complement signed integer. The offset in nanoseconds is PBOFF[5:0] x 0.101. Values greater than 1.4ns or less than -1.4ns may cause internal math errors and should not be used. See Section 7.7.7.5.

**Register Name:** PHLIM1
**Register Description:** Phase Limit Register 1
**Register Address:** 73h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | FLEN | NALOL | 1 | — | — | FINELIM[2:0] | | |
| **Default** | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

**Bit 7: Fine Phase Limit Enable (FLEN).** This configuration bit enables the fine phase limit specified in the FINELIM[2:0] field. The fine limit must be disabled for multi-UI jitter tolerance (see PHLIM2 fields). This field controls both T0 and T4. See Section 7.7.6.

0 = Disabled
1 = Enabled

**Bit 6: No-Activity Loss of Lock (NALOL).** The T0 and T4 DPLLs can detect that an input clock has no activity very quickly (within two clock cycles). When NALOL = 0, loss-of-lock is not declared when clock cycles are missing, and nearest edge locking (±180°) is used when the clock recovers. This gives tolerance to missing cycles. When NALOL = 1, loss-of-lock is indicated as soon as no activity is detected, and the device switches to phase/frequency locking (±360°). This field controls both T0 and T4. See Sections 7.5.3 and 7.7.6.

0 = No activity does not trigger loss-of-lock
1 = No activity does trigger loss-of-lock

**Bit 5:** Leave set to 1 (test control).

**Bits 2 to 0: Fine Phase Limit (FINELIM[2:0]).** This field specifies the fine phase limit window, outside of which loss-of-lock is declared. The FLEN bit enables this feature. The phase of the input clock has to be inside the fine limit window for two seconds before phase lock is declared. Loss-of-lock is declared immediately if the phase of the input clock is outside the phase limit window. The default value of 010 is appropriate for most situations. This field controls both T0 and T4. See Section 7.7.6.

000 = Always indicates loss of phase lock—do not use
001 = Small phase limit window, ±45 to ±90°
010 = Normal phase limit window, ±90 to ±180° (default)
100, 101, 110, 111 = Proportionately larger phase limit window

**Register Name:** PHLIM2
**Register Description:** Phase Limit Register 2
**Register Address:** 74h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | CLEN | MCPDEN | USEMCPD | — | COARSELIM[3:0] | | | |
| **Default** | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**Bit 7: Coarse Phase Limit Enable (CLEN).** This configuration bit enables the coarse phase limit specified in the COARSELIM[3:0] field. This field controls both T0 and T4. See Section 7.7.6.

0 = Disabled
1 = Enabled

**Bit 6: Multicycle Phase Detector Enable (MCPDEN).** This configuration bit enables the multicycle phase detector and allows the DPLL to tolerate large-amplitude jitter and wander. The range of this phase detector is the same as the coarse phase limit specified in the COARSELIM[3:0] field. This field controls both T0 and T4. See Section 7.7.5.

0 = Disabled
1 = Enabled

**Bit 5: Use Multicycle Phase Detector in the DPLL Algorithm (USEMCPD).** This configuration bit enables the DPLL algorithm to use the multicycle phase detector so that a large phase measurement drives faster DPLL pull-in. When USEMCPD = 0, phase measurement is limited to ±360°, giving slower pull-in at higher frequencies but with less overshoot. When USEMCPD = 1, phase measurement is set as specified in the COARSELIM[3:0] field, giving faster pull-in. MCPDEN should be set to 1 when USEMCPD = 1. This field controls both T0 and T4. See Section 7.7.5.

0 = Disabled
1 = Enabled

**Bits 3 to 0: Coarse Phase Limit (COARSELIM[3:0]).** This field specifies the coarse phase limit and the tracking range of the multicycle phase detector. The CLEN bit enables this feature. If jitter tolerance greater than 0.5UI is required and the input clock is a high-frequency signal, the DPLL can be configured to track phase errors over many UI using the multicycle phase detector. This field controls both T0 and T4. See Section 7.7.5 and 7.7.6.

0000 = ±1UI
0001 = ±3UI
0010 = ±7UI
0011 = ±15UI
0100 = ±31UI
0101 = ±63UI
0110 = ±127UI
0111 = ±255UI
1000 = ±511UI
1001 = ±1023UI
1010 = ±2047UI
1011 = ±4095UI
1100 to 1111 = ±8191UI

**Register Name:** PHMON
**Register Description:** Phase Monitor Register
**Register Address:** 76h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | NW | — | PMEN | PMPBEN | PMLIM[3:0] | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**Bit 7: Low-Frequency Input Clock Noise Window (NW).** For 2kHz, 4kHz, or 8kHz input clocks, this configuration bit enables a ±5% tolerance noise window centered around the expected clock edge location. Noise-induced edges outside this window are ignored, reducing the possibility of phase hits on the output clocks. NW should be enabled only when the device is locked to an input and TEST1:D180 = 0.

0 = All edges are recognized by the DPLL
1 = Only edges within the ±5% tolerance window are recognized by the DPLL

**Bit 5: Phase Monitor Enable (PMEN).** This configuration bit enables the phase monitor, which measures the phase error between the input clock reference and the DPLL output. When the DPLL is set for low bandwidth, a phase transient on the input causes an immediate phase error that is gradually reduced as the DPLL tracks the input. When the measured phase error exceeds the limit set in the PMLIM field, the phase monitor declares a phase monitor alarm by setting MSR3:PHMON. See Section 7.7.7.

0 = Disabled
1 = Enabled

**Bit 4: Phase Monitor to Phase Build-Out Enable (PMPBEN).** This bit enables phase build-out in response to phase hits on the selected reference. See Section 7.7.7.

0 = Phase monitor alarm does not trigger a phase build-out event
1 = Phase monitor alarm does trigger a phase build-out event

**Bits 3 to 0: Phase Monitor Limit (PMLIM[3:0]).** This field is an unsigned integer that specifies the magnitude of phase error that causes a phase monitor alarm to be declared (PHMON bit in the MSR3 register). The phase monitor limit in nanoseconds is equal to (PMLIM[3:0] + 7) x 156.25, which corresponds to a range of 1094ns to 3437ns in 156.25ns steps. The phase monitor is enabled by setting PMEN = 1. See Section 7.7.7.

**Register Name:** PHASE1
**Register Description:** Phase Register 1
**Register Address:** 77h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | PHASE[7:0] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The PHASE1 and PHASE2 registers must be read consecutively. See Section 8.3.

**Bits 7 to 0: Current DPLL Phase (PHASE[7:0]).** The full 16-bit PHASE[15:0] field spans this register and the PHASE2 register. PHASE is a two's-complement signed integer that indicates the current value of the phase detector. The value is the output of the phase averager. When T4T0 = 0 in the MCR11 register, PHASE indicates the current phase of the T0 DPLL. When T4T0 = 1, PHASE indicates the current phase of the T4 DPLL. The averaged phase difference in degrees is equal to PHASE x 0.707. See Section 7.7.10.

**Register Name:** PHASE2
**Register Description:** Phase Register 2
**Register Address:** 78h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | PHASE[15:8] | | | | | | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7 to 0: Current DPLL Phase (PHASE[15:8]).** See the PHASE1 register description.

**Register Name:** PHLKTO
**Register Description:** Phase Lock Timeout Register
**Register Address:** 79h

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | PHLKTOM[1:0] | | PHLKTO[5:0] | | | | | |
| **Default** | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

**Bits 7 to 6: Phase Lock Timeout Multiplier (PHLKTOM[1:0]).** This field is an unsigned integer that specifies the resolution of the phase lock timeout field PHLKTO[5:0].

00 = 2 seconds
01 = 4 seconds
10 = 8 seconds
11 = 16 seconds

**Bits 5 to 0: Phase Lock Timeout (PHLKTO[5:0]).** This field is an unsigned integer that, together with the PHLKTOM[1:0] field, specifies the length of time that the T0 DPLL attempts to lock to an input clock before declaring a phase lock alarm (by setting the corresponding LOCK bit in the ISR registers). The timeout period in seconds is PHLKTO[5:0] x 2^(PHLKTOM[1:0]+1). The state machine remains in the pre-locked, pre-locked 2, or phase-lost modes for the specified time before declaring a phase alarm on the selected input. See Section 7.7.1.

**Register Name:** FSCR1
**Register Description:** Frame Sync Configuration Register 1
**Register Address:** 7Ah

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | 2K8KSRC | — | — | — | 8KINV | 8KPUL | 2KINV | 2KPUL |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: 2kHz/8kHz Source (2K8KSRC).** This configuration bit specifies the source for the 2kHz and 8kHz outputs available on clock outputs OC1 to OC7. See Section 7.8.2.3.

0 = T0 DPLL
1 = T4 DPLL

**Bit 3: 8kHz Invert (8KINV).** When this bit is set to 1, the 8kHz signal on clock output OC10 is inverted. See Section 7.8.2.5.

0 = OC10 not inverted
1 = OC10 inverted

**Bit 2: 8kHz Pulse (8KPUL).** When this bit is set to 1, the 8kHz signal on clock output OC10 is pulsed rather than 50% duty cycle. In this mode output clock OC3 must be enabled, and the pulse width of OC10 is equal to the clock period of OC3. See Section 7.8.2.5.

0 = OC10 not pulsed; 50% duty cycle
1 = OC10 pulsed, with pulse width equal to OC3 period

**Bit 1: 2kHz Invert (2KINV).** When this bit is set to 1, the 2kHz signal on clock output OC11 is inverted. See Section 7.8.2.5.

0 = OC11 not inverted
1 = OC11 inverted

**Bit 0: 2kHz Pulse (2KPUL).** When this bit is set to 1, the 2kHz signal on clock output OC11 is pulsed rather than 50% duty cycle. In this mode output clock OC3 must be enabled, and the pulse width of OC11 is equal to the clock period of OC3. See Section 7.8.2.5.

0 = OC11 not pulsed; 50% duty cycle
1 = OC11 pulsed, with pulse width equal to OC3 period

**Register Name:** FSCR2
**Register Description:** Frame Sync Configuration Register 2
**Register Address:** 7Bh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | INDEP | OCN | — | — | — | — | PHASE[1:0] | |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7: Independent Frame Sync and Multiframe Sync (INDEP).** When this bit is set to 0, the 8kHz frame sync on OC10 and the 2kHz multiframe sync on OC11 are aligned with the other output clocks when synchronized with the SYNC2K input. When this bit is 1, the frame sync and multiframe sync are independent of the other output clocks, and their edge position may change without disturbing the other output clocks. See Section 7.9.3.

0 = OC10 and OC11 are aligned with other output clocks; all are synchronized by the SYNC2K input
1 = OC10 and OC11 are independent of the other clock outputs; only OC10 and OC11 are synchronized by the SYNC2K input

**Bit 6: Sync OC-N Rates (OCN).** See Section 7.9.3.

0 = SYNC2K is sampled with a 6.48MHz resolution; the selected reference must be 6.48MHz
1 = If the selected reference is 19.44MHz, SYNC2K is sampled at 19.44MHz and output alignment is to 19.44MHz. If the selected reference is 38.88MHz, SYNC2K is sampled at 38.88MHz. The selected reference must be either 19.44MHz or 38.88MHz

**Bits 1 to 0: External Sync Sampling Phase. (PHASE[1:0]).** This field adjusts the sampling of the SYNC2K input. Normally the falling edge of SYNC2K is aligned with the falling edge of the selected reference. All UI numbers listed below are UI of the sampling clock. See Section 7.9.3.

00 = Coincident
01 = 0.5UI early
10 = 1 UI late
11 = 0.5UI late

**Register Name:** FSCR3
**Register Description:** Frame Sync Configuration Register 3
**Register Address:** 7Ch

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | RECAL | MONLIM[2:0] | | | SOURCE[3:0] | | | |
| **Default** | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |

**Bit 7: Phase Offset Recalibration (RECAL).** When set to 1 this configuration bit causes a recalibration of the phase offset between the output clocks and the selected reference. This process puts the DPLL into mini holdover, internally ramps the phase offset to zero, resets all clock dividers, ramps the phase offset to the value stored in the OFFSET registers, and then switches the DPLL out of mini holdover. Unlike simply writing the OFFSET registers, the RECAL process causes no change in the phase offset of the output clocks. RECAL is automatically reset to 0 when recalibration is complete. See Section 7.7.8.

0 = Normal operation
1 = Phase offset recalibration

**Bits 6 to 4: Sync Monitor Limit (MONLIM[2:0]).** This field configures the sync monitor limit. When the external SYNC2K input is misaligned with respect to the OC11 output by the specified number of resampling clock cycles then a frame sync monitor alarm is declared in the FSMON bit of the OPSTATE register. See Section 7.9.3.

000 = ± 1 UI
001 = ± 2 UI
010 = ± 3 UI
011 = ± 4 UI
100 = ± 5 UI
101 = ± 6 UI
110 = ± 7 UI
111 = ± 8 UI

**Bits 3 to 0: Sync Reference Source (SOURCE[3:0]).** The external sync reference may be associated with one of the input clocks. When automatic external frame sync is enabled (AEFSEN = 1 in the MCR3 register, the SYNC2K pin is only enabled when the T0 DPLL is locked to the input clock specified by the SOURCE field. See Section 7.9.3.

0000 = {unused value}
0001 = IC1
0010 = IC2
0011 = IC3
0100 = IC4
0101 = IC5
0110 = IC6
0111 = IC7
1000 = IC8
1001 = IC9
1010 = IC10
1011 = IC11
1100 = IC12
1101 = IC13
1110 = IC14
1111 = {unused value}

**Register Name:** INTCR
**Register Description:** Interrupt Configuration Register
**Register Address:** 7Dh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | — | — | — | GPO | OD | POL |
| **Default** | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**Bit 2: INTREQ Pin General Purpose Output Enable (GPO).** When set to 1 this bit configures the interrupt request pin to be a general purpose output whose value is set by the POL bit.

0 = INTREQ is used for interrupts
1 = INTREQ is a general purpose output

**Bit 1: INTREQ Pin Open Drain Enable (OD).**

When GPO = 0:
0 = INTREQ is driven in both inactive and active states
1 = INTREQ is open-drain, i.e., it is driven in the active state but is high impedance in the inactive state
When GPO = 1:
0 = INTREQ is driven as specified by POL
1 = INTREQ is high impedance and POL has no effect

**Bit 0: INTREQ Pin Polarity (POL).**

When GPO = 0:
0 = INTREQ goes low to signal an interrupt (active low)
1 = INTREQ goes high to signal an interrupt (active high)
When GPO = 1:
0 = INTREQ driven low
1 = INTREQ driven high

**Register Name:** PROT
**Register Description:** Protection Register
**Register Address:** 7Eh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | PROT[7:0] | | | | | | | |
| **Default** | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**Bits 7 to 0: Protection Control (PROT[7:0]).** This field can be used to protect the rest of the register set from inadvertent writes. In protected mode writes to all other registers are ignored. In single unprotected mode, one register (other than PROT) can be written, but after that write the device reverts to protected mode (and the value of PROT is internally changed to 00h). In fully unprotected mode all register can be written without limitation. See Section 7.2.

1000 0101 = Fully unprotected mode
1000 0110 = Single unprotected mode
all other values = Protected mode

**Register Name:** IFCR
**Register Description:** Microprocessor Interface Configuration Register
**Register Address:** 7Fh

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | — | — | — | — | — | IFSEL[2:0] | | |
| **Default** | 0 | 0 | 0 | 0 | 0 | reset value of IFSEL[2:0] pins | | |

**Bits 2:0 Microprocessor Interface Selection (IFSEL[2:0]).** This read-only field specifies the microprocessor interface mode. The value of this register is latched from the IFSEL[2:0] pins during reset. After reset the state of the IFSEL[2:0] pins has no effect on this register but is shown in the IFSR register. See Section 7.11.

010 = Intel bus mode (multiplexed)
011 = Intel bus mode (nonmultiplexed)
100 = Motorola mode (nonmultiplexed)
101 = SPI mode (address and data transmitted LSB first)
110 = Motorola mode (multiplexed)
111 = SPI mode (address and data transmitted MSB first)
000, 001 = {unused value}

# 9. JTAG TEST ACCESS PORT AND BOUNDARY SCAN

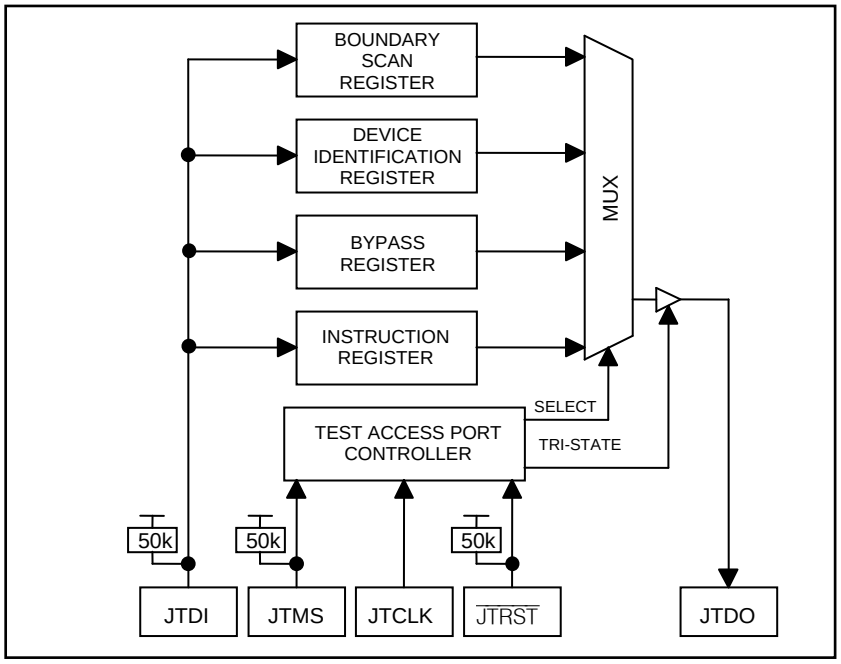
## 9.1 JTAG Description

The DS3101 supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. Figure 9-1 shows a block diagram. The DS3101 contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

| | |
|---|---|
| Test Access Port (TAP) | Bypass Register |
| TAP Controller | Boundary Scan Register |
| Instruction Register | Device Identification Register |

The TAP has the necessary interface pins, namely JTCLK, $\overline{\text{JTRST}}$, JTDI, JTDO, and JTMS. Details on these pins can be found in Table 6-6. Details about the boundary scan architecture and the TAP can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

### Figure 9-1. JTAG Block Diagram



## 9.2 JTAG TAP Controller State Machine Description

This section discusses the operation of the TAP controller state machine. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. Each of the states denoted in Figure 9-2 are described in the following paragraphs.

**Test-Logic-Reset.** Upon device power-up, the TAP controller starts in the Test-Logic-Reset state. The instruction register contains the IDCODE instruction. All system logic on the device operates normally.

**Run-Test-Idle.** Run-Test-Idle is used between scan operations or during specific tests. The instruction register and all test registers remain idle.

**Select-DR-Scan.** All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

**Capture-DR.** Data can be parallel-loaded into the test register selected by the current instruction. If the instruction does not call for a parallel load or the selected test register does not allow parallel loads, the register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or to the Exit1-DR state if JTMS is high.

**Shift-DR.** The test register selected by the current instruction is connected between JTDI and JTDO and data is shifted one stage toward the serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

**Exit1-DR.** While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state, which terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

**Pause-DR.** Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

**Exit2-DR.** While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

**Update-DR.** A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output because of changes in the shift register. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

**Select-IR-Scan.** All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

**Capture-IR.** The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

**Shift-IR.** In this state, the instruction register's shift register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK toward the serial output. The parallel register and the test registers remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state, while moving data one stage through the instruction shift register.

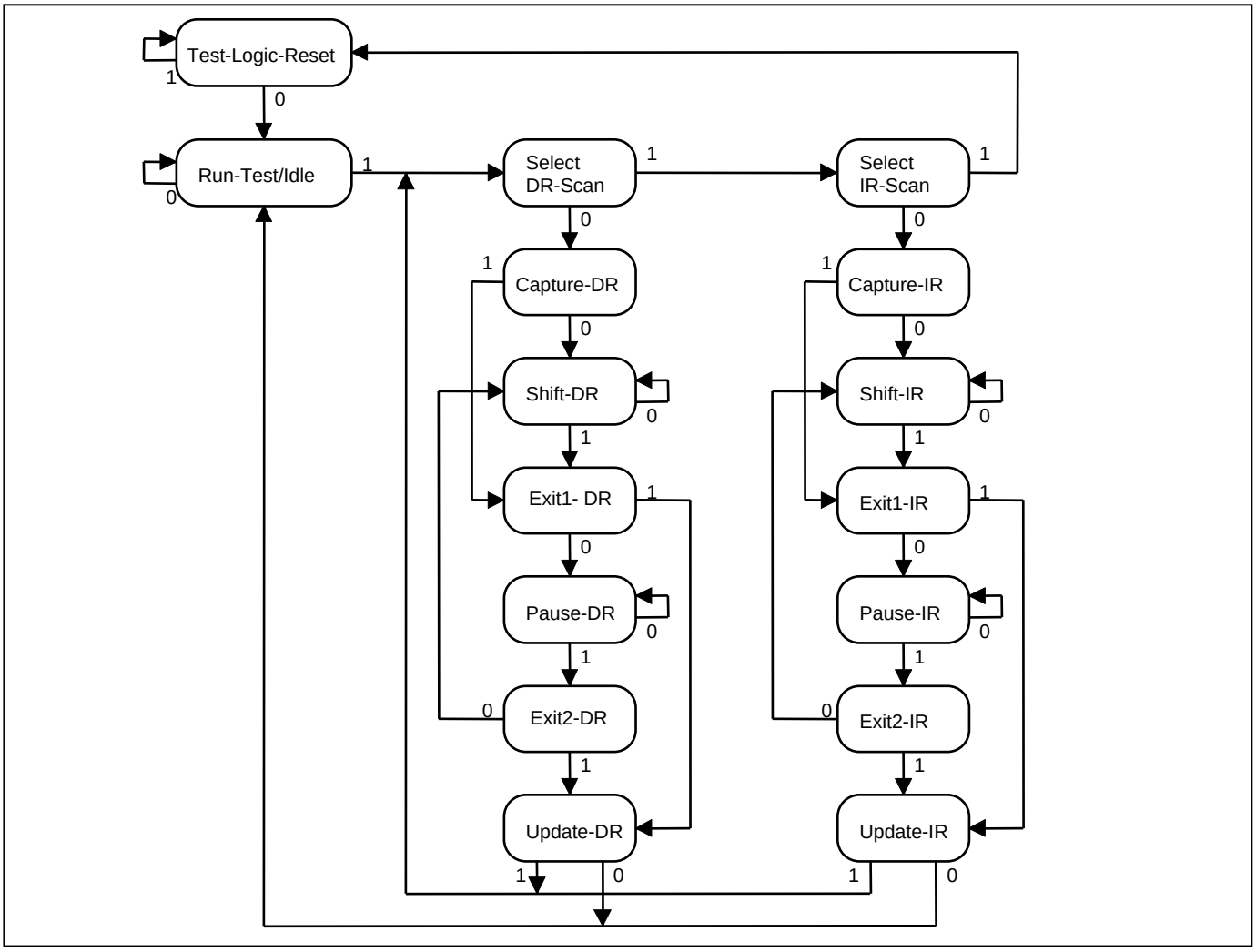
**Exit1-IR.** A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

**Pause-IR.** Shifting of the instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

**Exit2-IR.** A rising edge on JTCLK with JTMS high puts the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

**Update-IR.** The instruction shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

## Figure 9-2. JTAG TAP Controller State Machine



## 9.3 JTAG Instruction Register and Instructions

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage toward the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Table 9-1 shows the instructions supported by the DS3101 and their respective operational binary codes.

### Table 9-1. JTAG Instruction Codes

| INSTRUCTIONS | SELECTED REGISTER | INSTRUCTION CODES |
|---|---|---|
| SAMPLE/PRELOAD | Boundary Scan | 010 |
| BYPASS | Bypass | 111 |
| EXTEST | Boundary Scan | 000 |
| CLAMP | Bypass | 011 |
| HIGHZ | Bypass | 100 |
| IDCODE | Device Identification | 001 |

**SAMPLE/PRELOAD.** SAMPLE/RELOAD is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. First, the digital I/Os of the device can be sampled at the boundary scan register, using the Capture-DR state, without interfering with the device's normal operation. Second, data can be shifted into the boundary scan register through JTDI using the Shift-DR state.

**EXTEST.** EXTEST allows testing of the interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur: (1) Once the EXTEST instruction is enabled through the Update-IR state, the parallel outputs of the digital output pins are driven. (2) The boundary scan register is connected between JTDI and JTDO. (3) The Capture-DR state samples all digital inputs into the boundary scan register.

**BYPASS.** When the BYPASS instruction is latched into the parallel instruction register, JTDI is connected to JTDO through the 1-bit bypass register. This allows data to pass from JTDI to JTDO without affecting the device's normal operation.

**IDCODE.** When the IDCODE instruction is latched into the parallel instruction register, the device identification register is selected. The device ID code is loaded into the device identification register on the rising edge of JTCLK, following entry into the Capture-DR state. Shift-DR can be used to shift the ID code out serially through JTDO. During Test-Logic-Reset, the ID code is forced into the instruction register's parallel output.

**HIGHZ.** All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO.

**CLAMP.** All digital output pins output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

## 9.4 JTAG Test Registers

IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. An optional test register, the identification register, has been included in the device design. It is used with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

**Bypass Register.** This is a single 1-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions to provide a short path between JTDI and JTDO.

**Boundary Scan Register.** This register contains a shift register path and a latched parallel output for control cells and digital I/O cells. BSDL files are available at www.maxim-ic.com/TechSupport/telecom/bsdl.htm.

**Identification Register.** This register contains a 32-bit shift register and a 32-bit latched parallel output. It is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state. The device identification code for the DS3101 is shown in Table 9-2.

### Table 9-2. JTAG ID Code

| DEVICE | REVISION | DEVICE CODE | MANUFACTURER CODE | REQUIRED |
|---|---|---|---|---|
| DS3101 | Consult factory | 0000000000011101 | 00010100001 | 1 |

# 10. ELECTRICAL CHARACTERISTICS

## ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin with Respect to $V_{SS}$ (except $V_{DD}$)……..-0.3V to +5.5V
Supply Voltage Range ($V_{DD}$) with Respect to $V_{SS}$……..-0.3V to +1.98V
Supply Voltage Range ($V_{DDIO}$) with Respect to $V_{SS}$……-0.3V to +3.63V
Ambient Operating Temperature Range……..-40°C to +85°C (**Note 1**)
Junction Operating Temperature Range……..-40°C to +125°C
Storage Temperature Range……..-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

**Note 1:** Specifications to -40°C are guaranteed by design and not production tested.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device. Ambient operating temperature range when device is mounted on a four-layer JEDEC test board with no airflow.*

**Note:** The typical values listed in the tables of Section 10 are not production tested.

## 10.1 DC Characteristics

### Table 10-1. Recommended DC Operating Conditions

($T_A$ = -40°C to +85°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage, Core | $V_{DD}$ | | 1.62 | 1.8 | 1.98 | V |
| Supply Voltage, I/O | $V_{DDIO}$ | | 3.135 | 3.3 | 3.465 | V |
| Ambient Temperature Range | $T_A$ | | -40 | | +85 | °C |

### Table 10-2. DC Characteristics

($V_{DD}$ = 1.8V ±10%, $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C.)

| PARAMETER | | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Current | 1.8V | $I_{DD18}$ | (Note 2) | | 100 | 120 | mA |
| | 3.3V | $I_{DD33}$ | (Note 2) | | 37 | 53 | |
| Supply Current from VDD_OC6 When output OC6 is Enabled | | $I_{DDOC6}$ | (Note 3) | | 9 | | mA |
| Supply Current from VDD_OC7 When output OC7 is Enabled | | $I_{DDOC7}$ | (Note 3) | | 9 | | mA |
| Input Capacitance | | $C_{IN}$ | | | 5 | | pF |
| Output Capacitance | | $C_{OUT}$ | | | 7 | | pF |

**Note 2:** 12.800MHz clock applied to REFCLK. 19.44MHz clock applied to one CMOS/TTL input clock pin. One 19.44MHz CMOS/TTL output clock pin driving 100pF load; all other inputs at $V_{DDIO}$ or grounded; all other outputs open.

**Note 3:** 19.44MHz output clock frequency, driving the load shown in Figure 10-1.

## Table 10-3. CMOS/TTL Pins

($V_{DD}$ = 1.8V ±10%, $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | | 2.0 | | 5.5 | V |
| Input Low Voltage | $V_{IL}$ | | -0.3 | | +0.8 | V |
| Input Leakage | $I_{IL}$ | (Note 1) | -10 | | +10 | µA |
| Input Leakage, Pins with Internal Pullup Resistor (50kΩ typical) | $I_{ILPU}$ | (Note 1) | -85 | | +10 | µA |
| Input Leakage, Pins with Internal Pulldown Resistor (50kΩ typical) | $I_{ILPD}$ | (Note 1) | -10 | | +85 | µA |
| Output Leakage (when High-Z) | $I_{LO}$ | (Note 1) | -10 | | +10 | µA |
| Output High Voltage ($I_O$ = -4.0mA) | $V_{OH}$ | | 2.4 | | $V_{DDIO}$ | V |
| Output Low Voltage ($I_O$ = +4.0mA) | $V_{OL}$ | | 0 | | 0.4 | V |

**Note 1:** $0V < V_{IN} < V_{DDIO}$ for all other digital inputs.

## Table 10-4. LVDS Pins

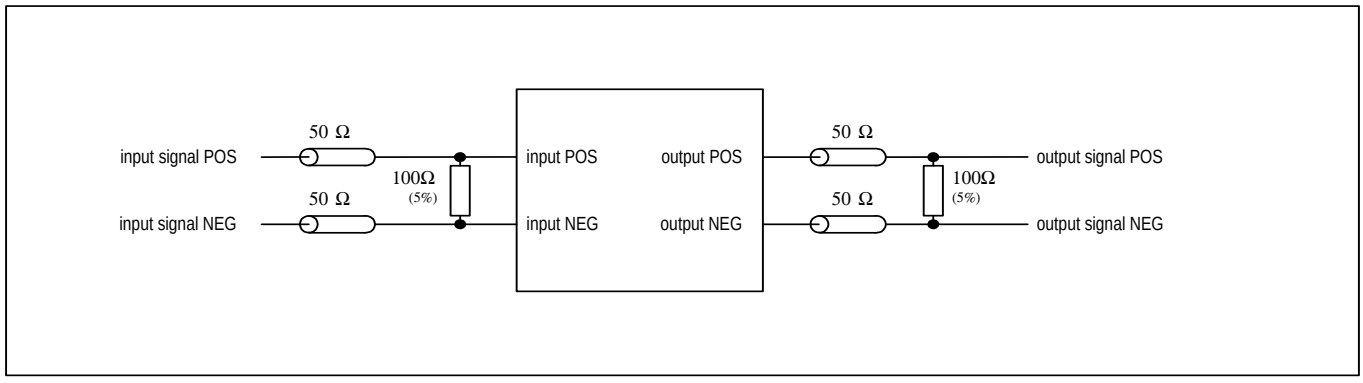
($V_{DD}$ = 1.8V ±10%, $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C.) (See Figure 10-1.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{INLVDS}$ | $V_{IDLVDS}$ = 100mV | 0 | | 2.4 | V |
| Differential Input Voltage | $V_{IDLVDS}$ | | 0.1 | | 1.4 | V |
| Differential Input Logic Threshold | $V_{THLVDS}$ | | -100 | | +100 | mV |
| Output High Voltage | $V_{OHLVDS}$ | (Note 1) | | 1.45 | 1.65 | V |
| Output Low Voltage | $V_{OLLVDS}$ | (Note 1) | 0.885 | 1.1 | | V |
| Differential Output Voltage | $V_{ODLVDS}$ | | 250 | | 450 | mV |
| Output Offset Voltage | $V_{OSLVDS}$ | +25°C (Note 1) | 1.08 | 1.28 | 1.45 | V |
| Difference in Magnitude of Output Differential Voltage for Complementary States | $V_{DOSLVDS}$ | | | | 25 | mV |

**Note 1:** With 100Ω load across the differential outputs.

**Note 2:** The DS3101's LVDS output pins can easily be interfaced to LVPECL and CML inputs on neighboring ICs using a few external passive components. Refer to Maxim App Note HFAN-1.0 for details.

## Figure 10-1. Recommended Termination for LVDS Pins



## Table 10-5. LVPECL Pins

($V_{DD}$ = 1.8V ±10%, $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C) (See Figure 10-2.)

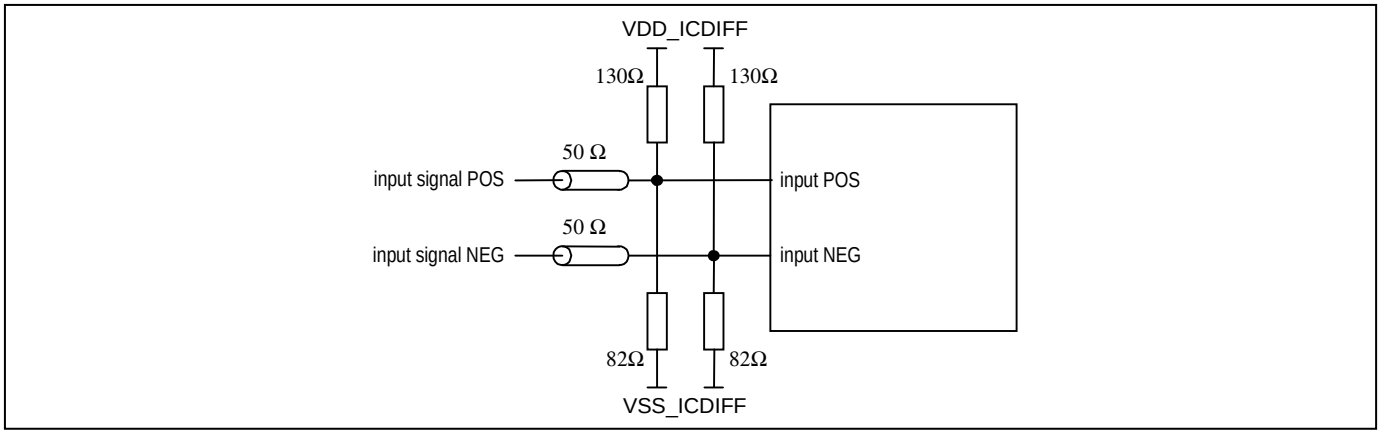
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input High Voltage, Differential Inputs | $V_{IHPECL}$ | (Note 1) | $V_{DDIO}$ - 2.4 | | $V_{DDIO}$ - 0.4 | V |
| Input Low Voltage, Differential Inputs | $V_{ILPECL}$ | (Note 1) | $V_{DDIO}$ - 2.5 | | $V_{DDIO}$ - 0.5 | V |
| Input Differential Voltage | $V_{IDPECL}$ | | 0.1 | | 1.4 | V |
| Input High Voltage, Single-Ended Inputs | $V_{IHPECL,S}$ | (Note 2) | $V_{DDIO}$ - 1.3 | | $V_{DDIO}$ - 0.5 | V |
| Input Low Voltage, Single-Ended Inputs | $V_{ILPECL,S}$ | (Note 2) | $V_{DDIO}$ - 2.4 | | $V_{DDIO}$ - 1.5 | V |

**Note 1:** For a differential input voltage ≥ 100mV.

**Note 2:** With the unused differential input tied to $V_{DDIO}$ - 1.4V.

**Note 3:** Although the DS3101's differential outputs do not directly drive standard LVPECL signals, these output pins can easily be interfaced to LVPECL and CML inputs on neighboring ICs using a few external passive components. Refer to Maxim App Note HFAN-1.0 for details.

## Figure 10-2. Recommended Termination for LVPECL Pins



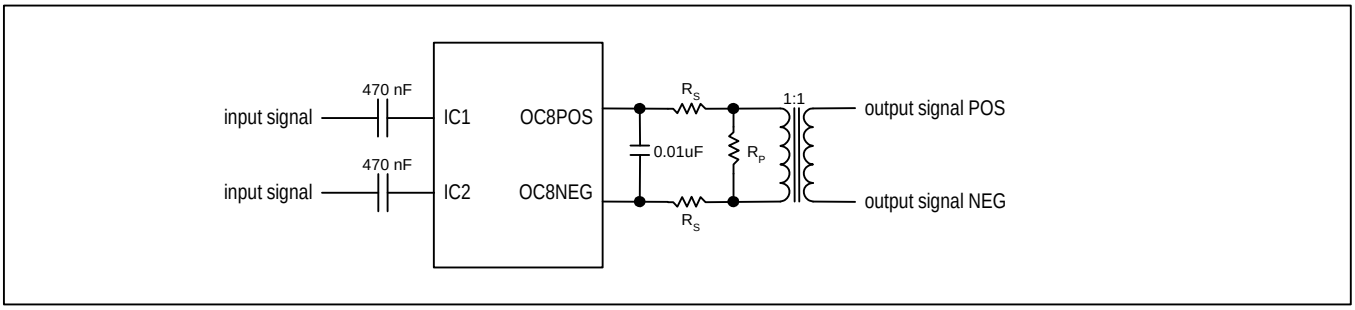
## Table 10-6. AMI Composite Clock Pins

($V_{DD}$ = 1.8V ±10%, $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C.) (Note 1) (See Figure 10-3.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IHAMI}$ | | 2.2 | | $V_{DDIO}$ + 0.3 | V |
| Input Middle Voltage | $V_{IMAMI}$ | | 1.5 | 1.65 | 1.8 | V |
| Input Low Voltage | $V_{ILAMI}$ | | -0.3 | | 1.1 | V |
| Input LOS Threshold | $V_{LOS}$ | At the IC1/IC2 pin | | 0.2 | | V |
| Input Pulse Width | $t_{PW}$ | | 1.6 | 7.8 | 14 | µs |
| Input Rise/Fall Time | $t_R$, $t_F$ | | | | 0.5 | µs |

**Note 1:** The timing parameters in this table are guaranteed by design (GBD).

## Figure 10-3. Recommended External Components for AMI Composite Clock Pins




For input CC signals compliant with Telcordia GR-378 (amplitude 2.7V to 5.5V) or ITU G.703 Section 4.2.2 option b) (3V±0.5V), the signal should be attenuated by a factor of 3 (or more) before being presented to IC1A or IC2A. Input CC signals with a 1V nominal pulse amplitude can be presented unattenuated.

For output CC signals, Table 10-7 specifies recommended values for the components in Figure 10-3. Recommended transformers include the PE-65540 from Pulse Engineering.

## Table 10-7. Recommended External Components for Output Clock OC8

| SIGNAL TYPE | $R_S$ | $R_P$ |
|---|---|---|
| GR-378 (133Ω, 2.7V–5.5V) | 0 | Open |
| G.703 4.2.2 option b) (110Ω, 3V ±0.5V) | 0 | Open |
| G.703 4.2.2 option a) and Appendix II.1 (110Ω, 1V ±0.1V) | 91Ω | 360Ω |
| G.703 4.2.3 (120Ω, 1V ±0.1V) | 91Ω | 300Ω |

## 10.2 Input Clock Timing

### Table 10-8. Input Clock Timing

($V_{DD}$ = 1.8V ±10%, $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C.)

| PARAMETER | SYMBOL | MIN | TYP | MAX |
|---|---|---|---|---|
| Input Clock Period, CMOS/TTL Input Pins | $t_{CYC}$ | 8ns (125MHz) | | 500µs (2kHz) |
| Input Clock Period, LVDS/LVPECL Input Pins | $t_{CYC}$ | 6.43ns (155.52MHz) | | 500µs (2kHz) |
| Input Clock High, Low Time | $t_H$, $t_L$ | 3ns or 30% of $t_{CYC}$, whichever is smaller | | |

## 10.3 Output Clock Timing

### Table 10-9. Input Clock to Output Clock Delay

| INPUT FREQUENCY | OUTPUT FREQUENCY | DELAY, INPUT CLOCK EDGE TO OUTPUT CLOCK EDGE |
|---|---|---|
| 8kHz | 8kHz | 0.0 ± 1.5ns |
| 6.48MHz | 6.48MHz | -12 ± 1.5ns |
| 19.44MHz | 19.44MHz | 0.0 ± 1.5ns |
| 25.92MHz | 25.92MHz | 0.0 ± 1.5ns |
| 38.88MHz | 38.88MHz | 0.0 ± 1.5ns |
| 51.84MHz | 51.84MHz | 0.0 ± 1.5ns |
| 77.76MHz | 77.76MHz | 0.0 ± 1.5ns |
| 155.52MHz | 155.52MHz | 0.0 ± 1.5ns |

### Table 10-10. Output Clock Phase Alignment, Frame Sync Alignment Mode

| OUTPUT FREQUENCY | DELAY, OC1 (2kHz) FALLING EDGE TO OUTPUT CLOCK FALLING EDGE |
|---|---|
| 8kHz (OC10) | 0.0 ± 0.5ns |
| 2kHz | 0.0 ± 0.5ns |
| 8kHz | 0.0 ± 0.5ns |
| 1.544MHz (OC9) | 0.0 ± 1.25ns |
| 2.048MHz (OC9) | 0.0 ± 1.25ns |
| 44.736MHz | -2.0 ± 1.25ns |
| 34.368MHz | -2.0 ± 1.25ns |
| 6.48MHz | -2.0 ± 1.25ns |
| 19.44MHz | -2.0 ± 1.25ns |
| 25.92MHz | -2.0 ± 1.25ns |
| 38.88MHz | -2.0 ± 1.25ns |
| 51.84MHz | -2.0 ± 1.25ns |
| 77.76MHz | -2.0 ± 1.25ns |
| 155.52MHz | -2.0 ± 1.25ns |
| 311.04MHz | -2.0 ± 1.25ns |

See Section 7.9.3 for details on frame sync alignment and the SYNC2K pin.

## 10.4 Parallel Interface Timing

### Table 10-11. Parallel Interface Timing

($V_{DD}$ = 1.8V ±10%, $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C.) (Note 1) (See Figure 10-4 and Figure 10-5.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Address Setup to $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active | t1a | (Note 2) | 10 | | | ns |
| ALE Setup to $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active | t1b | (Notes 2, 3) | 10 | | | ns |
| Address Setup to ALE Inactive | t2 | (Notes 2, 3) | 2 | | | ns |
| Address Hold from ALE Inactive | t3 | (Notes 2, 3) | 2 | | | ns |
| ALE Pulse Width | t4 | (Notes 2, 3) | 5 | | | ns |
| Address Hold from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Inactive | t5 | (Note 2) | 0 | | | ns |
| $\overline{CS}$ Setup to $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active | t6 | (Note 2) | 0 | | | ns |
| Data Valid from $\overline{RD}$, $\overline{DS}$ Active | t8 | (Note 2) | | | 80 | ns |
| $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Pulse Width if not Using $\overline{RDY}$ Handshake | t9a | (Notes 2, 4) | 90 | | | ns |
| $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Delay from $\overline{RDY}$ Active | t9b | (Note 2) | 15 | | | ns |
| Data Output High-Z from $\overline{RD}$, $\overline{DS}$ Inactive | t10 | (Notes 2, 5) | 2 | | 10 | ns |
| Data Output Enabled from $\overline{RD}$, $\overline{DS}$ Active | t11 | (Note 2) | 2 | | | ns |
| $\overline{CS}$ Hold from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Inactive | t12 | (Note 2) | 0 | | | ns |
| Data Setup to $\overline{WR}$, $\overline{DS}$ Inactive | t13 | (Note 2) | 10 | | | ns |
| Data Hold from $\overline{WR}$, $\overline{DS}$ inactive | t14 | (Note 2) | 5 | | | ns |
| $\overline{RDY}$ Active from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active | t15 | (Note 2) | 10 | | | ns |
| $\overline{RDY}$ Inactive from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Inactive | t16 | (Note 2) | 0 | | 10 | ns |
| $\overline{RDY}$ Output Enabled from $\overline{CS}$ Active | t17 | (Note 2) | | | 10 | ns |
| $\overline{RDY}$ Output High-Z from $\overline{CS}$ Inactive | t18 | (Note 2) | | | 10 | ns |
| $\overline{RDY}$ Ending High Pulse Width | t19 | (Note 2) | 2 | | | ns |
| R/$\overline{W}$ Setup to $\overline{DS}$ Active | t20 | (Note 2) | 2 | | | ns |
| R/$\overline{W}$ Hold from $\overline{DS}$ Inactive | t21 | (Note 2) | 2 | | | ns |

**Note 1:** The timing parameters in this table are guaranteed by design (GBD).
**Note 2:** The input/output timing reference level for all signals is VDD/2. Transition time (80/20%) on $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ inputs is 5ns max.
**Note 3:** Multiplexed mode timing only.
**Note 4:** Timing required if not using $\overline{RDY}$ handshake.
**Note 5:** D[7:0] output valid until not driven.

**Figure 10-4. Parallel Interface Timing Diagram (Nonmultiplexed)**

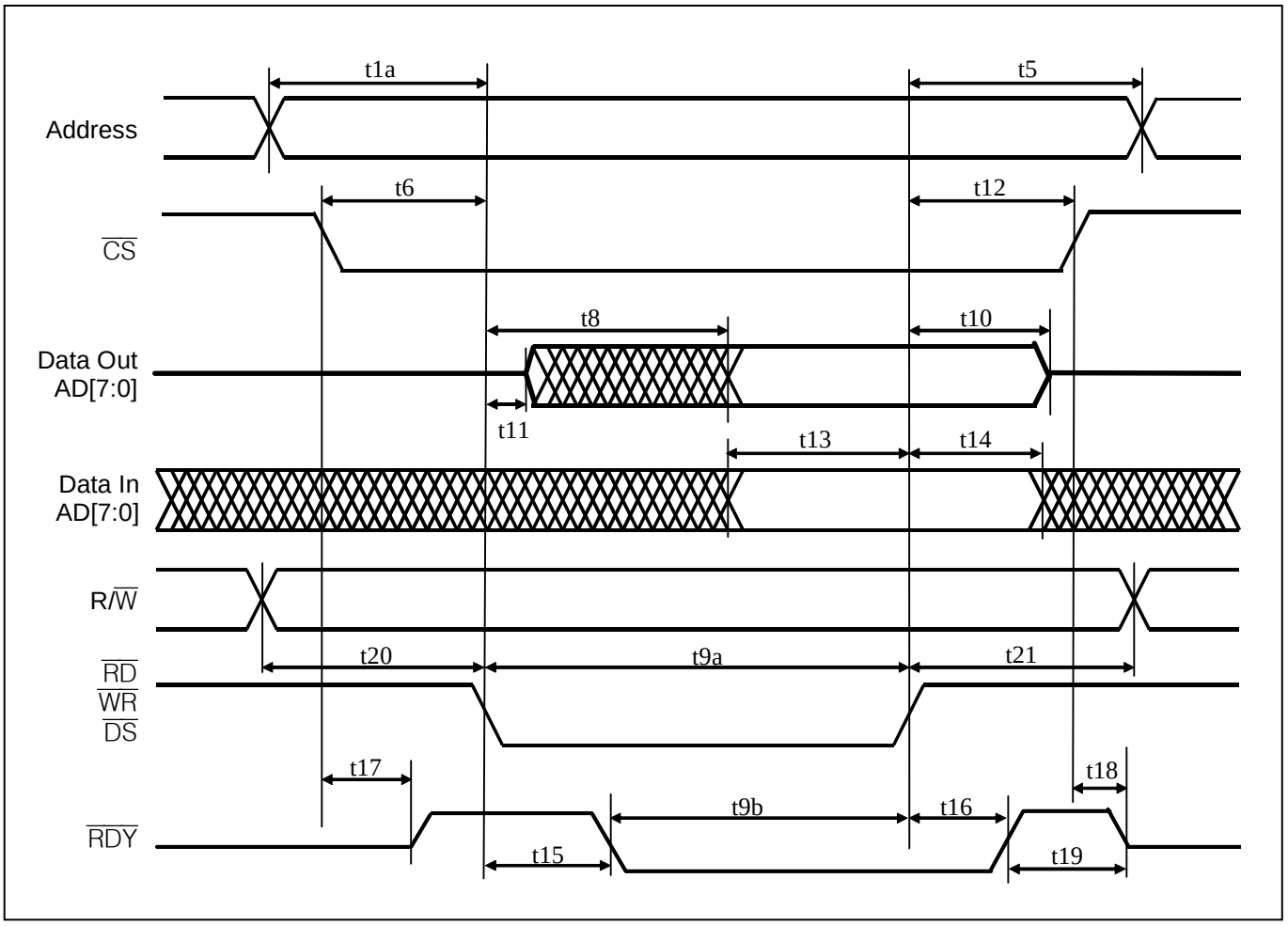
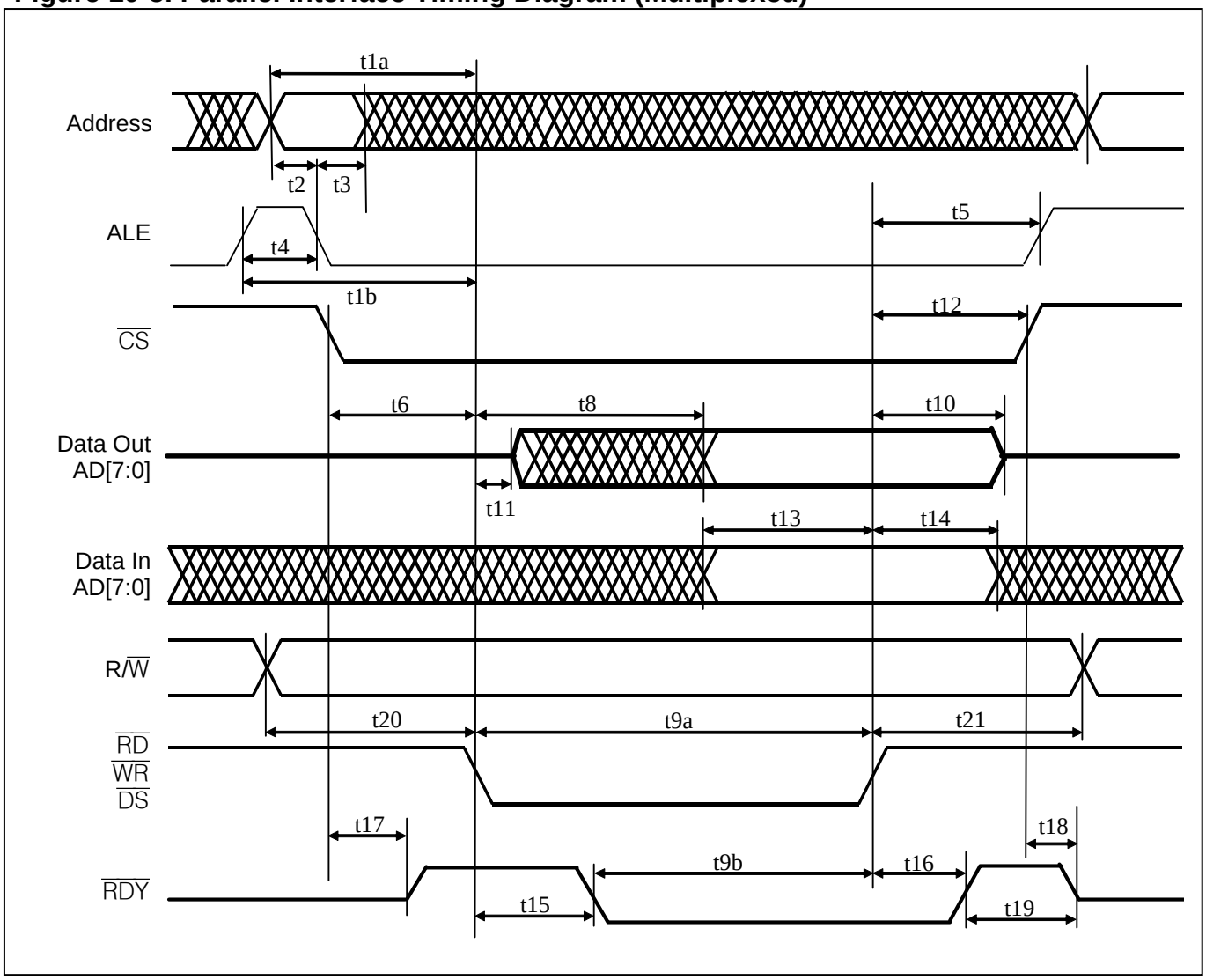


**Figure 10-5. Parallel Interface Timing Diagram (Multiplexed)**



## 10.5 SPI Interface Timing

### Table 10-12. SPI Interface Timing

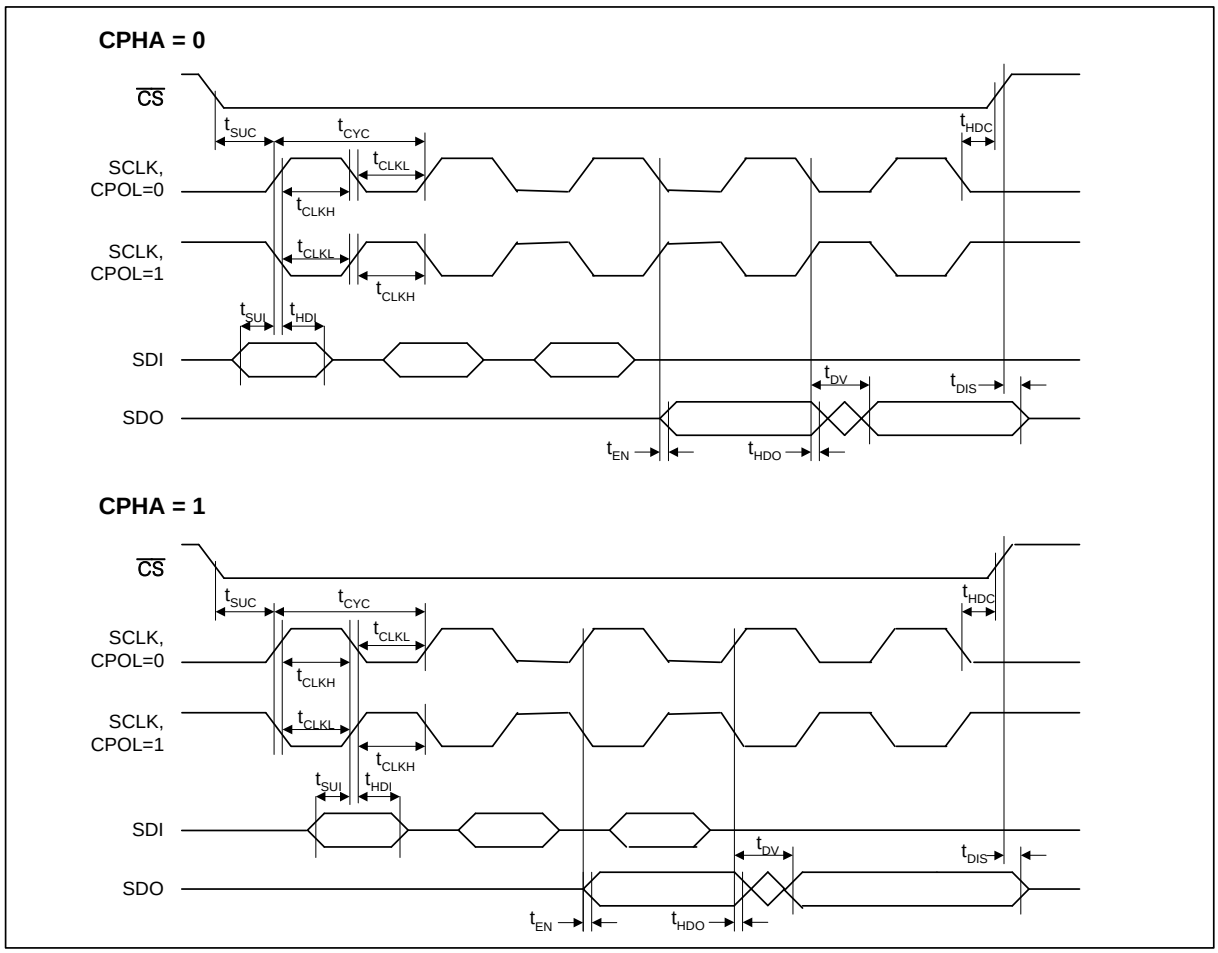
($V_{DD}$ = 1.8V ±10%, $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C.) (Note 1) (See Figure 10-6.)

| PARAMETER (Note 2) | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| SCLK Frequency | $f_{BUS}$ | | | 6 | MHz |
| SCLK Cycle Time | $t_{CYC}$ | 166 | | | ns |
| $\overline{CS}$ Setup to First SCLK Edge | $t_{SUC}$ | 15 | | | ns |
| $\overline{CS}$ Hold time After Last SCLK Edge | $t_{HDC}$ | 15 | | | ns |
| SCLK High Time | $t_{CLKH}$ | 50 | | | ns |
| SCLK Low Time | $t_{CLKL}$ | 50 | | | ns |
| SDI Data Setup Time | $t_{SUI}$ | 5 | | | ns |
| SDI Data Hold Time | $t_{HDI}$ | 15 | | | ns |
| SDO Enable Time (High-Impedance to Output Active) | $t_{EN}$ | 0 | | | ns |
| SDO Disable Time (Output Active to High Impedance) | $t_{DIS}$ | | | 25 | ns |
| SDO Data Valid Time | $t_{DV}$ | | | 40 | ns |
| SDO Data Hold Time After Update SCLK Edge | $t_{HDO}$ | 5 | | | ns |

**Note 1:** The timing parameters in this table are guaranteed by design (GBD).

**Note 2:** All timing is specified with 100pF load on all SPI pins.

### Figure 10-6. SPI Interface Timing Diagram



## 10.6 JTAG Interface Timing

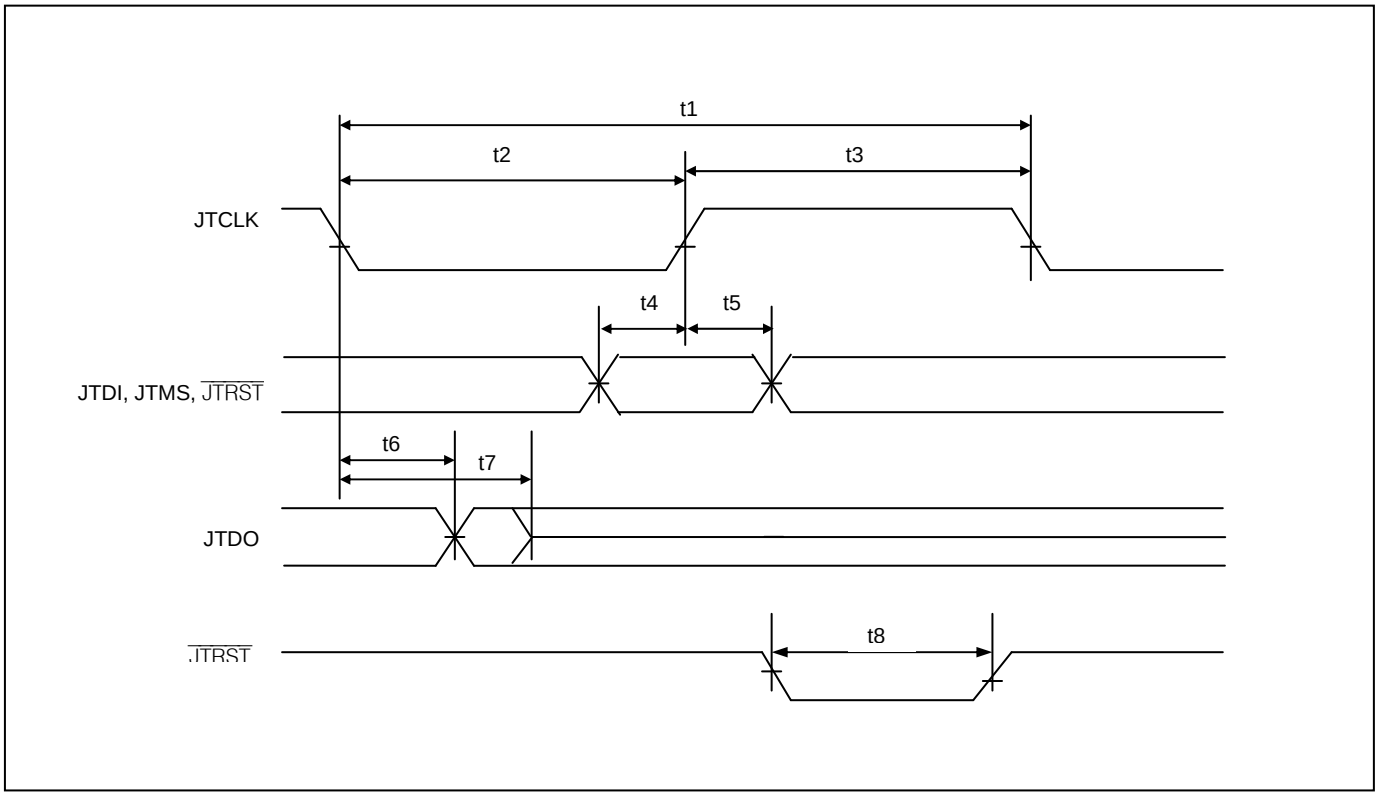
### Table 10-13. JTAG Interface Timing

($V_{DD}$ = 1.8V ±10%, $V_{DDIO}$ = 3.3V ±5%, $T_A$ = -40°C to +85°C.) (Note 1) (See Figure 10-7.)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| JTCLK Clock Period | t1 | | 1000 | | ns |
| JTCLK Clock High/Low Time (Note 2) | t2/t3 | 50 | 500 | | ns |
| JTCLK to JTDI, JTMS Setup Time | t4 | 50 | | | ns |
| JTCLK to JTDI, JTMS Hold Time | t5 | 50 | | | ns |
| JTCLK to JTDO Delay | t6 | 2 | | 50 | ns |
| JTCLK to JTDO High-Z Delay (Note 3) | t7 | 2 | | 50 | ns |
| $\overline{\text{JTRST}}$ Width Low Time | t8 | 100 | | | ns |

**Note 1:** The timing parameters in this table are guaranteed by design (GBD).
**Note 2:** Clock can be stopped high or low.
**Note 3:** Not tested during production test.

### Figure 10-7. JTAG Timing Diagram



# 11. PIN ASSIGNMENTS

Table 11-1 lists the DS3101 pin assignments sorted in alphabetical order by pin name. Figure 11-1 and Figure 11-2 show pin assignments arranged by pin number.

## Table 11-1. Pin Assignments Sorted by Signal Name

| PIN NAME | PIN NUMBER | BUS MODES | SIGNAL TYPE |
|---|---|---|---|
| A[0] | H16 | Parallel-Only | High-Speed Digital |
| A[1] | H15 | Parallel-Only | High-Speed Digital |
| A[2] | G16 | Parallel-Only | High-Speed Digital |
| A[3] | H14 | Parallel-Only | High-Speed Digital |
| A[4] | G15 | Parallel-Only | High-Speed Digital |
| A[5] | F16 | Parallel-Only | High-Speed Digital |
| A[6] | G14 | Parallel-Only | High-Speed Digital |
| A[7] | F15 | Parallel-Only | High-Speed Digital |
| A[8] | E16 | Parallel-Only | High-Speed Digital |
| AD[0] | E15 | Parallel-Only | High-Speed Digital |
| AD[1] | D16 | Parallel-Only | High-Speed Digital |
| AD[2] | C16 | Parallel-Only | High-Speed Digital |
| AD[3] | D15 | Parallel-Only | High-Speed Digital |
| AD[4] | C15 | Parallel-Only | High-Speed Digital |
| AD[5] | E14 | Parallel-Only | High-Speed Digital |
| AD[6] | D14 | Parallel-Only | High-Speed Digital |
| AD[7] | C14 | Parallel-Only | High-Speed Digital |
| ALE | K14 | Parallel-Only | High-Speed Digital |
| AVDD_PLL1 | D1 | All | Power Supply |
| AVDD_PLL2 | E1 | All | Power Supply |
| AVDD_PLL3 | F1 | All | Power Supply |
| AVDD_PLL4 | G1 | All | Power Supply |
| AVSS_PLL1 | D2 | All | Power Supply |
| AVSS_PLL2 | E3 | All | Power Supply |
| AVSS_PLL3 | G2 | All | Power Supply |
| AVSS_PLL4 | G3 | All | Power Supply |
| CPHA | D14 | SPI-Only | Low-Speed Digital |
| CPOL | C14 | SPI-Only | Low-Speed Digital |
| $\overline{CS}$ | J16 | All | High-Speed Digital |
| $\overline{DS}$ | J14 | Parallel-Only | High-Speed Digital |
| GPIO1 | E2 | All | Low-Speed Digital |
| GPIO2 | F3 | All | Low-Speed Digital |
| GPIO3 | H2 | All | Low-Speed Digital |
| GPIO4 | J1 | All | Low-Speed Digital |
| $\overline{HIZ}$ | R14 | All | Low-Speed Digital |
| IC1 | A10 | All | High-Speed Digital |
| IC10 | B12 | All | High-Speed Digital |
| IC11 | A13 | All | High-Speed Digital |
| IC12 | C12 | All | High-Speed Digital |
| IC13 | B13 | All | High-Speed Digital |
| IC14 | A14 | All | High-Speed Digital |

| PIN NAME | PIN NUMBER | BUS MODES | SIGNAL TYPE |
|---|---|---|---|
| IC1A | P6 | All | Low-Speed Analog |
| IC2 | B10 | All | High-Speed Digital |
| IC2A | P7 | All | Low-Speed Analog |
| IC3 | C10 | All | High-Speed Digital |
| IC4 | A11 | All | High-Speed Digital |
| IC5NEG | A5 | All | High-Speed Analog |
| IC5POS | B5 | All | High-Speed Analog |
| IC6NEG | A4 | All | High-Speed Analog |
| IC6POS | B4 | All | High-Speed Analog |
| IC7 | B11 | All | High-Speed Digital |
| IC8 | C11 | All | High-Speed Digital |
| IC9 | A12 | All | High-Speed Digital |
| IFSEL[0] | N1 | All | Low-Speed Digital |
| IFSEL[1] | N2 | All | Low-Speed Digital |
| IFSEL[2] | P1 | All | Low-Speed Digital |
| INTREQ | A15 | All | Low-Speed Digital |
| JTCLK | R8 | All | Low-Speed Digital |
| JTDI | R9 | All | Low-Speed Digital |
| JTDO | P9 | All | Low-Speed Digital |
| JTMS | T9 | All | Low-Speed Digital |
| $\overline{\text{JTRST}}$ | T8 | All | Low-Speed Digital |
| MASTSLV | R11 | All | Low-Speed Digital |
| N.C. | C13, F2, F14, H3, J3, K1, K2, K3, K15, K16, L1, L2, L3, L14, L15, L16, M1, M14, M15, M16, N3, N14, N15, N16, P2–P5, P8, P10–P16, R2–R7, R10, R12, R15, T2–T7, T10–T14 | All | No Connection |
| OC1 | C6 | All | High-Speed Digital |
| OC10 | B9 | All | Low-Speed Digital |
| OC11 | C9 | All | Low-Speed Digital |
| OC2 | A7 | All | High-Speed Digital |
| OC3 | B7 | All | High-Speed Digital |
| OC4 | C7 | All | High-Speed Digital |
| OC5 | A8 | All | High-Speed Digital |
| OC6NEG | A3 | All | High-Speed Analog |
| OC6POS | B3 | All | High-Speed Analog |
| OC7NEG | C1 | All | High-Speed Analog |
| OC7POS | C2 | All | High-Speed Analog |
| OC8NEG | B8 | All | Low-Speed Analog |
| OC8POS | C8 | All | Low-Speed Analog |
| OC9 | A9 | All | Low-Speed Digital |
| R/$\overline{\text{W}}$ | J15 | Parallel-Only | High-Speed Digital |
| $\overline{\text{RD}}$ | J14 | Parallel-Only | High-Speed Digital |
| $\overline{\text{RDY}}$ | B15 | Parallel-Only | High-Speed Digital |
| REFCLK | H1 | All | Low-Speed Digital |
| $\overline{\text{RST}}$ | B6 | All | Low-Speed Digital |

| PIN NAME | PIN NUMBER | BUS MODES | SIGNAL TYPE |
|---|---|---|---|
| SCLK | C16 | SPI-Only | Low-Speed Digital |
| SDI | D16 | SPI-Only | Low-Speed Digital |
| SDO | E15 | SPI-Only | Low-Speed Digital |
| SONSDH | M3 | All | Low-Speed Digital |
| SRCSW | M2 | All | Low-Speed Digital |
| SRFAIL | J2 | All | Low-Speed Digital |
| SYNC2K | B14 | All | Low-Speed Digital |
| TM1 | R13 | All | Test, Wire Low |
| TM2 | T15 | All | Test, Wire Low |
| TST_RA1 | R6 | All | Test, Do Not Connect |
| TST_RA2 | L14 | All | Test, Do Not Connect |
| TST_RB1 | T6 | All | Test, Do Not Connect |
| TST_RB2 | K16 | All | Test, Do Not Connect |
| TST_RC1 | R7 | All | Test, Do Not Connect |
| TST_RC2 | K15 | All | Test, Do Not Connect |
| TST_TA1 | P2 | All | Test, Do Not Connect |
| TST_TA2 | R15 | All | Test, Do Not Connect |
| TST_TB1 | N3 | All | Test, Do Not Connect |
| TST_TB2 | P13 | All | Test, Do Not Connect |
| TST_TC1 | P3 | All | Test, Do Not Connect |
| TST_TC2 | P14 | All | Test, Do Not Connect |
| $V_{DD}$ | D6, D8, D9, D11, E6, E11, F4, F5, F12, F13, H4, H13, J4, J13, L4, L5, L12, L13, M6, M11, N6, N8, N9, N11 | All | Power Supply |
| VDD_ICDIFF | A6 | All | Power Supply |
| VDD_OC6 | B2 | All | Power Supply |
| VDD_OC7 | C3 | All | Power Supply |
| $V_{DDIO}$ | B1, B16, D7, D10, E7–E10, G4, G5, G12, G13, H5, H12, J5, J12, K4, K5, K12, K13, M7, M8, M9, M10, N7, N10, R1, R16 | All | Power Supply |
| $V_{SS}$ | A1, A16, D4, D5, D12, D13, E4, E5, E12, E13, F6–F11, G6–G11, H6–H11, J6–J11, K6–K11, L6–L11, M4, M5, M12, M13, N4, N5, N12, N13, T1, T16 | All | Power Supply |
| VSS_ICDIFF | C4 | All | Power Supply |
| VSS_OC6 | A2 | All | Power Supply |
| VSS_OC7 | D3 | All | Power Supply |
| WDT | C5 | All | Low-Speed Analog |
| $\overline{WR}$ | J15 | Parallel-Only | High-Speed Digital |

## Figure 11-1. DS3101 Pin Assignment—Left Half

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| A | $V_{SS}$ | VSS_OC6 | OC6NEG | IC6NEG | IC5NEG | VDD_ICDIFF | OC2 | OC5 |
| B | $V_{DDIO}$ | VDD_OC6 | OC6POS | IC6POS | IC5POS | $\overline{RST}$ | OC3 | OC8NEG |
| C | OC7NEG | OC7POS | VDD_OC7 | VSS_ICDIFF | WDT | OC1 | OC4 | OC8POS |
| D | AVDD_PLL1 | AVSS_PLL1 | VSS_OC7 | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDIO}$ | $V_{DD}$ |
| E | AVDD_PLL2 | GPIO1 | AVSS_PLL2 | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDIO}$ | $V_{DDIO}$ |
| F | AVDD_PLL3 | N.C. | GPIO2 | $V_{DD}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| G | AVDD_PLL4 | AVSS_PLL3 | AVSS_PLL4 | $V_{DDIO}$ | $V_{DDIO}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| H | REFCLK | GPIO3 | N.C. | $V_{DD}$ | $V_{DDIO}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| J | GPIO4 | SRFAIL | N.C. | $V_{DD}$ | $V_{DDIO}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| K | N.C. | N.C. | N.C. | $V_{DDIO}$ | $V_{DDIO}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| L | N.C. | N.C. | N.C. | $V_{DD}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| M | N.C. | SRCSW | SONSDH | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDIO}$ | $V_{DDIO}$ |
| N | IFSEL[0] | IFSEL[1] | N.C. | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDIO}$ | $V_{DD}$ |
| P | IFSEL[2] | N.C. | N.C. | N.C. | N.C. | IC1A | IC2A | N.C. |
| R | $V_{DDIO}$ | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | JTCLK |
| T | $V_{SS}$ | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | JTRST |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |

- High-Speed Analog
- Low-Speed Analog
- High-Speed Digital
- Low-Speed Digital
- $V_{DD}$ 3.3V
- Analog $V_{DD}$ 3.3V
- $V_{DD}$ 1.8V
- Analog $V_{DD}$ 1.8V
- $V_{SS}$
- Analog $V_{SS}$
- N.C. = No Connection. Lead is not connected to anything inside the device.

## Figure 11-2. DS3101 Pin Assignment—Right Half

| 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|
| OC9 | IC1 | IC4 | IC9 | IC11 | IC14 | INTREQ | VSS | A |
| OC10 | IC2 | IC7 | IC10 | IC13 | SYNC2K | $\overline{RDY}$ | VDDIO | B |
| OC11 | IC3 | IC8 | IC12 | N.C. | AD[7]/CPOL | AD[4] | AD[2]/SCLK | C |
| $V_{DD}$ | $V_{DDIO}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | AD[6]/CPHA | AD[3] | AD[1] / SDI | D |
| $V_{DDIO}$ | $V_{DDIO}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | AD[5] | AD[0]/SDO | A[8] | E |
| $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DD}$ | N.C. | A[7] | A[5] | F |
| $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDIO}$ | $V_{DDIO}$ | A[6] | A[4] | A[2] | G |
| $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDIO}$ | $V_{DD}$ | A[3] | A[1] | A[0] | H |
| $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDIO}$ | $V_{DD}$ | $\overline{RD}/\overline{DS}$ | $\overline{WR}$/R/$\overline{W}$ | $\overline{CS}$ | J |
| $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDIO}$ | $V_{DDIO}$ | $\overline{ALE}$ | N.C. | N.C. | K |
| $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DD}$ | N.C. | N.C. | N.C. | L |
| $V_{DDIO}$ | $V_{DDIO}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | N.C. | N.C. | N.C. | M |
| $V_{DD}$ | $V_{DDIO}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | N.C. | N.C. | N.C. | N |
| JTDO | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | P |
| JTDI | N.C. | MASTSLV | N.C. | TM1 | HIZ | N.C. | $V_{DDIO}$ | R |
| JTMS | N.C. | N.C. | N.C. | N.C. | N.C. | TM2 | $V_{SS}$ | T |
| 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |

- High-Speed Analog
- Low-Speed Analog
- High-Speed Digital
- Low-Speed Digital
- $V_{DD}$ 3.3V
- Analog $V_{DD}$ 3.3V
- $V_{DD}$ 1.8V
- Analog $V_{DD}$ 1.8V
- $V_{SS}$
- Analog $V_{SS}$
- N.C. = No Connection. Lead is not connected to anything inside the device.

# 12. PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

## 12.1 256-Pin CSBGA (17mm x 17mm)

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 256 CSBGA | — | **21-0315** |

# 13. THERMAL INFORMATION

## Table 13-1. Thermal Properties, Natural Convection

| PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|
| Ambient Temperature (Note 1) | -40 | | +85 | °C |
| Junction Temperature | -40 | | +125 | °C |
| Theta-JA ($\theta_{JA}$), Still Air (Note 2) | | 26.7 | | °C/W |
| Theta-JB ($\theta_{JB}$), Still Air | | 14.0 | | °C/W |
| Theta-JC ($\theta_{JC}$), Still Air | | 11.0 | | °C/W |
| Psi-JB | | 13.5 | | °C/W |
| Psi-JT | | 0.7 | | °C/W |

**Note 1:** The package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

**Note 2:** Theta-JA ($\theta_{JA}$) is the junction to ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

# 14. GLOSSARY

| | |
|---|---|
| **Local Oscillator** | The 12.800MHz TCXO, OCXO, or other crystal oscillator connected to the REFCLK pin. The stability of the T0 DPLL in free-run and holdover modes is a function of the stability of this oscillator. |
| **Master Clock** | A 204.8MHz clock synthesized from the local oscillator and frequency adjusted by the XOFREQ register setting. |
| **Input Clock** | One of the 14 input clocks labeled IC1 to IC14. |
| **Output Clock** | One of the 11 output clocks labeled OC1 to OC11. |
| **Selected Reference** | The input clock to which the DPLL is currently phase locked. |
| **Valid Clock** | An input clock that has no alarms declared in the corresponding ISR register. A clock whose frequency is within the hard limit set in ILIMIT or CLIMIT and that does not have an inactivity alarm. |
| **Invalid Clock** | An input clock that has one or more alarms declared in the corresponding ISR register. |
| **External Reference Switching Mode** | EXTSW = 1 in MCR10. |

# 15. ACRONYMS AND ABBREVIATIONS

| | |
|---|---|
| AIS | Alarm Indication Signal |
| AMI | Alternate Mark Inversion |
| APLL | Analog Phase-Locked Loop |
| BITS | Building Integrated Timing Supply |
| BPV | Bipolar Violation |
| DFS | Digital Frequency Synthesis |
| DPLL | Digital Phase Locked Loop |
| ESF | Extended Superframe |
| EXZ | Excessive Zeros |
| GbE | Gigabit Ethernet |
| I/O | Input/Output |
| LOS | Loss of Signal |
| LVDS | Low-Voltage-Differential Signal |
| LVPECL | Low-Voltage Positive Emitter-Coupled Logic |
| MTIE | Maximum Time Interval Error |
| OCXO | Oven-Controlled Crystal Oscillator |
| OOF | Out-of-Frame Alignment |
| PBO | Phase Build-Out |
| PFD | Phase/Frequency Detector |
| PLL | Phase-Locked Loop |
| ppb | Parts per Billion |
| ppm | Parts per Million |
| pk-pk | Peak-to-Peak |
| RMS | Root-Mean-Square |
| RAI | Remote Alarm Indication |
| RO | Read-Only |
| R/W | Read/Write |
| SDH | Synchronous Digital Hierarchy |
| SEC | SDH Equipment Clock |
| SETS | Synchronous Equipment Timing Source |
| SF | Superframe |
| SONET | Synchronous Optical Network |
| SSM | Synchronization Status Message |
| SSU | Synchronization Supply Unit |
| STM | synchronous Transport Module |
| TDEV | Time Deviation |
| TCXO | Temperature-Compensated Crystal Oscillator |
| UI | Unit Interval |
| $UI_{P-P}$ | Unit Interval, Peak to Peak |

# 16. TRADEMARK ACKNOWLEDGEMENTS

SPI is a trademark of Motorola, Inc.
Telcordia is a registered trademark of Telcordia Technologies.

## 17. DATA SHEET REVISION HISTORY

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 101706 | Initial release. | — |
| 1 | 061307 | In the Feature bullets, changed “G.812 Types I and III” to “G.812 Types I, III, and IV”. Updated spec name from G.pactiming to G.8261. | 1 |
| | | In Table 1-1, deleted reference to IEEE 1596.3 standard. | 6 |
| | | Updated Figure 3-1 to show backplane traces going between timing cards. | 8 |
| | | Edited Section 7.4 to indicate minimum high time or low time is 3ns or 30% of clock period, whichever is smaller. | 20 |
| | | In Table 7-2, added indications that IC5 and IC6 can be CMOS/TTL inputs. | 21 |
| | | Added note at the end of Section 7.7.1.7 to indicate that mini-holdover follows the manual holdover setting. | 30 |
| | | In Section 7.7.2, corrected a typo to say the T4 DPLL only operates in revertive switching mode rather than “does not have revertive switching mode.” | |
| | | Edited section 7.7.6 and the DLIMIT1 and DLIMIT3:FLLOL descriptions to indicate the T4 DPLL’s hard limit is fixed at ±80ppm and is not controlled by the HARDLIM field. | 33, 89, 96 |
| | | In Section 7.8.1, added hyperlink to Maxim App Note HFAN-1.0. | 39 |
| | | In Table 7-13, updated many of the typical RMS and peak-to-peak jitter numbers to match actual device performance. | 44–47 |
| | | Added a 25MHz row to Table 7-13. | 46 |
| | | In the 125MHz row of Table 7-13, corrected a typo by changing “OC4 and OC5 only” to “OC5 only.” | 47 |
| | | Rewrote Section 7.14 to refer readers to the web or Telecom Support for the latest initialization scripts. | 58 |
| | | Edited the OFREQ1 to OFREQ7 fields in the OCR registers to indicate that if the T4 DPLL is configured for 62.5MHz, then OFREQ = 1100 specifies T4 APLL frequency divided by 10 to give an output frequency of 25MHz. | 101–104 |
| | | In Table 10-2, changed $I_{DD18}$ from 95mA typ to 100mA typ and 115mA max to 120mA max; changed $I_{DD33}$ from 25mA typ to 37mA typ and 30mA max to 53mA max; changed $I_{DDOC6}$ and $I_{DDOC7}$ from 8mA typ to 9mA typ. | 130 |
| | | In Table 10-3, changed $V_{DD}$ to $V_{DDIO}$ in Note 1. | 131 |
| | | In Table 10-4, changed $V_{OHLVDS}$ to 1.45V typ, 1.65V max; added $V_{OLLVDS}$ 1.1V typ; changed $V_{OSLVDS}$ to 1.08V min, 1.28V typ, 1.45V max. | |
| | | Added Note 2 to Table 10-4. | |
| | | In Table 10-5, deleted specs $I_{IHPECL}$ and $I_{IILPECL}$ specs and in Note 2 changed $V_{DD}$ to $V_{DDIO}$. Added Note 3 to Table 10-5. | 132 |
| | | In Table 10-6 in the $V_{IHAMI}$ spec, changed max from $V_{DD}$ + 0.3 to $V_{DDIO}$ + 0.3 and deleted the $I_{AMIOUT}$, $V_{OHAMI}$, and $V_{OLAMI}$ specs because the specs in Table 7-16 and Figure 7-7 are sufficient to govern output signal performance for OC8. | 133 |
| | | Updated Figure 10-3 and Table 10-7 and accompanying text to show new recommended external components. | |

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| | | Updated Table 10-8 to clarify minimum high time and low time (and therefore duty cycle) for input clocks. | 134 |
| | | Added GBD comments (Note 1) to AC timing characteristics in Section 10. | 133, 135, 138, 139 |
| 2 | 012108 | In Table 6-8, removed pins R13 and T15 from the N.C. row. (These pins are already listed in the TM1 and TM2 rows.) | 17 |
| | | Edited Section 7.12 to emphasize the need for the $\overline{RST}$ pin to be asserted once after power-up and to describe the need to wait at least 100µs after reset is deasserted before initializing the device. | 57 |
| | | In Section 10, added Note 1 to the Absolute Maximum Ratings. | 130 |
| 3 | 050708 | In Table 6-8, added pins H3, N3, P10, P11, R10, R12, T10–T14 to the N.C. pin row. | 17 |
| | | In Table 11-1, added pins H3, N3, P10, P11, R10, R12, T10–T14 to the N.C. pin row, and removed R13 and T15, which are in the TM1 and TM2 row. | 141 |
| 4 | 5/09 | On page 1 and various locations in the document, added mention of Stratum 2 compliance, expanded G.812 compliance to Types I – IV, and added G.8262 EEC compliance.<br>In Table 1-1, added G.8262.<br>In Table 6-1, indicated that differential inputs IC5 and IC6 could be configured as singled-ended CMOS/TTL and how to do it.<br>In Table 7-1, deleted the initial offset row since it is not an oscillator requirement.<br>Next to Table 8-1, added note indicating systems must be able to access entire address range 0-1FFh.<br>In Table 10-12, changed $t_{CYC}$ min to 166ns to match $f_{BUS}$ max. | 1, 6, 12, 19, 59, 138 |