

General Description

The WSF2060 is the highest performance trench N-ch MOSFET with extreme high cell density, which provide excellent RDS(on) and gate charge for most of the synchronous buck converter applications.

The WSF2060 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	60	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	42	A
I_{DM}	Pulsed Drain Current	210	A
EAS	Single Pulse Avalanche Energy	200	mJ
I_{AS}	Avalanche Current	41	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation ⁴	60	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State)	---	62	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ($t \leq 10\text{s}$)	---	25	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case	---	2.1	$^\circ\text{C/W}$

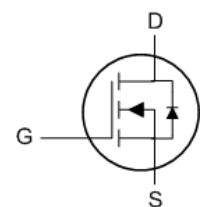
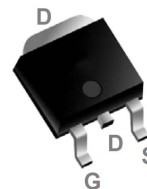
Product Summary

BVDSS	RDS(on)	ID
20V	3.9m Ω	60A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

TO-252 Pin Configuration



Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	20	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.028	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =4.5V, I _D =30A	---	3.9	5.5	mΩ
		V _{GS} =2.5V, I _D =20A	---	5.8	8.0	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	0.5	0.75	1.0	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-6.16	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =20V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =20V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =30A	15	---	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	1.0	3.1	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =15V, V _{GS} =4.5V, I _D =15A	---	27	---	nC
Q _{gs}	Gate-Source Charge		---	6.5	---	
Q _{gd}	Gate-Drain Charge		---	6.4	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =15V, V _{GS} =10V, R _G =3.3Ω I _D =15A	---	6.4	---	ns
T _r	Rise Time		---	17.2	---	
T _{d(off)}	Turn-Off Delay Time		---	29.6	---	
T _f	Fall Time		---	16.8	---	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	2000	---	pF
C _{oss}	Output Capacitance		---	500	---	
C _{rss}	Reverse Transfer Capacitance		---	200	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current	V _G =V _D =0V, Force Current	---	---	60	A
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	IF=20A, dI/dt=100A/μs, T _J =25°C	---	25	---	nS
Q _{rr}	Reverse Recovery Charge		---	24	---	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition : T_J=25°C, V_{DD}=10V, V_G=10V, L=0.5mH, R_G=25Ω,

Typical Characteristics

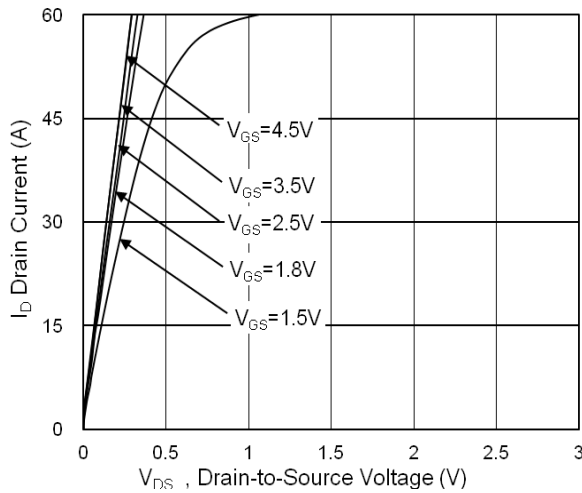


Fig.1 Typical Output Characteristics

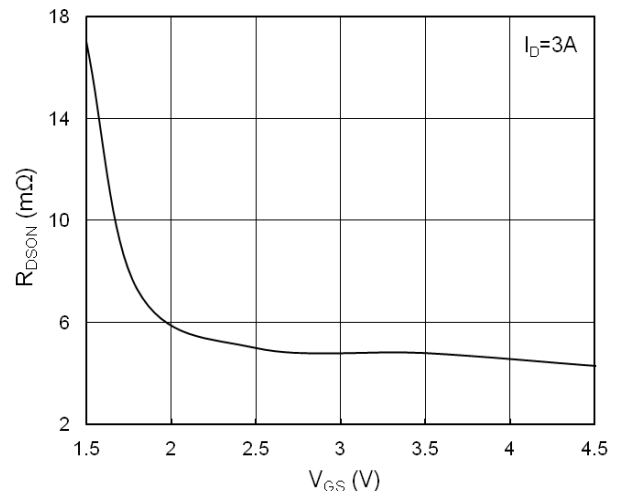


Fig.2 On-Resistance vs. Gate-Source

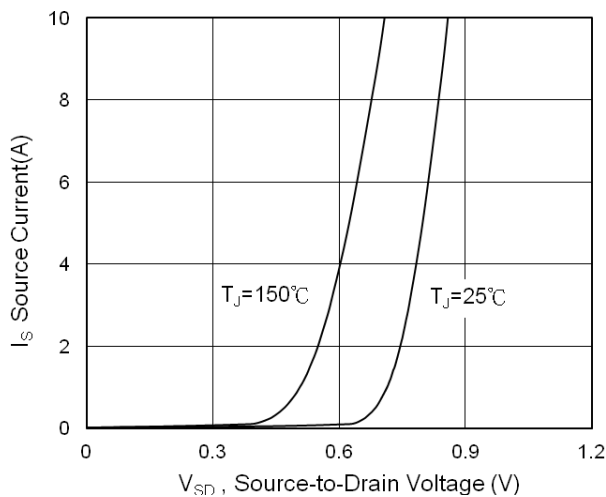


Fig.3 Forward Characteristics Of Reverse

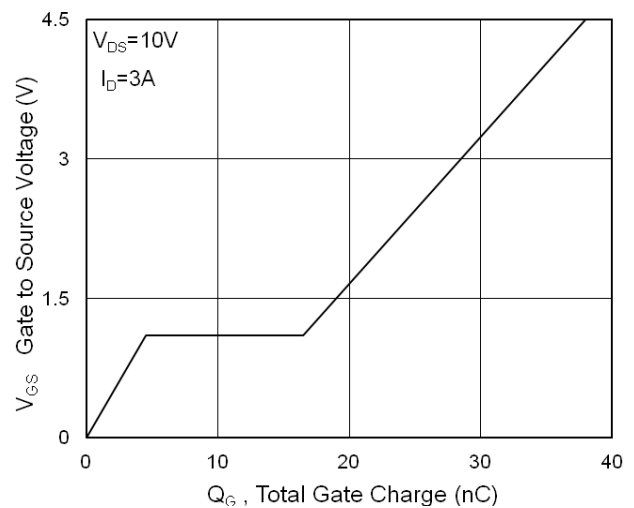


Fig.4 Gate-Charge Characteristics

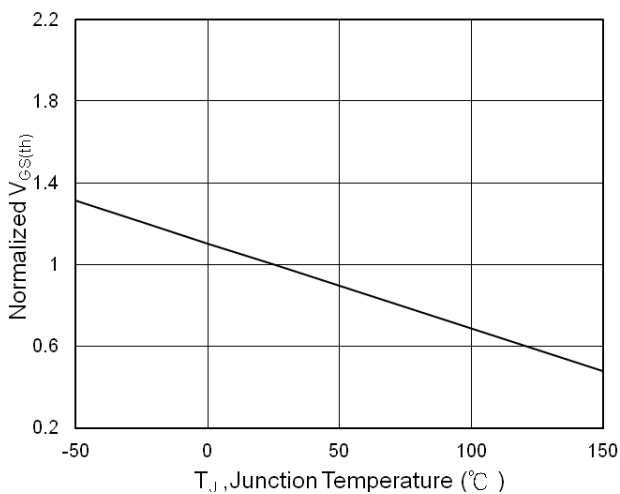


Fig.5 $V_{GS(th)}$ vs. T_J

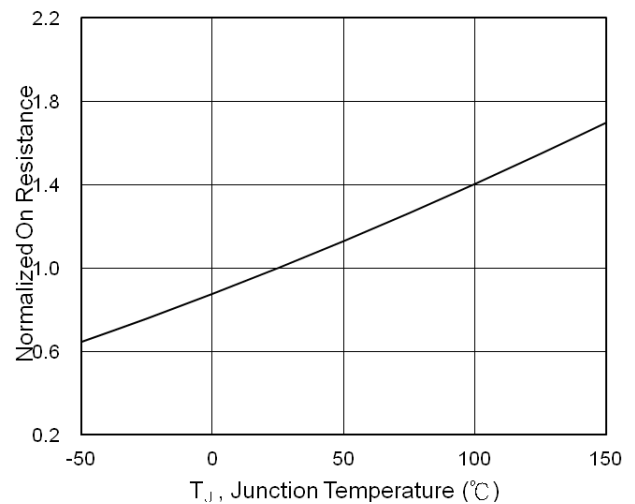


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

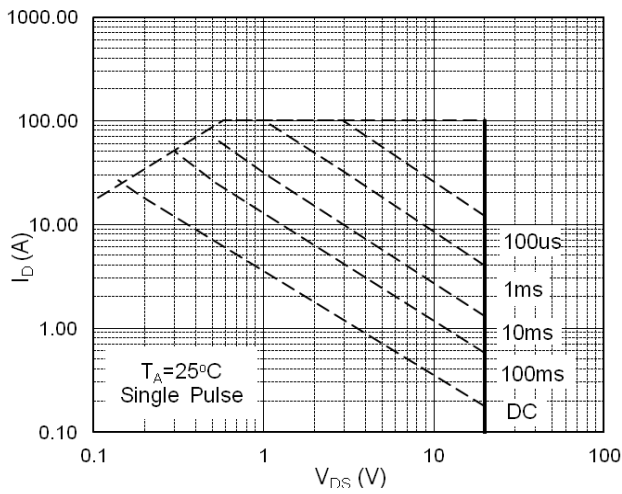


Fig.7 Capacitance

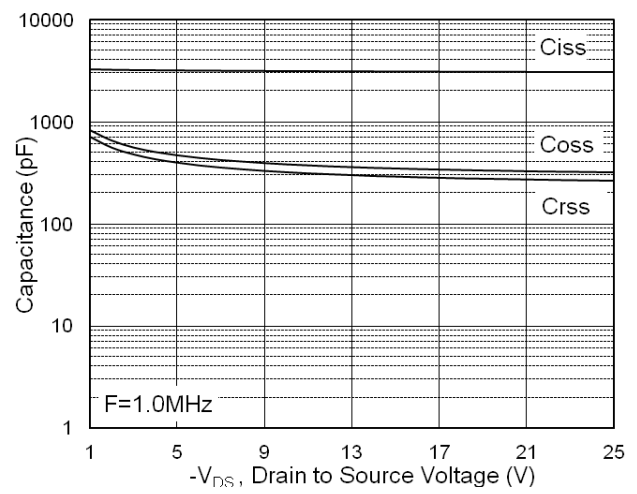


Fig.8 Safe Operating Area

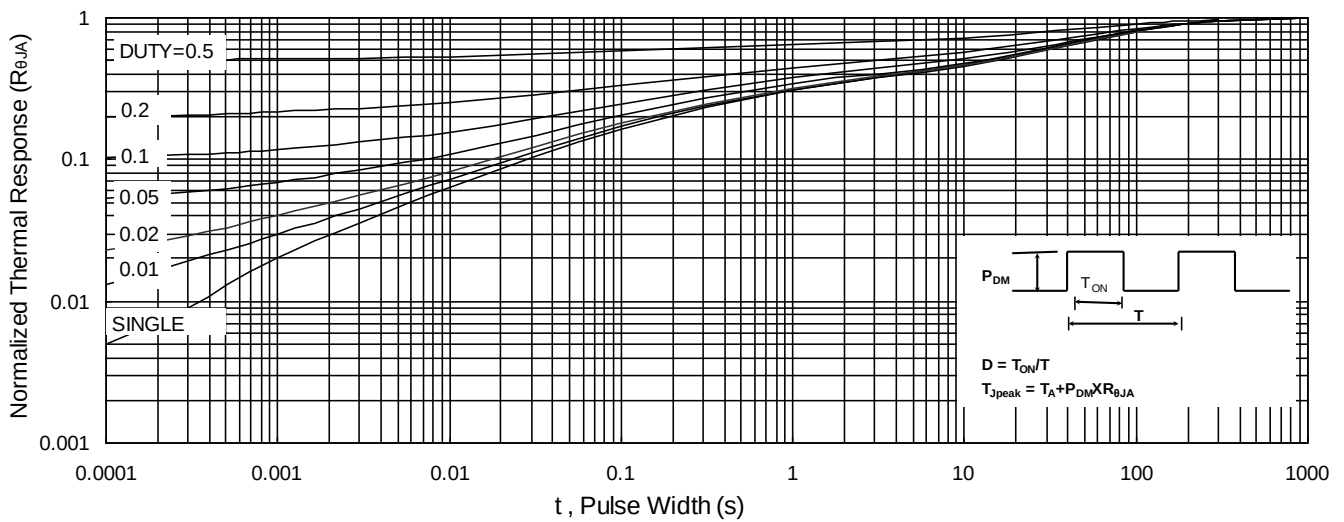


Fig.9 Normalized Maximum Transient Thermal Impedance

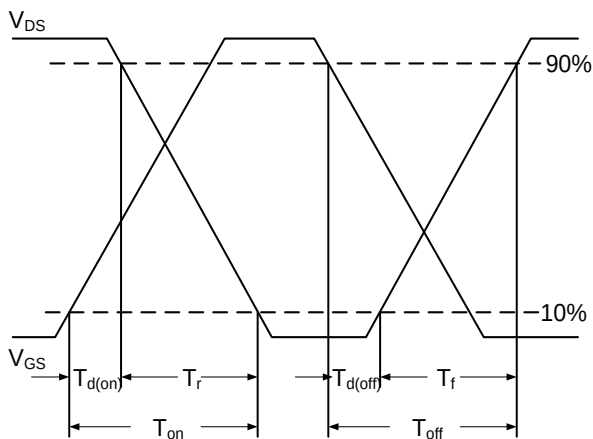


Fig.10 Switching Time Waveform

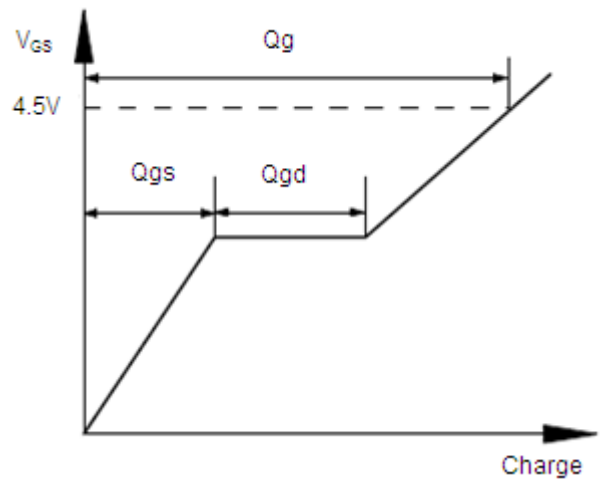


Fig.11 Gate Charge Waveform

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