Wire bonding Vertical Silicon Capacitor WBSC / WLSC 0303 10nF BV100

Rev.2.01

General description

WBSC / WLSC Capacitors targets power supplies decoupling and filtering of active devices. They are based on PICS Integrated Passive technology.

This product is a single 10nF capacitor in 0303 package size. Other capacitance values and other package size are available as a single die or capacitor array; please feel free to contact us.

WLSC capacitors are directly mounted on the PCB application using die bonding and wire bonding processes. Standard FR4 PCB can be used. The bottom electrode is in TiNiAu and the top electrode is in TiWAu. Other top finishings such as Aluminum are available on request.

Key features

- Compatible with MLCC footprint
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage <-0.02%/Volt
  - Negligible capacitance loss through ageing
- Low profile 0.1mm or 0.25mm
- Small size 0.80 x 0.80 mm (0303 format)
- Break down voltage : 100V
- Low leakage current
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 00303 footprint
- Applicable for standard wire bonding assembly (ball and wedge)

Key applications

- Any demanding applications, such as medical, aerospace, automotive industrial…
- Supply decoupling / filtering of active device
- High reliability applications
- Battery operated devices
- High temperature applications
- High volumetric efficiency *(i.e. capacitance per unit volume)*

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Functional diagram

The next figure provides implementation set-up diagram.

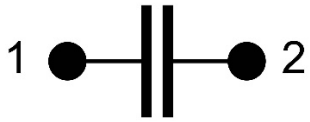

Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	10	-	nF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	20	150	°C
T_{STG}	Storage temperature (2)		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55°C to +150°C	-	41	-	ppm/K
RV_{DC}	Rated voltage (3)		-	-	33 (4) 29 (5)	V_{DC}
BV	Breakdown voltage	@+25°C	100	-	-	V_{DC}
ΔC_{RVDC}	DC Capacitance voltage variation	From 0V to RV_{DC}, @+25°C	-	-	-0.02	$\%/V_{DC}$
IR	Insulation resistance	@ RV_{DC}, +25°C, 120s	-	100	-	GΩ
ESR	Equivalent Series Resistance	@+25°C, shunt mode	-	250	-	mΩ
ESL	Equivalent Series Inductance	@+25°C, SRF shunt mode	-	20	-	pH
ESD	HBM stress (6)	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

(1): other tolerance available upon request
(2): without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic life time prediction at 100°C continuous operation
(5): 10 years of intrinsic life time prediction at 150°C continuous operation
(6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

For extended frequency range (up to 26GHz), see Ultra large band Wire bondable vertical Silicon Capacitor (UWSC).

Impedance characteristic of 10nF WLSC/WBSC in Shunt mode

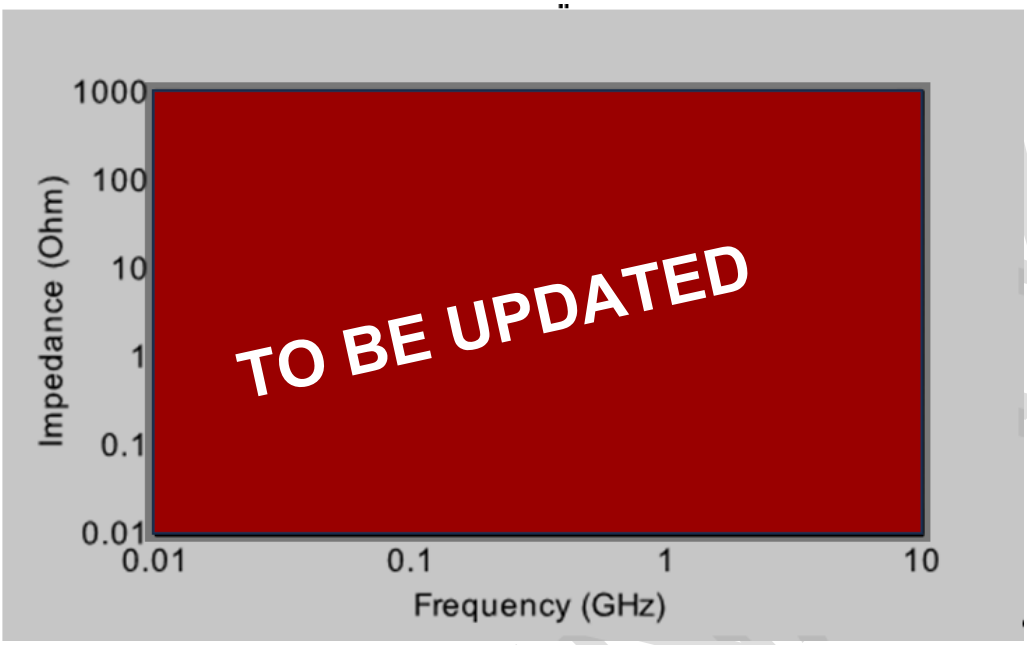

Figure 4 - 10nF WLSC/WBSC measurement results (Impedance characteristic

Schematic of 10nF WLSC/WBSC in Shunt mode

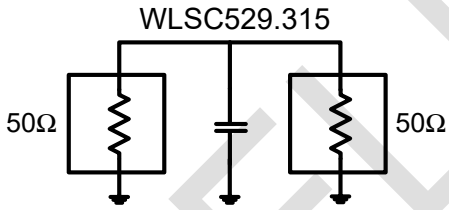

Figure 2 - 10nF WLSC/WBSC measurement schematic

Example of mounted 0303

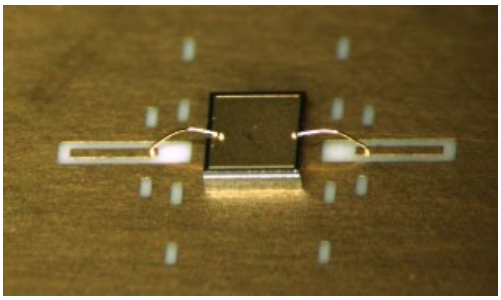

Figure 3 – micro picture of mounted 0303 WLSC

versus Frequency in shunt mode)

Pinning definition

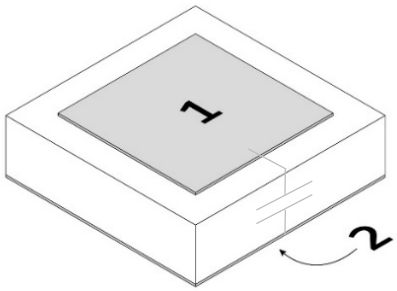

Figure 5 Pinning definition

pin #	Symbol	Metalization
1	Signal	TiWAu
2	GND	TiNiAu

Table 2 - Pining description.

Ordering Information

Murata Integrated Passive Devices delivers products with AQL level II (0.65). Tighter quality levels are available upon request.

Part number	Package			Die Name
	Packaging	Finishing	Description	
935142050510-F1T	6” FFC	Au (1)	WBSC 10nF/0303/BV>100V 1 bondpad 0.80 x 0.80mm x 0.25mm (2)	WK0303510
935142050510-F2T	8” FFC	Au (1)		
935142050510-T3T	T&R 1Kunits(3)	Au(1)		
935142050510-W0T	Waffle pack 400units	Au(1)		
935146050510-F1T	6” FFC	Au(1)	WLSC 10nF/0303/BV>100V 1 bondpad 0.80 x 0.80mm x 0.10mm (2)	WK0303510
935146050510-F2T	8” FFC	Au(1)		
935146050510-T3T	T&R 1Kunits(3)	Au(1)		
935146050510-W0T	Waffle pack 400units	Au(1)		

Table 3 - Packaging and ordering information

(1) detail for pad finishing: cf pad metallization chapter
(2) Refer to Package outline
(3) missing capacitors can reach 0.5% (only applicable to T&R)

Pad Metallization

This wire bondable capacitor is delivered as standard with the bottom electrode in TiNiAu ($_{Ti\ (0.1\ \mu m)/Ni\ (0.3\mu m)/Au\ (0.2\mu m)}$) and top electrode in TiWAu ($_{TiWAu\ (0.3\mu m)\ /\ Au\ (3\mu m)}$).

Other Metallization, such as thick Gold or Aluminum top pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a bare silicon die.

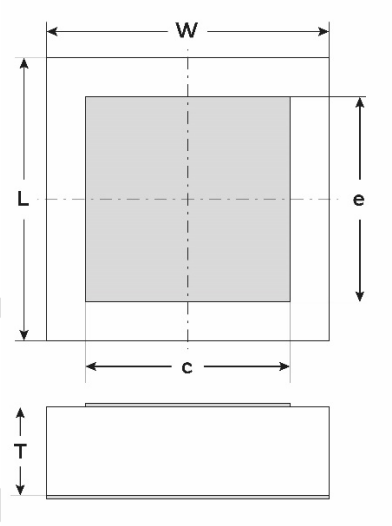

Figure 6 - Package outline drawing

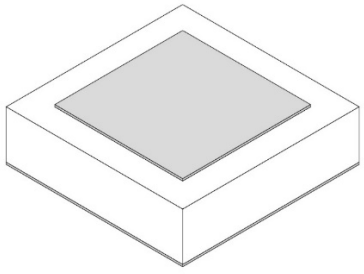

Figure 7 - Package isometric view

L (mm)	W (mm)	T (mm)	c (mm)	e (mm)
0.80 ±0.02	0.80 ±0.02	0.25 or 0.10 ±0.01	0.58	0.58

Table 4 - Dimensions and tolerances

Assembly

WBSC/WLSC capacitors are directly mounted on the PCB application using die bonding and wire bonding.

It is applicable for standard wire bonding assembly (ball and wedge).

For further information, please see our mounting application note.

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 8 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note ‘Products Storage Conditions and Shelf Life’.

Tape and Reel:

Die orientation (No flip) within the case related to T&R orientation).

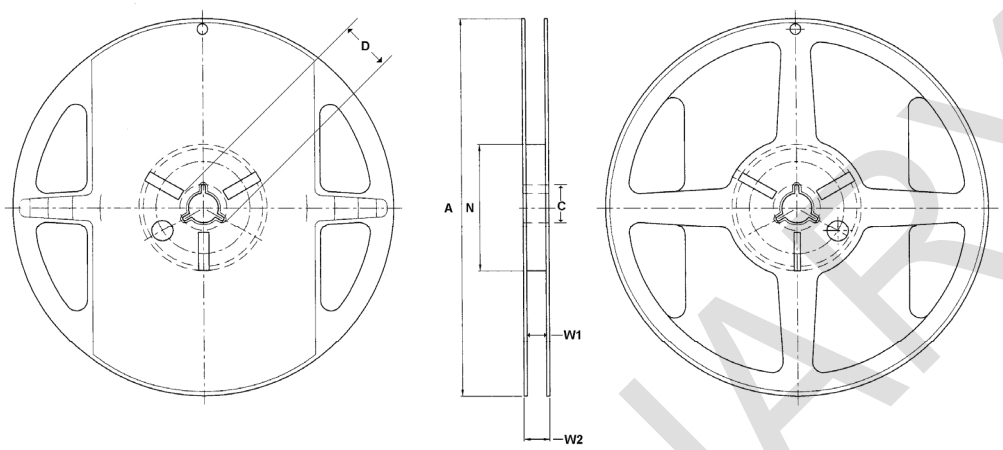

Figure 9 - Reel drawing

Tape Width	Diameter A	C	D	N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9.3	11.5

Table 5 – Reel dimensions (mm)

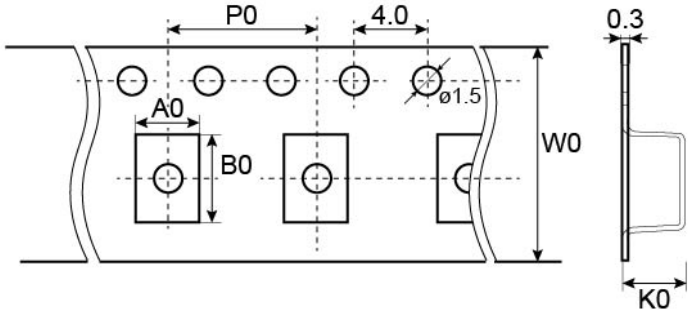

Figure 10 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Reel Capacity
Ao	Bo	Ko			
1.1	1.1	0.30	8 mm	4mm	1000

Table 6 - Tape dimensions (mm)

Film Frame Carrier:

With UV curable dicing tape (UV performed).

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

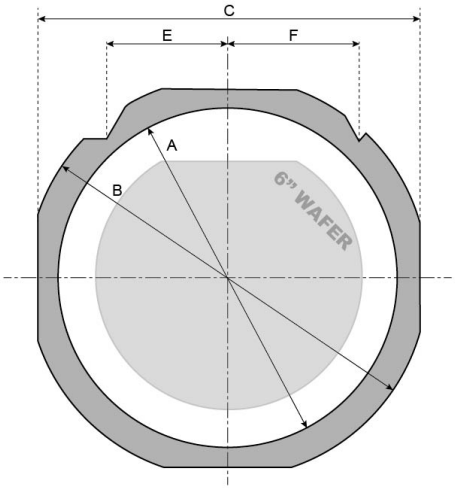

Figure 11 FF070 Frame with a 6" wafer

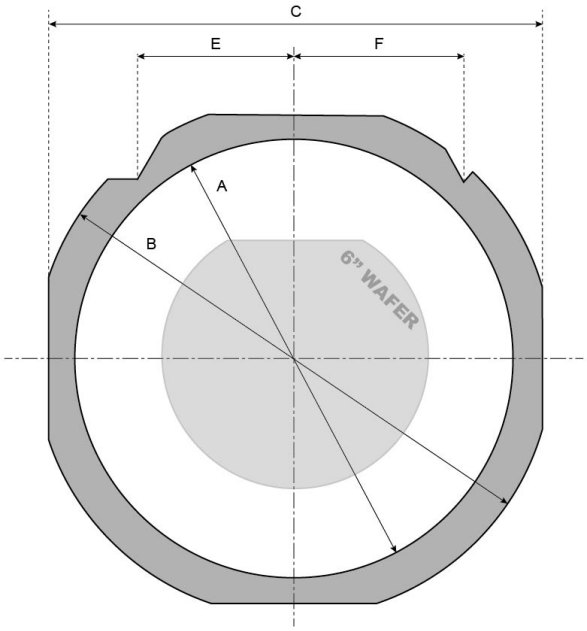

Figure 12 FF108 Frame with a 6" wafer

Frame Reference	Frame Style	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F
FF070 (1)	DTF-2-6-1	7.638”	8.976”	8.346”	0.048’’	2.370”	2.5’’
FF108 (1)	DTF-2-8-1	9.842”	11.653”	10.866”	0.048”	2.381”	2.5’’

Table 7 - Frame dimensions (inches)

(1) or equivalent

Expander grip ring 6” diameter:

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

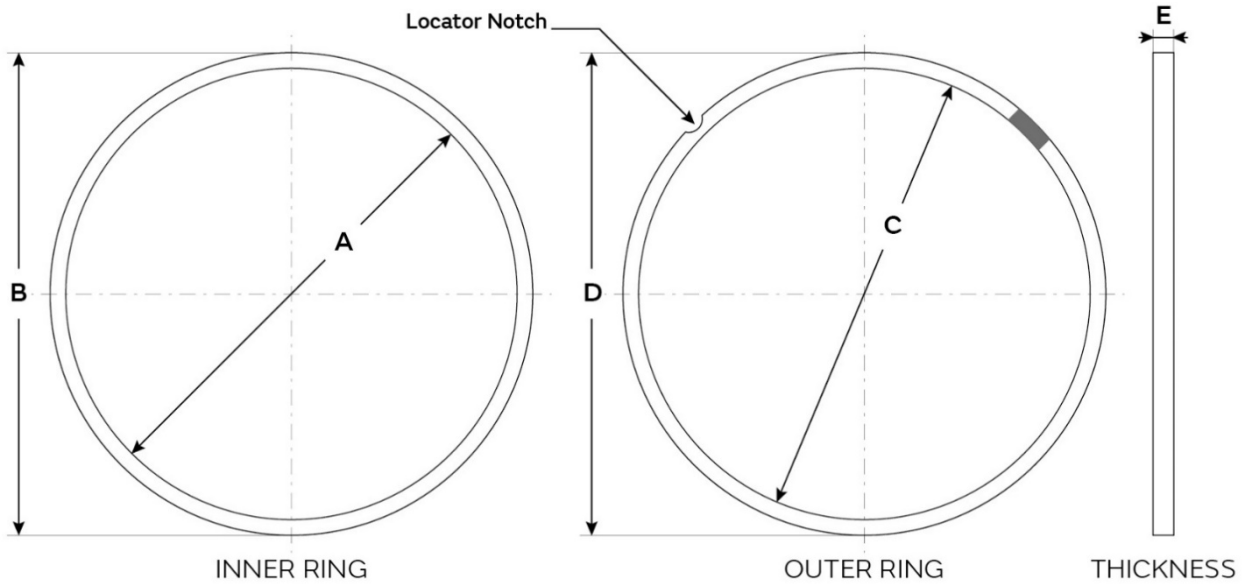

Figure 13 – Grip Ring drawing

Grip Ring Style	A	B	C	D	E	Locator Notch
GRP-2620-6 (1)	7.670”	7.973”	7.975”	8.280”	0.236”	None

Table 8 - Frame dimensions (inches)

(1) or equivalent

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information
Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
Rev 1.0	2018 January 09th	Objective specification	OGA
Rev 1.1	2018 April 06th	Update of specification	OGA
Rev 1.2	2018 June 28th	Update	OGA
Rev 1.3	2018 September 05th	Transfer FBC 0001	OGA
Rev 2.0	2020 March 10th	preliminary	SCA
Rev 2.01	2021, February 19th	Layout and content update	CGU /LLE/SCA/OGA

Disclaimer / Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.

www.murata.com
mis@murata.com