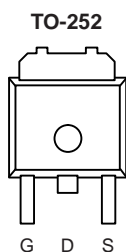


## N-Channel 650 V (D-S)MOSFET

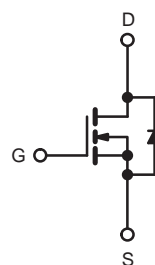
PRODUCT SUMMARY		
$V_{DS}$ (V)	650	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	3.8
$Q_g$ (Max.) (nC)	15	
$Q_{gs}$ (nC)	3	
$Q_{gd}$ (nC)	6	
Configuration	Single	

### FEATURES

- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Compliant to RoHS directive 2002/95/EC


 Available  
**RoHS**


Top View




N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	650	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current <sup>e</sup>	$V_{GS}$ at 10 V	$T_C = 25$ °C	A	
Continuous Drain Current		$T_C = 100$ °C		
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	8.0		
Linear Derating Factor		0.48	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	165	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	2	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	4	mJ	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	60	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>		$dV/dt$	2.8	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s		300	
Mounting Torque	6-32 or M3 screw		10	
			1.1	N · m

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25$  °C,  $L = 24$  mH,  $R_G = 25$   $\Omega$ ,  $I_{AS} = 3.2$  A (see fig. 12).
- $I_{SD} \leq 3.2$  A,  $dI/dt \leq 90$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.
- Drain current limited by maximum junction temperature.

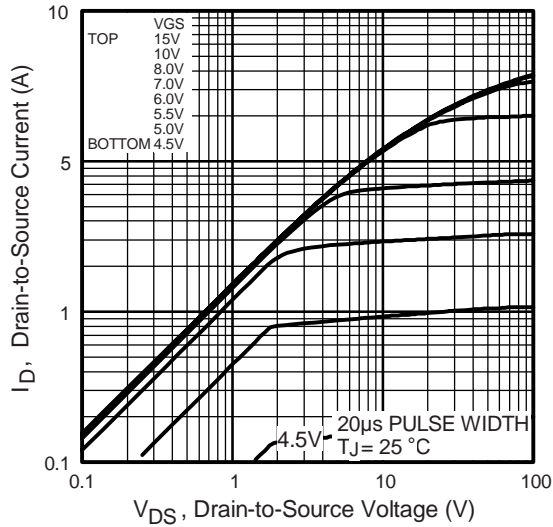
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	2.1	

SPECIFICATIONS $T_J = 25^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$		650	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25^\circ\text{C}$ , $I_D = 1\ \text{mA}^d$		-	670	-	mV/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\ \text{V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 650\ \text{V}, V_{GS} = 0\ \text{V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 520\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 125^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}$	$I_D = 3.1\ \text{A}^b$	-	3.8	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\ \text{V}, I_D = 3.1\ \text{A}$		3.9	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\ \text{V}, V_{DS} = 25\ \text{V}, f = 1.0\ \text{MHz}$ , see fig. 5		-	330	-	pF
Output Capacitance	$C_{oss}$			-	40	-	
Reverse Transfer Capacitance	$C_{rss}$			-	5.0	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\ \text{V}$	$V_{DS} = 1.0\ \text{V}, f = 1.0\ \text{MHz}$	-	912	-	pF
			$V_{DS} = 520\ \text{V}, f = 1.0\ \text{MHz}$	-	48	-	
Effective Output Capacitance	$C_{oss\ eff.}$	$V_{DS} = 0\ \text{V to } 520\ \text{V}^c$		-	84	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\ \text{V}$	$I_D = 3.2\ \text{A}, V_{DS} = 400\ \text{V}$ see fig. 6 and 13 <sup>b</sup>	-	-	15	nC
Gate-Source Charge	$Q_{gs}$			-	-	3	
Gate-Drain Charge	$Q_{gd}$			-	-	6	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 325\ \text{V}, I_D = 3.2\ \text{A}$ $R_G = 9.1\ \Omega, R_D = 62\ \Omega$ , see fig. 10 <sup>b</sup>		-	14	-	ns
Rise Time	$t_r$			-	20	-	
Turn-Off Delay Time	$t_{d(off)}$			-	34	-	
Fall Time	$t_f$			-	18	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	4	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	21	
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}, I_S = 3.2\ \text{A}, V_{GS} = 0\ \text{V}^b$		-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}, I_F = 3.2\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}^b$		-	493	739	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	2.1	3.2	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

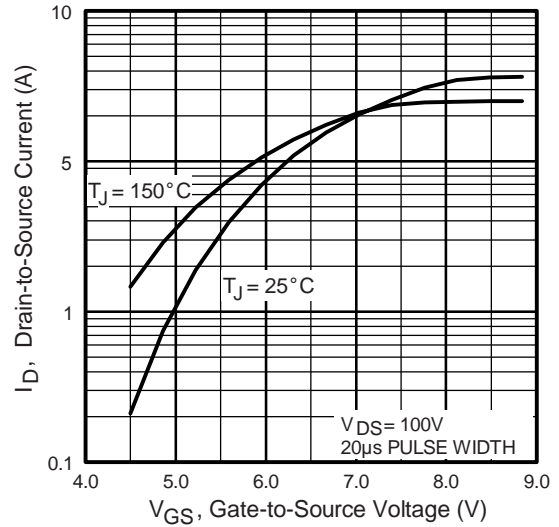
**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\ \mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\ eff.}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0% to 80%  $V_{DS}$ .
- $t = 60\ \text{s}, f = 60\ \text{Hz}$ .

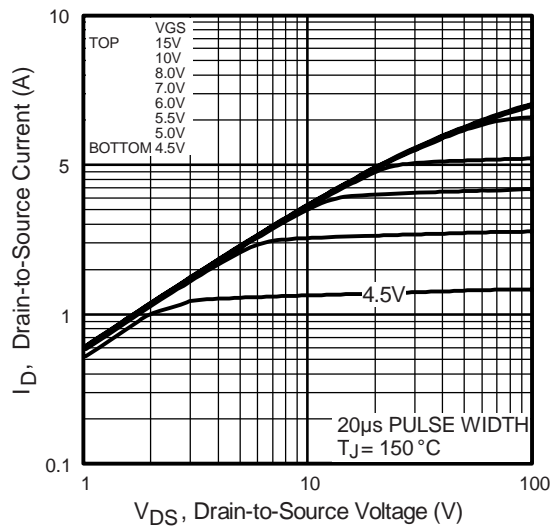
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



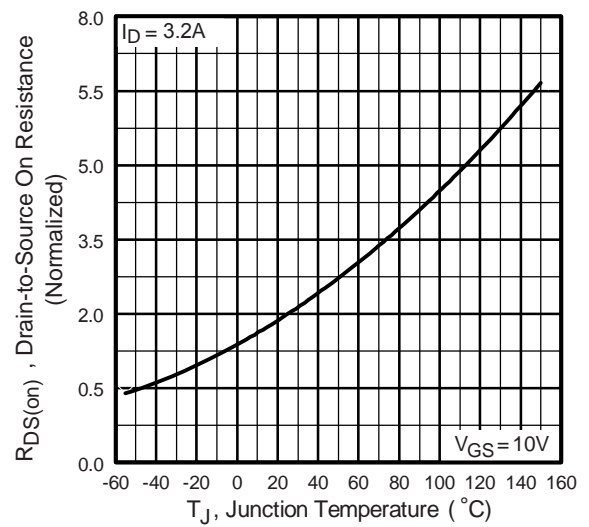
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

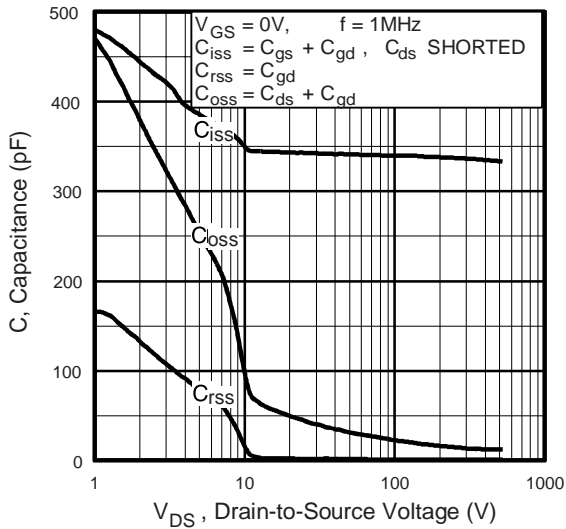


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage

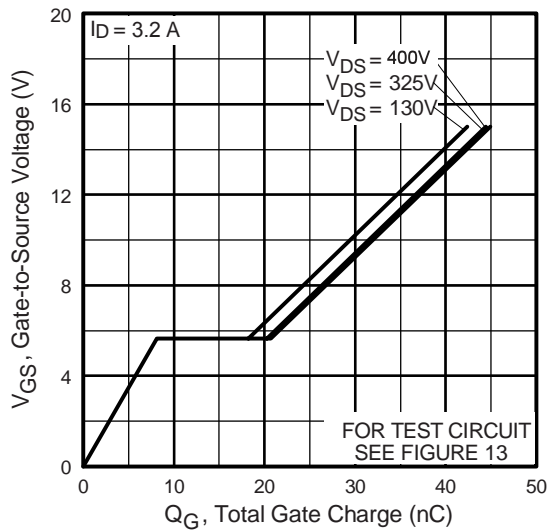


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

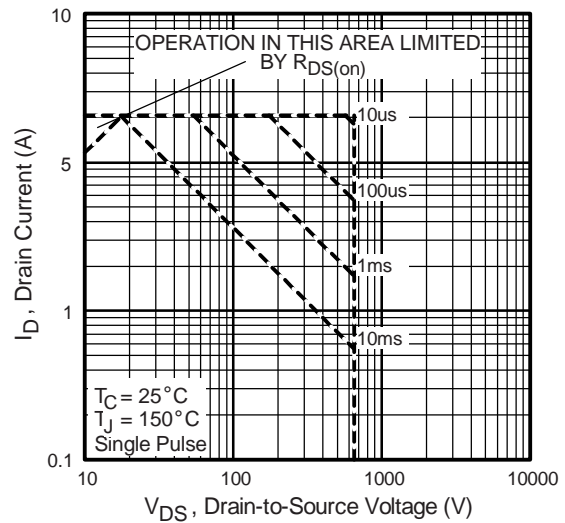


Fig. 8 - Maximum Safe Operating Area

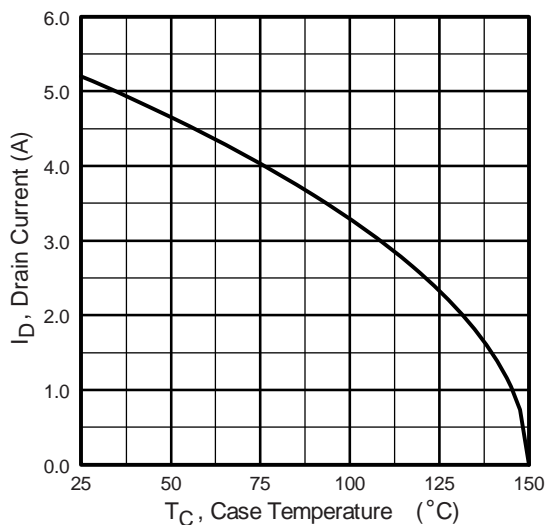


Fig. 9 - Maximum Drain Current vs. Case Temperature

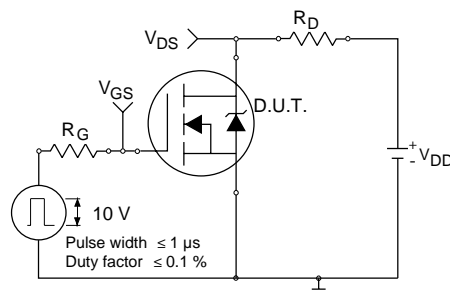


Fig. 10a - Switching Time Test Circuit

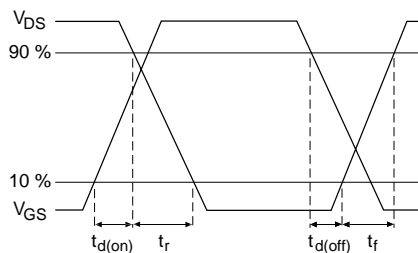


Fig. 10b - Switching Time Waveforms

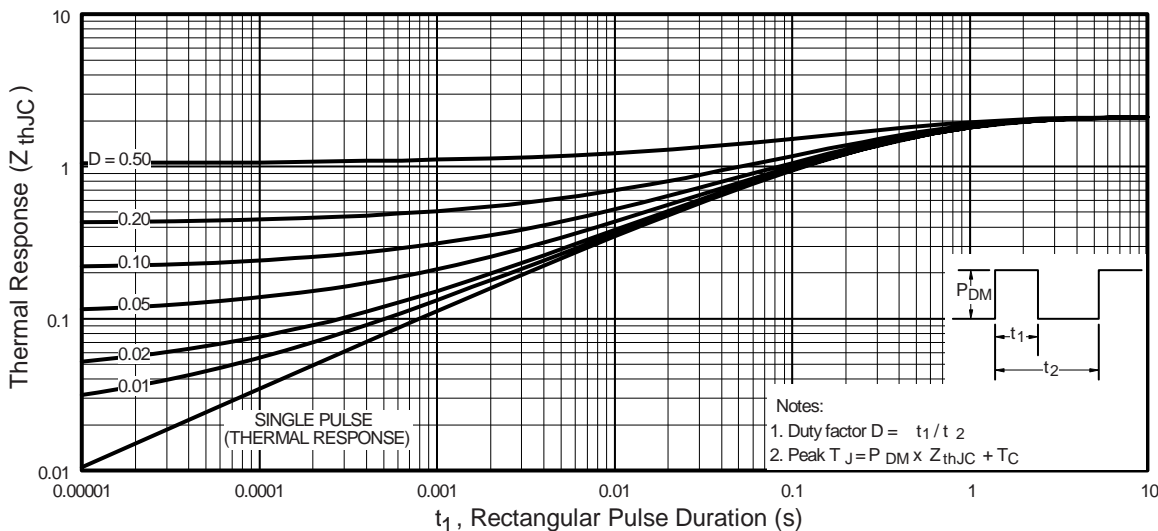


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

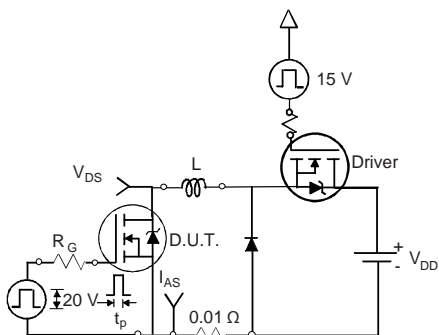


Fig. 12a - Unclamped Inductive Test Circuit

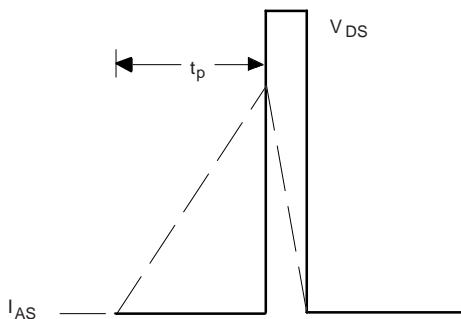


Fig. 12b - Unclamped Inductive Waveforms

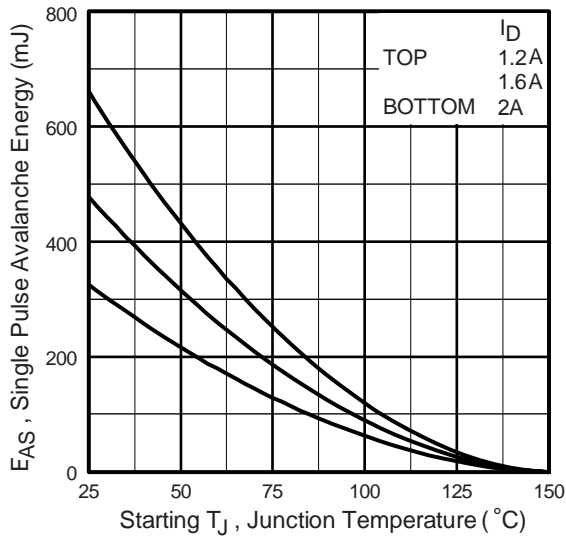


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

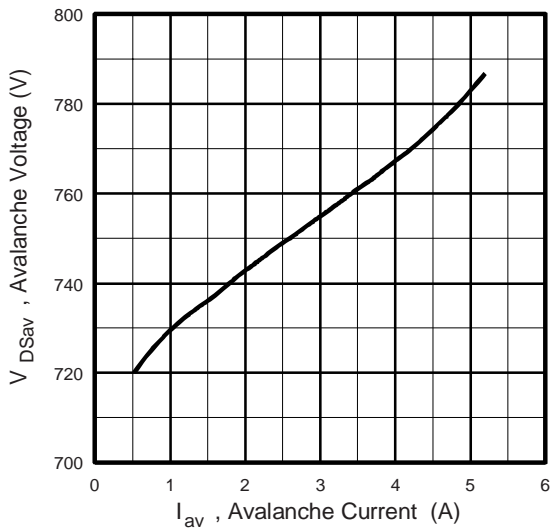


Fig. 12d - Typical Drain-to Source Voltage vs. Avalanche Current

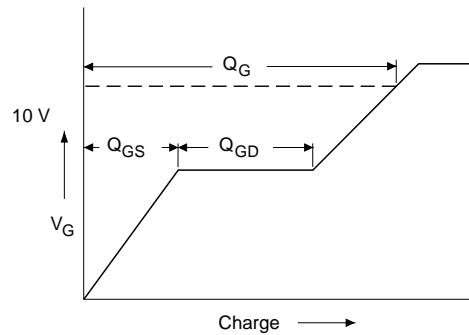


Fig. 13a - Basic Gate Charge Waveform

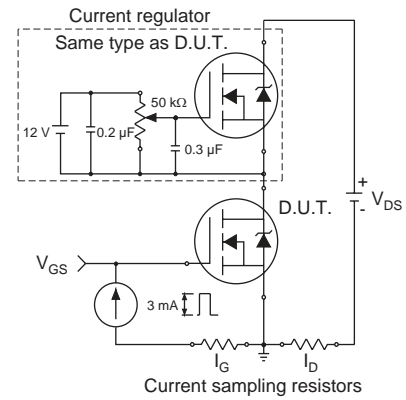
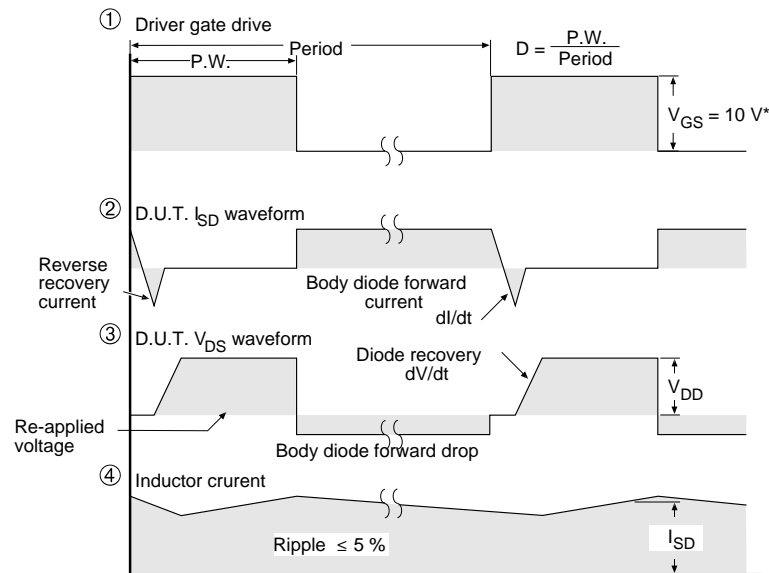
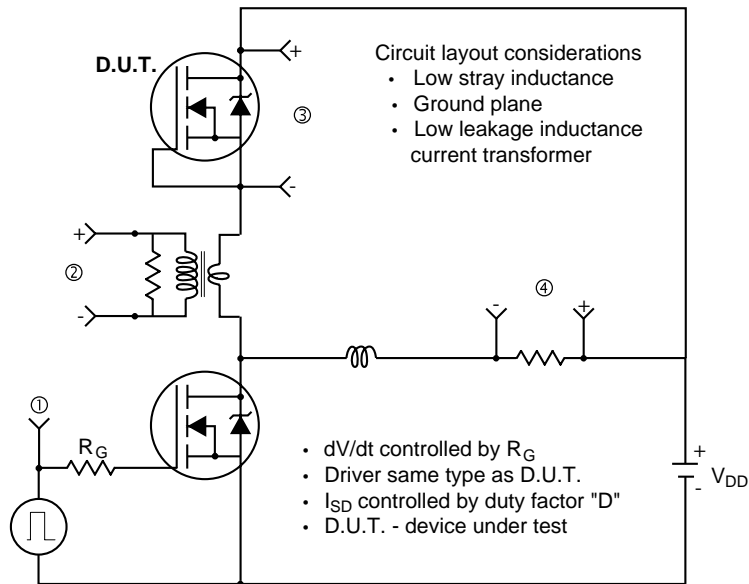


Fig. 13b - Gate Charge Test Circuit

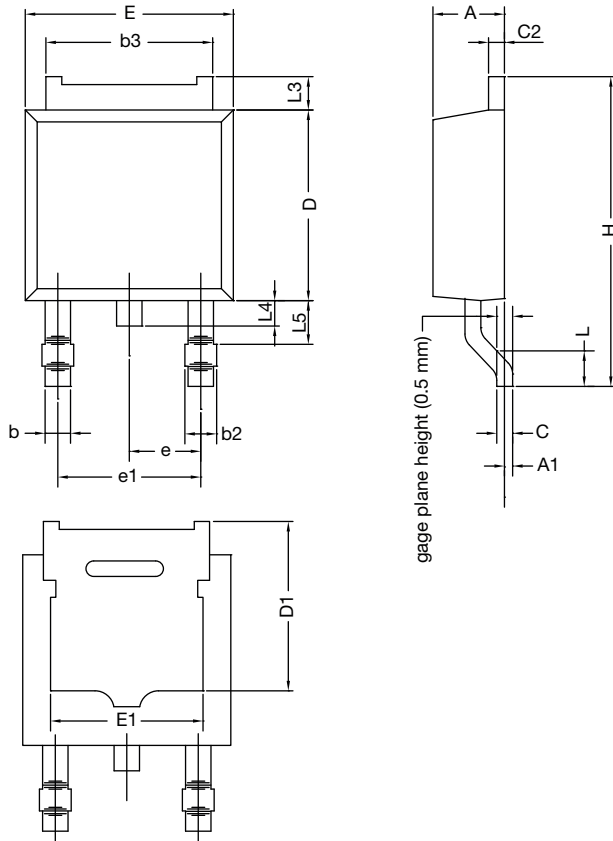
### Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5 V$  for logic level devices

Fig. 14 - For N-Channel

## TO-252AA CASE OUTLINE



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12 DWG: 5347				

**Note**

- Dimension L3 is for reference only.



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