LP8774x-Q1 Three Buck Converters and 5-V Boost for AWR and IWR Radar Sensors

1 Features

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
- Functional Safety -Compliant device
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 functional safety system design up to ASIL-C/ SIL-2
  - Input supply overvoltage and undervoltage monitoring
  - Regulator output overvoltage and undervoltage monitoring
  - Overvoltage and undervoltage monitoring for one external rail
  - Q&A Watchdog
  - Level or PWM error signal monitor (ESM)
  - BIST and CRC
- Input voltage: 3.3 V nominal (3 V to 4 V range)
- 3 high-efficiency step-down DC/DC converters:
  - Output voltage: 0.9 V to 1.9 V
  - Maximum output current: 3 A/ 3 A/ 3 A
  - Switching frequency: 4.4 MHz, 8.8 MHz, and 17.6 MHz
- 5 V boost converter
  - Maximum output current: 350 mA
- 150 mA LDO
  - Output voltage 1.8 V or 3.3 V
- Output short-circuit and overload protection
- Input overvoltage protection (OVP) and undervoltage lockout (UVLO)
- Overtemperature warning and protection
- Serial peripheral interface (SPI)

2 Applications

- Short range and medium range radar
- Ultra-short range radar
- Long range radar

3 Description

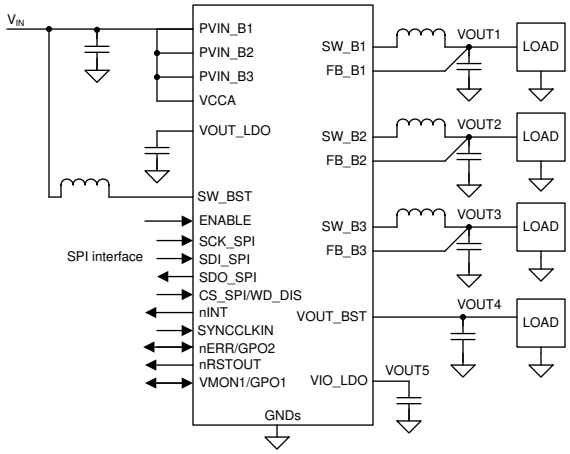
The LP8774x-Q1 device is designed to meet the power management requirements of the AWR and IWR MMICs in various automotive and industrial radar applications. The device has three step-down DC/DC converters, a 5 V boost converter and a 1.8 V/3.3 V LDO. The LDO is powered from the boost and intended for xWR IO supply. The device is controlled by an SPI serial interface and by enable signals.

The step-down DC/DC converters support programmable switching frequency of 4.4 MHz, 8.8 MHz, or 17.6 MHz. High switching frequency and low noise across wide frequency range enable LDO-free power solution with minimal or no passive filtering. This improves thermals and transient settling for the MMIC RF rails. The switching clock is forced to PWM mode for optimal RF performance and can also be synchronized to an external clock. The LP8774x-Q1 device supports remote voltage sensing to compensate IR drop between the regulator output and the point-of-load (POL) which improves the accuracy of the output voltage.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
LP8774x-Q1	VQFN-HR (28)	4.50 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Description (continued)....3
6 Pin Configuration and Functions....4
7 Device and Documentation Support....6
7.1 Receiving Notification of Documentation Updates....6
7.2 Support Resources....6
7.3 Trademarks....6
7.4 Electrostatic Discharge Caution....6
7.5 Glossary....6
8 Mechanical, Packaging, and Orderable Information....6
8.1 Packaging Option Addendum....7
8.2 Tape and Reel Information....8

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2021	*	Initial Release

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5 Description (continued)

The LP8774x-Q1 device supports programmable start-up and shutdown delays and sequences which are synchronized to the ENABLE signal. The sequences can also include GPO signals to control external regulators, load switches, and processor reset. The default settings for the device are programmed into nonvolatile memory (NVM). The device controls the output slew rate to minimize output voltage overshoot and in-rush current during device start-up.

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6 Pin Configuration and Functions

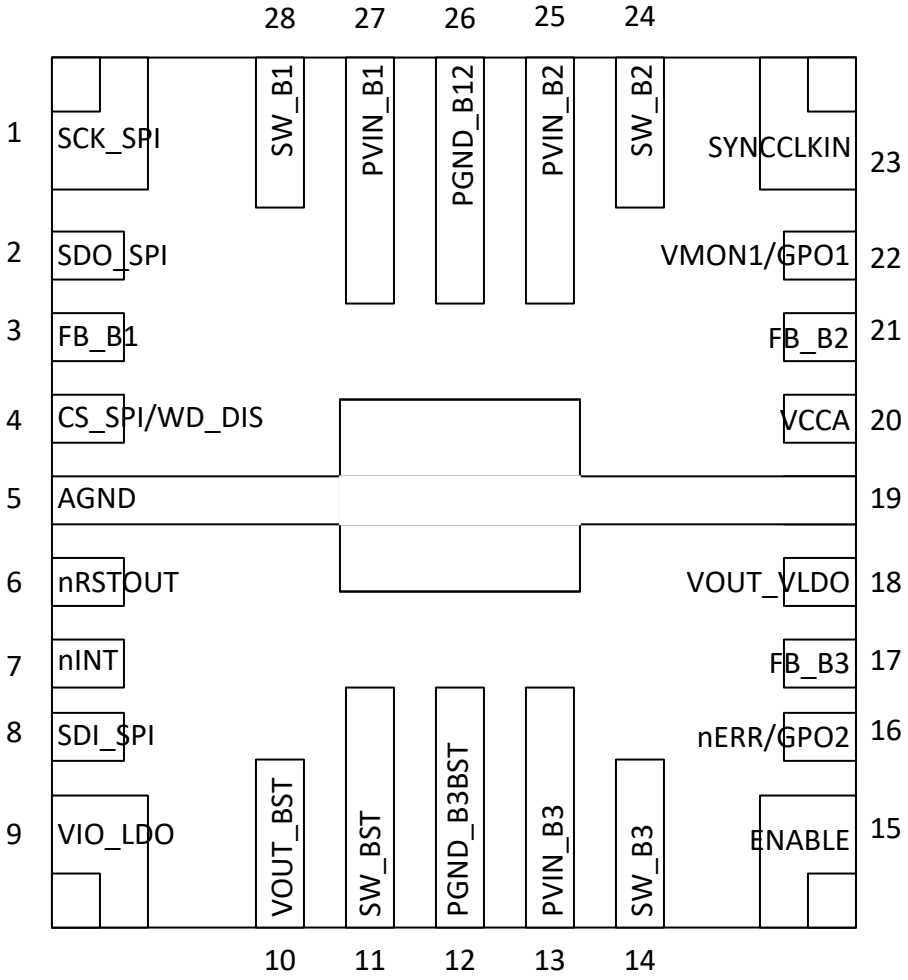


Figure 6-1. Package 28-Pin VQFN-HR Top View

Table 6-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
1	SCK_SPI	I	Digital	Clock signal for SPI interface.	Ground
2	SDO_SPI	O	Digital	Output data signal for SPI interface.	Floating
3	FB_B1	—	Analog	Output voltage feedback (positive) for BUCK1.	Ground
4	CS_SPI/ WD_DIS	I	Digital	Primary function: Chip select signal for SPI interface.	Ground
		I	Digital	Alternative programmable function: Watchdog Disable Input.	Not applicable
5	AGND	—	Ground	Ground.	Ground
6	NRSTOUT	O	Digital	Reset output.	Floating
7	nINT	O	Digital	Interrupt output and CAN PHY control or both.	Floating
8	SDI_SPI	I	Digital	Input data signal for SPI interface.	Ground
9	VIO_LDO	—	Analog	IO supply from the internal LDO or from external source. LDO enabled: regulator filter node. LDO disabled: input for connecting to an external IO supply source, with input filtering capacitor placed.	Not applicable
10	VOUT_BST	—	Analog	BOOST enabled: BOOST output (internally connected as VIO_LDO input). BOOST disabled and VIO_LDO disabled: short with VIO_LDO. BOOST disabled and VIO_LDO enabled: input for connecting to an external supply used as VIO_LDO input.	External supply

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Table 6-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
11	SW_BST	—	Analog	BOOST enabled: BOOST input. BOOST disabled: short with VOUT_BST.	Ground
12	PGND_B3BST	—	Ground	Power ground for BUCK3 and BOOST.	Ground
13	PVIN_B3	—	Power	Power input for BUCK3. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
14	SW_B3	—	Analog	BUCK3 switch node.	Floating
15	ENABLE	I	Digital	Programmable ENABLE signal.	Not applicable
16	nERR/GPO2	I	Digital	Primary function: System MCU Error Monitoring Input.	Ground
		O	Digital	Alternative programmable function: General Purpose Output signal (GPO2).	Floating
		O	Digital	Alternative programmable function: Fault Communication Output signal (FAULT2).	Floating
17	FB_B3	—	Analog	Output voltage feedback (positive) for BUCK3.	Ground
18	VOUT_LDO	—	Power	LDO regulator filter node. LDO is used for internal purposes.	-
19	AGND	—	Ground	Ground.	Ground
20	VCCA	—	Power	Supply voltage for internal LDO. VCCA and PVIN_Bxx pins must be connected together in the application and be locally bypassed.	System supply
21	FB_B2	—	Analog	Output voltage feedback (positive) for BUCK2.	Ground
22	VMON1/ GPO1	—	Analog	Voltage monitoring input.	Ground
		O	Digital	Alternative programmable function: General Purpose Output signal (GPO1).	Floating
		O	Digital	Alternative programmable function: Fault Communication Output signal (FAULT1).	Floating
		O	Digital	Alternative programmable function: CAN PHY control (CAN_DIS).	Floating
23	SYNCCLKIN	I	Digital	External clock input.	Ground
24	SW_B2	—	Analog	BUCK2 switch node.	Floating
25	PVIN_B2	—	Power	Power input for BUCK2. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
26	PGND_B12	—	Ground	Power ground for BUCK1 and BUCK2.	Ground
27	PVIN_B1	—	Power	Power input for BUCK1. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
28	SW_B1	—	Analog	BUCK1 switch node.	Floating

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7 Device and Documentation Support

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

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8.1 Packaging Option Addendum

Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
P877451A1RXVRQ1	PREVIEW	VQFN-HR	RXV	28	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-UNLIM	-40 to 125	P8774Q1 P8774RXVRQ1

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

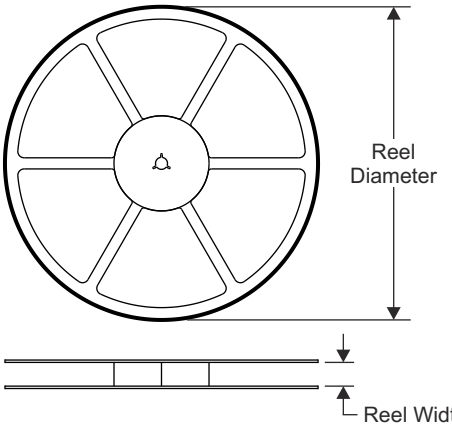
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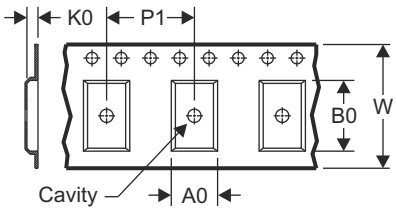
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8.2 Tape and Reel Information

REEL DIMENSIONS

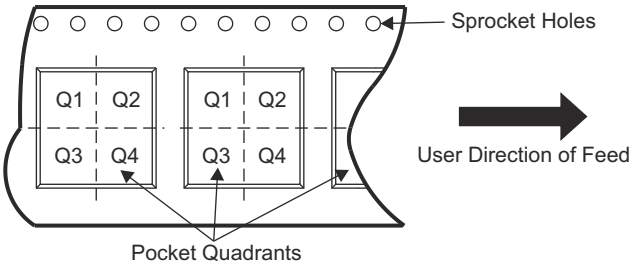


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

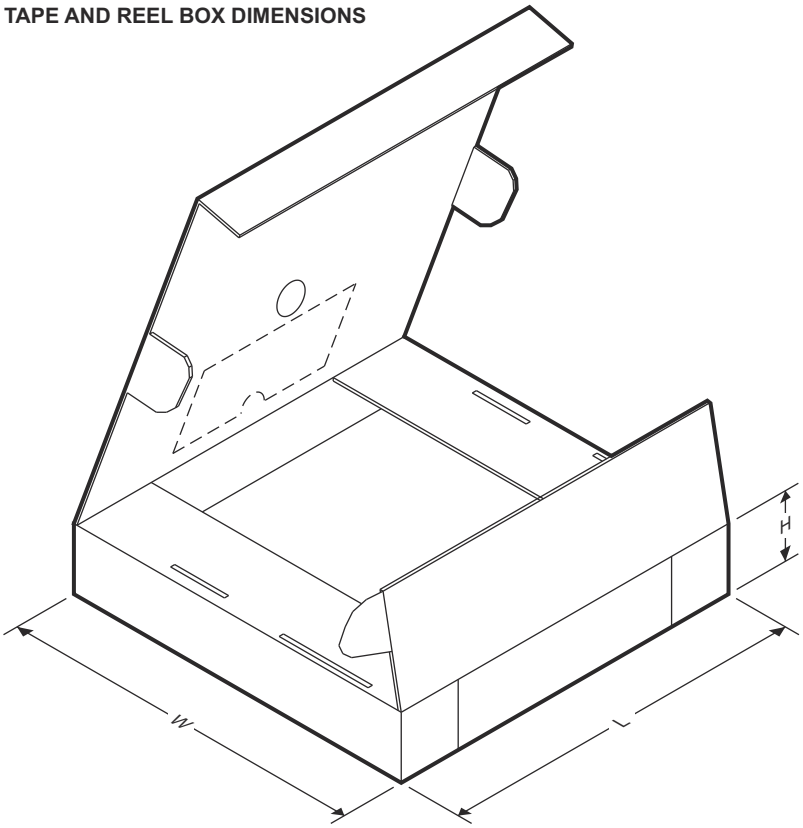


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
P877451A1RXVRQ1	VQFN-HR	RXV	28	3000	330	12.4	4.80	5.30	1.10	8.0	12.0	Q1

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
P877451A1RXVRQ1	VQFN-HR	RXV	28	3000	367	367	38

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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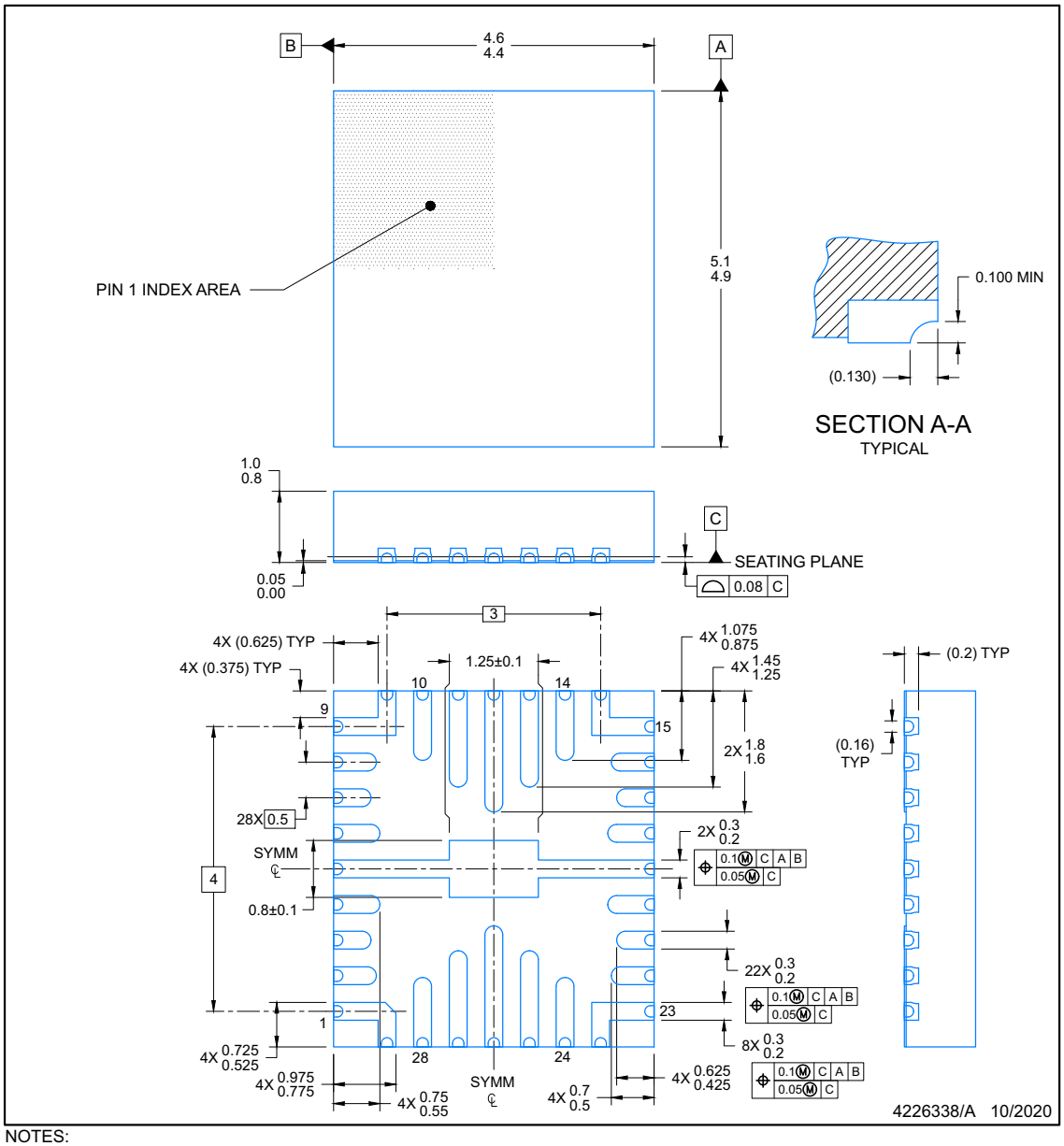
ADVANCE INFORMATION

PACKAGE OUTLINE

RXV0028A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

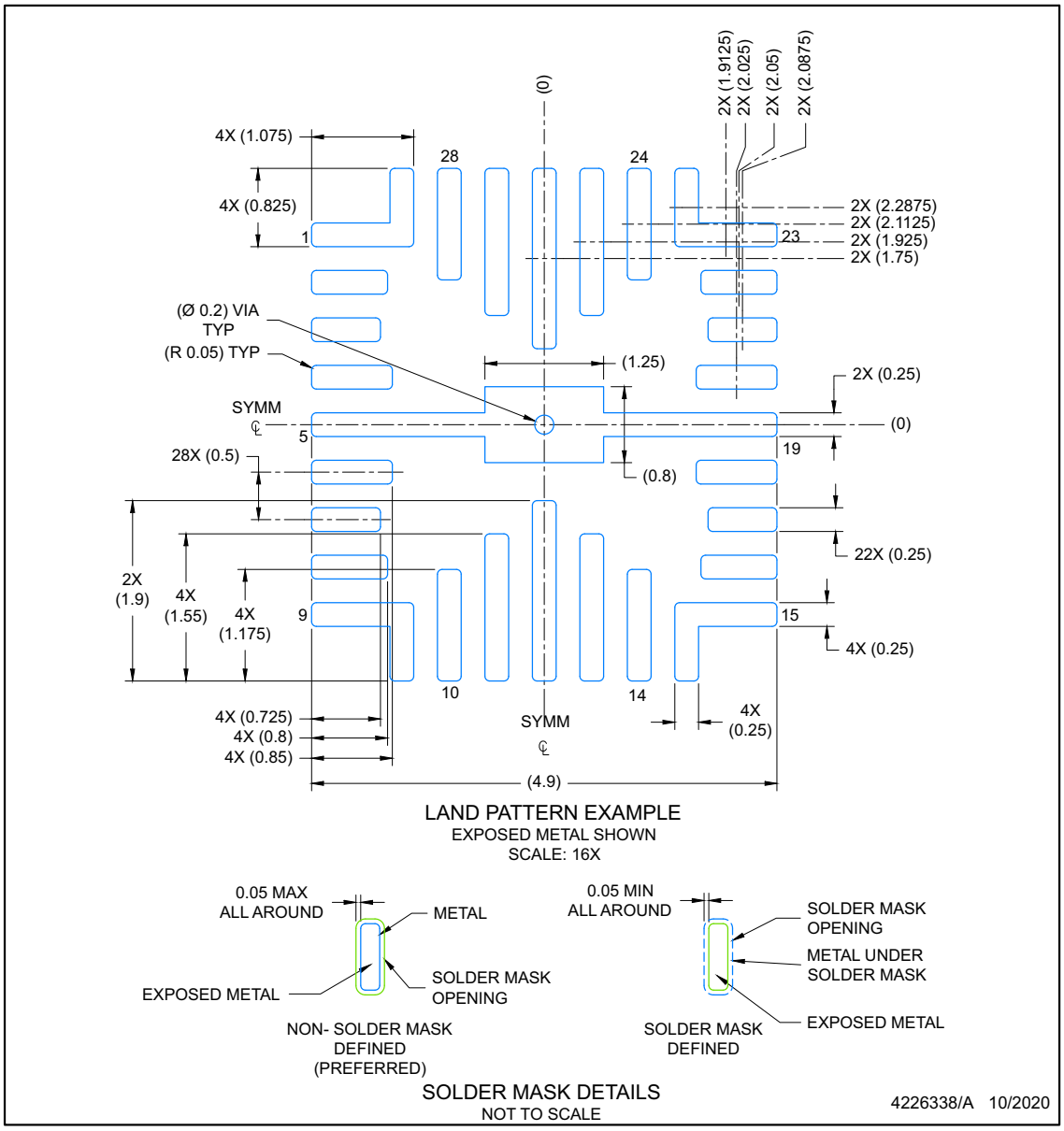
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EXAMPLE BOARD LAYOUT

RXV0028A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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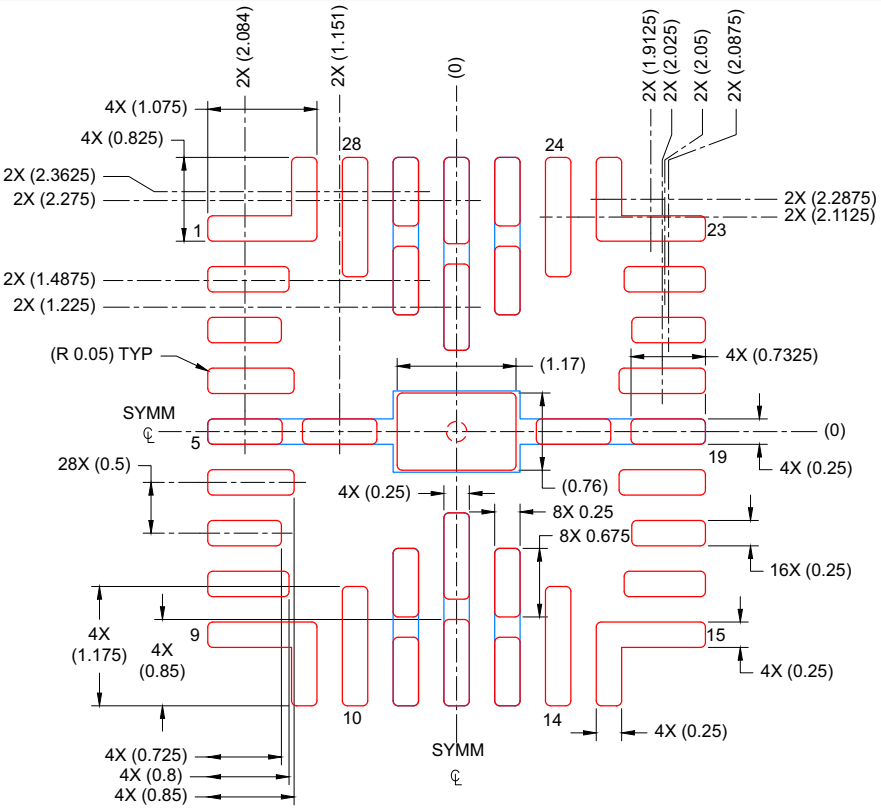
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ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RXV0028A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
FUSED PAD 5&19: 84%
PADS 11, 13, 25 & 27: 86%
PADS 12 & 26: 89%
SCALE: 16X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

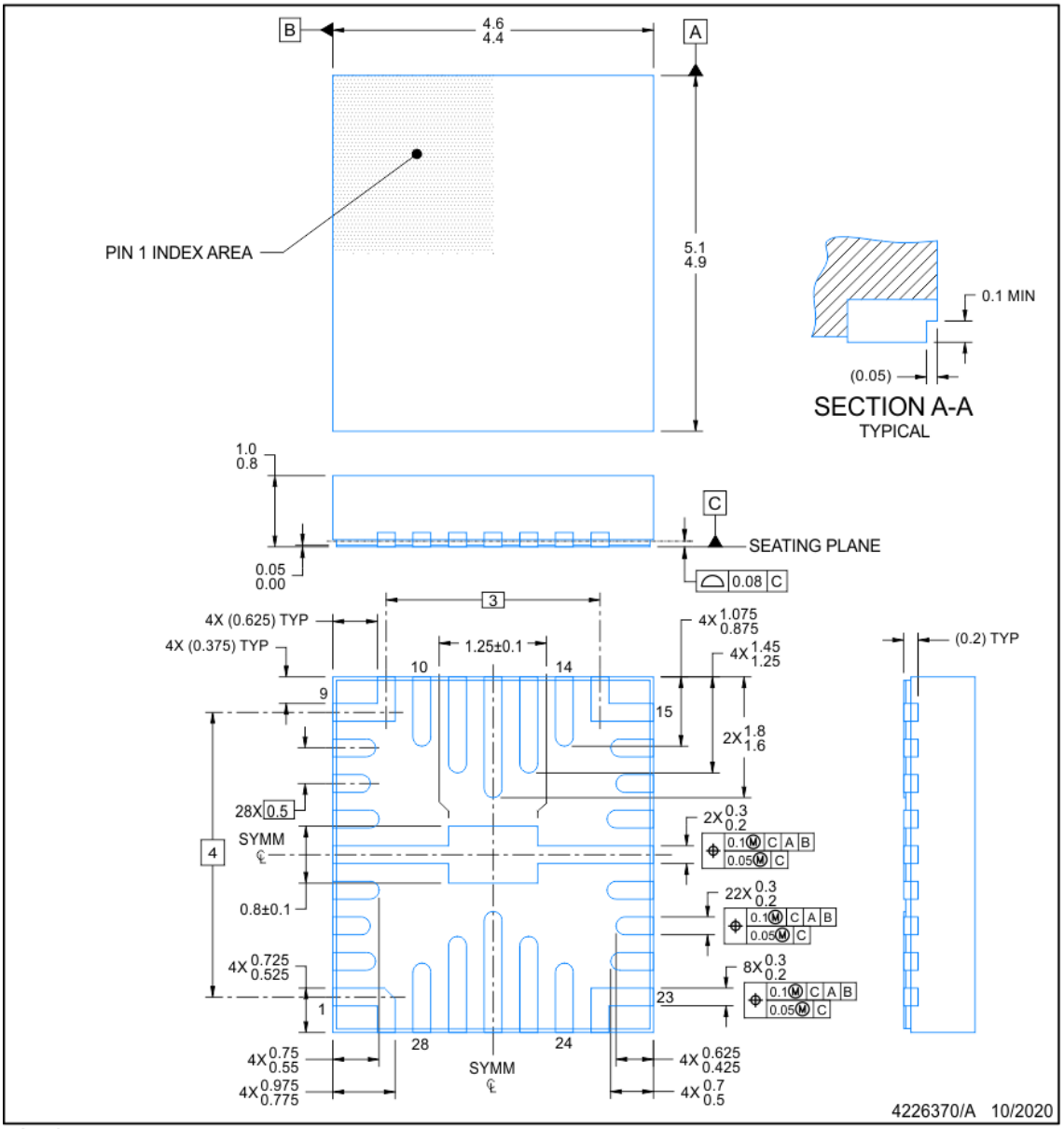
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PACKAGE OUTLINE

RXV0028B

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

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2. This drawing is subject to change without notice.

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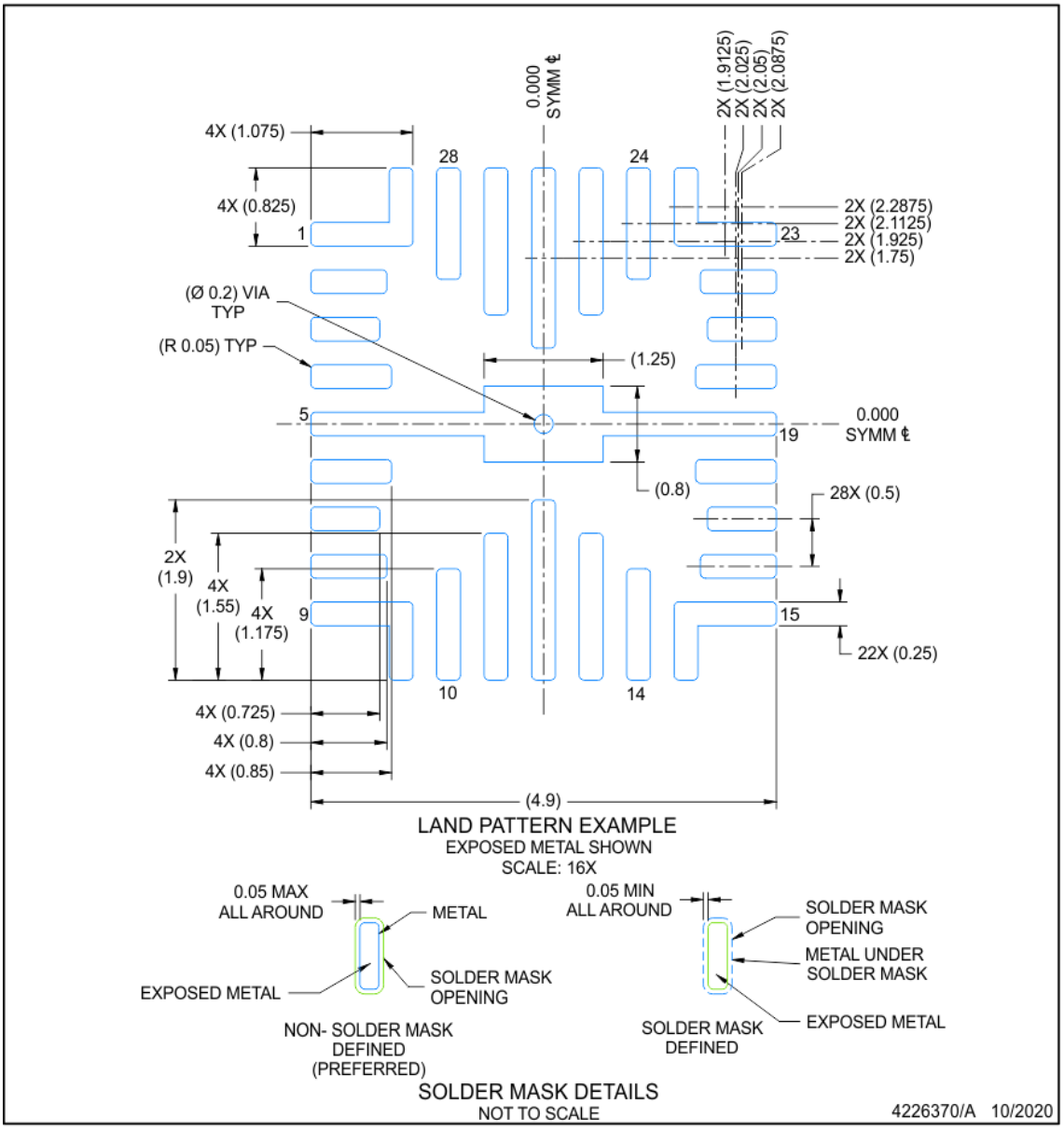
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ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RXV0028B — VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
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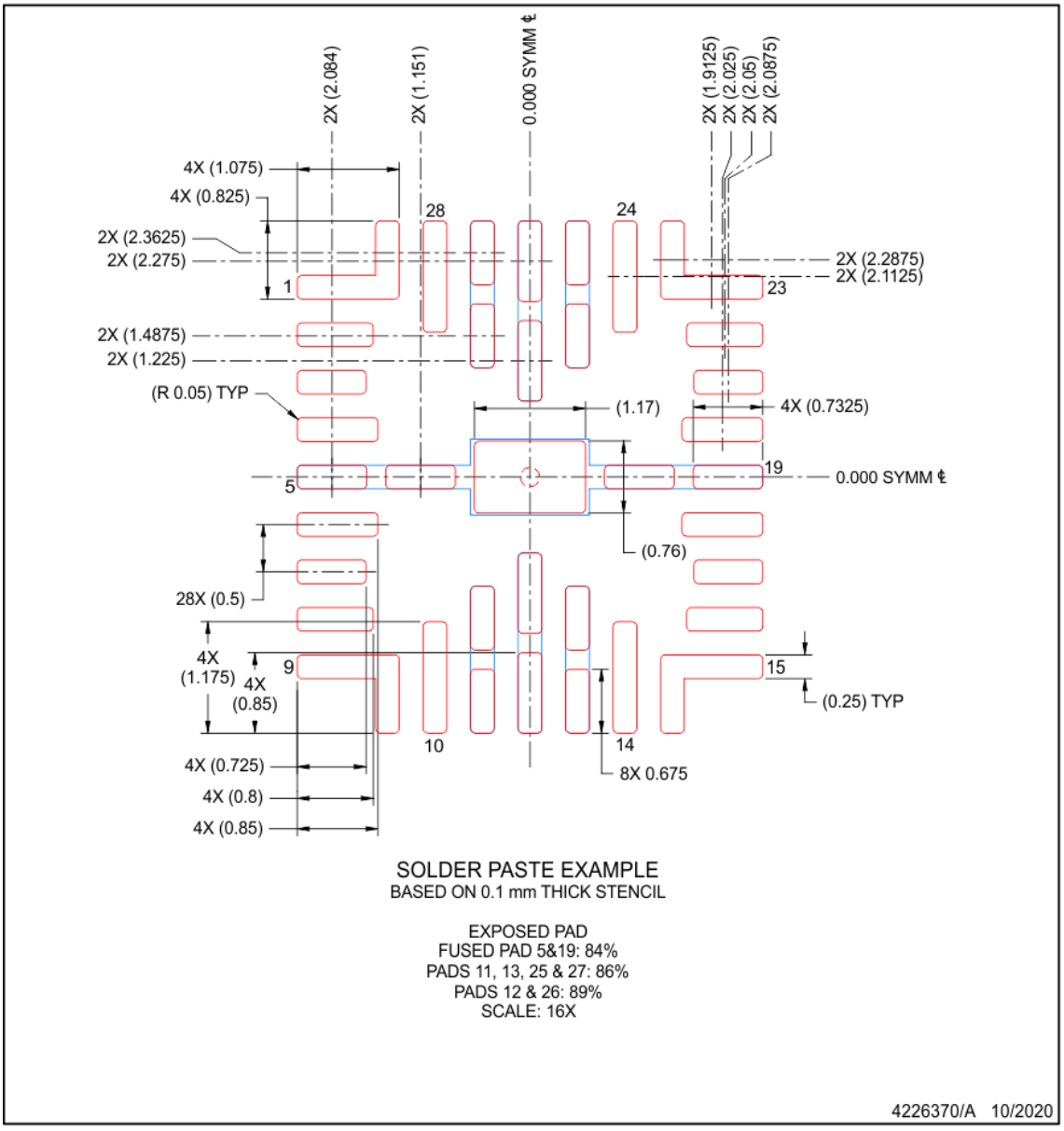
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EXAMPLE STENCIL DESIGN

RXV0028B

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
FUSED PAD 5&19: 84%
PADS 11, 13, 25 & 27: 86%
PADS 12 & 26: 89%
SCALE: 16X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
P877451A1RXVRQ1	ACTIVE	VQFN-HR	RXV	28	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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