# AM572x Sitara™ Processors
# Silicon Revision 2.0

## 1 Device Overview

### 1.1 Features

- Dual Arm® Cortex®-A15 microprocessor subsystem
- Up to 2 C66x floating-point VLIW DSP
  - Fully object-code compatible with C67x and C64x+
  - Up to thirty-two 16 × 16-bit fixed-point multiplies per cycle
- Up to 2.5MB of on-chip L3 RAM
- Two DDR3/DDR3L memory interface (EMIF) modules
  - Supports up to DDR3-1066
  - Up to 2GB supported per EMIF
- 2x dual Arm® Cortex®-M4 co-processors (IPU1 and IPU2)
- Up to four Embedded Vision Engines (EVEs)
- IVA-HD subsystem
  - 4K @ 15fps encode and decode support for H.264 CODEC
  - Other CODECs are up to 1080p60
- Display subsystem
  - Full-HD video (1920 × 1080p, 60 fps)
  - Multiple video input and video output
  - 2D and 3D graphics
  - Display controller with DMA engine and up to three pipelines
  - HDMI® encoder: HDMI 1.4a and DVI 1.0 compliant
- 2x dual-core Programmable Real-Time Unit and Industrial Communication SubSystem (PRU-ICSS)
- 2D-graphics accelerator (BB2D) subsystem
  - Vivante® GC320 core
- Video Processing Engine (VPE)
- Dual-core PowerVR® SGX544™ 3D GPU
- Crypto hardware accelerators
  - AES, SHA, RNG, DES and 3DES
- Three video Input Port (VIP) modules
- General-Purpose Memory Controller (GPMC)
- Enhanced Direct Memory Access (EDMA) controller
- 2-port gigabit ethernet (GMAC)
- Sixteen 32-bit general-purpose timers
- 32-bit MPU watchdog timer
- Five Inter-Integrated Circuit ( $I^2C$™) ports
- HDQ™/ 1-Wire® interface
- Ten configurable UART/IrDA/CIR modules
- Four Multichannel Serial Peripheral Interfaces (McSPI)
- Quad SPI interface (QSPI)
- SATA gen2 interface
- Eight Multichannel Audio Serial Port (McASP) modules
- SuperSpeed USB 3.0 dual-role device
- High-speed USB 2.0 dual-role device
- Four Multimedia Card/Secure Digital/Secure Digital Input Output interfaces ( MMC™/ SD®/SDIO)
- PCI-Express® 3.0 subsystems with two 5-Gbps lanes
  - One 2-lane gen2-compliant port
  - or two 1-lane gen2-compliant ports
- Dual Controller Area Network (DCAN) modules
  - CAN 2.0B protocol
- Up to 247 General-Purpose I/O (GPIO) pins
- Power, Reset, and Clock Management (PRCM)
- On-chip debug with CTools technology
- 28-nm CMOS technology
- 23 mm × 23 mm, 0.8-mm pitch, 760-pin BGA (ABC)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## 1.2 Applications

- Industrial communication
- Human Machine Interface (HMI)
- Automation and control
- High performance applications
- Analytics
- Other general use

## 1.3 Description

AM572x Sitara™ processors are Arm applications processors built to meet the intense processing needs of modern embedded products.

AM572x devices bring high processing performance through the maximum flexibility of a fully integrated mixed processor solution. The devices also combine programmable video processing with a highly integrated peripheral set. Cryptographic acceleration is available in every AM572x device.

Programmability is provided by dual-core Arm® Cortex®-A15 RISC CPUs with Arm® Neon™ extension, and two TI C66x VLIW floating-point DSP core, and Vision AccelerationPac (with 4x EVEs). The Arm allows developers to keep control functions separate from other algorithms programmed on the DSPs and coprocessors, thus reducing the complexity of the system software.

Additionally, TI provides a complete set of development tools for the Arm and C66x DSP, including C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a debugging interface for visibility into source code execution.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE |
|---|---|---|
| AM5729ABC | FCBGA (760) | 23.0 mm × 23.0 mm |
| AM5728ABC | FCBGA (760) | 23.0 mm × 23.0 mm |
| AM5726ABC | FCBGA (760) | 23.0 mm × 23.0 mm |

(1) For more information, see Section 10, *Mechanical, Packaging, and Orderable Information*.


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## 1.4 Functional Block Diagram

Figure 1-1 is functional block diagram for the device.

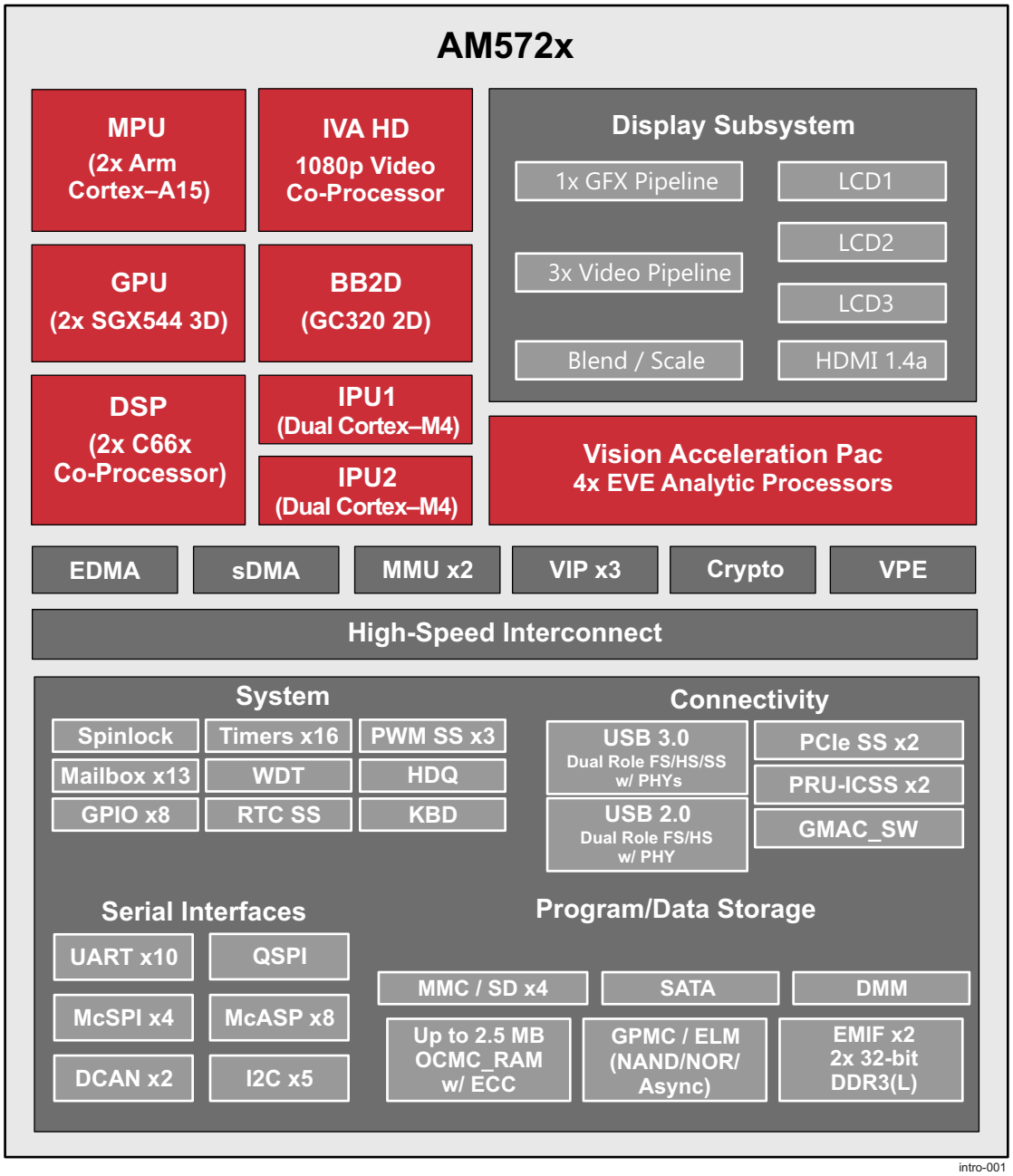


**Figure 1-1. AM572x Block Diagram**

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## 2 Revision History

**Changes from October 16, 2018 to May 15, 2019 (from E Revision (October 2018) to F Revision)** **Page**

- Added "Analytics" to Section 1.2, *Applications* ..... 2
- Added AM5729 details in Device Information table ..... 2
- Added AM5729 details in Table 3-1, *Device Comparison* ..... 6
- Fixed type direction to “O” for mii1_txer and mii0_txer signals in Table 4-20, *GMAC Signal Descriptions* ..... 132
- Added AM5729 details in Table 5-5, Table 5-8 and Table 5-9 ..... 163
- Added MII_TXER timing to GMAC MII Timings section ..... 309
- Updated MDIO Timing Diagram and MDIO7 parameter values ..... 310
- Added note regarding DDR ECC solutions to Table 8-3, *Supported DDR3 Device Combinations* ..... 377
- Added clarifications about validated DDR topology in Section 8.2.2.15, *CK and ADDR_CTRL Topologies and Routing Definition* ..... 386
- Updated a note for cosmetic marks on the package ..... 404
- Added AM5729 details in Table 9-1 ..... 405

# 3 Device Comparison

Table 3-1 shows a comparison between AM572x devices, highlighting the differences. For a comparison of the full AM57xx family of devices, refer to Parametric Table.

**Table 3-1. Device Comparison**

| FEATURES | | | DEVICE | | |
|---|---|---|---|---|---|
| | | | AM5729 | AM5728 | AM5726 |
| **Features** | | | | | |
| CTRL_WKUP_STD_FUSE_DIE_ID_2[31:24] Base PN register bitfield value [5] | | | AM5729: 78 (0x4E) | AM5728: 59 (0x3B) | AM5726: 57 (0x39) |
| | | | AM5729- E: 62 (0x3E) | AM5728- E: 60 (0x3C) | AM5726- E: 58 (0x3A) |
| **Processors/ Accelerators** | | | | | |
| Speed Grades | | | | See Table 5-5 | |
| Dual Arm Cortex-A15 Microprocessor Subsystem (MPU) | | MPU core 0 | Yes | Yes | Yes |
| | | MPU core 1 | Yes | Yes | Yes |
| C66x VLIW DSP | | DSP1 | Yes | Yes | Yes |
| | | DSP2 | Yes | Yes | Yes |
| BitBLT 2D Hardware Acceleration Engine (BB2D) | | BB2D | Yes | Yes | Not Supported [1] |
| Display Subsystem | | VOUT1 | Yes | Yes | Not Supported [1] |
| | | VOUT2 | Yes | Yes | Not Supported [1] |
| | | VOUT3 | Yes | Yes | Not Supported [1] |
| | | HDMI | Yes | Yes | Not Supported [1] |
| Embedded Vision Engine (EVE) | | EVE1 | Yes[6] | Not Supported [1] | |
| | | EVE2 | Yes[6] | Not Supported [1] | |
| | | EVE3 | Yes[6] | Not Supported [1] | |
| | | EVE4 | Yes[6] | Not Supported [1] | |
| Dual Arm Cortex-M4 Image Processing Unit (IPU) | | IPU1 | Yes | Yes | Yes |
| | | IPU2 | Yes | Yes | Yes |
| Image Video Accelarator (IVA) | | IVA | Yes | Yes | Not Supported [1] |
| SGX544 Dual-Core 3D Graphics Processing Unit (GPU) | | GPU | Yes | Yes | Not Supported [1] |
| Video Input Port (VIP) | VIP1 | vin1a | Yes | Yes | Yes |
| | | vin1b | Yes | Yes | Yes |
| | | vin2a | Yes | Yes | Yes |
| | | vin2b | Yes | Yes | Yes |
| | VIP2 | vin3a | Yes | Yes | Yes |
| | | vin3b | Yes | Yes | Yes |
| | | vin4a | Yes | Yes | Yes |
| | | vin4b | Yes | Yes | Yes |
| | VIP3 | vin5a | Yes | Yes | Yes |
| | | vin6a | Yes | Yes | Yes |
| Video Processing Engine (VPE) | | VPE | Yes | Yes | Yes |
| **Program/Data Storage** | | | | | |
| On-Chip Shared Memory (RAM) | | OCMC_RAM | 2.5MB | 2.5MB | 2.5MB |
| General-Purpose Memory Controller (GPMC) | | GPMC | Yes | Yes | Yes |
| DDR3 Memory Controller [2] | | EMIF1 | up to 2GB | up to 2GB | up to 2GB |
| | | EMIF2 | up to 2GB | up to 2GB | up to 2GB |
| Dynamic Memory Manager (DMM) | | DMM | Yes | Yes | Yes |
| **Radio Support** | | | | | |


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**Table 3-1. Device Comparison (continued)**

| FEATURES | | DEVICE | | |
|---|---|---|---|---|
| | | AM5729 | AM5728 | AM5726 |
| Audio Tracking Logic (ATL) | ATL | Not Supported (1) | | |
| Viterbi Coprocessor (VCP) | VCP1 | Not Supported (1) | | |
| | VCP2 | Not Supported (1) | | |
| **Peripherals** | | | | |
| Dual Controller Area Network Interface (DCAN) | DCAN1 | Yes | Yes | Yes |
| | DCAN2 | Yes | Yes | Yes |
| Enhanced DMA (EDMA) | EDMA | Yes | Yes | Yes |
| System DMA (DMA_SYSTEM) | DMA_SYSTEM | Yes | Yes | Yes |
| Ethernet Subsystem (Ethernet SS) | GMAC_SW[0] | MII, RMII, or RGMII | MII, RMII, or RGMII | MII, RMII, or RGMII |
| | GMAC_SW[1] | MII, RMII, or RGMII | MII, RMII, or RGMII | MII, RMII, or RGMII |
| General-Purpose I/O (GPIO) | GPIO | up to 247 | up to 247 | up to 247 |
| Inter-Integrated Circuit Interface ($I^2C$) | I2C | 5 | 5 | 5 |
| System Mailbox Module | MAILBOX | 13 | 13 | 13 |
| Media Local Bus Subsystem (MLB) (3) | MLB | Not Supported (1) | | |
| Multichannel Audio Serial Port (McASP) | McASP1 | 16 serializers | 16 serializers | 16 serializers |
| | McASP2 | 16 serializers | 16 serializers | 16 serializers |
| | McASP3 | 4 serializers | 4 serializers | 4 serializers |
| | McASP4 | 4 serializers | 4 serializers | 4 serializers |
| | McASP5 | 4 serializers | 4 serializers | 4 serializers |
| | McASP6 | 4 serializers | 4 serializers | 4 serializers |
| | McASP7 | 4 serializers | 4 serializers | 4 serializers |
| | McASP8 | 4 serializers | 4 serializers | 4 serializers |
| MultiMedia Card/Secure Digital/Secure Digital Input Output Interface (MMC/SD/SDIO) | MMC1 | 1x UHSI 4b | 1x UHSI 4b | 1x UHSI 4b |
| | MMC2 | 1x eMMC™ 8b | 1x eMMC™ 8b | 1x eMMC 8b |
| | MMC3 | 1x SDIO 8b | 1x SDIO 8b | 1x SDIO 8b |
| | MMC4 | 1x SDIO 4b | 1x SDIO 4b | 1x SDIO 4b |
| PCI Express 3.0 Port with Integrated PHY | PCIe_SS1 | Yes | Yes | Yes |
| | PCIe_SS2 | Yes | Yes | Yes |
| 2x Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS) | PRU-ICSS1 | Yes | Yes | Yes |
| | PRU-ICSS2 | Yes | Yes | Yes |
| Serial Advanced Technology Attachment (SATA) | SATA | Yes | Yes | Yes |
| Real-Time Clock Subsystem (RTCSS) | RTCSS (4) | Yes | Yes | Yes |
| Multichannel Serial Peripheral Interface (McSPI) | McSPI | 4 | 4 | 4 |
| HDQ / 1-Wire (HDQ1W) | HDQ1W | Yes | Yes | Yes |
| Quad SPI (QSPI) | QSPI | Yes | Yes | Yes |
| Spinlock Module | SPINLOCK | Yes | Yes | Yes |
| Keyboard Controller (KBD) | KBD | Yes | Yes | Yes |
| Timers, General-Purpose | TIMER | 16 | 16 | 16 |
| Timer, Watchdog | WATCHDOG TIMER | Yes | Yes | Yes |
| Pulse-Width Modulation Subsystem (PWMSS) | PWMSS1 | Yes | Yes | Yes |
| | PWMSS2 | Yes | Yes | Yes |
| | PWMSS3 | Yes | Yes | Yes |
| Universal Asynchronous Receiver/Transmitter (UART) | UART | 10 | 10 | 10 |

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**Table 3-1. Device Comparison (continued)**

| FEATURES | | DEVICE | | |
|---|---|---|---|---|
| | | AM5729 | AM5728 | AM5726 |
| Universal Serial Bus (USB3.0) | USB1 (SuperSpeed, Dual-Role-Device [DRD]) | Yes | Yes | Yes |
| Universal Serial Bus (USB2.0) | USB2 (High-Speed, Dual-Role-Device [DRD], with embedded HS PHY) | Yes | Yes | Yes |
| | USB3 (High-Speed, OTG2.0, with ULPI) | Not Supported (1) | | |
| | USB4 (High-Speed, OTG2.0, with ULPI) | Not Supported (1) | | |

(1) Features noted as "not supported," must not be used. Their functionality is not supported by TI for this family of devices. These features are subject to removal without notice on future device revisions. Any information regarding the unsupported features has been retained in the documentation solely for the purpose of clarifying signal names or for consistency with previous feature descriptions.

(2) In the Unified L3 memory map, there is maximum of 2GB of SDRAM space which is available to all L3 initiators including MPU (MPU, GPU, DSP, IVA, DMA, etc). Typically this space is interleaved across both EMIFs to optimize memory performance. If a system populates > 2GB of physical memory, that additional addressable space can be accessed only by the MPU via the Arm V7 Large Physical Address Extensions (LPAE).

(3) MLB power rails (vdds_mlbp) must be connected to a 1.8V power supply even this feature is not supported.

(4) RTC only mode is not supported feature.

(5) For more details about the CTRL_WKUP_STD_FUSE_DIE_ID_2 register and Base PN bitfield, see the *AM572x Sitara™ Processors Silicon Revision 2.0, 1.1* (SPRUHZ6).

(6) The Embedded Vision Engine (EVE) consumes additional power when enabled. Therefore all designs using the AM5729 device must implement the TPS6590379ZWSR PMIC which provides a separate SMPS output for vdd_dspeve. Please refer to the *TPS659037 User's Guide to Power AM574x, AM572x, and AM571x* (SLIU011) for more information. Be sure to use the Power Estimation Tool (PET) to correctly size your system thermal solution.

## 3.1 Related Products

**Sitara Processors** Scalable processors based on Arm® Cortex®-A cores with flexible peripherals, connectivity & unified software support – perfect for sensors to servers.

**TI's Arm Cortex-A15 Advantage** The Arm Cortex-A15 processor is proven in a range of different markets and is an increasingly popular choice in networking infrastructure, delivering high-performance processing capability combined with low power consumption. The Cortex-A15 processor delivers roughly twice the performance of the Cortex-A9 processor and can achieve 3.5 DMIPS/MHz.

**Sitara Applications** Sitara™ processors provide scalable solutions for a wide range of applications from HMIs and gateways to more complex equipment such as drives and substation automation equipment. Sitara Arm® processors offer scalability and reliability as well as multi-protocol support for industrial communication protocols such as EtherCAT, Ethernet/IP and Profinet.

**Reference Designs** TI provides many reference designs containing 'building block' solutions to enable customers to rapidly development of their unique products and solutions.

**Companion Products for AM572x** Review products that are frequently purchased or used in conjunction with this product.


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# 4 Terminal Configuration and Functions

## 4.1 Terminal Assignment

Figure 4-1 shows the ball locations for the 760 plastic ball grid array (PBGA) package and are used in conjunction with Table 4-2 through Table 4-34 to locate signal names and ball grid numbers.

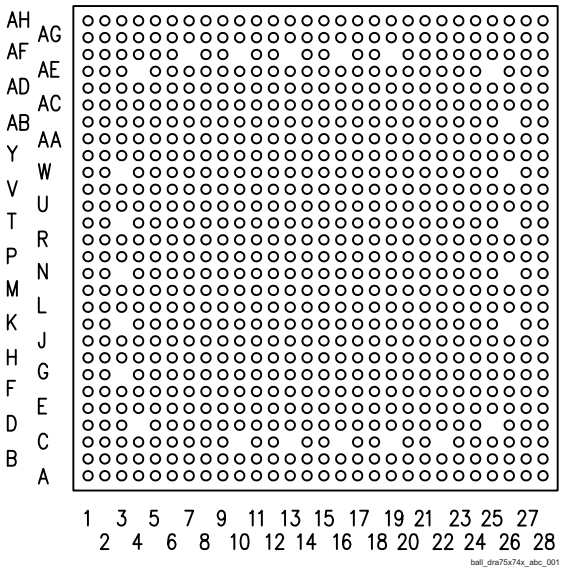


**Figure 4-1. ABC S-PBGA-N760 Package (Bottom View)**

**NOTE**

The following bottom balls are not connected: AF7 / AF10 / AF13 / AF16 / AF19 / AE4 / AE25 / AB26 / W3 / W26 / T3 / T26 / N3 / N26 / K3 / K26 / G3 / D4 / D25 / C10 / C13 / C16 / C19 / C22.

These balls do not exist on the package.

### *4.1.1 Unused Balls Connection Requirements*

This section describes the Unused/Reserved balls connection requirements.

**NOTE**

The following balls are reserved: Y5 / Y10 / K14 / B28 /A27

These balls must be left unconnected.

**NOTE**

All unused power supply balls must be supplied with the voltages specified in the Section 5.4, *Recommended Operating Conditions,* unless alternative tie-off options are included in Section 4.4, *Signal Descriptions*.

**Table 4-1. Unused Balls Specific Connection Requirements**

| BALLS | CONNECTION REQUIREMENTS |
|---|---|
| AE14 / AE15 / AD17 / AC15 / AC16 / AC17 / AB16 / V27 / D20 / AH25 / AE27 / AD27 / Y28 / G28 / H27 / K27 / M28 | These balls must be connected to GND through an external pull resistor if unused |

**Table 4-1. Unused Balls Specific Connection Requirements (continued)**

| BALLS | CONNECTION REQUIREMENTS |
|---|---|
| V28 / F18 / E20 / E23 / D21 / C20 / C21 / AG25 / AE28 / AD28 / Y27 / G27 / H28 / K28 / M27 / F17 / C25 | These balls must be connected to the corresponding power supply through an external pull resistor if unused |
| AF14 (rtc_iso) | This ball should be connected to the corresponding power supply through an external pull resistor if unused; or can be connected to F22 (porz) when RTC unused (level translation may be needed) |
| AB17 (rtc_porz) | This ball should be connected to VSS when RTC is unused; or can be connected to F22 (porz) when RTC unused (level translation may be needed) |

**NOTE**

All other unused signal balls **with** a Pad Configuration Register can be left unconnected with their internal pullup or pulldown resistor enabled.

**NOTE**

All other unused signal balls **without** Pad Configuration Register can be left unconnected.

## 4.2 Ball Characteristics

Table 4-2 describes the terminal characteristics and the signals multiplexed on each ball. The following list describes the table column headers:

1. **BALL NUMBER:** Ball number(s) on the bottom side associated with each signal on the bottom.
2. **BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
3. **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).

**NOTE**

Table 4-2 does not consider the subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 4.4, *Signal Descriptions*.

**NOTE**

In the Driver off mode, the buffer is configured in high-impedance.

4. **PN:** This column shows if the functionality is applicable for **AM5726** device. Note that the Ball Characteristics table presents a functionality of super set. If the cell is empty it means that the signal is available in all devices.
   - **Yes** - Functionality is presented in **AM5726**
   - **No** - Functionality is not presented in **AM5726**
   An empty box means Yes.
5. **MUXMODE:** Multiplexing mode number:
   a. MUXMODE 0 is the primary muxmode; this means that when MUXMODE=0, the function mapped on the pin corresponds to the name of the pin. The primary muxmode is not necessarily the default muxmode.

**NOTE**

The default muxmode is the mode at the release of the reset; also see the RESET REL. MUXMODE column.

   b. MUXMODE 1 through 15 are possible muxmodes for alternate functions. On each pin, some


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muxmodes are effectively used for alternate functions, while some muxmodes are not used. Only MUXMODE values which correspond to defined functions should be used.

c. An empty box means Not Applicable.

6. **TYPE:** Signal type and direction:
   - I = Input
   - O = Output
   - IO = Input or Output
   - D = Open drain
   - DS = Differential Signaling
   - A = Analog
   - PWR = Power
   - GND = Ground
   - CAP = LDO Capacitor
7. **BALL RESET STATE:** The state of the terminal at power-on reset:
   - drive 0 (OFF): The buffer drives $V_{OL}$ (pulldown or pullup resistor not activated).
   - drive 1 (OFF): The buffer drives $V_{OH}$ (pulldown or pullup resistor not activated).
   - OFF: High-impedance
   - PD: High-impedance with an active pulldown resistor
   - PU: High-impedance with an active pullup resistor
   - An empty box means Not Applicable
8. **BALL RESET REL. STATE:** The state of the terminal at the deactivation of the rstoutn signal (also mapped to the PRCM SYS_WARM_OUT_RST signal).
   - drive 0 (OFF): The buffer drives $V_{OL}$ (pulldown or pullup resistor not activated).
   - drive clk (OFF): The buffer drives a toggling clock (pulldown or pullup resistor not activated).
   - drive 1 (OFF): The buffer drives $V_{OH}$ (pulldown or pullup resistor not activated).
   - OFF: High-impedance
   - PD: High-impedance with an active pulldown resistor
   - PU: High-impedance with an active pullup resistor
   - An empty box means Not Applicable

**NOTE**

For more information on the CORE_PWRON_RET_RST reset signal and its reset sources, see the Power Reset and Clock Management / PRCM Reset Management Functional Description section of the Device TRM.

9. **BALL RESET REL. MUXMODE:** This muxmode is automatically configured at the release of the rstoutn signal (also mapped to the PRCM SYS_WARM_OUT_RST signal).
   An empty box means Not Applicable.
10. **I/O VOLTAGE VALUE**: This column describes the IO voltage value (VDDS supply).
    An empty box means Not Applicable.
11. **POWER:** The voltage supply that powers the terminal IO buffers.
    An empty box means Not Applicable.
12. **HYS:** Indicates if the input buffer is with hysteresis:
    - Yes: With hysteresis
    - No: Without hysteresis
    - An empty box: Not Applicable

**NOTE**

For more information, see the hysteresis values in Section 5.7, *Electrical Characteristics*.

13. **BUFFER TYPE:** Drive strength of the associated output buffer.

An empty box means Not Applicable.

**NOTE**

For programmable buffer strength:
- The default value is given in Table 4-2.
- A note describes all possible values according to the selected muxmode.

14. **PULLUP / PULLDOWN TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
    - PU: Internal pullup
    - PD: Internal pulldown
    - PU/PD: Internal pullup and pulldown
    - PUx/PDy: Programmable internal pullup and pulldown
    - PDy: Programmable internal pulldown
    - An empty box means No pull
15. **DSIS:** The deselected input state (DSIS) indicates the state driven on the peripheral input (logic "0", logic "1", or "PIN" level) when the peripheral pin function is not selected by any of the PINCNTLx registers.
    - 0: Logic 0 driven on the peripheral's input signal port.
    - 1: Logic 1 driven on the peripheral's input signal port.
    - blank: Pin state driven on the peripheral's input signal port.

**NOTE**

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (Hi-Z mode is not an input signal).

**NOTE**

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This should be avoided.

**CAUTION**

Not all exposed peripherals are supported on all AM572x devices. For peripherals supported on specific device from AM572x family of products refer to Table 3-1, Device Comparison Table.

**NOTE**

Some of the DDR1 and DDR2 signals have an additional state change at the release of porz. The state that the signals change to at the release of porz is as follows:

drive 0 (OFF) for: ddr1_csn0, ddr1_ck, ddr1_nck, ddr1_casn, ddr1_rasn, ddr1_wen, ddr1_ba[2:0], ddr1_a[15:0], ddr2_csn0, ddr2_ck, ddr2_nck, ddr2_casn, ddr2_rasn, ddr2_wen, ddr2_ba[2:0], ddr2_a[15:0].

OFF for: ddr1_ecc_d[7:0], ddr1_dqm[3:0], ddr1_dqm_ecc, ddr1_dqs[3:0], ddr1_dqsn[3:0], ddr1_dqs_ecc, ddr1_dqsn_ecc, ddr1_d[31:0], ddr2_dqm[3:0], ddr2_dqs[3:0], ddr2_dqsn[3:0], ddr2_d[31:0].


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## Table 4-2. Ball Characteristics[1]

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| K9 | cap_vbbldo_dspeve | cap_vbbldo_dspeve | | | CAP | | | | | | | | | |
| Y14 | cap_vbbldo_gpu | cap_vbbldo_gpu | | | CAP | | | | | | | | | |
| R20 | cap_vbbldo_iva | cap_vbbldo_iva | | | CAP | | | | | | | | | |
| J16 | cap_vbbldo_mpu | cap_vbbldo_mpu | | | CAP | | | | | | | | | |
| L9 | cap_vddram_core1 | cap_vddram_core1 | | | CAP | | | | | | | | | |
| J19 | cap_vddram_core2 | cap_vddram_core2 | | | CAP | | | | | | | | | |
| Y15 | cap_vddram_core3 | cap_vddram_core3 | | | CAP | | | | | | | | | |
| P19 | cap_vddram_core4 | cap_vddram_core4 | | | CAP | | | | | | | | | |
| Y16 | cap_vddram_core5 | cap_vddram_core5 | | | CAP | | | | | | | | | |
| J10 | cap_vddram_dspeve1 | cap_vddram_dspeve1 | | | CAP | | | | | | | | | |
| J9 | cap_vddram_dspeve2 | cap_vddram_dspeve2 | | | CAP | | | | | | | | | |
| Y13 | cap_vddram_gpu | cap_vddram_gpu | | | CAP | | | | | | | | | |
| T20 | cap_vddram_iva | cap_vddram_iva | | | CAP | | | | | | | | | |
| K16 | cap_vddram_mpu1 | cap_vddram_mpu1 | | | CAP | | | | | | | | | |
| K19 | cap_vddram_mpu2 | cap_vddram_mpu2 | | | CAP | | | | | | | | | |
| G19 | dcan1_rx | dcan1_rx | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | uart8_txd | | 2 | O | | | | | | | | | |
| | | mmc2_sdwp | | 3 | I | | | | | | | | | 0 |
| | | sata1_led | | 4 | O | | | | | | | | | |
| | | hdmi1_cec | No | 6 | IO | | | | | | | | | |
| | | gpio1_15 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| G20 | dcan1_tx | dcan1_tx | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | uart8_rxd | | 2 | I | | | | | | | | | 1 |
| | | mmc2_sdcd | | 3 | I | | | | | | | | | 1 |
| | | hdmi1_hpd | No | 6 | I | | | | | | | | | |
| | | gpio1_14 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AD20 | ddr1_a0 | ddr1_a0 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AC19 | ddr1_a1 | ddr1_a1 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AD21 | ddr1_a10 | ddr1_a10 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AD22 | ddr1_a11 | ddr1_a11 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AC21 | ddr1_a12 | ddr1_a12 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |

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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AF18 | ddr1_a13 | ddr1_a13 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AE17 | ddr1_a14 | ddr1_a14 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AD18 | ddr1_a15 | ddr1_a15 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AC20 | ddr1_a2 | ddr1_a2 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AB19 | ddr1_a3 | ddr1_a3 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AF21 | ddr1_a4 | ddr1_a4 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AH22 | ddr1_a5 | ddr1_a5 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AG23 | ddr1_a6 | ddr1_a6 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AE21 | ddr1_a7 | ddr1_a7 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AF22 | ddr1_a8 | ddr1_a8 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AE22 | ddr1_a9 | ddr1_a9 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AF17 | ddr1_ba0 | ddr1_ba0 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AE18 | ddr1_ba1 | ddr1_ba1 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AB18 | ddr1_ba2 | ddr1_ba2 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AC18 | ddr1_casn | ddr1_casn | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AG24 | ddr1_ck | ddr1_ck | | 0 | O | PD | drive clk (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AG22 | ddr1_cke | ddr1_cke | | 0 | O | PD | drive 0 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AH23 | ddr1_csn0 | ddr1_csn0 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AF25 | ddr1_d0 | ddr1_d0 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AF26 | ddr1_d1 | ddr1_d1 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AG27 | ddr1_d10 | ddr1_d10 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AF28 | ddr1_d11 | ddr1_d11 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AE26 | ddr1_d12 | ddr1_d12 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AC25 | ddr1_d13 | ddr1_d13 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AC24 | ddr1_d14 | ddr1_d14 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AD25 | ddr1_d15 | ddr1_d15 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| V20 | ddr1_d16 | ddr1_d16 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| W20 | ddr1_d17 | ddr1_d17 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AB28 | ddr1_d18 | ddr1_d18 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AC28 | ddr1_d19 | ddr1_d19 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AG26 | ddr1_d2 | ddr1_d2 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AC27 | ddr1_d20 | ddr1_d20 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| Y19 | ddr1_d21 | ddr1_d21 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AB27 | ddr1_d22 | ddr1_d22 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| Y20 | ddr1_d23 | ddr1_d23 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AA23 | ddr1_d24 | ddr1_d24 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| Y22 | ddr1_d25 | ddr1_d25 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| Y23 | ddr1_d26 | ddr1_d26 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AA24 | ddr1_d27 | ddr1_d27 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| Y24 | ddr1_d28 | ddr1_d28 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AA26 | ddr1_d29 | ddr1_d29 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AH26 | ddr1_d3 | ddr1_d3 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AA25 | ddr1_d30 | ddr1_d30 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AA28 | ddr1_d31 | ddr1_d31 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AF24 | ddr1_d4 | ddr1_d4 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AE24 | ddr1_d5 | ddr1_d5 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |

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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AF23 | ddr1_d6 | ddr1_d6 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AE23 | ddr1_d7 | ddr1_d7 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AC23 | ddr1_d8 | ddr1_d8 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AF27 | ddr1_d9 | ddr1_d9 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AD23 | ddr1_dqm0 | ddr1_dqm0 | | 0 | O | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AB23 | ddr1_dqm1 | ddr1_dqm1 | | 0 | O | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AC26 | ddr1_dqm2 | ddr1_dqm2 | | 0 | O | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AA27 | ddr1_dqm3 | ddr1_dqm3 | | 0 | O | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| V26 | ddr1_dqm_ecc | ddr1_dqm_ecc | | 0 | O | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AH25 | ddr1_dqs0 | ddr1_dqs0 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | | LVCMOS DDR | Pux/PDy | |
| AE27 | ddr1_dqs1 | ddr1_dqs1 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | | LVCMOS DDR | Pux/PDy | |
| AD27 | ddr1_dqs2 | ddr1_dqs2 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | | LVCMOS DDR | Pux/PDy | |
| Y28 | ddr1_dqs3 | ddr1_dqs3 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | | LVCMOS DDR | Pux/PDy | |
| AG25 | ddr1_dqsn0 | ddr1_dqsn0 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr1 | | LVCMOS DDR | Pux/PDy | |
| AE28 | ddr1_dqsn1 | ddr1_dqsn1 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr1 | | LVCMOS DDR | Pux/PDy | |
| AD28 | ddr1_dqsn2 | ddr1_dqsn2 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr1 | | LVCMOS DDR | Pux/PDy | |
| Y27 | ddr1_dqsn3 | ddr1_dqsn3 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr1 | | LVCMOS DDR | Pux/PDy | |
| V28 | ddr1_dqsn_ecc | ddr1_dqsn_ecc | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr1 | | LVCMOS DDR | Pux/PDy | |
| V27 | ddr1_dqs_ecc | ddr1_dqs_ecc | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | | LVCMOS DDR | Pux/PDy | |
| W22 | ddr1_ecc_d0 | ddr1_ecc_d0 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| V23 | ddr1_ecc_d1 | ddr1_ecc_d1 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| W19 | ddr1_ecc_d2 | ddr1_ecc_d2 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| W23 | ddr1_ecc_d3 | ddr1_ecc_d3 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Y25 | ddr1_ecc_d4 | ddr1_ecc_d4 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| V24 | ddr1_ecc_d5 | ddr1_ecc_d5 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| V25 | ddr1_ecc_d6 | ddr1_ecc_d6 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| Y26 | ddr1_ecc_d7 | ddr1_ecc_d7 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AH24 | ddr1_nck | ddr1_nck | | 0 | O | PD | drive clk (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AE20 | ddr1_odt0 | ddr1_odt0 | | 0 | O | PD | drive 0 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AF20 | ddr1_rasn | ddr1_rasn | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| AG21 | ddr1_rst | ddr1_rst | | 0 | O | PD | drive 0 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| Y18 | ddr1_vref0 | ddr1_vref0 | | 0 | PWR | OFF | OFF | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | | |
| AH21 | ddr1_wen | ddr1_wen | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr1 | No | LVCMOS DDR | Pux/PDy | |
| R25 | ddr2_a0 | ddr2_a0 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| R26 | ddr2_a1 | ddr2_a1 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| N23 | ddr2_a10 | ddr2_a10 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| P26 | ddr2_a11 | ddr2_a11 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| N28 | ddr2_a12 | ddr2_a12 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| T22 | ddr2_a13 | ddr2_a13 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| R22 | ddr2_a14 | ddr2_a14 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| U22 | ddr2_a15 | ddr2_a15 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| R28 | ddr2_a2 | ddr2_a2 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| R27 | ddr2_a3 | ddr2_a3 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| P23 | ddr2_a4 | ddr2_a4 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| P22 | ddr2_a5 | ddr2_a5 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| P25 | ddr2_a6 | ddr2_a6 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |

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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N20 | ddr2_a7 | ddr2_a7 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| P27 | ddr2_a8 | ddr2_a8 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| N27 | ddr2_a9 | ddr2_a9 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| U23 | ddr2_ba0 | ddr2_ba0 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| U27 | ddr2_ba1 | ddr2_ba1 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| U26 | ddr2_ba2 | ddr2_ba2 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| U28 | ddr2_casn | ddr2_casn | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| T28 | ddr2_ck | ddr2_ck | | 0 | O | PD | drive clk (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| U24 | ddr2_cke | ddr2_cke | | 0 | O | PD | drive 0 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| P24 | ddr2_csn0 | ddr2_csn0 | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| E26 | ddr2_d0 | ddr2_d0 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| G25 | ddr2_d1 | ddr2_d1 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| H24 | ddr2_d10 | ddr2_d10 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| H26 | ddr2_d11 | ddr2_d11 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| G26 | ddr2_d12 | ddr2_d12 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| J25 | ddr2_d13 | ddr2_d13 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| J26 | ddr2_d14 | ddr2_d14 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| J24 | ddr2_d15 | ddr2_d15 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| L22 | ddr2_d16 | ddr2_d16 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| K20 | ddr2_d17 | ddr2_d17 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| K21 | ddr2_d18 | ddr2_d18 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| L23 | ddr2_d19 | ddr2_d19 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| F25 | ddr2_d2 | ddr2_d2 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L24 | ddr2_d20 | ddr2_d20 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| J23 | ddr2_d21 | ddr2_d21 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| K22 | ddr2_d22 | ddr2_d22 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| J20 | ddr2_d23 | ddr2_d23 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| L27 | ddr2_d24 | ddr2_d24 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| L26 | ddr2_d25 | ddr2_d25 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| L25 | ddr2_d26 | ddr2_d26 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| L28 | ddr2_d27 | ddr2_d27 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| M23 | ddr2_d28 | ddr2_d28 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| M24 | ddr2_d29 | ddr2_d29 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| F24 | ddr2_d3 | ddr2_d3 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| M25 | ddr2_d30 | ddr2_d30 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| M26 | ddr2_d31 | ddr2_d31 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| F26 | ddr2_d4 | ddr2_d4 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| F27 | ddr2_d5 | ddr2_d5 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| E27 | ddr2_d6 | ddr2_d6 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| E28 | ddr2_d7 | ddr2_d7 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| H23 | ddr2_d8 | ddr2_d8 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| H25 | ddr2_d9 | ddr2_d9 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| F28 | ddr2_dqm0 | ddr2_dqm0 | | 0 | O | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| G24 | ddr2_dqm1 | ddr2_dqm1 | | 0 | O | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| K23 | ddr2_dqm2 | ddr2_dqm2 | | 0 | O | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| M22 | ddr2_dqm3 | ddr2_dqm3 | | 0 | O | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |

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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G28 | ddr2_dqs0 | ddr2_dqs0 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr2 | | LVCMOS DDR | Pux/PDy | |
| H27 | ddr2_dqs1 | ddr2_dqs1 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr2 | | LVCMOS DDR | Pux/PDy | |
| K27 | ddr2_dqs2 | ddr2_dqs2 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr2 | | LVCMOS DDR | Pux/PDy | |
| M28 | ddr2_dqs3 | ddr2_dqs3 | | 0 | IO | PD | PD | | 1.35/1.5/1.8 | vdds_ddr2 | | LVCMOS DDR | Pux/PDy | |
| G27 | ddr2_dqsn0 | ddr2_dqsn0 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | | LVCMOS DDR | Pux/PDy | |
| H28 | ddr2_dqsn1 | ddr2_dqsn1 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | | LVCMOS DDR | Pux/PDy | |
| K28 | ddr2_dqsn2 | ddr2_dqsn2 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | | LVCMOS DDR | Pux/PDy | |
| M27 | ddr2_dqsn3 | ddr2_dqsn3 | | 0 | IO | PU | PU | | 1.35/1.5/1.8 | vdds_ddr2 | | LVCMOS DDR | Pux/PDy | |
| T27 | ddr2_nck | ddr2_nck | | 0 | O | PD | drive clk (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| R23 | ddr2_odt0 | ddr2_odt0 | | 0 | O | PD | drive 0 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| T23 | ddr2_rasn | ddr2_rasn | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| R24 | ddr2_rst | ddr2_rst | | 0 | O | PD | drive 0 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| N22 | ddr2_vref0 | ddr2_vref0 | | 0 | PWR | OFF | OFF | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | | |
| U25 | ddr2_wen | ddr2_wen | | 0 | O | PD | drive 1 (OFF) | | 1.35/1.5/1.8 | vdds_ddr2 | No | LVCMOS DDR | Pux/PDy | |
| G21 | emu0 | emu0 | | 0 | IO | PU | PU | 0 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | gpio8_30 | | 14 | IO | | | | | | | | | |
| D24 | emu1 | emu1 | | 0 | IO | PU | PU | 0 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | gpio8_31 | | 14 | IO | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AC5 | gpio6_10 | gpio6_10 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mdio_mclk | | 1 | O | | | | | | | | | 1 |
| | | i2c3_sda | | 2 | IO | | | | | | | | | 1 |
| | | vin2b_hsync1 | | 4 | I | | | | | | | | | |
| | | vin5a_clk0 | | 9 | I | | | | | | | | | 0 |
| | | ehrpwm2A | | 10 | O | | | | | | | | | |
| | | pr2_mii_mt1_clk | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi0 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo0 | | 13 | O | | | | | | | | | |
| | | gpio6_10 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AB4 | gpio6_11 | gpio6_11 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mdio_d | | 1 | IO | | | | | | | | | 1 |
| | | i2c3_scl | | 2 | IO | | | | | | | | | 1 |
| | | vin2b_vsync1 | | 4 | I | | | | | | | | | |
| | | vin5a_de0 | | 9 | I | | | | | | | | | 0 |
| | | ehrpwm2B | | 10 | O | | | | | | | | | |
| | | pr2_mii1_txen | | 11 | O | | | | | | | | | |
| | | pr2_pru0_gpi1 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo1 | | 13 | O | | | | | | | | | |
| | | gpio6_11 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| E21 | gpio6_14 | gpio6_14 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mcasp1_axr8 | | 1 | IO | | | | | | | | | 0 |
| | | dcan2_tx | | 2 | IO | | | | | | | | | 1 |
| | | uart10_rxd | | 3 | I | | | | | | | | | 1 |
| | | vout2_hsync | No | 6 | O | | | | | | | | | |
| | | vin4a_hsync0 | | 8 | I | | | | | | | | | 0 |
| | | i2c3_sda | | 9 | IO | | | | | | | | | 1 |
| | | timer1 | | 10 | IO | | | | | | | | | |
| | | gpio6_14 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F20 | gpio6_15 | gpio6_15 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mcasp1_axr9 | | 1 | IO | | | | | | | | | 0 |
| | | dcan2_rx | | 2 | IO | | | | | | | | | 1 |
| | | uart10_txd | | 3 | O | | | | | | | | | |
| | | vout2_vsync | No | 6 | O | | | | | | | | | |
| | | vin4a_vsync0 | | 8 | I | | | | | | | | | 0 |
| | | i2c3_scl | | 9 | IO | | | | | | | | | 1 |
| | | timer2 | | 10 | IO | | | | | | | | | |
| | | gpio6_15 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| F21 | gpio6_16 | gpio6_16 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mcasp1_axr10 | | 1 | IO | | | | | | | | | 0 |
| | | vout2_fld | No | 6 | O | | | | | | | | | |
| | | vin4a_fld0 | | 8 | I | | | | | | | | | 0 |
| | | clkout1 | | 9 | O | | | | | | | | | |
| | | timer3 | | 10 | IO | | | | | | | | | |
| | | gpio6_16 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| R6 | gpmc_a0 | gpmc_a0 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin3a_d16 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d16 | No | 3 | O | | | | | | | | | |
| | | vin4a_d0 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d0 | | 6 | I | | | | | | | | | 0 |
| | | i2c4_scl | | 7 | IO | | | | | | | | | 1 |
| | | uart5_rxd | | 8 | I | | | | | | | | | 1 |
| | | gpio7_3 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| T9 | gpmc_a1 | gpmc_a1 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin3a_d17 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d17 | No | 3 | O | | | | | | | | | |
| | | vin4a_d1 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d1 | | 6 | I | | | | | | | | | 0 |
| | | i2c4_sda | | 7 | IO | | | | | | | | | 1 |
| | | uart5_txd | | 8 | O | | | | | | | | | |
| | | gpio7_4 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N9 | gpmc_a10 | gpmc_a10 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin3a_de0 | | 2 | I | | | | | | | | | 0 |
| | | vout3_de | No | 3 | O | | | | | | | | | |
| | | vin4b_clk1 | | 6 | I | | | | | | | | | 0 |
| | | timer10 | | 7 | IO | | | | | | | | | |
| | | spi4_d0 | | 8 | IO | | | | | | | | | 0 |
| | | gpio2_0 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| P9 | gpmc_a11 | gpmc_a11 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin3a_fld0 | | 2 | I | | | | | | | | | 0 |
| | | vout3_fld | No | 3 | O | | | | | | | | | |
| | | vin4a_fld0 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_de1 | | 6 | I | | | | | | | | | 0 |
| | | timer9 | | 7 | IO | | | | | | | | | |
| | | spi4_cs0 | | 8 | IO | | | | | | | | | 1 |
| | | gpio2_1 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| P4 | gpmc_a12 | gpmc_a12 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin4a_clk0 | | 4 | I | | | | | | | | | 0 |
| | | gpmc_a0 | | 5 | O | | | | | | | | | |
| | | vin4b_fld1 | | 6 | I | | | | | | | | | 0 |
| | | timer8 | | 7 | IO | | | | | | | | | |
| | | spi4_cs1 | | 8 | IO | | | | | | | | | 1 |
| | | dma_evt1 | | 9 | I | | | | | | | | | 0 |
| | | gpio2_2 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| R3 | gpmc_a13 | gpmc_a13 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | qspi1_rtclk | | 1 | I | | | | | | | | | 0 |
| | | vin4a_hsync0 | | 4 | I | | | | | | | | | 0 |
| | | timer7 | | 7 | IO | | | | | | | | | |
| | | spi4_cs2 | | 8 | IO | | | | | | | | | 1 |
| | | dma_evt2 | | 9 | I | | | | | | | | | 0 |
| | | gpio2_3 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| T2 | gpmc_a14 | gpmc_a14 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | qspi1_d3 | | 1 | I | | | | | | | | | 0 |
| | | vin4a_vsync0 | | 4 | I | | | | | | | | | 0 |
| | | timer6 | | 7 | IO | | | | | | | | | |
| | | spi4_cs3 | | 8 | IO | | | | | | | | | 1 |
| | | gpio2_4 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| U2 | gpmc_a15 | gpmc_a15 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | qspi1_d2 | | 1 | I | | | | | | | | | 0 |
| | | vin4a_d8 | | 4 | I | | | | | | | | | 0 |
| | | timer5 | | 7 | IO | | | | | | | | | |
| | | gpio2_5 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| U1 | gpmc_a16 | gpmc_a16 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | qspi1_d0 | | 1 | IO | | | | | | | | | 0 |
| | | vin4a_d9 | | 4 | I | | | | | | | | | 0 |
| | | gpio2_6 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| P3 | gpmc_a17 | gpmc_a17 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | qspi1_d1 | | 1 | I | | | | | | | | | 0 |
| | | vin4a_d10 | | 4 | I | | | | | | | | | 0 |
| | | gpio2_7 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| R2 | gpmc_a18 | gpmc_a18 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | qspi1_sclk | | 1 | O | | | | | | | | | |
| | | vin4a_d11 | | 4 | I | | | | | | | | | 0 |
| | | gpio2_8 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| K7 [(9)] | gpmc_a19 | gpmc_a19 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv11 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mmc2_dat4 | | 1 | IO | | | | | | | | | 1 |
| | | gpmc_a13 | | 2 | O | | | | | | | | | |
| | | vin4a_d12 | | 4 | I | | | | | | | | | 0 |
| | | vin3b_d0 | | 6 | I | | | | | | | | | 0 |
| | | gpio2_9 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[1] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| T6 | gpmc_a2 | gpmc_a2 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin3a_d18 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d18 | No | 3 | O | | | | | | | | | |
| | | vin4a_d2 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d2 | | 6 | I | | | | | | | | | 0 |
| | | uart7_rxd | | 7 | I | | | | | | | | | 1 |
| | | uart5_ctsn | | 8 | I | | | | | | | | | 1 |
| | | gpio7_5 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| M7 [9] | gpmc_a20 | gpmc_a20 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv11 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mmc2_dat5 | | 1 | IO | | | | | | | | | 1 |
| | | gpmc_a14 | | 2 | O | | | | | | | | | |
| | | vin4a_d13 | | 4 | I | | | | | | | | | 0 |
| | | vin3b_d1 | | 6 | I | | | | | | | | | 0 |
| | | gpio2_10 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| J5 [9] | gpmc_a21 | gpmc_a21 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv11 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mmc2_dat6 | | 1 | IO | | | | | | | | | 1 |
| | | gpmc_a15 | | 2 | O | | | | | | | | | |
| | | vin4a_d14 | | 4 | I | | | | | | | | | 0 |
| | | vin3b_d2 | | 6 | I | | | | | | | | | 0 |
| | | gpio2_11 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| K6 [9] | gpmc_a22 | gpmc_a22 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv11 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mmc2_dat7 | | 1 | IO | | | | | | | | | 1 |
| | | gpmc_a16 | | 2 | O | | | | | | | | | |
| | | vin4a_d15 | | 4 | I | | | | | | | | | 0 |
| | | vin3b_d3 | | 6 | I | | | | | | | | | 0 |
| | | gpio2_12 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| J7 | gpmc_a23 | gpmc_a23 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv11 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mmc2_clk | | 1 | IO | | | | | | | | | 1 |
| | | gpmc_a17 | | 2 | O | | | | | | | | | |
| | | vin4a_fld0 | | 4 | I | | | | | | | | | 0 |
| | | vin3b_d4 | | 6 | I | | | | | | | | | 0 |
| | | gpio2_13 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[1] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| J4 [9] | gpmc_a24 | gpmc_a24 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv11 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mmc2_dat0 | | 1 | IO | | | | | | | | | 1 |
| | | gpmc_a18 | | 2 | O | | | | | | | | | |
| | | vin3b_d5 | | 6 | I | | | | | | | | | 0 |
| | | gpio2_14 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| J6 [9] | gpmc_a25 | gpmc_a25 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv11 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mmc2_dat1 | | 1 | IO | | | | | | | | | 1 |
| | | gpmc_a19 | | 2 | O | | | | | | | | | |
| | | vin3b_d6 | | 6 | I | | | | | | | | | 0 |
| | | gpio2_15 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| H4 [9] | gpmc_a26 | gpmc_a26 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv11 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mmc2_dat2 | | 1 | IO | | | | | | | | | 1 |
| | | gpmc_a20 | | 2 | O | | | | | | | | | |
| | | vin3b_d7 | | 6 | I | | | | | | | | | 0 |
| | | gpio2_16 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| H5 [9] | gpmc_a27 | gpmc_a27 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv11 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mmc2_dat3 | | 1 | IO | | | | | | | | | 1 |
| | | gpmc_a21 | | 2 | O | | | | | | | | | |
| | | vin3b_hsync1 | | 6 | I | | | | | | | | | 0 |
| | | gpio2_17 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| T7 | gpmc_a3 | gpmc_a3 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | qspi1_cs2 | | 1 | O | | | | | | | | | 1 |
| | | vin3a_d19 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d19 | No | 3 | O | | | | | | | | | |
| | | vin4a_d3 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d3 | | 6 | I | | | | | | | | | 0 |
| | | uart7_txd | | 7 | O | | | | | | | | | |
| | | uart5_rtsn | | 8 | O | | | | | | | | | |
| | | gpio7_6 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P6 | gpmc_a4 | gpmc_a4 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | qspi1_cs3 | | 1 | O | | | | | | | | | 1 |
| | | vin3a_d20 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d20 | No | 3 | O | | | | | | | | | |
| | | vin4a_d4 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d4 | | 6 | I | | | | | | | | | 0 |
| | | i2c5_scl | | 7 | IO | | | | | | | | | 1 |
| | | uart6_rxd | | 8 | I | | | | | | | | | 1 |
| | | gpio1_26 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| R9 | gpmc_a5 | gpmc_a5 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin3a_d21 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d21 | No | 3 | O | | | | | | | | | |
| | | vin4a_d5 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d5 | | 6 | I | | | | | | | | | 0 |
| | | i2c5_sda | | 7 | IO | | | | | | | | | 1 |
| | | uart6_txd | | 8 | O | | | | | | | | | |
| | | gpio1_27 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| R5 | gpmc_a6 | gpmc_a6 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin3a_d22 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d22 | No | 3 | O | | | | | | | | | |
| | | vin4a_d6 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d6 | | 6 | I | | | | | | | | | 0 |
| | | uart8_rxd | | 7 | I | | | | | | | | | 1 |
| | | uart6_ctsn | | 8 | I | | | | | | | | | 1 |
| | | gpio1_28 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| P5 | gpmc_a7 | gpmc_a7 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin3a_d23 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d23 | No | 3 | O | | | | | | | | | |
| | | vin4a_d7 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d7 | | 6 | I | | | | | | | | | 0 |
| | | uart8_txd | | 7 | O | | | | | | | | | |
| | | uart6_rtsn | | 8 | O | | | | | | | | | |
| | | gpio1_29 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N7 | gpmc_a8 | gpmc_a8 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin3a_hsync0 | | 2 | I | | | | | | | | | 0 |
| | | vout3_hsync | No | 3 | O | | | | | | | | | |
| | | vin4b_hsync1 | | 6 | I | | | | | | | | | 0 |
| | | timer12 | | 7 | IO | | | | | | | | | |
| | | spi4_sclk | | 8 | IO | | | | | | | | | 0 |
| | | gpio1_30 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| R4 | gpmc_a9 | gpmc_a9 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin3a_vsync0 | | 2 | I | | | | | | | | | 0 |
| | | vout3_vsync | No | 3 | O | | | | | | | | | |
| | | vin4b_vsync1 | | 6 | I | | | | | | | | | 0 |
| | | timer11 | | 7 | IO | | | | | | | | | |
| | | spi4_d1 | | 8 | IO | | | | | | | | | 0 |
| | | gpio1_31 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| M6 | gpmc_ad0 | gpmc_ad0 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d0 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d0 | No | 3 | O | | | | | | | | | |
| | | gpio1_6 | | 14 | IO | | | | | | | | | |
| | | sysboot0 | | 15 | I | | | | | | | | | |
| M2 | gpmc_ad1 | gpmc_ad1 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d1 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d1 | No | 3 | O | | | | | | | | | |
| | | gpio1_7 | | 14 | IO | | | | | | | | | |
| | | sysboot1 | | 15 | I | | | | | | | | | |
| J1 | gpmc_ad10 | gpmc_ad10 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d10 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d10 | No | 3 | O | | | | | | | | | |
| | | gpio7_28 | | 14 | IO | | | | | | | | | |
| | | sysboot10 | | 15 | I | | | | | | | | | |
| J2 | gpmc_ad11 | gpmc_ad11 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d11 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d11 | No | 3 | O | | | | | | | | | |
| | | gpio7_29 | | 14 | IO | | | | | | | | | |
| | | sysboot11 | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H1 | gpmc_ad12 | gpmc_ad12 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d12 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d12 | No | 3 | O | | | | | | | | | |
| | | gpio1_18 | | 14 | IO | | | | | | | | | |
| | | sysboot12 | | 15 | I | | | | | | | | | |
| J3 | gpmc_ad13 | gpmc_ad13 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d13 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d13 | No | 3 | O | | | | | | | | | |
| | | gpio1_19 | | 14 | IO | | | | | | | | | |
| | | sysboot13 | | 15 | I | | | | | | | | | |
| H2 | gpmc_ad14 | gpmc_ad14 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d14 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d14 | No | 3 | O | | | | | | | | | |
| | | gpio1_20 | | 14 | IO | | | | | | | | | |
| | | sysboot14 | | 15 | I | | | | | | | | | |
| H3 | gpmc_ad15 | gpmc_ad15 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d15 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d15 | No | 3 | O | | | | | | | | | |
| | | gpio1_21 | | 14 | IO | | | | | | | | | |
| | | sysboot15 | | 15 | I | | | | | | | | | |
| L5 | gpmc_ad2 | gpmc_ad2 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d2 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d2 | No | 3 | O | | | | | | | | | |
| | | gpio1_8 | | 14 | IO | | | | | | | | | |
| | | sysboot2 | | 15 | I | | | | | | | | | |
| M1 | gpmc_ad3 | gpmc_ad3 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d3 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d3 | No | 3 | O | | | | | | | | | |
| | | gpio1_9 | | 14 | IO | | | | | | | | | |
| | | sysboot3 | | 15 | I | | | | | | | | | |
| L6 | gpmc_ad4 | gpmc_ad4 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d4 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d4 | No | 3 | O | | | | | | | | | |
| | | gpio1_10 | | 14 | IO | | | | | | | | | |
| | | sysboot4 | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L4 | gpmc_ad5 | gpmc_ad5 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d5 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d5 | No | 3 | O | | | | | | | | | |
| | | gpio1_11 | | 14 | IO | | | | | | | | | |
| | | sysboot5 | | 15 | I | | | | | | | | | |
| L3 | gpmc_ad6 | gpmc_ad6 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d6 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d6 | No | 3 | O | | | | | | | | | |
| | | gpio1_12 | | 14 | IO | | | | | | | | | |
| | | sysboot6 | | 15 | I | | | | | | | | | |
| L2 | gpmc_ad7 | gpmc_ad7 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d7 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d7 | No | 3 | O | | | | | | | | | |
| | | gpio1_13 | | 14 | IO | | | | | | | | | |
| | | sysboot7 | | 15 | I | | | | | | | | | |
| L1 | gpmc_ad8 | gpmc_ad8 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d8 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d8 | No | 3 | O | | | | | | | | | |
| | | gpio7_18 | | 14 | IO | | | | | | | | | |
| | | sysboot8 | | 15 | I | | | | | | | | | |
| K2 | gpmc_ad9 | gpmc_ad9 | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_d9 | | 2 | I | | | | | | | | | 0 |
| | | vout3_d9 | No | 3 | O | | | | | | | | | |
| | | gpio7_19 | | 14 | IO | | | | | | | | | |
| | | sysboot9 | | 15 | I | | | | | | | | | |
| N1 | gpmc_advn_ale | gpmc_advn_ale | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | gpmc_cs6 | | 1 | O | | | | | | | | | |
| | | clkout2 | | 2 | O | | | | | | | | | |
| | | gpmc_wait1 | | 3 | I | | | | | | | | | 1 |
| | | vin4a_vsync0 | | 4 | I | | | | | | | | | 0 |
| | | gpmc_a2 | | 5 | O | | | | | | | | | |
| | | gpmc_a23 | | 6 | O | | | | | | | | | |
| | | timer3 | | 7 | IO | | | | | | | | | |
| | | i2c3_sda | | 8 | IO | | | | | | | | | 1 |
| | | dma_evt2 | | 9 | I | | | | | | | | | 0 |
| | | gpio2_23 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N6 | gpmc_ben0 | gpmc_ben0 | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | gpmc_cs4 | | 1 | O | | | | | | | | | |
| | | vin1b_hsync1 | | 3 | I | | | | | | | | | 0 |
| | | vin3b_de1 | | 6 | I | | | | | | | | | 0 |
| | | timer2 | | 7 | IO | | | | | | | | | |
| | | dma_evt3 | | 9 | I | | | | | | | | | 0 |
| | | gpio2_26 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| M4 | gpmc_ben1 | gpmc_ben1 | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | gpmc_cs5 | | 1 | O | | | | | | | | | |
| | | vin1b_de1 | | 3 | I | | | | | | | | | 0 |
| | | vin3b_clk1 | | 4 | I | | | | | | | | | 0 |
| | | gpmc_a3 | | 5 | O | | | | | | | | | |
| | | vin3b_fld1 | | 6 | I | | | | | | | | | 0 |
| | | timer1 | | 7 | IO | | | | | | | | | |
| | | dma_evt4 | | 9 | I | | | | | | | | | 0 |
| | | gpio2_27 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| P7 | gpmc_clk | gpmc_clk | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | gpmc_cs7 | | 1 | O | | | | | | | | | |
| | | clkout1 | | 2 | O | | | | | | | | | |
| | | gpmc_wait1 | | 3 | I | | | | | | | | | 1 |
| | | vin4a_hsync0 | | 4 | I | | | | | | | | | 0 |
| | | vin4a_de0 | | 5 | I | | | | | | | | | 0 |
| | | vin3b_clk1 | | 6 | I | | | | | | | | | 0 |
| | | timer4 | | 7 | IO | | | | | | | | | |
| | | i2c3_scl | | 8 | IO | | | | | | | | | 1 |
| | | dma_evt1 | | 9 | I | | | | | | | | | 0 |
| | | gpio2_22 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| T1 | gpmc_cs0 | gpmc_cs0 | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | gpio2_19 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H6 | gpmc_cs1 | gpmc_cs1 | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv11 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mmc2_cmd | | 1 | IO | | | | | | | | | 1 |
| | | gpmc_a22 | | 2 | O | | | | | | | | | |
| | | vin4a_de0 | | 4 | I | | | | | | | | | 0 |
| | | vin3b_vsync1 | | 6 | I | | | | | | | | | 0 |
| | | gpio2_18 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| P2 | gpmc_cs2 | gpmc_cs2 | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | qspi1_cs0 | | 1 | O | | | | | | | | | 1 |
| | | gpio2_20 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| P1 | gpmc_cs3 | gpmc_cs3 | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | qspi1_cs1 | | 1 | O | | | | | | | | | 1 |
| | | vin3a_clk0 | | 2 | I | | | | | | | | | 0 |
| | | vout3_clk | No | 3 | O | | | | | | | | | |
| | | gpmc_a1 | | 5 | O | | | | | | | | | |
| | | gpio2_21 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| M5 | gpmc_oen_ren | gpmc_oen_ren | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | gpio2_24 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| N2 | gpmc_wait0 | gpmc_wait0 | | 0 | I | PU | PU | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | gpio2_28 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| M3 | gpmc_wen | gpmc_wen | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv10 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | gpio2_25 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AG16 | hdmi1_clockx | hdmi1_clockx | No | 0 | O | | | | 1.8 | vdda_hdmi | | HDMIPHY | PDy | |
| AH16 | hdmi1_clocky | hdmi1_clocky | No | 0 | O | | | | 1.8 | vdda_hdmi | | HDMIPHY | PDy | |
| AG17 | hdmi1_data0x | hdmi1_data0x | No | 0 | O | | | | 1.8 | vdda_hdmi | | HDMIPHY | PDy | |
| AH17 | hdmi1_data0y | hdmi1_data0y | No | 0 | O | | | | 1.8 | vdda_hdmi | | HDMIPHY | PDy | |
| AG18 | hdmi1_data1x | hdmi1_data1x | No | 0 | O | | | | 1.8 | vdda_hdmi | | HDMIPHY | PDy | |
| AH18 | hdmi1_data1y | hdmi1_data1y | No | 0 | O | | | | 1.8 | vdda_hdmi | | HDMIPHY | PDy | |
| AG19 | hdmi1_data2x | hdmi1_data2x | No | 0 | O | | | | 1.8 | vdda_hdmi | | HDMIPHY | PDy | |
| AH19 | hdmi1_data2y | hdmi1_data2y | No | 0 | O | | | | 1.8 | vdda_hdmi | | HDMIPHY | PDy | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C20 | i2c1_scl | i2c1_scl | | 0 | IO | OFF | OFF | | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS I2C | PU/PD | |
| C21 | i2c1_sda | i2c1_sda | | 0 | IO | OFF | OFF | | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS I2C | PU/PD | |
| F17 | i2c2_scl | i2c2_scl | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS I2C | PU/PD | 1 |
| | | hdmi1_ddc_sda | No | 1 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| C25 | i2c2_sda | i2c2_sda | | 0 | IO | OFF | OFF | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS I2C | PU/PD | 1 |
| | | hdmi1_ddc_scl | No | 1 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AH15 | ljcb_clkn | ljcb_clkn | | 0 | IO | | | | 1.8 | vdda_pcie | | LJCB | | |
| AG15 | ljcb_clkp | ljcb_clkp | | 0 | IO | | | | 1.8 | vdda_pcie | | LJCB | | |
| B14 | mcasp1_aclkr | mcasp1_aclkr | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp7_axr2 | | 1 | IO | | | | | | | | | 0 |
| | | vout2_d0 | No | 6 | O | | | | | | | | | |
| | | vin4a_d0 | | 8 | I | | | | | | | | | 0 |
| | | i2c4_sda | | 10 | IO | | | | | | | | | 1 |
| | | gpio5_0 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| C14 | mcasp1_aclkx | mcasp1_aclkx | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin6a_fld0 | | 7 | I | | | | | | | | | 0 |
| | | i2c3_sda | | 10 | IO | | | | | | | | | 1 |
| | | pr2_mdio_mdclk | | 11 | O | | | | | | | | | |
| | | pr2_pru1_gpi7 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo7 | | 13 | O | | | | | | | | | |
| | | gpio7_31 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G12 | mcasp1_axr0 | mcasp1_axr0 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | uart6_rxd | | 3 | I | | | | | | | | | 1 |
| | | vin6a_vsync0 | | 7 | I | | | | | | | | | 0 |
| | | i2c5_sda | | 10 | IO | | | | | | | | | 1 |
| | | pr2_mii0_rxer | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi8 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo8 | | 13 | O | | | | | | | | | |
| | | gpio5_2 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| F12 | mcasp1_axr1 | mcasp1_axr1 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | uart6_txd | | 3 | O | | | | | | | | | |
| | | vin6a_hsync0 | | 7 | I | | | | | | | | | 0 |
| | | i2c5_scl | | 10 | IO | | | | | | | | | 1 |
| | | pr2_mii_mt0_clk | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi9 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo9 | | 13 | O | | | | | | | | | |
| | | gpio5_3 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B13 | mcasp1_axr10 | mcasp1_axr10 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp6_aclkx | | 1 | IO | | | | | | | | | 0 |
| | | mcasp6_aclkr | | 2 | IO | | | | | | | | | |
| | | spi3_d0 | | 3 | IO | | | | | | | | | 0 |
| | | vin6a_d13 | | 7 | I | | | | | | | | | 0 |
| | | timer7 | | 10 | IO | | | | | | | | | |
| | | pr2_mii0_txd2 | | 11 | O | | | | | | | | | |
| | | pr2_pru1_gpi12 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo12 | | 13 | O | | | | | | | | | |
| | | gpio5_12 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A12 | mcasp1_axr11 | mcasp1_axr11 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp6_fsx | | 1 | IO | | | | | | | | | 0 |
| | | mcasp6_fsr | | 2 | IO | | | | | | | | | |
| | | spi3_cs0 | | 3 | IO | | | | | | | | | 1 |
| | | vin6a_d12 | | 7 | I | | | | | | | | | 0 |
| | | timer8 | | 10 | IO | | | | | | | | | |
| | | pr2_mii0_txd1 | | 11 | O | | | | | | | | | |
| | | pr2_pru1_gpi13 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo13 | | 13 | O | | | | | | | | | |
| | | gpio4_17 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| E14 | mcasp1_axr12 | mcasp1_axr12 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp7_axr0 | | 1 | IO | | | | | | | | | 0 |
| | | spi3_cs1 | | 3 | IO | | | | | | | | | 1 |
| | | vin6a_d11 | | 7 | I | | | | | | | | | 0 |
| | | timer9 | | 10 | IO | | | | | | | | | |
| | | pr2_mii0_txd0 | | 11 | O | | | | | | | | | |
| | | pr2_pru1_gpi14 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo14 | | 13 | O | | | | | | | | | |
| | | gpio4_18 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A13 | mcasp1_axr13 | mcasp1_axr13 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp7_axr1 | | 1 | IO | | | | | | | | | 0 |
| | | vin6a_d10 | | 7 | I | | | | | | | | | 0 |
| | | timer10 | | 10 | IO | | | | | | | | | |
| | | pr2_mii_mr0_clk | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi15 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo15 | | 13 | O | | | | | | | | | |
| | | gpio6_4 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G14 | mcasp1_axr14 | mcasp1_axr14 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp7_aclkx | | 1 | IO | | | | | | | | | 0 |
| | | mcasp7_aclkr | | 2 | IO | | | | | | | | | |
| | | vin6a_d9 | | 7 | I | | | | | | | | | 0 |
| | | timer11 | | 10 | IO | | | | | | | | | |
| | | pr2_mii0_rxdv | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi16 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo16 | | 13 | O | | | | | | | | | |
| | | gpio6_5 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| F14 | mcasp1_axr15 | mcasp1_axr15 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp7_fsx | | 1 | IO | | | | | | | | | 0 |
| | | mcasp7_fsr | | 2 | IO | | | | | | | | | |
| | | vin6a_d8 | | 7 | I | | | | | | | | | 0 |
| | | timer12 | | 10 | IO | | | | | | | | | |
| | | pr2_mii0_rxd3 | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi20 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo20 | | 13 | O | | | | | | | | | |
| | | gpio6_6 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| G13 | mcasp1_axr2 | mcasp1_axr2 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp6_axr2 | | 1 | IO | | | | | | | | | 0 |
| | | uart6_ctsn | | 3 | I | | | | | | | | | 1 |
| | | vout2_d2 | No | 6 | O | | | | | | | | | |
| | | vin4a_d2 | | 8 | I | | | | | | | | | 0 |
| | | gpio5_4 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| J11 | mcasp1_axr3 | mcasp1_axr3 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp6_axr3 | | 1 | IO | | | | | | | | | 0 |
| | | uart6_rtsn | | 3 | O | | | | | | | | | |
| | | vout2_d3 | No | 6 | O | | | | | | | | | |
| | | vin4a_d3 | | 8 | I | | | | | | | | | 0 |
| | | gpio5_5 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E12 | mcasp1_axr4 | mcasp1_axr4 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp4_axr2 | | 1 | IO | | | | | | | | | 0 |
| | | vout2_d4 | No | 6 | O | | | | | | | | | |
| | | vin4a_d4 | | 8 | I | | | | | | | | | 0 |
| | | gpio5_6 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| F13 | mcasp1_axr5 | mcasp1_axr5 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp4_axr3 | | 1 | IO | | | | | | | | | 0 |
| | | vout2_d5 | No | 6 | O | | | | | | | | | |
| | | vin4a_d5 | | 8 | I | | | | | | | | | 0 |
| | | gpio5_7 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| C12 | mcasp1_axr6 | mcasp1_axr6 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp5_axr2 | | 1 | IO | | | | | | | | | 0 |
| | | vout2_d6 | No | 6 | O | | | | | | | | | |
| | | vin4a_d6 | | 8 | I | | | | | | | | | 0 |
| | | gpio5_8 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| D12 | mcasp1_axr7 | mcasp1_axr7 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp5_axr3 | | 1 | IO | | | | | | | | | 0 |
| | | vout2_d7 | No | 6 | O | | | | | | | | | |
| | | vin4a_d7 | | 8 | I | | | | | | | | | 0 |
| | | timer4 | | 10 | IO | | | | | | | | | |
| | | gpio5_9 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B12 | mcasp1_axr8 | mcasp1_axr8 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp6_axr0 | | 1 | IO | | | | | | | | | 0 |
| | | spi3_sclk | | 3 | IO | | | | | | | | | 0 |
| | | vin6a_d15 | | 7 | I | | | | | | | | | 0 |
| | | timer5 | | 10 | IO | | | | | | | | | |
| | | pr2_mii0_txen | | 11 | O | | | | | | | | | |
| | | pr2_pru1_gpi10 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo10 | | 13 | O | | | | | | | | | |
| | | gpio5_10 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A11 | mcasp1_axr9 | mcasp1_axr9 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp6_axr1 | | 1 | IO | | | | | | | | | 0 |
| | | spi3_d1 | | 3 | IO | | | | | | | | | 0 |
| | | vin6a_d14 | | 7 | I | | | | | | | | | 0 |
| | | timer6 | | 10 | IO | | | | | | | | | |
| | | pr2_mii0_txd3 | | 11 | O | | | | | | | | | |
| | | pr2_pru1_gpi11 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo11 | | 13 | O | | | | | | | | | |
| | | gpio5_11 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| J14 | mcasp1_fsr | mcasp1_fsr | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp7_axr3 | | 1 | IO | | | | | | | | | 0 |
| | | vout2_d1 | No | 6 | O | | | | | | | | | |
| | | vin4a_d1 | | 8 | I | | | | | | | | | 0 |
| | | i2c4_scl | | 10 | IO | | | | | | | | | 1 |
| | | gpio5_1 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| D14 | mcasp1_fsx | mcasp1_fsx | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin6a_de0 | | 7 | I | | | | | | | | | 0 |
| | | i2c3_scl | | 10 | IO | | | | | | | | | 1 |
| | | pr2_mdio_data | | 11 | IO | | | | | | | | | 1 |
| | | gpio7_30 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| E15 | mcasp2_aclkr | mcasp2_aclkr | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp8_axr2 | | 1 | IO | | | | | | | | | 0 |
| | | vout2_d8 | No | 6 | O | | | | | | | | | |
| | | vin4a_d8 | | 8 | I | | | | | | | | | 0 |
| | | Driver off | | 15 | I | | | | | | | | | |
| A19 | mcasp2_aclkx | mcasp2_aclkx | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin6a_d7 | | 7 | I | | | | | | | | | 0 |
| | | pr2_mii0_rxd2 | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi18 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo18 | | 13 | O | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B15 | mcasp2_axr0 | mcasp2_axr0 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout2_d10 | No | 6 | O | | | | | | | | | |
| | | vin4a_d10 | | 8 | I | | | | | | | | | 0 |
| | | Driver off | | 15 | I | | | | | | | | | |
| A15 | mcasp2_axr1 | mcasp2_axr1 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout2_d11 | No | 6 | O | | | | | | | | | |
| | | vin4a_d11 | | 8 | I | | | | | | | | | 0 |
| | | Driver off | | 15 | I | | | | | | | | | |
| C15 | mcasp2_axr2 | mcasp2_axr2 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp3_axr2 | | 1 | IO | | | | | | | | | 0 |
| | | vin6a_d5 | | 7 | I | | | | | | | | | 0 |
| | | pr2_mii0_rxd0 | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi16 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo16 | | 13 | O | | | | | | | | | |
| | | gpio6_8 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A16 | mcasp2_axr3 | mcasp2_axr3 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp3_axr3 | | 1 | IO | | | | | | | | | 0 |
| | | vin6a_d4 | | 7 | I | | | | | | | | | 0 |
| | | pr2_mii0_rxlink | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi17 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo17 | | 13 | O | | | | | | | | | |
| | | gpio6_9 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| D15 | mcasp2_axr4 | mcasp2_axr4 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp8_axr0 | | 1 | IO | | | | | | | | | 0 |
| | | vout2_d12 | No | 6 | O | | | | | | | | | |
| | | vin4a_d12 | | 8 | I | | | | | | | | | 0 |
| | | gpio1_4 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B16 | mcasp2_axr5 | mcasp2_axr5 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp8_axr1 | | 1 | IO | | | | | | | | | 0 |
| | | vout2_d13 | No | 6 | O | | | | | | | | | |
| | | vin4a_d13 | | 8 | I | | | | | | | | | 0 |
| | | gpio6_7 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B17 | mcasp2_axr6 | mcasp2_axr6 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp8_aclkx | | 1 | IO | | | | | | | | | 0 |
| | | mcasp8_aclkr | | 2 | IO | | | | | | | | | |
| | | vout2_d14 | No | 6 | O | | | | | | | | | |
| | | vin4a_d14 | | 8 | I | | | | | | | | | 0 |
| | | gpio2_29 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A17 | mcasp2_axr7 | mcasp2_axr7 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp8_fsx | | 1 | IO | | | | | | | | | 0 |
| | | mcasp8_fsr | | 2 | IO | | | | | | | | | |
| | | vout2_d15 | No | 6 | O | | | | | | | | | |
| | | vin4a_d15 | | 8 | I | | | | | | | | | 0 |
| | | gpio1_5 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A20 | mcasp2_fsr | mcasp2_fsr | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp8_axr3 | | 1 | IO | | | | | | | | | 0 |
| | | vout2_d9 | No | 6 | O | | | | | | | | | |
| | | vin4a_d9 | | 8 | I | | | | | | | | | 0 |
| | | Driver off | | 15 | I | | | | | | | | | |
| A18 | mcasp2_fsx | mcasp2_fsx | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin6a_d6 | | 7 | I | | | | | | | | | 0 |
| | | pr2_mii0_rxd1 | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi19 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo19 | | 13 | O | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B18 | mcasp3_aclkx | mcasp3_aclkx | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp3_aclkr | | 1 | IO | | | | | | | | | |
| | | mcasp2_axr12 | | 2 | IO | | | | | | | | | 0 |
| | | uart7_rxd | | 3 | I | | | | | | | | | 1 |
| | | vin6a_d3 | | 7 | I | | | | | | | | | 0 |
| | | pr2_mii0_crs | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi12 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo12 | | 13 | O | | | | | | | | | |
| | | gpio5_13 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B19 | mcasp3_axr0 | mcasp3_axr0 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp2_axr14 | | 2 | IO | | | | | | | | | 0 |
| | | uart7_ctsn | | 3 | I | | | | | | | | | 1 |
| | | uart5_rxd | | 4 | I | | | | | | | | | 1 |
| | | vin6a_d1 | | 7 | I | | | | | | | | | 0 |
| | | pr2_mii1_rxer | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi14 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo14 | | 13 | O | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| C17 | mcasp3_axr1 | mcasp3_axr1 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp2_axr15 | | 2 | IO | | | | | | | | | 0 |
| | | uart7_rtsn | | 3 | O | | | | | | | | | |
| | | uart5_txd | | 4 | O | | | | | | | | | |
| | | vin6a_d0 | | 7 | I | | | | | | | | | 0 |
| | | vin5a_fld0 | | 9 | I | | | | | | | | | 0 |
| | | pr2_mii1_rxlink | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi15 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo15 | | 13 | O | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| F15 | mcasp3_fsx | mcasp3_fsx | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp3_fsr | | 1 | IO | | | | | | | | | |
| | | mcasp2_axr13 | | 2 | IO | | | | | | | | | 0 |
| | | uart7_txd | | 3 | O | | | | | | | | | |
| | | vin6a_d2 | | 7 | I | | | | | | | | | 0 |
| | | pr2_mii0_col | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi13 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo13 | | 13 | O | | | | | | | | | |
| | | gpio5_14 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C18 | mcasp4_aclkx | mcasp4_aclkx | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp4_aclkr | | 1 | IO | | | | | | | | | |
| | | spi3_sclk | | 2 | IO | | | | | | | | | 0 |
| | | uart8_rxd | | 3 | I | | | | | | | | | 1 |
| | | i2c4_sda | | 4 | IO | | | | | | | | | 1 |
| | | vout2_d16 | No | 6 | O | | | | | | | | | |
| | | vin4a_d16 | | 8 | I | | | | | | | | | 0 |
| | | vin5a_d15 | | 9 | I | | | | | | | | | 0 |
| | | Driver off | | 15 | I | | | | | | | | | |
| G16 | mcasp4_axr0 | mcasp4_axr0 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | spi3_d0 | | 2 | IO | | | | | | | | | 0 |
| | | uart8_ctsn | | 3 | I | | | | | | | | | 1 |
| | | uart4_rxd | | 4 | I | | | | | | | | | 1 |
| | | vout2_d18 | No | 6 | O | | | | | | | | | |
| | | vin4a_d18 | | 8 | I | | | | | | | | | 0 |
| | | vin5a_d13 | | 9 | I | | | | | | | | | 0 |
| | | Driver off | | 15 | I | | | | | | | | | |
| D17 | mcasp4_axr1 | mcasp4_axr1 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | spi3_cs0 | | 2 | IO | | | | | | | | | 1 |
| | | uart8_rtsn | | 3 | O | | | | | | | | | |
| | | uart4_txd | | 4 | O | | | | | | | | | |
| | | vout2_d19 | No | 6 | O | | | | | | | | | |
| | | vin4a_d19 | | 8 | I | | | | | | | | | 0 |
| | | vin5a_d12 | | 9 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi0 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo0 | | 13 | O | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A21 | mcasp4_fsx | mcasp4_fsx | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp4_fsr | | 1 | IO | | | | | | | | | |
| | | spi3_d1 | | 2 | IO | | | | | | | | | 0 |
| | | uart8_txd | | 3 | O | | | | | | | | | |
| | | i2c4_scl | | 4 | IO | | | | | | | | | 1 |
| | | vout2_d17 | No | 6 | O | | | | | | | | | |
| | | vin4a_d17 | | 8 | I | | | | | | | | | 0 |
| | | vin5a_d14 | | 9 | I | | | | | | | | | 0 |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AA3 | mcasp5_aclkx | mcasp5_aclkx | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp5_aclkr | | 1 | IO | | | | | | | | | |
| | | spi4_sclk | | 2 | IO | | | | | | | | | 0 |
| | | uart9_rxd | | 3 | I | | | | | | | | | 1 |
| | | i2c5_sda | | 4 | IO | | | | | | | | | 1 |
| | | vout2_d20 | No | 6 | O | | | | | | | | | |
| | | vin4a_d20 | | 8 | I | | | | | | | | | 0 |
| | | vin5a_d11 | | 9 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi1 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo1 | | 13 | O | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AB3 | mcasp5_axr0 | mcasp5_axr0 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | spi4_d0 | | 2 | IO | | | | | | | | | 0 |
| | | uart9_ctsn | | 3 | I | | | | | | | | | 1 |
| | | uart3_rxd | | 4 | I | | | | | | | | | 1 |
| | | vout2_d22 | No | 6 | O | | | | | | | | | |
| | | vin4a_d22 | | 8 | I | | | | | | | | | 0 |
| | | vin5a_d9 | | 9 | I | | | | | | | | | 0 |
| | | pr2_mdio_mdclk | | 11 | O | | | | | | | | | |
| | | pr2_pru1_gpi3 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo3 | | 13 | O | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AA4 | mcasp5_axr1 | mcasp5_axr1 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | spi4_cs0 | | 2 | IO | | | | | | | | | 1 |
| | | uart9_rtsn | | 3 | O | | | | | | | | | |
| | | uart3_txd | | 4 | O | | | | | | | | | |
| | | vout2_d23 | No | 6 | O | | | | | | | | | |
| | | vin4a_d23 | | 8 | I | | | | | | | | | 0 |
| | | vin5a_d8 | | 9 | I | | | | | | | | | 0 |
| | | pr2_mdio_data | | 11 | IO | | | | | | | | | 1 |
| | | pr2_pru1_gpi4 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo4 | | 13 | O | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AB9 | mcasp5_fsx | mcasp5_fsx | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mcasp5_fsr | | 1 | IO | | | | | | | | | |
| | | spi4_d1 | | 2 | IO | | | | | | | | | 0 |
| | | uart9_txd | | 3 | O | | | | | | | | | |
| | | i2c5_scl | | 4 | IO | | | | | | | | | 1 |
| | | vout2_d21 | No | 6 | O | | | | | | | | | |
| | | vin4a_d21 | | 8 | I | | | | | | | | | 0 |
| | | vin5a_d10 | | 9 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi2 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo2 | | 13 | O | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| U4 | mdio_d | mdio_d | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | uart3_ctsn | | 1 | I | | | | | | | | | 1 |
| | | mii0_txer | | 3 | O | | | | | | | | | 0 |
| | | vin2a_d0 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d0 | | 5 | I | | | | | | | | | 0 |
| | | pr1_mii0_rxlink | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi1 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo1 | | 13 | O | | | | | | | | | |
| | | gpio5_16 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| V1 | mdio_mclk | mdio_mclk | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | uart3_rtsn | | 1 | O | | | | | | | | | |
| | | mii0_col | | 3 | I | | | | | | | | | 0 |
| | | vin2a_clk0 | | 4 | I | | | | | | | | | |
| | | vin4b_clk1 | | 5 | I | | | | | | | | | 0 |
| | | pr1_mii0_col | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi0 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo0 | | 13 | O | | | | | | | | | |
| | | gpio5_15 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AB2 | mlbp_clk_n | mlbp_clk_n | | 0 | I | | | | 1.8 | vdds_mlbp | No | ILVDS18 | | |
| AB1 | mlbp_clk_p | mlbp_clk_p | | 0 | I | | | | 1.8 | vdds_mlbp | No | ILVDS18 | | |
| AA2 | mlbp_dat_n | mlbp_dat_n | | 0 | IO | OFF | OFF | | 1.8 | vdds_mlbp | No | BMLB18 | | |
| AA1 | mlbp_dat_p | mlbp_dat_p | | 0 | IO | OFF | OFF | | 1.8 | vdds_mlbp | No | BMLB18 | | |
| AC2 | mlbp_sig_n | mlbp_sig_n | | 0 | IO | OFF | OFF | | 1.8 | vdds_mlbp | No | BMLB18 | | |
| AC1 | mlbp_sig_p | mlbp_sig_p | | 0 | IO | OFF | OFF | | 1.8 | vdds_mlbp | No | BMLB18 | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W6 | mmc1_clk | mmc1_clk | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv8 | Yes | SDIO1833 | PU/PD | 1 |
| | | gpio6_21 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| Y6 | mmc1_cmd | mmc1_cmd | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv8 | Yes | SDIO1833 | PU/PD | 1 |
| | | gpio6_22 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AA6 | mmc1_dat0 | mmc1_dat0 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv8 | Yes | SDIO1833 | PU/PD | 1 |
| | | gpio6_23 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| Y4 | mmc1_dat1 | mmc1_dat1 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv8 | Yes | SDIO1833 | PU/PD | 1 |
| | | gpio6_24 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AA5 | mmc1_dat2 | mmc1_dat2 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv8 | Yes | SDIO1833 | PU/PD | 1 |
| | | gpio6_25 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| Y3 | mmc1_dat3 | mmc1_dat3 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv8 | Yes | SDIO1833 | PU/PD | 1 |
| | | gpio6_26 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| W7 | mmc1_sdcd | mmc1_sdcd | | 0 | I | PU | PU | 15 | 1.8/3.3 | vddshv8 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | uart6_rxd | | 3 | I | | | | | | | | | 1 |
| | | i2c4_sda | | 4 | IO | | | | | | | | | 1 |
| | | gpio6_27 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| Y9 | mmc1_sdwp | mmc1_sdwp | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv8 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | uart6_txd | | 3 | O | | | | | | | | | |
| | | i2c4_scl | | 4 | IO | | | | | | | | | 1 |
| | | gpio6_28 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AD4 | mmc3_clk | mmc3_clk | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | vin2b_d7 | | 4 | I | | | | | | | | | 0 |
| | | vin5a_d7 | | 9 | I | | | | | | | | | 0 |
| | | ehrpwm2_tripzone_input | | 10 | IO | | | | | | | | | 0 |
| | | pr2_mii1_txd3 | | 11 | O | | | | | | | | | |
| | | pr2_pru0_gpi2 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo2 | | 13 | O | | | | | | | | | |
| | | gpio6_29 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AC4 | mmc3_cmd | mmc3_cmd | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | spi3_sclk | | 1 | IO | | | | | | | | | 0 |
| | | vin2b_d6 | | 4 | I | | | | | | | | | 0 |
| | | vin5a_d6 | | 9 | I | | | | | | | | | 0 |
| | | eCAP2_in_PWM2_out | | 10 | IO | | | | | | | | | 0 |
| | | pr2_mii1_txd2 | | 11 | O | | | | | | | | | |
| | | pr2_pru0_gpi3 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo3 | | 13 | O | | | | | | | | | |
| | | gpio6_30 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AC7 | mmc3_dat0 | mmc3_dat0 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | spi3_d1 | | 1 | IO | | | | | | | | | 0 |
| | | uart5_rxd | | 2 | I | | | | | | | | | 1 |
| | | vin2b_d5 | | 4 | I | | | | | | | | | 0 |
| | | vin5a_d5 | | 9 | I | | | | | | | | | 0 |
| | | eQEP3A_in | | 10 | I | | | | | | | | | 0 |
| | | pr2_mii1_txd1 | | 11 | O | | | | | | | | | |
| | | pr2_pru0_gpi4 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo4 | | 13 | O | | | | | | | | | |
| | | gpio6_31 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AC6 | mmc3_dat1 | mmc3_dat1 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | spi3_d0 | | 1 | IO | | | | | | | | | 0 |
| | | uart5_txd | | 2 | O | | | | | | | | | |
| | | vin2b_d4 | | 4 | I | | | | | | | | | 0 |
| | | vin5a_d4 | | 9 | I | | | | | | | | | 0 |
| | | eQEP3B_in | | 10 | I | | | | | | | | | 0 |
| | | pr2_mii1_txd0 | | 11 | O | | | | | | | | | |
| | | pr2_pru0_gpi5 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo5 | | 13 | O | | | | | | | | | |
| | | gpio7_0 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AC9 | mmc3_dat2 | mmc3_dat2 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | spi3_cs0 | | 1 | IO | | | | | | | | | 1 |
| | | uart5_ctsn | | 2 | I | | | | | | | | | 1 |
| | | vin2b_d3 | | 4 | I | | | | | | | | | 0 |
| | | vin5a_d3 | | 9 | I | | | | | | | | | 0 |
| | | eQEP3_index | | 10 | IO | | | | | | | | | 0 |
| | | pr2_mii_mr1_clk | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi6 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo6 | | 13 | O | | | | | | | | | |
| | | gpio7_1 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AC3 | mmc3_dat3 | mmc3_dat3 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | spi3_cs1 | | 1 | IO | | | | | | | | | 1 |
| | | uart5_rtsn | | 2 | O | | | | | | | | | |
| | | vin2b_d2 | | 4 | I | | | | | | | | | 0 |
| | | vin5a_d2 | | 9 | I | | | | | | | | | 0 |
| | | eQEP3_strobe | | 10 | IO | | | | | | | | | 0 |
| | | pr2_mii1_rxdv | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi7 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo7 | | 13 | O | | | | | | | | | |
| | | gpio7_2 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AC8 | mmc3_dat4 | mmc3_dat4 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | spi4_sclk | | 1 | IO | | | | | | | | | 0 |
| | | uart10_rxd | | 2 | I | | | | | | | | | 1 |
| | | vin2b_d1 | | 4 | I | | | | | | | | | 0 |
| | | vin5a_d1 | | 9 | I | | | | | | | | | 0 |
| | | ehrpwm3A | | 10 | O | | | | | | | | | |
| | | pr2_mii1_rxd3 | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi8 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo8 | | 13 | O | | | | | | | | | |
| | | gpio1_22 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AD6 | mmc3_dat5 | mmc3_dat5 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | spi4_d1 | | 1 | IO | | | | | | | | | 0 |
| | | uart10_txd | | 2 | O | | | | | | | | | |
| | | vin2b_d0 | | 4 | I | | | | | | | | | 0 |
| | | vin5a_d0 | | 9 | I | | | | | | | | | 0 |
| | | ehrpwm3B | | 10 | O | | | | | | | | | |
| | | pr2_mii1_rxd2 | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi9 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo9 | | 13 | O | | | | | | | | | |
| | | gpio1_23 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AB8 | mmc3_dat6 | mmc3_dat6 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | spi4_d0 | | 1 | IO | | | | | | | | | 0 |
| | | uart10_ctsn | | 2 | I | | | | | | | | | 1 |
| | | vin2b_de1 | | 4 | I | | | | | | | | | |
| | | vin5a_hsync0 | | 9 | I | | | | | | | | | 0 |
| | | ehrpwm3_tripzone_input | | 10 | IO | | | | | | | | | 0 |
| | | pr2_mii1_rxd1 | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi10 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo10 | | 13 | O | | | | | | | | | |
| | | gpio1_24 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AB5 | mmc3_dat7 | mmc3_dat7 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv7 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | spi4_cs0 | | 1 | IO | | | | | | | | | 1 |
| | | uart10_rtsn | | 2 | O | | | | | | | | | |
| | | vin2b_clk1 | | 4 | I | | | | | | | | | |
| | | vin5a_vsync0 | | 9 | I | | | | | | | | | 0 |
| | | eCAP3_in_PWM3_out | | 10 | IO | | | | | | | | | 0 |
| | | pr2_mii1_rxd0 | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi11 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo11 | | 13 | O | | | | | | | | | |
| | | gpio1_25 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| D21 | nmin_dsp | nmin_dsp | | 0 | I | PD | PD | | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| Y11 | on_off | on_off | | 0 | O | PU | drive 1 (OFF) | | 1.8/3.3 | vddshv5 | Yes | BC1833IHHV | PU/PD | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AG13 | pcie_rxn0 | pcie_rxn0 | | 0 | I | OFF | OFF | | 1.8 | vdda_pcie0 | | SERDES | | |
| AG11 | pcie_rxn1 | pcie_rxn1 | | 0 | I | OFF | OFF | | 1.8 | vdda_pcie1 | | SERDES | | |
| AH13 | pcie_rxp0 | pcie_rxp0 | | 0 | I | OFF | OFF | | 1.8 | vdda_pcie0 | | SERDES | | |
| AH11 | pcie_rxp1 | pcie_rxp1 | | 0 | I | OFF | OFF | | 1.8 | vdda_pcie1 | | SERDES | | |
| AG14 | pcie_txn0 | pcie_txn0 | | 0 | O | | | | 1.8 | vdda_pcie0 | | SERDES | | |
| AG12 | pcie_txn1 | pcie_txn1 | | 0 | O | | | | 1.8 | vdda_pcie1 | | SERDES | | |
| AH14 | pcie_txp0 | pcie_txp0 | | 0 | O | | | | 1.8 | vdda_pcie0 | | SERDES | | |
| AH12 | pcie_txp1 | pcie_txp1 | | 0 | O | | | | 1.8 | vdda_pcie1 | | SERDES | | |
| F22 | porz | porz | | 0 | I | | | | 1.8/3.3 | vddshv3 | Yes | IHHV1833 | PU/PD | |
| E23 | resetn | resetn | | 0 | I | PU | PU | | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| U5 | rgmii0_rxc | rgmii0_rxc | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | rmii1_txen | | 2 | O | | | | | | | | | |
| | | mii0_txclk | | 3 | I | | | | | | | | | 0 |
| | | vin2a_d5 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d5 | | 5 | I | | | | | | | | | 0 |
| | | pr1_mii_mt0_clk | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi11 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo11 | | 13 | O | | | | | | | | | |
| | | gpio5_26 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| V5 | rgmii0_rxctl | rgmii0_rxctl | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | rmii1_txd1 | | 2 | O | | | | | | | | | |
| | | mii0_txd3 | | 3 | O | | | | | | | | | |
| | | vin2a_d6 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d6 | | 5 | I | | | | | | | | | 0 |
| | | pr1_mii0_txd3 | | 11 | O | | | | | | | | | |
| | | pr2_pru1_gpi12 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo12 | | 13 | O | | | | | | | | | |
| | | gpio5_27 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W2 | rgmii0_rxd0 | rgmii0_rxd0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | rmii0_txd0 | | 1 | O | | | | | | | | | |
| | | mii0_txd0 | | 3 | O | | | | | | | | | |
| | | vin2a_fld0 | | 4 | I | | | | | | | | | |
| | | vin4b_fld1 | | 5 | I | | | | | | | | | 0 |
| | | pr1_mii0_txd0 | | 11 | O | | | | | | | | | |
| | | pr2_pru1_gpi16 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo16 | | 13 | O | | | | | | | | | |
| | | gpio5_31 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| Y2 | rgmii0_rxd1 | rgmii0_rxd1 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | rmii0_txd1 | | 1 | O | | | | | | | | | |
| | | mii0_txd1 | | 3 | O | | | | | | | | | |
| | | vin2a_d9 | | 4 | I | | | | | | | | | 0 |
| | | pr1_mii0_txd1 | | 11 | O | | | | | | | | | |
| | | pr2_pru1_gpi15 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo15 | | 13 | O | | | | | | | | | |
| | | gpio5_30 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| V3 | rgmii0_rxd2 | rgmii0_rxd2 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | rmii0_txen | | 1 | O | | | | | | | | | |
| | | mii0_txen | | 3 | O | | | | | | | | | |
| | | vin2a_d8 | | 4 | I | | | | | | | | | 0 |
| | | pr1_mii0_txen | | 11 | O | | | | | | | | | |
| | | pr2_pru1_gpi14 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo14 | | 13 | O | | | | | | | | | |
| | | gpio5_29 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| V4 | rgmii0_rxd3 | rgmii0_rxd3 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | rmii1_txd0 | | 2 | O | | | | | | | | | |
| | | mii0_txd2 | | 3 | O | | | | | | | | | |
| | | vin2a_d7 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d7 | | 5 | I | | | | | | | | | 0 |
| | | pr1_mii0_txd2 | | 11 | O | | | | | | | | | |
| | | pr2_pru1_gpi13 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo13 | | 13 | O | | | | | | | | | |
| | | gpio5_28 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| W9 | rgmii0_txc | rgmii0_txc | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | uart3_ctsn | | 1 | I | | | | | | | | | 1 |
| | | rmii1_rxd1 | | 2 | I | | | | | | | | | 0 |
| | | mii0_rxd3 | | 3 | I | | | | | | | | | 0 |
| | | vin2a_d3 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d3 | | 5 | I | | | | | | | | | 0 |
| | | spi3_d0 | | 7 | IO | | | | | | | | | 0 |
| | | spi4_cs2 | | 8 | IO | | | | | | | | | 1 |
| | | pr1_mii0_rxd3 | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi5 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo5 | | 13 | O | | | | | | | | | |
| | | gpio5_20 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| V9 | rgmii0_txctl | rgmii0_txctl | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | uart3_rtsn | | 1 | O | | | | | | | | | |
| | | rmii1_rxd0 | | 2 | I | | | | | | | | | 0 |
| | | mii0_rxd2 | | 3 | I | | | | | | | | | 0 |
| | | vin2a_d4 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d4 | | 5 | I | | | | | | | | | 0 |
| | | spi3_cs0 | | 7 | IO | | | | | | | | | 1 |
| | | spi4_cs3 | | 8 | IO | | | | | | | | | 1 |
| | | pr1_mii0_rxd2 | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi6 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo6 | | 13 | O | | | | | | | | | |
| | | gpio5_21 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| U6 | rgmii0_txd0 | rgmii0_txd0 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | rmii0_rxd0 | | 1 | I | | | | | | | | | 0 |
| | | mii0_rxd0 | | 3 | I | | | | | | | | | 0 |
| | | vin2a_d10 | | 4 | I | | | | | | | | | 0 |
| | | spi4_cs0 | | 7 | IO | | | | | | | | | 1 |
| | | uart4_rtsn | | 8 | O | | | | | | | | | |
| | | pr1_mii0_rxd0 | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi10 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo10 | | 13 | O | | | | | | | | | |
| | | gpio5_25 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| V6 | rgmii0_txd1 | rgmii0_txd1 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | rmii0_rxd1 | | 1 | I | | | | | | | | | 0 |
| | | mii0_rxd1 | | 3 | I | | | | | | | | | 0 |
| | | vin2a_vsync0 | | 4 | I | | | | | | | | | |
| | | vin4b_vsync1 | | 5 | I | | | | | | | | | 0 |
| | | spi4_d0 | | 7 | IO | | | | | | | | | 0 |
| | | uart4_ctsn | | 8 | IO | | | | | | | | | 1 |
| | | pr1_mii0_rxd1 | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi9 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo9 | | 13 | O | | | | | | | | | |
| | | gpio5_24 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| U7 | rgmii0_txd2 | rgmii0_txd2 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | rmii0_rxer | | 1 | I | | | | | | | | | 0 |
| | | mii0_rxer | | 3 | I | | | | | | | | | 0 |
| | | vin2a_hsync0 | | 4 | I | | | | | | | | | |
| | | vin4b_hsync1 | | 5 | I | | | | | | | | | 0 |
| | | spi4_d1 | | 7 | IO | | | | | | | | | 0 |
| | | uart4_txd | | 8 | O | | | | | | | | | |
| | | pr1_mii0_rxer | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi8 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo8 | | 13 | O | | | | | | | | | |
| | | gpio5_23 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| V7 | rgmii0_txd3 | rgmii0_txd3 | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | rmii0_crs | | 1 | I | | | | | | | | | 0 |
| | | mii0_crs | | 3 | I | | | | | | | | | 0 |
| | | vin2a_de0 | | 4 | I | | | | | | | | | |
| | | vin4b_de1 | | 5 | I | | | | | | | | | 0 |
| | | spi4_sclk | | 7 | IO | | | | | | | | | 0 |
| | | uart4_rxd | | 8 | I | | | | | | | | | 1 |
| | | pr1_mii0_crs | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi7 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo7 | | 13 | O | | | | | | | | | |
| | | gpio5_22 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| U3 | RMII_MHZ_50_CLK | RMII_MHZ_50_CLK | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin2a_d11 | | 4 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi2 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo2 | | 13 | O | | | | | | | | | |
| | | gpio5_17 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| F23 | rstoutn | rstoutn | | 0 | O | PD | drive 1 (OFF) | | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| E18 | rtck | rtck | | 0 | O | PU | drive clk (OFF) | 0 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | gpio8_29 | | 14 | IO | | | | | | | | | |
| AF14 | rtc_iso | rtc_iso | | 0 | I | | | | 1.8/3.3 | vddshv5 | Yes | IHHV1833 | PU/PD | |
| AE14 | rtc_osc_xi_clkin32 | rtc_osc_xi_clkin32 | | 0 | I | | | | 1.8 | vdda_rtc | No | LVCMOS OSC | | |
| AD14 | rtc_osc_xo | rtc_osc_xo | | 0 | O | | | | 1.8 | vdda_rtc | No | LVCMOS OSC | | |
| AB17 | rtc_porz | rtc_porz | | 0 | I | | | | 1.8/3.3 | vddshv5 | Yes | IHHV1833 | PU/PD | |
| AH9 | sata1_rxn0 | sata1_rxn0 | | 0 | I | OFF | OFF | | 1.8 | vdda_sata | | SATAPHY | | |
| AG9 | sata1_rxp0 | sata1_rxp0 | | 0 | I | OFF | OFF | | 1.8 | vdda_sata | | SATAPHY | | |
| AG10 | sata1_txn0 | sata1_txn0 | | 0 | O | | | | 1.8 | vdda_sata | | SATAPHY | | |
| AH10 | sata1_txp0 | sata1_txp0 | | 0 | O | | | | 1.8 | vdda_sata | | SATAPHY | | |
| A24 | spi1_cs0 | spi1_cs0 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | gpio7_10 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A22 | spi1_cs1 | spi1_cs1 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | sata1_led | | 2 | O | | | | | | | | | |
| | | spi2_cs1 | | 3 | IO | | | | | | | | | 1 |
| | | gpio7_11 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B21 | spi1_cs2 | spi1_cs2 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | uart4_rxd | | 1 | I | | | | | | | | | 1 |
| | | mmc3_sdcd | | 2 | I | | | | | | | | | 1 |
| | | spi2_cs2 | | 3 | IO | | | | | | | | | 1 |
| | | dcan2_tx | | 4 | IO | | | | | | | | | 1 |
| | | mdio_mclk | | 5 | O | | | | | | | | | 1 |
| | | hdmi1_hpd | No | 6 | I | | | | | | | | | |
| | | gpio7_12 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B20 | spi1_cs3 | spi1_cs3 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | uart4_txd | | 1 | O | | | | | | | | | |
| | | mmc3_sdwp | | 2 | I | | | | | | | | | 0 |
| | | spi2_cs3 | | 3 | IO | | | | | | | | | 1 |
| | | dcan2_rx | | 4 | IO | | | | | | | | | 1 |
| | | mdio_d | | 5 | IO | | | | | | | | | 1 |
| | | hdmi1_cec | No | 6 | IO | | | | | | | | | |
| | | gpio7_13 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B25 | spi1_d0 | spi1_d0 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | gpio7_9 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| F16 | spi1_d1 | spi1_d1 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | gpio7_8 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A25 | spi1_sclk | spi1_sclk | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | gpio7_7 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B24 | spi2_cs0 | spi2_cs0 | | 0 | IO | PU | PU | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | uart3_rtsn | | 1 | O | | | | | | | | | |
| | | uart5_txd | | 2 | O | | | | | | | | | |
| | | gpio7_17 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G17 | spi2_d0 | spi2_d0 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | uart3_ctsn | | 1 | I | | | | | | | | | 1 |
| | | uart5_rxd | | 2 | I | | | | | | | | | 1 |
| | | gpio7_16 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B22 | spi2_d1 | spi2_d1 | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | uart3_txd | | 1 | O | | | | | | | | | |
| | | gpio7_15 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A26 | spi2_sclk | spi2_sclk | | 0 | IO | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | uart3_rxd | | 1 | I | | | | | | | | | 1 |
| | | gpio7_14 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| E20 | tclk | tclk | | 0 | I | PU | PU | 0 | 1.8/3.3 | vddshv3 | Yes | IQ1833 | PU/PD | |
| D23 | tdi | tdi | | 0 | I | PU | PU | 0 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | gpio8_27 | | 14 | I | | | | | | | | | |
| F19 | tdo | tdo | | 0 | O | PU | PU | 0 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | gpio8_28 | | 14 | IO | | | | | | | | | |
| F18 | tms | tms | | 0 | IO | OFF | OFF | 0 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| D20 | trstn | trstn | | 0 | I | PD | PD | | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| E25 | uart1_ctsn | uart1_ctsn | | 0 | I | PU | PU | 15 | 1.8/3.3 | vddshv4 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | uart9_rxd | | 2 | I | | | | | | | | | 1 |
| | | mmc4_clk | | 3 | IO | | | | | | | | | 1 |
| | | gpio7_24 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| C27 | uart1_rtsn | uart1_rtsn | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv4 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | uart9_txd | | 2 | O | | | | | | | | | |
| | | mmc4_cmd | | 3 | IO | | | | | | | | | 1 |
| | | gpio7_25 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B27 | uart1_rxd | uart1_rxd | | 0 | I | PU | PU | 15 | 1.8/3.3 | vddshv4 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | mmc4_sdcd | | 3 | I | | | | | | | | | 1 |
| | | gpio7_22 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C26 | uart1_txd | uart1_txd | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv4 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mmc4_sdwp | | 3 | I | | | | | | | | | 0 |
| | | gpio7_23 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| D27 | uart2_ctsn | uart2_ctsn | | 0 | I | PU | PU | 15 | 1.8/3.3 | vddshv4 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | uart3_rxd | | 2 | I | | | | | | | | | 1 |
| | | mmc4_dat2 | | 3 | IO | | | | | | | | | 1 |
| | | uart10_rxd | | 4 | I | | | | | | | | | 1 |
| | | uart1_dtrn | | 5 | O | | | | | | | | | |
| | | gpio1_16 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| C28 | uart2_rtsn | uart2_rtsn | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv4 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | uart3_txd | | 1 | O | | | | | | | | | |
| | | uart3_irtx | | 2 | O | | | | | | | | | |
| | | mmc4_dat3 | | 3 | IO | | | | | | | | | 1 |
| | | uart10_txd | | 4 | O | | | | | | | | | |
| | | uart1_rin | | 5 | I | | | | | | | | | 1 |
| | | gpio1_17 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| D28 | uart2_rxd | uart3_ctsn | | 1 | I | PU | PU | 15 | 1.8/3.3 | vddshv4 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | uart3_rctx | | 2 | O | | | | | | | | | |
| | | mmc4_dat0 | | 3 | IO | | | | | | | | | 1 |
| | | uart2_rxd | | 4 | I | | | | | | | | | 1 |
| | | uart1_dcdn | | 5 | I | | | | | | | | | 1 |
| | | gpio7_26 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| D26 | uart2_txd | uart2_txd | | 0 | O | PU | PU | 15 | 1.8/3.3 | vddshv4 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | uart3_rtsn | | 1 | O | | | | | | | | | |
| | | uart3_sd | | 2 | O | | | | | | | | | |
| | | mmc4_dat1 | | 3 | IO | | | | | | | | | 1 |
| | | uart2_txd | | 4 | O | | | | | | | | | |
| | | uart1_dsrn | | 5 | I | | | | | | | | | 0 |
| | | gpio7_27 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| V2 | uart3_rxd | uart3_rxd | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | 1 |
| | | rmii1_crs | | 2 | I | | | | | | | | | 0 |
| | | mii0_rxdv | | 3 | I | | | | | | | | | 0 |
| | | vin2a_d1 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d1 | | 5 | I | | | | | | | | | 0 |
| | | spi3_sclk | | 7 | IO | | | | | | | | | 0 |
| | | pr1_mii0_rxdv | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi3 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo3 | | 13 | O | | | | | | | | | |
| | | gpio5_18 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| Y1 | uart3_txd | uart3_txd | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv9 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | rmii1_rxer | | 2 | I | | | | | | | | | 0 |
| | | mii0_rxclk | | 3 | I | | | | | | | | | 0 |
| | | vin2a_d2 | | 4 | I | | | | | | | | | 0 |
| | | vin4b_d2 | | 5 | I | | | | | | | | | 0 |
| | | spi3_d1 | | 7 | IO | | | | | | | | | 0 |
| | | spi4_cs1 | | 8 | IO | | | | | | | | | 1 |
| | | pr1_mii_mr0_clk | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi4 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo4 | | 13 | O | | | | | | | | | |
| | | gpio5_19 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AC12 | usb1_dm | usb1_dm | | 0 | IO | OFF | OFF | | 3.3 | vdda33v_usb1 | | USB3PHY | | |
| AD12 | usb1_dp | usb1_dp | | 0 | IO | OFF | OFF | | 3.3 | vdda33v_usb1 | | USB3PHY | | |
| AB10 | usb1_drvvbus | usb1_drvvbus | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | timer16 | | 7 | IO | | | | | | | | | |
| | | gpio6_12 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AF11 | usb2_dm | usb2_dm | | 0 | IO | | | | 3.3 | vdda33v_usb2 | No | USB2PHY | | |
| AE11 | usb2_dp | usb2_dp | | 0 | IO | | | | 3.3 | vdda33v_usb2 | No | USB2PHY | | |
| AC10 | usb2_drvvbus | usb2_drvvbus | | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | timer15 | | 7 | IO | | | | | | | | | |
| | | gpio6_13 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AF12 | usb_rxn0 | usb_rxn0 | | 0 | I | OFF | OFF | | 1.8 | vdda_usb1 | | | | |
| AE12 | usb_rxp0 | usb_rxp0 | | 0 | I | OFF | OFF | | 1.8 | vdda_usb1 | | | | |
| AC11 | usb_txn0 | usb_txn0 | | 0 | O | | | | 1.8 | vdda_usb1 | | | | |
| AD11 | usb_txp0 | usb_txp0 | | 0 | O | | | | 1.8 | vdda_usb1 | | | | |
| H13, H14, J17, J18, L7, L8, N10, N13, P11, P12, P13, R11, R16, R19, T13, T16, T19, U13, U16, U8, U9, V16, V8 | vdd | vdd | | | PWR | | | | | | | | | |
| AA12 | vdda33v_usb1 | vdda33v_usb1 | | | PWR | | | | | | | | | |
| Y12 | vdda33v_usb2 | vdda33v_usb2 | | | PWR | | | | | | | | | |
| M14 | vdda_abe_per | vdda_abe_per | | | PWR | | | | | | | | | |
| P16 | vdda_ddr | vdda_ddr | | | PWR | | | | | | | | | |
| N11 | vdda_debug | vdda_debug | | | PWR | | | | | | | | | |
| N12 | vdda_dsp_eve | vdda_dsp_eve | | | PWR | | | | | | | | | |
| P15 | vdda_gmac_core | vdda_gmac_core | | | PWR | | | | | | | | | |
| R14 | vdda_gpu | vdda_gpu | | | PWR | | | | | | | | | |
| Y17 | vdda_hdmi | vdda_hdmi | | | PWR | | | | | | | | | |
| R17 | vdda_iva | vdda_iva | | | PWR | | | | | | | | | |
| N16 | vdda_mpu | vdda_mpu | | | PWR | | | | | | | | | |
| AD16, AE16 | vdda_osc | vdda_osc | | | PWR | | | | | | | | | |
| W14 | vdda_pcie | vdda_pcie | | | PWR | | | | | | | | | |
| AA17 | vdda_pcie0 | vdda_pcie0 | | | PWR | | | | | | | | | |
| AA16 | vdda_pcie1 | vdda_pcie1 | | | PWR | | | | | | | | | |
| AB13 | vdda_rtc | vdda_rtc | | | PWR | | | | | | | | | |
| V13 | vdda_sata | vdda_sata | | | PWR | | | | | | | | | |
| AA13 | vdda_usb1 | vdda_usb1 | | | PWR | | | | | | | | | |
| AB12 | vdda_usb2 | vdda_usb2 | | | PWR | | | | | | | | | |
| W12 | vdda_usb3 | vdda_usb3 | | | PWR | | | | | | | | | |
| P14 | vdda_video | vdda_video | | | PWR | | | | | | | | | |
| G18, H17, M8, M9, N8, P8, R8, T8, V21, V22, W17, W18 | vdds18v | vdds18v | | | PWR | | | | | | | | | |
| AA18, AA19, W21, Y21 | vdds18v_ddr1 | vdds18v_ddr1 | | | PWR | | | | | | | | | |
| J21, J22, N21, P20, P21 | vdds18v_ddr2 | vdds18v_ddr2 | | | PWR | | | | | | | | | |
| E3, E5, G4, G5, H8, H9 | vddshv1 | vddshv1 | | | PWR | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N4, N5, P10, R10, R7, T4, T5 | vddshv10 | vddshv10 | | | PWR | | | | | | | | | |
| J8, K8 | vddshv11 | vddshv11 | | | PWR | | | | | | | | | |
| B6, D10, E10, H10, H11 | vddshv2 | vddshv2 | | | PWR | | | | | | | | | |
| B23, D16, D22, E16, E22, G15, H15, H16, H18, H19 | vddshv3 | vddshv3 | | | PWR | | | | | | | | | |
| C24 | vddshv4 | vddshv4 | | | PWR | | | | | | | | | |
| V12 | vddshv5 | vddshv5 | | | PWR | | | | | | | | | |
| AD5, AD7, AE7, AF5 | vddshv6 | vddshv6 | | | PWR | | | | | | | | | |
| AB6, AB7 | vddshv7 | vddshv7 | | | PWR | | | | | | | | | |
| W8, Y8 | vddshv8 | vddshv8 | | | PWR | | | | | | | | | |
| U10, W4, W5 | vddshv9 | vddshv9 | | | PWR | | | | | | | | | |
| AA21, AA22, AB21, AB22, AB24, AB25, AC22, AD26, AG20, AG28, AH27, W16, W27 | vdds_ddr1 | vdds_ddr1 | | | PWR | | | | | | | | | |
| E24, G22, G23, H20, H21, H22, J27, L20, L21, M20, M21, T24, T25 | vdds_ddr2 | vdds_ddr2 | | | PWR | | | | | | | | | |
| AA7, Y7 | vdds_mlbp | vdds_mlbp | | | PWR | | | | | | | | | |
| J13, K10, K11, K12, K13, L10, L11, L12, M10, M11, M12, M13 | vdd_dspeve | vdd_dspeve | | | PWR | | | | | | | | | |
| U11, U12, V10, V11, V14, W10, W11, W13 | vdd_gpu | vdd_gpu | | | PWR | | | | | | | | | |
| U18, U19, V18, V19 | vdd_iva | vdd_iva | | | PWR | | | | | | | | | |
| K17, K18, L15, L16, L17, L18, L19, M15, M16, M17, M18, N17, N18, P17, P18, R18 | vdd_mpu | vdd_mpu | | | PWR | | | | | | | | | |
| AB15 | vdd_rtc | vdd_rtc | | | PWR | | | | | | | | | |
| AG8 | vin1a_clk0 | vin1a_clk0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout3_d16 [(8)] | No | 3 | O | | | | | | | | | |
| | | vout3_fld [(8)] | No | 4 | O | | | | | | | | | |
| | | gpio2_30 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AE8 | vin1a_d0 | vin1a_d0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout3_d7 [(8)] | No | 3 | O | | | | | | | | | |
| | | vout3_d23 [(8)] | No | 4 | O | | | | | | | | | |
| | | uart8_rxd | | 5 | I | | | | | | | | | 1 |
| | | ehrpwm1A | | 10 | O | | | | | | | | | |
| | | gpio3_4 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AD8 | vin1a_d1 | vin1a_d1 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout3_d6 [(8)] | No | 3 | O | | | | | | | | | |
| | | vout3_d22 [(8)] | No | 4 | O | | | | | | | | | |
| | | uart8_txd | | 5 | O | | | | | | | | | |
| | | ehrpwm1B | | 10 | O | | | | | | | | | |
| | | gpio3_5 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AG3 | vin1a_d10 | vin1a_d10 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d5 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d13 [(8)] | No | 4 | O | | | | | | | | | |
| | | kbd_row4 | | 9 | I | | | | | | | | | 0 |
| | | pr1_edc_latch0_in | | 10 | I | | | | | | | | | 0 |
| | | pr1_pru0_gpi7 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo7 | | 13 | O | | | | | | | | | |
| | | gpio3_14 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AG5 | vin1a_d11 | vin1a_d11 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d4 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d12 [(8)] | No | 4 | O | | | | | | | | | |
| | | gpmc_a23 | | 5 | O | | | | | | | | | |
| | | kbd_row5 | | 9 | I | | | | | | | | | 0 |
| | | pr1_edc_latch1_in | | 10 | I | | | | | | | | | 0 |
| | | pr1_pru0_gpi8 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo8 | | 13 | O | | | | | | | | | |
| | | gpio3_15 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AF2 | vin1a_d12 | vin1a_d12 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d3 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d11 [(8)] | No | 4 | O | | | | | | | | | |
| | | gpmc_a24 | | 5 | O | | | | | | | | | |
| | | kbd_row6 | | 9 | I | | | | | | | | | 0 |
| | | pr1_edc_sync0_out | | 10 | O | | | | | | | | | |
| | | pr1_pru0_gpi9 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo9 | | 13 | O | | | | | | | | | |
| | | gpio3_16 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AF6 | vin1a_d13 | vin1a_d13 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d2 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d10 [(8)] | No | 4 | O | | | | | | | | | |
| | | gpmc_a25 | | 5 | O | | | | | | | | | |
| | | kbd_row7 | | 9 | I | | | | | | | | | 0 |
| | | pr1_edc_sync1_out | | 10 | O | | | | | | | | | |
| | | pr1_pru0_gpi10 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo10 | | 13 | O | | | | | | | | | |
| | | gpio3_17 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AF3 | vin1a_d14 | vin1a_d14 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d1 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d9 [(8)] | No | 4 | O | | | | | | | | | |
| | | gpmc_a26 | | 5 | O | | | | | | | | | |
| | | kbd_row8 | | 9 | I | | | | | | | | | 0 |
| | | pr1_edio_latch_in | | 10 | I | | | | | | | | | 0 |
| | | pr1_pru0_gpi11 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo11 | | 13 | O | | | | | | | | | |
| | | gpio3_18 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AF4 | vin1a_d15 | vin1a_d15 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d0 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d8 [(8)] | No | 4 | O | | | | | | | | | |
| | | gpmc_a27 | | 5 | O | | | | | | | | | |
| | | kbd_col0 | | 9 | O | | | | | | | | | |
| | | pr1_edio_sof | | 10 | O | | | | | | | | | |
| | | pr1_pru0_gpi12 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo12 | | 13 | O | | | | | | | | | |
| | | gpio3_19 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AF1 | vin1a_d16 | vin1a_d16 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d7 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d7 [(8)] | No | 4 | O | | | | | | | | | |
| | | vin3a_d0 | | 6 | I | | | | | | | | | 0 |
| | | kbd_col1 | | 9 | O | | | | | | | | | |
| | | pr1_edio_data_in0 | | 10 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out0 | | 11 | O | | | | | | | | | |
| | | pr1_pru0_gpi13 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo13 | | 13 | O | | | | | | | | | |
| | | gpio3_20 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AE3 | vin1a_d17 | vin1a_d17 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d6 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d6 [(8)] | No | 4 | O | | | | | | | | | |
| | | vin3a_d1 | | 6 | I | | | | | | | | | 0 |
| | | kbd_col2 | | 9 | O | | | | | | | | | |
| | | pr1_edio_data_in1 | | 10 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out1 | | 11 | O | | | | | | | | | |
| | | pr1_pru0_gpi14 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo14 | | 13 | O | | | | | | | | | |
| | | gpio3_21 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AE5 | vin1a_d18 | vin1a_d18 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d5 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d5 [(8)] | No | 4 | O | | | | | | | | | |
| | | vin3a_d2 | | 6 | I | | | | | | | | | 0 |
| | | kbd_col3 | | 9 | O | | | | | | | | | |
| | | pr1_edio_data_in2 | | 10 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out2 | | 11 | O | | | | | | | | | |
| | | pr1_pru0_gpi15 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo15 | | 13 | O | | | | | | | | | |
| | | gpio3_22 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AE1 | vin1a_d19 | vin1a_d19 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d4 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d4 [(8)] | No | 4 | O | | | | | | | | | |
| | | vin3a_d3 | | 6 | I | | | | | | | | | 0 |
| | | kbd_col4 | | 9 | O | | | | | | | | | |
| | | pr1_edio_data_in3 | | 10 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out3 | | 11 | O | | | | | | | | | |
| | | pr1_pru0_gpi16 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo16 | | 13 | O | | | | | | | | | |
| | | gpio3_23 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AG7 | vin1a_d2 | vin1a_d2 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout3_d5 [(8)] | No | 3 | O | | | | | | | | | |
| | | vout3_d21 [(8)] | No | 4 | O | | | | | | | | | |
| | | uart8_ctsn | | 5 | I | | | | | | | | | 1 |
| | | ehrpwm1_tripzone_input | | 10 | IO | | | | | | | | | 0 |
| | | gpio3_6 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AE2 | vin1a_d20 | vin1a_d20 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d3 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d3 [(8)] | No | 4 | O | | | | | | | | | |
| | | vin3a_d4 | | 6 | I | | | | | | | | | 0 |
| | | kbd_col5 | | 9 | O | | | | | | | | | |
| | | pr1_edio_data_in4 | | 10 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out4 | | 11 | O | | | | | | | | | |
| | | pr1_pru0_gpi17 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo17 | | 13 | O | | | | | | | | | |
| | | gpio3_24 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AE6 | vin1a_d21 | vin1a_d21 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d2 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d2 [(8)] | No | 4 | O | | | | | | | | | |
| | | vin3a_d5 | | 6 | I | | | | | | | | | 0 |
| | | kbd_col6 | | 9 | O | | | | | | | | | |
| | | pr1_edio_data_in5 | | 10 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out5 | | 11 | O | | | | | | | | | |
| | | pr1_pru0_gpi18 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo18 | | 13 | O | | | | | | | | | |
| | | gpio3_25 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AD2 | vin1a_d22 | vin1a_d22 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d1 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d1 [(8)] | No | 4 | O | | | | | | | | | |
| | | vin3a_d6 | | 6 | I | | | | | | | | | 0 |
| | | kbd_col7 | | 9 | O | | | | | | | | | |
| | | pr1_edio_data_in6 | | 10 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out6 | | 11 | O | | | | | | | | | |
| | | pr1_pru0_gpi19 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo19 | | 13 | O | | | | | | | | | |
| | | gpio3_26 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AD3 | vin1a_d23 | vin1a_d23 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d0 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d0 [(8)] | No | 4 | O | | | | | | | | | |
| | | vin3a_d7 | | 6 | I | | | | | | | | | 0 |
| | | kbd_col8 | | 9 | O | | | | | | | | | |
| | | pr1_edio_data_in7 | | 10 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out7 | | 11 | O | | | | | | | | | |
| | | pr1_pru0_gpi20 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo20 | | 13 | O | | | | | | | | | |
| | | gpio3_27 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AH6 | vin1a_d3 | vin1a_d3 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout3_d4 [(8)] | No | 3 | O | | | | | | | | | |
| | | vout3_d20 [(8)] | No | 4 | O | | | | | | | | | |
| | | uart8_rtsn | | 5 | O | | | | | | | | | |
| | | eCAP1_in_PWM1_out | | 10 | IO | | | | | | | | | 0 |
| | | pr1_pru0_gpi0 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo0 | | 13 | O | | | | | | | | | |
| | | gpio3_7 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AH3 | vin1a_d4 | vin1a_d4 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout3_d3 [(8)] | No | 3 | O | | | | | | | | | |
| | | vout3_d19 [(8)] | No | 4 | O | | | | | | | | | |
| | | ehrpwm1_synci | | 10 | I | | | | | | | | | 0 |
| | | pr1_pru0_gpi1 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo1 | | 13 | O | | | | | | | | | |
| | | gpio3_8 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AH5 | vin1a_d5 | vin1a_d5 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout3_d2 [(8)] | No | 3 | O | | | | | | | | | |
| | | vout3_d18 [(8)] | No | 4 | O | | | | | | | | | |
| | | ehrpwm1_synco | | 10 | O | | | | | | | | | |
| | | pr1_pru0_gpi2 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo2 | | 13 | O | | | | | | | | | |
| | | gpio3_9 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AG6 | vin1a_d6 | vin1a_d6 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout3_d1 [(8)] | No | 3 | O | | | | | | | | | |
| | | vout3_d17 [(8)] | No | 4 | O | | | | | | | | | |
| | | eQEP2A_in | | 10 | I | | | | | | | | | 0 |
| | | pr1_pru0_gpi3 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo3 | | 13 | O | | | | | | | | | |
| | | gpio3_10 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AH4 | vin1a_d7 | vin1a_d7 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout3_d0[(8)] | No | 3 | O | | | | | | | | | |
| | | vout3_d16 [(8)] | No | 4 | O | | | | | | | | | |
| | | eQEP2B_in | | 10 | I | | | | | | | | | 0 |
| | | pr1_pru0_gpi4 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo4 | | 13 | O | | | | | | | | | |
| | | gpio3_11 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AG4 | vin1a_d8 | vin1a_d8 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d7 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d15 [(8)] | No | 4 | O | | | | | | | | | |
| | | kbd_row2 | | 9 | I | | | | | | | | | 0 |
| | | eQEP2_index | | 10 | IO | | | | | | | | | 0 |
| | | pr1_pru0_gpi5 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo5 | | 13 | O | | | | | | | | | |
| | | gpio3_12 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AG2 | vin1a_d9 | vin1a_d9 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_d6 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d14 [(8)] | No | 4 | O | | | | | | | | | |
| | | kbd_row3 | | 9 | I | | | | | | | | | 0 |
| | | eQEP2_strobe | | 10 | IO | | | | | | | | | 0 |
| | | pr1_pru0_gpi6 | | 12 | I | | | | | | | | | |
| | | pr1_pru0_gpo6 | | 13 | O | | | | | | | | | |
| | | gpio3_13 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AD9 | vin1a_de0 | vin1a_de0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_hsync1 | | 1 | I | | | | | | | | | 0 |
| | | vout3_d17 [(8)] | No | 3 | O | | | | | | | | | |
| | | vout3_de [(8)] | No | 4 | O | | | | | | | | | |
| | | uart7_rxd | | 5 | I | | | | | | | | | 1 |
| | | timer16 | | 7 | IO | | | | | | | | | |
| | | spi3_sclk | | 8 | IO | | | | | | | | | 0 |
| | | kbd_row0 | | 9 | I | | | | | | | | | 0 |
| | | eQEP1A_in | | 10 | I | | | | | | | | | 0 |
| | | gpio3_0 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AF9 | vin1a_fld0 | vin1a_fld0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_vsync1 | | 1 | I | | | | | | | | | 0 |
| | | vout3_clk [(8)] | No | 4 | O | | | | | | | | | |
| | | uart7_txd | | 5 | O | | | | | | | | | |
| | | timer15 | | 7 | IO | | | | | | | | | |
| | | spi3_d1 | | 8 | IO | | | | | | | | | 0 |
| | | kbd_row1 | | 9 | I | | | | | | | | | 0 |
| | | eQEP1B_in | | 10 | I | | | | | | | | | 0 |
| | | gpio3_1 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AE9 | vin1a_hsync0 | vin1a_hsync0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_fld1 | | 1 | I | | | | | | | | | 0 |
| | | vout3_hsync [(8)] | No | 4 | O | | | | | | | | | |
| | | uart7_ctsn | | 5 | I | | | | | | | | | 1 |
| | | timer14 | | 7 | IO | | | | | | | | | |
| | | spi3_d0 | | 8 | IO | | | | | | | | | 0 |
| | | eQEP1_index | | 10 | IO | | | | | | | | | 0 |
| | | gpio3_2 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AF8 | vin1a_vsync0 | vin1a_vsync0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin1b_de1 | | 1 | I | | | | | | | | | 0 |
| | | vout3_vsync [(8)] | No | 4 | O | | | | | | | | | |
| | | uart7_rtsn | | 5 | O | | | | | | | | | |
| | | timer13 | | 7 | IO | | | | | | | | | |
| | | spi3_cs0 | | 8 | IO | | | | | | | | | 1 |
| | | eQEP1_strobe | | 10 | IO | | | | | | | | | 0 |
| | | gpio3_3 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AH7 | vin1b_clk1 | vin1b_clk1 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv6 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin3a_clk0 | | 6 | I | | | | | | | | | 0 |
| | | gpio2_31 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| E1 | vin2a_clk0 | vin2a_clk0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vout2_fld | No | 4 | O | | | | | | | | | |
| | | emu5 | | 5 | O | | | | | | | | | |
| | | kbd_row0 | | 9 | I | | | | | | | | | 0 |
| | | eQEP1A_in | | 10 | I | | | | | | | | | 0 |
| | | pr1_edio_data_in0 | | 12 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out0 | | 13 | O | | | | | | | | | |
| | | gpio3_28 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| F2 | vin2a_d0 | vin2a_d0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout2_d23 | No | 4 | O | | | | | | | | | |
| | | emu10 | | 5 | O | | | | | | | | | |
| | | uart9_ctsn | | 7 | I | | | | | | | | | 1 |
| | | spi4_d0 | | 8 | IO | | | | | | | | | 0 |
| | | kbd_row4 | | 9 | I | | | | | | | | | 0 |
| | | ehrpwm1B | | 10 | O | | | | | | | | | |
| | | pr1_uart0_rxd | | 11 | I | | | | | | | | | 1 |
| | | pr1_edio_data_in5 | | 12 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out5 | | 13 | O | | | | | | | | | |
| | | gpio4_1 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F3 | vin2a_d1 | vin2a_d1 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout2_d22 | No | 4 | O | | | | | | | | | |
| | | emu11 | | 5 | O | | | | | | | | | |
| | | uart9_rtsn | | 7 | O | | | | | | | | | |
| | | spi4_cs0 | | 8 | IO | | | | | | | | | 1 |
| | | kbd_row5 | | 9 | I | | | | | | | | | 0 |
| | | ehrpwm1_tripzone_input | | 10 | IO | | | | | | | | | 0 |
| | | pr1_uart0_txd | | 11 | O | | | | | | | | | |
| | | pr1_edio_data_in6 | | 12 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out6 | | 13 | O | | | | | | | | | |
| | | gpio4_2 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| D3 | vin2a_d10 | vin2a_d10 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mdio_mclk | | 3 | O | | | | | | | | | 1 |
| | | vout2_d13 | No | 4 | O | | | | | | | | | |
| | | kbd_col7 | | 9 | O | | | | | | | | | |
| | | ehrpwm2B | | 10 | O | | | | | | | | | |
| | | pr1_mdio_mdclk | | 11 | O | | | | | | | | | |
| | | pr1_pru1_gpi7 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo7 | | 13 | O | | | | | | | | | |
| | | gpio4_11 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| F6 | vin2a_d11 | vin2a_d11 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | mdio_d | | 3 | IO | | | | | | | | | 1 |
| | | vout2_d12 | No | 4 | O | | | | | | | | | |
| | | kbd_row7 | | 9 | I | | | | | | | | | 0 |
| | | ehrpwm2_tripzone_input | | 10 | IO | | | | | | | | | 0 |
| | | pr1_mdio_data | | 11 | IO | | | | | | | | | 1 |
| | | pr1_pru1_gpi8 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo8 | | 13 | O | | | | | | | | | |
| | | gpio4_12 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D5 | vin2a_d12 | vin2a_d12 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | rgmii1_txc | | 3 | O | | | | | | | | | |
| | | vout2_d11 | No | 4 | O | | | | | | | | | |
| | | mii1_rxclk | | 8 | I | | | | | | | | | 0 |
| | | kbd_col8 | | 9 | O | | | | | | | | | |
| | | eCAP2_in_PWM2_out | | 10 | IO | | | | | | | | | 0 |
| | | pr1_mii1_txd1 | | 11 | O | | | | | | | | | |
| | | pr1_pru1_gpi9 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo9 | | 13 | O | | | | | | | | | |
| | | gpio4_13 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| C2 | vin2a_d13 | vin2a_d13 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | rgmii1_txctl | | 3 | O | | | | | | | | | |
| | | vout2_d10 | No | 4 | O | | | | | | | | | |
| | | mii1_rxdv | | 8 | I | | | | | | | | | 0 |
| | | kbd_row8 | | 9 | I | | | | | | | | | 0 |
| | | eQEP3A_in | | 10 | I | | | | | | | | | 0 |
| | | pr1_mii1_txd0 | | 11 | O | | | | | | | | | |
| | | pr1_pru1_gpi10 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo10 | | 13 | O | | | | | | | | | |
| | | gpio4_14 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| C3 | vin2a_d14 | vin2a_d14 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | rgmii1_txd3 | | 3 | O | | | | | | | | | |
| | | vout2_d9 | No | 4 | O | | | | | | | | | |
| | | mii1_txclk | | 8 | I | | | | | | | | | 0 |
| | | eQEP3B_in | | 10 | I | | | | | | | | | 0 |
| | | pr1_mii_mr1_clk | | 11 | I | | | | | | | | | 0 |
| | | pr1_pru1_gpi11 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo11 | | 13 | O | | | | | | | | | |
| | | gpio4_15 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[1] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C4 | vin2a_d15 | vin2a_d15 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | rgmii1_txd2 | | 3 | O | | | | | | | | | |
| | | vout2_d8 | No | 4 | O | | | | | | | | | |
| | | mii1_txd0 | | 8 | O | | | | | | | | | |
| | | eQEP3_index | | 10 | IO | | | | | | | | | 0 |
| | | pr1_mii1_rxdv | | 11 | I | | | | | | | | | 0 |
| | | pr1_pru1_gpi12 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo12 | | 13 | O | | | | | | | | | |
| | | gpio4_16 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B2 | vin2a_d16 | vin2a_d16 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin2b_d7 | | 2 | I | | | | | | | | | 0 |
| | | rgmii1_txd1 | | 3 | O | | | | | | | | | |
| | | vout2_d7 | No | 4 | O | | | | | | | | | |
| | | vin3a_d8 | | 6 | I | | | | | | | | | 0 |
| | | mii1_txd1 | | 8 | O | | | | | | | | | |
| | | eQEP3_strobe | | 10 | IO | | | | | | | | | 0 |
| | | pr1_mii1_rxd3 | | 11 | I | | | | | | | | | 0 |
| | | pr1_pru1_gpi13 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo13 | | 13 | O | | | | | | | | | |
| | | gpio4_24 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| D6 | vin2a_d17 | vin2a_d17 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin2b_d6 | | 2 | I | | | | | | | | | 0 |
| | | rgmii1_txd0 | | 3 | O | | | | | | | | | |
| | | vout2_d6 | No | 4 | O | | | | | | | | | |
| | | vin3a_d9 | | 6 | I | | | | | | | | | 0 |
| | | mii1_txd2 | | 8 | O | | | | | | | | | |
| | | ehrpwm3A | | 10 | O | | | | | | | | | |
| | | pr1_mii1_rxd2 | | 11 | I | | | | | | | | | 0 |
| | | pr1_pru1_gpi14 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo14 | | 13 | O | | | | | | | | | |
| | | gpio4_25 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C5 | vin2a_d18 | vin2a_d18 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin2b_d5 | | 2 | I | | | | | | | | | 0 |
| | | rgmii1_rxc | | 3 | I | | | | | | | | | 0 |
| | | vout2_d5 | No | 4 | O | | | | | | | | | |
| | | vin3a_d10 | | 6 | I | | | | | | | | | 0 |
| | | mii1_txd3 | | 8 | O | | | | | | | | | |
| | | ehrpwm3B | | 10 | O | | | | | | | | | |
| | | pr1_mii1_rxd1 | | 11 | I | | | | | | | | | 0 |
| | | pr1_pru1_gpi15 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo15 | | 13 | O | | | | | | | | | |
| | | gpio4_26 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A3 | vin2a_d19 | vin2a_d19 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin2b_d4 | | 2 | I | | | | | | | | | 0 |
| | | rgmii1_rxctl | | 3 | I | | | | | | | | | 0 |
| | | vout2_d4 | No | 4 | O | | | | | | | | | |
| | | vin3a_d11 | | 6 | I | | | | | | | | | 0 |
| | | mii1_txer | | 8 | O | | | | | | | | | 0 |
| | | ehrpwm3_tripzone_input | | 10 | IO | | | | | | | | | 0 |
| | | pr1_mii1_rxd0 | | 11 | I | | | | | | | | | 0 |
| | | pr1_pru1_gpi16 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo16 | | 13 | O | | | | | | | | | |
| | | gpio4_27 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| D1 | vin2a_d2 | vin2a_d2 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout2_d21 | No | 4 | O | | | | | | | | | |
| | | emu12 | | 5 | O | | | | | | | | | |
| | | uart10_rxd | | 8 | I | | | | | | | | | 1 |
| | | kbd_row6 | | 9 | I | | | | | | | | | 0 |
| | | eCAP1_in_PWM1_out | | 10 | IO | | | | | | | | | 0 |
| | | pr1_ecap0_ecap_capin_apwm_o | | 11 | IO | | | | | | | | | 0 |
| | | pr1_edio_data_in7 | | 12 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out7 | | 13 | O | | | | | | | | | |
| | | gpio4_3 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B3 | vin2a_d20 | vin2a_d20 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin2b_d3 | | 2 | I | | | | | | | | | 0 |
| | | rgmii1_rxd3 | | 3 | I | | | | | | | | | 0 |
| | | vout2_d3 | No | 4 | O | | | | | | | | | |
| | | vin3a_de0 | | 5 | I | | | | | | | | | 0 |
| | | vin3a_d12 | | 6 | I | | | | | | | | | 0 |
| | | mii1_rxer | | 8 | I | | | | | | | | | 0 |
| | | eCAP3_in_PWM3_out | | 10 | IO | | | | | | | | | 0 |
| | | pr1_mii1_rxer | | 11 | I | | | | | | | | | 0 |
| | | pr1_pru1_gpi17 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo17 | | 13 | O | | | | | | | | | |
| | | gpio4_28 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B4 | vin2a_d21 | vin2a_d21 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin2b_d2 | | 2 | I | | | | | | | | | 0 |
| | | rgmii1_rxd2 | | 3 | I | | | | | | | | | 0 |
| | | vout2_d2 | No | 4 | O | | | | | | | | | |
| | | vin3a_fld0 | | 5 | I | | | | | | | | | 0 |
| | | vin3a_d13 | | 6 | I | | | | | | | | | 0 |
| | | mii1_col | | 8 | I | | | | | | | | | 0 |
| | | pr1_mii1_rxlink | | 11 | I | | | | | | | | | 0 |
| | | pr1_pru1_gpi18 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo18 | | 13 | O | | | | | | | | | |
| | | gpio4_29 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B5 | vin2a_d22 | vin2a_d22 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin2b_d1 | | 2 | I | | | | | | | | | 0 |
| | | rgmii1_rxd1 | | 3 | I | | | | | | | | | 0 |
| | | vout2_d1 | No | 4 | O | | | | | | | | | |
| | | vin3a_hsync0 | | 5 | I | | | | | | | | | 0 |
| | | vin3a_d14 | | 6 | I | | | | | | | | | 0 |
| | | mii1_crs | | 8 | I | | | | | | | | | 0 |
| | | pr1_mii1_col | | 11 | I | | | | | | | | | 0 |
| | | pr1_pru1_gpi19 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo19 | | 13 | O | | | | | | | | | |
| | | gpio4_30 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A4 | vin2a_d23 | vin2a_d23 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vin2b_d0 | | 2 | I | | | | | | | | | 0 |
| | | rgmii1_rxd0 | | 3 | I | | | | | | | | | 0 |
| | | vout2_d0 | No | 4 | O | | | | | | | | | |
| | | vin3a_vsync0 | | 5 | I | | | | | | | | | 0 |
| | | vin3a_d15 | | 6 | I | | | | | | | | | 0 |
| | | mii1_txen | | 8 | O | | | | | | | | | |
| | | pr1_mii1_crs | | 11 | I | | | | | | | | | 0 |
| | | pr1_pru1_gpi20 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo20 | | 13 | O | | | | | | | | | |
| | | gpio4_31 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| E2 | vin2a_d3 | vin2a_d3 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout2_d20 | No | 4 | O | | | | | | | | | |
| | | emu13 | | 5 | O | | | | | | | | | |
| | | uart10_txd | | 8 | O | | | | | | | | | |
| | | kbd_col0 | | 9 | O | | | | | | | | | |
| | | ehrpwm1_synci | | 10 | I | | | | | | | | | 0 |
| | | pr1_edc_latch0_in | | 11 | I | | | | | | | | | 0 |
| | | pr1_pru1_gpi0 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo0 | | 13 | O | | | | | | | | | |
| | | gpio4_4 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| D2 | vin2a_d4 | vin2a_d4 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout2_d19 | No | 4 | O | | | | | | | | | |
| | | emu14 | | 5 | O | | | | | | | | | |
| | | uart10_ctsn | | 8 | I | | | | | | | | | 1 |
| | | kbd_col1 | | 9 | O | | | | | | | | | |
| | | ehrpwm1_synco | | 10 | O | | | | | | | | | |
| | | pr1_edc_sync0_out | | 11 | O | | | | | | | | | |
| | | pr1_pru1_gpi1 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo1 | | 13 | O | | | | | | | | | |
| | | gpio4_5 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F4 | vin2a_d5 | vin2a_d5 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout2_d18 | No | 4 | O | | | | | | | | | |
| | | emu15 | | 5 | O | | | | | | | | | |
| | | uart10_rtsn | | 8 | O | | | | | | | | | |
| | | kbd_col2 | | 9 | O | | | | | | | | | |
| | | eQEP2A_in | | 10 | I | | | | | | | | | 0 |
| | | pr1_edio_sof | | 11 | O | | | | | | | | | |
| | | pr1_pru1_gpi2 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo2 | | 13 | O | | | | | | | | | |
| | | gpio4_6 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| C1 | vin2a_d6 | vin2a_d6 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout2_d17 | No | 4 | O | | | | | | | | | |
| | | emu16 | | 5 | O | | | | | | | | | |
| | | mii1_rxd1 | | 8 | I | | | | | | | | | 0 |
| | | kbd_col3 | | 9 | O | | | | | | | | | |
| | | eQEP2B_in | | 10 | I | | | | | | | | | 0 |
| | | pr1_mii_mt1_clk | | 11 | I | | | | | | | | | 0 |
| | | pr1_pru1_gpi3 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo3 | | 13 | O | | | | | | | | | |
| | | gpio4_7 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| E4 | vin2a_d7 | vin2a_d7 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout2_d16 | No | 4 | O | | | | | | | | | |
| | | emu17 | | 5 | O | | | | | | | | | |
| | | mii1_rxd2 | | 8 | I | | | | | | | | | 0 |
| | | kbd_col4 | | 9 | O | | | | | | | | | |
| | | eQEP2_index | | 10 | IO | | | | | | | | | 0 |
| | | pr1_mii1_txen | | 11 | O | | | | | | | | | |
| | | pr1_pru1_gpi4 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo4 | | 13 | O | | | | | | | | | |
| | | gpio4_8 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F5 | vin2a_d8 | vin2a_d8 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout2_d15 | No | 4 | O | | | | | | | | | |
| | | emu18 | | 5 | O | | | | | | | | | |
| | | mii1_rxd3 | | 8 | I | | | | | | | | | 0 |
| | | kbd_col5 | | 9 | O | | | | | | | | | |
| | | eQEP2_strobe | | 10 | IO | | | | | | | | | 0 |
| | | pr1_mii1_txd3 | | 11 | O | | | | | | | | | |
| | | pr1_pru1_gpi5 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo5 | | 13 | O | | | | | | | | | |
| | | gpio4_9 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| E6 | vin2a_d9 | vin2a_d9 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | 0 |
| | | vout2_d14 | No | 4 | O | | | | | | | | | |
| | | emu19 | | 5 | O | | | | | | | | | |
| | | mii1_rxd0 | | 8 | I | | | | | | | | | 0 |
| | | kbd_col6 | | 9 | O | | | | | | | | | |
| | | ehrpwm2A | | 10 | O | | | | | | | | | |
| | | pr1_mii1_txd2 | | 11 | O | | | | | | | | | |
| | | pr1_pru1_gpi6 | | 12 | I | | | | | | | | | |
| | | pr1_pru1_gpo6 | | 13 | O | | | | | | | | | |
| | | gpio4_10 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| G2 | vin2a_de0 | vin2a_de0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin2a_fld0 | | 1 | I | | | | | | | | | |
| | | vin2b_fld1 | | 2 | I | | | | | | | | | |
| | | vin2b_de1 | | 3 | I | | | | | | | | | |
| | | vout2_de | No | 4 | O | | | | | | | | | |
| | | emu6 | | 5 | O | | | | | | | | | |
| | | kbd_row1 | | 9 | I | | | | | | | | | 0 |
| | | eQEP1B_in | | 10 | I | | | | | | | | | 0 |
| | | pr1_edio_data_in1 | | 12 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out1 | | 13 | O | | | | | | | | | |
| | | gpio3_29 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H7 | vin2a_fld0 | vin2a_fld0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin2b_clk1 | | 2 | I | | | | | | | | | |
| | | vout2_clk | No | 4 | O | | | | | | | | | |
| | | emu7 | | 5 | O | | | | | | | | | |
| | | eQEP1_index | | 10 | IO | | | | | | | | | 0 |
| | | pr1_edio_data_in2 | | 12 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out2 | | 13 | O | | | | | | | | | |
| | | gpio3_30 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| G1 | vin2a_hsync0 | vin2a_hsync0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin2b_hsync1 | | 3 | I | | | | | | | | | |
| | | vout2_hsync | No | 4 | O | | | | | | | | | |
| | | emu8 | | 5 | O | | | | | | | | | |
| | | uart9_rxd | | 7 | I | | | | | | | | | 1 |
| | | spi4_sclk | | 8 | IO | | | | | | | | | 0 |
| | | kbd_row2 | | 9 | I | | | | | | | | | 0 |
| | | eQEP1_strobe | | 10 | IO | | | | | | | | | 0 |
| | | pr1_uart0_cts_n | | 11 | I | | | | | | | | | 1 |
| | | pr1_edio_data_in3 | | 12 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out3 | | 13 | O | | | | | | | | | |
| | | gpio3_31 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| G6 | vin2a_vsync0 | vin2a_vsync0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv1 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin2b_vsync1 | | 3 | I | | | | | | | | | |
| | | vout2_vsync | No | 4 | O | | | | | | | | | |
| | | emu9 | | 5 | O | | | | | | | | | |
| | | uart9_txd | | 7 | O | | | | | | | | | |
| | | spi4_d1 | | 8 | IO | | | | | | | | | 0 |
| | | kbd_row3 | | 9 | I | | | | | | | | | 0 |
| | | ehrpwm1A | | 10 | O | | | | | | | | | |
| | | pr1_uart0_rts_n | | 11 | O | | | | | | | | | |
| | | pr1_edio_data_in4 | | 12 | I | | | | | | | | | 0 |
| | | pr1_edio_data_out4 | | 13 | O | | | | | | | | | |
| | | gpio4_0 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D11 | vout1_clk | vout1_clk | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin4a_fld0 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_fld0 | | 4 | I | | | | | | | | | 0 |
| | | spi3_cs0 | | 8 | IO | | | | | | | | | 1 |
| | | gpio4_19 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| F11 | vout1_d0 | vout1_d0 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | uart5_rxd | | 2 | I | | | | | | | | | 1 |
| | | vin4a_d16 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d16 | | 4 | I | | | | | | | | | 0 |
| | | spi3_cs2 | | 8 | IO | | | | | | | | | 1 |
| | | pr1_uart0_cts_n | | 10 | I | | | | | | | | | 1 |
| | | pr2_pru1_gpi18 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo18 | | 13 | O | | | | | | | | | |
| | | gpio8_0 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| G10 | vout1_d1 | vout1_d1 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | uart5_txd | | 2 | O | | | | | | | | | |
| | | vin4a_d17 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d17 | | 4 | I | | | | | | | | | 0 |
| | | pr1_uart0_rts_n | | 10 | O | | | | | | | | | |
| | | pr2_pru1_gpi19 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo19 | | 13 | O | | | | | | | | | |
| | | gpio8_1 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| D7 | vout1_d10 | vout1_d10 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu3 | | 2 | O | | | | | | | | | |
| | | vin4a_d10 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d10 | | 4 | I | | | | | | | | | 0 |
| | | obs5 | | 5 | O | | | | | | | | | |
| | | obs21 | | 6 | O | | | | | | | | | |
| | | obs_irq2 | | 7 | O | | | | | | | | | |
| | | pr2_edio_sof | | 10 | O | | | | | | | | | |
| | | pr2_pru0_gpi7 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo7 | | 13 | O | | | | | | | | | |
| | | gpio8_10 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D8 | vout1_d11 | vout1_d11 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu10 | | 2 | O | | | | | | | | | |
| | | vin4a_d11 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d11 | | 4 | I | | | | | | | | | 0 |
| | | obs6 | | 5 | O | | | | | | | | | |
| | | obs22 | | 6 | O | | | | | | | | | |
| | | obs_dmarq2 | | 7 | O | | | | | | | | | |
| | | pr2_uart0_cts_n | | 10 | I | | | | | | | | | 1 |
| | | pr2_pru0_gpi8 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo8 | | 13 | O | | | | | | | | | |
| | | gpio8_11 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A5 | vout1_d12 | vout1_d12 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu11 | | 2 | O | | | | | | | | | |
| | | vin4a_d12 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d12 | | 4 | I | | | | | | | | | 0 |
| | | obs7 | | 5 | O | | | | | | | | | |
| | | obs23 | | 6 | O | | | | | | | | | |
| | | pr2_uart0_rts_n | | 10 | O | | | | | | | | | |
| | | pr2_pru0_gpi9 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo9 | | 13 | O | | | | | | | | | |
| | | gpio8_12 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| C6 | vout1_d13 | vout1_d13 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu12 | | 2 | O | | | | | | | | | |
| | | vin4a_d13 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d13 | | 4 | I | | | | | | | | | 0 |
| | | obs8 | | 5 | O | | | | | | | | | |
| | | obs24 | | 6 | O | | | | | | | | | |
| | | pr2_uart0_rxd | | 10 | I | | | | | | | | | 1 |
| | | pr2_pru0_gpi10 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo10 | | 13 | O | | | | | | | | | |
| | | gpio8_13 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C8 | vout1_d14 | vout1_d14 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu13 | | 2 | O | | | | | | | | | |
| | | vin4a_d14 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d14 | | 4 | I | | | | | | | | | 0 |
| | | obs9 | | 5 | O | | | | | | | | | |
| | | obs25 | | 6 | O | | | | | | | | | |
| | | pr2_uart0_txd | | 10 | O | | | | | | | | | |
| | | pr2_pru0_gpi11 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo11 | | 13 | O | | | | | | | | | |
| | | gpio8_14 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| C7 | vout1_d15 | vout1_d15 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu14 | | 2 | O | | | | | | | | | |
| | | vin4a_d15 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d15 | | 4 | I | | | | | | | | | 0 |
| | | obs10 | | 5 | O | | | | | | | | | |
| | | obs26 | | 6 | O | | | | | | | | | |
| | | pr2_ecap0_ecap_capin_apwm_o | | 10 | IO | | | | | | | | | 0 |
| | | pr2_pru0_gpi12 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo12 | | 13 | O | | | | | | | | | |
| | | gpio8_15 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B7 | vout1_d16 | vout1_d16 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | uart7_rxd | | 2 | I | | | | | | | | | 1 |
| | | vin4a_d0 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d0 | | 4 | I | | | | | | | | | 0 |
| | | pr2_edio_data_in0 | | 10 | I | | | | | | | | | 0 |
| | | pr2_edio_data_out0 | | 11 | O | | | | | | | | | |
| | | pr2_pru0_gpi13 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo13 | | 13 | O | | | | | | | | | |
| | | gpio8_16 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B8 | vout1_d17 | vout1_d17 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | uart7_txd | | 2 | O | | | | | | | | | |
| | | vin4a_d1 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d1 | | 4 | I | | | | | | | | | 0 |
| | | pr2_edio_data_in1 | | 10 | I | | | | | | | | | 0 |
| | | pr2_edio_data_out1 | | 11 | O | | | | | | | | | |
| | | pr2_pru0_gpi14 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo14 | | 13 | O | | | | | | | | | |
| | | gpio8_17 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A7 | vout1_d18 | vout1_d18 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu4 | | 2 | O | | | | | | | | | |
| | | vin4a_d2 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d2 | | 4 | I | | | | | | | | | 0 |
| | | obs11 | | 5 | O | | | | | | | | | |
| | | obs27 | | 6 | O | | | | | | | | | |
| | | pr2_edio_data_in2 | | 10 | I | | | | | | | | | 0 |
| | | pr2_edio_data_out2 | | 11 | O | | | | | | | | | |
| | | pr2_pru0_gpi15 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo15 | | 13 | O | | | | | | | | | |
| | | gpio8_18 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A8 | vout1_d19 | vout1_d19 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu15 | | 2 | O | | | | | | | | | |
| | | vin4a_d3 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d3 | | 4 | I | | | | | | | | | 0 |
| | | obs12 | | 5 | O | | | | | | | | | |
| | | obs28 | | 6 | O | | | | | | | | | |
| | | pr2_edio_data_in3 | | 10 | I | | | | | | | | | 0 |
| | | pr2_edio_data_out3 | | 11 | O | | | | | | | | | |
| | | pr2_pru0_gpi16 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo16 | | 13 | O | | | | | | | | | |
| | | gpio8_19 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F10 | vout1_d2 | vout1_d2 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu2 | | 2 | O | | | | | | | | | |
| | | vin4a_d18 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d18 | | 4 | I | | | | | | | | | 0 |
| | | obs0 | | 5 | O | | | | | | | | | |
| | | obs16 | | 6 | O | | | | | | | | | |
| | | obs_irq1 | | 7 | O | | | | | | | | | |
| | | pr1_uart0_rxd | | 10 | I | | | | | | | | | 1 |
| | | pr2_pru1_gpi20 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo20 | | 13 | O | | | | | | | | | |
| | | gpio8_2 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| C9 | vout1_d20 | vout1_d20 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu16 | | 2 | O | | | | | | | | | |
| | | vin4a_d4 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d4 | | 4 | I | | | | | | | | | 0 |
| | | obs13 | | 5 | O | | | | | | | | | |
| | | obs29 | | 6 | O | | | | | | | | | |
| | | pr2_edio_data_in4 | | 10 | I | | | | | | | | | 0 |
| | | pr2_edio_data_out4 | | 11 | O | | | | | | | | | |
| | | pr2_pru0_gpi17 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo17 | | 13 | O | | | | | | | | | |
| | | gpio8_20 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A9 | vout1_d21 | vout1_d21 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu17 | | 2 | O | | | | | | | | | |
| | | vin4a_d5 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d5 | | 4 | I | | | | | | | | | 0 |
| | | obs14 | | 5 | O | | | | | | | | | |
| | | obs30 | | 6 | O | | | | | | | | | |
| | | pr2_edio_data_in5 | | 10 | I | | | | | | | | | 0 |
| | | pr2_edio_data_out5 | | 11 | O | | | | | | | | | |
| | | pr2_pru0_gpi18 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo18 | | 13 | O | | | | | | | | | |
| | | gpio8_21 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B9 | vout1_d22 | vout1_d22 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu18 | | 2 | O | | | | | | | | | |
| | | vin4a_d6 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d6 | | 4 | I | | | | | | | | | 0 |
| | | obs15 | | 5 | O | | | | | | | | | |
| | | obs31 | | 6 | O | | | | | | | | | |
| | | pr2_edio_data_in6 | | 10 | I | | | | | | | | | 0 |
| | | pr2_edio_data_out6 | | 11 | O | | | | | | | | | |
| | | pr2_pru0_gpi19 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo19 | | 13 | O | | | | | | | | | |
| | | gpio8_22 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A10 | vout1_d23 | vout1_d23 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu19 | | 2 | O | | | | | | | | | |
| | | vin4a_d7 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d7 | | 4 | I | | | | | | | | | 0 |
| | | spi3_cs3 | | 8 | IO | | | | | | | | | 1 |
| | | pr2_edio_data_in7 | | 10 | I | | | | | | | | | 0 |
| | | pr2_edio_data_out7 | | 11 | O | | | | | | | | | |
| | | pr2_pru0_gpi20 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo20 | | 13 | O | | | | | | | | | |
| | | gpio8_23 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| G11 | vout1_d3 | vout1_d3 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu5 | | 2 | O | | | | | | | | | |
| | | vin4a_d19 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d19 | | 4 | I | | | | | | | | | 0 |
| | | obs1 | | 5 | O | | | | | | | | | |
| | | obs17 | | 6 | O | | | | | | | | | |
| | | obs_dmarq1 | | 7 | O | | | | | | | | | |
| | | pr1_uart0_txd | | 10 | O | | | | | | | | | |
| | | pr2_pru0_gpi0 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo0 | | 13 | O | | | | | | | | | |
| | | gpio8_3 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E9 | vout1_d4 | vout1_d4 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu6 | | 2 | O | | | | | | | | | |
| | | vin4a_d20 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d20 | | 4 | I | | | | | | | | | 0 |
| | | obs2 | | 5 | O | | | | | | | | | |
| | | obs18 | | 6 | O | | | | | | | | | |
| | | pr1_ecap0_ecap_capin_apwm_o | | 10 | IO | | | | | | | | | 0 |
| | | pr2_pru0_gpi1 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo1 | | 13 | O | | | | | | | | | |
| | | gpio8_4 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| F9 | vout1_d5 | vout1_d5 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu7 | | 2 | O | | | | | | | | | |
| | | vin4a_d21 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d21 | | 4 | I | | | | | | | | | 0 |
| | | obs3 | | 5 | O | | | | | | | | | |
| | | obs19 | | 6 | O | | | | | | | | | |
| | | pr2_edc_latch0_in | | 10 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi2 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo2 | | 13 | O | | | | | | | | | |
| | | gpio8_5 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| F8 | vout1_d6 | vout1_d6 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu8 | | 2 | O | | | | | | | | | |
| | | vin4a_d22 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d22 | | 4 | I | | | | | | | | | 0 |
| | | obs4 | | 5 | O | | | | | | | | | |
| | | obs20 | | 6 | O | | | | | | | | | |
| | | pr2_edc_latch1_in | | 10 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi3 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo3 | | 13 | O | | | | | | | | | |
| | | gpio8_6 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E7 | vout1_d7 | vout1_d7 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | emu9 | | 2 | O | | | | | | | | | |
| | | vin4a_d23 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d23 | | 4 | I | | | | | | | | | 0 |
| | | pr2_edc_sync0_out | | 10 | O | | | | | | | | | |
| | | pr2_pru0_gpi4 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo4 | | 13 | O | | | | | | | | | |
| | | gpio8_7 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| E8 | vout1_d8 | vout1_d8 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | uart6_rxd | | 2 | I | | | | | | | | | 1 |
| | | vin4a_d8 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d8 | | 4 | I | | | | | | | | | 0 |
| | | pr2_edc_sync1_out | | 10 | O | | | | | | | | | |
| | | pr2_pru0_gpi5 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo5 | | 13 | O | | | | | | | | | |
| | | gpio8_8 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| D9 | vout1_d9 | vout1_d9 | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | uart6_txd | | 2 | O | | | | | | | | | |
| | | vin4a_d9 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_d9 | | 4 | I | | | | | | | | | 0 |
| | | pr2_edio_latch_in | | 10 | I | | | | | | | | | 0 |
| | | pr2_pru0_gpi6 | | 12 | I | | | | | | | | | |
| | | pr2_pru0_gpo6 | | 13 | O | | | | | | | | | |
| | | gpio8_9 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B10 | vout1_de | vout1_de | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin4a_de0 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_de0 | | 4 | I | | | | | | | | | 0 |
| | | spi3_d1 | | 8 | IO | | | | | | | | | 0 |
| | | gpio4_20 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B11 | vout1_fld | vout1_fld | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin4a_clk0 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_clk0 | | 4 | I | | | | | | | | | 0 |
| | | spi3_cs1 | | 8 | IO | | | | | | | | | 1 |
| | | gpio4_21 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| C11 | vout1_hsync | vout1_hsync | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin4a_hsync0 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_hsync0 | | 4 | I | | | | | | | | | 0 |
| | | spi3_d0 | | 8 | IO | | | | | | | | | 0 |
| | | gpio4_22 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| E11 | vout1_vsync | vout1_vsync | No | 0 | O | PD | PD | 15 | 1.8/3.3 | vddshv2 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | vin4a_vsync0 | | 3 | I | | | | | | | | | 0 |
| | | vin3a_vsync0 | | 4 | I | | | | | | | | | 0 |
| | | spi3_sclk | | 8 | IO | | | | | | | | | 0 |
| | | pr2_pru1_gpi17 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo17 | | 13 | O | | | | | | | | | |
| | | gpio4_23 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| A1, A14, A2, A23, A28, A6, AA10, AA14, AA15, AA20, AA8, AA9, AB14, AB20, AD1, AD24, AG1, AH1, AH2, AH20, AH28, AH8, B1, D13, D19, E13, E19, F1, F7, G7, G8, G9, H12, J12, J15, J28, K1, K15, K24, K25, K4, K5, L13, L14, M19, N14, N15, N19, N24, N25, P28, R1, R12, R13, R15, R21, T10, T11, T12, T14, T15, T17, T18, T21, U15, U17, U20, U21, V15, V17, W1, W15, W24, W25, W28 | vss | vss | | | GND | | | | | | | | | |
| AD19, AE19 | vssa_hdmi | vssa_hdmi | | | GND | | | | | | | | | |
| AF15 | vssa_osc0 | vssa_osc0 | | | GND | | | | | | | | | |


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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AC14 | vssa_osc1 | vssa_osc1 | | | GND | | | | | | | | | |
| AD13, AE13 | vssa_pcie | vssa_pcie | | | GND | | | | | | | | | |
| AE10 | vssa_sata | vssa_sata | | | GND | | | | | | | | | |
| AA11, AB11 | vssa_usb | vssa_usb | | | GND | | | | | | | | | |
| AD10 | vssa_usb3 | vssa_usb3 | | | GND | | | | | | | | | |
| U14 | vssa_video | vssa_video | | | GND | | | | | | | | | |
| AD17 | Wakeup0 | Wakeup0 | | 0 | I | OFF | OFF | 15 | 1.8/3.3 | vddshv5 | Yes | IHHV1833 | PU/PD | |
| | | dcan1_rx | | 1 | I | | | | | | | | | 1 |
| | | gpio1_0 | | 14 | I | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AC17 | Wakeup1 | Wakeup1 | | 0 | I | OFF | OFF | 15 | 1.8/3.3 | vddshv5 | Yes | IHHV1833 | PU/PD | |
| | | dcan2_rx | | 1 | I | | | | | | | | | 1 |
| | | gpio1_1 | | 14 | I | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AB16 | Wakeup2 | Wakeup2 | | 0 | I | OFF | OFF | 15 | 1.8/3.3 | vddshv5 | Yes | IHHV1833 | PU/PD | |
| | | sys_nirq2 | | 1 | I | | | | | | | | | |
| | | gpio1_2 | | 14 | I | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AC16 | Wakeup3 | Wakeup3 | | 0 | I | OFF | OFF | 15 | 1.8/3.3 | vddshv5 | Yes | IHHV1833 | PU/PD | |
| | | sys_nirq1 | | 1 | I | | | | | | | | | |
| | | gpio1_3 | | 14 | I | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| AE15 | xi_osc0 | xi_osc0 | | 0 | I | | | | 1.8 | vdda_osc | No | LVCMOS Analog | | |
| AC15 | xi_osc1 | xi_osc1 | | 0 | I | | | | 1.8 | vdda_osc | No | LVCMOS Analog | | |
| AD15 | xo_osc0 | xo_osc0 | | 0 | O | | | | 1.8 | vdda_osc | No | LVCMOS Analog | | |
| AC13 | xo_osc1 | xo_osc1 | | 0 | A | | | | 1.8 | vdda_osc | No | LVCMOS Analog | | |

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## Table 4-2. Ball Characteristics[(1)] (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D18 | xref_clk0 | xref_clk0 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mcasp2_axr8 | | 1 | IO | | | | | | | | | 0 |
| | | mcasp1_axr4 | | 2 | IO | | | | | | | | | 0 |
| | | mcasp1_ahclkx | | 3 | O | | | | | | | | | |
| | | mcasp5_ahclkx | | 4 | O | | | | | | | | | |
| | | vin6a_d0 | | 7 | I | | | | | | | | | 0 |
| | | hdq0 | | 8 | IO | | | | | | | | | 1 |
| | | clkout2 | | 9 | O | | | | | | | | | |
| | | timer13 | | 10 | IO | | | | | | | | | |
| | | pr2_mii1_col | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi5 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo5 | | 13 | O | | | | | | | | | |
| | | gpio6_17 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| E17 | xref_clk1 | xref_clk1 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mcasp2_axr9 | | 1 | IO | | | | | | | | | 0 |
| | | mcasp1_axr5 | | 2 | IO | | | | | | | | | 0 |
| | | mcasp2_ahclkx | | 3 | O | | | | | | | | | |
| | | mcasp6_ahclkx | | 4 | O | | | | | | | | | |
| | | vin6a_clk0 | | 7 | I | | | | | | | | | 0 |
| | | timer14 | | 10 | IO | | | | | | | | | |
| | | pr2_mii1_crs | | 11 | I | | | | | | | | | 0 |
| | | pr2_pru1_gpi6 | | 12 | I | | | | | | | | | |
| | | pr2_pru1_gpo6 | | 13 | O | | | | | | | | | |
| | | gpio6_18 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |
| B26 | xref_clk2 | xref_clk2 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mcasp2_axr10 | | 1 | IO | | | | | | | | | 0 |
| | | mcasp1_axr6 | | 2 | IO | | | | | | | | | 0 |
| | | mcasp3_ahclkx | | 3 | O | | | | | | | | | |
| | | mcasp7_ahclkx | | 4 | O | | | | | | | | | |
| | | vout2_clk | No | 6 | O | | | | | | | | | |
| | | vin4a_clk0 | | 8 | I | | | | | | | | | 0 |
| | | timer15 | | 10 | IO | | | | | | | | | |
| | | gpio6_19 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |


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**Table 4-2. Ball Characteristics(1) (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PN [4] | MUXMODE [5] | TYPE [6] | BALL RESET STATE [7] | BALL RESET REL. STATE [8] | BALL RESET REL. MUXMODE [9] | I/O VOLTAGE VALUE [10] | POWER [11] | HYS [12] | BUFFER TYPE [13] | PULL UP/DOWN TYPE [14] | DSIS [15] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C23 | xref_clk3 | xref_clk3 | | 0 | I | PD | PD | 15 | 1.8/3.3 | vddshv3 | Yes | Dual Voltage LVCMOS | PU/PD | |
| | | mcasp2_axr11 | | 1 | IO | | | | | | | | | 0 |
| | | mcasp1_axr7 | | 2 | IO | | | | | | | | | 0 |
| | | mcasp4_ahclkx | | 3 | O | | | | | | | | | |
| | | mcasp8_ahclkx | | 4 | O | | | | | | | | | |
| | | vout2_de | No | 6 | O | | | | | | | | | |
| | | hdq0 | | 7 | IO | | | | | | | | | 1 |
| | | vin4a_de0 | | 8 | I | | | | | | | | | 0 |
| | | clkout3 | | 9 | O | | | | | | | | | |
| | | timer16 | | 10 | IO | | | | | | | | | |
| | | gpio6_20 | | 14 | IO | | | | | | | | | |
| | | Driver off | | 15 | I | | | | | | | | | |

(1) NA in this table stands for Not Applicable.

(2) For more information on recommended operating conditions, see Table 5-4, *Recommended Operating Conditions*.

(3) The pullup or pulldown block strength is equal to: minimum = 50 µA, typical = 100 µA, maximum = 250 µA.

(4) The output impedance settings of this IO cell are programmable; by default, the value is DS[1:0] = 10, this means 40 Ω. For more information on DS[1:0] register configuration, see the Device TRM.

(5) IO drive strength for usb1_dp, usb1_dm, usb2_dp and usb2_dm: minimum 18.3 mA, maximum 89 mA (for a power supply vdda33v_usb1 and vdda33v_usb2 = 3.46 V).

(6) Minimum PU = 900 Ω, maximum PU = 3.090 kΩ and minimum PD = 14.25 kΩ, maximum PD = 24.8 kΩ.
For more information, see chapter 7 of the USB2.0 specification, in particular section Signaling / Device Speed Identification.

(7) In PUx / PDy, x and y = 60 to 200 µA.
The output impedance settings (or drive strengths) of this IO are programmable (34 Ω, 40 Ω, 48 Ω, 60 Ω, 80 Ω) depending on the values of the I[2:0] registers.

(8) The VOUT3 interface when multiplexed onto balls mapped to the VDDSHV6 supply rail is restricted to operating in 1.8V mode only (VDDSHV6 must be supplied with 1.8V). 3.3V mode is not supported. This must be considered in the pin mux programming and VDDSHVx supply connections.

(9) The internal pull resistors for balls K7, M7, J5, K6, J4, J6, H4, H5 are permanently disabled when sysboot15 is set to 1 as described in the section *Sysboot Configuration* of the Device TRM. If internal pull-up/down resistors are desired on these balls then sysboot15 should be set to 0. If gpmc boot mode is used with SYSBOOT15=1 (not recommended) then external pull-downs should be implemented to keep the address bus at logic-0 value during boot since the gpmc ms-address bits are high-z during boot.

## 4.3 Multiplexing Characteristics

Table 4-3 describes the device multiplexing (no characteristics are available in this table).

**NOTE**

This table doesn't take into account subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 4.4, *Signal Descriptions*.

**NOTE**

For more information, see the Control Module / Control Module Functional Description / PAD Functional Multiplexing and Configuration section of the Device TRM.

**NOTE**

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (Hi-Z mode is not an input signal).

**NOTE**

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This should be avoided.

**CAUTION**

The I/O timings provided in Section 7, *Timing Requirements and Switching Characteristics* are valid only if signals within a single IOSET are used. The IOSETs are defined in the corresponding tables.

**Table 4-3. Multiplexing Characteristics**

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| | | P25 | ddr2_a6 | | | | | | | | | | | | | | | |
| | | Y23 | ddr1_d26 | | | | | | | | | | | | | | | |
| | | Y19 | ddr1_d21 | | | | | | | | | | | | | | | |
| | | AE15 | xi_osc0 | | | | | | | | | | | | | | | |
| | | AH24 | ddr1_nck | | | | | | | | | | | | | | | |
| | | AG15 | ljcb_clkp | | | | | | | | | | | | | | | |
| | | AF24 | ddr1_d4 | | | | | | | | | | | | | | | |
| | | U25 | ddr2_wen | | | | | | | | | | | | | | | |
| | | F27 | ddr2_d5 | | | | | | | | | | | | | | | |
| | | V25 | ddr1_ecc_d6 | | | | | | | | | | | | | | | |
| | | M27 | ddr2_dqsn3 | | | | | | | | | | | | | | | |
| | | G26 | ddr2_d12 | | | | | | | | | | | | | | | |
| | | AG19 | hdmi1_data2x | | | | | | | | | | | | | | | |


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## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| | | AF21 | ddr1_a4 | | | | | | | | | | | | | | | |
| | | E27 | ddr2_d6 | | | | | | | | | | | | | | | |
| | | F24 | ddr2_d3 | | | | | | | | | | | | | | | |
| | | H26 | ddr2_d11 | | | | | | | | | | | | | | | |
| | | W23 | ddr1_ecc_d3 | | | | | | | | | | | | | | | |
| | | Y27 | ddr1_dqsn3 | | | | | | | | | | | | | | | |
| | | AC24 | ddr1_d14 | | | | | | | | | | | | | | | |
| | | J24 | ddr2_d15 | | | | | | | | | | | | | | | |
| | | R26 | ddr2_a1 | | | | | | | | | | | | | | | |
| | | G27 | ddr2_dqsn0 | | | | | | | | | | | | | | | |
| | | AF28 | ddr1_d11 | | | | | | | | | | | | | | | |
| | | AA23 | ddr1_d24 | | | | | | | | | | | | | | | |
| | | AD18 | ddr1_a15 | | | | | | | | | | | | | | | |
| | | H23 | ddr2_d8 | | | | | | | | | | | | | | | |
| | | AH16 | hdmi1_clocky | | | | | | | | | | | | | | | |
| | | AC20 | ddr1_a2 | | | | | | | | | | | | | | | |
| | | AA24 | ddr1_d27 | | | | | | | | | | | | | | | |
| | | W19 | ddr1_ecc_d2 | | | | | | | | | | | | | | | |
| | | L24 | ddr2_d20 | | | | | | | | | | | | | | | |
| | | AG11 | pcie_rxn1 | | | | | | | | | | | | | | | |
| | | AG21 | ddr1_rst | | | | | | | | | | | | | | | |
| | | AE28 | ddr1_dqsn1 | | | | | | | | | | | | | | | |
| | | AC11 | usb_txn0 | | | | | | | | | | | | | | | |
| | | L22 | ddr2_d16 | | | | | | | | | | | | | | | |
| | | U28 | ddr2_casn | | | | | | | | | | | | | | | |
| | | K22 | ddr2_d22 | | | | | | | | | | | | | | | |
| | | AG25 | ddr1_dqsn0 | | | | | | | | | | | | | | | |
| | | W20 | ddr1_d17 | | | | | | | | | | | | | | | |
| | | AF14 | rtc_iso | | | | | | | | | | | | | | | |
| | | AA27 | ddr1_dqm3 | | | | | | | | | | | | | | | |
| | | AF25 | ddr1_d0 | | | | | | | | | | | | | | | |
| | | AF23 | ddr1_d6 | | | | | | | | | | | | | | | |
| | | AG18 | hdmi1_data1x | | | | | | | | | | | | | | | |
| | | AG10 | sata1_txn0 | | | | | | | | | | | | | | | |
| | | AF20 | ddr1_rasn | | | | | | | | | | | | | | | |

## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| | | V26 | ddr1_dqm_ecc | | | | | | | | | | | | | | | |
| | | V20 | ddr1_d16 | | | | | | | | | | | | | | | |
| | | G25 | ddr2_d1 | | | | | | | | | | | | | | | |
| | | AH13 | pcie_rxp0 | | | | | | | | | | | | | | | |
| | | AC18 | ddr1_casn | | | | | | | | | | | | | | | |
| | | AG9 | sata1_rxp0 | | | | | | | | | | | | | | | |
| | | AH23 | ddr1_csn0 | | | | | | | | | | | | | | | |
| | | AE11 | usb2_dp | | | | | | | | | | | | | | | |
| | | R25 | ddr2_a0 | | | | | | | | | | | | | | | |
| | | Y24 | ddr1_d28 | | | | | | | | | | | | | | | |
| | | AH15 | ljcb_clkn | | | | | | | | | | | | | | | |
| | | AD20 | ddr1_a0 | | | | | | | | | | | | | | | |
| | | AA25 | ddr1_d30 | | | | | | | | | | | | | | | |
| | | L23 | ddr2_d19 | | | | | | | | | | | | | | | |
| | | AA1 | mlbp_dat_p | | | | | | | | | | | | | | | |
| | | AD14 | rtc_osc_xo | | | | | | | | | | | | | | | |
| | | J25 | ddr2_d13 | | | | | | | | | | | | | | | |
| | | AC25 | ddr1_d13 | | | | | | | | | | | | | | | |
| | | AB23 | ddr1_dqm1 | | | | | | | | | | | | | | | |
| | | U22 | ddr2_a15 | | | | | | | | | | | | | | | |
| | | T22 | ddr2_a13 | | | | | | | | | | | | | | | |
| | | AH19 | hdmi1_data2y | | | | | | | | | | | | | | | |
| | | M26 | ddr2_d31 | | | | | | | | | | | | | | | |
| | | AB27 | ddr1_d22 | | | | | | | | | | | | | | | |
| | | AG14 | pcie_txn0 | | | | | | | | | | | | | | | |
| | | Y28 | ddr1_dqs3 | | | | | | | | | | | | | | | |
| | | J20 | ddr2_d23 | | | | | | | | | | | | | | | |
| | | AB19 | ddr1_a3 | | | | | | | | | | | | | | | |
| | | AH10 | sata1_txp0 | | | | | | | | | | | | | | | |
| | | G28 | ddr2_dqs0 | | | | | | | | | | | | | | | |
| | | AG24 | ddr1_ck | | | | | | | | | | | | | | | |
| | | AE24 | ddr1_d5 | | | | | | | | | | | | | | | |
| | | AC15 | xi_osc1 | | | | | | | | | | | | | | | |
| | | AC21 | ddr1_a12 | | | | | | | | | | | | | | | |
| | | K28 | ddr2_dqsn2 | | | | | | | | | | | | | | | |
| | | AB1 | mlbp_clk_p | | | | | | | | | | | | | | | |
| | | AF12 | usb_rxn0 | | | | | | | | | | | | | | | |


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## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| | | L28 | ddr2_d27 | | | | | | | | | | | | | | | |
| | | M24 | ddr2_d29 | | | | | | | | | | | | | | | |
| | | AH9 | sata1_rxn0 | | | | | | | | | | | | | | | |
| | | AC26 | ddr1_dqm2 | | | | | | | | | | | | | | | |
| | | AA28 | ddr1_d31 | | | | | | | | | | | | | | | |
| | | H28 | ddr2_dqsn1 | | | | | | | | | | | | | | | |
| | | AD23 | ddr1_dqm0 | | | | | | | | | | | | | | | |
| | | E26 | ddr2_d0 | | | | | | | | | | | | | | | |
| | | AE27 | ddr1_dqs1 | | | | | | | | | | | | | | | |
| | | AF27 | ddr1_d9 | | | | | | | | | | | | | | | |
| | | V24 | ddr1_ecc_d5 | | | | | | | | | | | | | | | |
| | | K23 | ddr2_dqm2 | | | | | | | | | | | | | | | |
| | | K20 | ddr2_d17 | | | | | | | | | | | | | | | |
| | | T28 | ddr2_ck | | | | | | | | | | | | | | | |
| | | H24 | ddr2_d10 | | | | | | | | | | | | | | | |
| | | AG27 | ddr1_d10 | | | | | | | | | | | | | | | |
| | | R23 | ddr2_odt0 | | | | | | | | | | | | | | | |
| | | U27 | ddr2_ba1 | | | | | | | | | | | | | | | |
| | | AF22 | ddr1_a8 | | | | | | | | | | | | | | | |
| | | AA2 | mlbp_dat_n | | | | | | | | | | | | | | | |
| | | U23 | ddr2_ba0 | | | | | | | | | | | | | | | |
| | | AH21 | ddr1_wen | | | | | | | | | | | | | | | |
| | | AE21 | ddr1_a7 | | | | | | | | | | | | | | | |
| | | AC12 | usb1_dm | | | | | | | | | | | | | | | |
| | | AH12 | pcie_txp1 | | | | | | | | | | | | | | | |
| | | Y20 | ddr1_d23 | | | | | | | | | | | | | | | |
| | | AC27 | ddr1_d20 | | | | | | | | | | | | | | | |
| | | AE23 | ddr1_d7 | | | | | | | | | | | | | | | |
| | | T27 | ddr2_nck | | | | | | | | | | | | | | | |
| | | AG22 | ddr1_cke | | | | | | | | | | | | | | | |
| | | AD27 | ddr1_dqs2 | | | | | | | | | | | | | | | |
| | | AH14 | pcie_txp0 | | | | | | | | | | | | | | | |
| | | AH26 | ddr1_d3 | | | | | | | | | | | | | | | |
| | | AD21 | ddr1_a10 | | | | | | | | | | | | | | | |
| | | N28 | ddr2_a12 | | | | | | | | | | | | | | | |
| | | Y25 | ddr1_ecc_d4 | | | | | | | | | | | | | | | |
| | | AE17 | ddr1_a14 | | | | | | | | | | | | | | | |

## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| | | AH18 | hdmi1_data1y | | | | | | | | | | | | | | | |
| | | AH22 | ddr1_a5 | | | | | | | | | | | | | | | |
| | | J26 | ddr2_d14 | | | | | | | | | | | | | | | |
| | | W22 | ddr1_ecc_d0 | | | | | | | | | | | | | | | |
| | | V23 | ddr1_ecc_d1 | | | | | | | | | | | | | | | |
| | | AE12 | usb_rxp0 | | | | | | | | | | | | | | | |
| | | AE14 | rtc_osc_xi_clkin32 | | | | | | | | | | | | | | | |
| | | AH11 | pcie_rxp1 | | | | | | | | | | | | | | | |
| | | AB2 | mlbp_clk_n | | | | | | | | | | | | | | | |
| | | AG23 | ddr1_a6 | | | | | | | | | | | | | | | |
| | | H27 | ddr2_dqs1 | | | | | | | | | | | | | | | |
| | | AB18 | ddr1_ba2 | | | | | | | | | | | | | | | |
| | | AG17 | hdmi1_data0x | | | | | | | | | | | | | | | |
| | | AF26 | ddr1_d1 | | | | | | | | | | | | | | | |
| | | H25 | ddr2_d9 | | | | | | | | | | | | | | | |
| | | M25 | ddr2_d30 | | | | | | | | | | | | | | | |
| | | AD11 | usb_txp0 | | | | | | | | | | | | | | | |
| | | AC1 | mlbp_sig_p | | | | | | | | | | | | | | | |
| | | L27 | ddr2_d24 | | | | | | | | | | | | | | | |
| | | V27 | ddr1_dqs_ecc | | | | | | | | | | | | | | | |
| | | AF17 | ddr1_ba0 | | | | | | | | | | | | | | | |
| | | AE26 | ddr1_d12 | | | | | | | | | | | | | | | |
| | | G24 | ddr2_dqm1 | | | | | | | | | | | | | | | |
| | | K27 | ddr2_dqs2 | | | | | | | | | | | | | | | |
| | | AC19 | ddr1_a1 | | | | | | | | | | | | | | | |
| | | AG13 | pcie_rxn0 | | | | | | | | | | | | | | | |
| | | L26 | ddr2_d25 | | | | | | | | | | | | | | | |
| | | AB28 | ddr1_d18 | | | | | | | | | | | | | | | |
| | | N23 | ddr2_a10 | | | | | | | | | | | | | | | |
| | | M22 | ddr2_dqm3 | | | | | | | | | | | | | | | |
| | | U26 | ddr2_ba2 | | | | | | | | | | | | | | | |
| | | Y26 | ddr1_ecc_d7 | | | | | | | | | | | | | | | |
| | | P24 | ddr2_csn0 | | | | | | | | | | | | | | | |
| | | R22 | ddr2_a14 | | | | | | | | | | | | | | | |


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## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| | | AD22 | ddr1_a11 | | | | | | | | | | | | | | | |
| | | N20 | ddr2_a7 | | | | | | | | | | | | | | | |
| | | M23 | ddr2_d28 | | | | | | | | | | | | | | | |
| | | AD28 | ddr1_dqsn2 | | | | | | | | | | | | | | | |
| | | U24 | ddr2_cke | | | | | | | | | | | | | | | |
| | | P22 | ddr2_a5 | | | | | | | | | | | | | | | |
| | | AE18 | ddr1_ba1 | | | | | | | | | | | | | | | |
| | | F26 | ddr2_d4 | | | | | | | | | | | | | | | |
| | | AE20 | ddr1_odt0 | | | | | | | | | | | | | | | |
| | | N22 | ddr2_vref0 | | | | | | | | | | | | | | | |
| | | E28 | ddr2_d7 | | | | | | | | | | | | | | | |
| | | F25 | ddr2_d2 | | | | | | | | | | | | | | | |
| | | AF11 | usb2_dm | | | | | | | | | | | | | | | |
| | | R24 | ddr2_rst | | | | | | | | | | | | | | | |
| | | AD15 | xo_osc0 | | | | | | | | | | | | | | | |
| | | R27 | ddr2_a3 | | | | | | | | | | | | | | | |
| | | AE22 | ddr1_a9 | | | | | | | | | | | | | | | |
| | | Y18 | ddr1_vref0 | | | | | | | | | | | | | | | |
| | | AC13 | xo_osc1 | | | | | | | | | | | | | | | |
| | | F28 | ddr2_dqm0 | | | | | | | | | | | | | | | |
| | | J23 | ddr2_d21 | | | | | | | | | | | | | | | |
| | | P26 | ddr2_a11 | | | | | | | | | | | | | | | |
| | | M28 | ddr2_dqs3 | | | | | | | | | | | | | | | |
| | | AC2 | mlbp_sig_n | | | | | | | | | | | | | | | |
| | | AD12 | usb1_dp | | | | | | | | | | | | | | | |
| | | Y22 | ddr1_d25 | | | | | | | | | | | | | | | |
| | | T23 | ddr2_rasn | | | | | | | | | | | | | | | |
| | | AH17 | hdmi1_data0y | | | | | | | | | | | | | | | |
| | | N27 | ddr2_a9 | | | | | | | | | | | | | | | |
| | | P23 | ddr2_a4 | | | | | | | | | | | | | | | |
| | | AG26 | ddr1_d2 | | | | | | | | | | | | | | | |
| | | AH25 | ddr1_dqs0 | | | | | | | | | | | | | | | |
| | | AG12 | pcie_txn1 | | | | | | | | | | | | | | | |
| | | AF18 | ddr1_a13 | | | | | | | | | | | | | | | |
| | | K21 | ddr2_d18 | | | | | | | | | | | | | | | |
| | | AC28 | ddr1_d19 | | | | | | | | | | | | | | | |
| | | V28 | ddr1_dqsn_ecc | | | | | | | | | | | | | | | |

## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| | | P27 | ddr2_a8 | | | | | | | | | | | | | | | |
| | | AC23 | ddr1_d8 | | | | | | | | | | | | | | | |
| | | F22 | porz | | | | | | | | | | | | | | | |
| | | L25 | ddr2_d26 | | | | | | | | | | | | | | | |
| | | AG16 | hdmi1_clockx | | | | | | | | | | | | | | | |
| | | R28 | ddr2_a2 | | | | | | | | | | | | | | | |
| | | AA26 | ddr1_d29 | | | | | | | | | | | | | | | |
| | | AD25 | ddr1_d15 | | | | | | | | | | | | | | | |
| 0x1400 | CTRL_CORE_PAD_GPMC_AD0 | M6 | gpmc_ad0 | | vin3a_d0 | vout3_d0 | | | | | | | | | | | gpio1_6 | sysboot0 |
| 0x1404 | CTRL_CORE_PAD_GPMC_AD1 | M2 | gpmc_ad1 | | vin3a_d1 | vout3_d1 | | | | | | | | | | | gpio1_7 | sysboot1 |
| 0x1408 | CTRL_CORE_PAD_GPMC_AD2 | L5 | gpmc_ad2 | | vin3a_d2 | vout3_d2 | | | | | | | | | | | gpio1_8 | sysboot2 |
| 0x140C | CTRL_CORE_PAD_GPMC_AD3 | M1 | gpmc_ad3 | | vin3a_d3 | vout3_d3 | | | | | | | | | | | gpio1_9 | sysboot3 |
| 0x1410 | CTRL_CORE_PAD_GPMC_AD4 | L6 | gpmc_ad4 | | vin3a_d4 | vout3_d4 | | | | | | | | | | | gpio1_10 | sysboot4 |
| 0x1414 | CTRL_CORE_PAD_GPMC_AD5 | L4 | gpmc_ad5 | | vin3a_d5 | vout3_d5 | | | | | | | | | | | gpio1_11 | sysboot5 |
| 0x1418 | CTRL_CORE_PAD_GPMC_AD6 | L3 | gpmc_ad6 | | vin3a_d6 | vout3_d6 | | | | | | | | | | | gpio1_12 | sysboot6 |
| 0x141C | CTRL_CORE_PAD_GPMC_AD7 | L2 | gpmc_ad7 | | vin3a_d7 | vout3_d7 | | | | | | | | | | | gpio1_13 | sysboot7 |
| 0x1420 | CTRL_CORE_PAD_GPMC_AD8 | L1 | gpmc_ad8 | | vin3a_d8 | vout3_d8 | | | | | | | | | | | gpio7_18 | sysboot8 |
| 0x1424 | CTRL_CORE_PAD_GPMC_AD9 | K2 | gpmc_ad9 | | vin3a_d9 | vout3_d9 | | | | | | | | | | | gpio7_19 | sysboot9 |
| 0x1428 | CTRL_CORE_PAD_GPMC_AD10 | J1 | gpmc_ad10 | | vin3a_d10 | vout3_d10 | | | | | | | | | | | gpio7_28 | sysboot10 |
| 0x142C | CTRL_CORE_PAD_GPMC_AD11 | J2 | gpmc_ad11 | | vin3a_d11 | vout3_d11 | | | | | | | | | | | gpio7_29 | sysboot11 |
| 0x1430 | CTRL_CORE_PAD_GPMC_AD12 | H1 | gpmc_ad12 | | vin3a_d12 | vout3_d12 | | | | | | | | | | | gpio1_18 | sysboot12 |
| 0x1434 | CTRL_CORE_PAD_GPMC_AD13 | J3 | gpmc_ad13 | | vin3a_d13 | vout3_d13 | | | | | | | | | | | gpio1_19 | sysboot13 |
| 0x1438 | CTRL_CORE_PAD_GPMC_AD14 | H2 | gpmc_ad14 | | vin3a_d14 | vout3_d14 | | | | | | | | | | | gpio1_20 | sysboot14 |
| 0x143C | CTRL_CORE_PAD_GPMC_AD15 | H3 | gpmc_ad15 | | vin3a_d15 | vout3_d15 | | | | | | | | | | | gpio1_21 | sysboot15 |
| 0x1440 | CTRL_CORE_PAD_GPMC_A0 | R6 | gpmc_a0 | | vin3a_d16 | vout3_d16 | vin4a_d0 | | vin4b_d0 | i2c4_scl | uart5_rxd | | | | | | gpio7_3 | Driver off |
| 0x1444 | CTRL_CORE_PAD_GPMC_A1 | T9 | gpmc_a1 | | vin3a_d17 | vout3_d17 | vin4a_d1 | | vin4b_d1 | i2c4_sda | uart5_txd | | | | | | gpio7_4 | Driver off |


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## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0x1448 | CTRL_CORE_PAD_GPMC_A2 | T6 | gpmc_a2 | | vin3a_d18 | vout3_d18 | vin4a_d2 | | vin4b_d2 | uart7_rxd | uart5_ctsn | | | | | | gpio7_5 | Driver off |
| 0x144C | CTRL_CORE_PAD_GPMC_A3 | T7 | gpmc_a3 | qspi1_cs2 | vin3a_d19 | vout3_d19 | vin4a_d3 | | vin4b_d3 | uart7_txd | uart5_rtsn | | | | | | gpio7_6 | Driver off |
| 0x1450 | CTRL_CORE_PAD_GPMC_A4 | P6 | gpmc_a4 | qspi1_cs3 | vin3a_d20 | vout3_d20 | vin4a_d4 | | vin4b_d4 | i2c5_scl | uart6_rxd | | | | | | gpio1_26 | Driver off |
| 0x1454 | CTRL_CORE_PAD_GPMC_A5 | R9 | gpmc_a5 | | vin3a_d21 | vout3_d21 | vin4a_d5 | | vin4b_d5 | i2c5_sda | uart6_txd | | | | | | gpio1_27 | Driver off |
| 0x1458 | CTRL_CORE_PAD_GPMC_A6 | R5 | gpmc_a6 | | vin3a_d22 | vout3_d22 | vin4a_d6 | | vin4b_d6 | uart8_rxd | uart6_ctsn | | | | | | gpio1_28 | Driver off |
| 0x145C | CTRL_CORE_PAD_GPMC_A7 | P5 | gpmc_a7 | | vin3a_d23 | vout3_d23 | vin4a_d7 | | vin4b_d7 | uart8_txd | uart6_rtsn | | | | | | gpio1_29 | Driver off |
| 0x1460 | CTRL_CORE_PAD_GPMC_A8 | N7 | gpmc_a8 | | vin3a_hsync0 | vout3_hsync | | | vin4b_hsync1 | timer12 | spi4_sclk | | | | | | gpio1_30 | Driver off |
| 0x1464 | CTRL_CORE_PAD_GPMC_A9 | R4 | gpmc_a9 | | vin3a_vsync0 | vout3_vsync | | | vin4b_vsync1 | timer11 | spi4_d1 | | | | | | gpio1_31 | Driver off |
| 0x1468 | CTRL_CORE_PAD_GPMC_A10 | N9 | gpmc_a10 | | vin3a_de0 | vout3_de | | | vin4b_clk1 | timer10 | spi4_d0 | | | | | | gpio2_0 | Driver off |
| 0x146C | CTRL_CORE_PAD_GPMC_A11 | P9 | gpmc_a11 | | vin3a_fld0 | vout3_fld | vin4a_fld0 | | vin4b_de1 | timer9 | spi4_cs0 | | | | | | gpio2_1 | Driver off |
| 0x1470 | CTRL_CORE_PAD_GPMC_A12 | P4 | gpmc_a12 | | | | vin4a_clk0 | gpmc_a0 | vin4b_fld1 | timer8 | spi4_cs1 | dma_evt1 | | | | | gpio2_2 | Driver off |
| 0x1474 | CTRL_CORE_PAD_GPMC_A13 | R3 | gpmc_a13 | qspi1_rtclk | | | vin4a_hsync0 | | | timer7 | spi4_cs2 | dma_evt2 | | | | | gpio2_3 | Driver off |
| 0x1478 | CTRL_CORE_PAD_GPMC_A14 | T2 | gpmc_a14 | qspi1_d3 | | | vin4a_vsync0 | | | timer6 | spi4_cs3 | | | | | | gpio2_4 | Driver off |
| 0x147C | CTRL_CORE_PAD_GPMC_A15 | U2 | gpmc_a15 | qspi1_d2 | | | vin4a_d8 | | | timer5 | | | | | | | gpio2_5 | Driver off |
| 0x1480 | CTRL_CORE_PAD_GPMC_A16 | U1 | gpmc_a16 | qspi1_d0 | | | vin4a_d9 | | | | | | | | | | gpio2_6 | Driver off |
| 0x1484 | CTRL_CORE_PAD_GPMC_A17 | P3 | gpmc_a17 | qspi1_d1 | | | vin4a_d10 | | | | | | | | | | gpio2_7 | Driver off |
| 0x1488 | CTRL_CORE_PAD_GPMC_A18 | R2 | gpmc_a18 | qspi1_sclk | | | vin4a_d11 | | | | | | | | | | gpio2_8 | Driver off |
| 0x148C | CTRL_CORE_PAD_GPMC_A19 | K7 | gpmc_a19 | mmc2_dat4 | gpmc_a13 | | vin4a_d12 | | vin3b_d0 | | | | | | | | gpio2_9 | Driver off |
| 0x1490 | CTRL_CORE_PAD_GPMC_A20 | M7 | gpmc_a20 | mmc2_dat5 | gpmc_a14 | | vin4a_d13 | | vin3b_d1 | | | | | | | | gpio2_10 | Driver off |
| 0x1494 | CTRL_CORE_PAD_GPMC_A21 | J5 | gpmc_a21 | mmc2_dat6 | gpmc_a15 | | vin4a_d14 | | vin3b_d2 | | | | | | | | gpio2_11 | Driver off |
| 0x1498 | CTRL_CORE_PAD_GPMC_A22 | K6 | gpmc_a22 | mmc2_dat7 | gpmc_a16 | | vin4a_d15 | | vin3b_d3 | | | | | | | | gpio2_12 | Driver off |
| 0x149C | CTRL_CORE_PAD_GPMC_A23 | J7 | gpmc_a23 | mmc2_clk | gpmc_a17 | | vin4a_fld0 | | vin3b_d4 | | | | | | | | gpio2_13 | Driver off |
| 0x14A0 | CTRL_CORE_PAD_GPMC_A24 | J4 | gpmc_a24 | mmc2_dat0 | gpmc_a18 | | | | vin3b_d5 | | | | | | | | gpio2_14 | Driver off |
| 0x14A4 | CTRL_CORE_PAD_GPMC_A25 | J6 | gpmc_a25 | mmc2_dat1 | gpmc_a19 | | | | vin3b_d6 | | | | | | | | gpio2_15 | Driver off |

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## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0x14A8 | CTRL_CORE_PAD_GPMC_A26 | H4 | gpmc_a26 | mmc2_dat2 | gpmc_a20 | | | | vin3b_d7 | | | | | | | | gpio2_16 | Driver off |
| 0x14AC | CTRL_CORE_PAD_GPMC_A27 | H5 | gpmc_a27 | mmc2_dat3 | gpmc_a21 | | | | vin3b_hsync1 | | | | | | | | gpio2_17 | Driver off |
| 0x14B0 | CTRL_CORE_PAD_GPMC_CS1 | H6 | gpmc_cs1 | mmc2_cmd | gpmc_a22 | | vin4a_de0 | | vin3b_vsync1 | | | | | | | | gpio2_18 | Driver off |
| 0x14B4 | CTRL_CORE_PAD_GPMC_CS0 | T1 | gpmc_cs0 | | | | | | | | | | | | | | gpio2_19 | Driver off |
| 0x14B8 | CTRL_CORE_PAD_GPMC_CS2 | P2 | gpmc_cs2 | qspi1_cs0 | | | | | | | | | | | | | gpio2_20 | Driver off |
| 0x14BC | CTRL_CORE_PAD_GPMC_CS3 | P1 | gpmc_cs3 | qspi1_cs1 | vin3a_clk0 | vout3_clk | | gpmc_a1 | | | | | | | | | gpio2_21 | Driver off |
| 0x14C0 | CTRL_CORE_PAD_GPMC_CLK | P7 | gpmc_clk | gpmc_cs7 | clkout1 | gpmc_wait1 | vin4a_hsync0 | vin4a_de0 | vin3b_clk1 | timer4 | i2c3_scl | dma_evt1 | | | | | gpio2_22 | Driver off |
| 0x14C4 | CTRL_CORE_PAD_GPMC_ADVN_ALE | N1 | gpmc_advn_ale | gpmc_cs6 | clkout2 | gpmc_wait1 | vin4a_vsync0 | gpmc_a2 | gpmc_a23 | timer3 | i2c3_sda | dma_evt2 | | | | | gpio2_23 | Driver off |
| 0x14C8 | CTRL_CORE_PAD_GPMC_OEN_REN | M5 | gpmc_oen_ren | | | | | | | | | | | | | | gpio2_24 | Driver off |
| 0x14CC | CTRL_CORE_PAD_GPMC_WEN | M3 | gpmc_wen | | | | | | | | | | | | | | gpio2_25 | Driver off |
| 0x14D0 | CTRL_CORE_PAD_GPMC_BEN0 | N6 | gpmc_ben0 | gpmc_cs4 | | vin1b_hsync1 | | | vin3b_de1 | timer2 | | dma_evt3 | | | | | gpio2_26 | Driver off |
| 0x14D4 | CTRL_CORE_PAD_GPMC_BEN1 | M4 | gpmc_ben1 | gpmc_cs5 | | vin1b_de1 | vin3b_clk1 | gpmc_a3 | vin3b_fld1 | timer1 | | dma_evt4 | | | | | gpio2_27 | Driver off |
| 0x14D8 | CTRL_CORE_PAD_GPMC_WAIT0 | N2 | gpmc_wait0 | | | | | | | | | | | | | | gpio2_28 | Driver off |
| 0x14DC | CTRL_CORE_PAD_VIN1A_CLK0 | AG8 | vin1a_clk0 | | | vout3_d16 | vout3_fld | | | | | | | | | | gpio2_30 | Driver off |
| 0x14E0 | CTRL_CORE_PAD_VIN1B_CLK1 | AH7 | vin1b_clk1 | | | | | | vin3a_clk0 | | | | | | | | gpio2_31 | Driver off |
| 0x14E4 | CTRL_CORE_PAD_VIN1A_DE0 | AD9 | vin1a_de0 | vin1b_hsync1 | | vout3_d17 | vout3_de | uart7_rxd | | timer16 | spi3_sclk | kbd_row0 | eQEP1A_in | | | | gpio3_0 | Driver off |
| 0x14E8 | CTRL_CORE_PAD_VIN1A_FLD0 | AF9 | vin1a_fld0 | vin1b_vsync1 | | | vout3_clk | uart7_txd | | timer15 | spi3_d1 | kbd_row1 | eQEP1B_in | | | | gpio3_1 | Driver off |
| 0x14EC | CTRL_CORE_PAD_VIN1A_HSYNC0 | AE9 | vin1a_hsync0 | vin1b_fld1 | | | vout3_hsync | uart7_ctsn | | timer14 | spi3_d0 | | eQEP1_index | | | | gpio3_2 | Driver off |
| 0x14F0 | CTRL_CORE_PAD_VIN1A_VSYNC0 | AF8 | vin1a_vsync0 | vin1b_de1 | | | vout3_vsync | uart7_rtsn | | timer13 | spi3_cs0 | | eQEP1_strobe | | | | gpio3_3 | Driver off |
| 0x14F4 | CTRL_CORE_PAD_VIN1A_D0 | AE8 | vin1a_d0 | | | vout3_d7 | vout3_d23 | uart8_rxd | | | | | ehrpwm1A | | | | gpio3_4 | Driver off |
| 0x14F8 | CTRL_CORE_PAD_VIN1A_D1 | AD8 | vin1a_d1 | | | vout3_d6 | vout3_d22 | uart8_txd | | | | | ehrpwm1B | | | | gpio3_5 | Driver off |
| 0x14FC | CTRL_CORE_PAD_VIN1A_D2 | AG7 | vin1a_d2 | | | vout3_d5 | vout3_d21 | uart8_ctsn | | | | | ehrpwm1_tripzone_input | | | | gpio3_6 | Driver off |


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## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0x1500 | CTRL_CORE_PAD_VIN1A_D3 | AH6 | vin1a_d3 | | | vout3_d4 | vout3_d20 | uart8_rtsn | | | | | eCAP1_in_PWM1_out | | pr1_pru0_gpi0 | pr1_pru0_gpo0 | gpio3_7 | Driver off |
| 0x1504 | CTRL_CORE_PAD_VIN1A_D4 | AH3 | vin1a_d4 | | | vout3_d3 | vout3_d19 | | | | | | ehrpwm1_synci | | pr1_pru0_gpi1 | pr1_pru0_gpo1 | gpio3_8 | Driver off |
| 0x1508 | CTRL_CORE_PAD_VIN1A_D5 | AH5 | vin1a_d5 | | | vout3_d2 | vout3_d18 | | | | | | ehrpwm1_synco | | pr1_pru0_gpi2 | pr1_pru0_gpo2 | gpio3_9 | Driver off |
| 0x150C | CTRL_CORE_PAD_VIN1A_D6 | AG6 | vin1a_d6 | | | vout3_d1 | vout3_d17 | | | | | | eQEP2A_in | | pr1_pru0_gpi3 | pr1_pru0_gpo3 | gpio3_10 | Driver off |
| 0x1510 | CTRL_CORE_PAD_VIN1A_D7 | AH4 | vin1a_d7 | | | vout3_d0 | vout3_d16 | | | | | | eQEP2B_in | | pr1_pru0_gpi4 | pr1_pru0_gpo4 | gpio3_11 | Driver off |
| 0x1514 | CTRL_CORE_PAD_VIN1A_D8 | AG4 | vin1a_d8 | vin1b_d7 | | | vout3_d15 | | | | | kbd_row2 | eQEP2_index | | pr1_pru0_gpi5 | pr1_pru0_gpo5 | gpio3_12 | Driver off |
| 0x1518 | CTRL_CORE_PAD_VIN1A_D9 | AG2 | vin1a_d9 | vin1b_d6 | | | vout3_d14 | | | | | kbd_row3 | eQEP2_strobe | | pr1_pru0_gpi6 | pr1_pru0_gpo6 | gpio3_13 | Driver off |
| 0x151C | CTRL_CORE_PAD_VIN1A_D10 | AG3 | vin1a_d10 | vin1b_d5 | | | vout3_d13 | | | | | kbd_row4 | pr1_edc_latch0_in | | pr1_pru0_gpi7 | pr1_pru0_gpo7 | gpio3_14 | Driver off |
| 0x1520 | CTRL_CORE_PAD_VIN1A_D11 | AG5 | vin1a_d11 | vin1b_d4 | | | vout3_d12 | gpmc_a23 | | | | kbd_row5 | pr1_edc_latch1_in | | pr1_pru0_gpi8 | pr1_pru0_gpo8 | gpio3_15 | Driver off |
| 0x1524 | CTRL_CORE_PAD_VIN1A_D12 | AF2 | vin1a_d12 | vin1b_d3 | | | vout3_d11 | gpmc_a24 | | | | kbd_row6 | pr1_edc_sync0_out | | pr1_pru0_gpi9 | pr1_pru0_gpo9 | gpio3_16 | Driver off |
| 0x1528 | CTRL_CORE_PAD_VIN1A_D13 | AF6 | vin1a_d13 | vin1b_d2 | | | vout3_d10 | gpmc_a25 | | | | kbd_row7 | pr1_edc_sync1_out | | pr1_pru0_gpi10 | pr1_pru0_gpo10 | gpio3_17 | Driver off |
| 0x152C | CTRL_CORE_PAD_VIN1A_D14 | AF3 | vin1a_d14 | vin1b_d1 | | | vout3_d9 | gpmc_a26 | | | | kbd_row8 | pr1_edio_latch_in | | pr1_pru0_gpi11 | pr1_pru0_gpo11 | gpio3_18 | Driver off |
| 0x1530 | CTRL_CORE_PAD_VIN1A_D15 | AF4 | vin1a_d15 | vin1b_d0 | | | vout3_d8 | gpmc_a27 | | | | kbd_col0 | pr1_edio_sof | | pr1_pru0_gpi12 | pr1_pru0_gpo12 | gpio3_19 | Driver off |
| 0x1534 | CTRL_CORE_PAD_VIN1A_D16 | AF1 | vin1a_d16 | vin1b_d7 | | | vout3_d7 | | vin3a_d0 | | | kbd_col1 | pr1_edio_data_in0 | pr1_edio_data_out0 | pr1_pru0_gpi13 | pr1_pru0_gpo13 | gpio3_20 | Driver off |
| 0x1538 | CTRL_CORE_PAD_VIN1A_D17 | AE3 | vin1a_d17 | vin1b_d6 | | | vout3_d6 | | vin3a_d1 | | | kbd_col2 | pr1_edio_data_in1 | pr1_edio_data_out1 | pr1_pru0_gpi14 | pr1_pru0_gpo14 | gpio3_21 | Driver off |
| 0x153C | CTRL_CORE_PAD_VIN1A_D18 | AE5 | vin1a_d18 | vin1b_d5 | | | vout3_d5 | | vin3a_d2 | | | kbd_col3 | pr1_edio_data_in2 | pr1_edio_data_out2 | pr1_pru0_gpi15 | pr1_pru0_gpo15 | gpio3_22 | Driver off |
| 0x1540 | CTRL_CORE_PAD_VIN1A_D19 | AE1 | vin1a_d19 | vin1b_d4 | | | vout3_d4 | | vin3a_d3 | | | kbd_col4 | pr1_edio_data_in3 | pr1_edio_data_out3 | pr1_pru0_gpi16 | pr1_pru0_gpo16 | gpio3_23 | Driver off |
| 0x1544 | CTRL_CORE_PAD_VIN1A_D20 | AE2 | vin1a_d20 | vin1b_d3 | | | vout3_d3 | | vin3a_d4 | | | kbd_col5 | pr1_edio_data_in4 | pr1_edio_data_out4 | pr1_pru0_gpi17 | pr1_pru0_gpo17 | gpio3_24 | Driver off |
| 0x1548 | CTRL_CORE_PAD_VIN1A_D21 | AE6 | vin1a_d21 | vin1b_d2 | | | vout3_d2 | | vin3a_d5 | | | kbd_col6 | pr1_edio_data_in5 | pr1_edio_data_out5 | pr1_pru0_gpi18 | pr1_pru0_gpo18 | gpio3_25 | Driver off |
| 0x154C | CTRL_CORE_PAD_VIN1A_D22 | AD2 | vin1a_d22 | vin1b_d1 | | | vout3_d1 | | vin3a_d6 | | | kbd_col7 | pr1_edio_data_in6 | pr1_edio_data_out6 | pr1_pru0_gpi19 | pr1_pru0_gpo19 | gpio3_26 | Driver off |
| 0x1550 | CTRL_CORE_PAD_VIN1A_D23 | AD3 | vin1a_d23 | vin1b_d0 | | | vout3_d0 | | vin3a_d7 | | | kbd_col8 | pr1_edio_data_in7 | pr1_edio_data_out7 | pr1_pru0_gpi20 | pr1_pru0_gpo20 | gpio3_27 | Driver off |
| 0x1554 | CTRL_CORE_PAD_VIN2A_CLK0 | E1 | vin2a_clk0 | | | | vout2_fld | emu5 | | | | kbd_row0 | eQEP1A_in | | pr1_edio_data_in0 | pr1_edio_data_out0 | gpio3_28 | Driver off |
| 0x1558 | CTRL_CORE_PAD_VIN2A_DE0 | G2 | vin2a_de0 | vin2a_fld0 | vin2b_fld1 | vin2b_de1 | vout2_de | emu6 | | | | kbd_row1 | eQEP1B_in | | pr1_edio_data_in1 | pr1_edio_data_out1 | gpio3_29 | Driver off |
| 0x155C | CTRL_CORE_PAD_VIN2A_FLD0 | H7 | vin2a_fld0 | | vin2b_clk1 | | vout2_clk | emu7 | | | | | eQEP1_index | | pr1_edio_data_in2 | pr1_edio_data_out2 | gpio3_30 | Driver off |

## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0x1560 | CTRL_CORE_PAD_VIN2A_HSYNC0 | G1 | vin2a_hsync0 | | | vin2b_hsync1 | vout2_hsync | emu8 | | uart9_rxd | spi4_sclk | kbd_row2 | eQEP1_strobe | pr1_uart0_cts_n | pr1_edio_data_in3 | pr1_edio_data_out3 | gpio3_31 | Driver off |
| 0x1564 | CTRL_CORE_PAD_VIN2A_VSYNC0 | G6 | vin2a_vsync0 | | | vin2b_vsync1 | vout2_vsync | emu9 | | uart9_txd | spi4_d1 | kbd_row3 | ehrpwm1A | pr1_uart0_rts_n | pr1_edio_data_in4 | pr1_edio_data_out4 | gpio4_0 | Driver off |
| 0x1568 | CTRL_CORE_PAD_VIN2A_D0 | F2 | vin2a_d0 | | | | vout2_d23 | emu10 | | uart9_ctsn | spi4_d0 | kbd_row4 | ehrpwm1B | pr1_uart0_rxd | pr1_edio_data_in5 | pr1_edio_data_out5 | gpio4_1 | Driver off |
| 0x156C | CTRL_CORE_PAD_VIN2A_D1 | F3 | vin2a_d1 | | | | vout2_d22 | emu11 | | uart9_rtsn | spi4_cs0 | kbd_row5 | ehrpwm1_tripzone_input | pr1_uart0_txd | pr1_edio_data_in6 | pr1_edio_data_out6 | gpio4_2 | Driver off |
| 0x1570 | CTRL_CORE_PAD_VIN2A_D2 | D1 | vin2a_d2 | | | | vout2_d21 | emu12 | | | uart10_rxd | kbd_row6 | eCAP1_in_PWM1_out | pr1_ecap0_ecap_capin_apwm_o | pr1_edio_data_in7 | pr1_edio_data_out7 | gpio4_3 | Driver off |
| 0x1574 | CTRL_CORE_PAD_VIN2A_D3 | E2 | vin2a_d3 | | | | vout2_d20 | emu13 | | | uart10_txd | kbd_col0 | ehrpwm1_synci | pr1_edc_latch0_in | pr1_pru1_gpi0 | pr1_pru1_gpo0 | gpio4_4 | Driver off |
| 0x1578 | CTRL_CORE_PAD_VIN2A_D4 | D2 | vin2a_d4 | | | | vout2_d19 | emu14 | | | uart10_ctsn | kbd_col1 | ehrpwm1_synco | pr1_edc_sync0_out | pr1_pru1_gpi1 | pr1_pru1_gpo1 | gpio4_5 | Driver off |
| 0x157C | CTRL_CORE_PAD_VIN2A_D5 | F4 | vin2a_d5 | | | | vout2_d18 | emu15 | | | uart10_rtsn | kbd_col2 | eQEP2A_in | pr1_edio_sof | pr1_pru1_gpi2 | pr1_pru1_gpo2 | gpio4_6 | Driver off |
| 0x1580 | CTRL_CORE_PAD_VIN2A_D6 | C1 | vin2a_d6 | | | | vout2_d17 | emu16 | | | mii1_rxd1 | kbd_col3 | eQEP2B_in | pr1_mii_mt1_clk | pr1_pru1_gpi3 | pr1_pru1_gpo3 | gpio4_7 | Driver off |
| 0x1584 | CTRL_CORE_PAD_VIN2A_D7 | E4 | vin2a_d7 | | | | vout2_d16 | emu17 | | | mii1_rxd2 | kbd_col4 | eQEP2_index | pr1_mii1_txen | pr1_pru1_gpi4 | pr1_pru1_gpo4 | gpio4_8 | Driver off |
| 0x1588 | CTRL_CORE_PAD_VIN2A_D8 | F5 | vin2a_d8 | | | | vout2_d15 | emu18 | | | mii1_rxd3 | kbd_col5 | eQEP2_strobe | pr1_mii1_txd3 | pr1_pru1_gpi5 | pr1_pru1_gpo5 | gpio4_9 | Driver off |
| 0x158C | CTRL_CORE_PAD_VIN2A_D9 | E6 | vin2a_d9 | | | | vout2_d14 | emu19 | | | mii1_rxd0 | kbd_col6 | ehrpwm2A | pr1_mii1_txd2 | pr1_pru1_gpi6 | pr1_pru1_gpo6 | gpio4_10 | Driver off |
| 0x1590 | CTRL_CORE_PAD_VIN2A_D10 | D3 | vin2a_d10 | | | mdio_mclk | vout2_d13 | | | | | kbd_col7 | ehrpwm2B | pr1_mdio_mdclk | pr1_pru1_gpi7 | pr1_pru1_gpo7 | gpio4_11 | Driver off |
| 0x1594 | CTRL_CORE_PAD_VIN2A_D11 | F6 | vin2a_d11 | | | mdio_d | vout2_d12 | | | | | kbd_row7 | ehrpwm2_tripzone_input | pr1_mdio_data | pr1_pru1_gpi8 | pr1_pru1_gpo8 | gpio4_12 | Driver off |
| 0x1598 | CTRL_CORE_PAD_VIN2A_D12 | D5 | vin2a_d12 | | | rgmii1_txc | vout2_d11 | | | | mii1_rxclk | kbd_col8 | eCAP2_in_PWM2_out | pr1_mii1_txd1 | pr1_pru1_gpi9 | pr1_pru1_gpo9 | gpio4_13 | Driver off |
| 0x159C | CTRL_CORE_PAD_VIN2A_D13 | C2 | vin2a_d13 | | | rgmii1_txctl | vout2_d10 | | | | mii1_rxdv | kbd_row8 | eQEP3A_in | pr1_mii1_txd0 | pr1_pru1_gpi10 | pr1_pru1_gpo10 | gpio4_14 | Driver off |
| 0x15A0 | CTRL_CORE_PAD_VIN2A_D14 | C3 | vin2a_d14 | | | rgmii1_txd3 | vout2_d9 | | | | mii1_txclk | | eQEP3B_in | pr1_mii_mr1_clk | pr1_pru1_gpi11 | pr1_pru1_gpo11 | gpio4_15 | Driver off |
| 0x15A4 | CTRL_CORE_PAD_VIN2A_D15 | C4 | vin2a_d15 | | | rgmii1_txd2 | vout2_d8 | | | | mii1_txd0 | | eQEP3_index | pr1_mii1_rxdv | pr1_pru1_gpi12 | pr1_pru1_gpo12 | gpio4_16 | Driver off |
| 0x15A8 | CTRL_CORE_PAD_VIN2A_D16 | B2 | vin2a_d16 | | vin2b_d7 | rgmii1_txd1 | vout2_d7 | | vin3a_d8 | | mii1_txd1 | | eQEP3_strobe | pr1_mii1_rxd3 | pr1_pru1_gpi13 | pr1_pru1_gpo13 | gpio4_24 | Driver off |
| 0x15AC | CTRL_CORE_PAD_VIN2A_D17 | D6 | vin2a_d17 | | vin2b_d6 | rgmii1_txd0 | vout2_d6 | | vin3a_d9 | | mii1_txd2 | | ehrpwm3A | pr1_mii1_rxd2 | pr1_pru1_gpi14 | pr1_pru1_gpo14 | gpio4_25 | Driver off |
| 0x15B0 | CTRL_CORE_PAD_VIN2A_D18 | C5 | vin2a_d18 | | vin2b_d5 | rgmii1_rxc | vout2_d5 | | vin3a_d10 | | mii1_txd3 | | ehrpwm3B | pr1_mii1_rxd1 | pr1_pru1_gpi15 | pr1_pru1_gpo15 | gpio4_26 | Driver off |
| 0x15B4 | CTRL_CORE_PAD_VIN2A_D19 | A3 | vin2a_d19 | | vin2b_d4 | rgmii1_rxctl | vout2_d4 | | vin3a_d11 | | mii1_txer | | ehrpwm3_tripzone_input | pr1_mii1_rxd0 | pr1_pru1_gpi16 | pr1_pru1_gpo16 | gpio4_27 | Driver off |


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## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0x15B8 | CTRL_CORE_PAD_VIN2A_D20 | B3 | vin2a_d20 | | vin2b_d3 | rgmii1_rxd3 | vout2_d3 | vin3a_de0 | vin3a_d12 | | mii1_rxer | | eCAP3_in_PWM3_out | pr1_mii1_rxer | pr1_pru1_gpi17 | pr1_pru1_gpo17 | gpio4_28 | Driver off |
| 0x15BC | CTRL_CORE_PAD_VIN2A_D21 | B4 | vin2a_d21 | | vin2b_d2 | rgmii1_rxd2 | vout2_d2 | vin3a_fld0 | vin3a_d13 | | mii1_col | | | pr1_mii1_rxlink | pr1_pru1_gpi18 | pr1_pru1_gpo18 | gpio4_29 | Driver off |
| 0x15C0 | CTRL_CORE_PAD_VIN2A_D22 | B5 | vin2a_d22 | | vin2b_d1 | rgmii1_rxd1 | vout2_d1 | vin3a_hsync0 | vin3a_d14 | | mii1_crs | | | pr1_mii1_col | pr1_pru1_gpi19 | pr1_pru1_gpo19 | gpio4_30 | Driver off |
| 0x15C4 | CTRL_CORE_PAD_VIN2A_D23 | A4 | vin2a_d23 | | vin2b_d0 | rgmii1_rxd0 | vout2_d0 | vin3a_vsync0 | vin3a_d15 | | mii1_txen | | | pr1_mii1_crs | pr1_pru1_gpi20 | pr1_pru1_gpo20 | gpio4_31 | Driver off |
| 0x15C8 | CTRL_CORE_PAD_VOUT1_CLK | D11 | vout1_clk | | | vin4a_fld0 | vin3a_fld0 | | | | spi3_cs0 | | | | | | gpio4_19 | Driver off |
| 0x15CC | CTRL_CORE_PAD_VOUT1_DE | B10 | vout1_de | | | vin4a_de0 | vin3a_de0 | | | | spi3_d1 | | | | | | gpio4_20 | Driver off |
| 0x15D0 | CTRL_CORE_PAD_VOUT1_FLD | B11 | vout1_fld | | | vin4a_clk0 | vin3a_clk0 | | | | spi3_cs1 | | | | | | gpio4_21 | Driver off |
| 0x15D4 | CTRL_CORE_PAD_VOUT1_HSYNC | C11 | vout1_hsync | | | vin4a_hsync0 | vin3a_hsync0 | | | | spi3_d0 | | | | | | gpio4_22 | Driver off |
| 0x15D8 | CTRL_CORE_PAD_VOUT1_VSYNC | E11 | vout1_vsync | | | vin4a_vsync0 | vin3a_vsync0 | | | | spi3_sclk | | | | pr2_pru1_gpi17 | pr2_pru1_gpo17 | gpio4_23 | Driver off |
| 0x15DC | CTRL_CORE_PAD_VOUT1_D0 | F11 | vout1_d0 | | uart5_rxd | vin4a_d16 | vin3a_d16 | | | | spi3_cs2 | | pr1_uart0_cts_n | | pr2_pru1_gpi18 | pr2_pru1_gpo18 | gpio8_0 | Driver off |
| 0x15E0 | CTRL_CORE_PAD_VOUT1_D1 | G10 | vout1_d1 | | uart5_txd | vin4a_d17 | vin3a_d17 | | | | | | pr1_uart0_rts_n | | pr2_pru1_gpi19 | pr2_pru1_gpo19 | gpio8_1 | Driver off |
| 0x15E4 | CTRL_CORE_PAD_VOUT1_D2 | F10 | vout1_d2 | | emu2 | vin4a_d18 | vin3a_d18 | obs0 | obs16 | obs_irq1 | | | pr1_uart0_rxd | | pr2_pru1_gpi20 | pr2_pru1_gpo20 | gpio8_2 | Driver off |
| 0x15E8 | CTRL_CORE_PAD_VOUT1_D3 | G11 | vout1_d3 | | emu5 | vin4a_d19 | vin3a_d19 | obs1 | obs17 | obs_dmarq1 | | | pr1_uart0_txd | | pr2_pru0_gpi0 | pr2_pru0_gpo0 | gpio8_3 | Driver off |
| 0x15EC | CTRL_CORE_PAD_VOUT1_D4 | E9 | vout1_d4 | | emu6 | vin4a_d20 | vin3a_d20 | obs2 | obs18 | | | | pr1_ecap0_ecap_capin_apwm_o | | pr2_pru0_gpi1 | pr2_pru0_gpo1 | gpio8_4 | Driver off |
| 0x15F0 | CTRL_CORE_PAD_VOUT1_D5 | F9 | vout1_d5 | | emu7 | vin4a_d21 | vin3a_d21 | obs3 | obs19 | | | | pr2_edc_latch0_in | | pr2_pru0_gpi2 | pr2_pru0_gpo2 | gpio8_5 | Driver off |
| 0x15F4 | CTRL_CORE_PAD_VOUT1_D6 | F8 | vout1_d6 | | emu8 | vin4a_d22 | vin3a_d22 | obs4 | obs20 | | | | pr2_edc_latch1_in | | pr2_pru0_gpi3 | pr2_pru0_gpo3 | gpio8_6 | Driver off |
| 0x15F8 | CTRL_CORE_PAD_VOUT1_D7 | E7 | vout1_d7 | | emu9 | vin4a_d23 | vin3a_d23 | | | | | | pr2_edc_sync0_out | | pr2_pru0_gpi4 | pr2_pru0_gpo4 | gpio8_7 | Driver off |
| 0x15FC | CTRL_CORE_PAD_VOUT1_D8 | E8 | vout1_d8 | | uart6_rxd | vin4a_d8 | vin3a_d8 | | | | | | pr2_edc_sync1_out | | pr2_pru0_gpi5 | pr2_pru0_gpo5 | gpio8_8 | Driver off |
| 0x1600 | CTRL_CORE_PAD_VOUT1_D9 | D9 | vout1_d9 | | uart6_txd | vin4a_d9 | vin3a_d9 | | | | | | pr2_edio_latch_in | | pr2_pru0_gpi6 | pr2_pru0_gpo6 | gpio8_9 | Driver off |
| 0x1604 | CTRL_CORE_PAD_VOUT1_D10 | D7 | vout1_d10 | | emu3 | vin4a_d10 | vin3a_d10 | obs5 | obs21 | obs_irq2 | | | pr2_edio_sof | | pr2_pru0_gpi7 | pr2_pru0_gpo7 | gpio8_10 | Driver off |
| 0x1608 | CTRL_CORE_PAD_VOUT1_D11 | D8 | vout1_d11 | | emu10 | vin4a_d11 | vin3a_d11 | obs6 | obs22 | obs_dmarq2 | | | pr2_uart0_cts_n | | pr2_pru0_gpi8 | pr2_pru0_gpo8 | gpio8_11 | Driver off |
| 0x160C | CTRL_CORE_PAD_VOUT1_D12 | A5 | vout1_d12 | | emu11 | vin4a_d12 | vin3a_d12 | obs7 | obs23 | | | | pr2_uart0_rts_n | | pr2_pru0_gpi9 | pr2_pru0_gpo9 | gpio8_12 | Driver off |
| 0x1610 | CTRL_CORE_PAD_VOUT1_D13 | C6 | vout1_d13 | | emu12 | vin4a_d13 | vin3a_d13 | obs8 | obs24 | | | | pr2_uart0_rxd | | pr2_pru0_gpi10 | pr2_pru0_gpo10 | gpio8_13 | Driver off |

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## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0x1614 | CTRL_CORE_PAD_VOUT1_D14 | C8 | vout1_d14 | | emu13 | vin4a_d14 | vin3a_d14 | obs9 | obs25 | | | | pr2_uart0_txd | | pr2_pru0_gpi11 | pr2_pru0_gpo11 | gpio8_14 | Driver off |
| 0x1618 | CTRL_CORE_PAD_VOUT1_D15 | C7 | vout1_d15 | | emu14 | vin4a_d15 | vin3a_d15 | obs10 | obs26 | | | | pr2_ecap0_ecap_capin_apwm_o | | pr2_pru0_gpi12 | pr2_pru0_gpo12 | gpio8_15 | Driver off |
| 0x161C | CTRL_CORE_PAD_VOUT1_D16 | B7 | vout1_d16 | | uart7_rxd | vin4a_d0 | vin3a_d0 | | | | | | pr2_edio_data_in0 | pr2_edio_data_out0 | pr2_pru0_gpi13 | pr2_pru0_gpo13 | gpio8_16 | Driver off |
| 0x1620 | CTRL_CORE_PAD_VOUT1_D17 | B8 | vout1_d17 | | uart7_txd | vin4a_d1 | vin3a_d1 | | | | | | pr2_edio_data_in1 | pr2_edio_data_out1 | pr2_pru0_gpi14 | pr2_pru0_gpo14 | gpio8_17 | Driver off |
| 0x1624 | CTRL_CORE_PAD_VOUT1_D18 | A7 | vout1_d18 | | emu4 | vin4a_d2 | vin3a_d2 | obs11 | obs27 | | | | pr2_edio_data_in2 | pr2_edio_data_out2 | pr2_pru0_gpi15 | pr2_pru0_gpo15 | gpio8_18 | Driver off |
| 0x1628 | CTRL_CORE_PAD_VOUT1_D19 | A8 | vout1_d19 | | emu15 | vin4a_d3 | vin3a_d3 | obs12 | obs28 | | | | pr2_edio_data_in3 | pr2_edio_data_out3 | pr2_pru0_gpi16 | pr2_pru0_gpo16 | gpio8_19 | Driver off |
| 0x162C | CTRL_CORE_PAD_VOUT1_D20 | C9 | vout1_d20 | | emu16 | vin4a_d4 | vin3a_d4 | obs13 | obs29 | | | | pr2_edio_data_in4 | pr2_edio_data_out4 | pr2_pru0_gpi17 | pr2_pru0_gpo17 | gpio8_20 | Driver off |
| 0x1630 | CTRL_CORE_PAD_VOUT1_D21 | A9 | vout1_d21 | | emu17 | vin4a_d5 | vin3a_d5 | obs14 | obs30 | | | | pr2_edio_data_in5 | pr2_edio_data_out5 | pr2_pru0_gpi18 | pr2_pru0_gpo18 | gpio8_21 | Driver off |
| 0x1634 | CTRL_CORE_PAD_VOUT1_D22 | B9 | vout1_d22 | | emu18 | vin4a_d6 | vin3a_d6 | obs15 | obs31 | | | | pr2_edio_data_in6 | pr2_edio_data_out6 | pr2_pru0_gpi19 | pr2_pru0_gpo19 | gpio8_22 | Driver off |
| 0x1638 | CTRL_CORE_PAD_VOUT1_D23 | A10 | vout1_d23 | | emu19 | vin4a_d7 | vin3a_d7 | | | | spi3_cs3 | | pr2_edio_data_in7 | pr2_edio_data_out7 | pr2_pru0_gpi20 | pr2_pru0_gpo20 | gpio8_23 | Driver off |
| 0x163C | CTRL_CORE_PAD_MDIO_MCLK | V1 | mdio_mclk | uart3_rtsn | | mii0_col | vin2a_clk0 | vin4b_clk1 | | | | | | pr1_mii0_col | pr2_pru1_gpi0 | pr2_pru1_gpo0 | gpio5_15 | Driver off |
| 0x1640 | CTRL_CORE_PAD_MDIO_D | U4 | mdio_d | uart3_ctsn | | mii0_txer | vin2a_d0 | vin4b_d0 | | | | | | pr1_mii0_rxlink | pr2_pru1_gpi1 | pr2_pru1_gpo1 | gpio5_16 | Driver off |
| 0x1644 | CTRL_CORE_PAD_RMII_MHZ_50_CLK | U3 | RMII_MHZ_50_CLK | | | | vin2a_d11 | | | | | | | | pr2_pru1_gpi2 | pr2_pru1_gpo2 | gpio5_17 | Driver off |
| 0x1648 | CTRL_CORE_PAD_UART3_RXD | V2 | uart3_rxd | | rmii1_crs | mii0_rxdv | vin2a_d1 | vin4b_d1 | | spi3_sclk | | | | pr1_mii0_rxdv | pr2_pru1_gpi3 | pr2_pru1_gpo3 | gpio5_18 | Driver off |
| 0x164C | CTRL_CORE_PAD_UART3_TXD | Y1 | uart3_txd | | rmii1_rxer | mii0_rxclk | vin2a_d2 | vin4b_d2 | | spi3_d1 | spi4_cs1 | | | pr1_mii_mr0_clk | pr2_pru1_gpi4 | pr2_pru1_gpo4 | gpio5_19 | Driver off |
| 0x1650 | CTRL_CORE_PAD_RGMII0_TXC | W9 | rgmii0_txc | uart3_ctsn | rmii1_rxd1 | mii0_rxd3 | vin2a_d3 | vin4b_d3 | | spi3_d0 | spi4_cs2 | | | pr1_mii0_rxd3 | pr2_pru1_gpi5 | pr2_pru1_gpo5 | gpio5_20 | Driver off |
| 0x1654 | CTRL_CORE_PAD_RGMII0_TXCTL | V9 | rgmii0_txctl | uart3_rtsn | rmii1_rxd0 | mii0_rxd2 | vin2a_d4 | vin4b_d4 | | spi3_cs0 | spi4_cs3 | | | pr1_mii0_rxd2 | pr2_pru1_gpi6 | pr2_pru1_gpo6 | gpio5_21 | Driver off |
| 0x1658 | CTRL_CORE_PAD_RGMII0_TXD3 | V7 | rgmii0_txd3 | rmii0_crs | | mii0_crs | vin2a_de0 | vin4b_de1 | | spi4_sclk | uart4_rxd | | | pr1_mii0_crs | pr2_pru1_gpi7 | pr2_pru1_gpo7 | gpio5_22 | Driver off |
| 0x165C | CTRL_CORE_PAD_RGMII0_TXD2 | U7 | rgmii0_txd2 | rmii0_rxer | | mii0_rxer | vin2a_hsync0 | vin4b_hsync1 | | spi4_d1 | uart4_txd | | | pr1_mii0_rxer | pr2_pru1_gpi8 | pr2_pru1_gpo8 | gpio5_23 | Driver off |
| 0x1660 | CTRL_CORE_PAD_RGMII0_TXD1 | V6 | rgmii0_txd1 | rmii0_rxd1 | | mii0_rxd1 | vin2a_vsync0 | vin4b_vsync1 | | spi4_d0 | uart4_ctsn | | | pr1_mii0_rxd1 | pr2_pru1_gpi9 | pr2_pru1_gpo9 | gpio5_24 | Driver off |
| 0x1664 | CTRL_CORE_PAD_RGMII0_TXD0 | U6 | rgmii0_txd0 | rmii0_rxd0 | | mii0_rxd0 | vin2a_d10 | | | spi4_cs0 | uart4_rtsn | | | pr1_mii0_rxd0 | pr2_pru1_gpi10 | pr2_pru1_gpo10 | gpio5_25 | Driver off |
| 0x1668 | CTRL_CORE_PAD_RGMII0_RXC | U5 | rgmii0_rxc | | rmii1_txen | mii0_txclk | vin2a_d5 | vin4b_d5 | | | | | | pr1_mii_mt0_clk | pr2_pru1_gpi11 | pr2_pru1_gpo11 | gpio5_26 | Driver off |
| 0x166C | CTRL_CORE_PAD_RGMII0_RXCTL | V5 | rgmii0_rxctl | | rmii1_txd1 | mii0_txd3 | vin2a_d6 | vin4b_d6 | | | | | | pr1_mii0_txd3 | pr2_pru1_gpi12 | pr2_pru1_gpo12 | gpio5_27 | Driver off |


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## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0x1670 | CTRL_CORE_PAD_RGMII0_RXD3 | V4 | rgmii0_rxd3 | | rmii1_txd0 | mii0_txd2 | vin2a_d7 | vin4b_d7 | | | | | | pr1_mii0_txd2 | pr2_pru1_gpi13 | pr2_pru1_gpo13 | gpio5_28 | Driver off |
| 0x1674 | CTRL_CORE_PAD_RGMII0_RXD2 | V3 | rgmii0_rxd2 | rmii0_txen | | mii0_txen | vin2a_d8 | | | | | | | pr1_mii0_txen | pr2_pru1_gpi14 | pr2_pru1_gpo14 | gpio5_29 | Driver off |
| 0x1678 | CTRL_CORE_PAD_RGMII0_RXD1 | Y2 | rgmii0_rxd1 | rmii0_txd1 | | mii0_txd1 | vin2a_d9 | | | | | | | pr1_mii0_txd1 | pr2_pru1_gpi15 | pr2_pru1_gpo15 | gpio5_30 | Driver off |
| 0x167C | CTRL_CORE_PAD_RGMII0_RXD0 | W2 | rgmii0_rxd0 | rmii0_txd0 | | mii0_txd0 | vin2a_fld0 | vin4b_fld1 | | | | | | pr1_mii0_txd0 | pr2_pru1_gpi16 | pr2_pru1_gpo16 | gpio5_31 | Driver off |
| 0x1680 | CTRL_CORE_PAD_USB1_DRVVBUS | AB10 | usb1_drvvbus | | | | | | | timer16 | | | | | | | gpio6_12 | Driver off |
| 0x1684 | CTRL_CORE_PAD_USB2_DRVVBUS | AC10 | usb2_drvvbus | | | | | | | timer15 | | | | | | | gpio6_13 | Driver off |
| 0x1688 | CTRL_CORE_PAD_GPIO6_14 | E21 | gpio6_14 | mcasp1_axr8 | dcan2_tx | uart10_rxd | | | vout2_hsync | | vin4a_hsync0 | i2c3_sda | timer1 | | | | gpio6_14 | Driver off |
| 0x168C | CTRL_CORE_PAD_GPIO6_15 | F20 | gpio6_15 | mcasp1_axr9 | dcan2_rx | uart10_txd | | | vout2_vsync | | vin4a_vsync0 | i2c3_scl | timer2 | | | | gpio6_15 | Driver off |
| 0x1690 | CTRL_CORE_PAD_GPIO6_16 | F21 | gpio6_16 | mcasp1_axr10 | | | | | vout2_fld | | vin4a_fld0 | clkout1 | timer3 | | | | gpio6_16 | Driver off |
| 0x1694 | CTRL_CORE_PAD_XREF_CLK0 | D18 | xref_clk0 | mcasp2_axr8 | mcasp1_axr4 | mcasp1_ahclkx | mcasp5_ahclkx | | | vin6a_d0 | hdq0 | clkout2 | timer13 | pr2_mii1_col | pr2_pru1_gpi5 | pr2_pru1_gpo5 | gpio6_17 | Driver off |
| 0x1698 | CTRL_CORE_PAD_XREF_CLK1 | E17 | xref_clk1 | mcasp2_axr9 | mcasp1_axr5 | mcasp2_ahclkx | mcasp6_ahclkx | | | vin6a_clk0 | | | timer14 | pr2_mii1_crs | pr2_pru1_gpi6 | pr2_pru1_gpo6 | gpio6_18 | Driver off |
| 0x169C | CTRL_CORE_PAD_XREF_CLK2 | B26 | xref_clk2 | mcasp2_axr10 | mcasp1_axr6 | mcasp3_ahclkx | mcasp7_ahclkx | | vout2_clk | | vin4a_clk0 | | timer15 | | | | gpio6_19 | Driver off |
| 0x16A0 | CTRL_CORE_PAD_XREF_CLK3 | C23 | xref_clk3 | mcasp2_axr11 | mcasp1_axr7 | mcasp4_ahclkx | mcasp8_ahclkx | | vout2_de | hdq0 | vin4a_de0 | clkout3 | timer16 | | | | gpio6_20 | Driver off |
| 0x16A4 | CTRL_CORE_PAD_MCASP1_ACLKX | C14 | mcasp1_aclkx | | | | | | | vin6a_fld0 | | | i2c3_sda | pr2_mdio_mdclk | pr2_pru1_gpi7 | pr2_pru1_gpo7 | gpio7_31 | Driver off |
| 0x16A8 | CTRL_CORE_PAD_MCASP1_FSX | D14 | mcasp1_fsx | | | | | | | vin6a_de0 | | | i2c3_scl | pr2_mdio_data | | | gpio7_30 | Driver off |
| 0x16AC | CTRL_CORE_PAD_MCASP1_ACLKR | B14 | mcasp1_aclkr | mcasp7_axr2 | | | | | vout2_d0 | | vin4a_d0 | | i2c4_sda | | | | gpio5_0 | Driver off |
| 0x16B0 | CTRL_CORE_PAD_MCASP1_FSR | J14 | mcasp1_fsr | mcasp7_axr3 | | | | | vout2_d1 | | vin4a_d1 | | i2c4_scl | | | | gpio5_1 | Driver off |
| 0x16B4 | CTRL_CORE_PAD_MCASP1_AXR0 | G12 | mcasp1_axr0 | | | uart6_rxd | | | | vin6a_vsync0 | | | i2c5_sda | pr2_mii0_rxer | pr2_pru1_gpi8 | pr2_pru1_gpo8 | gpio5_2 | Driver off |
| 0x16B8 | CTRL_CORE_PAD_MCASP1_AXR1 | F12 | mcasp1_axr1 | | | uart6_txd | | | | vin6a_hsync0 | | | i2c5_scl | pr2_mii_mt0_clk | pr2_pru1_gpi9 | pr2_pru1_gpo9 | gpio5_3 | Driver off |
| 0x16BC | CTRL_CORE_PAD_MCASP1_AXR2 | G13 | mcasp1_axr2 | mcasp6_axr2 | | uart6_ctsn | | | vout2_d2 | | vin4a_d2 | | | | | | gpio5_4 | Driver off |
| 0x16C0 | CTRL_CORE_PAD_MCASP1_AXR3 | J11 | mcasp1_axr3 | mcasp6_axr3 | | uart6_rtsn | | | vout2_d3 | | vin4a_d3 | | | | | | gpio5_5 | Driver off |
| 0x16C4 | CTRL_CORE_PAD_MCASP1_AXR4 | E12 | mcasp1_axr4 | mcasp4_axr2 | | | | | vout2_d4 | | vin4a_d4 | | | | | | gpio5_6 | Driver off |
| 0x16C8 | CTRL_CORE_PAD_MCASP1_AXR5 | F13 | mcasp1_axr5 | mcasp4_axr3 | | | | | vout2_d5 | | vin4a_d5 | | | | | | gpio5_7 | Driver off |
| 0x16CC | CTRL_CORE_PAD_MCASP1_AXR6 | C12 | mcasp1_axr6 | mcasp5_axr2 | | | | | vout2_d6 | | vin4a_d6 | | | | | | gpio5_8 | Driver off |

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## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0x16D0 | CTRL_CORE_PAD_MCASP1_AXR7 | D12 | mcasp1_axr7 | mcasp5_axr3 | | | | | vout2_d7 | | vin4a_d7 | | timer4 | | | | gpio5_9 | Driver off |
| 0x16D4 | CTRL_CORE_PAD_MCASP1_AXR8 | B12 | mcasp1_axr8 | mcasp6_axr0 | | spi3_sclk | | | | vin6a_d15 | | | timer5 | pr2_mii0_txen | pr2_pru1_gpi10 | pr2_pru1_gpo10 | gpio5_10 | Driver off |
| 0x16D8 | CTRL_CORE_PAD_MCASP1_AXR9 | A11 | mcasp1_axr9 | mcasp6_axr1 | | spi3_d1 | | | | vin6a_d14 | | | timer6 | pr2_mii0_txd3 | pr2_pru1_gpi11 | pr2_pru1_gpo11 | gpio5_11 | Driver off |
| 0x16DC | CTRL_CORE_PAD_MCASP1_AXR10 | B13 | mcasp1_axr10 | mcasp6_aclkx | mcasp6_aclkr | spi3_d0 | | | | vin6a_d13 | | | timer7 | pr2_mii0_txd2 | pr2_pru1_gpi12 | pr2_pru1_gpo12 | gpio5_12 | Driver off |
| 0x16E0 | CTRL_CORE_PAD_MCASP1_AXR11 | A12 | mcasp1_axr11 | mcasp6_fsx | mcasp6_fsr | spi3_cs0 | | | | vin6a_d12 | | | timer8 | pr2_mii0_txd1 | pr2_pru1_gpi13 | pr2_pru1_gpo13 | gpio4_17 | Driver off |
| 0x16E4 | CTRL_CORE_PAD_MCASP1_AXR12 | E14 | mcasp1_axr12 | mcasp7_axr0 | | spi3_cs1 | | | | vin6a_d11 | | | timer9 | pr2_mii0_txd0 | pr2_pru1_gpi14 | pr2_pru1_gpo14 | gpio4_18 | Driver off |
| 0x16E8 | CTRL_CORE_PAD_MCASP1_AXR13 | A13 | mcasp1_axr13 | mcasp7_axr1 | | | | | | vin6a_d10 | | | timer10 | pr2_mii_mr0_clk | pr2_pru1_gpi15 | pr2_pru1_gpo15 | gpio6_4 | Driver off |
| 0x16EC | CTRL_CORE_PAD_MCASP1_AXR14 | G14 | mcasp1_axr14 | mcasp7_aclkx | mcasp7_aclkr | | | | | vin6a_d9 | | | timer11 | pr2_mii0_rxdv | pr2_pru1_gpi16 | pr2_pru1_gpo16 | gpio6_5 | Driver off |
| 0x16F0 | CTRL_CORE_PAD_MCASP1_AXR15 | F14 | mcasp1_axr15 | mcasp7_fsx | mcasp7_fsr | | | | | vin6a_d8 | | | timer12 | pr2_mii0_rxd3 | pr2_pru0_gpi20 | pr2_pru0_gpo20 | gpio6_6 | Driver off |
| 0x16F4 | CTRL_CORE_PAD_MCASP2_ACLKX | A19 | mcasp2_aclkx | | | | | | | vin6a_d7 | | | | pr2_mii0_rxd2 | pr2_pru0_gpi18 | pr2_pru0_gpo18 | | Driver off |
| 0x16F8 | CTRL_CORE_PAD_MCASP2_FSX | A18 | mcasp2_fsx | | | | | | | vin6a_d6 | | | | pr2_mii0_rxd1 | pr2_pru0_gpi19 | pr2_pru0_gpo19 | | Driver off |
| 0x16FC | CTRL_CORE_PAD_MCASP2_ACLKR | E15 | mcasp2_aclkr | mcasp8_axr2 | | | | | vout2_d8 | | vin4a_d8 | | | | | | | Driver off |
| 0x1700 | CTRL_CORE_PAD_MCASP2_FSR | A20 | mcasp2_fsr | mcasp8_axr3 | | | | | vout2_d9 | | vin4a_d9 | | | | | | | Driver off |
| 0x1704 | CTRL_CORE_PAD_MCASP2_AXR0 | B15 | mcasp2_axr0 | | | | | | vout2_d10 | | vin4a_d10 | | | | | | | Driver off |
| 0x1708 | CTRL_CORE_PAD_MCASP2_AXR1 | A15 | mcasp2_axr1 | | | | | | vout2_d11 | | vin4a_d11 | | | | | | | Driver off |
| 0x170C | CTRL_CORE_PAD_MCASP2_AXR2 | C15 | mcasp2_axr2 | mcasp3_axr2 | | | | | | vin6a_d5 | | | | pr2_mii0_rxd0 | pr2_pru0_gpi16 | pr2_pru0_gpo16 | gpio6_8 | Driver off |
| 0x1710 | CTRL_CORE_PAD_MCASP2_AXR3 | A16 | mcasp2_axr3 | mcasp3_axr3 | | | | | | vin6a_d4 | | | | pr2_mii0_rxlink | pr2_pru0_gpi17 | pr2_pru0_gpo17 | gpio6_9 | Driver off |
| 0x1714 | CTRL_CORE_PAD_MCASP2_AXR4 | D15 | mcasp2_axr4 | mcasp8_axr0 | | | | | vout2_d12 | | vin4a_d12 | | | | | | gpio1_4 | Driver off |
| 0x1718 | CTRL_CORE_PAD_MCASP2_AXR5 | B16 | mcasp2_axr5 | mcasp8_axr1 | | | | | vout2_d13 | | vin4a_d13 | | | | | | gpio6_7 | Driver off |
| 0x171C | CTRL_CORE_PAD_MCASP2_AXR6 | B17 | mcasp2_axr6 | mcasp8_aclkx | mcasp8_aclkr | | | | vout2_d14 | | vin4a_d14 | | | | | | gpio2_29 | Driver off |
| 0x1720 | CTRL_CORE_PAD_MCASP2_AXR7 | A17 | mcasp2_axr7 | mcasp8_fsx | mcasp8_fsr | | | | vout2_d15 | | vin4a_d15 | | | | | | gpio1_5 | Driver off |
| 0x1724 | CTRL_CORE_PAD_MCASP3_ACLKX | B18 | mcasp3_aclkx | mcasp3_aclkr | mcasp2_axr12 | uart7_rxd | | | | vin6a_d3 | | | | pr2_mii0_crs | pr2_pru0_gpi12 | pr2_pru0_gpo12 | gpio5_13 | Driver off |
| 0x1728 | CTRL_CORE_PAD_MCASP3_FSX | F15 | mcasp3_fsx | mcasp3_fsr | mcasp2_axr13 | uart7_txd | | | | vin6a_d2 | | | | pr2_mii0_col | pr2_pru0_gpi13 | pr2_pru0_gpo13 | gpio5_14 | Driver off |
| 0x172C | CTRL_CORE_PAD_MCASP3_AXR0 | B19 | mcasp3_axr0 | | mcasp2_axr14 | uart7_ctsn | uart5_rxd | | | vin6a_d1 | | | | pr2_mii1_rxer | pr2_pru0_gpi14 | pr2_pru0_gpo14 | | Driver off |


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## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0x1730 | CTRL_CORE_PAD_MCASP3_AXR1 | C17 | mcasp3_axr1 | | mcasp2_axr15 | uart7_rtsn | uart5_txd | | | vin6a_d0 | | vin5a_fld0 | | pr2_mii1_rxlink | pr2_pru0_gpi15 | pr2_pru0_gpo15 | | Driver off |
| 0x1734 | CTRL_CORE_PAD_MCASP4_ACLKX | C18 | mcasp4_aclkx | mcasp4_aclkr | spi3_sclk | uart8_rxd | i2c4_sda | | vout2_d16 | | vin4a_d16 | vin5a_d15 | | | | | | Driver off |
| 0x1738 | CTRL_CORE_PAD_MCASP4_FSX | A21 | mcasp4_fsx | mcasp4_fsr | spi3_d1 | uart8_txd | i2c4_scl | | vout2_d17 | | vin4a_d17 | vin5a_d14 | | | | | | Driver off |
| 0x173C | CTRL_CORE_PAD_MCASP4_AXR0 | G16 | mcasp4_axr0 | | spi3_d0 | uart8_ctsn | uart4_rxd | | vout2_d18 | | vin4a_d18 | vin5a_d13 | | | | | | Driver off |
| 0x1740 | CTRL_CORE_PAD_MCASP4_AXR1 | D17 | mcasp4_axr1 | | spi3_cs0 | uart8_rtsn | uart4_txd | | vout2_d19 | | vin4a_d19 | vin5a_d12 | | | pr2_pru1_gpi0 | pr2_pru1_gpo0 | | Driver off |
| 0x1744 | CTRL_CORE_PAD_MCASP5_ACLKX | AA3 | mcasp5_aclkx | mcasp5_aclkr | spi4_sclk | uart9_rxd | i2c5_sda | | vout2_d20 | | vin4a_d20 | vin5a_d11 | | | pr2_pru1_gpi1 | pr2_pru1_gpo1 | | Driver off |
| 0x1748 | CTRL_CORE_PAD_MCASP5_FSX | AB9 | mcasp5_fsx | mcasp5_fsr | spi4_d1 | uart9_txd | i2c5_scl | | vout2_d21 | | vin4a_d21 | vin5a_d10 | | | pr2_pru1_gpi2 | pr2_pru1_gpo2 | | Driver off |
| 0x174C | CTRL_CORE_PAD_MCASP5_AXR0 | AB3 | mcasp5_axr0 | | spi4_d0 | uart9_ctsn | uart3_rxd | | vout2_d22 | | vin4a_d22 | vin5a_d9 | | pr2_mdio_mdclk | pr2_pru1_gpi3 | pr2_pru1_gpo3 | | Driver off |
| 0x1750 | CTRL_CORE_PAD_MCASP5_AXR1 | AA4 | mcasp5_axr1 | | spi4_cs0 | uart9_rtsn | uart3_txd | | vout2_d23 | | vin4a_d23 | vin5a_d8 | | pr2_mdio_data | pr2_pru1_gpi4 | pr2_pru1_gpo4 | | Driver off |
| 0x1754 | CTRL_CORE_PAD_MMC1_CLK | W6 | mmc1_clk | | | | | | | | | | | | | | gpio6_21 | Driver off |
| 0x1758 | CTRL_CORE_PAD_MMC1_CMD | Y6 | mmc1_cmd | | | | | | | | | | | | | | gpio6_22 | Driver off |
| 0x175C | CTRL_CORE_PAD_MMC1_DAT0 | AA6 | mmc1_dat0 | | | | | | | | | | | | | | gpio6_23 | Driver off |
| 0x1760 | CTRL_CORE_PAD_MMC1_DAT1 | Y4 | mmc1_dat1 | | | | | | | | | | | | | | gpio6_24 | Driver off |
| 0x1764 | CTRL_CORE_PAD_MMC1_DAT2 | AA5 | mmc1_dat2 | | | | | | | | | | | | | | gpio6_25 | Driver off |
| 0x1768 | CTRL_CORE_PAD_MMC1_DAT3 | Y3 | mmc1_dat3 | | | | | | | | | | | | | | gpio6_26 | Driver off |
| 0x176C | CTRL_CORE_PAD_MMC1_SDCD | W7 | mmc1_sdcd | | | uart6_rxd | i2c4_sda | | | | | | | | | | gpio6_27 | Driver off |
| 0x1770 | CTRL_CORE_PAD_MMC1_SDWP | Y9 | mmc1_sdwp | | | uart6_txd | i2c4_scl | | | | | | | | | | gpio6_28 | Driver off |
| 0x1774 | CTRL_CORE_PAD_GPIO6_10 | AC5 | gpio6_10 | mdio_mclk | i2c3_sda | | vin2b_hsync1 | | | | | vin5a_clk0 | ehrpwm2A | pr2_mii_mt1_clk | pr2_pru0_gpi0 | pr2_pru0_gpo0 | gpio6_10 | Driver off |
| 0x1778 | CTRL_CORE_PAD_GPIO6_11 | AB4 | gpio6_11 | mdio_d | i2c3_scl | | vin2b_vsync1 | | | | | vin5a_de0 | ehrpwm2B | pr2_mii1_txen | pr2_pru0_gpi1 | pr2_pru0_gpo1 | gpio6_11 | Driver off |
| 0x177C | CTRL_CORE_PAD_MMC3_CLK | AD4 | mmc3_clk | | | | vin2b_d7 | | | | | vin5a_d7 | ehrpwm2_tripzone_input | pr2_mii1_txd3 | pr2_pru0_gpi2 | pr2_pru0_gpo2 | gpio6_29 | Driver off |
| 0x1780 | CTRL_CORE_PAD_MMC3_CMD | AC4 | mmc3_cmd | spi3_sclk | | | vin2b_d6 | | | | | vin5a_d6 | eCAP2_in_PWM2_out | pr2_mii1_txd2 | pr2_pru0_gpi3 | pr2_pru0_gpo3 | gpio6_30 | Driver off |
| 0x1784 | CTRL_CORE_PAD_MMC3_DAT0 | AC7 | mmc3_dat0 | spi3_d1 | uart5_rxd | | vin2b_d5 | | | | | vin5a_d5 | eQEP3A_in | pr2_mii1_txd1 | pr2_pru0_gpi4 | pr2_pru0_gpo4 | gpio6_31 | Driver off |
| 0x1788 | CTRL_CORE_PAD_MMC3_DAT1 | AC6 | mmc3_dat1 | spi3_d0 | uart5_txd | | vin2b_d4 | | | | | vin5a_d4 | eQEP3B_in | pr2_mii1_txd0 | pr2_pru0_gpi5 | pr2_pru0_gpo5 | gpio7_0 | Driver off |

## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0x178C | CTRL_CORE_PAD_MMC3_DAT2 | AC9 | mmc3_dat2 | spi3_cs0 | uart5_ctsn | | vin2b_d3 | | | | | vin5a_d3 | eQEP3_index | pr2_mii_mr1_clk | pr2_pru0_gpi6 | pr2_pru0_gpo6 | gpio7_1 | Driver off |
| 0x1790 | CTRL_CORE_PAD_MMC3_DAT3 | AC3 | mmc3_dat3 | spi3_cs1 | uart5_rtsn | | vin2b_d2 | | | | | vin5a_d2 | eQEP3_strobe | pr2_mii1_rxdv | pr2_pru0_gpi7 | pr2_pru0_gpo7 | gpio7_2 | Driver off |
| 0x1794 | CTRL_CORE_PAD_MMC3_DAT4 | AC8 | mmc3_dat4 | spi4_sclk | uart10_rxd | | vin2b_d1 | | | | | vin5a_d1 | ehrpwm3A | pr2_mii1_rxd3 | pr2_pru0_gpi8 | pr2_pru0_gpo8 | gpio1_22 | Driver off |
| 0x1798 | CTRL_CORE_PAD_MMC3_DAT5 | AD6 | mmc3_dat5 | spi4_d1 | uart10_txd | | vin2b_d0 | | | | | vin5a_d0 | ehrpwm3B | pr2_mii1_rxd2 | pr2_pru0_gpi9 | pr2_pru0_gpo9 | gpio1_23 | Driver off |
| 0x179C | CTRL_CORE_PAD_MMC3_DAT6 | AB8 | mmc3_dat6 | spi4_d0 | uart10_ctsn | | vin2b_de1 | | | | | vin5a_hsync0 | ehrpwm3_tripzone_input | pr2_mii1_rxd1 | pr2_pru0_gpi10 | pr2_pru0_gpo10 | gpio1_24 | Driver off |
| 0x17A0 | CTRL_CORE_PAD_MMC3_DAT7 | AB5 | mmc3_dat7 | spi4_cs0 | uart10_rtsn | | vin2b_clk1 | | | | | vin5a_vsync0 | eCAP3_in_PWM3_out | pr2_mii1_rxd0 | pr2_pru0_gpi11 | pr2_pru0_gpo11 | gpio1_25 | Driver off |
| 0x17A4 | CTRL_CORE_PAD_SPI1_SCLK | A25 | spi1_sclk | | | | | | | | | | | | | | gpio7_7 | Driver off |
| 0x17A8 | CTRL_CORE_PAD_SPI1_D1 | F16 | spi1_d1 | | | | | | | | | | | | | | gpio7_8 | Driver off |
| 0x17AC | CTRL_CORE_PAD_SPI1_D0 | B25 | spi1_d0 | | | | | | | | | | | | | | gpio7_9 | Driver off |
| 0x17B0 | CTRL_CORE_PAD_SPI1_CS0 | A24 | spi1_cs0 | | | | | | | | | | | | | | gpio7_10 | Driver off |
| 0x17B4 | CTRL_CORE_PAD_SPI1_CS1 | A22 | spi1_cs1 | | sata1_led | spi2_cs1 | | | | | | | | | | | gpio7_11 | Driver off |
| 0x17B8 | CTRL_CORE_PAD_SPI1_CS2 | B21 | spi1_cs2 | uart4_rxd | mmc3_sdcd | spi2_cs2 | dcan2_tx | mdio_mclk | hdmi1_hpd | | | | | | | | gpio7_12 | Driver off |
| 0x17BC | CTRL_CORE_PAD_SPI1_CS3 | B20 | spi1_cs3 | uart4_txd | mmc3_sdwp | spi2_cs3 | dcan2_rx | mdio_d | hdmi1_cec | | | | | | | | gpio7_13 | Driver off |
| 0x17C0 | CTRL_CORE_PAD_SPI2_SCLK | A26 | spi2_sclk | uart3_rxd | | | | | | | | | | | | | gpio7_14 | Driver off |
| 0x17C4 | CTRL_CORE_PAD_SPI2_D1 | B22 | spi2_d1 | uart3_txd | | | | | | | | | | | | | gpio7_15 | Driver off |
| 0x17C8 | CTRL_CORE_PAD_SPI2_D0 | G17 | spi2_d0 | uart3_ctsn | uart5_rxd | | | | | | | | | | | | gpio7_16 | Driver off |
| 0x17CC | CTRL_CORE_PAD_SPI2_CS0 | B24 | spi2_cs0 | uart3_rtsn | uart5_txd | | | | | | | | | | | | gpio7_17 | Driver off |
| 0x17D0 | CTRL_CORE_PAD_DCAN1_TX | G20 | dcan1_tx | | uart8_rxd | mmc2_sdcd | | | hdmi1_hpd | | | | | | | | gpio1_14 | Driver off |
| 0x17D4 | CTRL_CORE_PAD_DCAN1_RX | G19 | dcan1_rx | | uart8_txd | mmc2_sdwp | sata1_led | | hdmi1_cec | | | | | | | | gpio1_15 | Driver off |
| 0x17E0 | CTRL_CORE_PAD_UART1_RXD | B27 | uart1_rxd | | | mmc4_sdcd | | | | | | | | | | | gpio7_22 | Driver off |
| 0x17E4 | CTRL_CORE_PAD_UART1_TXD | C26 | uart1_txd | | | mmc4_sdwp | | | | | | | | | | | gpio7_23 | Driver off |
| 0x17E8 | CTRL_CORE_PAD_UART1_CTSN | E25 | uart1_ctsn | | uart9_rxd | mmc4_clk | | | | | | | | | | | gpio7_24 | Driver off |
| 0x17EC | CTRL_CORE_PAD_UART1_RTSN | C27 | uart1_rtsn | | uart9_txd | mmc4_cmd | | | | | | | | | | | gpio7_25 | Driver off |


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## Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0x17F0 | CTRL_CORE_PAD_UART2_RXD | D28 | | uart3_ctsn | uart3_rctx | mmc4_dat0 | uart2_rxd | uart1_dcdn | | | | | | | | | gpio7_26 | Driver off |
| 0x17F4 | CTRL_CORE_PAD_UART2_TXD | D26 | uart2_txd | uart3_rtsn | uart3_sd | mmc4_dat1 | uart2_txd | uart1_dsrn | | | | | | | | | gpio7_27 | Driver off |
| 0x17F8 | CTRL_CORE_PAD_UART2_CTSN | D27 | uart2_ctsn | | uart3_rxd | mmc4_dat2 | uart10_rxd | uart1_dtrn | | | | | | | | | gpio1_16 | Driver off |
| 0x17FC | CTRL_CORE_PAD_UART2_RTSN | C28 | uart2_rtsn | uart3_txd | uart3_irtx | mmc4_dat3 | uart10_txd | uart1_rin | | | | | | | | | gpio1_17 | Driver off |
| 0x1800 | CTRL_CORE_PAD_I2C1_SDA | C21 | i2c1_sda | | | | | | | | | | | | | | | |
| 0x1804 | CTRL_CORE_PAD_I2C1_SCL | C20 | i2c1_scl | | | | | | | | | | | | | | | |
| 0x1808 | CTRL_CORE_PAD_I2C2_SDA | C25 | i2c2_sda | hdmi1_ddc_scl | | | | | | | | | | | | | | Driver off |
| 0x180C | CTRL_CORE_PAD_I2C2_SCL | F17 | i2c2_scl | hdmi1_ddc_sda | | | | | | | | | | | | | | Driver off |
| 0x1818 | CTRL_CORE_PAD_WAKEUP0 | AD17 | Wakeup0 | dcan1_rx | | | | | | | | | | | | | gpio1_0 | Driver off |
| 0x181C | CTRL_CORE_PAD_WAKEUP1 | AC17 | Wakeup1 | dcan2_rx | | | | | | | | | | | | | gpio1_1 | Driver off |
| 0x1820 | CTRL_CORE_PAD_WAKEUP2 | AB16 | Wakeup2 | sys_nirq2 | | | | | | | | | | | | | gpio1_2 | Driver off |
| 0x1824 | CTRL_CORE_PAD_WAKEUP3 | AC16 | Wakeup3 | sys_nirq1 | | | | | | | | | | | | | gpio1_3 | Driver off |
| 0x1828 | CTRL_CORE_PAD_ON_OFF | Y11 | on_off | | | | | | | | | | | | | | | |
| 0x182C | CTRL_CORE_PAD_RTC_PORZ | AB17 | rtc_porz | | | | | | | | | | | | | | | |
| 0x1830 | CTRL_CORE_PAD_TMS | F18 | tms | | | | | | | | | | | | | | | |
| 0x1834 | CTRL_CORE_PAD_TDI | D23 | tdi | | | | | | | | | | | | | | gpio8_27 | |
| 0x1838 | CTRL_CORE_PAD_TDO | F19 | tdo | | | | | | | | | | | | | | gpio8_28 | |
| 0x183C | CTRL_CORE_PAD_TCLK | E20 | tclk | | | | | | | | | | | | | | | |
| 0x1840 | CTRL_CORE_PAD_TRSTN | D20 | trstn | | | | | | | | | | | | | | | |
| 0x1844 | CTRL_CORE_PAD_RTCK | E18 | rtck | | | | | | | | | | | | | | gpio8_29 | |
| 0x1848 | CTRL_CORE_PAD_EMU0 | G21 | emu0 | | | | | | | | | | | | | | gpio8_30 | |
| 0x184C | CTRL_CORE_PAD_EMU1 | D24 | emu1 | | | | | | | | | | | | | | gpio8_31 | |
| 0x185C | CTRL_CORE_PAD_RESETN | E23 | resetn | | | | | | | | | | | | | | | |
| 0x1860 | CTRL_CORE_PAD_NMIN_DSP | D21 | nmin_dsp | | | | | | | | | | | | | | | |

### Table 4-3. Multiplexing Characteristics (continued)

| ADDRESS | REGISTER NAME | BALL NUMBER | MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0]) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0x1864 | CTRL_CORE_PAD_RSTOUTN | F23 | rstoutn | | | | | | | | | | | | | | | |

1. NA in table stands for Not Applicable.


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## 4.4 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

Texas Instruments has developed an application called Pin Mux Utility that helps a system designer select the appropriate pin-multiplexing configuration for their device-based product design. The Pin Mux Utility provides a way to select valid IO Sets of specific peripheral interfaces to ensure the pinmultiplexing configuration selected for a design only uses valid IO Sets supported by the device.

1. **SIGNAL NAME:** The name of the signal passing through the pin.

**NOTE**

The subsystem multiplexing signals are not described in Table 4-2 and Table 4-3.

2. **DESCRIPTION:** Description of the signal
3. **TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - IO = Input or output
   - D = Open Drain
   - DS = Differential
   - A = Analog
   - PWR = Power
   - GND = Ground
4. **BALL:** Associated ball(s) bottom

**NOTE**

For more information, see the Control Module / Control Module Register Manual section of the device TRM.

### *4.4.1 Video Input Port (VIP)*

**CAUTION**

The I/O timings provided in Section 7, *Timing Requirements and Switching Characteristics* are applicable for all combinations of signals for vin1, vin5 and vin6. However, the timings are valid only for vin2, vin3, and vin4 if signals within a single IOSET are used. The IOSETs are defined in the Table 7-4.

**NOTE**

For more information, see the Video Input Port (VIP) section of the device TRM.

**Table 4-4. VIP Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **Video Input 1** | | | |
| vin1a_clk0 | Video Input 1 Port A Clock input. Input clock for 8-bit 16-bit or 24-bit Port A video capture. Input data is sampled on the CLK0 edge. | I | AG8 |
| vin1a_de0 | Video Input 1 Data Enable input | I | AD9 |
| vin1a_fld0 | Video Input 1 Port A Field ID input | I | AF9 |

**Table 4-4. VIP Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| vin1a_hsync0 | Video Input 1 Port A Horizontal Sync input | I | AE9 |
| vin1a_vsync0 | Video Input 1 Port A Vertical Sync input | I | AF8 |
| vin1a_d0 | Video Input 1 Port A Data input | I | AE8 |
| vin1a_d1 | Video Input 1 Port A Data input | I | AD8 |
| vin1a_d2 | Video Input 1 Port A Data input | I | AG7 |
| vin1a_d3 | Video Input 1 Port A Data input | I | AH6 |
| vin1a_d4 | Video Input 1 Port A Data input | I | AH3 |
| vin1a_d5 | Video Input 1 Port A Data input | I | AH5 |
| vin1a_d6 | Video Input 1 Port A Data input | I | AG6 |
| vin1a_d7 | Video Input 1 Port A Data input | I | AH4 |
| vin1a_d8 | Video Input 1 Port A Data input | I | AG4 |
| vin1a_d9 | Video Input 1 Port A Data input | I | AG2 |
| vin1a_d10 | Video Input 1 Port A Data input | I | AG3 |
| vin1a_d11 | Video Input 1 Port A Data input | I | AG5 |
| vin1a_d12 | Video Input 1 Port A Data input | I | AF2 |
| vin1a_d13 | Video Input 1 Port A Data input | I | AF6 |
| vin1a_d14 | Video Input 1 Port A Data input | I | AF3 |
| vin1a_d15 | Video Input 1 Port A Data input | I | AF4 |
| vin1a_d16 | Video Input 1 Port A Data input | I | AF1 |
| vin1a_d17 | Video Input 1 Port A Data input | I | AE3 |
| vin1a_d18 | Video Input 1 Port A Data input | I | AE5 |
| vin1a_d19 | Video Input 1 Port A Data input | I | AE1 |
| vin1a_d20 | Video Input 1 Port A Data input | I | AE2 |
| vin1a_d21 | Video Input 1 Port A Data input | I | AE6 |
| vin1a_d22 | Video Input 1 Port A Data input | I | AD2 |
| vin1a_d23 | Video Input 1 Port A Data input | I | AD3 |
| vin1b_hsync1 | Video Input 1 Port B Horizontal Sync input | I | N6 / AD9 |
| vin1b_vsync1 | Video Input 1 Port B Vertical Sync input | I | AF9 |
| vin1b_fld1 | Video Input 1 Port B Field ID input | I | AE9 |
| vin1b_de1 | Video Input 1 Port B Data Enable input | I | AF8 / M4 |
| vin1b_clk1 | Video Input 1 Port B Clock input | I | AH7 |
| vin1b_d0 | Video Input 1 Port B Data input | I | AF4 / AD3 |
| vin1b_d1 | Video Input 1 Port B Data input | I | AF3 / AD2 |
| vin1b_d2 | Video Input 1 Port B Data input | I | AF6 / AE6 |
| vin1b_d3 | Video Input 1 Port B Data input | I | AF2 / AE2 |
| vin1b_d4 | Video Input 1 Port B Data input | I | AG5 / AE1 |
| vin1b_d5 | Video Input 1 Port B Data input | I | AG3 / AE5 |
| vin1b_d6 | Video Input 1 Port B Data input | I | AG2 / AE3 |
| vin1b_d7 | Video Input 1 Port B Data input | I | AG4 / AF1 |
| **Video Input 2** | | | |
| vin2a_clk0 | Video Input 2 Port A Clock input. | I | E1 / V1 |
| vin2a_de0 | Video Input 2 Port A Data Enable input | I | G2 / V7 |
| vin2a_fld0 | Video Input 2 Port A Field ID input | I | H7 / G2 / W2 |
| vin2a_hsync0 | Video Input 2 Port A Horizontal Sync input | I | G1 / U7 |
| vin2a_vsync0 | Video Input 2 Port A Vertical Sync input | I | G6 / V6 |
| vin2a_d0 | Video Input 2 Port A Data input | I | F2 / U4 |
| vin2a_d1 | Video Input 2 Port A Data input | I | F3 / V2 |


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**Table 4-4. VIP Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| vin2a_d2 | Video Input 2 Port A Data input | I | D1 / Y1 |
| vin2a_d3 | Video Input 2 Port A Data input | I | E2 / W9 |
| vin2a_d4 | Video Input 2 Port A Data input | I | D2 / V9 |
| vin2a_d5 | Video Input 2 Port A Data input | I | F4 / U5 |
| vin2a_d6 | Video Input 2 Port A Data input | I | C1 / V5 |
| vin2a_d7 | Video Input 2 Port A Data input | I | E4 / V4 |
| vin2a_d8 | Video Input 2 Port A Data input | I | F5 / V3 |
| vin2a_d9 | Video Input 2 Port A Data input | I | E6 / Y2 |
| vin2a_d10 | Video Input 2 Port A Data input | I | D3 / U6 |
| vin2a_d11 | Video Input 2 Port A Data input | I | F6 / U3 |
| vin2a_d12 | Video Input 2 Port A Data input | I | D5 |
| vin2a_d13 | Video Input 2 Port A Data input | I | C2 |
| vin2a_d14 | Video Input 2 Port A Data input | I | C3 |
| vin2a_d15 | Video Input 2 Port A Data input | I | C4 |
| vin2a_d16 | Video Input 2 Port A Data input | I | B2 |
| vin2a_d17 | Video Input 2 Port A Data input | I | D6 |
| vin2a_d18 | Video Input 2 Port A Data input | I | C5 |
| vin2a_d19 | Video Input 2 Port A Data input | I | A3 |
| vin2a_d20 | Video Input 2 Port A Data input | I | B3 |
| vin2a_d21 | Video Input 2 Port A Data input | I | B4 |
| vin2a_d22 | Video Input 2 Port A Data input | I | B5 |
| vin2a_d23 | Video Input 2 Port A Data input | I | A4 |
| vin2b_clk1 | Video Input 2 Port B Clock input | I | AB5 / H7 |
| vin2b_de1 | Video Input 2 Port B Data Enable input | I | AB8 / G2 |
| vin2b_fld1 | Video Input 2 Port B Field ID input | I | G2 |
| vin2b_hsync1 | Video Input 2 Port B Horizontal Sync input | I | AC5 / G1 |
| vin2b_vsync1 | Video Input 2 Port B Vertical Sync input | I | AB4 / G6 |
| vin2b_d0 | Video Input 2 Port B Data input | I | AD6 / A4 |
| vin2b_d1 | Video Input 2 Port B Data input | I | AC8 / B5 |
| vin2b_d2 | Video Input 2 Port B Data input | I | AC3 / B4 |
| vin2b_d3 | Video Input 2 Port B Data input | I | AC9 / B3 |
| vin2b_d4 | Video Input 2 Port B Data input | I | AC6 / A3 |
| vin2b_d5 | Video Input 2 Port B Data input | I | AC7 / C5 |
| vin2b_d6 | Video Input 2 Port B Data input | I | AC4 / D6 |
| vin2b_d7 | Video Input 2 Port B Data input | I | AD4 / B2 |
| **Video Input 3** | | | |
| vin3a_clk0 | Video Input 3 Port A Clock input | I | B11 / AH7 / P1 |
| vin3a_de0 | Video Input 3 Port A Data Enable input | I | N9 / B3 / B10 |
| vin3a_fld0 | Video Input 3 Port A Field ID input | I | P9 / B4 / D11 |
| vin3a_hsync0 | Video Input 3 Port A Horizontal Sync input | I | N7 / B5 / C11 |
| vin3a_vsync0 | Video Input 3 Port A Vertical Sync input | I | R4 / A4 / E11 |
| vin3a_d0 | Video Input 3 Port A Data input | I | M6 / AF1 / B7 |
| vin3a_d1 | Video Input 3 Port A Data input | I | M2 / AE3 / B8 |
| vin3a_d2 | Video Input 3 Port A Data input | I | L5 / AE5 / A7 |
| vin3a_d3 | Video Input 3 Port A Data input | I | M1 / AE1 / A8 |
| vin3a_d4 | Video Input 3 Port A Data input | I | L6 / AE2 / C9 |
| vin3a_d5 | Video Input 3 Port A Data input | I | L4 / AE6 / A9 |

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**Table 4-4. VIP Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| vin3a_d6 | Video Input 3 Port A Data input | I | L3 / AD2 / B9 |
| vin3a_d7 | Video Input 3 Port A Data input | I | L2 / AD3 / A10 |
| vin3a_d8 | Video Input 3 Port A Data input | I | L1 / B2 / E8 |
| vin3a_d9 | Video Input 3 Port A Data input | I | K2 / D6 / D9 |
| vin3a_d10 | Video Input 3 Port A Data input | I | J1 / C5 / D7 |
| vin3a_d11 | Video Input 3 Port A Data input | I | J2 / A3 / D8 |
| vin3a_d12 | Video Input 3 Port A Data input | I | H1 / B3 / A5 |
| vin3a_d13 | Video Input 3 Port A Data input | I | J3 / B4 / C6 |
| vin3a_d14 | Video Input 3 Port A Data input | I | H2 / B5 / C8 |
| vin3a_d15 | Video Input 3 Port A Data input | I | H3 / A4 / C7 |
| vin3a_d16 | Video Input 3 Port A Data input | I | R6 / F11 |
| vin3a_d17 | Video Input 3 Port A Data input | I | T9 / G10 |
| vin3a_d18 | Video Input 3 Port A Data input | I | T6 / F10 |
| vin3a_d19 | Video Input 3 Port A Data input | I | T7 / G11 |
| vin3a_d20 | Video Input 3 Port A Data input | I | P6 / E9 |
| vin3a_d21 | Video Input 3 Port A Data input | I | R9 / F9 |
| vin3a_d22 | Video Input 3 Port A Data input | I | R5 / F8 |
| vin3a_d23 | Video Input 3 Port A Data input | I | P5 / E7 |
| vin3b_clk1 | Video Input 3 Port B Clock input | I | P7 / M4 |
| vin3b_de1 | Video Input 3 Port B Data Enable input | I | N6 |
| vin3b_fld1 | Video Input 3 Port A Field ID input | I | M4 |
| vin3b_hsync1 | Video Input 3 Port A Horizontal Sync input | I | H5 |
| vin3b_vsync1 | Video Input 3 Port A Vertical Sync input | I | H6 |
| vin3b_d0 | Video Input 3 Port B Data input | I | K7 |
| vin3b_d1 | Video Input 3 Port B Data input | I | M7 |
| vin3b_d2 | Video Input 3 Port B Data input | I | J5 |
| vin3b_d3 | Video Input 3 Port B Data input | I | K6 |
| vin3b_d4 | Video Input 3 Port B Data input | I | J7 |
| vin3b_d5 | Video Input 3 Port B Data input | I | J4 |
| vin3b_d6 | Video Input 3 Port B Data input | I | J6 |
| vin3b_d7 | Video Input 3 Port B Data input | I | H4 |
| **Video Input 4** | | | |
| vin4a_clk0 | Video Input 4 Port A Clock input | I | P4 / B26 / B11 |
| vin4a_de0 | Video Input 4 Port A Data Enable input | I | H6 / C23 / B10 / P7 |
| vin4a_fld0 | Video Input 4 Port A Field ID input | I | J7 / F21 / P9 / D11 |
| vin4a_hsync0 | Video Input 4 Port A Horizontal Sync input | I | R3 / E21 / C11 / P7 |
| vin4a_vsync0 | Video Input 4 Port A Vertical Sync input | I | T2 / F20 / E11 / N1 |
| vin4a_d0 | Video Input 4 Port A Data input | I | R6 / B7 / B14 |
| vin4a_d1 | Video Input 4 Port A Data input | I | T9 / B8 / J14 |
| vin4a_d2 | Video Input 4 Port A Data input | I | T6 / A7 / G13 |
| vin4a_d3 | Video Input 4 Port A Data input | I | T7 / A8 / J11 |
| vin4a_d4 | Video Input 4 Port A Data input | I | P6 / C9 / E12 |
| vin4a_d5 | Video Input 4 Port A Data input | I | R9 / A9 / F13 |
| vin4a_d6 | Video Input 4 Port A Data input | I | R5 / B9 / C12 |
| vin4a_d7 | Video Input 4 Port A Data input | I | P5 / A10 / D12 |
| vin4a_d8 | Video Input 4 Port A Data input | I | E8 / U2 / E15 |
| vin4a_d9 | Video Input 4 Port A Data input | I | D9 / U1 / A20 |


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**Table 4-4. VIP Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| vin4a_d10 | Video Input 4 Port A Data input | I | D7 / P3 / B15 |
| vin4a_d11 | Video Input 4 Port A Data input | I | D8 / R2 / A15 |
| vin4a_d12 | Video Input 4 Port A Data input | I | A5 / K7 / D15 |
| vin4a_d13 | Video Input 4 Port A Data input | I | C6 / M7 / B16 |
| vin4a_d14 | Video Input 4 Port A Data input | I | C8 / J5 / B17 |
| vin4a_d15 | Video Input 4 Port A Data input | I | C7 / K6 / A17 |
| vin4a_d16 | Video Input 4 Port A Data input | I | C18 / F11 |
| vin4a_d17 | Video Input 4 Port A Data input | I | A21 / G10 |
| vin4a_d18 | Video Input 4 Port A Data input | I | G16 / F10 |
| vin4a_d19 | Video Input 4 Port A Data input | I | D17 / G11 |
| vin4a_d20 | Video Input 4 Port A Data input | I | AA3 / E9 |
| vin4a_d21 | Video Input 4 Port A Data input | I | AB9 / F9 |
| vin4a_d22 | Video Input 4 Port A Data input | I | AB3 / F8 |
| vin4a_d23 | Video Input 4 Port A Data input | I | AA4 / E7 |
| vin4b_clk1 | Video Input 4 Port B Clock input | I | N9 / V1 |
| vin4b_de1 | Video Input 4 Port B Data Enable input | I | P9 / V7 |
| vin4b_fld1 | Video Input 4 Port B Field ID input | I | P4 / W2 |
| vin4b_hsync1 | Video Input 4 Port B Horizontal Sync input | I | N7 / U7 |
| vin4b_vsync1 | Video Input 4 Port B Vertical Sync input | I | R4 / V6 |
| vin4b_d0 | Video Input 4 Port B Data input | I | R6 / U4 |
| vin4b_d1 | Video Input 4 Port B Data input | I | T9 / V2 |
| vin4b_d2 | Video Input 4 Port B Data input | I | T6 / Y1 |
| vin4b_d3 | Video Input 4 Port B Data input | I | T7 / W9 |
| vin4b_d4 | Video Input 4 Port B Data input | I | P6 / V9 |
| vin4b_d5 | Video Input 4 Port B Data input | I | R9 / U5 |
| vin4b_d6 | Video Input 4 Port B Data input | I | R5 / V5 |
| vin4b_d7 | Video Input 4 Port B Data input | I | P5 / V4 |
| **Video Input 5** | | | |
| vin5a_clk0 | Video Input 5 Port A Clock input | I | AC5 |
| vin5a_de0 | Video Input 5 Port A Data Enable input | I | AB4 |
| vin5a_fld0 | Video Input 5 Port A Field ID input | I | C17 |
| vin5a_hsync0 | Video Input 5 Port A Horizontal Sync input | I | AB8 |
| vin5a_vsync0 | Video Input 5 Port A Vertical Sync input | I | AB5 |
| vin5a_d0 | Video Input 5 Port A Data input | I | AD6 |
| vin5a_d1 | Video Input 5 Port A Data input | I | AC8 |
| vin5a_d2 | Video Input 5 Port A Data input | I | AC3 |
| vin5a_d3 | Video Input 5 Port A Data input | I | AC9 |
| vin5a_d4 | Video Input 5 Port A Data input | I | AC6 |
| vin5a_d5 | Video Input 5 Port A Data input | I | AC7 |
| vin5a_d6 | Video Input 5 Port A Data input | I | AC4 |
| vin5a_d7 | Video Input 5 Port A Data input | I | AD4 |
| vin5a_d8 | Video Input 5 Port A Data input | I | AA4 |
| vin5a_d9 | Video Input 5 Port A Data input | I | AB3 |
| vin5a_d10 | Video Input 5 Port A Data input | I | AB9 |
| vin5a_d11 | Video Input 5 Port A Data input | I | AA3 |
| vin5a_d12 | Video Input 5 Port A Data input | I | D17 |
| vin5a_d13 | Video Input 5 Port A Data input | I | G16 |

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**Table 4-4. VIP Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| vin5a_d14 | Video Input 5 Port A Data input | I | A21 |
| vin5a_d15 | Video Input 5 Port A Data input | I | C18 |
| **Video Input 6** | | | |
| vin6a_clk0 | Video Input 6 Port A Clock input | I | E17 |
| vin6a_de0 | Video Input 6 Port B Data Enable input | I | D14 |
| vin6a_fld0 | Video Input 6 Port A Field ID input | I | C14 |
| vin6a_hsync0 | Video Input 6 Port A Horizontal Sync input | I | F12 |
| vin6a_vsync0 | Video Input 6 Port A Vertical Sync input | I | G12 |
| vin6a_d0 | Video Input 6 Port A Data input | I | C17 / D18 |
| vin6a_d1 | Video Input 6 Port A Data input | I | B19 |
| vin6a_d2 | Video Input 6 Port A Data input | I | F15 |
| vin6a_d3 | Video Input 6 Port A Data input | I | B18 |
| vin6a_d4 | Video Input 6 Port A Data input | I | A16 |
| vin6a_d5 | Video Input 6 Port A Data input | I | C15 |
| vin6a_d6 | Video Input 6 Port A Data input | I | A18 |
| vin6a_d7 | Video Input 6 Port A Data input | I | A19 |
| vin6a_d8 | Video Input 6 Port A Data input | I | F14 |
| vin6a_d9 | Video Input 6 Port A Data input | I | G14 |
| vin6a_d10 | Video Input 6 Port A Data input | I | A13 |
| vin6a_d11 | Video Input 6 Port A Data input | I | E14 |
| vin6a_d12 | Video Input 6 Port A Data input | I | A12 |
| vin6a_d13 | Video Input 6 Port A Data input | I | B13 |
| vin6a_d14 | Video Input 6 Port A Data input | I | A11 |
| vin6a_d15 | Video Input 6 Port A Data input | I | B12 |

### *4.4.2 Display Subsystem – Video Output Ports*

**CAUTION**

The I/O timings provided in Section 7, *Timing Requirements and Switching Characteristics* are valid only if signals within a single IOSET are used. The IOSETs are defined in the Table 7-19 and Table 7-20.

**Table 4-5. DSS Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **DPI Video Output 1** | | | |
| vout1_clk | Video Output 1 Clock output | O | D11 |
| vout1_de | Video Output 1 Data Enable output | O | B10 |
| vout1_fld | Video Output 1 Field ID output.This signal is not used for embedded sync modes. | O | B11 |
| vout1_hsync | Video Output 1 Horizontal Sync output.This signal is not used for embedded sync modes. | O | C11 |
| vout1_vsync | Video Output 1 Vertical Sync output.This signal is not used for embedded sync modes. | O | E11 |
| vout1_d0 | Video Output 1 Data output | O | F11 |
| vout1_d1 | Video Output 1 Data output | O | G10 |
| vout1_d2 | Video Output 1 Data output | O | F10 |
| vout1_d3 | Video Output 1 Data output | O | G11 |
| vout1_d4 | Video Output 1 Data output | O | E9 |


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**Table 4-5. DSS Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| vout1_d5 | Video Output 1 Data output | O | F9 |
| vout1_d6 | Video Output 1 Data output | O | F8 |
| vout1_d7 | Video Output 1 Data output | O | E7 |
| vout1_d8 | Video Output 1 Data output | O | E8 |
| vout1_d9 | Video Output 1 Data output | O | D9 |
| vout1_d10 | Video Output 1 Data output | O | D7 |
| vout1_d11 | Video Output 1 Data output | O | D8 |
| vout1_d12 | Video Output 1 Data output | O | A5 |
| vout1_d13 | Video Output 1 Data output | O | C6 |
| vout1_d14 | Video Output 1 Data output | O | C8 |
| vout1_d15 | Video Output 1 Data output | O | C7 |
| vout1_d16 | Video Output 1 Data output | O | B7 |
| vout1_d17 | Video Output 1 Data output | O | B8 |
| vout1_d18 | Video Output 1 Data output | O | A7 |
| vout1_d19 | Video Output 1 Data output | O | A8 |
| vout1_d20 | Video Output 1 Data output | O | C9 |
| vout1_d21 | Video Output 1 Data output | O | A9 |
| vout1_d22 | Video Output 1 Data output | O | B9 |
| vout1_d23 | Video Output 1 Data output | O | A10 |
| **DPI Video Output 2** | | | |
| vout2_clk | Video Output 2 Clock output | O | H7/ B26 |
| vout2_de | Video Output 2 Data Enable output | O | G2/ C23 |
| vout2_fld | Video Output 2 Field ID output.This signal is not used for embedded sync modes. | O | E1/ F21 |
| vout2_hsync | Video Output 2 Horizontal Sync output.This signal is not used for embedded sync modes. | O | G1/ E21 |
| vout2_vsync | Video Output 2 Vertical Sync output.This signal is not used for embedded sync modes. | O | G6/ F20 |
| vout2_d0 | Video Output 2 Data output | O | A4/ B14 |
| vout2_d1 | Video Output 2 Data output | O | B5/ J14 |
| vout2_d2 | Video Output 2 Data output | O | B4/ G13 |
| vout2_d3 | Video Output 2 Data output | O | B3/ J11 |
| vout2_d4 | Video Output 2 Data output | O | A3/ E12 |
| vout2_d5 | Video Output 2 Data output | O | C5/ F13 |
| vout2_d6 | Video Output 2 Data output | O | D6/ C12 |
| vout2_d7 | Video Output 2 Data output | O | B2/ D12 |
| vout2_d8 | Video Output 2 Data output | O | C4/ E15 |
| vout2_d9 | Video Output 2 Data output | O | C3/ A20 |
| vout2_d10 | Video Output 2 Data output | O | C2/ B15 |
| vout2_d11 | Video Output 2 Data output | O | D5/ A15 |
| vout2_d12 | Video Output 2 Data output | O | F6/ D15 |
| vout2_d13 | Video Output 2 Data output | O | D3/ B16 |
| vout2_d14 | Video Output 2 Data output | O | E6/ B17 |
| vout2_d15 | Video Output 2 Data output | O | F5/ A17 |
| vout2_d16 | Video Output 2 Data output | O | E4/ C18 |
| vout2_d17 | Video Output 2 Data output | O | C1/ A21 |
| vout2_d18 | Video Output 2 Data output | O | F4/ G16 |
| vout2_d19 | Video Output 2 Data output | O | D2/ D17 |
| vout2_d20 | Video Output 2 Data output | O | E2/ AA3 |
| vout2_d21 | Video Output 2 Data output | O | D1/ AB9 |

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**Table 4-5. DSS Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| vout2_d22 | Video Output 2 Data output | O | F3/ AB3 |
| vout2_d23 | Video Output 2 Data output | O | F2/ AA4 |
| **DPI Video Output 3** | | | |
| vout3_clk | Video Output 3 Clock output | O | P1/ AF9 (1) |
| vout3_de | Video Output 3 Data Enable output | O | N9/ AD9 (1) |
| vout3_fld | Video Output 3 Field ID output.This signal is not used for embedded sync modes. | O | P9/ AG8 (1) |
| vout3_hsync | Video Output 3 Horizontal Sync output.This signal is not used for embedded sync modes. | O | N7/ AE9 (1) |
| vout3_vsync | Video Output 3 Vertical Sync output.This signal is not used for embedded sync modes. | O | R4/ AF8 (1) |
| vout3_d0 | Video Output 3 Data output | O | M6/ AH4 (1)/ AD3 (1) |
| vout3_d1 | Video Output 3 Data output | O | M2/ AG6 (1)/ AD2 (1) |
| vout3_d2 | Video Output 3 Data output | O | L5/ AH5 (1)/ AE6 (1) |
| vout3_d3 | Video Output 3 Data output | O | M1/ AH3 (1)/ AE2 (1) |
| vout3_d4 | Video Output 3 Data output | O | L6/ AH6 (1)/ AE1 (1) |
| vout3_d5 | Video Output 3 Data output | O | L4/ AG7 (1)/ AE5 (1) |
| vout3_d6 | Video Output 3 Data output | O | L3/ AD8 (1)/ AE3 (1) |
| vout3_d7 | Video Output 3 Data output | O | L2/ AE8 (1)/ AF1 (1) |
| vout3_d8 | Video Output 3 Data output | O | L1/ AF4 (1) |
| vout3_d9 | Video Output 3 Data output | O | K2/ AF3 (1) |
| vout3_d10 | Video Output 3 Data output | O | J1/ AF6 (1) |
| vout3_d11 | Video Output 3 Data output | O | J2/ AF2 (1) |
| vout3_d12 | Video Output 3 Data output | O | H1/ AG5 (1) |
| vout3_d13 | Video Output 3 Data output | O | J3/ AG3 (1) |
| vout3_d14 | Video Output 3 Data output | O | H2/ AG2 (1) |
| vout3_d15 | Video Output 3 Data output | O | H3/ AG4 (1) |
| vout3_d16 | Video Output 3 Data output | O | R6/ AG8 (1)/ AH4 (1) |
| vout3_d17 | Video Output 3 Data output | O | T9/ AD9 (1)/ AG6 (1) |
| vout3_d18 | Video Output 3 Data output | O | T6/ AH5 (1) |
| vout3_d19 | Video Output 3 Data output | O | T7/ AH3 (1) |
| vout3_d20 | Video Output 3 Data output | O | P6/ AH6 (1) |
| vout3_d21 | Video Output 3 Data output | O | R9/ AG7 (1) |
| vout3_d22 | Video Output 3 Data output | O | R5/ AD8 (1) |
| vout3_d23 | Video Output 3 Data output | O | P5/ AE8 (1) |

(1) The VOUT3 interface when multiplexed onto balls mapped to the VDDSHV6 supply rail is restricted to operating in 1.8V mode only (VDDSHV6 must be supplied with 1.8V). 3.3V mode is not supported. This must be considered in the pin mux programming and VDDSHVx supply connections.

### *4.4.3 Display Subsystem – High-Definition Multimedia Interface (HDMI)*

**NOTE**

For more information, see the Display Subsystem / Display Subsystem Overview of the device TRM.


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**Table 4-6. HDMI Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| hdmi1_cec | HDMI consumer electronic control | IOD | B20/ G19 |
| hdmi1_hpd | HDMI display hot plug detect | I | B21/ G20 |
| hdmi1_ddc_scl | HDMI display data channel clock | IOD | C25 |
| hdmi1_ddc_sda | HDMI display data channel data | IOD | F17 |
| hdmi1_clockx | HDMI clock differential positive or negative | ODS | AG16 |
| hdmi1_clocky | HDMI clock differential positive or negative | ODS | AH16 |
| hdmi1_data2x | HDMI data 2 differential positive or negative | ODS | AG19 |
| hdmi1_data2y | HDMI data 2 differential positive or negative | ODS | AH19 |
| hdmi1_data1x | HDMI data 1 differential positive or negative | ODS | AG18 |
| hdmi1_data1y | HDMI data 1 differential positive or negative | ODS | AH18 |
| hdmi1_data0x | HDMI data 0 differential positive or negative | ODS | AG17 |
| hdmi1_data0y | HDMI data 0 differential positive or negative | ODS | AH17 |

### *4.4.4 External Memory Interface - (EMIF)*

**NOTE**

For more information, see the Memory Subsystem / EMIF Controller section of the device TRM.

**Table 4-7. EMIF Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **EMIF Channel 1** | | | |
| ddr1_csn0 | EMIF1 Chip Select 0 | O | AH23 |
| ddr1_cke | EMIF1 Clock Enable | O | AG22 |
| ddr1_ck | EMIF1 Clock | O | AG24 |
| ddr1_nck | EMIF1 Negative Clock | O | AH24 |
| ddr1_odt0 | EMIF1 On-Die Termination for Chip Select 0 | O | AE20 |
| ddr1_casn | EMIF1 Column Address Strobe | O | AC18 |
| ddr1_rasn | EMIF1 Row Address Strobe | O | AF20 |
| ddr1_wen | EMIF1 Write Enable | O | AH21 |
| ddr1_rst | EMIF1 Reset output (DDR3-SDRAM only) | O | AG21 |
| ddr1_ba0 | EMIF1 Bank Address | O | AF17 |
| ddr1_ba1 | EMIF1 Bank Address | O | AE18 |
| ddr1_ba2 | EMIF1 Bank Address | O | AB18 |
| ddr1_a0 | EMIF1 Address Bus | O | AD20 |
| ddr1_a1 | EMIF1 Address Bus | O | AC19 |
| ddr1_a2 | EMIF1 Address Bus | O | AC20 |
| ddr1_a3 | EMIF1 Address Bus | O | AB19 |
| ddr1_a4 | EMIF1 Address Bus | O | AF21 |
| ddr1_a5 | EMIF1 Address Bus | O | AH22 |
| ddr1_a6 | EMIF1 Address Bus | O | AG23 |
| ddr1_a7 | EMIF1 Address Bus | O | AE21 |
| ddr1_a8 | EMIF1 Address Bus | O | AF22 |
| ddr1_a9 | EMIF1 Address Bus | O | AE22 |
| ddr1_a10 | EMIF1 Address Bus | O | AD21 |
| ddr1_a11 | EMIF1 Address Bus | O | AD22 |
| ddr1_a12 | EMIF1 Address Bus | O | AC21 |

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**Table 4-7. EMIF Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| ddr1_a13 | EMIF1 Address Bus | O | AF18 |
| ddr1_a14 | EMIF1 Address Bus | O | AE17 |
| ddr1_a15 | EMIF1 Address Bus | O | AD18 |
| ddr1_d0 | EMIF1 Data Bus | IO | AF25 |
| ddr1_d1 | EMIF1 Data Bus | IO | AF26 |
| ddr1_d2 | EMIF1 Data Bus | IO | AG26 |
| ddr1_d3 | EMIF1 Data Bus | IO | AH26 |
| ddr1_d4 | EMIF1 Data Bus | IO | AF24 |
| ddr1_d5 | EMIF1 Data Bus | IO | AE24 |
| ddr1_d6 | EMIF1 Data Bus | IO | AF23 |
| ddr1_d7 | EMIF1 Data Bus | IO | AE23 |
| ddr1_d8 | EMIF1 Data Bus | IO | AC23 |
| ddr1_d9 | EMIF1 Data Bus | IO | AF27 |
| ddr1_d10 | EMIF1 Data Bus | IO | AG27 |
| ddr1_d11 | EMIF1 Data Bus | IO | AF28 |
| ddr1_d12 | EMIF1 Data Bus | IO | AE26 |
| ddr1_d13 | EMIF1 Data Bus | IO | AC25 |
| ddr1_d14 | EMIF1 Data Bus | IO | AC24 |
| ddr1_d15 | EMIF1 Data Bus | IO | AD25 |
| ddr1_d16 | EMIF1 Data Bus | IO | V20 |
| ddr1_d17 | EMIF1 Data Bus | IO | W20 |
| ddr1_d18 | EMIF1 Data Bus | IO | AB28 |
| ddr1_d19 | EMIF1 Data Bus | IO | AC28 |
| ddr1_d20 | EMIF1 Data Bus | IO | AC27 |
| ddr1_d21 | EMIF1 Data Bus | IO | Y19 |
| ddr1_d22 | EMIF1 Data Bus | IO | AB27 |
| ddr1_d23 | EMIF1 Data Bus | IO | Y20 |
| ddr1_d24 | EMIF1 Data Bus | IO | AA23 |
| ddr1_d25 | EMIF1 Data Bus | IO | Y22 |
| ddr1_d26 | EMIF1 Data Bus | IO | Y23 |
| ddr1_d27 | EMIF1 Data Bus | IO | AA24 |
| ddr1_d28 | EMIF1 Data Bus | IO | Y24 |
| ddr1_d29 | EMIF1 Data Bus | IO | AA26 |
| ddr1_d30 | EMIF1 Data Bus | IO | AA25 |
| ddr1_d31 | EMIF1 Data Bus | IO | AA28 |
| ddr1_ecc_d0 | EMIF1 ECC Data Bus | IO | W22 |
| ddr1_ecc_d1 | EMIF1 ECC Data Bus | IO | V23 |
| ddr1_ecc_d2 | EMIF1 ECC Data Bus | IO | W19 |
| ddr1_ecc_d3 | EMIF1 ECC Data Bus | IO | W23 |
| ddr1_ecc_d4 | EMIF1 ECC Data Bus | IO | Y25 |
| ddr1_ecc_d5 | EMIF1 ECC Data Bus | IO | V24 |
| ddr1_ecc_d6 | EMIF1 ECC Data Bus | IO | V25 |
| ddr1_ecc_d7 | EMIF1 ECC Data Bus | IO | Y26 |
| ddr1_dqm0 | EMIF1 Data Mask | O | AD23 |
| ddr1_dqm1 | EMIF1 Data Mask | O | AB23 |
| ddr1_dqm2 | EMIF1 Data Mask | O | AC26 |
| ddr1_dqm3 | EMIF1 Data Mask | O | AA27 |


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**Table 4-7. EMIF Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| ddr1_dqm_ecc | EMIF1 ECC Data Mask | O | V26 |
| ddr1_dqs0 | Data strobe 0 input/output for byte 0 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading. | IO | AH25 |
| ddr1_dqsn0 | Data strobe 0 invert | IO | AG25 |
| ddr1_dqs1 | Data strobe 1 input/output for byte 1 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading. | IO | AE27 |
| ddr1_dqsn1 | Data strobe 1 invert | IO | AE28 |
| ddr1_dqs2 | Data strobe 2 input/output for byte 2 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading. | IO | AD27 |
| ddr1_dqsn2 | Data strobe 2 invert | IO | AD28 |
| ddr1_dqs3 | Data strobe 3 input/output for byte 3 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading. | IO | Y28 |
| ddr1_dqsn3 | Data strobe 3 invert | IO | Y27 |
| ddr1_dqs_ecc | EMIF1 ECC Data strobe input/output. This signal is output to the EMIF1 memory when writing and input when reading. | IO | V27 |
| ddr1_dqsn_ecc | EMIF1 ECC Complementary Data strobe | IO | V28 |
| ddr1_vref0 | Reference Power Supply EMIF1 | A | Y18 |
| **EMIF Channel 2** | | | |
| ddr2_csn0 | EMIF2 Chip Select 0 | O | P24 |
| ddr2_cke | EMIF2 Clock Enable | O | U24 |
| ddr2_ck | EMIF2 Clock | O | T28 |
| ddr2_nck | EMIF2 Negative Clock | O | T27 |
| ddr2_odt0 | EMIF2 On-Die Termination for Chip Select 0 | O | R23 |
| ddr2_casn | EMIF2 Column Address Strobe | O | U28 |
| ddr2_rasn | EMIF2 Row Address Strobe | O | T23 |
| ddr2_wen | EMIF2 Write Enable | O | U25 |
| ddr2_rst | EMIF2 Reset output (DDR3-SDRAM only) | O | R24 |
| ddr2_ba0 | EMIF2 Bank Address | O | U23 |
| ddr2_ba1 | EMIF2 Bank Address | O | U27 |
| ddr2_ba2 | EMIF2 Bank Address | O | U26 |
| ddr2_a0 | EMIF2 Address Bus | O | R25 |
| ddr2_a1 | EMIF2 Address Bus | O | R26 |
| ddr2_a2 | EMIF2 Address Bus | O | R28 |
| ddr2_a3 | EMIF2 Address Bus | O | R27 |
| ddr2_a4 | EMIF2 Address Bus | O | P23 |
| ddr2_a5 | EMIF2 Address Bus | O | P22 |
| ddr2_a6 | EMIF2 Address Bus | O | P25 |
| ddr2_a7 | EMIF2 Address Bus | O | N20 |
| ddr2_a8 | EMIF2 Address Bus | O | P27 |
| ddr2_a9 | EMIF2 Address Bus | O | N27 |
| ddr2_a10 | EMIF2 Address Bus | O | N23 |
| ddr2_a11 | EMIF2 Address Bus | O | P26 |
| ddr2_a12 | EMIF2 Address Bus | O | N28 |
| ddr2_a13 | EMIF2 Address Bus | O | T22 |
| ddr2_a14 | EMIF2 Address Bus | O | R22 |
| ddr2_a15 | EMIF2 Address Bus | O | U22 |
| ddr2_d0 | EMIF2 Data Bus | IO | E26 |
| ddr2_d1 | EMIF2 Data Bus | IO | G25 |
| ddr2_d2 | EMIF2 Data Bus | IO | F25 |

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**Table 4-7. EMIF Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| ddr2_d3 | EMIF2 Data Bus | IO | F24 |
| ddr2_d4 | EMIF2 Data Bus | IO | F26 |
| ddr2_d5 | EMIF2 Data Bus | IO | F27 |
| ddr2_d6 | EMIF2 Data Bus | IO | E27 |
| ddr2_d7 | EMIF2 Data Bus | IO | E28 |
| ddr2_d8 | EMIF2 Data Bus | IO | H23 |
| ddr2_d9 | EMIF2 Data Bus | IO | H25 |
| ddr2_d10 | EMIF2 Data Bus | IO | H24 |
| ddr2_d11 | EMIF2 Data Bus | IO | H26 |
| ddr2_d12 | EMIF2 Data Bus | IO | G26 |
| ddr2_d13 | EMIF2 Data Bus | IO | J25 |
| ddr2_d14 | EMIF2 Data Bus | IO | J26 |
| ddr2_d15 | EMIF2 Data Bus | IO | J24 |
| ddr2_d16 | EMIF2 Data Bus | IO | L22 |
| ddr2_d17 | EMIF2 Data Bus | IO | K20 |
| ddr2_d18 | EMIF2 Data Bus | IO | K21 |
| ddr2_d19 | EMIF2 Data Bus | IO | L23 |
| ddr2_d20 | EMIF2 Data Bus | IO | L24 |
| ddr2_d21 | EMIF2 Data Bus | IO | J23 |
| ddr2_d22 | EMIF2 Data Bus | IO | K22 |
| ddr2_d23 | EMIF2 Data Bus | IO | J20 |
| ddr2_d24 | EMIF2 Data Bus | IO | L27 |
| ddr2_d25 | EMIF2 Data Bus | IO | L26 |
| ddr2_d26 | EMIF2 Data Bus | IO | L25 |
| ddr2_d27 | EMIF2 Data Bus | IO | L28 |
| ddr2_d28 | EMIF2 Data Bus | IO | M23 |
| ddr2_d29 | EMIF2 Data Bus | IO | M24 |
| ddr2_d30 | EMIF2 Data Bus | IO | M25 |
| ddr2_d31 | EMIF2 Data Bus | IO | M26 |
| ddr2_dqm0 | EMIF2 Data Mask | O | F28 |
| ddr2_dqm1 | EMIF2 Data Mask | O | G24 |
| ddr2_dqm2 | EMIF2 Data Mask | O | K23 |
| ddr2_dqm3 | EMIF2 Data Mask | O | M22 |
| ddr2_dqs0 | Data strobe 0 input/output for byte 0 of the 32-bit data bus. This signal is output to the EMIF2 memory when writing and input when reading. | IO | G28 |
| ddr2_dqsn0 | Data strobe 0 invert | IO | G27 |
| ddr2_dqs1 | Data strobe 1 input/output for byte 1 of the 32-bit data bus. This signal is output to the EMIF2 memory when writing and input when reading. | IO | H27 |
| ddr2_dqsn1 | Data strobe 1 invert | IO | H28 |
| ddr2_dqs2 | Data strobe 2 input/output for byte 2 of the 32-bit data bus. This signal is output to the EMIF2 memory when writing and input when reading. | IO | K27 |
| ddr2_dqsn2 | Data strobe 2 invert | IO | K28 |
| ddr2_dqs3 | Data strobe 3 input/output for byte 3 of the 32-bit data bus. This signal is output to the EMIF2 memory when writing and input when reading. | IO | M28 |
| ddr2_dqsn3 | Data strobe 3 invert | IO | M27 |
| ddr2_vref0 | Reference Power Supply EMIF2 | A | N22 |


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**NOTE**

The index numbers 1 and 2 which are part of the EMIF1 and EMIF2 signal prefixes (ddr1_* and ddr2_*) listed in Table 4-7, EMIF Signal Descriptions, not to be confused with DDR1 and DDR2 types of SDRAM memories.

### 4.4.5 General-Purpose Memory Controller (GPMC)

**NOTE**

For more information, see the Memory Subsystem / General-Purpose Memory Controller section of the device TRM.

**Table 4-8. GPMC Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| gpmc_ad0 | GPMC Data 0 in A/D nonmultiplexed mode and additionally Address 1 in A/D multiplexed mode | IO | M6 |
| gpmc_ad1 | GPMC Data 1 in A/D nonmultiplexed mode and additionally Address 2 in A/D multiplexed mode | IO | M2 |
| gpmc_ad2 | GPMC Data 2 in A/D nonmultiplexed mode and additionally Address 3 in A/D multiplexed mode | IO | L5 |
| gpmc_ad3 | GPMC Data 3 in A/D nonmultiplexed mode and additionally Address 4 in A/D multiplexed mode | IO | M1 |
| gpmc_ad4 | GPMC Data 4 in A/D nonmultiplexed mode and additionally Address 5 in A/D multiplexed mode | IO | L6 |
| gpmc_ad5 | GPMC Data 5 in A/D nonmultiplexed mode and additionally Address 6 in A/D multiplexed mode | IO | L4 |
| gpmc_ad6 | GPMC Data 6 in A/D nonmultiplexed mode and additionally Address 7 in A/D multiplexed mode | IO | L3 |
| gpmc_ad7 | GPMC Data 7 in A/D nonmultiplexed mode and additionally Address 8 in A/D multiplexed mode | IO | L2 |
| gpmc_ad8 | GPMC Data 8 in A/D nonmultiplexed mode and additionally Address 9 in A/D multiplexed mode | IO | L1 |
| gpmc_ad9 | GPMC Data 9 in A/D nonmultiplexed mode and additionally Address 10 in A/D multiplexed mode | IO | K2 |
| gpmc_ad10 | GPMC Data 10 in A/D nonmultiplexed mode and additionally Address 11 in A/D multiplexed mode | IO | J1 |
| gpmc_ad11 | GPMC Data 11 in A/D nonmultiplexed mode and additionally Address 12 in A/D multiplexed mode | IO | J2 |
| gpmc_ad12 | GPMC Data 12 in A/D nonmultiplexed mode and additionally Address 13 in A/D multiplexed mode | IO | H1 |
| gpmc_ad13 | GPMC Data 13 in A/D nonmultiplexed mode and additionally Address 14 in A/D multiplexed mode | IO | J3 |
| gpmc_ad14 | GPMC Data 14 in A/D nonmultiplexed mode and additionally Address 15 in A/D multiplexed mode | IO | H2 |
| gpmc_ad15 | GPMC Data 15 in A/D nonmultiplexed mode and additionally Address 16 in A/D multiplexed mode | IO | H3 |
| gpmc_a0 | GPMC Address 0. Only used to effectively address 8-bit data nonmultiplexed memories | O | R6/ P4 |
| gpmc_a1 | GPMC address 1 in A/D nonmultiplexed mode and Address 17 in A/D multiplexed mode | O | T9/ P1 |
| gpmc_a2 | GPMC address 2 in A/D nonmultiplexed mode and Address 18 in A/D multiplexed mode | O | T6/ N1 |
| gpmc_a3 | GPMC address 3 in A/D nonmultiplexed mode and Address 19 in A/D multiplexed mode | O | T7/ M4 |

**Table 4-8. GPMC Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| gpmc_a4 | GPMC address 4 in A/D nonmultiplexed mode and Address 20 in A/D multiplexed mode | O | P6 |
| gpmc_a5 | GPMC address 5 in A/D nonmultiplexed mode and Address 21 in A/D multiplexed mode | O | R9 |
| gpmc_a6 | GPMC address 6 in A/D nonmultiplexed mode and Address 22 in A/D multiplexed mode | O | R5 |
| gpmc_a7 | GPMC address 7 in A/D nonmultiplexed mode and Address 23 in A/D multiplexed mode | O | P5 |
| gpmc_a8 | GPMC address 8 in A/D nonmultiplexed mode and Address 24 in A/D multiplexed mode | O | N7 |
| gpmc_a9 | GPMC address 9 in A/D nonmultiplexed mode and Address 25 in A/D multiplexed mode | O | R4 |
| gpmc_a10 | GPMC address 10 in A/D nonmultiplexed mode and Address 26 in A/D multiplexed mode | O | N9 |
| gpmc_a11 | GPMC address 11 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | P9 |
| gpmc_a12 | GPMC address 12 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | P4 |
| gpmc_a13 | GPMC address 13 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | R3/ K7 |
| gpmc_a14 | GPMC address 14 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | T2/ M7 |
| gpmc_a15 | GPMC address 15 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | U2/ J5 |
| gpmc_a16 | GPMC address 16 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | U1/ K6 |
| gpmc_a17 | GPMC address 17 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | P3/ J7 |
| gpmc_a18 | GPMC address 18 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | R2/ J4 |
| gpmc_a19 | GPMC address 19 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | K7(3) / J6 |
| gpmc_a20 | GPMC address 20 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | M7(3) / H4 |
| gpmc_a21 | GPMC address 21 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | J5(3) / H5 |
| gpmc_a22 | GPMC address 22 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | K6(3) / H6 |
| gpmc_a23 | GPMC address 23 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | J7/ AG5/ N1 |
| gpmc_a24 | GPMC address 24 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | J4(3) / AF2 |
| gpmc_a25 | GPMC address 25 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | J6(3) / AF6 |
| gpmc_a26 | GPMC address 26 in A/D nonmultiplexed mode and unused in A/D multiplexed mode | O | H4(3) / AF3 |
| gpmc_a27 | GPMC address 27 in A/D nonmultiplexed mode and Address 27 in A/D multiplexed mode | O | H5(3) / AF4 |
| gpmc_cs0 | GPMC Chip Select 0 (active low) | O | T1 |
| gpmc_cs1 | GPMC Chip Select 1 (active low) | O | H6 |
| gpmc_cs2 | GPMC Chip Select 2 (active low) | O | P2 |
| gpmc_cs3 | GPMC Chip Select 3 (active low) | O | P1 |
| gpmc_cs4 | GPMC Chip Select 4 (active low) | O | N6 |
| gpmc_cs5 | GPMC Chip Select 5 (active low) | O | M4 |
| gpmc_cs6 | GPMC Chip Select 6 (active low) | O | N1 |


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**Table 4-8. GPMC Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| gpmc_cs7 | GPMC Chip Select 7 (active low) | O | P7 |
| gpmc_clk(1) (2) | GPMC Clock output | IO | P7 |
| gpmc_advn_ale | GPMC address valid active low or address latch enable | O | N1 |
| gpmc_oen_ren | GPMC output enable active low or read enable | O | M5 |
| gpmc_wen | GPMC write enable active low | O | M3 |
| gpmc_ben0 | GPMC lower-byte enable active low | O | N6 |
| gpmc_ben1 | GPMC upper-byte enable active low | O | M4 |
| gpmc_wait0 | GPMC external indication of wait 0 | I | N2 |
| gpmc_wait1 | GPMC external indication of wait 1 | I | P7/ N1 |

(1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between $V_{IH}$ and $V_{IL}$ must be less than $V_{HYS}$.

(2) The gpio6_16.clkout1 signal can be used as an “always-on” alternative to gpmc_clk provided that the external device can support the associated timing. See Table 7-26 *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Default* and Table 7-28 *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate* for timing information.

(3) The internal pull resistors for balls K7, M7, J5, K6, J4, J6, H4, H5 are permanently disabled when sysboot15 is set to 1 as described in the section *Sysboot Configuration* of the Device TRM. If internal pull-up/down resistors are desired on these balls then sysboot15 should be set to 0. If gpmc boot mode is used with SYSBOOT15=1 (not recommended) then external pull-downs should be implemented to keep the address bus at logic-0 value during boot since the gpmc ms-address bits are high-z during boot.

### 4.4.6 Timer

**NOTE**

For more information, see the Timers section of the device TRM.

**Table 4-9. Timer Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| timer1 | PWM output/event trigger input | IO | M4/ E21 |
| timer2 | PWM output/event trigger input | IO | N6/ F20 |
| timer3 | PWM output/event trigger input | IO | N1/ F21 |
| timer4 | PWM output/event trigger input | IO | P7/ D12 |
| timer5 | PWM output/event trigger input | IO | U2/ B12 |
| timer6 | PWM output/event trigger input | IO | T2/ A11 |
| timer7 | PWM output/event trigger input | IO | R3/ B13 |
| timer8 | PWM output/event trigger input | IO | P4/ A12 |
| timer9 | PWM output/event trigger input | IO | P9/ E14 |
| timer10 | PWM output/event trigger input | IO | N9/ A13 |
| timer11 | PWM output/event trigger input | IO | R4/ G14 |
| timer12 | PWM output/event trigger input | IO | N7/ F14 |
| timer13 | PWM output/event trigger input | IO | D18/ AF8 |
| timer14 | PWM output/event trigger input | IO | E17/ AE9 |
| timer15 | PWM output/event trigger input | IO | B26/ AF9/ AC10 |
| timer16 | PWM output/event trigger input | IO | C23/ AD9/ AB10 |

### 4.4.7 Inter-Integrated Circuit Interface ($I^2C$)

**NOTE**

For more information, see the Serial Communication Interface / Multimaster High-Speed I2C Controller / HS I2C Environment / HS I2C in I2C Mode section of the device TRM.

**NOTE**

I2C1 and I2C2 do NOT support HS-mode.

**Table 4-10. I²C Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **Inter-Integrated Circuit Interface 1 (I2C1)** | | | |
| i2c1_scl | I2C1 Clock | IOD | C20 |
| i2c1_sda | I2C1 Data | IOD | C21 |
| **Inter-Integrated Circuit Interface 2 (I2C2)** | | | |
| i2c2_scl | I2C2 Clock | IOD | F17 |
| i2c2_sda | I2C2 Data | IOD | C25 |
| **Inter-Integrated Circuit Interface 3 (I2C3)** | | | |
| i2c3_scl | I2C3 Clock | IOD | P7/ D14/ AB4/ F20 |
| i2c3_sda | I2C3 Data | IOD | N1/ C14/ AC5/ E21 |
| **Inter-Integrated Circuit Interface 4 (I2C4)** | | | |
| i2c4_scl | I2C4 Clock | IOD | R6/ J14/ A21/ Y9 |
| i2c4_sda | I2C4 Data | IOD | T9/ B14/ C18/ W7 |
| **Inter-Integrated Circuit Interface 5 (I2C5)** | | | |
| i2c5_scl | I2C5 Clock | IOD | AB9/ P6/ F12 |
| i2c5_sda | I2C5 Data | IOD | AA3/ R9/ G12 |

### *4.4.8 HDQ / 1-Wire Interface (HDQ1W)*

**NOTE**

For more information, see the Serial Communication Interface / HDQ/1-Wire section of the device TRM.

**Table 4-11. HDQ / 1-Wire Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| hdq0 | HDQ or 1-wire protocol single interface pin | IOD | D18/ C23 |

### *4.4.9 Universal Asynchronous Receiver Transmitter (UART)*

**NOTE**

For more information see the Serial Communication Interface / UART/IrDA/CIR section of the device TRM.

**Table 4-12. UART Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **Universal Asynchronous Receiver/Transmitter 1 (UART1)** | | | |
| uart1_dcdn | UART1 Data Carrier Detect active low | I | D28 |
| uart1_dsrn | UART1 Data Set Ready Active Low | I | D26 |
| uart1_dtrn | UART1 Data Terminal Ready Active Low | O | D27 |
| uart1_rin | UART1 Ring Indicator | I | C28 |
| uart1_rxd | UART1 Receive Data | I | B27 |
| uart1_txd | UART1 Transmit Data | O | C26 |
| uart1_ctsn | UART1 clear to send active low | I | E25 |


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**Table 4-12. UART Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| uart1_rtsn | UART1 request to send active low | O | C27 |
| **Universal Asynchronous Receiver/Transmitter 2 (UART2)** | | | |
| uart2_rxd | UART2 Receive Data | I | D28 |
| uart2_txd | UART2 Transmit Data | O | D26 |
| uart2_ctsn | UART2 clear to send active low | I | D27 |
| uart2_rtsn | UART2 request to send active low | O | C28 |
| **Universal Asynchronous Receiver/Transmitter 3 (UART3)/IrDA** | | | |
| uart3_rxd | UART3 Receive Data for both normal UART mode and IrDA mode. | I | V2/ AB3/ A26 / D27 |
| uart3_txd | UART3 Transmit Data | O | Y1/ AA4/ B22/ C28 |
| uart3_ctsn | UART3 clear to send active low | I | U4/ W9/ G17/ D28 |
| uart3_rtsn | UART3 request to send active low | O | V1/ V9/ D26/ B24 |
| uart3_rctx | Remote control data | O | D28 |
| uart3_sd | Infrared transceiver configure/shutdown | O | D26 |
| uart3_irtx | Infrared data output | O | C28 |
| **Universal Asynchronous Receiver/Transmitter 4 (UART4)** | | | |
| uart4_rxd | UART4 Receive Data | I | V7/ G16/ B21 |
| uart4_txd | UART4 Transmit Data | O | U7/ D17/ B20 |
| uart4_ctsn | UART4 clear to send active low | I | V6 |
| uart4_rtsn | UART4 request to send active low | O | U6 |
| **Universal Asynchronous Receiver/Transmitter 5 (UART5)** | | | |
| uart5_rxd | UART5 Receive Data | I | R6/ F11/ B19/ AC7/ G17 |
| uart5_txd | UART5 Transmit Data | O | T9/ G10/ C17/ AC6/ B24 |
| uart5_ctsn | UART5 clear to send active low | I | T6/ AC9 |
| uart5_rtsn | UART5 request to send active low | O | T7/ AC3 |
| **Universal Asynchronous Receiver/Transmitter 6 (UART6)** | | | |
| uart6_rxd | UART6 Receive Data | I | P6/ E8/ G12/ W7 |
| uart6_txd | UART6 Transmit Data | O | R9/ D9/ F12/ Y9 |
| uart6_ctsn | UART6 clear to send active low | I | R5/ G13 |
| uart6_rtsn | UART6 request to send active low | O | P5/ J11 |
| **Universal Asynchronous Receiver/Transmitter 7 (UART7)** | | | |
| uart7_rxd | UART7 Receive Data | I | T6/ AD9/ B7/ B18 |
| uart7_txd | UART7 Transmit Data | O | T7/ AF9/ B8/ F15 |
| uart7_ctsn | UART7 clear to send active low | I | AE9/ B19 |
| uart7_rtsn | UART7 request to send active low | O | AF8/ C17 |
| **Universal Asynchronous Receiver/Transmitter 8 (UART8)** | | | |
| uart8_rxd | UART8 Receive Data | I | AE8/ R5/ C18/ G20 |
| uart8_txd | UART8 Transmit Data | O | AD8/ P5/ A21/ G19 |
| uart8_ctsn | UART8 clear to send active low | I | AG7/ G16 |
| uart8_rtsn | UART8 request to send active low | O | AH6/ D17 |
| **Universal Asynchronous Receiver/Transmitter 9 (UART9)** | | | |
| uart9_rxd | UART9 Receive Data | I | G1/ AA3/ E25 |
| uart9_txd | UART9 Transmit Data | O | G6/ AB9/ C27 |
| uart9_ctsn | UART9 clear to send active low | I | F2/ AB3 |
| uart9_rtsn | UART9 request to send active low | O | F3/ AA4 |
| **Universal Asynchronous Receiver/Transmitter 10 (UART10)** | | | |
| uart10_rxd | UART10 Receive Data | I | D1/ E21/ AC8/ D27 |

**Table 4-12. UART Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| uart10_txd | UART10 Transmit Data | O | E2/ F20/ AD6/ C28 |
| uart10_ctsn | UART10 clear to send active low | I | D2/ AB8 |
| uart10_rtsn | UART10 request to send active low | O | F4/ AB5 |

### 4.4.10 Multichannel Serial Peripheral Interface (McSPI)

**CAUTION**

The I/O timings provided in Section 7, *Timing Requirements and Switching Characteristics* are applicable for all combinations of signals for SPI1 and SPI2. However, the timings are valid only for SPI3 and SPI4 if signals within a single IOSET are used. The IOSETS are defined in the Table 7-45.

**NOTE**

For more information, see the Serial Communication Interface / Multichannel Serial Peripheral Interface (McSPI) section of the device TRM.

**Table 4-13. SPI Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **Serial Peripheral Interface 1** | | | |
| spi1_sclk(1) | SPI1 Clock | IO | A25 |
| spi1_d1 | SPI1 Data. Can be configured as either MISO or MOSI. | IO | F16 |
| spi1_d0 | SPI1 Data. Can be configured as either MISO or MOSI. | IO | B25 |
| spi1_cs0 | SPI1 Chip Select | IO | A24 |
| spi1_cs1 | SPI1 Chip Select | IO | A22 |
| spi1_cs2 | SPI1 Chip Select | IO | B21 |
| spi1_cs3 | SPI1 Chip Select | IO | B20 |
| **Serial Peripheral Interface 2** | | | |
| spi2_sclk(1) | SPI2 Clock | IO | A26 |
| spi2_d1 | SPI2 Data. Can be configured as either MISO or MOSI. | IO | B22 |
| spi2_d0 | SPI2 Data. Can be configured as either MISO or MOSI. | IO | G17 |
| spi2_cs0 | SPI2 Chip Select | IO | B24 |
| spi2_cs1 | SPI2 Chip Select | IO | A22 |
| spi2_cs2 | SPI2 Chip Select | IO | B21 |
| spi2_cs3 | SPI2 Chip Select | IO | B20 |
| **Serial Peripheral Interface 3** | | | |
| spi3_sclk(1) | SPI3 Clock | IO | AD9/ V2/ B12/ E11/ AC4/ C18 |
| spi3_d1 | SPI3 Data. Can be configured as either MISO or MOSI. | IO | AF9/ Y1/ B10/ A11/ A21/ AC7 |
| spi3_d0 | SPI3 Data. Can be configured as either MISO or MOSI. | IO | AE9/ W9/ C11/ B13/ AC6/ G16 |
| spi3_cs0 | SPI3 Chip Select | IO | AF8/ V9/ D11/ A12/ AC9/ D17 |
| spi3_cs1 | SPI3 Chip Select | IO | B11/ AC3/ E14 |
| spi3_cs2 | SPI3 Chip Select | IO | F11 |
| spi3_cs3 | SPI3 Chip Select | IO | A10 |


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**Table 4-13. SPI Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **Serial Peripheral Interface 4** | | | |
| spi4_sclk[(1)] | SPI4 Clock | IO | N7/ G1/ AA3/ V7/ AC8 |
| spi4_d1 | SPI4 Data. Can be configured as either MISO or MOSI. | IO | R4/ G6/ AB9/ U7/ AD6 |
| spi4_d0 | SPI4 Data. Can be configured as either MISO or MOSI. | IO | N9/ F2/ AB3/ V6/ AB8 |
| spi4_cs0 | SPI4 Chip Select | IO | P9/ F3/ AA4/ U6/ AB5 |
| spi4_cs1 | SPI4 Chip Select | IO | P4/ Y1 |
| spi4_cs2 | SPI4 Chip Select | IO | R3/ W9 |
| spi4_cs3 | SPI4 Chip Select | IO | T2/ V9 |

(1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between $V_{IH}$ and $V_{IL}$ must be less than $V_{HYS}$.

### 4.4.11 Quad Serial Peripheral Interface (QSPI)

**NOTE**

For more information see the Serial Communication Interface / Quad Serial Peripheral Interface section of the device TRM.

**Table 4-14. QSPI Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| qspi1_sclk | QSPI1 Serial Clock | O | R2 |
| qspi1_rtclk | QSPI1 Return Clock Input. Must be connected from QSPI1_SCLK on PCB. Refer to PCB Guidelines for QSPI1. | I | R3 |
| qspi1_d0 | QSPI1 Data[0]. This pin is output data for all commands/writes and for dual read and quad read modes it becomes input data pin during read phase. | IO | U1 |
| qspi1_d1 | QSPI1 Data[1]. Input read data in all modes. | I | P3 |
| qspi1_d2 | QSPI1 Data[2]. This pin is used only in quad read mode as input data pin during read phase | I | U2 |
| qspi1_d3 | QSPI1 Data[3]. This pin is used only in quad read mode as input data pin during read phase | I | T2 |
| qspi1_cs0 | QSPI1 Chip Select[0]. This pin is Used for QSPI1 boot modes. | O | P2 |
| qspi1_cs1 | QSPI1 Chip Select[1] | O | P1 |
| qspi1_cs2 | QSPI1 Chip Select[2] | O | T7 |
| qspi1_cs3 | QSPI1 Chip Select[3] | O | P6 |

### 4.4.12 Multichannel Audio Serial Port (McASP)

**NOTE**

For more information, see the Serial Communication Interface / Multichannel Audio Serial Port (McASP) section of the device TRM.

**Table 4-15. McASP Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **Multichannel Audio Serial Port 1** | | | |
| mcasp1_axr0 | McASP1 Transmit/Receive Data | IO | G12 |

**Table 4-15. McASP Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| mcasp1_axr1 | McASP1 Transmit/Receive Data | IO | F12 |
| mcasp1_axr2 | McASP1 Transmit/Receive Data | IO | G13 |
| mcasp1_axr3 | McASP1 Transmit/Receive Data | IO | J11 |
| mcasp1_axr4 | McASP1 Transmit/Receive Data | IO | D18/ E12 |
| mcasp1_axr5 | McASP1 Transmit/Receive Data | IO | E17/ F13 |
| mcasp1_axr6 | McASP1 Transmit/Receive Data | IO | B26/ C12 |
| mcasp1_axr7 | McASP1 Transmit/Receive Data | IO | C23/ D12 |
| mcasp1_axr8 | McASP1 Transmit/Receive Data | IO | E21/ B12 |
| mcasp1_axr9 | McASP1 Transmit/Receive Data | IO | F20/ A11 |
| mcasp1_axr10 | McASP1 Transmit/Receive Data | IO | F21/ B13 |
| mcasp1_axr11 | McASP1 Transmit/Receive Data | IO | A12 |
| mcasp1_axr12 | McASP1 Transmit/Receive Data | IO | E14 |
| mcasp1_axr13 | McASP1 Transmit/Receive Data | IO | A13 |
| mcasp1_axr14 | McASP1 Transmit/Receive Data | IO | G14 |
| mcasp1_axr15 | McASP1 Transmit/Receive Data | IO | F14 |
| mcasp1_fsx | McASP1 Transmit Frame Sync | IO | D14 |
| mcasp1_aclkr(1) | McASP1 Receive Bit Clock | IO | B14 |
| mcasp1_fsr | McASP1 Receive Frame Sync | IO | J14 |
| mcasp1_ahclkx | McASP1 Transmit High-Frequency Master Clock | O | D18 |
| mcasp1_aclkx(1) | McASP1 Transmit Bit Clock | IO | C14 |
| **Multichannel Audio Serial Port 2** | | | |
| mcasp2_axr0 | McASP2 Transmit/Receive Data | IO | B15 |
| mcasp2_axr1 | McASP2 Transmit/Receive Data | IO | A15 |
| mcasp2_axr2 | McASP2 Transmit/Receive Data | IO | C15 |
| mcasp2_axr3 | McASP2 Transmit/Receive Data | IO | A16 |
| mcasp2_axr4 | McASP2 Transmit/Receive Data | IO | D15 |
| mcasp2_axr5 | McASP2 Transmit/Receive Data | IO | B16 |
| mcasp2_axr6 | McASP2 Transmit/Receive Data | IO | B17 |
| mcasp2_axr7 | McASP2 Transmit/Receive Data | IO | A17 |
| mcasp2_axr8 | McASP2 Transmit/Receive Data | IO | D18 |
| mcasp2_axr9 | McASP2 Transmit/Receive Data | IO | E17 |
| mcasp2_axr10 | McASP2 Transmit/Receive Data | IO | B26 |
| mcasp2_axr11 | McASP2 Transmit/Receive Data | IO | C23 |
| mcasp2_axr12 | McASP2 Transmit/Receive Data | IO | B18 |
| mcasp2_axr13 | McASP2 Transmit/Receive Data | IO | F15 |
| mcasp2_axr14 | McASP2 Transmit/Receive Data | IO | B19 |
| mcasp2_axr15 | McASP2 Transmit/Receive Data | IO | C17 |
| mcasp2_fsx | McASP2 Transmit Frame Sync | IO | A18 |
| mcasp2_aclkr(1) | McASP2 Receive Bit Clock | IO | E15 |
| mcasp2_fsr | McASP2 Receive Frame Sync | IO | A20 |
| mcasp2_ahclkx | McASP2 Transmit High-Frequency Master Clock | O | E17 |
| mcasp2_aclkx(1) | McASP2 Transmit Bit Clock | IO | A19 |
| **Multichannel Audio Serial Port 3** | | | |
| mcasp3_axr0 | McASP3 Transmit/Receive Data | IO | B19 |
| mcasp3_axr1 | McASP3 Transmit/Receive Data | IO | C17 |
| mcasp3_axr2 | McASP3 Transmit/Receive Data | IO | C15 |
| mcasp3_axr3 | McASP3 Transmit/Receive Data | IO | A16 |


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**Table 4-15. McASP Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| mcasp3_fsx | McASP3 Transmit Frame Sync | IO | F15 |
| mcasp3_ahclkx | McASP3 Transmit High-Frequency Master Clock | O | B26 |
| mcasp3_aclkx(1) | McASP3 Transmit Bit Clock | IO | B18 |
| mcasp3_aclkr(1) | McASP3 Receive Bit Clock | IO | B18 |
| mcasp3_fsr | McASP3 Receive Frame Sync | IO | F15 |
| **Multichannel Audio Serial Port 4** | | | |
| mcasp4_axr0 | McASP4 Transmit/Receive Data | IO | G16 |
| mcasp4_axr1 | McASP4 Transmit/Receive Data | IO | D17 |
| mcasp4_axr2 | McASP4 Transmit/Receive Data | IO | E12 |
| mcasp4_axr3 | McASP4 Transmit/Receive Data | IO | F13 |
| mcasp4_fsx | McASP4 Transmit Frame Sync | IO | A21 |
| mcasp4_ahclkx | McASP4 Transmit High-Frequency Master Clock | O | C23 |
| mcasp4_aclkx(1) | McASP4 Transmit Bit Clock | IO | C18 |
| mcasp4_aclkr(1) | McASP4 Receive Bit Clock | IO | C18 |
| mcasp4_fsr | McASP4 Receive Frame Sync | IO | A21 |
| **Multichannel Audio Serial Port 5** | | | |
| mcasp5_axr0 | McASP5 Transmit/Receive Data | IO | AB3 |
| mcasp5_axr1 | McASP5 Transmit/Receive Data | IO | AA4 |
| mcasp5_axr2 | McASP5 Transmit/Receive Data | IO | C12 |
| mcasp5_axr3 | McASP5 Transmit/Receive Data | IO | D12 |
| mcasp5_fsx | McASP5 Transmit Frame Sync | IO | AB9 |
| mcasp5_ahclkx | McASP5 Transmit High-Frequency Master Clock | O | D18 |
| mcasp5_aclkx(1) | McASP5 Transmit Bit Clock | IO | AA3 |
| mcasp5_aclkr(1) | McASP5 Receive Bit Clock | IO | AA3 |
| mcasp5_fsr | McASP5 Receive Frame Sync | IO | AB9 |
| **Multichannel Audio Serial Port 6** | | | |
| mcasp6_axr0 | McASP6 Transmit/Receive Data | IO | B12 |
| mcasp6_axr1 | McASP6 Transmit/Receive Data | IO | A11 |
| mcasp6_axr2 | McASP6 Transmit/Receive Data | IO | G13 |
| mcasp6_axr3 | McASP6 Transmit/Receive Data | IO | J11 |
| mcasp6_ahclkx | McASP6 Transmit High-Frequency Master Clock | O | E17 |
| mcasp6_aclkx(1) | McASP6 Transmit Bit Clock | IO | B13 |
| mcasp6_fsx | McASP6 Transmit Frame Sync | IO | A12 |
| mcasp6_aclkr(1) | McASP6 Receive Bit Clock | IO | B13 |
| mcasp6_fsr | McASP6 Receive Frame Sync | IO | A12 |
| **Multichannel Audio Serial Port 7** | | | |
| mcasp7_axr0 | McASP7 Transmit/Receive Data | IO | E14 |
| mcasp7_axr1 | McASP7 Transmit/Receive Data | IO | A13 |
| mcasp7_axr2 | McASP7 Transmit/Receive Data | IO | B14 |
| mcasp7_axr3 | McASP7 Transmit/Receive Data | IO | J14 |
| mcasp7_ahclkx | McASP7 Transmit High-Frequency Master Clock | O | B26 |
| mcasp7_aclkx(1) | McASP7 Transmit Bit Clock | IO | G14 |
| mcasp7_fsx | McASP7 Transmit Frame Sync | IO | F14 |
| mcasp7_aclkr(1) | McASP7 Receive Bit Clock | IO | G14 |
| mcasp7_fsr | McASP7 Receive Frame Sync | IO | F14 |
| **Multichannel Audio Serial Port 8** | | | |
| mcasp8_axr0 | McASP8 Transmit/Receive Data | IO | D15 |

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**Table 4-15. McASP Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| mcasp8_axr1 | McASP8 Transmit/Receive Data | IO | B16 |
| mcasp8_axr2 | McASP8 Transmit/Receive Data | IO | E15 |
| mcasp8_axr3 | McASP8 Transmit/Receive Data | IO | A20 |
| mcasp8_ahclkx | McASP8 Transmit High-Frequency Master Clock | O | C23 |
| mcasp8_aclkx(1) | McASP8 Transmit Bit Clock | IO | B17 |
| mcasp8_fsx | McASP8 Transmit Frame Sync | IO | A17 |
| mcasp8_aclkr(1) | McASP8 Receive Bit Clock | IO | B17 |
| mcasp8_fsr | McASP8 Receive Frame Sync | IO | A17 |

(1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between $V_{IH}$ and $V_{IL}$ must be less than $V_{HYS}$.

### 4.4.13 Universal Serial Bus (USB)

**NOTE**

For more information, see: Serial Communication Interface / SuperSpeed USB DRD Subsystem section of the device TRM.

**Table 4-16. USB Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **Universal Serial Bus 1** | | | |
| usb1_dp | USB1 USB2.0 differential signal pair (positive) | IODS | AD12 |
| usb1_dm | USB1 USB2.0 differential signal pair (negative) | IODS | AC12 |
| usb1_drvvbus | USB1 Drive VBUS signal | O | AB10 |
| usb_rxn0 | USB1 USB3.0 receiver negative lane | IDS | AF12 |
| usb_rxp0 | USB1 USB3.0 receiver positive lane | IDS | AE12 |
| usb_txn0 | USB1 USB3.0 transmitter negative lane | ODS | AC11 |
| usb_txp0 | USB1 USB3.0 transmitter positive lane | ODS | AD11 |
| **Universal Serial Bus 2** | | | |
| usb2_dp | USB2 USB2.0 differential signal pair (positive) | IODS | AE11 |
| usb2_dm | USB2 USB2.0 differential signal pair (negative) | IODS | AF11 |
| usb2_drvvbus | USB2 Drive VBUS signal | O | AC10 |

### 4.4.14 Serial Advanced Technology Attachment (SATA)

**NOTE**

For more information, see the Serial Communication Interfaces / SATA section of the device TRM.

**Table 4-17. SATA Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| sata1_rxn0 | SATA differential negative receiver lane 0 | IDS | AH9 |
| sata1_rxp0 | SATA differential positive receiver lane 0 | IDS | AG9 |
| sata1_txn0 | SATA differential negative transmitter lane 0 | ODS | AG10 |
| sata1_txp0 | SATA differential positive transmitter lane 0 | ODS | AH10 |
| sata1_led | SATA channel activity indicator | O | A22/ G19 |


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### 4.4.15 Peripheral Component Interconnect Express (PCIe)

**NOTE**

For more information, see the *Serial Communication Interfaces / PCIe Controllers* and the *Shared PHY Component Subsystems / PCIe Shared PHY Subsystem* sections of the device TRM.

**Table 4-18. PCIe Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| pcie_rxn0 | PCIe1_PHY_RX Receive Data Lane 0 (negative) - mapped to PCIe_SS1 only. | IDS | AG13 |
| pcie_rxp0 | PCIe1_PHY_RX Receive Data Lane 0 (positive) - mapped to PCIe_SS1 only. | IDS | AH13 |
| pcie_txn0 | PCIe1_PHY_TX Transmit Data Lane 0 (negative) - mapped to PCIe_SS1 only. | ODS | AG14 |
| pcie_txp0 | PCIe1_PHY_TX Transmit Data Lane 0 (positive) - mapped to PCIe_SS1 only. | ODS | AH14 |
| pcie_rxn1 | PCIe2_PHY_RX Receive Data Lane 1 (negative) - mapped to either PCIe_SS1 (dual lane- mode) or PCIe_SS2 (single lane- mode) | IDS | AG11 |
| pcie_rxp1 | PCIe2_PHY_RX Receive Data Lane 1 (positive) - mapped to either PCIe_SS1 (dual lane- mode) or PCIe_SS2 (single lane- mode) | IDS | AH11 |
| pcie_txn1 | PCIe2_PHY_TX Transmit Data Lane 1 (negative) - mapped to either PCIe_SS1 (dual lane- mode) or PCIe_SS2 (single lane- mode) | ODS | AG12 |
| pcie_txp1 | PCIe2_PHY_TX Transmit Data Lane 1 (positive) - mapped to either PCIe_SS1 (dual lane- mode) or PCIe_SS2 (single lane- mode) | ODS | AH12 |
| ljcb_clkp | PCIe1_PHY / PCIe2_PHY shared Reference Clock Input / Output Differential Pair (positive) | IODS | AG15 |
| ljcb_clkn | PCIe1_PHY / PCIe2_PHY shared Reference Clock Input / Output Differential Pair (negative) | IODS | AH15 |

### 4.4.16 Controller Area Network Interface (DCAN)

**NOTE**

For more information, see the Serial Communication Interface / DCAN section of the device TRM.

**Table 4-19. DCAN Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **DCAN 1** | | | |
| dcan1_tx | DCAN1 transmit data pin | IO | G20 |
| dcan1_rx | DCAN1 receive data pin | IO | G19/ AD17 |
| **DCAN 2** | | | |
| dcan2_tx | DCAN2 transmit data pin | IO | E21/ B21 |
| dcan2_rx | DCAN2 receive data pin | IO | F20/ AC17/ B20 |

### 4.4.17 Ethernet Interface (GMAC_SW)

**CAUTION**

The I/O timings provided in Section 7, *Timing Requirements and Switching Characteristics* are valid only if signals within a single IOSET are used. The IOSETs are defined in the Table 7-72, Table 7-75, Table 7-80 and Table 7-87.

**NOTE**

For more information, see the Serial Communication Interfaces / Ethernet Controller section of the device TRM.

### Table 4-20. GMAC Signal Descriptions

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| rgmii0_txc | RGMII0 Transmit Clock | O | W9 |
| rgmii0_txctl | RGMII0 Transmit Enable | O | V9 |
| rgmii0_txd3 | RGMII0 Transmit Data | O | V7 |
| rgmii0_txd2 | RGMII0 Transmit Data | O | U7 |
| rgmii0_txd1 | RGMII0 Transmit Data | O | V6 |
| rgmii0_txd0 | RGMII0 Transmit Data | O | U6 |
| rgmii0_rxc | RGMII0 Receive Clock | I | U5 |
| rgmii0_rxctl | RGMII0 Receive Control | I | V5 |
| rgmii0_rxd3 | RGMII0 Receive Data | I | V4 |
| rgmii0_rxd2 | RGMII0 Receive Data | I | V3 |
| rgmii0_rxd1 | RGMII0 Receive Data | I | Y2 |
| rgmii0_rxd0 | RGMII0 Receive Data | I | W2 |
| rgmii1_txc | RGMII1 Transmit Clock | O | D5 |
| rgmii1_txctl | RGMII1 Transmit Enable | O | C2 |
| rgmii1_txd3 | RGMII1 Transmit Data | O | C3 |
| rgmii1_txd2 | RGMII1 Transmit Data | O | C4 |
| rgmii1_txd1 | RGMII1 Transmit Data | O | B2 |
| rgmii1_txd0 | RGMII1 Transmit Data | O | D6 |
| rgmii1_rxc | RGMII1 Receive Clock | I | C5 |
| rgmii1_rxctl | RGMII1 Receive Control | I | A3 |
| rgmii1_rxd3 | RGMII1 Receive Data | I | B3 |
| rgmii1_rxd2 | RGMII1 Receive Data | I | B4 |
| rgmii1_rxd1 | RGMII1 Receive Data | I | B5 |
| rgmii1_rxd0 | RGMII1 Receive Data | I | A4 |
| mii1_rxd1 | MII1 Receive Data | I | C1 |
| mii1_rxd2 | MII1 Receive Data | I | E4 |
| mii1_rxd3 | MII1 Receive Data | I | F5 |
| mii1_rxd0 | MII1 Receive Data | I | E6 |
| mii1_rxclk | MII1 Receive Clock | I | D5 |
| mii1_rxdv | MII1 Receive Data Valid | I | C2 |
| mii1_txclk | MII1 Transmit Clock | I | C3 |
| mii1_txd0 | MII1 Transmit Data | O | C4 |
| mii1_txd1 | MII1 Transmit Data | O | B2 |
| mii1_txd2 | MII1 Transmit Data | O | D6 |
| mii1_txd3 | MII1 Transmit Data | O | C5 |
| mii1_txer | MII1 Transmit Error | O | A3 |
| mii1_rxer | MII1 Receive Data Error | I | B3 |
| mii1_col | MII1 Collision Detect (Sense) | I | B4 |
| mii1_crs | MII1 Carrier Sense | I | B5 |
| mii1_txen | MII1 Transmit Data Enable | O | A4 |
| mii0_rxd1 | MII0 Receive Data | I | V6 |
| mii0_rxd2 | MII0 Receive Data | I | V9 |


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**Table 4-20. GMAC Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| mii0_rxd3 | MII0 Receive Data | I | W9 |
| mii0_rxd0 | MII0 Receive Data | I | U6 |
| mii0_rxclk | MII0 Receive Clock | I | Y1 |
| mii0_rxdv | MII0 Receive Data Valid | I | V2 |
| mii0_txclk | MII0 Transmit Clock | I | U5 |
| mii0_txd0 | MII0 Transmit Data | O | W2 |
| mii0_txd1 | MII0 Transmit Data | O | Y2 |
| mii0_txd2 | MII0 Transmit Data | O | V4 |
| mii0_txd3 | MII0 Transmit Data | O | V5 |
| mii0_txer | MII0 Transmit Error | O | U4 |
| mii0_rxer | MII0 Receive Data Error | I | U7 |
| mii0_col | MII0 Collision Detect (Sense) | I | V1 |
| mii0_crs | MII0 Carrier Sense | I | V7 |
| mii0_txen | MII0 Transmit Data Enable | O | V3 |
| rmii0_crs | RMII0 Carrier Sense | I | V7 |
| rmii0_rxer | RMII0 Receive Data Error | I | U7 |
| rmii0_rxd1 | RMII0 Receive Data | I | V6 |
| rmii0_rxd0 | RMII0 Receive Data | I | U6 |
| rmii0_txen | RMII0 Transmit Data Enable | O | V3 |
| rmii1_crs | RMII1 Carrier Sense | I | V2 |
| rmii1_rxer | RMII1 Receive Data Error | I | Y1 |
| rmii1_rxd1 | RMII1 Receive Data | I | W9 |
| rmii1_rxd0 | RMII1 Receive Data | I | V9 |
| rmii1_txen | RMII1 Transmit Data Enable | O | U5 |
| rmii1_txd1 | RMII1 Transmit Data | O | V5 |
| rmii1_txd0 | RMII1 Transmit Data | O | V4 |
| rmii0_txd1 | RMII0 Transmit Data | O | Y2 |
| rmii0_txd0 | RMII0 Transmit Data | O | W2 |
| mdio_d | MDIO Data | O | AB4/ B20/ F6/ U4 |
| mdio_mclk | MDIO Clock | O | AC5/ B21/ D3/ V1 |

### *4.4.18 Media Local Bus (MLB) Interface*

**NOTE**

Media Local Bus (MLB) is not available on this device, and balls listed in Table 4-21 must be left unconnected.

**Table 4-21. MLB Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| mlbp_sig_p | Media Local Bus (MLB) Subsystem signal differential pair (positive) | IODS | AC1 |
| mlbp_sig_n | Media Local Bus (MLB) Subsystem signal differential pair (negative) | IODS | AC2 |
| mlbp_dat_p | Media Local Bus (MLB) Subsystem data differential pair (positive) | IODS | AA1 |
| mlbp_dat_n | Media Local Bus (MLB) Subsystem data differential pair (negative) | IODS | AA2 |
| mlbp_clk_p | Media Local Bus (MLB) Subsystem clock differential pair (positive) | IDS | AB1 |
| mlbp_clk_n | Media Local Bus (MLB) Subsystem clock differential pair (negative) | IDS | AB2 |

### 4.4.19 eMMC/SD/SDIO

**NOTE**
For more information, see the HS MMC/SDIO section of the device TRM.

**Table 4-22. eMMC/SD/SDIO Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **Multi Media Card 1** | | | |
| mmc1_clk[(1)] | MMC1 clock | IO | W6 |
| mmc1_cmd | MMC1 command | IO | Y6 |
| mmc1_sdcd | MMC1 Card Detect | I | W7 |
| mmc1_sdwp | MMC1 Write Protect | I | Y9 |
| mmc1_dat0 | MMC1 data bit 0 | IO | AA6 |
| mmc1_dat1 | MMC1 data bit 1 | IO | Y4 |
| mmc1_dat2 | MMC1 data bit 2 | IO | AA5 |
| mmc1_dat3 | MMC1 data bit 3 | IO | Y3 |
| **Multi Media Card 2** | | | |
| mmc2_clk[(1)] | MMC2 clock | IO | J7 |
| mmc2_cmd | MMC2 command | IO | H6 |
| mmc2_sdcd | MMC2 Card Detect | I | G20 |
| mmc2_sdwp | MMC2 Write Protect | I | G19 |
| mmc2_dat0 | MMC2 data bit 0 | IO | J4 |
| mmc2_dat1 | MMC2 data bit 1 | IO | J6 |
| mmc2_dat2 | MMC2 data bit 2 | IO | H4 |
| mmc2_dat3 | MMC2 data bit 3 | IO | H5 |
| mmc2_dat4 | MMC2 data bit 4 | IO | K7 |
| mmc2_dat5 | MMC2 data bit 5 | IO | M7 |
| mmc2_dat6 | MMC2 data bit 6 | IO | J5 |
| mmc2_dat7 | MMC2 data bit 7 | IO | K6 |
| **Multi Media Card 3** | | | |
| mmc3_clk[(1)] | MMC3 clock | IO | AD4 |
| mmc3_cmd | MMC3 command | IO | AC4 |
| mmc3_sdcd | MMC3 Card Detect | I | B21 |
| mmc3_sdwp | MMC3 Write Protect | I | B20 |
| mmc3_dat0 | MMC3 data bit 0 | IO | AC7 |
| mmc3_dat1 | MMC3 data bit 1 | IO | AC6 |
| mmc3_dat2 | MMC3 data bit 2 | IO | AC9 |
| mmc3_dat3 | MMC3 data bit 3 | IO | AC3 |
| mmc3_dat4 | MMC3 data bit 4 | IO | AC8 |
| mmc3_dat5 | MMC3 data bit 5 | IO | AD6 |
| mmc3_dat6 | MMC3 data bit 6 | IO | AB8 |
| mmc3_dat7 | MMC3 data bit 7 | IO | AB5 |
| **Multi Media Card 4** | | | |
| mmc4_clk[(1)] | MMC4 clock | IO | E25 |
| mmc4_cmd | MMC4 command | IO | C27 |
| mmc4_sdcd | MMC4 Card Detect | I | B27 |
| mmc4_sdwp | MMC4 Write Protect | I | C26 |
| mmc4_dat0 | MMC4 data bit 0 | IO | D28 |
| mmc4_dat1 | MMC4 data bit 1 | IO | D26 |


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**Table 4-22. eMMC/SD/SDIO Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| mmc4_dat2 | MMC4 data bit 2 | IO | D27 |
| mmc4_dat3 | MMC4 data bit 3 | IO | C28 |

(1) By default, this clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. mmc1_clk and mmc2_clk have an optional software programmable setting to use an 'internal loopback clock' instead of the default 'pad loopback clock'. If the 'pad loopback clock' is used, series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between $V_{IH}$ and $V_{IL}$ must be less than $V_{HYS}$.

### *4.4.20 General-Purpose Interface (GPIO)*

**NOTE**

For more information, see the General-Purpose Interface section of the device TRM.

**Table 4-23. GPIOs Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **GPIO 1** | | | |
| gpio1_0 | General-Purpose Input | I | AD17 |
| gpio1_1 | General-Purpose Input | I | AC17 |
| gpio1_2 | General-Purpose Input | I | AB16 |
| gpio1_3 | General-Purpose Input | I | AC16 |
| gpio1_4 | General-Purpose Input/Output | IO | D15 |
| gpio1_5 | General-Purpose Input/Output | IO | A17 |
| gpio1_6 | General-Purpose Input/Output | IO | M6 |
| gpio1_7 | General-Purpose Input/Output | IO | M2 |
| gpio1_8 | General-Purpose Input/Output | IO | L5 |
| gpio1_9 | General-Purpose Input/Output | IO | M1 |
| gpio1_10 | General-Purpose Input/Output | IO | L6 |
| gpio1_11 | General-Purpose Input/Output | IO | L4 |
| gpio1_12 | General-Purpose Input/Output | IO | L3 |
| gpio1_13 | General-Purpose Input/Output | IO | L2 |
| gpio1_14 | General-Purpose Input/Output | IO | G20 |
| gpio1_15 | General-Purpose Input/Output | IO | G19 |
| gpio1_16 | General-Purpose Input/Output | IO | D27 |
| gpio1_17 | General-Purpose Input/Output | IO | C28 |
| gpio1_18 | General-Purpose Input/Output | IO | H1 |
| gpio1_19 | General-Purpose Input/Output | IO | J3 |
| gpio1_20 | General-Purpose Input/Output | IO | H2 |
| gpio1_21 | General-Purpose Input/Output | IO | H3 |
| gpio1_22 | General-Purpose Input/Output | IO | AC8 |
| gpio1_23 | General-Purpose Input/Output | IO | AD6 |
| gpio1_24 | General-Purpose Input/Output | IO | AB8 |
| gpio1_25 | General-Purpose Input/Output | IO | AB5 |
| gpio1_26 | General-Purpose Input/Output | IO | P6 |
| gpio1_27 | General-Purpose Input/Output | IO | R9 |
| gpio1_28 | General-Purpose Input/Output | IO | R5 |
| gpio1_29 | General-Purpose Input/Output | IO | P5 |
| gpio1_30 | General-Purpose Input/Output | IO | N7 |
| gpio1_31 | General-Purpose Input/Output | IO | R4 |

### Table 4-23. GPIOs Signal Descriptions (continued)

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **GPIO 2** | | | |
| gpio2_0 | General-Purpose Input/Output | IO | N9 |
| gpio2_1 | General-Purpose Input/Output | IO | P9 |
| gpio2_2 | General-Purpose Input/Output | IO | P4 |
| gpio2_3 | General-Purpose Input/Output | IO | R3 |
| gpio2_4 | General-Purpose Input/Output | IO | T2 |
| gpio2_5 | General-Purpose Input/Output | IO | U2 |
| gpio2_6 | General-Purpose Input/Output | IO | U1 |
| gpio2_7 | General-Purpose Input/Output | IO | P3 |
| gpio2_8 | General-Purpose Input/Output | IO | R2 |
| gpio2_9 | General-Purpose Input/Output | IO | K7 |
| gpio2_10 | General-Purpose Input/Output | IO | M7 |
| gpio2_11 | General-Purpose Input/Output | IO | J5 |
| gpio2_12 | General-Purpose Input/Output | IO | K6 |
| gpio2_13 | General-Purpose Input/Output | IO | J7 |
| gpio2_14 | General-Purpose Input/Output | IO | J4 |
| gpio2_15 | General-Purpose Input/Output | IO | J6 |
| gpio2_16 | General-Purpose Input/Output | IO | H4 |
| gpio2_17 | General-Purpose Input/Output | IO | H5 |
| gpio2_18 | General-Purpose Input/Output | IO | H6 |
| gpio2_19 | General-Purpose Input/Output | IO | T1 |
| gpio2_20 | General-Purpose Input/Output | IO | P2 |
| gpio2_21 | General-Purpose Input/Output | IO | P1 |
| gpio2_22 | General-Purpose Input/Output | IO | P7 |
| gpio2_23 | General-Purpose Input/Output | IO | N1 |
| gpio2_24 | General-Purpose Input/Output | IO | M5 |
| gpio2_25 | General-Purpose Input/Output | IO | M3 |
| gpio2_26 | General-Purpose Input/Output | IO | N6 |
| gpio2_27 | General-Purpose Input/Output | IO | M4 |
| gpio2_28 | General-Purpose Input/Output | IO | N2 |
| gpio2_29 | General-Purpose Input/Output | IO | B17 |
| gpio2_30 | General-Purpose Input/Output | IO | AG8 |
| gpio2_31 | General-Purpose Input/Output | IO | AH7 |
| **GPIO 3** | | | |
| gpio3_0 | General-Purpose Input/Output | IO | AD9 |
| gpio3_1 | General-Purpose Input/Output | IO | AF9 |
| gpio3_2 | General-Purpose Input/Output | IO | AE9 |
| gpio3_3 | General-Purpose Input/Output | IO | AF8 |
| gpio3_4 | General-Purpose Input/Output | IO | AE8 |
| gpio3_5 | General-Purpose Input/Output | IO | AD8 |
| gpio3_6 | General-Purpose Input/Output | IO | AG7 |
| gpio3_7 | General-Purpose Input/Output | IO | AH6 |
| gpio3_8 | General-Purpose Input/Output | IO | AH3 |
| gpio3_9 | General-Purpose Input/Output | IO | AH5 |
| gpio3_10 | General-Purpose Input/Output | IO | AG6 |
| gpio3_11 | General-Purpose Input/Output | IO | AH4 |
| gpio3_12 | General-Purpose Input/Output | IO | AG4 |


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**Table 4-23. GPIOs Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| gpio3_13 | General-Purpose Input/Output | IO | AG2 |
| gpio3_14 | General-Purpose Input/Output | IO | AG3 |
| gpio3_15 | General-Purpose Input/Output | IO | AG5 |
| gpio3_16 | General-Purpose Input/Output | IO | AF2 |
| gpio3_17 | General-Purpose Input/Output | IO | AF6 |
| gpio3_18 | General-Purpose Input/Output | IO | AF3 |
| gpio3_19 | General-Purpose Input/Output | IO | AF4 |
| gpio3_20 | General-Purpose Input/Output | IO | AF1 |
| gpio3_21 | General-Purpose Input/Output | IO | AE3 |
| gpio3_22 | General-Purpose Input/Output | IO | AE5 |
| gpio3_23 | General-Purpose Input/Output | IO | AE1 |
| gpio3_24 | General-Purpose Input/Output | IO | AE2 |
| gpio3_25 | General-Purpose Input/Output | IO | AE6 |
| gpio3_26 | General-Purpose Input/Output | IO | AD2 |
| gpio3_27 | General-Purpose Input/Output | IO | AD3 |
| gpio3_28 | General-Purpose Input/Output | IO | E1 |
| gpio3_29 | General-Purpose Input/Output | IO | G2 |
| gpio3_30 | General-Purpose Input/Output | IO | H7 |
| gpio3_31 | General-Purpose Input/Output | IO | G1 |
| **GPIO 4** | | | |
| gpio4_0 | General-Purpose Input/Output | IO | G6 |
| gpio4_1 | General-Purpose Input/Output | IO | F2 |
| gpio4_2 | General-Purpose Input/Output | IO | F3 |
| gpio4_3 | General-Purpose Input/Output | IO | D1 |
| gpio4_4 | General-Purpose Input/Output | IO | E2 |
| gpio4_5 | General-Purpose Input/Output | IO | D2 |
| gpio4_6 | General-Purpose Input/Output | IO | F4 |
| gpio4_7 | General-Purpose Input/Output | IO | C1 |
| gpio4_8 | General-Purpose Input/Output | IO | E4 |
| gpio4_9 | General-Purpose Input/Output | IO | F5 |
| gpio4_10 | General-Purpose Input/Output | IO | E6 |
| gpio4_11 | General-Purpose Input/Output | IO | D3 |
| gpio4_12 | General-Purpose Input/Output | IO | F6 |
| gpio4_13 | General-Purpose Input/Output | IO | D5 |
| gpio4_14 | General-Purpose Input/Output | IO | C2 |
| gpio4_15 | General-Purpose Input/Output | IO | C3 |
| gpio4_16 | General-Purpose Input/Output | IO | C4 |
| gpio4_17 | General-Purpose Input/Output | IO | A12 |
| gpio4_18 | General-Purpose Input/Output | IO | E14 |
| gpio4_19 | General-Purpose Input/Output | IO | D11 |
| gpio4_20 | General-Purpose Input/Output | IO | B10 |
| gpio4_21 | General-Purpose Input/Output | IO | B11 |
| gpio4_22 | General-Purpose Input/Output | IO | C11 |
| gpio4_23 | General-Purpose Input/Output | IO | E11 |
| gpio4_24 | General-Purpose Input/Output | IO | B2 |
| gpio4_25 | General-Purpose Input/Output | IO | D6 |
| gpio4_26 | General-Purpose Input/Output | IO | C5 |

### Table 4-23. GPIOs Signal Descriptions (continued)

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| gpio4_27 | General-Purpose Input/Output | IO | A3 |
| gpio4_28 | General-Purpose Input/Output | IO | B3 |
| gpio4_29 | General-Purpose Input/Output | IO | B4 |
| gpio4_30 | General-Purpose Input/Output | IO | B5 |
| gpio4_31 | General-Purpose Input/Output | IO | A4 |
| **GPIO 5** | | | |
| gpio5_0 | General-Purpose Input/Output | IO | B14 |
| gpio5_1 | General-Purpose Input/Output | IO | J14 |
| gpio5_2 | General-Purpose Input/Output | IO | G12 |
| gpio5_3 | General-Purpose Input/Output | IO | F12 |
| gpio5_4 | General-Purpose Input/Output | IO | G13 |
| gpio5_5 | General-Purpose Input/Output | IO | J11 |
| gpio5_6 | General-Purpose Input/Output | IO | E12 |
| gpio5_7 | General-Purpose Input/Output | IO | F13 |
| gpio5_8 | General-Purpose Input/Output | IO | C12 |
| gpio5_9 | General-Purpose Input/Output | IO | D12 |
| gpio5_10 | General-Purpose Input/Output | IO | B12 |
| gpio5_11 | General-Purpose Input/Output | IO | A11 |
| gpio5_12 | General-Purpose Input/Output | IO | B13 |
| gpio5_13 | General-Purpose Input/Output | IO | B18 |
| gpio5_14 | General-Purpose Input/Output | IO | F15 |
| gpio5_15 | General-Purpose Input/Output | IO | V1 |
| gpio5_16 | General-Purpose Input/Output | IO | U4 |
| gpio5_17 | General-Purpose Input/Output | IO | U3 |
| gpio5_18 | General-Purpose Input/Output | IO | V2 |
| gpio5_19 | General-Purpose Input/Output | IO | Y1 |
| gpio5_20 | General-Purpose Input/Output | IO | W9 |
| gpio5_21 | General-Purpose Input/Output | IO | V9 |
| gpio5_22 | General-Purpose Input/Output | IO | V7 |
| gpio5_23 | General-Purpose Input/Output | IO | U7 |
| gpio5_24 | General-Purpose Input/Output | IO | V6 |
| gpio5_25 | General-Purpose Input/Output | IO | U6 |
| gpio5_26 | General-Purpose Input/Output | IO | U5 |
| gpio5_27 | General-Purpose Input/Output | IO | V5 |
| gpio5_28 | General-Purpose Input/Output | IO | V4 |
| gpio5_29 | General-Purpose Input/Output | IO | V3 |
| gpio5_30 | General-Purpose Input/Output | IO | Y2 |
| gpio5_31 | General-Purpose Input/Output | IO | W2 |
| **GPIO 6** | | | |
| gpio6_4 | General-Purpose Input/Output | IO | A13 |
| gpio6_5 | General-Purpose Input/Output | IO | G14 |
| gpio6_6 | General-Purpose Input/Output | IO | F14 |
| gpio6_7 | General-Purpose Input/Output | IO | B16 |
| gpio6_8 | General-Purpose Input/Output | IO | C15 |
| gpio6_9 | General-Purpose Input/Output | IO | A16 |
| gpio6_10 | General-Purpose Input/Output | IO | AC5 |
| gpio6_11 | General-Purpose Input/Output | IO | AB4 |


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**Table 4-23. GPIOs Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| gpio6_12 | General-Purpose Input/Output | IO | AB10 |
| gpio6_13 | General-Purpose Input/Output | IO | AC10 |
| gpio6_14 | General-Purpose Input/Output | IO | E21 |
| gpio6_15 | General-Purpose Input/Output | IO | F20 |
| gpio6_16 | General-Purpose Input/Output | IO | F21 |
| gpio6_17 | General-Purpose Input/Output | IO | D18 |
| gpio6_18 | General-Purpose Input/Output | IO | E17 |
| gpio6_19 | General-Purpose Input/Output | IO | B26 |
| gpio6_20 | General-Purpose Input/Output | IO | C23 |
| gpio6_21 | General-Purpose Input/Output | IO | W6 |
| gpio6_22 | General-Purpose Input/Output | IO | Y6 |
| gpio6_23 | General-Purpose Input/Output | IO | AA6 |
| gpio6_24 | General-Purpose Input/Output | IO | Y4 |
| gpio6_25 | General-Purpose Input/Output | IO | AA5 |
| gpio6_26 | General-Purpose Input/Output | IO | Y3 |
| gpio6_27 | General-Purpose Input/Output | IO | W7 |
| gpio6_28 | General-Purpose Input/Output | IO | Y9 |
| gpio6_29 | General-Purpose Input/Output | IO | AD4 |
| gpio6_30 | General-Purpose Input/Output | IO | AC4 |
| gpio6_31 | General-Purpose Input/Output | IO | AC7 |
| **GPIO 7** | | | |
| gpio7_0 | General-Purpose Input/Output | IO | AC6 |
| gpio7_1 | General-Purpose Input/Output | IO | AC9 |
| gpio7_2 | General-Purpose Input/Output | IO | AC3 |
| gpio7_3 | General-Purpose Input/Output | IO | R6 |
| gpio7_4 | General-Purpose Input/Output | IO | T9 |
| gpio7_5 | General-Purpose Input/Output | IO | T6 |
| gpio7_6 | General-Purpose Input/Output | IO | T7 |
| gpio7_7 | General-Purpose Input/Output | IO | A25 |
| gpio7_8 | General-Purpose Input/Output | IO | F16 |
| gpio7_9 | General-Purpose Input/Output | IO | B25 |
| gpio7_10 | General-Purpose Input/Output | IO | A24 |
| gpio7_11 | General-Purpose Input/Output | IO | A22 |
| gpio7_12 | General-Purpose Input/Output | IO | B21 |
| gpio7_13 | General-Purpose Input/Output | IO | B20 |
| gpio7_14 | General-Purpose Input/Output | IO | A26 |
| gpio7_15 | General-Purpose Input/Output | IO | B22 |
| gpio7_16 | General-Purpose Input/Output | IO | G17 |
| gpio7_17 | General-Purpose Input/Output | IO | B24 |
| gpio7_18 | General-Purpose Input/Output | IO | L1 |
| gpio7_19 | General-Purpose Input/Output | IO | K2 |
| gpio7_22 | General-Purpose Input/Output | IO | B27 |
| gpio7_23 | General-Purpose Input/Output | IO | C26 |
| gpio7_24 | General-Purpose Input/Output | IO | E25 |
| gpio7_25 | General-Purpose Input/Output | IO | C27 |
| gpio7_26 | General-Purpose Input/Output | IO | D28 |
| gpio7_27 | General-Purpose Input/Output | IO | D26 |

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**Table 4-23. GPIOs Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| gpio7_28 | General-Purpose Input/Output | IO | J1 |
| gpio7_29 | General-Purpose Input/Output | IO | J2 |
| gpio7_30 | General-Purpose Input/Output | IO | D14 |
| gpio7_31 | General-Purpose Input/Output | IO | C14 |
| **GPIO 8** | | | |
| gpio8_0 | General-Purpose Input/Output | IO | F11 |
| gpio8_1 | General-Purpose Input/Output | IO | G10 |
| gpio8_2 | General-Purpose Input/Output | IO | F10 |
| gpio8_3 | General-Purpose Input/Output | IO | G11 |
| gpio8_4 | General-Purpose Input/Output | IO | E9 |
| gpio8_5 | General-Purpose Input/Output | IO | F9 |
| gpio8_6 | General-Purpose Input/Output | IO | F8 |
| gpio8_7 | General-Purpose Input/Output | IO | E7 |
| gpio8_8 | General-Purpose Input/Output | IO | E8 |
| gpio8_9 | General-Purpose Input/Output | IO | D9 |
| gpio8_10 | General-Purpose Input/Output | IO | D7 |
| gpio8_11 | General-Purpose Input/Output | IO | D8 |
| gpio8_12 | General-Purpose Input/Output | IO | A5 |
| gpio8_13 | General-Purpose Input/Output | IO | C6 |
| gpio8_14 | General-Purpose Input/Output | IO | C8 |
| gpio8_15 | General-Purpose Input/Output | IO | C7 |
| gpio8_16 | General-Purpose Input/Output | IO | B7 |
| gpio8_17 | General-Purpose Input/Output | IO | B8 |
| gpio8_18 | General-Purpose Input/Output | IO | A7 |
| gpio8_19 | General-Purpose Input/Output | IO | A8 |
| gpio8_20 | General-Purpose Input/Output | IO | C9 |
| gpio8_21 | General-Purpose Input/Output | IO | A9 |
| gpio8_22 | General-Purpose Input/Output | IO | B9 |
| gpio8_23 | General-Purpose Input/Output | IO | A10 |
| gpio8_27 | General-Purpose Input | I | D23 |
| gpio8_28 | General-Purpose Input/Output | IO | F19 |
| gpio8_29 | General-Purpose Input/Output | IO | E18 |
| gpio8_30(1) | General-Purpose Input/Output | IO | G21 |
| gpio8_31(1) | General-Purpose Input/Output | IO | D24 |

(1) gpio8_30 is multiplexed with EMU0 and gpio8_31 is multiplexed with EMU1. These pins will be sampled at reset release by the test and emulation logic. Therefore, if they are used as GPIO pins, they must return to the high state whenever the device enters reset. This can be controlled by logic driven from rstoutn. After the device exits reset (indicated by rstoutn rising), these can return to GPIO mode.

### 4.4.21 Keyboard controller (KBD)

**NOTE**

For more information, see Keyboard Controller section of the device TRM.

**Table 4-24. Keyboard Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| kbd_row0 | Keypad row 0 | I | AD9/ E1 |
| kbd_row1 | Keypad row 1 | I | AF9/ G2 |


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**Table 4-24. Keyboard Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| kbd_row2 | Keypad row 2 | I | AG4/ G1 |
| kbd_row3 | Keypad row 3 | I | AG2/ G6 |
| kbd_row4 | Keypad row 4 | I | AG3/ F2 |
| kbd_row5 | Keypad row 5 | I | AG5/ F3 |
| kbd_row6 | Keypad row 6 | I | AF2/ D1 |
| kbd_row7 | Keypad row 7 | I | AF6/ F6 |
| kbd_row8 | Keypad row 8 | I | AF3/ C2 |
| kbd_col0 | Keypad column 0 | O | AF4/ E2 |
| kbd_col1 | Keypad column 1 | O | AF1/ D2 |
| kbd_col2 | Keypad column 2 | O | AE3/ F4 |
| kbd_col3 | Keypad column 3 | O | AE5/ C1 |
| kbd_col4 | Keypad column 4 | O | AE1/ E4 |
| kbd_col5 | Keypad column 5 | O | AE2/ F5 |
| kbd_col6 | Keypad column 6 | O | AE6/ E6 |
| kbd_col7 | Keypad column 7 | O | AD2/ D3 |
| kbd_col8 | Keypad column 8 | O | AD3/ D5 |

### *4.4.22 Pulse Width Modulation (PWM)*

**NOTE**

For more information, see the Pulse-Width Modulation (PWM) subsystem section of the device TRM.

**Table 4-25. PWM Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **PWMSS1** | | | |
| eQEP1A_in | EQEP1 Quadrature Input A | I | E1/ AD9 |
| eQEP1B_in | EQEP1 Quadrature Input B | I | G2/ AF9 |
| eQEP1_index | EQEP1 Index Input | IO | AE9/ H7 |
| eQEP1_strobe | EQEP1 Strobe Input | IO | G1/ AF8 |
| ehrpwm1A | EHRPWM1 Output A | O | AE8/ G6 |
| ehrpwm1B | EHRPWM1 Output B | O | AD8/ F2 |
| ehrpwm1_tripzone_input | EHRPWM1 Trip Zone Input | IO | AG7/ F3 |
| eCAP1_in_PWM1_out | ECAP1 Capture Input / PWM Output | IO | AH6/ D1 |
| ehrpwm1_synci | EHRPWM1 Sync Input | I | AH3/ E2 |
| ehrpwm1_synco | EHRPWM1 Sync Output | O | AH5/ D2 |
| **PWMSS2** | | | |
| eQEP2A_in | EQEP2 Quadrature Input A | I | AG6/ F4 |
| eQEP2B_in | EQEP2 Quadrature Input B | I | AH4/ C1 |
| eQEP2_index | EQEP2 Index Input | IO | AG4/ E4 |
| eQEP2_strobe | EQEP2 Strobe Input | IO | AG2/ F5 |
| ehrpwm2A | EHRPWM2 Output A | O | AC5/ E6 |
| ehrpwm2B | EHRPWM2 Output B | O | AB4/ D3 |
| ehrpwm2_tripzone_input | EHRPWM2 Trip Zone Input | IO | AD4/ F6 |
| eCAP2_in_PWM2_out | ECAP2 Capture Input / PWM Output | IO | AC4/ D5 |

**Table 4-25. PWM Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| **PWMSS3** | | | |
| eQEP3A_in | EQEP3 Quadrature Input A | I | AC7/ C2 |
| eQEP3B_in | EQEP3 Quadrature Input B | I | AC6/ C3 |
| eQEP3_index | EQEP3 Index Input | IO | AC9/ C4 |
| eQEP3_strobe | EQEP3 Strobe Input | IO | AC3/ B2 |
| ehrpwm3A | EHRPWM3 Output A | O | AC8/ D6 |
| ehrpwm3B | EHRPWM3 Output B | O | AD6/ C5 |
| ehrpwm3_tripzone_input | EHRPWM3 Trip Zone Input | IO | AB8/ A3 |
| eCAP3_in_PWM3_out | ECAP3 Capture Input / PWM Output | IO | AB5/ B3 |

### *4.4.23 Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)*

**CAUTION**

The I/O timings provided in Section 7, *Timing Requirements and Switching Characteristics* are valid only if signals within a single IOSET are used. The IOSETs are defined in the Table 7-154 and Table 7-155.

**NOTE**

For more information see the Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem section of the device TRM.

**Table 4-26. PRU-ICSS Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL BOTTOM |
|---|---|---|---|
| **PRU-ICSS 1** | | | |
| pr1_pru0_gpo0 | PRU0 General-Purpose Output | O | AH6 |
| pr1_pru0_gpo1 | PRU0 General-Purpose Output | O | AH3 |
| pr1_pru0_gpo2 | PRU0 General-Purpose Output | O | AH5 |
| pr1_pru0_gpo3 | PRU0 General-Purpose Output | O | AG6 |
| pr1_pru0_gpo4 | PRU0 General-Purpose Output | O | AH4 |
| pr1_pru0_gpo5 | PRU0 General-Purpose Output | O | AG4 |
| pr1_pru0_gpo6 | PRU0 General-Purpose Output | O | AG2 |
| pr1_pru0_gpo7 | PRU0 General-Purpose Output | O | AG3 |
| pr1_pru0_gpo8 | PRU0 General-Purpose Output | O | AG5 |
| pr1_pru0_gpo9 | PRU0 General-Purpose Output | O | AF2 |
| pr1_pru0_gpo10 | PRU0 General-Purpose Output | O | AF6 |
| pr1_pru0_gpo11 | PRU0 General-Purpose Output | O | AF3 |
| pr1_pru0_gpo12 | PRU0 General-Purpose Output | O | AF4 |
| pr1_pru0_gpo13 | PRU0 General-Purpose Output | O | AF1 |
| pr1_pru0_gpo14 | PRU0 General-Purpose Output | O | AE3 |
| pr1_pru0_gpo15 | PRU0 General-Purpose Output | O | AE5 |
| pr1_pru0_gpo16 | PRU0 General-Purpose Output | O | AE1 |
| pr1_pru0_gpo17 | PRU0 General-Purpose Output | O | AE2 |


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**Table 4-26. PRU-ICSS Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL BOTTOM |
|---|---|---|---|
| pr1_pru0_gpo18 | PRU0 General-Purpose Output | O | AE6 |
| pr1_pru0_gpo19 | PRU0 General-Purpose Output | O | AD2 |
| pr1_pru0_gpo20 | PRU0 General-Purpose Output | O | AD3 |
| pr1_pru0_gpi0 | PRU0 General-Purpose Input | I | AH6 |
| pr1_pru0_gpi1 | PRU0 General-Purpose Input | I | AH3 |
| pr1_pru0_gpi2 | PRU0 General-Purpose Input | I | AH5 |
| pr1_pru0_gpi3 | PRU0 General-Purpose Input | I | AG6 |
| pr1_pru0_gpi4 | PRU0 General-Purpose Input | I | AH4 |
| pr1_pru0_gpi5 | PRU0 General-Purpose Input | I | AG4 |
| pr1_pru0_gpi6 | PRU0 General-Purpose Input | I | AG2 |
| pr1_pru0_gpi7 | PRU0 General-Purpose Input | I | AG3 |
| pr1_pru0_gpi8 | PRU0 General-Purpose Input | I | AG5 |
| pr1_pru0_gpi9 | PRU0 General-Purpose Input | I | AF2 |
| pr1_pru0_gpi10 | PRU0 General-Purpose Input | I | AF6 |
| pr1_pru0_gpi11 | PRU0 General-Purpose Input | I | AF3 |
| pr1_pru0_gpi12 | PRU0 General-Purpose Input | I | AF4 |
| pr1_pru0_gpi13 | PRU0 General-Purpose Input | I | AF1 |
| pr1_pru0_gpi14 | PRU0 General-Purpose Input | I | AE3 |
| pr1_pru0_gpi15 | PRU0 General-Purpose Input | I | AE5 |
| pr1_pru0_gpi16 | PRU0 General-Purpose Input | I | AE1 |
| pr1_pru0_gpi17 | PRU0 General-Purpose Input | I | AE2 |
| pr1_pru0_gpi18 | PRU0 General-Purpose Input | I | AE6 |
| pr1_pru0_gpi19 | PRU0 General-Purpose Input | I | AD2 |
| pr1_pru0_gpi20 | PRU0 General-Purpose Input | I | AD3 |
| pr1_pru1_gpo0 | PRU1 General-Purpose Output | O | E2 |
| pr1_pru1_gpo1 | PRU1 General-Purpose Output | O | D2 |
| pr1_pru1_gpo2 | PRU1 General-Purpose Output | O | F4 |
| pr1_pru1_gpo3 | PRU1 General-Purpose Output | O | C1 |
| pr1_pru1_gpo4 | PRU1 General-Purpose Output | O | E4 |
| pr1_pru1_gpo5 | PRU1 General-Purpose Output | O | F5 |
| pr1_pru1_gpo6 | PRU1 General-Purpose Output | O | E6 |
| pr1_pru1_gpo7 | PRU1 General-Purpose Output | O | D3 |
| pr1_pru1_gpo8 | PRU1 General-Purpose Output | O | F6 |
| pr1_pru1_gpo9 | PRU1 General-Purpose Output | O | D5 |
| pr1_pru1_gpo10 | PRU1 General-Purpose Output | O | C2 |
| pr1_pru1_gpo11 | PRU1 General-Purpose Output | O | C3 |
| pr1_pru1_gpo12 | PRU1 General-Purpose Output | O | C4 |
| pr1_pru1_gpo13 | PRU1 General-Purpose Output | O | B2 |
| pr1_pru1_gpo14 | PRU1 General-Purpose Output | O | D6 |
| pr1_pru1_gpo15 | PRU1 General-Purpose Output | O | C5 |
| pr1_pru1_gpo16 | PRU1 General-Purpose Output | O | A3 |
| pr1_pru1_gpo17 | PRU1 General-Purpose Output | O | B3 |
| pr1_pru1_gpo18 | PRU1 General-Purpose Output | O | B4 |
| pr1_pru1_gpo19 | PRU1 General-Purpose Output | O | B5 |
| pr1_pru1_gpo20 | PRU1 General-Purpose Output | O | A4 |
| pr1_pru1_gpi0 | PRU1 General-Purpose Input | I | E2 |
| pr1_pru1_gpi1 | PRU1 General-Purpose Input | I | D2 |

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**Table 4-26. PRU-ICSS Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL BOTTOM |
|---|---|---|---|
| pr1_pru1_gpi2 | PRU1 General-Purpose Input | I | F4 |
| pr1_pru1_gpi3 | PRU1 General-Purpose Input | I | C1 |
| pr1_pru1_gpi4 | PRU1 General-Purpose Input | I | E4 |
| pr1_pru1_gpi5 | PRU1 General-Purpose Input | I | F5 |
| pr1_pru1_gpi6 | PRU1 General-Purpose Input | I | E6 |
| pr1_pru1_gpi7 | PRU1 General-Purpose Input | I | D3 |
| pr1_pru1_gpi8 | PRU1 General-Purpose Input | I | F6 |
| pr1_pru1_gpi9 | PRU1 General-Purpose Input | I | D5 |
| pr1_pru1_gpi10 | PRU1 General-Purpose Input | I | C2 |
| pr1_pru1_gpi11 | PRU1 General-Purpose Input | I | C3 |
| pr1_pru1_gpi12 | PRU1 General-Purpose Input | I | C4 |
| pr1_pru1_gpi13 | PRU1 General-Purpose Input | I | B2 |
| pr1_pru1_gpi14 | PRU1 General-Purpose Input | I | D6 |
| pr1_pru1_gpi15 | PRU1 General-Purpose Input | I | C5 |
| pr1_pru1_gpi16 | PRU1 General-Purpose Input | I | A3 |
| pr1_pru1_gpi17 | PRU1 General-Purpose Input | I | B3 |
| pr1_pru1_gpi18 | PRU1 General-Purpose Input | I | B4 |
| pr1_pru1_gpi19 | PRU1 General-Purpose Input | I | B5 |
| pr1_pru1_gpi20 | PRU1 General-Purpose Input | I | A4 |
| pr1_mii_mt0_clk | MII0 Transmit Clock | I | U5 |
| pr1_mii0_txen | MII0 Transmit Enable | O | V3 |
| pr1_mii0_txd3 | MII0 Transmit Data | O | V5 |
| pr1_mii0_txd2 | MII0 Transmit Data | O | V4 |
| pr1_mii0_txd1 | MII0 Transmit Data | O | Y2 |
| pr1_mii0_txd0 | MII0 Transmit Data | O | W2 |
| pr1_mii0_rxdv | MII0 Data Valid | I | V2 |
| pr1_mii_mr0_clk | MII0 Receive Clock | I | Y1 |
| pr1_mii0_rxd3 | MII0 Receive Data | I | W9 |
| pr1_mii0_rxd2 | MII0 Receive Data | I | V9 |
| pr1_mii0_crs | MII0 Carrier Sense | I | V7 |
| pr1_mii0_rxer | MII0 Receive Error | I | U7 |
| pr1_mii0_rxd1 | MII0 Receive Data | I | V6 |
| pr1_mii0_rxd0 | MII0 Receive Data | I | U6 |
| pr1_mii0_col | MII0 Collision Detect | I | V1 |
| pr1_mii0_rxlink | MII0 Receive Link | I | U4 |
| pr1_mii_mt1_clk | MII1 Transmit Clock | I | C1 |
| pr1_mii1_txen | MII1 Transmit Enable | O | E4 |
| pr1_mii1_txd3 | MII1 Transmit Data | O | F5 |
| pr1_mii1_txd2 | MII1 Transmit Data | O | E6 |
| pr1_mii1_txd1 | MII1 Transmit Data | O | D5 |
| pr1_mii1_txd0 | MII1 Transmit Data | O | C2 |
| pr1_mii_mr1_clk | MII1 Receive Clock | I | C3 |
| pr1_mii1_rxdv | MII1 Data Valid | I | C4 |
| pr1_mii1_rxd3 | MII1 Receive Data | I | B2 |
| pr1_mii1_rxd2 | MII1 Receive Data | I | D6 |
| pr1_mii1_rxd1 | MII1 Receive Data | I | C5 |
| pr1_mii1_rxd0 | MII1 Receive Data | I | A3 |


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**Table 4-26. PRU-ICSS Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL BOTTOM |
|---|---|---|---|
| pr1_mii1_rxer | MII1 Receive Error | I | B3 |
| pr1_mii1_rxlink | MII1 Receive Link | I | B4 |
| pr1_mii1_col | MII1 Collision Detect | I | B5 |
| pr1_mii1_crs | MII1 Carrier Sense | I | A4 |
| pr1_mdio_mdclk | MDIO Clock | O | D3 |
| pr1_mdio_data | MDIO Data | IO | F6 |
| pr1_edc_latch0_in | Latch Input 0 | I | AG3/ E2 |
| pr1_edc_latch1_in | Latch Input 1 | I | AG5 |
| pr1_edc_sync0_out | SYNC 0 Output | O | AF2/ D2 |
| pr1_edc_sync1_out | SYNC 1 Output | O | AF6 |
| pr1_edio_latch_in | Latch Input | I | AF3 |
| pr1_edio_sof | Start Of Frame | O | AF4/ F4 |
| pr1_edio_data_in0 | Ethernet Digital Input | I | AF1/ E1 |
| pr1_edio_data_in1 | Ethernet Digital Input | I | AE3/ G2 |
| pr1_edio_data_in2 | Ethernet Digital Input | I | AE5/ H7 |
| pr1_edio_data_in3 | Ethernet Digital Input | I | AE1/ G1 |
| pr1_edio_data_in4 | Ethernet Digital Input | I | AE2/ G6 |
| pr1_edio_data_in5 | Ethernet Digital Input | I | AE6/ F2 |
| pr1_edio_data_in6 | Ethernet Digital Input | I | AD2/ F3 |
| pr1_edio_data_in7 | Ethernet Digital Input | I | AD3/ D1 |
| pr1_edio_data_out0 | Ethernet Digital Output | O | AF1/ E1 |
| pr1_edio_data_out1 | Ethernet Digital Output | O | AE3/ G2 |
| pr1_edio_data_out2 | Ethernet Digital Output | O | AE5/ H7 |
| pr1_edio_data_out3 | Ethernet Digital Output | O | AE1/ G1 |
| pr1_edio_data_out4 | Ethernet Digital Output | O | AE2/ G6 |
| pr1_edio_data_out5 | Ethernet Digital Output | O | AE6/ F2 |
| pr1_edio_data_out6 | Ethernet Digital Output | O | AD2/ F3 |
| pr1_edio_data_out7 | Ethernet Digital Output | O | AD3/ D1 |
| pr1_uart0_cts_n | UART Clear-To-Send | I | G1/ F11 |
| pr1_uart0_rts_n | UART Ready-To-Send | O | G6/ G10 |
| pr1_uart0_rxd | UART Receive Data | I | F2/ F10 |
| pr1_uart0_txd | UART Transmit Data | O | F3/ G11 |
| pr1_ecap0_ecap_capin_apwm_o | Capture Input / PWM output | IO | D1/ E9 |
| **PRU-ICSS 2** | | | |
| pr2_pru0_gpo0 | PRU0 General-Purpose Output | O | G11/ AC5 |
| pr2_pru0_gpo1 | PRU0 General-Purpose Output | O | E9/ AB4 |
| pr2_pru0_gpo2 | PRU0 General-Purpose Output | O | F9/ AD4 |
| pr2_pru0_gpo3 | PRU0 General-Purpose Output | O | F8/ AC4 |
| pr2_pru0_gpo4 | PRU0 General-Purpose Output | O | E7/ AC7 |
| pr2_pru0_gpo5 | PRU0 General-Purpose Output | O | E8/ AC6 |
| pr2_pru0_gpo6 | PRU0 General-Purpose Output | O | D9/ AC9 |
| pr2_pru0_gpo7 | PRU0 General-Purpose Output | O | D7/ AC3 |
| pr2_pru0_gpo8 | PRU0 General-Purpose Output | O | D8/ AC8 |
| pr2_pru0_gpo9 | PRU0 General-Purpose Output | O | A5/ AD6 |
| pr2_pru0_gpo10 | PRU0 General-Purpose Output | O | C6/ AB8 |
| pr2_pru0_gpo11 | PRU0 General-Purpose Output | O | C8/ AB5 |
| pr2_pru0_gpo12 | PRU0 General-Purpose Output | O | C7/ B18 |

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**Table 4-26. PRU-ICSS Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL BOTTOM |
|---|---|---|---|
| pr2_pru0_gpo13 | PRU0 General-Purpose Output | O | B7/ F15 |
| pr2_pru0_gpo14 | PRU0 General-Purpose Output | O | B8/ B19 |
| pr2_pru0_gpo15 | PRU0 General-Purpose Output | O | A7/ C17 |
| pr2_pru0_gpo16 | PRU0 General-Purpose Output | O | A8/ C15 |
| pr2_pru0_gpo17 | PRU0 General-Purpose Output | O | C9/ A16 |
| pr2_pru0_gpo18 | PRU0 General-Purpose Output | O | A9/ A19 |
| pr2_pru0_gpo19 | PRU0 General-Purpose Output | O | B9/ A18 |
| pr2_pru0_gpo20 | PRU0 General-Purpose Output | O | A10/ F14 |
| pr2_pru0_gpi0 | PRU0 General-Purpose Input | I | G11/ AC5 |
| pr2_pru0_gpi1 | PRU0 General-Purpose Input | I | E9/ AB4 |
| pr2_pru0_gpi2 | PRU0 General-Purpose Input | I | F9/ AD4 |
| pr2_pru0_gpi3 | PRU0 General-Purpose Input | I | F8/ AC4 |
| pr2_pru0_gpi4 | PRU0 General-Purpose Input | I | E7/ AC7 |
| pr2_pru0_gpi5 | PRU0 General-Purpose Input | I | E8/ AC6 |
| pr2_pru0_gpi6 | PRU0 General-Purpose Input | I | D9/ AC9 |
| pr2_pru0_gpi7 | PRU0 General-Purpose Input | I | D7/ AC3 |
| pr2_pru0_gpi8 | PRU0 General-Purpose Input | I | D8/ AC8 |
| pr2_pru0_gpi9 | PRU0 General-Purpose Input | I | A5/ AD6 |
| pr2_pru0_gpi10 | PRU0 General-Purpose Input | I | C6/ AB8 |
| pr2_pru0_gpi11 | PRU0 General-Purpose Input | I | C8/ AB5 |
| pr2_pru0_gpi12 | PRU0 General-Purpose Input | I | C7/ B18 |
| pr2_pru0_gpi13 | PRU0 General-Purpose Input | I | B7/ F15 |
| pr2_pru0_gpi14 | PRU0 General-Purpose Input | I | B8/ B19 |
| pr2_pru0_gpi15 | PRU0 General-Purpose Input | I | A7/ C17 |
| pr2_pru0_gpi16 | PRU0 General-Purpose Input | I | A8/ C15 |
| pr2_pru0_gpi17 | PRU0 General-Purpose Input | I | C9/ A16 |
| pr2_pru0_gpi18 | PRU0 General-Purpose Input | I | A9/ A19 |
| pr2_pru0_gpi19 | PRU0 General-Purpose Input | I | B9/ A18 |
| pr2_pru0_gpi20 | PRU0 General-Purpose Input | I | A10/ F14 |
| pr2_pru1_gpo0 | PRU1 General-Purpose Output | O | V1/ D17 |
| pr2_pru1_gpo1 | PRU1 General-Purpose Output | O | U4/ AA3 |
| pr2_pru1_gpo2 | PRU1 General-Purpose Output | O | U3/ AB9 |
| pr2_pru1_gpo3 | PRU1 General-Purpose Output | O | V2/ AB3 |
| pr2_pru1_gpo4 | PRU1 General-Purpose Output | O | Y1/ AA4 |
| pr2_pru1_gpo5 | PRU1 General-Purpose Output | O | W9/ D18 |
| pr2_pru1_gpo6 | PRU1 General-Purpose Output | O | V9/ E17 |
| pr2_pru1_gpo7 | PRU1 General-Purpose Output | O | V7/ C14 |
| pr2_pru1_gpo8 | PRU1 General-Purpose Output | O | U7/ G12 |
| pr2_pru1_gpo9 | PRU1 General-Purpose Output | O | V6/ F12 |
| pr2_pru1_gpo10 | PRU1 General-Purpose Output | O | U6/ B12 |
| pr2_pru1_gpo11 | PRU1 General-Purpose Output | O | U5/ A11 |
| pr2_pru1_gpo12 | PRU1 General-Purpose Output | O | V5/ B13 |
| pr2_pru1_gpo13 | PRU1 General-Purpose Output | O | V4/ A12 |
| pr2_pru1_gpo14 | PRU1 General-Purpose Output | O | V3/ E14 |
| pr2_pru1_gpo15 | PRU1 General-Purpose Output | O | Y2/ A13 |
| pr2_pru1_gpo16 | PRU1 General-Purpose Output | O | W2/ G14 |
| pr2_pru1_gpo17 | PRU1 General-Purpose Output | O | E11 |


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**Table 4-26. PRU-ICSS Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL BOTTOM |
|---|---|---|---|
| pr2_pru1_gpo18 | PRU1 General-Purpose Output | O | F11 |
| pr2_pru1_gpo19 | PRU1 General-Purpose Output | O | G10 |
| pr2_pru1_gpo20 | PRU1 General-Purpose Output | O | F10 |
| pr2_pru1_gpi0 | PRU1 General-Purpose Input | I | V1/ D17 |
| pr2_pru1_gpi1 | PRU1 General-Purpose Input | I | U4/ AA3 |
| pr2_pru1_gpi2 | PRU1 General-Purpose Input | I | U3/ AB9 |
| pr2_pru1_gpi3 | PRU1 General-Purpose Input | I | V2/ AB3 |
| pr2_pru1_gpi4 | PRU1 General-Purpose Input | I | Y1/ AA4 |
| pr2_pru1_gpi5 | PRU1 General-Purpose Input | I | W9/ D18 |
| pr2_pru1_gpi6 | PRU1 General-Purpose Input | I | V9/ E17 |
| pr2_pru1_gpi7 | PRU1 General-Purpose Input | I | V7 / C14 |
| pr2_pru1_gpi8 | PRU1 General-Purpose Input | I | U7 / G12 |
| pr2_pru1_gpi9 | PRU1 General-Purpose Input | I | V6 / F12 |
| pr2_pru1_gpi10 | PRU1 General-Purpose Input | I | U6 / B12 |
| pr2_pru1_gpi11 | PRU1 General-Purpose Input | I | U5 / A11 |
| pr2_pru1_gpi12 | PRU1 General-Purpose Input | I | V5 / B13 |
| pr2_pru1_gpi13 | PRU1 General-Purpose Input | I | V4 / A12 |
| pr2_pru1_gpi14 | PRU1 General-Purpose Input | I | V3 / E14 |
| pr2_pru1_gpi15 | PRU1 General-Purpose Input | I | Y2 / A13 |
| pr2_pru1_gpi16 | PRU1 General-Purpose Input | I | W2 / G14 |
| pr2_pru1_gpi17 | PRU1 General-Purpose Input | I | E11 |
| pr2_pru1_gpi18 | PRU1 General-Purpose Input | I | F11 |
| pr2_pru1_gpi19 | PRU1 General-Purpose Input | I | G10 |
| pr2_pru1_gpi20 | PRU1 General-Purpose Input | I | F10 |
| pr2_edc_latch0_in | Latch Input 0 | I | F9 |
| pr2_edc_latch1_in | Latch Input 1 | I | F8 |
| pr2_edc_sync0_out | SYNC 0 Output | O | E7 |
| pr2_edc_sync1_out | SYNC 1 Output | O | E8 |
| pr2_edio_latch_in | Latch Input | I | D9 |
| pr2_edio_sof | Start Of Frame | O | D7 |
| pr2_uart0_cts_n | UART Clear-To-Send | I | D8 |
| pr2_uart0_rts_n | UART Ready-To-Send | O | A5 |
| pr2_uart0_rxd | UART Receive Data | I | C6 |
| pr2_uart0_txd | UART Transmit Data | O | C8 |
| pr2_ecap0_ecap_capin_apwm_o | Capture Input / PWM output | IO | C7 |
| pr2_edio_data_in0 | Ethernet Digital Input | I | B7 |
| pr2_edio_data_in1 | Ethernet Digital Input | I | B8 |
| pr2_edio_data_in2 | Ethernet Digital Input | I | A7 |
| pr2_edio_data_in3 | Ethernet Digital Input | I | A8 |
| pr2_edio_data_in4 | Ethernet Digital Input | I | C9 |
| pr2_edio_data_in5 | Ethernet Digital Input | I | A9 |
| pr2_edio_data_in6 | Ethernet Digital Input | I | B9 |
| pr2_edio_data_in7 | Ethernet Digital Input | I | A10 |
| pr2_edio_data_out0 | Ethernet Digital Output | O | B7 |
| pr2_edio_data_out1 | Ethernet Digital Output | O | B8 |
| pr2_edio_data_out2 | Ethernet Digital Output | O | A7 |
| pr2_edio_data_out3 | Ethernet Digital Output | O | A8 |

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**Table 4-26. PRU-ICSS Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL BOTTOM |
|---|---|---|---|
| pr2_edio_data_out4 | Ethernet Digital Output | O | C9 |
| pr2_edio_data_out5 | Ethernet Digital Output | O | A9 |
| pr2_edio_data_out6 | Ethernet Digital Output | O | B9 |
| pr2_edio_data_out7 | Ethernet Digital Output | O | A10 |
| pr2_mii1_col | MII1 Collision Detect | I | D18 |
| pr2_mii1_crs | MII1 Carrier Sense | I | E17 |
| pr2_mdio_mdclk | MDIO Clock | O | C14/ AB3 |
| pr2_mdio_data | MDIO Data | IO | D14/ AA4 |
| pr2_mii0_rxer | MII0 Receive Error | I | G12 |
| pr2_mii_mt0_clk | MII0 Transmit Clock | I | F12 |
| pr2_mii0_txen | MII0 Transmit Enable | O | B12 |
| pr2_mii0_txd3 | MII0 Transmit Data | O | A11 |
| pr2_mii0_txd2 | MII0 Transmit Data | O | B13 |
| pr2_mii0_txd1 | MII0 Transmit Data | O | A12 |
| pr2_mii0_txd0 | MII0 Transmit Data | O | E14 |
| pr2_mii_mr0_clk | MII0 Receive Clock | I | A13 |
| pr2_mii0_rxdv | MII0 Data Valid | I | G14 |
| pr2_mii0_rxd3 | MII0 Receive Data | I | F14 |
| pr2_mii0_rxd2 | MII0 Receive Data | I | A19 |
| pr2_mii0_rxd1 | MII0 Receive Data | I | A18 |
| pr2_mii0_rxd0 | MII0 Receive Data | I | C15 |
| pr2_mii0_rxlink | MII0 Receive Link | I | A16 |
| pr2_mii0_crs | MII0 Carrier Sense | I | B18 |
| pr2_mii0_col | MII0 Collision Detect | I | F15 |
| pr2_mii1_rxer | MII1 Receive Error | I | B19 |
| pr2_mii1_rxlink | MII1 Receive Link | I | C17 |
| pr2_mii_mt1_clk | MII1 Transmit Clock | I | AC5 |
| pr2_mii1_txen | MII1 Transmit Enable | O | AB4 |
| pr2_mii1_txd3 | MII1 Transmit Data | O | AD4 |
| pr2_mii1_txd2 | MII1 Transmit Data | O | AC4 |
| pr2_mii1_txd1 | MII1 Transmit Data | O | AC7 |
| pr2_mii1_txd0 | MII1 Transmit Data | O | AC6 |
| pr2_mii_mr1_clk | MII1 Receive Clock | I | AC9 |
| pr2_mii1_rxdv | MII1 Data Valid | I | AC3 |
| pr2_mii1_rxd3 | MII1 Receive Data | I | AC8 |
| pr2_mii1_rxd2 | MII1 Receive Data | I | AD6 |
| pr2_mii1_rxd1 | MII1 Receive Data | I | AB8 |
| pr2_mii1_rxd0 | MII1 Receive Data | I | AB5 |

**NOTE**

PRU-ICSS has internal multiplexing capability of pin functions. See *PRU-ICSS EGPIO Internal Pinmux* in device TRM. Besides, EGPIO module can be configured to export additional functions to EGPIO pins in place of simple GPIO. See *Enhanced General-Purpose Module/Serial Capture Unit* in device TRM.


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### 4.4.24 Test Interfaces

**CAUTION**

The I/O timings provided in Section 7, *Timing Requirements and Switching Characteristics* are valid only if signals within a single IOSET are used. The IOSETs are defined in the Table 7-179.

**NOTE**

For more information, see the On-Chip Debug Support / Debug Ports section of the device TRM.

**Table 4-27. Debug Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| tms | JTAG test port mode select. An external pullup resistor should be used on this ball. | IO | F18 |
| tdi | JTAG test data | I | D23 |
| tdo | JTAG test port data | O | F19 |
| tclk | JTAG test clock | I | E20 |
| trstn | JTAG test reset | I | D20 |
| rtck | JTAG return clock | O | E18 |
| emu0(1) | Emulator pin 0 | IO | G21 |
| emu1(1) | Emulator pin 1 | IO | D24 |
| emu2 | Emulator pin 2 | O | F10 |
| emu3 | Emulator pin 3 | O | D7 |
| emu4 | Emulator pin 4 | O | A7 |
| emu5 | Emulator pin 5 | O | E1/ G11 |
| emu6 | Emulator pin 6 | O | G2/ E9 |
| emu7 | Emulator pin 7 | O | H7/ F9 |
| emu8 | Emulator pin 8 | O | G1/ F8 |
| emu9 | Emulator pin 9 | O | G6/ E7 |
| emu10 | Emulator pin 10 | O | F2/ D8 |
| emu11 | Emulator pin 11 | O | F3/ A5 |
| emu12 | Emulator pin 12 | O | D1/ C6 |
| emu13 | Emulator pin 13 | O | E2/ C8 |
| emu14 | Emulator pin 14 | O | D2/ C7 |
| emu15 | Emulator pin 15 | O | F4/ A8 |
| emu16 | Emulator pin 16 | O | C1/ C9 |
| emu17 | Emulator pin 17 | O | E4/ A9 |
| emu18 | Emulator pin 18 | O | F5/ B9 |
| emu19 | Emulator pin 19 | O | E6/ A10 |

(1) EMU0 and EMU1 are multiplexed with GPIO. These pins will be sampled at reset release by the test and emulation logic. Therefore, if they are used as GPIO pins, they must return to the high state whenever the device enters reset. This can be controlled by logic driven from rstoutn. After the device exits reset (indicated by rstoutn rising), these can return to GPIO mode.

### 4.4.25 System and Miscellaneous

#### 4.4.25.1 Sysboot

**NOTE**
For more information, see the Initialization (ROM Code) section of the device TRM.

**Table 4-28. Sysboot Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| sysboot0 | Boot Mode Configuration 0. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | M6 |
| sysboot1 | Boot Mode Configuration 1. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | M2 |
| sysboot2 | Boot Mode Configuration 2. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | L5 |
| sysboot3 | Boot Mode Configuration 3. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | M1 |
| sysboot4 | Boot Mode Configuration 4. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | L6 |
| sysboot5 | Boot Mode Configuration 5. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | L4 |
| sysboot6 | Boot Mode Configuration 6. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | L3 |
| sysboot7 | Boot Mode Configuration 7. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | L2 |
| sysboot8 | Boot Mode Configuration 8. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | L1 |
| sysboot9 | Boot Mode Configuration 9. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | K2 |
| sysboot10 | Boot Mode Configuration 10. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | J1 |
| sysboot11 | Boot Mode Configuration 11. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | J2 |
| sysboot12 | Boot Mode Configuration 12. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | H1 |
| sysboot13 | Boot Mode Configuration 13. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | J3 |
| sysboot14 | Boot Mode Configuration 14. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | H2 |
| sysboot15 | Boot Mode Configuration 15. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device. | I | H3 |

#### 4.4.25.2 Power, Reset and Clock Management (PRCM)

**NOTE**
For more information, see PRCM section of the device TRM.

**Table 4-29. PRCM Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| clkout1 | Device Clock output 1. Can be used externally for devices with non-critical timing requirements, or for debug, or as a reference clock on GPMC as described in Table 7-26 *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Default* and Table 7-28 *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate*. | O | F21/ P7 |


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**Table 4-29. PRCM Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| clkout2 | Device Clock output 2. Can be used externally for devices with noncritical timing requirements, or for debug. | O | D18/ N1 |
| clkout3 | Device Clock output 3. Can be used externally for devices with noncritical timing requirements, or for debug. | O | C23 |
| rstoutn | Reset out (Active low). This pin asserts low in response to any global reset condition on the device. (2) | O | F23 |
| resetn | Device Reset Input | I | E23 |
| porz | Power on Reset (active low). This pin must be asserted low until all device supplies are valid (see reset sequence/requirements) | I | F22 |
| xref_clk0 | External Reference Clock 0. For Audio and other Peripherals. | I | D18 |
| xref_clk1 | External Reference Clock 1. For Audio and other Peripherals. | I | E17 |
| xref_clk2 | External Reference Clock 2. For Audio and other Peripherals. | I | B26 |
| xref_clk3 | External Reference Clock 3. For Audio and other Peripherals. | I | C23 |
| xi_osc0 | System Oscillator OSC0 Crystal input / LVCMOS clock input. Functions as the input connection to a crystal when the internal oscillator OSC0 is used. Functions as an LVCMOS-compatible input clock when an external oscillator is used. | I | AE15 |
| xo_osc0 | System Oscillator OSC0 Crystal output | O | AD15 |
| xi_osc1 | Auxiliary Oscillator OSC1 Crystal input / LVCMOS clock input.Functions as the input connection to a crystal when the internal oscillator OSC1 is used. Functions as an LVCMOS-compatible input clock when an external oscillator is used | I | AC15 |
| xo_osc1 | Auxiliary Oscillator OSC1 Crystal output | O | AC13 |
| RMII_MHZ_50_CLK(1) | RMII Reference Clock (50MHz). This pin is an input when external reference is used or output when internal reference is used. | IO | U3 |

(1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between $V_{IH}$ and $V_{IL}$ must be less than $V_{HYS}$.

(2) Note that rstoutn is only valid after vddshv3 is valid. If the rstoutn signal will be used as a reset into other devices attached to the SOC, it must be AND'ed with porz. This will prevent glitches occurring during supply ramping being propagated.

### 4.4.25.3 Real-Time Clock (RTC) Interface

**NOTE**

For more information, see the Real-Time Clock (RTC) chapter of the device TRM.

**NOTE**

RTC only mode is not supported feature.

**Table 4-30. RTC Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| Wakeup0 | RTC External Wakeup Input 0 | I | AD17 |
| Wakeup1 | RTC External Wakeup Input 1 | I | AC17 |
| Wakeup2 | RTC External Wakeup Input 2 | I | AB16 |
| Wakeup3 | RTC External Wakeup Input 3 | I | AC16 |
| rtc_porz | RTC Power Domain Power-On Reset Input | I | AB17 |
| rtc_osc_xi_clkin32 | RTC Oscillator Input. Crystal connection to internal RTC oscillator. Functions as an RTC clock input when an external oscillator is used. | I | AE14 |
| rtc_osc_xo | RTC Oscillator Output | O | AD14 |
| rtc_iso(1) | RTC Domain Isolation Signal | I | AF14 |
| on_off | RTC Power Enable output pin | O | Y11 |

(1) This signal must be kept 0 if device power supplies are not valid during RTC mode and 1 during normal operation. This can typically be achieved by connecting rtc_iso to the same signal driving porz (not rtc_porz) with appropriate voltage level translation if necessary.

#### 4.4.25.4 System Direct Memory Access (SDMA)

**NOTE**
For more information, see the DMA Controllers / System DMA section of the device TRM.

**Table 4-31. System DMA Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| dma_evt1 | System DMA Event Input 1 | I | P7/ P4 |
| dma_evt2 | System DMA Event Input 2 | I | N1/ R3 |
| dma_evt3 | System DMA Event Input 3 | I | N6 |
| dma_evt4 | System DMA Event Input 4 | I | M4 |

#### 4.4.25.5 Interrupt Controllers (INTC)

**NOTE**
For more information, see the Interrupt Controllers chapter of the device TRM.

**Table 4-32. INTC Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| nmin_dsp | Non maskable interrupt input, active-low. This pin can be optionally routed to the DSP NMI input or as generic input to the Arm cores. Note that by default this pin has an internal pulldown resistor enabled. This internal pulldown should be disabled or countered by a stronger external pullup resistor before routing to the DSP or Arm processors. | I | D21 |
| sys_nirq2 | External interrupt event to any device INTC | I | AB16 |
| sys_nirq1 | External interrupt event to any device INTC | I | AC16 |

#### 4.4.25.6 Observability

**NOTE**
For more information, see the Control Module section of the device TRM.

**Table 4-33. Observability Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| obs0 | Observation Output 0 | O | F10 |
| obs1 | Observation Output 1 | O | G11 |
| obs2 | Observation Output 2 | O | E9 |
| obs3 | Observation Output 3 | O | F9 |
| obs4 | Observation Output 4 | O | F8 |
| obs5 | Observation Output 5 | O | D7 |
| obs6 | Observation Output 6 | O | D8 |
| obs7 | Observation Output 7 | O | A5 |
| obs8 | Observation Output 8 | O | C6 |
| obs9 | Observation Output 9 | O | C8 |
| obs10 | Observation Output 10 | O | C7 |
| obs11 | Observation Output 11 | O | A7 |


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**Table 4-33. Observability Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| obs12 | Observation Output 12 | O | A8 |
| obs13 | Observation Output 13 | O | C9 |
| obs14 | Observation Output 14 | O | A9 |
| obs15 | Observation Output 15 | O | B9 |
| obs16 | Observation Output 16 | O | F10 |
| obs17 | Observation Output 17 | O | G11 |
| obs18 | Observation Output 18 | O | E9 |
| obs19 | Observation Output 19 | O | F9 |
| obs20 | Observation Output 20 | O | F8 |
| obs21 | Observation Output 21 | O | D7 |
| obs22 | Observation Output 22 | O | D8 |
| obs23 | Observation Output 23 | O | A5 |
| obs24 | Observation Output 24 | O | C6 |
| obs25 | Observation Output 25 | O | C8 |
| obs26 | Observation Output 26 | O | C7 |
| obs27 | Observation Output 27 | O | A7 |
| obs28 | Observation Output 28 | O | A8 |
| obs29 | Observation Output 29 | O | C9 |
| obs30 | Observation Output 30 | O | A9 |
| obs31 | Observation Output 31 | O | B9 |
| obs_dmarq1 | DMA Request External Observation Output 1 | O | G11 |
| obs_dmarq2 | DMA Request External Observation Output 2 | O | D8 |
| obs_irq1 | IRQ External Observation Output 1 | O | F10 |
| obs_irq2 | IRQ External Observation Output 2 | O | D7 |

### 4.4.25.7 Power Supplies

**NOTE**

For more information, see Power, Reset, and Clock Management / PRCM Subsystem Environment / External Voltage Inputs section of the device TRM.

**Table 4-34. Power Supply Signal Descriptions**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| vdd | Core voltage domain supply | PWR | H13/ H14/ J17/ J18/ L7/ L8/ N10/ N13/ P11/ P12/ P13/ R11/ R16/ R19/ T13/ T16/ T19/ U8/ U9/ U13/ U16/ V8/ V16 |

**Table 4-34. Power Supply Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| vss | Ground | GND | A1/ A2/ A6/ A14/ A23/ A28/ B1/ D13/ D19/ E13/ E19/ F1/ F7/ G7/ G8/ G9/ H12/ J12/ J15/ J28/ K1/ K4/ K5/ K15/ K24/ K25/ L13/ L14/ M19/ N14/ N15/ N19/ N24/ N25/ P28/ R1/ R12/ R13/ R15/ R21/ T10/ T11/ T12/ T14/ T15/ T17/ T18/ T21/ U15/ U17/ U20/ U21/ V15/ V17/ W1/ W15/ W24/ W25/ W28/ AA8/ AA9/ AA10/ AA14/ AA15/ AA20/ AB14/ AB20/ AD1/ AD24/ AG1/ AH1/ AH2/ AH8/ AH20/ AH28 |
| vdd_dspeve | DSP voltage domain supply | PWR | J13/ K10/ K11/ K12/ K13/ L10/ L11/ L12/ M10/ M11/ M12/ M13 |
| vdd_iva | IVA voltage domain supply | PWR | U18/ U19/ V18/ V19 |
| vdd_gpu | GPU voltage domain supply | PWR | U11/ U12/ V10/ V11/ V14/ W10/ W11/ W13 |
| vdd_mpu | MPU voltage domain supply | PWR | K17/ K18/ L15/ L16/ L17/ L18/ L19/ M15/ M16/ M17/ M18/ N17/ N18/ P17/ P18/ R18 |
| vdd_rtc | RTC voltage domain supply | PWR | AB15 |
| vdda_usb1 | DPLL_USB and HS USB1 1.8V analog power supply | PWR | AA13 |
| vssa_usb | HS USB1 and HS USB2 analog ground | GND | AB11/ AA11 |
| vdda_usb2 | HS USB2 1.8V analog power supply | PWR | AB12 |
| vdda33v_usb1 | HS USB1 3.3V analog power supply. If USB1 is not used, this pin can alternatively be connected to VSS if the following requirements are met:<br>- The usb1_dm/usb1_dp pins are left unconnected<br>- The USB1 PHY is kept powered down | PWR | AA12 |
| vdda33v_usb2 | HS USB2 3.3V analog power supply. If USB2 is not used, this pin can alternatively be connected to VSS if the following requirements are met:<br>- The usb2_dm/usb2_dp pins are left unconnected<br>- The USB2 PHY is kept powered down | PWR | Y12 |
| vdda_abe_per | DPLL_ABE, DPLL_PER, and PER HSDIVIDER analog power supply | PWR | M14 |
| vdda_ddr | DPLL_DDR and DDR HSDIVIDER analog power supply | PWR | P16 |
| vdda_debug | DPLL_DEBUG analog power supply | PWR | N11 |
| vdda_dsp_eve | DPLL_DSP analog power supply | PWR | N12 |
| vdda_gmac_core | DPLL_CORE and CORE HSDIVIDER analog power supply | PWR | P15 |
| vdda_gpu | DPLL_GPU analog power supply | PWR | R14 |
| vdda_hdmi | PLL_HDMI and HDMI analog power supply | PWR | Y17 |
| vssa_hdmi | DPLL_HDMI and HDMI PHY analog ground | GND | AE19/ AD19 |
| vdda_iva | DPLL_IVA analog power supply | PWR | R17 |
| vdda_pcie | DPLL_PCIe_REF and PCIe analog power supply | PWR | W14 |
| vssa_pcie | PCIe analog ground | GND | AE13/ AD13 |
| vdda_pcie0 | PCIe ch0 RX/TX analog power supply | PWR | AA17 |
| vdda_pcie1 | PCIe ch1 RX/TX analog power supply | PWR | AA16 |
| vdda_sata | DPLL_SATA and SATA RX/TX analog power supply | PWR | V13 |
| vssa_sata | SATA analog ground | GND | AE10 |


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**Table 4-34. Power Supply Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| vdda_usb3 | DPLL_USB_OTG_SS and USB3.0 RX/TX analog power supply | PWR | W12 |
| vssa_usb3 | DPLL_USB and USB3.0 RX/TX analog ground | GND | AD10 |
| vdda_video | DPLL_VIDEO1 and DPLL_VIDEO2 analog power supply | PWR | P14 |
| vssa_video | DPLL_VIDEO1 and DPLL_VIDEO2 analog ground | GND | U14 |
| vdds_mlbp | MLBP IO power supply | PWR | AA7/ Y7 |
| vdda_mpu | DPLL_MPU analog power supply | PWR | N16 |
| vdda_osc | HFOSC analog power supply | PWR | AE16/ AD16 |
| vssa_osc0 | OSC0 analog ground | GND | AF15 |
| vssa_osc1 | OSC1 analog ground | GND | AC14 |
| vdda_rtc | RTC bias and RTC LFOSC analog power supply | PWR | AB13 |
| vdds18v | 1.8V power supply | PWR | W17/ W18/ V21/ V22/ T8/ R8/ P8/ N8/ M8/ M9/ H17/ G18 |
| vdds18v_ddr1 | DDR1 bias power supply | PWR | AA18/ AA19/ Y21/ W21 |
| vdds18v_ddr2 | DDR2 bias power supply | PWR | P20/ P21/ N21/ J21/ J22 |
| vdds_ddr2 | DDR2 power supply (1.8V for DDR2 mode/ 1.5V for DDR3 mode / 1.35V for DDR3L mode) | PWR | T24/ T25/ M20/ M21/ L20/ L21/ J27/ H20/ H21/ H22/ G22/ G23/ E24 |
| vdds_ddr1 | DDR1 power supply (1.8V for DDR2 mode/ 1.5V for DDR3 mode / 1.35V for DDR3L mode) | PWR | AH27/ AG20/ AG28/ AD26/ AC22/ AB21/ AB22/ AB24/ AB25/ AA21/ AA22/ W16/ W27 |
| vddshv5 | Dual Voltage (1.8V or 3.3V) power supply for the RTC Power Group pins | PWR | V12 |
| vddshv1 | Dual Voltage (1.8V or 3.3V) power supply for the VIN2 Power Group pins | PWR | H8/ H9/ G4/ G5/ E3/ E5 |
| vddshv10 | Dual Voltage (1.8V or 3.3V) power supply for the GPMC Power Group pins | PWR | T4/ T5/ R7/ R10/ P10/ N4/ N5 |
| vddshv11 | Dual Voltage (1.8V or 3.3V) power supply for the MMC2 Power Group pins | PWR | K8/ J8 |
| vddshv2 | Dual Voltage (1.8V or 3.3V) power supply for the VOUT Power Group pins | PWR | H10/ H11/ E10/ D10/ B6 |
| vddshv3 | Dual Voltage (1.8V or 3.3V) power supply for the GENERAL Power Group pins | PWR | H15/ H16/ H18/ H19/ G15/ E16/ E22/ D16/ D22/ B23 |
| vddshv4 | Dual Voltage (1.8V or 3.3V) power supply for the MMC4 Power Group pins | PWR | C24 |
| vddshv6 | Dual Voltage (1.8V or 3.3V) power supply for the VIN1 Power Group pins | PWR | AF5/ AE7/ AD5/ AD7 |
| vddshv7 | Dual Voltage (1.8V or 3.3V) power supply for the WIFI Power Group pins | PWR | AB6/ AB7 |
| vddshv8 | Dual Voltage (1.8V or 3.3V) power supply for the MMC1 Power Group pins | PWR | Y8/ W8 |
| vddshv9 | Dual Voltage (1.8V or 3.3V) power supply for the RGMII Power Group pins | PWR | W4/ W5/ U10 |
| cap_vddram_dspeve2[(1)] | External capacitor connection for the DSP SRAM array ldo2 output | CAP | J9 |
| cap_vddram_dspeve1[(1)] | External capacitor connection for the DSP SRAM array ldo1 output | CAP | J10 |
| cap_vbbldo_mpu[(1)] | External capacitor connection for the MPU vbb ldo output | CAP | J16 |
| cap_vddram_core2[(1)] | External capacitor connection for the Core SRAM array ldo2 output | CAP | J19 |
| cap_vbbldo_dspeve[(1)] | External capacitor connection for the DSP vbb ldo output | CAP | K9 |
| cap_vddram_mpu1[(1)] | External capacitor connection for the MPU SRAM array ldo1 output | CAP | K16 |

**Table 4-34. Power Supply Signal Descriptions (continued)**

| SIGNAL NAME | DESCRIPTION | TYPE | BALL |
|---|---|---|---|
| cap_vddram_mpu2[(1)] | External capacitor connection for the MPU SRAM array ldo2 output | CAP | K19 |
| cap_vddram_core1[(1)] | External capacitor connection for the Core SRAM array ldo1 output | CAP | L9 |
| cap_vddram_core4[(1)] | External capacitor connection for the Core SRAM array ldo4 output | CAP | P19 |
| cap_vbbldo_iva[(1)] | External capacitor connection for the IVA vbb ldo output | CAP | R20 |
| cap_vddram_iva[(1)] | External capacitor connection for the IVA SRAM array ldo output | CAP | T20 |
| cap_vddram_gpu[(1)] | External capacitor connection for the GPU SRAM array ldo output | CAP | Y13 |
| cap_vbbldo_gpu[(1)] | External capacitor connection for the GPU vbb ldo output | CAP | Y14 |
| cap_vddram_core3[(1)] | External capacitor connection for the Core SRAM array ldo3 output | CAP | Y15 |
| cap_vddram_core5[(1)] | External capacitor connection for the Core SRAM array ldo5 output | CAP | Y16 |

(1) This pin must always be connected via a 1-µF capacitor to vss.


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# 5 Specifications

**NOTE**

For more information, see Power, Reset, and Clock Management / PRCM Subsystem Environment / External Voltage Inputs or Initialization / Preinitialization / Power Requirements section of the Device TRM.

**NOTE**

The index numbers 1 and 2 which is part of the EMIF1 and EMIF2 signal prefixes (ddr1_* and ddr2_*) listed in Table 4-7, *EMIF Signal Descriptions*, column "SIGNAL NAME" not to be confused with DDR1 and DDR2 types of SDRAM memories.

**NOTE**

Audio Back End (ABE) module is not supported for this family of devices, but “ABE” name is still present in some clock or DPLL names.

**CAUTION**

All IO Cells are NOT Fail-safe compliant and should not be externally driven in absence of their IO supply.

## 5.1 Absolute Maximum Ratings

Stresses beyond those listed as absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Section 5.4, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

**Table 5-1. Absolute Maximum Rating Over Junction Temperature Range**

| PARAMETER[(1)] | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{SUPPLY}$ (Steady-State) | Supply Voltage Ranges (Steady-State) | Core (vdd, vdd_mpu, vdd_gpu, vdd_dspeve, vdd_iva, vdd_rtc) | –0.3 | 1.5 | V |
| | | Analog (vdda_usb1, vdda_usb2, vdda_abe_per, vdda_ddr, vdda_debug, vdda_dsp_eve, vdda_gmac_core, vdda_gpu, vdda_hdmi, vdda_iva, vdda_pcie, vdda_pcie0, vdda_pcie1, vdda_sata, vdda_usb3, vdda_video, vdda_mpu, vdda_osc, vdda_rtc) | –0.3 | 2.0 | |
| | | Analog 3.3V (vdda33v_usb1, vdda33v_usb2) | -0.3 | 3.8 | |
| | | vdds18v, vdds18v_ddr1, vdds18v_ddr2, vdds_mlbp, vdds_ddr1, vdds_ddr2 | –0.3 | 2.1 | |
| | | vddshv1-11 (1.8V mode) | –0.3 | 2.1 | |
| | | vddshv1-7 (3.3V mode), vddshv9-11 (3.3V mode) | –0.3 | 3.8 | |
| | | vddshv8 (3.3V mode) | –0.3 | 3.6 | |

**Table 5-1. Absolute Maximum Rating Over Junction Temperature Range (continued)**

| PARAMETER[1] | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IO}$ (Steady-State) | Input and Output Voltage Ranges (Steady-State) | Core I/Os | –0.3 | 1.5 | V |
| | | Analog I/Os (except HDMI) | –0.3 | 2.0 | |
| | | HDMI I/Os | –0.3 | 3.5 | |
| | | I/O 1.35 V | –0.3 | 1.65 | |
| | | I/O 1.5 V | –0.3 | 1.8 | |
| | | 1.8 V I/Os | –0.3 | 2.1 | |
| | | 3.3 V I/Os (except those powered by vddshv8) | –0.3 | 3.8 | |
| | | 3.3 V I/Os (powered by vddshv8) | –0.3 | 3.6 | |
| SR | Maximum slew rate, all supplies | | | $10^5$ | V/s |
| $V_{IO}$ (Transient Overshoot / Undershoot) | Input and Output Voltage Ranges (Transient Overshoot/Undershoot) Note: valid for up to 20% of the signal period. See Figure 5-1, *IO transient voltage ranges* | | | 0.2*VDD [2] | V |
| $T_{STG}$ | Storage temperature range after soldered onto PC Board | | –55 | +150 | °C |
| Latch-up I-Test | I-test[3], All I/Os (if different levels then one line per level) | | –100 | 100 | mA |
| Latch-up OV-Test | Over-voltage Test[4], All supplies (if different levels then one line per level) | | N/A | $1.5*V_{SUPPLY\ MAX}$ | V |

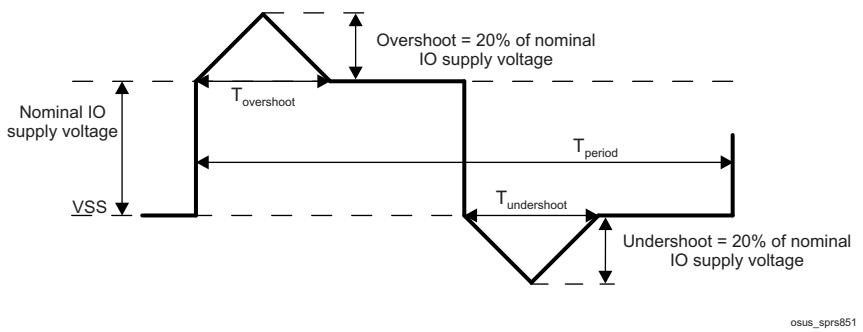
(1) See I/Os supplied by this power pin in Table 4-2 *Ball Characteristics*

(2) VDD is the voltage on the corresponding power-supply pin(s) for the I/O.

(3) Per JEDEC JESD78 at 125°C with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

(4) Per JEDEC JESD78 at 125°C.

(5) The maximum valid input voltage on an IO pin cannot exceed 0.3 volts when the supply powering the IO is turned off. This requirement applies to all the IO pins which are not fail-safe and for all values of IO supply voltage. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.




(1) $T_{overshoot} + T_{undershoot} < 20\%$ of $T_{period}$

**Figure 5-1. IO transient voltage ranges**

## 5.2 ESD Ratings

**Table 5-2. ESD Ratings**

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±250 | |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(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Power on Hours (POH) Limits

The information in the section below is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

**NOTE**

POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH.

**Table 5-3. Power on Hour (POH) Limits[(1)]**

| OPERATING CONDITION | | COMMERCIAL JUNCTION TEMP RANGE 0°C ~ 90°C | | EXTENDED JUNCTION TEMP RANGE -40°C ~ 105°C | | | |
|---|---|---|---|---|---|---|---|
| OPP | HDMI | JUNCTION TEMP (Tj) | LIFETIME (POH) | JUNCTION TEMP (Tj) | LIFETIME (POH) | JUNCTION TEMP (Tj) | LIFETIME (POH) |
| OPP_NOM or OPP_OD | Not Used | 90°C | 100k | 100°C | 100k | 105°C | 100k[(3)] |
| | Used | 90°C | 100k | 100°C | 63k | 105°C | 45k |
| OPP_HIGH | Not Used | 90°C | 65k | 100°C | 55k | 105°C | 50k |
| | Used | 90°C | 65k | 100°C | 55k | 105°C | 45k |

(1) Unless specified in Table 5-3, all voltage domains and operating conditions are supported in the device at the noted temperatures.
(2) Power on hours (POH) assume HDMI is used at the maximum supported bit rate continuously and/or operating the device continuously at the VD_MPU operating point (OPP) noted.
(3) 90k POH only if SuperSpeed USB 3.0 Dual-Role-Device (at 5 Gbps) or PCIe in Gen-II mode (at 5 Gbps) are used.

## 5.4 Recommended Operating Conditions

The device is used under the recommended operating conditions described in Table 5-4.

**NOTE**

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

**Table 5-4. Recommended Operating Conditions**

| PARAMETER | DESCRIPTION | MIN [2] | NOM | MAX DC [3] | MAX [2] | UNIT |
|---|---|---|---|---|---|---|
| **Input Power Supply Voltage Range** | | | | | | |
| vdd | Core voltage domain supply | See Section 5.5 | | | | V |
| vdd_mpu | Supply voltage range for MPU domain | See Section 5.5 | | | | V |
| vdd_gpu | GPU voltage domain supply | See Section 5.5 | | | | V |
| vdd_dspeve | DSP voltage domain supply | See Section 5.5 | | | | V |
| vdd_iva | IVA voltage domain supply | See Section 5.5 | | | | V |
| vdd_rtc | RTC voltage domain supply | See Section 5.5 | | | | V |
| vdda_usb1 | DPLL_USB and HS USB1 1.8V analog power supply | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | 50 | | | $mV_{PPmax}$ |
| vdda_usb2 | HS USB2 1.8V analog power supply | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | 50 | | | $mV_{PPmax}$ |
| vdda33v_usb1 | HS USB1 3.3V analog power supply.If USB1 is not used, this pin can alternatively be connected to VSS if the following requirements are met:<br>- The usb1_dm/usb1_dp pins are left unconnected<br>- The USB1 PHY is kept powered down | 3.135 | 3.3 | 3.366 | 3.465 | V |
| | Maximum noise (peak-peak) | | 50 | | | $mV_{PPmax}$ |
| vdda33v_usb2 | HS USB2 3.3V analog power supply. If USB2 is not used, this pin can alternatively be connected to VSS if the following requirements are met:<br>- The usb2_dm/usb2_dp pins are left unconnected<br>- The USB2 PHY is kept powered down | 3.135 | 3.3 | 3.366 | 3.465 | V |
| | Maximum noise (peak-peak) | | 50 | | | $mV_{PPmax}$ |
| vdda_abe_per | DPLL_ABE, DPLL_PER, and PER HSDIVIDER analog power supply | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | 50 | | | $mV_{PPmax}$ |
| vdda_ddr | DPLL_DDR and DDR HSDIVIDER analog power supply | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | 50 | | | $mV_{PPmax}$ |
| vdda_debug | DPLL_DEBUG analog power supply | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | 50 | | | $mV_{PPmax}$ |
| vdda_dsp_eve | DPLL_DSP analog power supply | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | 50 | | | $mV_{PPmax}$ |
| vdda_gmac_core | DPLL_CORE and CORE HSDIVIDER analog power supply | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | 50 | | | $mV_{PPmax}$ |
| vdda_gpu | DPLL_GPU analog power supply | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | 50 | | | $mV_{PPmax}$ |


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**Table 5-4. Recommended Operating Conditions (continued)**

| PARAMETER | DESCRIPTION | | MIN (2) | NOM | MAX DC (3) | MAX (2) | UNIT |
|---|---|---|---|---|---|---|---|
| vdda_hdmi | PLL_HDMI and HDMI analog power supply | | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdda_iva | DPLL_IVA analog power supply | | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdda_pcie | DPLL_PCIe_REF and PCIe analog power supply | | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdda_pcie0 | PCIe ch0 RX/TX analog power supply | | 1.71 | 1.80 | | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdda_pcie1 | PCIe ch1 RX/TX analog power supply | | 1.71 | 1.80 | | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdda_sata | DPLL_SATA and SATA RX/TX analog power supply | | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdda_usb3 | DPLL_USB_OTG_SS and USB3.0 RX/TX analog power supply | | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdda_video | DPLL_VIDEO1 and DPLL_VIDEO2 analog power supply | | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdda_mpu | DPLL_MPU analog power supply | | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdda_osc | HFOSC analog power supply | | 1.71 | 1.80 | | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdda_rtc | RTC bias and RTC LFOSC analog power supply | | 1.71 | 1.80 | | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdds18v | 1.8V power supply | | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdds18v_ddr1 | EMIF1 bias power supply | | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdds18v_ddr2 | EMIF2 bias power supply | | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | Maximum noise (peak-peak) | | | 50 | | | $mV_{PPmax}$ |
| vdds_ddr1 | EMIF1 power supply (1.5V for DDR3 mode / 1.35V for DDR3L mode) | 1.35-V Mode | 1.28 | 1.35 | 1.377 | 1.42 | V |
| | | 1.5-V Mode | 1.43 | 1.50 | 1.53 | 1.57 | |
| | Maximum noise (peak-peak) | 1.35-V Mode | | 50 | | | $mV_{PPmax}$ |
| | | 1.5-V Mode | | | | | |
| vdds_ddr2 | EMIF2 power supply (1.5V for DDR3 mode / 1.35V for DDR3L mode) | 1.35-V Mode | 1.28 | 1.35 | 1.377 | 1.42 | V |
| | | 1.5-V Mode | 1.43 | 1.50 | 1.53 | 1.57 | |
| | Maximum noise (peak-peak) | 1.35-V Mode | | 50 | | | $mV_{PPmax}$ |
| | | 1.5-V Mode | | | | | |

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**Table 5-4. Recommended Operating Conditions (continued)**

| PARAMETER | DESCRIPTION | | MIN (2) | NOM | MAX DC (3) | MAX (2) | UNIT |
|---|---|---|---|---|---|---|---|
| vddshv5 | Dual Voltage (1.8V or 3.3V) power supply for the RTC Power Group pins | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | | 3.3-V Mode | 3.135 | 3.30 | 3.366 | 3.465 | |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | $mV_{PPmax}$ |
| | | 3.3-V Mode | | | | | |
| vddshv1 | Dual Voltage (1.8V or 3.3V) power supply for the VIN2 Power Group pins | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | | 3.3-V Mode | 3.135 | 3.30 | 3.366 | 3.465 | |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | $mV_{PPmax}$ |
| | | 3.3-V Mode | | | | | |
| vddshv10 | Dual Voltage (1.8V or 3.3V) power supply for the GPMC Power Group pins | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | | 3.3-V Mode | 3.135 | 3.30 | 3.366 | 3.465 | |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | $mV_{PPmax}$ |
| | | 3.3-V Mode | | | | | |
| vddshv11 | Dual Voltage (1.8V or 3.3V) power supply for the MMC2 Power Group pins | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | | 3.3-V Mode | 3.135 | 3.30 | 3.366 | 3.465 | |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | $mV_{PPmax}$ |
| | | 3.3-V Mode | | | | | |
| vddshv2 | Dual Voltage (1.8V or 3.3V) power supply for the VOUT Power Group pins | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | | 3.3-V Mode | 3.135 | 3.30 | 3.366 | 3.465 | |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | $mV_{PPmax}$ |
| | | 3.3-V Mode | | | | | |
| vddshv3 | Dual Voltage (1.8V or 3.3V) power supply for the GENERAL Power Group pins | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | | 3.3-V Mode | 3.135 | 3.30 | 3.366 | 3.465 | |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | $mV_{PPmax}$ |
| | | 3.3-V Mode | | | | | |
| vddshv4 | Dual Voltage (1.8V or 3.3V) power supply for the MMC4 Power Group pins | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | | 3.3-V Mode | 3.135 | 3.30 | 3.366 | 3.465 | |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | $mV_{PPmax}$ |
| | | 3.3-V Mode | | | | | |
| vddshv6 | Dual Voltage (1.8V or 3.3V) power supply for the VIN1 Power Group pins | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | | 3.3-V Mode | 3.135 | 3.30 | 3.366 | 3.465 | |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | $mV_{PPmax}$ |
| | | 3.3-V Mode | | | | | |
| vddshv7 | Dual Voltage (1.8V or 3.3V) power supply for the WIFI Power Group pins | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | | 3.3-V Mode | 3.135 | 3.30 | 3.366 | 3.465 | |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | $mV_{PPmax}$ |
| | | 3.3-V Mode | | | | | |


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**Table 5-4. Recommended Operating Conditions (continued)**

| PARAMETER | DESCRIPTION | | MIN (2) | NOM | MAX DC (3) | MAX (2) | UNIT |
|---|---|---|---|---|---|---|---|
| vddshv8 | Dual Voltage (1.8V or 3.3V) power supply for the MMC1 Power Group pins | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | | 3.3-V Mode | 3.135 | 3.30 | 3.366 | 3.465 | |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | $mV_{PPmax}$ |
| | | 3.3-V Mode | | | | | |
| vddshv9 | Dual Voltage (1.8V or 3.3V) power supply for the RGMII Power Group pins | 1.8-V Mode | 1.71 | 1.80 | 1.836 | 1.89 | V |
| | | 3.3-V Mode | 3.135 | 3.30 | 3.366 | 3.465 | |
| | Maximum noise (peak-peak) | 1.8-V Mode | | 50 | | | $mV_{PPmax}$ |
| | | 3.3-V Mode | | | | | |
| vss | Ground supply | | | | | 0 | V |
| vssa_hdmi | DPLL_HDMI and HDMI PHY analog ground | | | | | 0 | V |
| vssa_pcie | PCIe analog ground | | | | | 0 | V |
| vssa_usb | HS USB1 and HS USB2 analog ground | | | | | 0 | V |
| vssa_usb3 | DPLL_USB and USB3.0 RX/TX analog ground | | | | | 0 | V |
| vssa_video | DPLL_VIDEO1 and DPLL_VIDEO2 analog ground | | | | | 0 | V |
| vssa_osc0 | OSC0 analog ground | | | | | 0 | V |
| vssa_osc1 | OSC1 analog ground | | | | | 0 | V |
| $T_J$ | Operating junction temperature range | Commercial | 0 | | | 90 | °C |
| | | Extended | -40 | | | 105 | |
| ddr1_vref0 | Reference Power Supply EMIF1 | | 0.5*vdds_ddr1 | | | | V |
| ddr2_vref0 | Reference Power Supply EMIF2 | | 0.5*vdds_ddr2 | | | | V |

(1) Refer to Section 5.3, Power on Hour (POH) Limits for limitations.

(2) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.

(3) The DC voltage at the device ball should never be above the MAX DC voltage to avoid impact on device reliability and lifetime POH (Power on Hour). The MAX DC voltage is defined as the highest allowed DC regulated voltage, without transients, seen at the ball.

## 5.5 Operating Performance Points

This section describes the operating conditions of the AM572x device. This section also contains the description of each OPP (operating performance point) for processor clocks and device core clocks.

Table 5-5 describes the maximum supported frequency per speed grade for AM572x devices.

**Table 5-5. Speed Grade Maximum Frequency**

| DEVICE SPEED | MAXIMUM FREQUENCY (MHz) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | MPU | DSP | EVE | IVA | GPU | IPU | L3 | DDR3/DDR3L |
| AM5729 | 1500 | 750 | 650 | 532 | 532 | 212.8 | 266 | 533 (DDR3-1066) |
| AM5728 | 1500 | 750 | N/A | 532 | 532 | 212.8 | 266 | 533 (DDR3-1066) |
| AM5726 | 1500 | 750 | N/A | N/A | N/A | 212.8 | 266 | 533 (DDR3-1066) |

(1) N/A in this table stands for Not Applicable

### *5.5.1 AVS and ABB Requirements*

Adaptive Voltage Scaling (AVS) and Adaptive Body Biasing (ABB) are required on most of the vdd_* supplies as defined in Table 5-6.

**Table 5-6. AVS and ABB Requirements per vdd_* Supply**

| SUPPLY | AVS REQUIRED? | ABB REQUIRED? |
|---|---|---|
| vdd_core | Yes, for all OPPs | No |
| vdd_mpu | Yes, for all OPPs | Yes, for all OPPs |
| vdd_ivahd | Yes, for all OPPs | Yes, for all OPPs |
| vdd_dspeve | Yes, for all OPPs | Yes, for all OPPs |
| vdd_gpu | Yes, for all OPPs | Yes, for all OPPs |
| vdd_rtc | No | No |

### 5.5.2 Voltage And Core Clock Specifications

Table 5-7 shows the recommended OPP per voltage domain.

**Table 5-7. Voltage Domains Operating Performance Points**

| DOMAIN | CONDITION | OPP_NOM | | | OPP_OD | | | OPP_HIGH | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN (2) | NOM (1) | MAX (2) | MIN (2) | NOM (1) | MAX (2) | MIN (2) | NOM (1) | MAX DC (3) | MAX (2) |
| VD_CORE (V) | BOOT (Before AVS is enabled) (4) | 1.11 | 1.15 | 1.2 | Not Applicable | | | Not Applicable | | | |
| | After AVS is enabled (4) | AVS Voltage (5) – 3.5% | AVS Voltage (5) | 1.2 | Not Applicable | | | Not Applicable | | | |
| VD_MPU (V) | BOOT (Before AVS is enabled)(4) | 1.06 | 1.15 | 1.2 | Not Applicable | | | Not Applicable | | | |
| | After AVS is enabled(4) | AVS Voltage (5) – 3.5% | AVS Voltage (5) | 1.2 | AVS Voltage (5) – 3.5% | AVS Voltage (5) | AVS Voltage (5) + 5% | AVS Voltage (5) – 3.5% | AVS Voltage (5) | AVS Voltage (5) +2% | AVS Voltage (5) + 5% |
| VD_RTC (V) (6) | - | 0.84 | 0.88 to 1.06 | 1.16 | Not Applicable | | | Not Applicable | | | |
| Others (V) | BOOT (Before AVS is enabled) (4) | 1.02 | 1.06 | 1.16 | Not Applicable | | | Not Applicable | | | |
| | After AVS is enabled(4) | AVS Voltage (5) – 3.5% | AVS Voltage (5) | 1.16 | AVS Voltage (5) – 3.5% | AVS Voltage (5) | AVS Voltage (5) + 5% | AVS Voltage (5) – 3.5% | AVS Voltage (5) | AVS Voltage (5) +2% | AVS Voltage (5) + 5% |

(1) In a typical implementation, the power supply should target the NOM voltage.

(2) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.

(3) The DC voltage at the device ball should never be above the MAX DC voltage to avoid impact on device reliability and lifetime POH (Power on Hour). The MAX DC voltage is defined as the highest allowed DC regulated voltage, without transients, seen at the ball.

(4) For all OPPs, AVS must be enabled to avoid impact on device reliability, lifetime POH (Power on Hour), and device power.

(5) The AVS voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the STD_FUSE_OPP. For information about STD_FUSE_OPP Registers address, please refer to Control Module Section of the TRM. The power supply should be adjustable over the following ranges for each required OPP:

- OPP_NOM for MPU: 0.85 V – 1.15 V
- OPP_NOM for CORE and Others: 0.85 V - 1.15 V
- OPP_OD: 0.885 V - 1.15 V
- OPP_HIGH: 0.95 V - 1.25 V

The AVS voltages will be within the above specified ranges.

(6) VD_RTC can optionally be tied to VD_CORE and operate at the VD_CORE AVS voltages.

(7) The power supply must be programmed with the AVS voltages for the MPU and the CORE voltage domain, either just after the ROM boot or at the earliest possible time in the secondary boot loader before there is significant activity seen on these domains.

Table 5-8 describes the standard processor clocks speed characteristics vs OPP of the device.


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**Table 5-8. Supported OPP vs Max Frequency (2)**

| DESCRIPTION | OPP_NOM | OPP_OD | OPP_HIGH |
|---|---|---|---|
| | MAX FREQ. (MHz) | MAX FREQ. (MHz) | MAX FREQ. (MHz) |
| **VD_MPU** | | | |
| MPU_CLK | 1000 | 1176 | 1500 |
| **VD_DSPEVE** | | | |
| DSP_CLK | 600 | 700 | 750 |
| EVE_FCLK | 535 | 650 | 650 |
| **VD_IVA** | | | |
| IVA_GCLK | 388.3 | 430 | 532 |
| **VD_GPU** | | | |
| GPU_CLK | 425.6 | 500 | 532 |
| **VD_CORE** | | | |
| CORE_IPUx_CLK | 212.8 | N/A | N/A |
| L3_CLK | 266 | N/A | N/A |
| DDR3 / DDR3L | 532 (DDR3-1066) | N/A | N/A |
| **VD_RTC** | | | |
| RTC_FCLK | 0.034 | N/A | N/A |

(1) N/A in this table stands for Not Applicable.

(2) Maximum supported frequency is limited according to Table 5-5, *Speed Grade Maximum Frequency*).

### 5.5.3 Maximum Supported Frequency

Device modules either receive their clock directly from an external clock input, directly from a PLL, or from a PRCM. Table 5-9 lists the clock source options for each module on this device, along with the maximum frequency that module can accept. To ensure proper module functionality, the device PLLs and dividers must be programmed not to exceed the maximum frequencies listed in this table.

**Table 5-9. Maximum Supported Frequency**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| AES1 | AES1_L3_CLK | Int | 266 | L4SEC_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| AES2 | AES2_L3_CLK | Int | 266 | L4SEC_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| BB2D | BB2D_FCLK | Func | 354.6 | BB2D_GFCLK | BB2D_GFCLK | DPLL_CORE |
| | BB2D_ICLK | Int | 266 | DSS_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| COUNTER_32K | COUNTER_32K_FCLK | Func | 0.032 | FUNC_32K_CLK | SYS_CLK1/610 | OSC1 |
| | COUNTER_32K_ICLK | Int | 38.4 | WKUPAON_GICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| CTRL_MODULE_BANDGAP | L3INSTR_TS_GCLK | Int | 4.8 | L3INSTR_TS_GCLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| CTRL_MODULE_CORE | L4CFG_L4_GICLK | Int | 133 | L4CFG_L4_GICLK | CORE_X2_CLK | DPLL_CORE |
| CTRL_MODULE_WKUP | WKUPAON_GICLK | Int | 38.4 | WKUPAON_GICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| DCAN1 | DCAN1_FCLK | Func | 38.4 | DCAN1_SYS_CLK | SYS_CLK1 | OSC1 |
| | | | | | SYS_CLK2 | OSC2 |
| | DCAN1_ICLK | Int | 266 | WKUPAON_GICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |

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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| **Instance Name** | **Input Clock Name** | **Clock Type** | **Max. Clock Allowed (MHz)** | **PRCM Clock Name** | **PLL / OSC / Source Clock Name** | **PLL / OSC / Source Name** |
| DCAN2 | DCAN2_FCLK | Func | 38.4 | DCAN2_SYS_CLK | SYS_CLK1 | OSC1 |
| | DCAN2_ICLK | Int | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| DES3DES | DES_CLK_L3 | Int | 266 | L4SEC_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| DLL | EMIF_DLL_FCLK | Func | EMIF_DLL_FCLK | EMIF_DLL_GCLK | EMIF_DLL_GCLK | DPLL_DDR |
| DLL_AGING | FCLK | Int | 38.4 | L3INSTR_DLL_AGING_GCLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| DMM | DMM_CLK | Int | 266 | EMIF_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| DPLL_DEBUG | SYSCLK | Int | 38.4 | EMU_SYS_CLK | SYS_CLK1 | OSC1 |
| DSP1 | DSP1_FICLK | Int & Func | DSP_CLK | DSP1_GFCLK | DSP_GFCLK | DPLL_DSP |
| DSP2 | DSP2_FICLK | Int & Func | DSP_CLK | DSP2_GFCLK | DSP_GFCLK | DPLL_DSP |
| DSS | DSS_HDMI_CEC_CLK | Func | 0.032 | HDMI_CEC_GFCLK | SYS_CLK1/610 | OSC1 |
| | DSS_HDMI_PHY_CLK | Func | 48 | HDMI_PHY_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | DSS_CLK | Func | 192 | DSS_GFCLK | DSS_CLK | DPLL_PER |
| | HDMI_CLKINP | Func | 38.4 | HDMI_DPLL_CLK | SYS_CLK1 | OSC1 |
| | | | | | SYS_CLK2 | OSC2 |
| | DSS_L3_ICLK | Int | 266 | DSS_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | VIDEO1_CLKINP | Func | 38.4 | VIDEO1_DPLL_CLK | SYS_CLK1 | OSC1 |
| | | | | | SYS_CLK2 | OSC2 |
| | VIDEO2_CLKINP | Func | 38.4 | VIDEO2_DPLL_CLK | SYS_CLK1 | OSC1 |
| | | | | | SYS_CLK2 | OSC2 |
| | DPLL_DSI1_A_CLK1 | Func | 209.3 | N/A | HDMI_CLK | DPLL_HDMI |
| | | | | | VIDEO1_CLKOUT1 | DPLL_VIDEO1 |
| | DPLL_DSI1_B_CLK1 | Func | 209.3 | N/A | VIDEO1_CLKOUT3 | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLKOUT3 | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | DPLL_DSI1_C_CLK1 | Func | 209.3 | N/A | HDMI_CLK | DPLL_HDMI |
| | | | | | VIDEO1_CLKOUT3 | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLKOUT1 | DPLL_VIDEO2 |
| | DPLL_HDMI_CLK1 | Func | 185.6 | N/A | HDMI_CLK | DPLL_HDMI |
| DSS DISPC | LCD1_CLK | Func | 209.3 | N/A | DPLL_DSI1_A_CLK1 | See DSS data in the rows above |
| | | | | | DSS_CLK | |
| | LCD2_CLK | Func | 209.3 | N/A | DPLL_DSI1_B_CLK1 | |
| | | | | | DSS_CLK | |
| | LCD3_CLK | Func | 209.3 | N/A | DPLL_DSI1_C_CLK1 | |
| | | | | | DSS_CLK | |
| | F_CLK | Func | 209.3 | N/A | DPLL_DSI1_A_CLK1 | |
| | | | | | DPLL_DSI1_B_CLK1 | |
| | | | | | DPLL_DSI1_C_CLK1 | |
| | | | | | DSS_CLK | |
| | | | | | DPLL_HDMI_CLK1 | |


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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| **Instance Name** | **Input Clock Name** | **Clock Type** | **Max. Clock Allowed (MHz)** | **PRCM Clock Name** | **PLL / OSC / Source Clock Name** | **PLL / OSC / Source Name** |
| EFUSE_CTRL_CUST | ocp_clk | Int | 133 | CUSTEFUSE_L4_GICLK | CORE_X2_CLK | DPLL_CORE |
| | sys_clk | Func | 38.4 | CUSTEFUSE_SYS_GFCLK | SYS_CLK1 | OSC1 |
| ELM | ELM_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| EMIF_OCP_FW | L3_CLK | Int | 266 | EMIF_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| EMIF_PHY1 | EMIF_PHY1_FCLK | Func | DDR | EMIF_PHY_GCLK | EMIF_PHY_GCLK | DPLL_DDR |
| EMIF_PHY2 | EMIF_PHY2_FCLK | Func | DDR | EMIF_PHY_GCLK | EMIF_PHY_GCLK | DPLL_DDR |
| EMIF1 | EMIF1_ICLK | Int | 266 | EMIF_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| EMIF2 | EMIF2_ICLK | Int | 266 | EMIF_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| EVE1 | EVE1_FCLK | Func | EVE_FCLK | EVE1_GFCLK | - | DPLL_DSP |
| | | | | | EVE_GFCLK | DPLL_EVE |
| EVE2 | EVE2_FCLK | Func | EVE_FCLK | EVE2_GFCLK | - | DPLL_DSP |
| | | | | | EVE_GFCLK | DPLL_EVE |
| EVE3 | EVE3_FCLK | Func | EVE_FCLK | EVE3_GFCLK | - | DPLL_DSP |
| | | | | | EVE_GFCLK | DPLL_EVE |
| EVE4 | EVE4_FCLK | Func | EVE_FCLK | EVE4_GFCLK | - | DPLL_DSP |
| | | | | | EVE_GFCLK | DPLL_EVE |
| FPKA | PKA_CLK | Int & Func | 266 | L4SEC_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| GMAC_SW | CPTS_RFT_CLK | Func | 266 | GMAC_RFT_CLK | PER_ABE_X1_GFCLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | | | | | CORE_X2_CLK | DPLL_CORE |
| | MAIN_CLK | Int | 125 | GMAC_MAIN_CLK | GMAC_250M_CLK | DPLL_GMAC |
| | MHZ_250_CLK | Func | 250 | GMII_250MHZ_CLK | GMII_250MHZ_CLK | DPLL_GMAC |
| | MHZ_5_CLK | Func | 5 | RGMII_5MHZ_CLK | GMAC_RMII_HS_CLK | DPLL_GMAC |
| | MHZ_50_CLK | Func | 50 | RMII_50MHZ_CLK | GMAC_RMII_HS_CLK | DPLL_GMAC |
| | RMII1_MHZ_50_CLK | Func | 50 | RMII_50MHZ_CLK | GMAC_RMII_HS_CLK | DPLL_GMAC |
| | RMII2_MHZ_50_CLK | Func | 50 | RMII_50MHZ_CLK | GMAC_RMII_HS_CLK | DPLL_GMAC |
| GPIO1 | GPIO1_ICLK | Int | 38.4 | WKUPAON_GICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | GPIO1_DBCLK | Func | 0.032 | WKUPAON_SYS_GFCLK | WKUPAON_32K_GFCLK | OSC1 |
| | | | | | | RTC Oscillator |
| GPIO2 | GPIO2_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | GPIO2_DBCLK | Func | 0.032 | GPIO_GFCLK | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| GPIO3 | GPIO3_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | GPIO3_DBCLK | Func | 0.032 | GPIO_GFCLK | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| GPIO4 | GPIO4_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | GPIO4_DBCLK | Func | 0.032 | GPIO_GFCLK | FUNC_32K_CLK | OSC1 |
| | PIDBCLK | Func | 0.032 | GPIO_GFCLK | | RTC Oscillator |

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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| GPIO5 | GPIO5_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | GPIO5_DBCLK | Func | 0.032 | GPIO_GFCLK | FUNC_32K_CLK | OSC1 |
| | PIDBCLK | Func | 0.032 | GPIO_GFCLK | | RTC Oscillator |
| GPIO6 | GPIO6_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | GPIO6_DBCLK | Func | 0.032 | GPIO_GFCLK | FUNC_32K_CLK | OSC1 |
| | PIDBCLK | Func | 0.032 | GPIO_GFCLK | | RTC Oscillator |
| GPIO7 | GPIO7_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | GPIO7_DBCLK | Func | 0.032 | GPIO_GFCLK | FUNC_32K_CLK | OSC1 |
| | PIDBCLK | Func | 0.032 | GPIO_GFCLK | | RTC Oscillator |
| GPIO8 | GPIO8_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | GPIO8_DBCLK | Func | 0.032 | GPIO_GFCLK | FUNC_32K_CLK | OSC1 |
| | PIDBCLK | Func | 0.032 | GPIO_GFCLK | | RTC Oscillator |
| GPMC | GPMC_FCLK | Int | 266 | L3MAIN1_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| GPU | GPU_FCLK1 | Func | GPU_CLK | GPU_CORE_GCLK | CORE_GPU_CLK | DPLL_CORE |
| | | | | | PER_GPU_CLK | DPLL_PER |
| | | | | | GPU_GCLK | DPLL_GPU |
| | GPU_FCLK2 | Func | GPU_CLK | GPU_HYD_GCLK | CORE_GPU_CLK | DPLL_CORE |
| | | | | | PER_GPU_CLK | DPLL_PER |
| | | | | | GPU_GCLK | DPLL_GPU |
| | GPU_ICLK | Int | 266 | GPU_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| HDMI PHY | DSS_HDMI_PHY_CLK | Func | 38.4 | HDMI_PHY_GFCLK | FUNC_192M_CLK | DPLL_PER |
| HDQ1W | HDQ1W_ICLK | Int & Func | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | HDQ1W_FCLK | Func | 12 | PER_12M_GFCLK | FUNC_192M_CLK | DPLL_PER |
| I2C1 | I2C1_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | I2C1_FCLK | Func | 96 | PER_96M_GFCLK | FUNC_192M_CLK | DPLL_PER |
| I2C2 | I2C2_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | I2C2_FCLK | Func | 96 | PER_96M_GFCLK | FUNC_192M_CLK | DPLL_PER |
| I2C3 | I2C3_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | I2C3_FCLK | Func | 96 | PER_96M_GFCLK | FUNC_192M_CLK | DPLL_PER |
| I2C4 | I2C4_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | I2C4_FCLK | Func | 96 | PER_96M_GFCLK | FUNC_192M_CLK | DPLL_PER |
| I2C5 | I2C5_ICLK | Int | 266 | IPU_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | I2C5_FCLK | Func | 96 | IPU_96M_GFCLK | FUNC_192M_CLK | DPLL_PER |
| IEEE1500_2_OCP | PI_L3CLK | Int & Func | 266 | L3INIT_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| IPU1 | IPU1_GFCLK | Int & Func | 425.6 | IPU1_GFCLK | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | CORE_IPU_ISS_BOOST_CLK | DPLL_CORE |
| IPU2 | IPU2_GFCLK | Int & Func | 425.6 | IPU2_GFCLK | CORE_IPU_ISS_BOOST_CLK | DPLL_CORE |
| IVA | IVA_GCLK | Int | IVA_GCLK | IVA_GCLK | IVA_GFCLK | DPLL_IVA |


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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| **Instance Name** | **Input Clock Name** | **Clock Type** | **Max. Clock Allowed (MHz)** | **PRCM Clock Name** | **PLL / OSC / Source Clock Name** | **PLL / OSC / Source Name** |
| KBD | KBD_FCLK | Func | 0.032 | WKUPAON_SYS_GFCLK | WKUPAON_32K_GFCLK | OSC1 |
| | PICLKKBD | Func | 0.032 | WKUPAON_SYS_GFCLK | RTC Oscillator | |
| | KBD_ICLK | Int | 38.4 | WKUPAON_GICLK | SYS_CLK1 | OSC1 |
| | PICLKOCP | Int | 38.4 | WKUPAON_GICLK | DPLL_ABE_X2_CLK | DPLL_ABE |
| L3_INSTR | L3_CLK | Int | L3_CLK | L3INSTR_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| L3_MAIN | L3_CLK1 | Int | L3_CLK | L3MAIN1_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | L3_CLK2 | Int | L3_CLK | L3INSTR_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| L4_CFG | L4_CFG_CLK | Int | 133 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| L4_PER1 | L4_PER1_CLK | Int | 133 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| L4_PER2 | L4_PER2_CLK | Int | 133 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| L4_PER3 | L4_PER3_CLK | Int | 133 | L4PER3_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| L4_WKUP | L4_WKUP_CLK | Int | 38.4 | WKUPAON_GICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| MAILBOX1 | MAILBOX1_FLCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MAILBOX2 | MAILBOX2_FLCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MAILBOX3 | MAILBOX3_FLCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MAILBOX4 | MAILBOX4_FLCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MAILBOX5 | MAILBOX5_FLCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MAILBOX6 | MAILBOX6_FLCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MAILBOX7 | MAILBOX7_FLCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MAILBOX8 | MAILBOX8_FLCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MAILBOX9 | MAILBOX9_FLCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MAILBOX10 | MAILBOX10_FLCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MAILBOX11 | MAILBOX11_FLCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MAILBOX12 | MAILBOX12_FLCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MAILBOX13 | MAILBOX13_FLCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |

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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| McASP1 | MCASP1_AHCLKR | Func | 100 | MCASP1_AHCLKR | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | SYS_CLK1 | OSC1 |
| | | | | | FUNC_96M_AON_CLK | DPLL_PER |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | MLB_CLK | Module MLB |
| | | | | | MLBP_CLK | Module MLB |
| | MCASP1_AHCLKX | Func | 100 | MCASP1_AHCLKX | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | SYS_CLK1 | OSC1 |
| | | | | | FUNC_96M_AON_CLK | DPLL_PER |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | MLB_CLK | Module MLB |
| | | | | | MLBP_CLK | Module MLB |
| | MCASP1_FCLK | Func | 192 | MCASP1_AUX_GFCLK | PER_ABE_X1_GFCLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | MCASP1_ICLK | Int | 266 | IPU_L3_GICLK | CORE_X2_CLK | DPLL_CORE |


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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| **Instance Name** | **Input Clock Name** | **Clock Type** | **Max. Clock Allowed (MHz)** | **PRCM Clock Name** | **PLL / OSC / Source Clock Name** | **PLL / OSC / Source Name** |
| McASP2 | MCASP2_AHCLKR | Func | 100 | MCASP2_AHCLKR | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | SYS_CLK1 | OSC1 |
| | | | | | FUNC_96M_AON_CLK | DPLL_PER |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | MLB_CLK | Module MLB |
| | | | | | MLBP_CLK | Module MLB |
| | MCASP2_AHCLKX | Func | 100 | MCASP2_AHCLKX | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | SYS_CLK1 | OSC1 |
| | | | | | FUNC_96M_AON_CLK | DPLL_PER |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | MLB_CLK | Module MLB |
| | | | | | MLBP_CLK | Module MLB |
| | MCASP2_FCLK | Func | 192 | MCASP2_AUX_GFCLK | PER_ABE_X1_GFCLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | MCASP2_ICLK | Int | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| McASP3 | MCASP3_AHCLKX | Func | 100 | MCASP3_AHCLKX | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | SYS_CLK1 | OSC1 |
| | | | | | FUNC_96M_AON_CLK | DPLL_PER |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | MLB_CLK | Module MLB |
| | | | | | MLBP_CLK | Module MLB |
| | MCASP3_FCLK | Func | 192 | MCASP3_AUX_GFCLK | PER_ABE_X1_GFCLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_ABE |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | MCASP3_ICLK | Int | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |

**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| McASP4 | MCASP4_AHCLKX | Func | 100 | MCASP4_AHCLKX | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | SYS_CLK1 | OSC1 |
| | | | | | FUNC_96M_AON_CLK | DPLL_PER |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | MLB_CLK | Module MLB |
| | | | | | MLBP_CLK | Module MLB |
| | MCASP4_FCLK | Func | 192 | MCASP4_AUX_GFCLK | PER_ABE_X1_GFCLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_ABE |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | MCASP4_ICLK | Int | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| McASP5 | MCASP5_AHCLKX | Func | 100 | MCASP5_AHCLKX | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | SYS_CLK1 | OSC1 |
| | | | | | FUNC_96M_AON_CLK | DPLL_PER |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | MLB_CLK | Module MLB |
| | | | | | MLBP_CLK | Module MLB |
| | MCASP5_FCLK | Func | 192 | MCASP5_AUX_GFCLK | PER_ABE_X1_GFCLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_ABE |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | MCASP5_ICLK | Int | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| McASP6 | MCASP6_AHCLKX | Func | 100 | MCASP6_AHCLKX | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | FUNC_96M_AON_CLK | DPLL_PER |
| | | | | | MLB_CLK | Module MLB |
| | | | | | MLBP_CLK | Module MLB |
| | | | | | SYS_CLK1 | OSC1 |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | MCASP6_FCLK | Func | 192 | MCASP6_AUX_GFCLK | PER_ABE_X1_GFCLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_ABE |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | MCASP6_ICLK | Int | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |


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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| McASP7 | MCASP7_AHCLKX | Func | 100 | MCASP7_AHCLKX | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | SYS_CLK1 | OSC1 |
| | | | | | FUNC_96M_AON_CLK | DPLL_PER |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | MLB_CLK | Module MLB |
| | | | | | MLBP_CLK | Module MLB |
| | MCASP7_FCLK | Func | 192 | MCASP7_AUX_GFCLK | PER_ABE_X1_GFCLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_ABE |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | MCASP7_ICLK | Int | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| McASP8 | MCASP8_AHCLKX | Func | 100 | MCASP8_AHCLKX | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | SYS_CLK1 | OSC1 |
| | | | | | FUNC_96M_AON_CLK | DPLL_PER |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | MLB_CLK | Module MLB |
| | | | | | MLBP_CLK | Module MLB |
| | MCASP8_FCLK | Func | 192 | MCASP8_AUX_GFCLK | PER_ABE_X1_GFCLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_ABE |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | MCASP8_ICLK | Int | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| McSPI1 | SPI1_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | SPI1_FCLK | Func | 48 | PER_48M_GFCLK | PER_48M_GFCLK | DPLL_PER |
| McSPI2 | SPI2_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | SPI2_FCLK | Func | 48 | PER_48M_GFCLK | PER_48M_GFCLK | DPLL_PER |
| McSPI3 | SPI3_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | SPI3_FCLK | Func | 48 | PER_48M_GFCLK | PER_48M_GFCLK | DPLL_PER |
| McSPI4 | SPI4_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | SPI4_FCLK | Func | 48 | PER_48M_GFCLK | PER_48M_GFCLK | DPLL_PER |
| MLB_SS | MLB_L3_ICLK | Int | 266 | MLB_SHB_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | MLB_L4_ICLK | Int | 133 | MLB_SPB_L4_GICLK | CORE_X2_CLK | DPLL_CORE |
| | MLB_FCLK | Func | 266 | MLB_SYS_L3_GFCLK | CORE_X2_CLK | DPLL_CORE |
| MMC1 | MMC1_CLK_32K | Func | 0.032 | L3INIT_32K_GFCLK | FUNC_32K_CLK | OSC1 |
| | MMC1_FCLK | Func | 192 | MMC1_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | | | 128 | | FUNC_256M_CLK | DPLL_PER |
| | MMC1_ICLK1 | Int | 266 | L3INIT_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | MMC1_ICLK2 | Int | 133 | L3INIT_L4_GICLK | CORE_X2_CLK | DPLL_CORE |

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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| MMC2 | MMC2_CLK_32K | Func | 0.032 | L3INIT_32K_GFCLK | FUNC_32K_CLK | OSC1 |
| | MMC2_FCLK | Func | 192 | MMC2_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | | | 128 | | FUNC_256M_CLK | DPLL_PER |
| | MMC2_ICLK1 | Int | 266 | L3INIT_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | MMC2_ICLK2 | Int | 133 | L3INIT_L4_GICLK | CORE_X2_CLK | DPLL_CORE |
| MMC3 | MMC3_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | MMC3_CLK_32K | Func | 0.032 | L4PER_32K_GFCLK | FUNC_32K_CLK | OSC1 |
| | MMC3_FCLK | Func | 48 | MMC3_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | | | 192 | | | |
| MMC4 | MMC4_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | MMC4_CLK_32K | Func | 0.032 | L4PER_32K_GFCLK | FUNC_32K_CLK | OSC1 |
| | MMC4_FCLK | Func | 48 | MMC4_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | | | 192 | | | |
| MMU_EDMA | MMU1_CLK | Int | 266 | L3MAIN1_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MMU_PCIESS | MMU2_CLK | Int | 266 | L3MAIN1_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| MPU | MPU_CLK | Int & Func | MPU_CLK | MPU_GCLK | MPU_GCLK | DPLL_MPU |
| MPU_EMU_DBG | FCLK | Int | 38.4 | EMU_SYS_CLK | SYS_CLK1 | OSC1 |
| | | | | | MPU_GCLK | DPLL_MPU |
| OCMC_RAM1 | OCMC1_L3_CLK | Int | 266 | L3MAIN1_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| OCMC_RAM2 | OCMC2_L3_CLK | Int | 266 | L3MAIN1_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| OCMC_RAM3 | OCMC3_L3_CLK | Int | 266 | L3MAIN1_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| OCMC_ROM | OCMC_L3_CLK | Int | 266 | L3MAIN1_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| OCP_WP_NOC | PICLKOCPL3 | Int | 266 | L3INSTR_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| OCP2SCP1 | L4CFG1_ADAPTER_CLKIN | Int | 133 | L3INIT_L4_GICLK | CORE_X2_CLK | DPLL_CORE |
| OCP2SCP2 | L4CFG2_ADAPTER_CLKIN | Int | 133 | L4CFG_L4_GICLK | CORE_X2_CLK | DPLL_CORE |
| OCP2SCP3 | L4CFG3_ADAPTER_CLKIN | Int | 133 | L3INIT_L4_GICLK | CORE_X2_CLK | DPLL_CORE |
| PCIe_SS1 | PCIE1_PHY_WKUP_CLK | Func | 0.032 | PCIE_32K_GFCLK | FUNC_32K_CLK | RTC Oscillator |
| | PCIe_SS1_FICLK | Int | 266 | PCIE_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | PCIEPHY_CLK | Func | 2500 | PCIE_PHY_GCLK | PCIE_PHY_GCLK | APLL_PCIE |
| | PCIEPHY_CLK_DIV | Func | 1250 | PCIE_PHY_DIV_GCLK | PCIE_PHY_DIV_GCLK | APLL_PCIE |
| | PCIE1_REF_CLKIN | Func | 34.3 | PCIE_REF_GFCLK | CORE_USB_OTG_SS_LFPS_TX_CLK | DPLL_CORE |
| | PCIE1_PWR_CLK | Func | 38.4 | PCIE_SYS_GFCLK | SYS_CLK1 | OSC1 |
| PCIe_SS2 | PCIE2_PHY_WKUP_CLK | Func | 0.032 | PCIE_32K_GFCLK | FUNC_32K_CLK | RTC Oscillator |
| | PCIe_SS2_FICLK | Func | 266 | PCIE_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | PCIEPHY_CLK | Func | 2500 | PCIE_PHY_GCLK | PCIE_PHY_GCLK | APLL_PCIE |
| | PCIEPHY_CLK_DIV | Func | 1250 | PCIE_PHY_DIV_GCLK | PCIE_PHY_DIV_GCLK | APLL_PCIE |
| | PCIE2_REF_CLKIN | Func | 34.3 | PCIE_REF_GFCLK | CORE_USB_OTG_SS_LFPS_TX_CLK | DPLL_CORE |
| | PCIE2_PWR_CLK | Func | 38.4 | PCIE_SYS_GFCLK | SYS_CLK1 | OSC1 |


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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| **Instance Name** | **Input Clock Name** | **Clock Type** | **Max. Clock Allowed (MHz)** | **PRCM Clock Name** | **PLL / OSC / Source Clock Name** | **PLL / OSC / Source Name** |
| PRCM_MPU | 32K_CLK | Func | 0.032 | FUNC_32K_CLK | SYS_CLK1/610 | OSC1 |
| | SYS_CLK | Func | 38.4 | WKUPAON_ICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| PRU-ICSS1 | PRUSS1_IEP_CLK | Func | 200 | ICSS_IEP_CLK | ICSS_IEP_CLK | DPLL_GMAC |
| | PRUSS1_GICLK | Int | 200 | ICSS_CLK | ICSS_CLK | DPLL_GMAC |
| | PRUSS1_UART_GFCLK | Func | 192 | PER_192M_GFCLK | FUNC_192M_CLK | DPLL_PER |
| PRU-ICSS2 | PRUSS2_IEP_CLK | Func | 200 | ICSS_IEP_CLK | ICSS_IEP_CLK | DPLL_GMAC |
| | PRUSS2_GICLK | Int | 200 | ICSS_CLK | ICSS_CLK | DPLL_GMAC |
| | PRUSS2_UART_GFCLK | Func | 192 | PER_192M_GFCLK | FUNC_192M_CLK | DPLL_PER |
| PWMSS1 | PWMSS1_GICLK | Int & Func | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| PWMSS2 | PWMSS2_GICLK | Int & Func | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| PWMSS3 | PWMSS3_GICLK | Int & Func | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| QSPI | QSPI_ICLK | Int | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | QSPI_FCLK | Func | 128 | QSPI_GFCLK | FUNC_256M_CLK | DPLL_PER |
| | | | | | PER_QSPI_CLK | DPLL_PER |
| RNG | RNG_ICLK | Int | 266 | L4SEC_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| RTC_SS | RTC_ICLK | Int | 133 | RTC_L4_GICLK | CORE_X2_CLK | DPLL_CORE |
| | RTC_FCLK | Func | RTC_FCLK | RTC_AUX_CLK | FUNC_32K_CLK | RTC Oscillator |
| | | | | FUNC_32K_CLK | SYS_CLK1/610 | OSC1 |
| SAR_ROM | PRCM_ROM_CLOCK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| SATA | SATA_FICLK | Int | 266 | L3INIT_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | SATA_PMALIVE_FCLK | Func | 48 | L3INIT_48M_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | REF_CLK | Func | 38 | SATA_REF_GFCLK | SYS_CLK1 | OSC1 |
| SDMA | SDMA_FCLK | Int & Func | 266 | DMA_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| SHA2MD51 | SHAM_1_CLK | Int | 266 | L4SEC_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| SHA2MD52 | SHAM_2_CLK | Int | 266 | L4SEC_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| SL2 | IVA_GCLK | Int | IVA_GCLK | IVA_GCLK | IVA_GFCLK | DPLL_IVA |
| SMARTREFLEX_CORE | MCLK | Int | 133 | COREAON_L4_GICLK | CORE_X2_CLK | DPLL_CORE |
| | SYSCLK | Func | 38.4 | WKUPAON_ICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| SMARTREFLEX_DSPEVE | MCLK | Int | 133 | COREAON_L4_GICLK | CORE_X2_CLK | DPLL_CORE |
| | SYSCLK | Func | 38.4 | WKUPAON_ICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| SMARTREFLEX_GPU | MCLK | Int | 133 | COREAON_L4_GICLK | CORE_X2_CLK | DPLL_CORE |
| | SYSCLK | Func | 38.4 | WKUPAON_ICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| SMARTREFLEX_IVAHD | MCLK | Int | 133 | COREAON_L4_GICLK | CORE_X2_CLK | DPLL_CORE |
| | SYSCLK | Func | 38.4 | WKUPAON_ICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |

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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| SMARTREFLEX_MPU | MCLK | Int | 133 | COREAON_L4_GICLK | CORE_X2_CLK | DPLL_CORE |
| | SYSCLK | Func | 38.4 | WKUPAON_ICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| SPINLOCK | SPINLOCK_ICLK | Int | 266 | L4CFG_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| TIMER1 | TIMER1_ICLK | Int | 38.4 | WKUPAON_GICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | TIMER1_FCLK | Func | 100 | TIMER1_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| TIMER2 | TIMER2_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER2_FCLK | Func | 100 | TIMER2_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| TIMER3 | TIMER3_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER3_FCLK | Func | 100 | TIMER3_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |


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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| **Instance Name** | **Input Clock Name** | **Clock Type** | **Max. Clock Allowed (MHz)** | **PRCM Clock Name** | **PLL / OSC / Source Clock Name** | **PLL / OSC / Source Name** |
| TIMER4 | TIMER4_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER4_FCLK | Func | 100 | TIMER4_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| TIMER5 | TIMER5_ICLK | Int | 266 | IPU_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER5_FCLK | Func | 100 | TIMER5_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | | | | | CLKOUTMUX[0] | CLKOUTMUX[0] |
| TIMER6 | TIMER6_ICLK | Int | 266 | IPU_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER6_FCLK | Func | 100 | TIMER6_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | | | | | CLKOUTMUX[0] | CLKOUTMUX[0] |

**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| TIMER7 | TIMER7_ICLK | Int | 266 | IPU_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER7_FCLK | Func | 100 | TIMER7_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | | | | | CLKOUTMUX[0] | CLKOUTMUX[0] |
| TIMER8 | TIMER8_ICLK | Int | 266 | IPU_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER8_FCLK | Func | 100 | TIMER8_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| | | | | | CLKOUTMUX[0] | CLKOUTMUX[0] |
| TIMER9 | TIMER9_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER9_FCLK | Func | 100 | TIMER9_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |


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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| **Instance Name** | **Input Clock Name** | **Clock Type** | **Max. Clock Allowed (MHz)** | **PRCM Clock Name** | **PLL / OSC / Source Clock Name** | **PLL / OSC / Source Name** |
| TIMER10 | TIMER10_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER10_FCLK | Func | 100 | TIMER10_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| TIMER11 | TIMER11_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER11_FCLK | Func | 100 | TIMER11_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| TIMER12 | TIMER12_ICLK | Int | 38.4 | WKUPAON_GICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | TIMER12_FCLK | Func | 0.032 | OSC_32K_CLK | RC_CLK | RC oscillator |
| TIMER13 | TIMER13_ICLK | Int | 266 | L4PER3_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER13_FCLK | Func | 100 | TIMER13_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |

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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| TIMER14 | TIMER14_ICLK | Int | 266 | L4PER3_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER14_FCLK | Func | 100 | TIMER14_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| TIMER15 | TIMER15_ICLK | Int | 266 | L4PER3_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER15_FCLK | Func | 100 | TIMER15_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| TIMER16 | TIMER16_ICLK | Int | 266 | L4PER3_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | TIMER16_FCLK | Func | 100 | TIMER16_GFCLK | SYS_CLK1 | OSC1 |
| | | | | | FUNC_32K_CLK | OSC1 |
| | | | | | | RTC Oscillator |
| | | | | | SYS_CLK2 | OSC2 |
| | | | | | XREF_CLK0 | XREF_CLK0 |
| | | | | | XREF_CLK1 | XREF_CLK1 |
| | | | | | XREF_CLK2 | XREF_CLK2 |
| | | | | | XREF_CLK3 | XREF_CLK3 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | | | | | VIDEO1_CLK | DPLL_VIDEO1 |
| | | | | | VIDEO2_CLK | DPLL_VIDEO2 |
| | | | | | HDMI_CLK | DPLL_HDMI |
| TPCC | TPCC_GCLK | Int | 266 | L3MAIN1_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| TPTC1 | TPTC0_GCLK | Int | 266 | L3MAIN1_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| TPTC2 | TPTC1_GCLK | Int | 266 | L3MAIN1_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| UART1 | UART1_FCLK | Func | 48 | UART1_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | UART1_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| UART2 | UART2_FCLK | Func | 48 | UART2_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | UART2_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |


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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| UART3 | UART3_FCLK | Func | 48 | UART3_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | UART3_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| UART4 | UART4_FCLK | Func | 48 | UART4_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | UART4_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| UART5 | UART5_FCLK | Func | 48 | UART5_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | UART5_ICLK | Int | 266 | L4PER_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| UART6 | UART6_FCLK | Func | 48 | UART6_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | UART6_ICLK | Int | 266 | IPU_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| UART7 | UART7_FCLK | Func | 48 | UART7_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | UART7_ICLK | Int | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| UART8 | UART8_FCLK | Func | 48 | UART8_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | UART8_ICLK | Int | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| UART9 | UART9_FCLK | Func | 48 | UART9_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | UART9_ICLK | Int | 266 | L4PER2_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| UART10 | UART10_FCLK | Func | 48 | UART10_GFCLK | FUNC_192M_CLK | DPLL_PER |
| | UART10_ICLK | Int | 38.4 | WKUPAON_GICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| USB1 | USB1_MICLK | Int | 266 | L3INIT_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | USB3PHY_REF_CLK | Func | 34.3 | USB_LFPS_TX_GFCLK | CORE_USB_OTG_SS_LFPS_TX_CLK | DPLL_CORE |
| | USB2PHY1_TREF_CLK | Func | 38.4 | USB_OTG_SS_REF_CLK | SYS_CLK1 | OSC1 |
| | USB2PHY1_REF_CLK | Func | 960 | L3INIT_960M_GFCLK | L3INIT_960_GFCLK | DPLL_USB |
| USB2 | USB2_MICLK | Int | 266 | L3INIT_L3_GICLK | CORE_X2_CLK | DPLL_CORE |
| | USB2PHY2_TREF_CLK | Func | 38.4 | USB_OTG_SS_REF_CLK | SYS_CLK1 | OSC1 |
| | USB2PHY2_REF_CLK | Func | 960 | L3INIT_960M_GFCLK | L3INIT_960_GFCLK | DPLL_USB |
| USB_PHY1_CORE | USB2PHY1_WKUP_CLK | Func | 0.032 | COREAON_32K_GFCLK | SYS_CLK1/610 | OSC1 |
| USB_PHY2_CORE | USB2PHY2_WKUP_CLK | Func | 0.032 | COREAON_32K_GFCLK | SYS_CLK1/610 | OSC1 |
| USB_PHY3_CORE | USB3PHY_WKUP_CLK | Func | 0.032 | COREAON_32K_GFCLK | SYS_CLK1/610 | OSC1 |
| VIP1 | L3_CLK_PROC_CLK | Int & Func | 266 | VIP1_GCLK | CORE_X2_CLK | DPLL_CORE |
| | | | | | CORE_ISS_MAIN_CLK | DPLL_CORE |
| VIP2 | L3_CLK_PROC_CLK | Int & Func | 266 | VIP2_GCLK | CORE_X2_CLK | DPLL_CORE |
| | | | | | CORE_ISS_MAIN_CLK | DPLL_CORE |
| VIP3 | L3_CLK_PROC_CLK | Int & Func | 266 | VIP3_GCLK | CORE_X2_CLK | DPLL_CORE |
| | | | | | CORE_ISS_MAIN_CLK | DPLL_CORE |
| VPE | L3_CLK_PROC_CLK | Int & Func | 300 | VPE_GCLK | CORE_ISS_MAIN_CLK | DPLL_CORE |
| | | | | | VIDEO1_CLKOUT4 | DPLL_VIDEO1 |
| WD_TIMER1 | PIOCPCLK | Int | 38.4 | WKUPAON_GICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | PITIMERCLK | Func | 0.032 | OSC_32K_CLK | RC_CLK | RC oscillator |

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**Table 5-9. Maximum Supported Frequency (continued)**

| Module | | | | Clock Sources | | |
|---|---|---|---|---|---|---|
| Instance Name | Input Clock Name | Clock Type | Max. Clock Allowed (MHz) | PRCM Clock Name | PLL / OSC / Source Clock Name | PLL / OSC / Source Name |
| WD_TIMER2 | WD_TIMER2_ICLK | Int | 38.4 | WKUPAON_GICLK | SYS_CLK1 | OSC1 |
| | | | | | DPLL_ABE_X2_CLK | DPLL_ABE |
| | WD_TIMER2_FCLK | Func | 0.032 | WKUPAON_SYS_GFCLK | WKUPAON_32K_GFCLK | RTC Oscillator |

## 5.6 Power Consumption Summary

**NOTE**

Maximum power consumption for this SoC depends on the specific use conditions for the end system. Contact your TI representative for assistance in estimating maximum power consumption for the end system use case.

## 5.7 Electrical Characteristics

**NOTE**

The data specified in Section 5.7.1 through Section 5.7.12 are subject to change.

**NOTE**

The interfaces or signals described in Section 5.7.1 through Section 5.7.12 correspond to the interfaces or signals available in multiplexing mode 0 (Function 1).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY/GPIO combination in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

### *5.7.1 LVCMOS DDR DC Electrical Characteristics*

Table 5-10 summarizes the DC electrical characteristics for LVCMOS DDR Buffers.

**NOTE**

For more information on the I/O cell configurations (i[2:0], sr[1:0]), see the Chapter *Control Module* of the Device TRM.


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## Table 5-10. LVCMOS DDR DC Electrical Characteristics

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Signal Names in MUXMODE 0 (Single-Ended Signals):** ddr1_d[31:0], ddr1_a[15:0], ddr1_dqm[3:0], ddr1_ba[2:0], ddr1_csn[0], ddr1_cke, ddr1_odt[0], ddr1_casn, ddr1_rasn, ddr1_wen, ddr1_rst, ddr1_ecc_d[7:0], ddr1_dqm_ecc, ddr2_d[31:0], ddr2_a[15:0], ddr2_dqm[3:0], ddr2_ba[2:0], ddr2_csn[0], ddr2_cke, ddr2_odt[0], ddr2_casn, ddr2_rasn, ddr2_wen, ddr2_rst; | | | | | | |
| **Balls:** AA28 / AA25 / AA26 / Y24 / AA24 / Y23 / Y22 / AA23 / Y20 / AB27 / Y19 / AC27 / AC28 / AB28 / W20 / V20 / AD25 / AC24 / AC25 / AE26 / AF28 / AG27 / AF27 / AC23 / AE23 / AF23 / AE24 / AF24 / AH26 / AG26 / AF26 / AF25 / AD18 / AE17 / AF18 / AC21 / AD22 / AD21 / AE22 / AF22 / AE21 / AE21 / AH22 / AF21 / AB19 / AC20 / AC19 / AD20 / AA27 / AC26 / AB23 / AD23 / AB18 / AE18 / AF17 / AH23 / AG22 / AE20 / AC18 / AF20 / AH21 / AG21 / Y26 / V25 / V24 / Y25 / W23 / W19 / V23 / W22 / V26 / M26 / M25 / M24 / M23 / L28 / L25 / L26 / L27 / J20 / K22 / J23 / L24 / L23 / K21 / K20 / L22 / J24 / J26 / J25 / G26 / H26 / H24 / H25 / H23 / E28 / E27 / F27 / F26 / F24 / F25 / G25 / E26 / U22 / R22 / T22 / N28 / P26 / N23 / N27 / P27 / N20 / P25 / P22 / P23 / R27 / R28 / R26 / R25 / M22 / K23 / G24 / F28 / U26 / U27 / U23 / P24 / U24 / R23 / U28 / T23 / U25 / R24; | | | | | | |
| **Driver Mode** | | | | | | |
| $V_{OH}$ | High-level output threshold ($I_{OH}$ = 0.1 mA) | | 0.9*VDDS | | | V |
| $V_{OL}$ | Low-level output threshold ($I_{OL}$ = 0.1 mA) | | | | 0.1*VDDS | V |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | | 3 | pF |
| $Z_O$ | Output impedance (drive strength) | I[2:0] = 000 (Imp80) | | 80 | | Ω |
| | | I[2:0] = 001 (Imp60) | | 60 | | |
| | | I[2:0] = 010 (Imp48) | | 48 | | |
| | | I[2:0] = 011 (Imp40) | | 40 | | |
| | | I[2:0] = 100 (Imp34) | | 34 | | |
| **Single-Ended Receiver Mode** | | | | | | |
| $V_{IH}$ | High-level input threshold | DDR3/DDR3L | VREF+0.1 | | VDDS+0.2 | V |
| $V_{IL}$ | Low-level input threshold | DDR3/DDR3L | -0.2 | | VREF-0.1 | V |
| $V_{CM}$ | Input common-mode voltage | | VREF -10%vdds | | VREF+ 10%vdds | V |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | | 3 | pF |
| **Signal Names in MUXMODE 0 (Differential Signals):** ddr1_dqs[3:0], ddr1_dqsn[3:0], ddr1_ck, ddr1_nck, ddr2_dqs[3:0], ddr2_dqsn[3:0], ddr2_ck, ddr2_nck, ddr1_dqs_ecc, ddr1_dqsn_ecc; | | | | | | |
| **Bottom Balls:** Y28 / AD27 / AE27 / AH25 / Y27 / AD28 / AE28 / AG25 / AG24 / AH24 / M28 / K27 / H27 / G28 / M27 / K28 / H28 / G27 / T28 / T27 / V27 / V28; | | | | | | |
| **Driver Mode** | | | | | | |
| $V_{OH}$ | High-level output threshold ($I_{OH}$ = 0.1 mA) | | 0.9*VDDS | | | V |
| $V_{OL}$ | Low-level output threshold ($I_{OL}$ = 0.1 mA) | | | | 0.1*VDDS | V |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | | 3 | pF |
| $Z_O$ | Output impedance (drive strength) | I[2:0] = 000 (Imp80) | | 80 | | Ω |
| | | I[2:0] = 001 (Imp60) | | 60 | | |
| | | I[2:0] = 010 (Imp48) | | 48 | | |
| | | I[2:0] = 011 (Imp40) | | 40 | | |
| | | I[2:0] = 100 (Imp34) | | 34 | | |
| **Single-Ended Receiver Mode** | | | | | | |
| $V_{IH}$ | High-level input threshold | DDR3/DDR3L | VREF+0.1 | | VDDS+0.2 | V |
| $V_{IL}$ | Low-level input threshold | DDR3/DDR3L | -0.2 | | VREF-0.1 | V |
| $V_{CM}$ | Input common-mode voltage | | VREF -10%vdds | | VREF+ 10%vdds | V |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | | 3 | pF |

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**Table 5-10. LVCMOS DDR DC Electrical Characteristics (continued)**

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Differential Receiver Mode** | | | | | | |
| $V_{SWING}$ | Input voltage swing | DDR3/DDR3L | 0.2 | | vdds+0.4 | V |
| $V_{CM}$ | Input common-mode voltage | | VREF -10%vdds | | VREF+ 10%vdds | |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | | 3 | pF |

(1) VDDS stands for corresponding power supply (that is vdds_ddr1 or vdds_ddr2). For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [11] column.

(2) VREF in this table stands for corresponding Reference Power Supply (that is ddr1_vref0 or ddr2_vref0). For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [11] column.

### 5.7.2 HDMIPHY DC Electrical Characteristics

The HDMIPHY DC Electrical Characteristics are compliant with the HDMI 1.4a specification and are not reproduced here.

### 5.7.3 Dual Voltage LVCMOS I²C DC Electrical Characteristics

Table 5-11 summarizes the DC electrical characteristics for Dual Voltage LVCMOS I2C Buffers.

**NOTE**

For more information on the I/O cell configurations, see the Control Module section of the Device TRM.

**Table 5-11. Dual Voltage LVCMOS I2C DC Electrical Characteristics**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **Signal Names in MUXMODE 0:** i2c2_scl, i2c1_scl, i2c1_sda, i2c2_sda; | | | | | |
| **Balls:** F17 / C20 / C21 / C25; | | | | | |
| **I²C Standard Mode – 1.8 V** | | | | | |
| $V_{IH}$ | Input high-level threshold | 0.7*VDDS | | | V |
| $V_{IL}$ | Input low-level threshold | | | 0.3*VDDS | V |
| $V_{hys}$ | Hysteresis | 0.1*VDDS | | | V |
| $I_{IN}$ | Input current at each I/O pin with an input voltage between 0.1*VDDS to 0.9*VDDS | | | 12 | µA |
| $I_{OZ}$ | $I_{OZ}$($I_{PAD}$ Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as $I_{OZ}$ | | | 12 | µA |
| $C_{IN}$ | Input capacitance | | | 10 | pF |
| $V_{OL3}$ | Output low-level threshold open-drain at 3-mA sink current | | | 0.2*VDDS | V |
| $I_{OLmin}$ | Low-level output current @$V_{OL}$=0.2*VDDS | 3 | | | mA |
| $t_{OF}$ | Output fall time from $V_{IHmin}$ to $V_{ILmax}$ with a bus capacitance CB from 5 pF to 400 pF | | | 250 | ns |
| **I²C Fast Mode – 1.8 V** | | | | | |
| $V_{IH}$ | Input high-level threshold | 0.7*VDDS | | | V |
| $V_{IL}$ | Input low-level threshold | | | 0.3*VDDS | V |
| $V_{hys}$ | Hysteresis | 0.1*VDDS | | | V |
| $I_{IN}$ | Input current at each I/O pin with an input voltage between 0.1*VDDS to 0.9*VDDS | | | 12 | µA |


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### Table 5-11. Dual Voltage LVCMOS I2C DC Electrical Characteristics (continued)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{OZ}$ | $I_{OZ}$($I_{PAD}$ Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as $I_{OZ}$ | | | 12 | µA |
| $C_{IN}$ | Input capacitance | | | 10 | pF |
| $V_{OL3}$ | Output low-level threshold open-drain at 3-mA sink current | | | 0.2*VDDS | V |
| $I_{OLmin}$ | Low-level output current @$V_{OL}$=0.2*VDDS | 3 | | | mA |
| $t_{OF}$ | Output fall time from $V_{IHmin}$ to $V_{ILmax}$ with a bus capacitance CB from 10 pF to 400 pF | 20+0.1*Cb | | 250 | ns |
| **$I^2C$ Standard Mode – 3.3 V** | | | | | |
| $V_{IH}$ | Input high-level threshold | 0.7*VDDS | | | V |
| $V_{IL}$ | Input low-level threshold | | | 0.3*VDDS | V |
| $V_{hys}$ | Hysteresis | 0.05*VDDS | | | V |
| $I_{IN}$ | Input current at each I/O pin with an input voltage between 0.1*VDDS to 0.9*VDDS | 31 | | 80 | µA |
| $I_{OZ}$ | $I_{OZ}$($I_{PAD}$ Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as $I_{OZ}$ | 31 | | 80 | µA |
| $C_{IN}$ | Input capacitance | | | 10 | pF |
| $V_{OL3}$ | Output low-level threshold open-drain at 3-mA sink current | | | 0.4 | V |
| $I_{OLmin}$ | Low-level output current @$V_{OL}$=0.4V | 3 | | | mA |
| $I_{OLmin}$ | Low-level output current @$V_{OL}$=0.6V for full drive load (400pF/400KHz) | 6 | | | mA |
| $t_{OF}$ | Output fall time from VIHmin to VILmax with a bus capacitance CB from 5 pF to 400 pF | | | 250 | ns |
| **$I^2C$ Fast Mode – 3.3 V** | | | | | |
| $V_{IH}$ | Input high-level threshold | 0.7*VDDS | | | V |
| $V_{IL}$ | Input low-level threshold | | | 0.3*VDDS | V |
| $V_{hys}$ | Hysteresis | 0.05*VDDS | | | V |
| $I_{IN}$ | Input current at each I/O pin with an input voltage between 0.1*VDDS to 0.9*VDDSS | 31 | | 80 | µA |
| $I_{OZ}$ | $I_{OZ}$($I_{PAD}$ Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as $I_{OZ}$ | 31 | | 80 | µA |
| $C_{IN}$ | Input capacitance | | | 10 | pF |
| $V_{OL3}$ | Output low-level threshold open-drain at 3-mA sink current | | | 0.4 | V |
| $I_{OLmin}$ | Low-level output current @$V_{OL}$=0.4V | 3 | | | mA |
| $I_{OLmin}$ | Low-level output current @$V_{OL}$=0.6V for full drive load (400pF/400KHz) | 6 | | | mA |
| $t_{OF}$ | Output fall time from $V_{IHmin}$ to $V_{ILmax}$ with a bus capacitance CB from 10 pF to 200 pF (Proper External Resistor Value should be used as per I2C spec) | 20+0.1*Cb | | 250 | ns |
| | Output fall time from $V_{IHmin}$ to $V_{ILmax}$ with a bus capacitance CB from 300 pF to 400 pF (Proper External Resistor Value should be used as per I2C spec) | 40 | | 290 | |

(1) VDDS stands for corresponding power supply (that is vddshv3). For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [11] column.

### 5.7.4 IQ1833 Buffers DC Electrical Characteristics

Table 5-12 summarizes the DC electrical characteristics for IQ1833 Buffers.

**Table 5-12. IQ1833 Buffers DC Electrical Characteristics**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **Signal Names in MUXMODE 0:** tclk; | | | | | |
| **Balls:** E20; | | | | | |
| **1.8-V Mode** | | | | | |
| $V_{IH}$ | Input high-level threshold (Does not meet JEDEC $V_{IH}$) | 0.75 * VDDS | | | V |
| $V_{IL}$ | Input low-level threshold (Does not meet JEDEC $V_{IL}$) | | | 0.25 * VDDS | V |
| $V_{HYS}$ | Input hysteresis voltage | 100 | | | mV |
| $I_{IN}$ | Input current at each I/O pin | 2 | | 11 | µA |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | 1 | pF |
| **3.3-V Mode** | | | | | |
| $V_{IH}$ | Input high-level threshold (Does not meet JEDEC $V_{IH}$) | 2.0 | | | V |
| $V_{IL}$ | Input low-level threshold (Does not meet JEDEC $V_{IL}$) | | | 0.6 | V |
| $V_{HYS}$ | Input hysteresis voltage | 400 | | | mV |
| $I_{IN}$ | Input current at each I/O pin | 5 | | 11 | µA |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | 1 | pF |

(1) VDDS stands for corresponding power supply (that is vddshv3). For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [11] column.

### 5.7.5 IHHV1833 Buffers DC Electrical Characteristics

Table 5-13 summarizes the DC electrical characteristics for IHHV1833 Buffers.

**Table 5-13. IHHV1833 Buffers DC Electrical Characteristics**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **Signal Names in MUXMODE 0:** porz, rtc_iso, rtc_porz, wakeup [3:0]; | | | | | |
| **Balls:** F22 / AF14 / AB17 / AD17 / AC17 / AB16 / AC16; | | | | | |
| **1.8-V Mode** | | | | | |
| $V_{IH}$ | Input high-level threshold | 1.2[(1)] | | | V |
| $V_{IL}$ | Input low-level threshold | | | 0.4 | V |
| $V_{HYS}$ | Input hysteresis voltage | 40 | | | mV |
| $I_{IN}$ | Input current at each I/O pin | 0.02 | | 1 | µA |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | 1 | pF |
| **3.3-V Mode** | | | | | |
| $V_{IH}$ | Input high-level threshold | 1.2[(1)] | | | V |
| $V_{IL}$ | Input low-level threshold | | | 0.4 | V |
| $V_{HYS}$ | Input hysteresis voltage | 40 | | | mV |
| $I_{IN}$ | Input current at each I/O pin | 5 | | 8 | µA |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | 1 | pF |


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(1) The IHHV1833 buffer exists in the dual-voltage IO logic that can be powered by either 1.8V or 3.3V provided by vddshv3. However, the vddshv3 supply is only used for input protection circuitry, not for logic functionality. The logic in this buffer operates entirely on the vdds18v supply. Therefore, IHHV control is asserted whenever the input is low and vdds18v is valid.

### 5.7.6 LVCMOS OSC Buffers DC Electrical Characteristics

Table 5-14 summarizes the DC electrical characteristics for LVCMOS OSC Buffers.

**Table 5-14. LVCMOS OSC Buffers DC Electrical Characteristics**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **Signal Names in MUXMODE 0:** rtc_osc_xi_clkin32 / rtc_osc_xo; | | | | | |
| **Balls:** AE14 / AD14; | | | | | |
| **1.8-V Mode** | | | | | |
| $V_{IH}$ | Input high-level threshold | 0.65 * VDDS | | | V |
| $V_{IL}$ | Input low-level threshold | | | 0.35 * VDDS | V |
| $V_{HYS}$ | Input hysteresis voltage | 150 | | | mV |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | 3 | pF |

(1) VDDS stands for corresponding power supply (that is vdda_rtc). For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [11] column.

### 5.7.7 BC1833IHHV Buffers DC Electrical Characteristics

Table 5-15 summarizes the DC electrical characteristics for BC1833IHHV Buffers.

**Table 5-15. BC1833IHHV Buffers DC Electrical Characteristics**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **Signal Names in MUXMODE 0:** on_off; | | | | | |
| **Balls:** Y11; | | | | | |
| **1.8-V Mode** | | | | | |
| $V_{OH}$ | Output high-level threshold ($I_{OH}$ = 2 mA) | VDDS-0.45 | | | V |
| $V_{OL}$ | Output low-level threshold ($I_{OL}$ = 2 mA) | | | 0.45 | V |
| $I_{DRIVE}$ | Pin Drive strength at PAD Voltage = 0.45V or VDDS-0.45V | 6 | | | mA |
| $I_{IN}$ | Input current at each I/O pin | 6 | | 12 | µA |
| $I_{OZ}$ | $I_{OZ}$($I_{PAD}$ Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as $I_{OZ}$ | | | 6 | µA |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | 4 | pF |
| **3.3-V Mode** | | | | | |
| $V_{OH}$ | Output high-level threshold ($I_{OH}$ =100 µA) | VDDS-0.2 | | | V |
| $V_{OL}$ | Output low-level threshold ($I_{OL}$ = 100 µA) | | | 0.2 | V |
| $I_{DRIVE}$ | Pin Drive strength at PAD Voltage = 0.45V or VDDS-0.45V | 6 | | | mA |
| $I_{IN}$ | Input current at each I/O pin | | | 60 | µA |
| $I_{OZ}$ | $I_{OZ}$($I_{PAD}$ Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as $I_{OZ}$ | | | 60 | µA |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | 4 | pF |

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(1) VDDS stands for corresponding power supply (that is vddshv5). For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [11] column.

### 5.7.8 USBPHY DC Electrical Characteristics

**NOTE**

USB1 instance is compliant with the USB3.0 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the USB3.0 Specification Rev 1.0 dated June 6, 2011.

**NOTE**

USB1 and USB2 Electrical Characteristics are compliant with USB2.0 Specification Rev 2.0 dated April 27, 2000 including ECNs and Errata as applicable.

### 5.7.9 Dual Voltage SDIO1833 DC Electrical Characteristics

Table 5-16 summarizes the DC electrical characteristics for Dual Voltage SDIO1833 Buffers.

**Table 5-16. Dual Voltage SDIO1833 DC Electrical Characteristics**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **Signal Names in Mode 0:** mmc1_clk, mmc1_cmd, mmc1_data[3:0]; | | | | | |
| **Bottom Balls:** W6 / Y6 / AA6 / Y4 / AA5 / Y3; | | | | | |
| **1.8-V Mode** | | | | | |
| $V_{IH}$ | Input high-level threshold | 1.27 | | | V |
| $V_{IL}$ | Input low-level threshold | | | 0.58 | V |
| $V_{HYS}$ | Input hysteresis voltage | 50 (2) | | | mV |
| $I_{IN}$ | Input current at each I/O pin | | | 30 | µA |
| $I_{OZ}$ | $I_{OZ}$($I_{PAD}$ Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max(I(PAD)) is measured and is reported as $I_{OZ}$ | | | 30 | µA |
| $I_{IN\ with\ pulldown\ enabled}$ | Input current at each I/O pin with weak pulldown enabled measured when PAD = VDDS | 50 | 120 | 210 | µA |
| $I_{IN\ with\ pullup\ enabled}$ | Input current at each I/O pin with weak pullup enabled measured when PAD = 0 | 60 | 120 | 200 | µA |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | 5 | pF |
| $V_{OH}$ | Output high-level threshold ($I_{OH}$ = 2 mA) | 1.4 | | | V |
| $V_{OL}$ | Output low-level threshold ($I_{OL}$ = 2 mA) | | | 0.45 | V |
| **3.3-V Mode** | | | | | |
| $V_{IH}$ | Input high-level threshold | 0.625 × VDDS | | | V |
| $V_{IL}$ | Input low-level threshold | | | 0.25 × VDDS | V |
| $V_{HYS}$ | Input hysteresis voltage | 40 (2) | | | mV |
| $I_{IN}$ | Input current at each I/O pin | | | 110 | µA |
| $I_{OZ}$ | $I_{OZ}$($I_{PAD}$ Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max(I(PAD)) is measured and is reported as $I_{OZ}$ | | | 110 | µA |
| $I_{IN\ with\ pulldown\ enabled}$ | Input current at each I/O pin with weak pulldown enabled measured when PAD = VDDS | 40 | 100 | 290 | µA |


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**Table 5-16. Dual Voltage SDIO1833 DC Electrical Characteristics (continued)**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{IN\ with\ pullup\ enabled}$ | Input current at each I/O pin with weak pullup enabled measured when PAD = 0 | 10 | 100 | 290 | µA |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | 5 | pF |
| $V_{OH}$ | Output high-level threshold ($I_{OH}$ = 2 mA) | 0.75 × VDDS | | | V |
| $V_{OL}$ | Output low-level threshold ($I_{OL}$ = 2 mA) | | | 0.125 × VDDS | V |

(1) VDDS stands for corresponding power supply (that is vddshv8). For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [11] column.

(2) Hysteresis is enabled/disabled with CTRL_CORE_CONTROL_HYST_1.SDCARD_HYST register.

### 5.7.10 Dual Voltage LVCMOS DC Electrical Characteristics

Table 5-17 summarizes the DC electrical characteristics for Dual Voltage LVCMOS Buffers.

**Table 5-17. Dual Voltage LVCMOS DC Electrical Characteristics**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **1.8-V Mode** | | | | | |
| $V_{IH}$ | Input high-level threshold | 0.65*VDDS | | | V |
| $V_{IL}$ | Input low-level threshold | | | 0.35*VDDS | V |
| $V_{HYS}$ | Input hysteresis voltage | 100 | | | mV |
| $V_{OH}$ | Output high-level threshold ($I_{OH}$ = 2 mA) | VDDS-0.45 | | | V |
| $V_{OL}$ | Output low-level threshold ($I_{OL}$ = 2 mA) | | | 0.45 | V |
| $I_{DRIVE}$ | Pin Drive strength at PAD Voltage = 0.45V or VDDS-0.45V | 6 | | | mA |
| $I_{IN}$ | Input current at each I/O pin | | | 16 | µA |
| $I_{OZ}$ | $I_{OZ}$($I_{PAD}$ Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as $I_{OZ}$ | | | 16 | µA |
| $I_{IN\ with\ pulldown\ enabled}$ | Input current at each I/O pin with weak pulldown enabled measured when PAD = VDDS | 50 | 120 | 210 | µA |
| $I_{IN\ with\ pullup\ enabled}$ | Input current at each I/O pin with weak pullup enabled measured when PAD = 0 | 60 | 120 | 200 | µA |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | 4 | pF |
| $Z_O$ | Output impedance (drive strength) | | 40 | | Ω |
| **3.3-V Mode** | | | | | |
| $V_{IH}$ | Input high-level threshold | 2 | | | V |
| $V_{IL}$ | Input low-level threshold | | | 0.8 | V |
| $V_{HYS}$ | Input hysteresis voltage | 200 | | | mV |
| $V_{OH}$ | Output high-level threshold ($I_{OH}$ =100µA) | VDDS-0.2 | | | V |
| $V_{OL}$ | Output low-level threshold ($I_{OL}$ = 100µA) | | | 0.2 | V |
| $I_{DRIVE}$ | Pin Drive strength at PAD Voltage = 0.45V or VDDS-0.45V | 6 | | | mA |
| $I_{IN}$ | Input current at each I/O pin | | | 65 | µA |
| $I_{OZ}$ | $I_{OZ}$($I_{PAD}$ Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as $I_{OZ}$ | | | 65 | µA |
| $I_{IN\ with\ pulldown\ enabled}$ | Input current at each I/O pin with weak pulldown enabled measured when PAD = VDDS | 40 | 100 | 200 | µA |

**Table 5-17. Dual Voltage LVCMOS DC Electrical Characteristics (continued)**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{IN\ with\ pullup\ enabled}$ | Input current at each I/O pin with weak pullup enabled measured when PAD = 0 | 10 | 100 | 290 | µA |
| $C_{PAD}$ | Pad capacitance (including package capacitance) | | | 4 | pF |
| $Z_O$ | Output impedance (drive strength) | | 40 | | Ω |

(1) VDDS stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [11] column.

### 5.7.11 SATAPHY DC Electrical Characteristics

**NOTE**

The SATA module is compliant with the electrical parameters specified in the *SATA-IO SATA Specification*, Revision 3.2, August 7, 2013.

### 5.7.12 PCIEPHY DC Electrical Characteristics

**NOTE**

The PCIe interfaces are compliant with the electrical parameters specified in PCI Express Base Specification Revision 3.0.

## 5.8 Thermal Characteristics

For reliability and operability concerns, the maximum junction temperature of the Device has to be at or below the $T_J$ value identified in Table 5-4, *Recommended Operating Conditions*.

It is recommended to perform thermal simulations at the system level with the worst case device power consumption.

### 5.8.1 Package Thermal Characteristics

Table 5-18 provides the thermal resistance characteristics for the package used on this device.

**NOTE**

Power dissipation of 1.5 W and an ambient temperature of 85ºC is assumed for ABC package.

**Table 5-18. Thermal Resistance Characteristics (ABC Package)**

| NO. | PARAMETER | DESCRIPTION | °C/W[(1)] | AIR FLOW (m/s)[(2)] |
|---|---|---|---|---|
| T1 | $R\Theta_{JC}$ | Junction-to-case | 0.82 | N/A |
| T2 | $R\Theta_{JB}$ | Junction-to-board | 3.78 | N/A |
| T3 | $R\Theta_{JA}$ | Junction-to-free air | 11.1 | 0 |
| T4 | | Junction-to-moving air | 8.8 | 1 |
| T5 | | | 8.0 | 2 |
| T6 | | | 7.5 | 3 |
| T7 | $\Psi_{JT}$ | Junction-to-package top | 0.62 | 0 |
| T8 | | | 0.66 | 1 |
| T9 | | | 0.66 | 2 |
| T10 | | | 0.66 | 3 |


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**Table 5-18. Thermal Resistance Characteristics (ABC Package) (continued)**

| NO. | PARAMETER | DESCRIPTION | °C/W[(1)] | AIR FLOW (m/s)[(2)] |
|---|---|---|---|---|
| T11 | $\Psi_{JB}$ | Junction-to-board | 3.43 | 0 |
| T12 | | | 3.22 | 1 |
| T13 | | | 3.12 | 2 |
| T14 | | | 3.04 | 3 |

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second

## 5.9 Power Supply Sequences

This section describes the power-up and power-down sequence required to ensure proper device operation. The power supply names described in this section comprise a superset of a family of compatible devices. Some members of this family will not include a subset of these power supplies and their associated device modules. Refer to the Section 4.2, *Ball Characteristics* of the Section 4, *Terminal Configuration and Functions* to determine which power supplies are applicable.

**NOTE**

RTC only mode is not supported feature.


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Figure 5-2 and Figure 5-3 describe the device Power Sequencing when RTC-mode is NOT used.

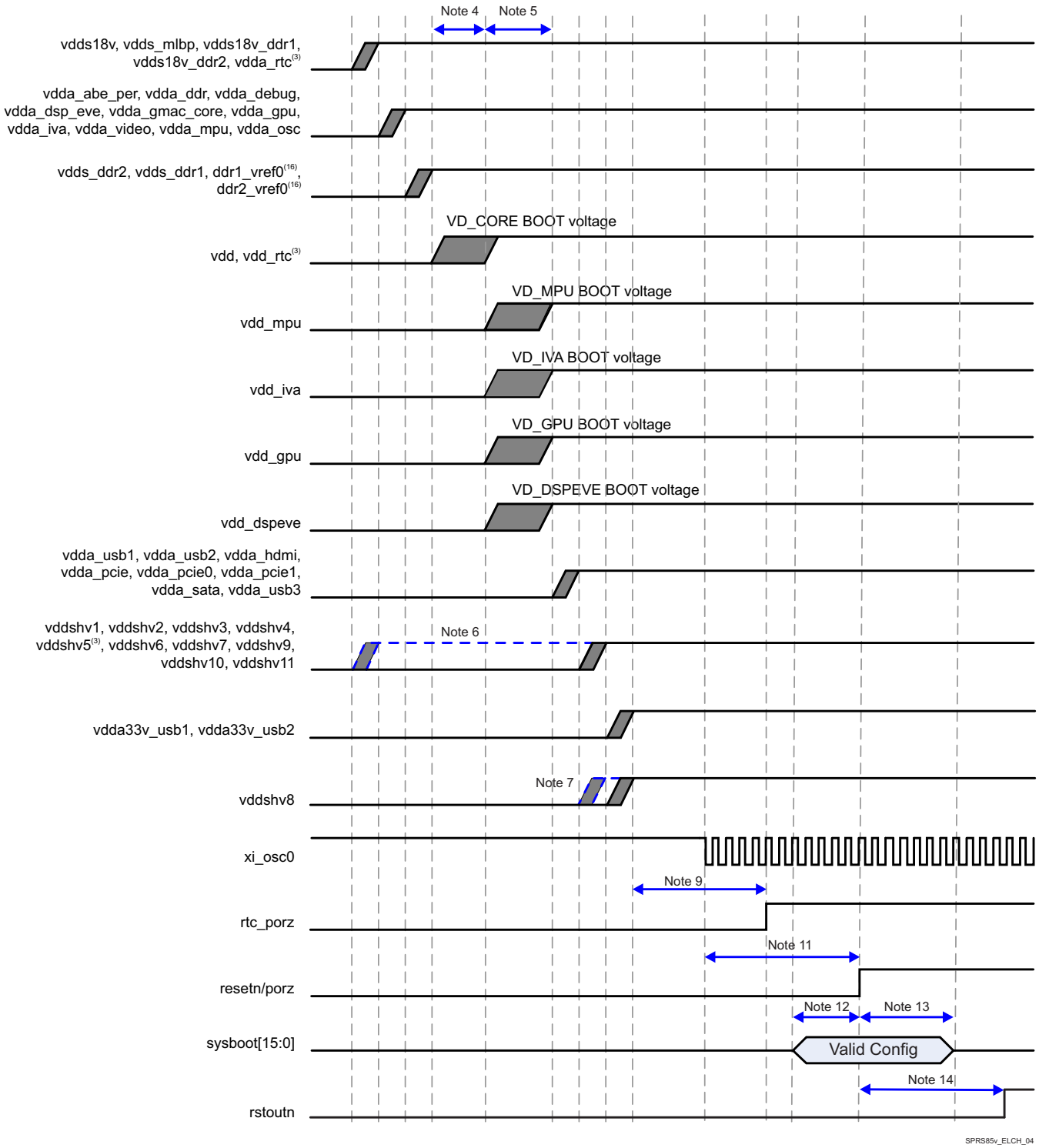


**Figure 5-2. Power-Up Sequencing**

(1) Grey shaded areas are windows where it is valid to ramp the voltage rail.

(2) Blue dashed lines are not valid windows but show alternate ramp possibilities based on the associated note.

(3) If RTC-only mode is not used then the following combinations are approved:
- vdda_rtc can be combined with vdds18v
- vdd_rtc can be combined with vdd

- vddshv5 can be combined with other 1.8V or 3.3V vddshvn rails.
If combinations listed above are not followed then sequencing for these 3 voltage rails should follow the RTC mode timing requirements.
When using RTC mode timing:
- vdda_rtc rises coincident with, or before, the 1.8V interface supplies (such as vdds18v).
- vdd_rtc rises coincident with vdd, or it may rise earlier. If rising earlier, it must rise after the 1.8V interface supplies.
- vddshv5 rises coincident with the other vddshvn rails (of the same voltage) or it can rise about the same time as the 1.8V PHY supplies (such as vdd_usb1).

(4) vdd must ramp before or at the same time as vdd_mpu, vdd_gpu, vdd_dspeve and vdd_iva.

(5) vdd_mpu, vdd_gpu, vdd_dspeve, vdd_iva can be ramped at the same time or can be staggered.

(6) If any of the vddshv[1-7,9-11] rails (not including vddshv8) are used as 1.8V only, then these rails can be combined with vdds18v.

(7) vddshv8 is separated out to show support for dual voltage. If single voltage is used then vddshv8 can be combined with other vddshvn rails but vddshv8 must ramp after vdd.

(8) vdds and vdda rails must not be combined together, with the one exception of vdda_rtc when RTC-mode is not supported.

(9) Pulse duration: rtc_porz must remain low 1ms after vdda_rtc, vddshv5, and vdd_rtc are ramped and stable.

(10) The FUNC_32K_CLK source must be stable and at a valid frequency 1ms prior to deasserting rtc_porz high.

(11) porz must remain asserted low until all of the following conditions are met:
- All device supply rails reach stable operational levels.
- xi_osc0 is stable and at a valid frequency.
- Minimum of 12P after both of the above conditions are met, where P = 1 / (SYS_CLK1/610), units in ns.
resetn must be high prior to, or rise simultaneous with, porz but not before its power supply, vddshv3, rising.

(12) Setup time: sysboot[15:0] pins must be valid 2P[(15)] before porz is de-asserted high.

(13) Hold time: sysboot[15:0] pins must be valid 15P[(15)] after porz is de-asserted high.

(14) rstoutn will be asserted low when porz is low, and de-asserted following an internal 2ms delay. rstoutn is only valid after vddshv3 reaches an operational level. If used as a peripheral component reset, it should be AND gated with porz to avoid possible reset glitches during power up.

(15) P = 1/(SYS_CLK1/610) frequency in ns.

(16) ddr1_vref0 / ddr2_vref0 may rise coincident with vdds_ddr1 / vdds_ddr2, respectively or at a later time. However, it must be valid before porz rising.


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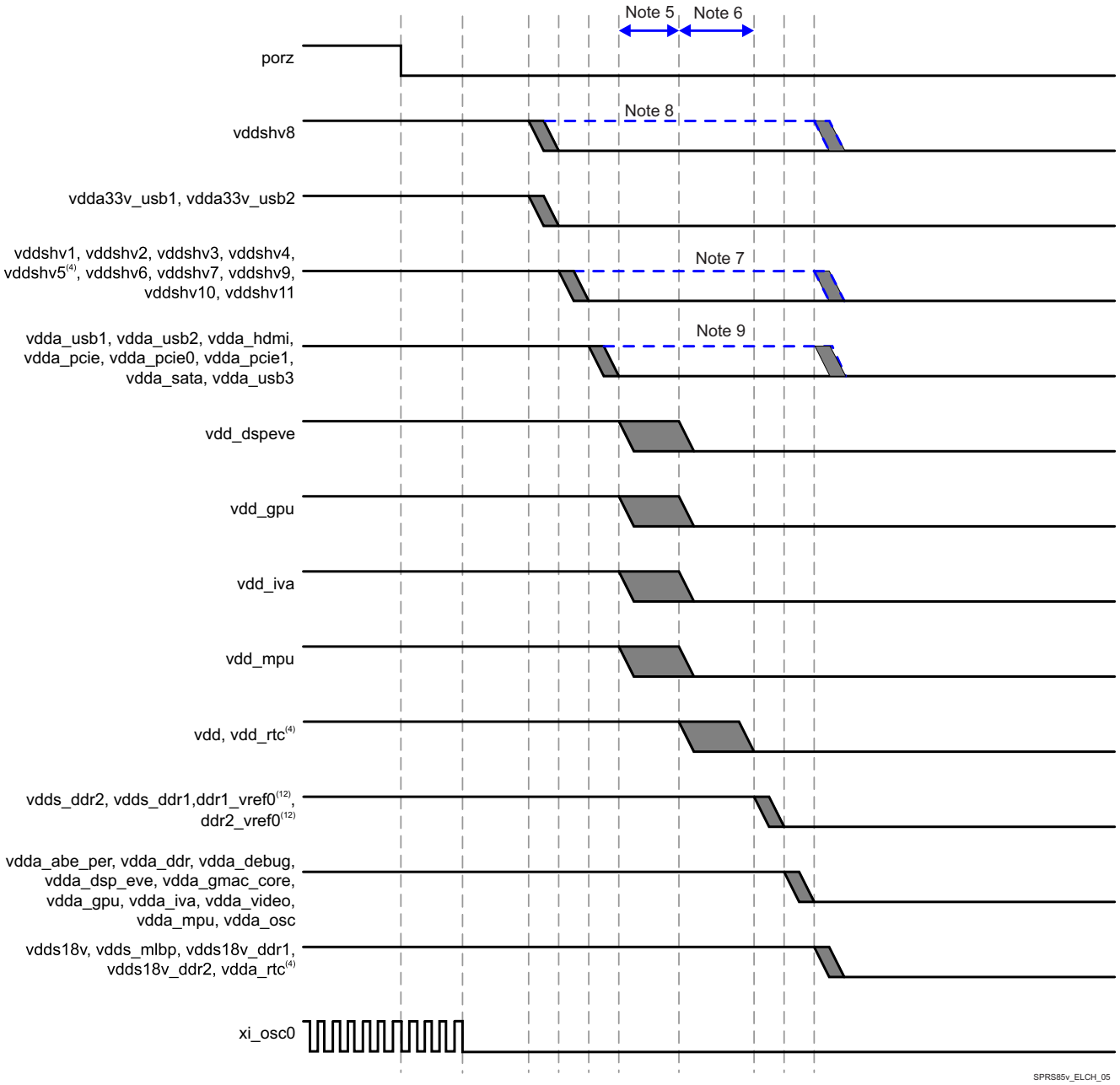


**Figure 5-3. Power-Down Sequencing(10)(11)**

(1) Grey shaded areas are windows where it is valid to ramp the voltage rail.

(2) Blue dashed lines are not valid windows but show alternate ramp possibilities based on the associated note.

(3) xi_osc0 can be turned off anytime after porz assertion and must be turned off before vdda_osc voltage rail is shutdown.

(4) If RTC-mode is not used then the following combinations are approved:
- vdda_rtc can be combined with vdds18v
- vdd_rtc can be combined with vdd
- vddshv5 can be combined with other 1.8V or 3.3V vddshv* rails

If combinations listed above are not followed then sequencing for these 3 voltage rails should follow the RTC mode timing requirements. When using RTC mode timing:
- vdda_rtc falls coincident with, or later than, the 1.8V interface supplies (such as vdds18v).
- vdd_rtc falls coincident with vdd, or it may fall later. If falling later, it must fall before, or coincident with, the 1.8V interface supplies.
- vddshv5 falls coincident with the other vddshvn rails (of the same voltage) or it can fall about the same time as the 1.8V PHY supplies (such as vdd_usb1).

(5) vdd_mpu, vdd_gpu, vdd_dspeve, vdd_iva can be ramped at the same time or can be staggered.

(6) vdd must ramp after or at the same time as vdd_mpu, vdd_gpu, vdd_dspeve and vdd_iva.

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(7) If any of the vddshv[1-7,9-11] rails (not including vddshv8) are used as 1.8V only, then these rails can be combined with vdds18v. vddshv[1-7,9-11] is allowed to ramp down at either of the two points shown in the timing diagram in either 1.8V mode or in 3.3V mode. If vddshv[1-7,9-11] ramps down at the later time in the diagram then the board design must ensure that the vddshv[1-7,9-11] rail is never higher than 2.0 V above the vdds18v rail.

(8) vddshv8 is separated out to show support for dual voltage. If a dedicated LDO/supply source is used for vddshv8, then vddshv8 ramp down should occur at one of the two earliest points in the timing diagram. If vddshv8 is powered by the same supply source as the other vddshv[1-7,9-11] rails, then it is allowed to ramp down at either of the last two points in the timing diagram.

(9) The 1.8V vdda_* supplies can either ramp down at the earlier time period shown or can be delayed to ramp down after the core supplies coincident with the vdds18v supply as long as porz is asserted (low) during the power down sequence.

(10) The power down sequence shown is the most general case and is always valid. An accelerated power down sequence is also available but is only valid when porz is asserted (low). This accelerated power down sequence has been implemented in the companion PMIC that is recommended for use with this SOC. The accelerated sequence has porz go low first, then all 3.3V supplies simultaneously second, core supplies, DDR supplies and DDR references simultaneously third and all 1.8V supplies simultaneously last.

(11) Ramped Down is defined as reaching a voltage level of no more than 0.6V.

(12) ddr1_vref0 / ddr2_vref0 may fall coincident with vdds_ddr1 / vdds_ddr2, respectively or at a prior time but after porz is asserted low.

Figure 5-4 describes vddshv[1-7,9-11] Supplies Falling Before vdds18v Supplies Delta.

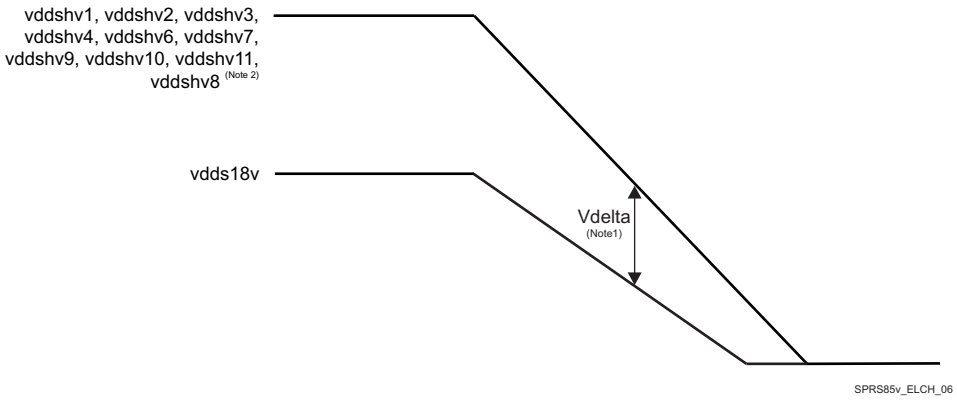


**Figure 5-4. vddshv* Supplies Falling After vdds18v Supplies Delta**

(1) Vdelta MAX = 2V

(2) If vddshv8 is powered by the same supply source as the other vddshv[1-7,9-11] rails.


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# 6 Clock Specifications

**NOTE**

For more information, see Power, Reset, and Clock Management / PRCM Subsystem Environment / External Clock Signals and External Reset Signals, and Clock Management Functional Description sections of the Device TRM.

**NOTE**

Audio Back End (ABE) module is not supported for this family of devices, but “ABE” name is still present in some clock or DPLL names.

The device operation requires the following clocks:

- The 32 kHz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. This is an optional clock and will be supplied by on chip divider + mux (FUNC_32K_CLK) incase it is not available on external pin.
- The system clocks, SYS_CLK1(Mandatory) and SYS_CLK2(Optional) are the main clock sources of the device. They supply the reference clock to the DPLLs as well as functional clock to several modules.

The Device also embeds an internal free-running 32-kHz oscillator that is always active as long as the the wake-up (WKUP) domain is supplied.

Figure 6-1 shows the external input clock sources and the output clocks to peripherals.

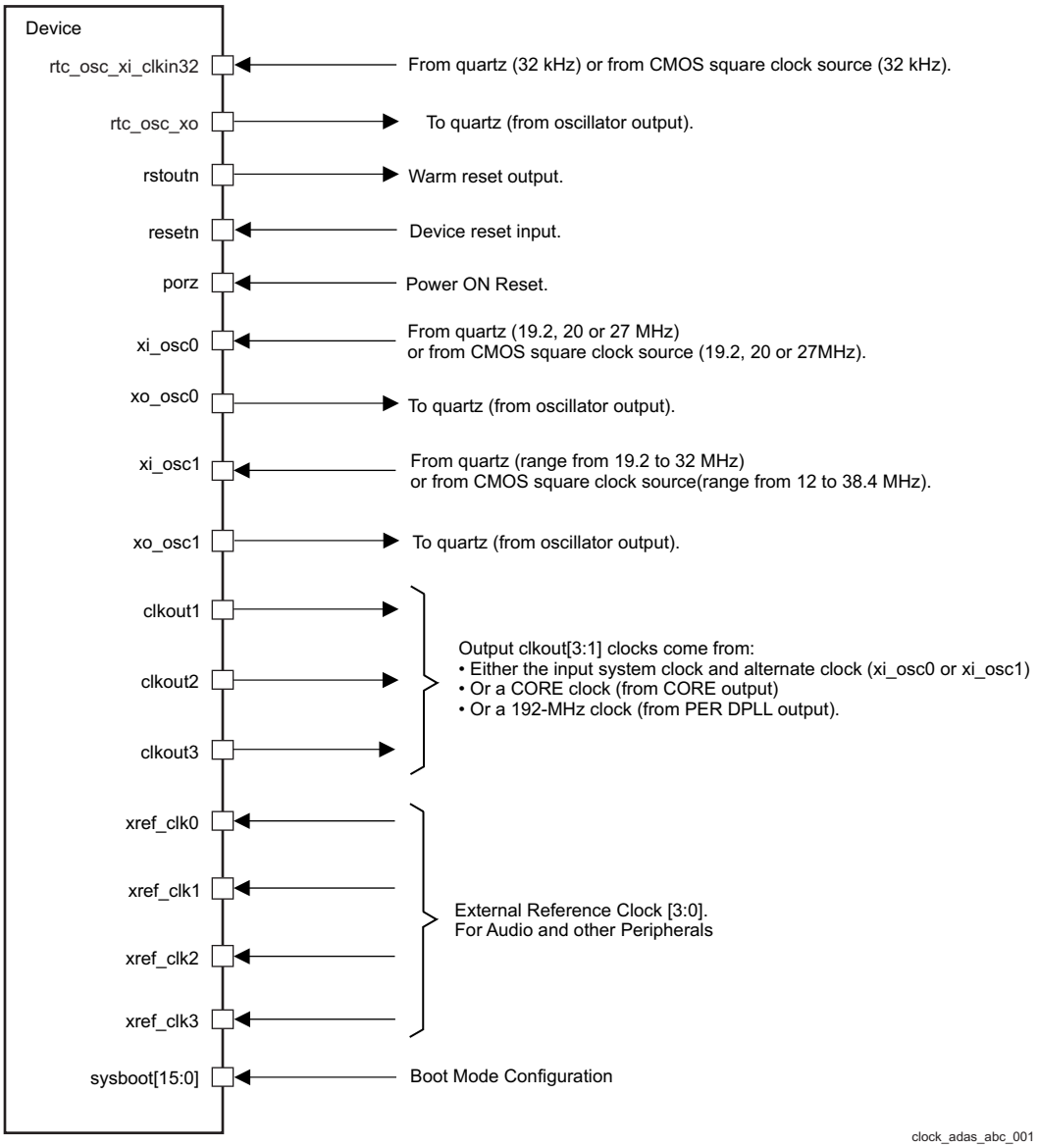


**Figure 6-1. Clock Interface**

## 6.1 Input Clock Specifications

### *6.1.1 Input Clock Requirements*

- The source of the internal system clock (SYS_CLK1) could be either:
  - A CMOS clock that enters on the xi_osc0 ball (with xo_osc0 left unconnected on the CMOS clock case).
  - A crystal oscillator clock managed by xi_osc0 and xo_osc0.
- The source of the internal system clock (SYS_CLK2) could be either:
  - A CMOS clock that enters on the xi_osc1 ball (with xo_osc1 left unconnected on the CMOS clock case).
  - A crystal oscillator clock managed by xi_osc1 and xo_osc1.


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- The source of the internal system clock (FUNC_32K_CLK) could be either:
  - A CMOS clock that enters on the rtc_osc_xi_clkin32 ball and supports external LVCMOS clock generators
  - A crystal oscillator clock managed by rtc_osc_xi_clkin32 and rtc_osc_xo.

### 6.1.2 System Oscillator OSC0 Input Clock

SYS_CLK1 is received directly from oscillator OSC0. For more information about SYS_CLK1 see Device TRM, Chapter: *Power, Reset, and Clock Management.*

#### 6.1.2.1 OSC0 External Crystal

An external crystal is connected to the device pins. Figure 6-2 describes the crystal implementation.

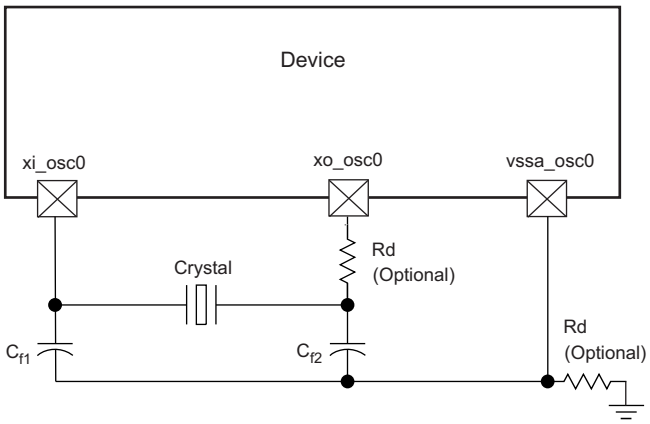


**Figure 6-2. Crystal Implementation**

**NOTE**

The load capacitors, $C_{f1}$ and $C_{f2}$ in Figure 6-2, should be chosen such that the below equation is satisfied. $C_L$ in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator xi_osc0, xo_osc0, and vssa_osc0 pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

**Figure 6-3. Load Capacitance Equation**

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-1 summarizes the required electrical constraints.

**Table 6-1. OSC0 Crystal Electrical Characteristics**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_p$ | Parallel resonance crystal frequency | | | 19.2, 20, 27 | MHz |
| $C_{f1}$ | $C_{f1}$ load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | 12 | | 24 | pF |
| $C_{f2}$ | $C_{f2}$ load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | 12 | | 24 | pF |
| ESR($C_{f1}$,$C_{f2}$) | Crystal ESR | | | 100 | Ω |

**Table 6-1. OSC0 Crystal Electrical Characteristics (continued)**

| NAME | DESCRIPTION | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_O$ | Crystal shunt capacitance | ESR = 30 Ω<br>ESR = 40 Ω | 19.2 MHz, 20 MHz, 27 MHz | | | 7 | pF |
| | | ESR = 50 Ω | 19.2 MHz, 20 MHz | | | 7 | pF |
| | | | 27 MHz | | | 5 | pF |
| | | ESR = 60 Ω | 19.2 MHz, 20 MHz | | | 7 | pF |
| | | | 27 MHz | | | Not Supported | - |
| | | ESR = 80 Ω | 19.2 MHz, 20 MHz | | | 5 | pF |
| | | | 27 MHz | | | Not Supported | - |
| | | ESR = 100 Ω | 19.2 MHz, 20 MHz | | | 3 | pF |
| | | | 27 MHz | | | Not Supported | - |
| $L_M$ | Crystal motional inductance for $f_p$ = 20 MHz | | | | 10.16 | | mH |
| $C_M$ | Crystal motional capacitance | | | | 3.42 | | fF |
| $t_{j(xiosc0)}$ | Frequency accuracy (1), xi_osc0 | | Ethernet not used | | | ±200 | ppm |
| | | | Ethernet RGMII and RMII using derived clock | | | ±50 | |
| | | | Ethernet MII using derived clock | | | ±100 | |

(1) Crystal characteristics should account for tolerance+stability+aging.

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 6-2 details the switching characteristics of the oscillator and the requirements of the input clock.

**Table 6-2. Oscillator Switching Characteristics—Crystal Mode**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_p$ | Oscillation frequency | | | 19.2, 20, 27 | MHz |
| $t_{sX}$ | Start-up time | | | 4 | ms |

### 6.1.2.2 OSC0 Input Clock

A 1.8-V LVCMOS-Compatible Clock Input can be used instead of the internal oscillator to provide the SYS_CLK1 clock input to the system. The external connections to support this are shown in Figure 6-4. The xi_osc0 pin is connected to the 1.8-V LVCMOS-Compatible clock source. The xi_osc0 pin is left unconnected. The vssa_osc0 pin is connected to board ground (VSS).

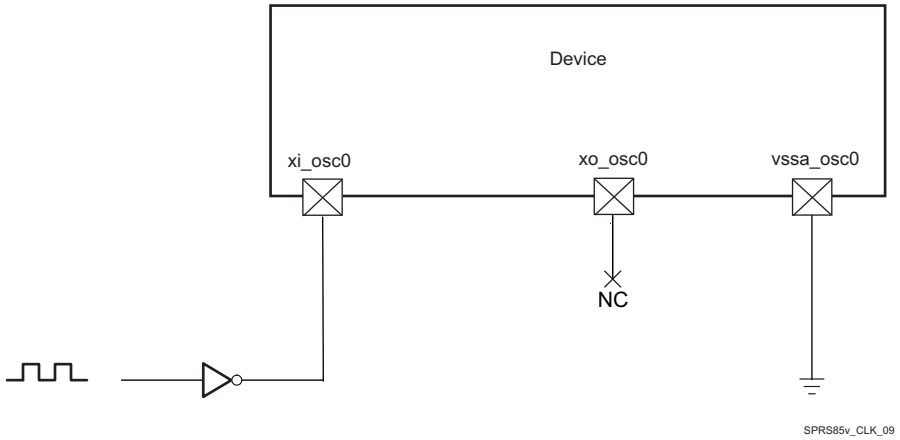


**Figure 6-4. 1.8-V LVCMOS-Compatible Clock Input**

Table 6-3 summarizes the OSC0 input clock electrical characteristics.


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**Table 6-3. OSC0 Input Clock Electrical Characteristics—Bypass Mode**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| f | Frequency | | | 19.2, 20, or 27 | MHz |
| $C_{In}$ | Input capacitance | 2.184 | 2.384 | 2.584 | pF |
| $I_{In}$ | Input current (3.3V mode) | 4 | 6 | 10 | µA |

Table 6-4 details the OSC0 input clock timing requirements.

**Table 6-4. OSC0 Input Clock Timing Requirements**

| NAME | DESCRIPTION | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| CK0 | $1 / t_{c(xiosc0)}$ | Frequency, xi_osc0 | | | | 19.2, 20, 27 | MHz |
| CK1 | $t_{w(xiosc0)}$ | Pulse duration, xi_osc0 low or high | | 0.45 * $t_{c(xiosc0)}$ | | 0.55 * $t_{c(xiosc0)}$ | ns |
| | $t_{j(xiosc0)}$ | Period jitter(1), xi_osc0 | | | | 0.01 × $t_{c(xiosc0)}$ | ns |
| | $t_{R(xiosc0)}$ | Rise time, xi_osc0 | | | | 5 | ns |
| | $t_{F(xiosc0)}$ | Fall time, xi_osc0 | | | | 5 | ns |
| | $t_{j(xiosc0)}$ | Frequency accuracy(2), xi_osc0 | Ethernet not used | | | ±200 | ppm |
| | | | Ethernet RGMII and RMII using derived clock | | | ±50 | |
| | | | Ethernet MII using derived clock | | | ±100 | |

(1) Period jitter is meant here as follows:

– The maximum value is the difference between the longest measured clock period and the expected clock period

– The minimum value is the difference between the shortest measured clock period and the expected clock period

(2) Crystal characteristics should account for tolerance+stability+aging.

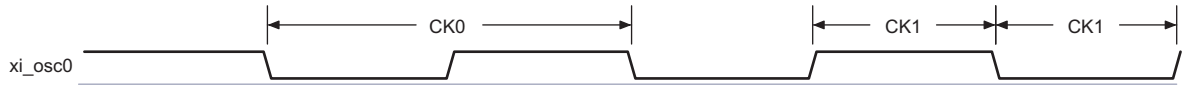


**Figure 6-5. xi_osc0 Input Clock**

### *6.1.3 Auxiliary Oscillator OSC1 Input Clock*

SYS_CLK2 is received directly from oscillator OSC1. For more information about SYS_CLK2 see Device TRM, Chapter: *Power, Reset, and Clock Management.*

#### 6.1.3.1 OSC1 External Crystal

An external crystal is connected to the device pins. Figure 6-6 describes the crystal implementation.

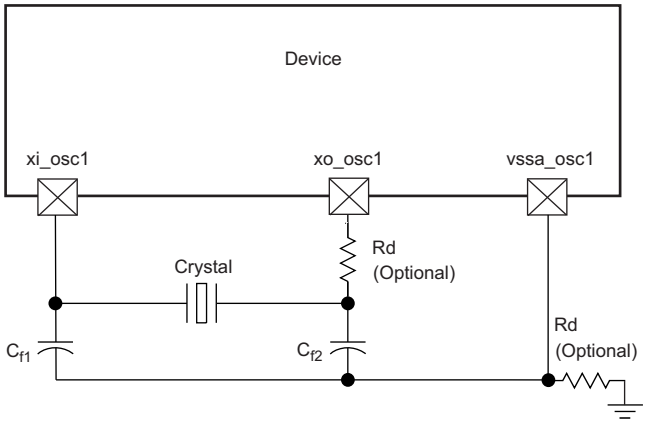


**Figure 6-6. Crystal Implementation**

**NOTE**

The load capacitors, $C_{f1}$ and $C_{f2}$ in Figure 6-6, should be chosen such that the below equation is satisfied. $C_L$ in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator xi_osc1, xo_osc1, and vssa_osc1 pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

**Figure 6-7. Load Capacitance Equation**

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-5 summarizes the required electrical constraints.

**Table 6-5. OSC1 Crystal Electrical Characteristics**

| NAME | DESCRIPTION | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_p$ | Parallel resonance crystal frequency | | | | Range from 19.2 to 32 | | MHz |
| $C_{f1}$ | $C_{f1}$ load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | | | 12 | | 24 | pF |
| $C_{f2}$ | $C_{f2}$ load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | | | 12 | | 24 | pF |
| ESR($C_{f1}$,$C_{f2}$) | Crystal ESR | | | | | 100 | Ω |
| $C_O$ | Crystal shunt capacitance | ESR = 30 Ω | 19.2 MHz ≤ $f_p$ ≤ 32 MHz | | | 7 | pF |
| | | ESR = 40 Ω | 19.2 MHz ≤ $f_p$ ≤ 32 MHz | | | 5 | pF |
| | | ESR = 50 Ω | 19.2 MHz ≤ $f_p$ ≤ 25 MHz | | | 7 | pF |
| | | | 25 MHz < $f_p$ ≤ 27 MHz | | | 5 | pF |
| | | | 27 MHz < $f_p$ ≤ 32 MHz | | | Not Supported | - |
| | | ESR = 60 Ω | 19.2 MHz ≤ $f_p$ ≤ 23 MHz | | | 7 | pF |
| | | | 23 MHz < $f_p$ ≤ 25 MHz | | | 5 | pF |
| | | | 25 MHz < $f_p$ ≤ 32 MHz | | | Not Supported | - |
| | | ESR = 80 Ω | 19.2 MHz ≤ $f_p$ ≤ 23 MHz | | | 5 | pF |
| | | | 23 MHz ≤ $f_p$ ≤ 25 MHz | | | 3 | pF |
| | | | 25 MHz < $f_p$ ≤ 32 MHz | | | Not Supported | - |
| | | ESR = 100 Ω | 19.2 MHz ≤ $f_p$ ≤ 20 MHz | | | 3 | pF |
| | | | 20 MHz < $f_p$ ≤ 32 MHz | | | Not Supported | - |
| $L_M$ | Crystal motional inductance for $f_p$ = 20 MHz | | | | 10.16 | | mH |
| $C_M$ | Crystal motional capacitance | | | | 3.42 | | fF |


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**Table 6-5. OSC1 Crystal Electrical Characteristics (continued)**

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{j(xiosc1)}$ | Frequency accuracy[(1)], xi_osc1 | Ethernet not used | | | ±200 | ppm |
| | | Ethernet RGMII and RMII using derived clock | | | ±50 | |
| | | Ethernet MII using derived clock | | | ±100 | |

(1) Crystal characteristics should account for tolerance+stability+aging.

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 6-6 details the switching characteristics of the oscillator and the requirements of the input clock.

**Table 6-6. Oscillator Switching Characteristics—Crystal Mode**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_p$ | Oscillation frequency | | Range from 19.2 to 32 | | MHz |
| $t_{sX}$ | Start-up time | | | 4 | ms |

### 6.1.3.2 OSC1 Input Clock

A 1.8-V LVCMOS-Compatible Clock Input can be used instead of the internal oscillator to provide the SYS_CLK2 clock input to the system. The external connections to support this are shown in, Figure 6-8. The xi_osc1 pin is connected to the 1.8-V LVCMOS-Compatible clock sources. The xo_osc1 pin is left unconnected. The vssa_osc1 pin is connected to board ground (vss).

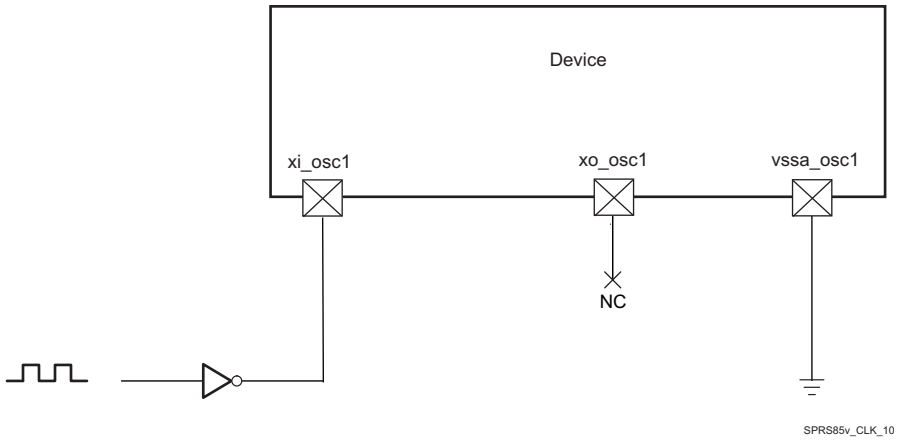


**Figure 6-8. 1.8-V LVCMOS-Compatible Clock Input**

Table 6-7 summarizes the OSC1 input clock electrical characteristics.

**Table 6-7. OSC1 Input Clock Electrical Characteristics—Bypass Mode**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| f | Frequency | | Range from 12 to 38.4 | | MHz |
| $C_I$ | Input capacitance | 2.819 | 3.019 | 3.219 | pF |
| $I_I$ | Input current (3.3V mode) | 4 | 6 | 10 | µA |
| $t_{sX}$ | Start-up time[(1)] | | | See[(2)] | ms |

(1) To switch from bypass mode to crystal or from crystal mode to bypass mode, there is a waiting time about 100 µs; however, if the chip comes from bypass mode to crystal mode the crystal will start-up after time mentioned in Table 6-6, $t_{sX}$ parameter.

(2) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a wave. The switching time in this case is about 100 µs.

Table 6-8 details the OSC1 input clock timing requirements.

**Table 6-8. OSC1 Input Clock Timing Requirements**

| NAME | | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| CK0 | 1 / $t_{c(xiosc1)}$ | Frequency, xi_osc1 | | Range from 12 to 38.4 | | | MHz |
| CK1 | $t_{w(xiosc1)}$ | Pulse duration, xi_osc1 low or high | | 0.45 * $t_{c(xiosc1)}$ | | 0.55 * $t_{c(xiosc1)}$ | ns |
| | $t_{j(xiosc1)}$ | Period jitter(1), xi_osc1 | | | | 0.01 × $t_{c(xiosc1)}$ (3) | ns |
| | $t_{R(xiosc1)}$ | Rise time, xi_osc1 | | | | 5 | ns |
| | $t_{F(xiosc1)}$ | Fall time, xi_osc1 | | | | 5 | ns |
| | $t_{j(xiosc1)}$ | Frequency accuracy(2), xi_osc1 | Ethernet not used | | | ±200 | ppm |
| | | | Ethernet RGMII and RMII using derived clock | | | ±50 | |
| | | | Ethernet MII using derived clock | | | ±100 | |

(1) Period jitter is meant here as follows:
- The maximum value is the difference between the longest measured clock period and the expected clock period
- The minimum value is the difference between the shortest measured clock period and the expected clock period

(2) Crystal characteristics should account for tolerance+stability+aging.

(3) The Period jitter requirement for osc1 can be relaxed to 0.02*$t_{c(xiosc1)}$ under the following constraints:
a.The osc1/SYS_CLK2 clock bypasses all device PLLs
b.The osc1/SYS_CLK2 clock is only used to source the DSS pixel clock outputs

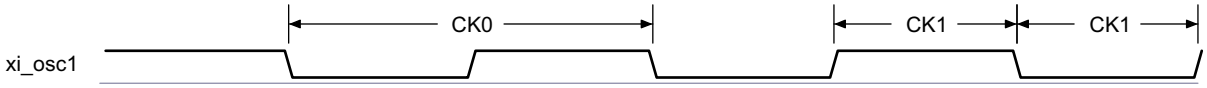


**Figure 6-9. xi_osc1 Input Clock**

### 6.1.4 RTC Oscillator Input Clock

FUNC_32K_CLK is received directly from RTC Oscillator. For more information about FUNC_32K_CLK see Device TRM, Chapter: *Power, Reset, and Clock Management.*

**NOTE**

RTC only mode is not supported feature.

#### 6.1.4.1 RTC Oscillator External Crystal

An external crystal is connected to the device pins. Figure 6-10 describes the crystal implementation.


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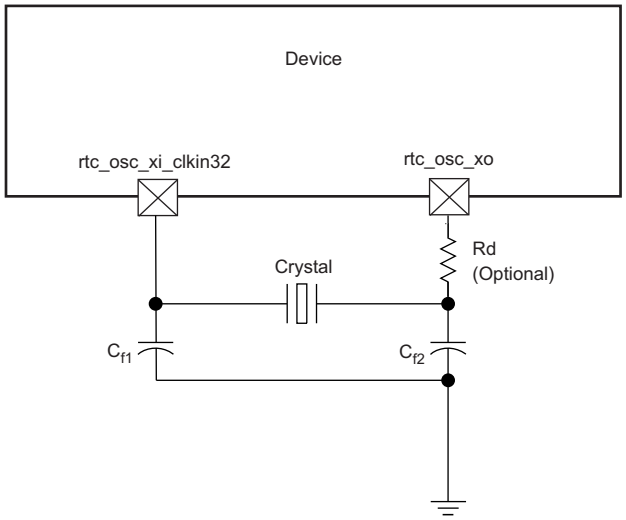


**Figure 6-10. Crystal Implementation**

**NOTE**

The load capacitors, $C_{f1}$ and $C_{f2}$ in Figure 6-10, should be chosen such that the below equation is satisfied. $C_L$ in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator rtc_osc_xi_clkin32 and rtc_osc_xo pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

**Figure 6-11. Load Capacitance Equation**

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-9 summarizes the required electrical constraints.

**Table 6-9. RTC Crystal Electrical Characteristics**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_p$ | Parallel resonance crystal frequency | | | 32.768 | kHz |
| $C_{f1}$ | $C_{f1}$ load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | 12 | | 24 | pF |
| $C_{f2}$ | $C_{f2}$ load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | 12 | | 24 | pF |
| ESR($C_{f1}$,$C_{f2}$) | Crystal ESR | | | 80 | kΩ |
| $C_O$ | Crystal shunt capacitance | | | 5 | pF |
| $L_M$ | Crystal motional inductance for $f_p$ = 32.768 kHz | | 10.7 | | mH |
| $C_M$ | Crystal motional capacitance | | 2.2 | | fF |
| $t_{j(rtc_osc_xi_clkin32)}$ | Frequency accuracy, rtc_osc_xi_clkin32 | | | ±200 | ppm |

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 6-10 details the switching characteristics of the oscillator and the requirements of the input clock.

**Table 6-10. Oscillator Switching Characteristics—Crystal Mode**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_p$ | Oscillation frequency | | | 32.768 | kHz |
| $t_{sX}$ | Start-up time | | | 4 | ms |

#### 6.1.4.2 RTC Oscillator Input Clock

A 1.8-V LVCMOS-Compatible Clock Input can be used instead of the internal oscillator to provide the FUNC_32K_CLK clock input to the system. The external connections to support this are shown in Figure 6-12. The rtc_osc_xi_clkin32 pin is connected to the 1.8-V LVCMOS-Compatible clock sources. The rtc_osc_xo pin is left unconnected.

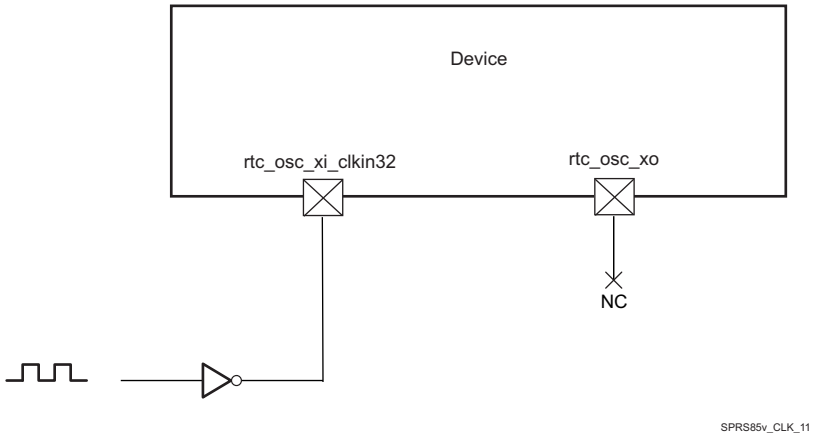


**Figure 6-12. LVCMOS-Compatible Clock Input**

Table 6-11 summarizes the RTC Oscillator input clock electrical characteristics.

**Table 6-11. RTC Oscillator Input Clock Electrical Characteristics—Bypass Mode**

| NAME | | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| CK0 | $1/t_{c(rtc_osc_xi_clkin32)}$ | Frequency, rtc_osc_xi_clkin32 | | | 32.768 | kHz |
| CK1 | $t_{w(rtc_osc_xi_clkin32)}$ | Pulse duration, rtc_osc_xi_clkin32 low or high | 0.45 * $t_{c(rtc_osc_xi_clkin32)}$ | | 0.55 * $t_{c(rtc_osc_xi_clkin32)}$ | ns |
| | $C_{IN}$ | Input capacitance | 2.178 | 2.378 | 2.578 | pF |
| | $I_{IN}$ | Input current (3.3V mode) | 4 | 6 | 10 | µA |
| | $t_{sX}$ | Start-up time | | | See (1) | ms |

(1) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is inapplication mode and receives a wave. The switching time in this case is about 100 µs.

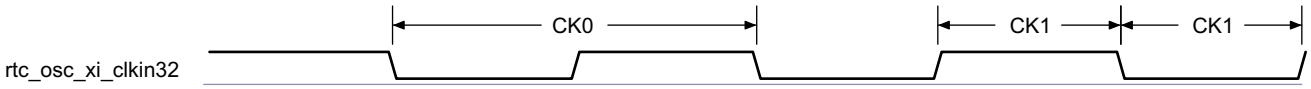


**Figure 6-13. rtc_osc_xi_clkin32 Input Clock**

## 6.2 RC On-die Oscillator Clock

**NOTE**

The OSC_32K_CLK clock, provided by the On-die 32K RC oscillator, inside of the SoC, is not accurate 32kHz clock.

The frequency may significantly vary with temperature and silicon characteristics.

For more information about OSC_32K_CLK see the Device TRM, Chapter: *Power, Reset, and Clock Management*.

## 6.3 DPLLs, DLLs Specifications


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**NOTE**

For more information, see:

- Power, Reset, and Clock Management / Clock Management Functional / Internal Clock Sources and Generators / Generic DPLL Overview section

  and
- Display Subsystem / Display Subsystem Overview section of the Device TRM.

To generate high-frequency clocks, the device supports multiple on-chip DPLLs controlled directly by the PRCM module. They are of two types: type A and type B DPLLs.

- They have their own independent power domain (each one embeds its own switch and can be controlled as an independent functional power domain)
- They are fed with ALWAYS ON system clock, with independent control per DPLL.

The different DPLLs managed by the PRCM are listed below:

- DPLL_MPU: It supplies the MPU subsystem clocking internally.
- DPLL_IVA: It feeds the IVA subsystem clocking.
- DPLL_CORE: It supplies all interface clocks and also few module functional clocks.
- DPLL_PER: It supplies several clock sources: a 192-MHz clock for the display functional clock, a 96-MHz functional clock to subsystems and peripherals.
- DPLL_ABE: It provides clocks to various modules within the device.
- DPLL_USB: It provides 960M clock for USB modules (USB1/2/3/4).
- DPLL_GMAC: It supplies several clocks for the Gigabit Ethernet Switch (GMAC_SW).
- DPLL_DSP: It feeds the DSP Subsystem clocking.
- DPLL_GPU: It supplies clock for the GPU Subsystem.
- DPLL_DDR: It generates clocks for the two External Memory Interface (EMIF) controllers and their associated EMIF PHYs.
- DPLL_PCIE_REF: It provides reference clock for the APLL_PCIE in PCIE Subsystem.
- APLL_PCIE: It feeds clocks for the device Peripheral Component Interconnect Express (PCIe) controllers.

**NOTE**

The following DPLLs are controlled by the clock manager located in the always-on Core power domain (CM_CORE_AON):

- DPLL_MPU, DPLL_IVA, DPLL_CORE, DPLL_ABE, DPLL_DDR, DPLL_GMAC, DPLL_PCIE_REF, DPLL_PER, DPLL_USB, DPLL_DSP, DPLL_GPU, APLL_PCIE_REF.

For more information on CM_CORE_AON and CM_CORE or PRCM DPLLs, see the Power, Reset, and Clock Management chapter of the Device TRM.

The following DPLLs are not managed by the PRCM:

- DPLL_VIDEO1; (It is controlled from DSS)
- DPLL_VIDEO2; (It is controlled from DSS)
- DPLL_HDMI; (It is controlled from DSS)
- DPLL_SATA; (It is controlled from SATA)
- DPLL_DEBUG; (It is controlled from DEBUGSS)
- DPLL_USB_OTG_SS; (It is controlled from OCP2SCP1)

**NOTE**

For more information for not controlled from PRCM DPLL's see the related chapters in TRM.

### 6.3.1 DPLL Characteristics

The DPLL has three relevant input clocks. One of them is the reference clock (CLKINP) used to generated the synthesized clock but can also be used as the bypass clock whenever the DPLL enters a bypass mode. It is therefore mandatory. The second one is a fast bypass clock (CLKINPULOW) used when selected as the bypass clock and is optional. The third clock (CLKINPHIF) is explained in the next paragraph.

The DPLL has three output clocks (namely CLKOUT, CLKOUTX2, and CLKOUTHIF). CLKOUT and CLKOUTX2 run at the bypass frequency whenever the DPLL enters a bypass mode. Both of them are generated from the lock frequency divided by a post-divider (namely M2 post-divider). The third clock, CLKOUTHIF, has no automatic bypass capability. It is an output of a post-divider (M3 post-divider) with the input clock selectable between the internal lock clock (Fdpll) and CLKINPHIF input of the PLL through an asynchronous multplexing.

For more information, see the Power, Reset, and Clock Management chapter of the Device TRM.

Table 6-12 summarizes DPLL type described in Section 6.3, *DPLLs, DLLs Specifications* introduction.

**Table 6-12. DPLL Control Type**

| DPLL NAME | TYPE | CONTROLLED BY PRCM |
|---|---|---|
| DPLL_ABE | Table 6-13 (Type A) | Yes(1) |
| DPLL_CORE | Table 6-13 (Type A) | Yes(1) |
| DPLL_DEBUGSS | Table 6-13 (Type A) | No(2) |
| DPLL_DSP | Table 6-13 (Type A) | Yes(1) |
| DPLL_GMAC | Table 6-13 (Type A) | Yes(1) |
| DPLL_HDMI | Table 6-14 (Type B) | No(2) |
| DPLL_IVA | Table 6-13 (Type A) | Yes(1) |
| DPLL_MPU | Table 6-13 (Type A) | Yes(1) |
| DPLL_PER | Table 6-13 (Type A) | Yes(1) |
| APLL_PCIE | Table 6-13 (Type A) | Yes(1) |
| DPLL_PCIE_REF | Table 6-14 (Type B) | Yes(1) |
| DPLL_SATA | Table 6-14 (Type B) | No(2) |
| DPLL_USB | Table 6-14 (Type B) | Yes(1) |
| DPLL_USB_OTG_SS | Table 6-14 (Type B) | No(2) |
| DPLL_VIDEO1 | Table 6-13 (Type A) | No(2) |
| DPLL_VIDEO2 | Table 6-13 (Type A) | No(2) |
| DPLL_DDR | Table 6-13 (Type A) | Yes(1) |
| DPLL_GPU | Table 6-13 (Type A) | Yes(1) |

(1) DPLL is in the always-on domain.

(2) DPLL is not controlled by the PRCM.

Table 6-13 and Table 6-14 summarize the DPLL characteristics and assume testing over recommended operating conditions.

**Table 6-13. DPLL Type A Characteristics**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| $f_{input}$ | CLKINP input frequency | 0.032 | | 52 | MHz | $F_{INP}$ |
| $f_{internal}$ | Internal reference frequency | 0.15 | | 52 | MHz | REFCLK |


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### Table 6-13. DPLL Type A Characteristics (continued)

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| $f_{CLKINPHIF}$ | CLKINPHIF input frequency | 10 | | 1400 | MHz | $F_{INPHIF}$ |
| $f_{CLKINPULOW}$ | CLKINPULOW input frequency | 0.001 | | 600 | MHz | Bypass mode: $f_{CLKOUT}$ = $f_{CLKINPULOW}$ / (M1 + 1) if ulowclken = 1[6] |
| $f_{CLKOUT}$ | CLKOUT output frequency | 20[1] | | 1800[2] | MHz | [M / (N + 1)] × $F_{INP}$ × [1 / M2] (in locked condition) |
| $f_{CLKOUTx2}$ | CLKOUTx2 output frequency | 40[1] | | 2200[2] | MHz | 2 × [M / (N + 1)] × $F_{INP}$ × [1 / M2] (in locked condition) |
| $f_{CLKOUTHIF}$ | CLKOUTHIF output frequency | 20[3] | | 1400[4] | MHz | $F_{INPHIF}$ / M3 if clkinphifsel = 1 |
| | | 40[3] | | 2200[4] | MHz | 2 × [M / (N + 1)] × $F_{INP}$ × [1 / M3] if clkinphifsel = 0 |
| $f_{CLKDCOLDO}$ | DCOCLKLDO output frequency | 40 | | 2800 | MHz | 2 × [M / (N + 1)] × $F_{INP}$ (in locked condition) |
| $t_{lock}$ | Frequency lock time | | | 6 + 350 × REFCLK | µs | |
| $p_{lock}$ | Phase lock time | | | 6 + 500 × REFCLK | µs | |
| $t_{relock-L}$ | Relock time—Frequency lock[5] (LP relock time from bypass) | | | 6 + 70 × REFCLK | µs | DPLL in LP relock time: lowcurrstdby = 1 |
| $p_{relock-L}$ | Relock time—Phase lock[5] (LP relock time from bypass) | | | 6 + 120 × REFCLK | µs | DPLL in LP relock time: lowcurrstdby = 1 |
| $t_{relock-F}$ | Relock time—Frequency lock[5] (fast relock time from bypass) | | | 3.55 + 70 × REFCLK | µs | DPLL in fast relock time: lowcurrstdby = 0 |
| $p_{relock-F}$ | Relock time—Phase lock[5] (fast relock time from bypass) | | | 3.55 + 120 × REFCLK | µs | DPLL in fast relock time: lowcurrstdby = 0 |

(1) The minimum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

For M2 > 1, the minimum frequency on these clocks will further scale down by factor of M2.

(2) The maximum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

(3) The minimum frequency on CLKOUTHIF is assuming M3 = 1. For M3 > 1, the minimum frequency on this clock will further scale down by factor of M3.

(4) The maximum frequency on CLKOUTHIF is assuming M3 = 1.

(5) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

(6) Bypass mode: $f_{CLKOUT}$ = $F_{INP}$ if ULOWCLKEN = 0. For more information, see the Device TRM.

### Table 6-14. DPLL Type B Characteristics

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| $f_{input}$ | CLKINP input clock frequency | 0.62 | | 60 | MHz | $F_{INP}$ |
| $f_{internal}$ | REFCLK internal reference clock frequency | 0.62 | | 2.5 | MHz | [1 / (N + 1)] × $F_{INP}$ |
| $f_{CLKINPULOW}$ | CLKINPULOW bypass input clock frequency | 0.001 | | 600 | MHz | Bypass mode: $f_{CLKOUT}$ = $f_{CLKINPULOW}$ / (M1 + 1) If ulowclken = 1[4] |
| $f_{CLKLDOOUT}$ | CLKOUTLDO output clock frequency | 20[1][5] | | 2500[2][5] | MHz | M / (N + 1)] × $F_{INP}$ × [1 / M2] (in locked condition) |
| $f_{CLKOUT}$ | CLKOUT output clock frequency | 20[1][5] | | 1450[2][5] | MHz | [M / (N + 1)] × $F_{INP}$ × [1 / M2] (in locked condition) |
| $f_{CLKDCOLDO}$ | Internal oscillator (DCO) output clock frequency | 750[5] | | 1500[5] | MHz | [M / (N + 1)] × $F_{INP}$ (in locked condition) |
| | | 1250[5] | | 2500[5] | MHz | |
| $t_J$ | CLKOUTLDO period jitter | –2.5% | | 2.5% | | The period jitter at the output clocks is ± 2.5% peak to peak |
| | CLKOUT period jitter | | | | | |
| | CLKDCOLDO period jitter | | | | | |

**Table 6-14. DPLL Type B Characteristics (continued)**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| $t_{lock}$ | Frequency lock time | | | 350 × REFCLKs | µs | |
| $p_{lock}$ | Phase lock time | | | 500 × REFCLKs | µs | |
| $t_{relock-L}$ | Relock time—Frequency lock(3) (LP relock time from bypass) | | | 9 + 30 × REFCLKs | µs | |
| $p_{relock-L}$ | Relock time—Phase lock(3) (LP relock time from bypass) | | | 9 + 125 × REFCLKs | µs | |

(1) The minimum frequency on CLKOUT is assuming M2 = 1.

For M2 > 1, the minimum frequency on this clock will further scale down by factor of M2.

(2) The maximum frequency on CLKOUT is assuming M2 = 1.

(3) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

(4) Bypass mode: $f_{CLKOUT} = F_{INP}$ if ULOWCLKEN = 0. For more information, see the Device TRM.

(5) For output clocks, there are two frequency ranges according to the SELFREQDCO setting. For more information, see the Device TRM.

### 6.3.2 DLL Characteristics

Table 6-15 summarizes the DLL characteristics and assumes testing over recommended operating conditions.

**Table 6-15. DLL Characteristics**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{input}$ | Input clock frequency (EMIF_DLL_FCLK) | | | 266 | MHz |
| $t_{lock}$ | Lock time | | | 50k | cycles |
| $t_{relock}$ | Relock time (a change of the DLL frequency implies that DLL must relock) | | | 50k | cycles |


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# 7 Timing Requirements and Switching Characteristics

## 7.1 Timing Test Conditions

All timing requirements and switching characteristics are valid over the recommended operating conditions unless otherwise specified.

## 7.2 Interface Clock Specifications

### *7.2.1 Interface Clock Terminology*

The interface clock is used at the system level to sequence the data and/or to control transfers accordingly with the interface protocol.

### *7.2.2 Interface Clock Frequency*

The two interface clock characteristics are:

- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented in this document is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the Device IC and does not take into account any system consideration (PCB, peripherals).

The system designer will have to consider these system considerations and the Device IC timing characteristics as well to define properly the maximum operating frequency that corresponds to the maximum frequency supported to transfer the data on this interface.

## 7.3 Timing Parameters and Information

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of pin names and other related terminologies have been abbreviated as follows:

**Table 7-1. Timing Parameters**

| SUBSCRIPTS | |
|---|---|
| **SYMBOL** | **PARAMETER** |
| c | Cycle time (period) |
| d | Delay time |
| dis | Disable time |
| en | Enable time |
| h | Hold time |
| su | Setup time |
| START | Start bit |
| t | Transition time |
| v | Valid time |
| w | Pulse duration (width) |
| X | Unknown, changing, or don't care level |
| F | Fall time |
| H | High |
| L | Low |
| R | Rise time |
| V | Valid |
| IV | Invalid |

**Table 7-1. Timing Parameters (continued)**

| SUBSCRIPTS | |
|---|---|
| **SYMBOL** | **PARAMETER** |
| AE | Active Edge |
| FE | First Edge |
| LE | Last Edge |
| Z | High impedance |

### *7.3.1 Parameter Information*

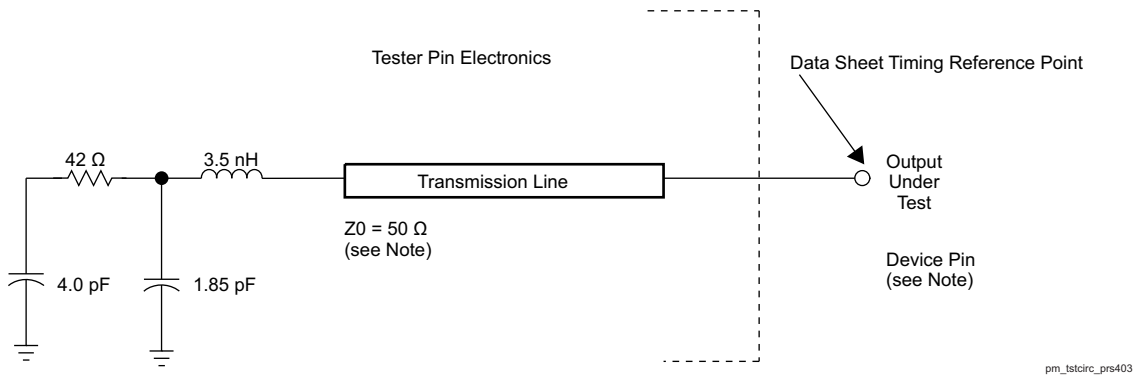


**Figure 7-1. Test Load Circuit for AC Timing Measurements**

The load capacitance value stated is only for characterization and measurement of AC timing signals.

This load capacitance value does not indicate the maximum load the device is capable of driving.

#### 7.3.1.1 1.8V and 3.3V Signal Transition Levels

All input and output timing parameters are referenced to $V_{ref}$ for both "0" and "1" logic levels. $V_{ref}$ = (VDD I/O)/2.

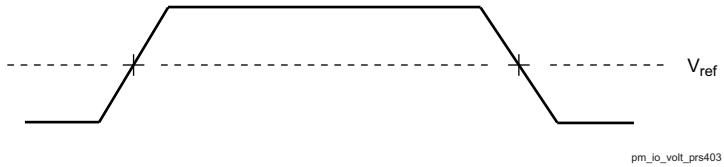


**Figure 7-2. Input and Output Voltage Reference Levels for AC Timing Measurements**

All rise and fall transition timing parameters are referenced to $V_{IL}$ MAX and $V_{IH}$ MIN for input clocks, $V_{OL}$ MAX and $V_{OH}$ MIN for output clocks.

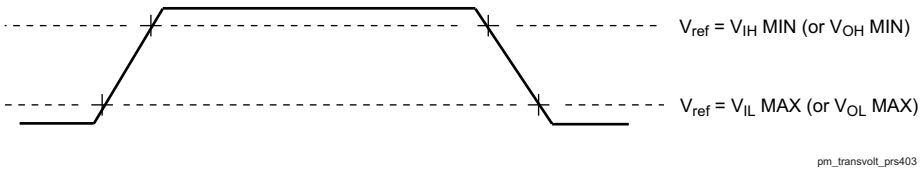


**Figure 7-3. Rise and Fall Transition Time Voltage Reference Levels**

#### 7.3.1.2 1.8V and 3.3V Signal Transition Rates

The default SLEWCONTROL settings in each pad configuration register must be used to ensure timings, unless specific instructions otherwise are given in the individual timing sub-sections of the datasheet.


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All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

#### 7.3.1.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data manual do not include delays by board routes. As a good board design practice, such delays must always be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends using the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for timing Analysis* application report (literature number SPRA839). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

## 7.4 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals must transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner. Monotonic transitions are more easily ensured with faster switching signals. Slower input transitions are more susceptible to glitches due to noise and special care should be taken for slow input clocks.

## 7.5 Virtual and Manual I/O Timing Modes

Some of the timings described in the following sections require the use of Virtual or Manual I/O Timing Modes. Table 7-2 provides a summary of the Virtual and Manual I/O Timing Modes across all device interfaces. The individual interface timing sections found later in this document provide the full description of each applicable Virtual and Manual I/O Timing Mode. Refer to the Pad Configuration section of the device TRM for the procedure on implementing the Virtual and Manual Timing Modes in a system.

**Table 7-2. Modes Summary**

| Virtual or Manual IO Mode Name | Data Manual Timing Mode |
|---|---|
| **VIP** | |
| VIP1_MANUAL1 | VIN1A/1B/2A Rise-Edge Capture Mode Timings |
| VIP1_2B_MANUAL1 | VIN2B Rise-Edge Capture Mode Timings |
| VIP1_MANUAL2 | VIN1A/1B/2A Fall-Edge Capture Mode Timings |
| VIP1_2B_MANUAL2 | VIN2B Fall-Edge Capture Mode Timings |
| VIP2_MANUAL1 | VIN3A, VIN3B IOSET1 Rise-Edge Capture Mode Timings |
| VIP2_4A_MANUAL1 | VIN4A IOSET1/2 Rise-Edge Capture Mode Timings |
| VIP2_4A_IOSET3_MANUAL1 | VIN4A IOSET3 Rise-Edge Capture Mode Timings |
| VIP2_4B_MANUAL1 | VIN4B Rise-Edge Capture Mode Timings |
| VIP2_3B_IOSET2_MANUAL1 | VIN3B IOSET2 Rise-Edge Capture Mode Timings |
| VIP2_3B_IOSET2_MANUAL2 | VIN3B IOSET2 Fall-Edge Capture Mode Timings |
| VIP2_MANUAL2 | VIN3A, VIN3B IOSET1, VIN4A IOSET1/2 Fall-Edge Capture Mode Timings |
| VIP2_4A_MANUAL2 | VIN4A IOSET1/2 Fall-Edge Capture Mode Timings |
| VIP2_4A_IOSET3_MANUAL2 | VIN4A IOSET3 Fall-Edge Capture Mode Timings |
| VIP2_4B_MANUAL2 | VIN4B Fall-Edge Capture Mode Timings |
| VIP3_MANUAL1 | VIN5A and VIN6A Rise-Edge Capture Mode Timings |
| VIP3_MANUAL2 | VIN5A and VIN6A Fall-Edge Capture Mode Timings |
| **DPI Video Output** | |
| VOUT1_MANUAL1 | DPI1 Video Output Alternate Timings |
| VOUT1_MANUAL2 | DPI1 Video Output Default Timings |
| VOUT1_MANUAL3 | DPI1 Video Output MANUAL3 Timings |
| VOUT1_MANUAL4 | DPI1 Video Output MANUAL4 Timings |
| VOUT2_IOSET1_MANUAL1 | DPI2 Video Output IOSET1 Alternate Timings |
| VOUT2_IOSET1_MANUAL2 | DPI2 Video Output IOSET1 Default Timings |

**Table 7-2. Modes Summary (continued)**

| Virtual or Manual IO Mode Name | Data Manual Timing Mode |
|---|---|
| VOUT2_IOSET1_MANUAL3 | DPI2 Video Output IOSET1 MANUAL3 Timings |
| VOUT2_IOSET1_MANUAL4 | DPI2 Video Output IOSET1 MANUAL4 Timings |
| VOUT2_IOSET2_MANUAL1 | DPI2 Video Output IOSET2 Alternate Timings |
| VOUT2_IOSET2_MANUAL2 | DPI2 Video Output IOSET2 Default Timings |
| VOUT2_IOSET2_MANUAL3 | DPI2 Video Output IOSET2 MANUAL3 Timings |
| VOUT2_IOSET2_MANUAL4 | DPI2 Video Output IOSET2 MANUAL4 Timings |
| VOUT3_MANUAL1 | DPI3 Video Output Alternate Timings |
| VOUT3_MANUAL2 | DPI3 Video Output Default Timings |
| VOUT3_MANUAL3 | DPI3 Video Output MANUAL3 Timings |
| VOUT3_MANUAL4 | DPI3 Video Output MANUAL4 Timings |
| **HDMI, EMIF, Timers, I2C, HDQ/1-Wire, UART, McSPI, USB, SATA, PCIe, DCAN, GPIO, KBD, PWM, JTAG, TPIU, RTC, SDMA, INTC** | |
| No Virtual or Manual IO Timing Mode Required | All Modes |
| **GPMC** | |
| No Virtual or Manual IO Timing Mode Required | GPMC Asyncronous Mode Timings and Synchronous Mode - Default Timings |
| GPMC_VIRTUAL1 | GPMC Synchronous Mode - Alternate Timings |
| **QSPI** | |
| No Virtual or Manual IO Timing Mode Required | QSPI Mode 3 Default Timing Mode |
| QSPI_MODE0_MANUAL1 | QSPI Mode 0 Default Timing Mode |
| **McASP** | |
| No Virtual or Manual IO Timing Mode Required | McASP1 Synchronous Transmit Timings |
| MCASP1_VIRTUAL1_ASYNC_TX | See Table 7-55 |
| MCASP1_VIRTUAL2_SYNC_RX | See Table 7-55 |
| MCASP1_VIRTUAL3_ASYNC_RX | See Table 7-55 |
| No Virtual or Manual IO Timing Mode Required | McASP2 Synchronous Transmit Timings |
| MCASP2_VIRTUAL1_ASYNC_RX_80M | See Table 7-56 |
| MCASP2_VIRTUAL2_ASYNC_RX | See Table 7-56 |
| MCASP2_VIRTUAL3_ASYNC_TX | See Table 7-56 |
| MCASP2_VIRTUAL4_SYNC_RX | See Table 7-56 |
| MCASP2_VIRTUAL5_SYNC_RX_80M | See Table 7-56 |
| No Virtual or Manual IO Timing Mode Required | McASP3 Synchronous Transmit Timings |
| MCASP3_VIRTUAL2_SYNC_RX | See Table 7-57 |
| No Virtual or Manual IO Timing Mode Required | McASP4 Synchronous Transmit Timings |
| MCASP4_VIRTUAL1_SYNC_RX | See Table 7-58 |
| No Virtual or Manual IO Timing Mode Required | McASP5 Synchronous Transmit Timings |
| MCASP5_VIRTUAL1_SYNC_RX | See Table 7-59 |
| No Virtual or Manual IO Timing Mode Required | McASP6 Synchronous Transmit Timings |
| MCASP6_VIRTUAL1_SYNC_RX | See Table 7-60 |
| No Virtual or Manual IO Timing Mode Required | McASP7 Synchronous Transmit Timings |
| MCASP7_VIRTUAL2_SYNC_RX | See Table 7-61 |
| No Virtual or Manual IO Timing Mode Required | McASP8 Synchronous Transmit Timings |


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**Table 7-2. Modes Summary (continued)**

| Virtual or Manual IO Mode Name | Data Manual Timing Mode |
|---|---|
| MCASP8_VIRTUAL1_SYNC_RX | See Table 7-62 |
| **GMAC** | |
| No Virtual or Manual IO Timing Mode Required | GMAC MII0 and MII1 |
| GMAC_RMII0_MANUAL1 | GMAC RMII0 Timings |
| GMAC_RMII1_MANUAL1 | GMAC RMII1 Timings |
| GMAC_RGMII0_MANUAL1 | GMAC RGMII0 Internal Delay Enabled Timings Mode |
| GMAC_RGMII1_MANUAL1 | GMAC RGMII1 Internal Delay Enabled Timings Mode |
| **eMMC/SD/SDIO** | |
| No Virtual or Manual IO Timing Mode Required | MMC1 DS (Pad Loopback) and SDR12 (Pad Loopback) Timings |
| MMC1_VIRTUAL1 | MMC1 HS (Internal Loopback and Pad Loopback), SDR12 (Internal Loopback), SDR25 Timings (Internal Loopback and Pad Loopback) |
| MMC1_VIRTUAL2 | SDR50 (Pad Loopback) Timings |
| MMC1_VIRTUAL5 | MMC1 DS (Internal Loopback) Timings |
| MMC1_VIRTUAL6 | MMC1 SDR50 (Internal Loopback) Timings |
| MMC1_VIRTUAL7 | MMC1 DDR50 (Internal Loopback) Timings |
| MMC1_DDR_MANUAL1 | MMC1 DDR50 (Pad Loopback) Timings |
| MMC1_SDR104_MANUAL1 | MMC1 SDR104 Timings |
| No Virtual or Manual IO Timing Mode Required | MMC2 Standard (Pad Loopback), High Speed (Pad Loopback), and DDR (Pad Loopback) Timings |
| MMC2_DDR_LB_MANUAL1 | MMC2 DDR (Internal Loopback) Timings |
| MMC2_HS200_MANUAL1 | MMC2 HS200 Timings |
| MMC2_STD_HS_LB_MANUAL1 | MMC2 Standard (Internal Loopback), High Speed (Internal Loopback) Timings |
| MMC3_MANUAL1 | MMC3 DS, SDR12, HS, SDR25 Timings, SDR50 Timings |
| MMC4_MANUAL1 | MMC4 SDR12, HS, SDR25 Timings |
| MMC4_DS_MANUAL1 | MMC4 DS Timings |
| **PRU-ICSS** | |
| PR1_PRU0_DIR_OUT_MANUAL | PRU-ICSS1 PRU0 Direct Output Mode Timings |
| PR1_PRU1_DIR_OUT_MANUAL | PRU-ICSS1 PRU1 Direct Output Mode Timings |
| PR1_PRU0_DIR_IN_MANUAL | PRU-ICSS1 PRU0 Direct Input Mode Timings |
| PR1_PRU1_DIR_IN_MANUAL | PRU-ICSS1 PRU1 Direct Input Mode Timings |
| PR1_PRU0_PAR_CAP_MANUAL | PRU-ICSS1 PRU0 Parallel Capture Mode Timings |
| PR1_PRU1_PAR_CAP_MANUAL | PRU-ICSS1 PRU1 Parallel Capture Mode Timings |
| PR2_PRU0_DIR_IN_MANUAL1 | PRU-ICSS2 PRU0 IOSET1 Direct Input Mode Timings |
| PR2_PRU0_DIR_IN_MANUAL2 | PRU-ICSS2 PRU0 IOSET2 Direct Input Mode Timings |
| PR2_PRU0_DIR_OUT_MANUAL1 | PRU-ICSS2 PRU0 IOSET1 Direct Output Mode Timings |
| PR2_PRU0_DIR_OUT_MANUAL2 | PRU-ICSS2 PRU0 IOSET2 Direct Output Mode Timings |
| PR2_PRU1_DIR_IN_MANUAL1 | PRU-ICSS2 PRU1 IOSET1 Direct Input Mode Timings |
| PR2_PRU1_DIR_IN_MANUAL2 | PRU-ICSS2 PRU1 IOSET2 Direct Input Mode Timings |
| PR2_PRU1_DIR_OUT_MANUAL1 | PRU-ICSS2 PRU1 IOSET1 Direct Output Mode Timings |
| PR2_PRU1_DIR_OUT_MANUAL2 | PRU-ICSS2 PRU1 IOSET2 Direct Output Mode Timings |
| PR2_PRU0_PAR_CAP_MANUAL1 | PRU-ICSS2 PRU0 IOSET1 Parallel Capture Mode Timings |
| PR2_PRU0_PAR_CAP_MANUAL2 | PRU-ICSS2 PRU0 IOSET2 Parallel Capture Mode Timings |
| PR2_PRU1_PAR_CAP_MANUAL1 | PRU-ICSS2 PRU1 IOSET1 Parallel Capture Mode Timings |
| PR2_PRU1_PAR_CAP_MANUAL2 | PRU-ICSS2 PRU1 IOSET2 Parallel Capture Mode Timings |

## 7.6 Video Input Ports (VIP)

The Device includes 3 Video Input Ports (VIP).

Table 7-3, Figure 7-4 and Figure 7-5 present timings and switching characteristics of the VIPs.

**CAUTION**

The IO timings provided in this section are applicable for all combinations of signals for vin1, vin5 and vin6. However, the timings are only valid for vin2, vin3, and vin4 if signals within a single IOSET are used. The IOSETs are defined in the Table 7-4.

**Table 7-3. Timing Requirements for VIP (1)(2)**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| V1 | $t_{c(CLK)}$ | Cycle time, vin*x*_clk*i* (3) (5) | | 6.06 (1) | | ns |
| V2 | $t_{w(CLKH)}$ | Pulse duration, vin*x*_clk*i* high (3) (5) | | 0.45*P (2) | | ns |
| V3 | $t_{w(CLKL)}$ | Pulse duration, vin*x*_clk*i* low (3) (5) | | 0.45*P (2) | | ns |
| V4 | $t_{su(CTL/DATA-CLK)}$ | Input setup time, Control (vin*x*_de*i*, vin*x*_vsync*i*, vin*x*_fld*i*, vin*x*_hsync*i*) and Data (vin*x*_d*n*) valid to vin*x*_clk*i* transition (3) (4) (5) | vin1*x*, vin2*x* | 2.93 | | ns |
| | | | vin5*x*, vin6*x* | 3.11 | | ns |
| | | | vin3*x*, vin4*x* | 3.11 | | ns |
| V5 | $t_{h(CLK-CTL/DATA)}$ | Input hold time, Control (vin*x*_de*i*, vin*x*_vsync*i*, vin*x*_fld*i*, vin*x*_hsync*i*) and Data (vin*x*_d*n*) valid from vin*x*_clk*i* transition (3) (4) (5) | | -0.05 | | ns |

(1) For maximum frequency of 165 MHz.

(2) P = vin*x*_clk*i* period.

(3) *x* in vin*x* = 1a, 1b, 2a, 2b, 3a, 3b, 4a, 4b, 5a and 6a.

(4) *n* in d*n* = 0 to 7 when x = 1b, 2b, 3b and 4b;
*n* = 0 to 15 when *x* = 5a and 6a;
*n* = 0 to 23 when *x* = 1a, 2a, 3a and 4a;

(5) *i* in clk*i*, de*i*, vsync*i*, hsync*i* and fld*i* = 0 or 1.

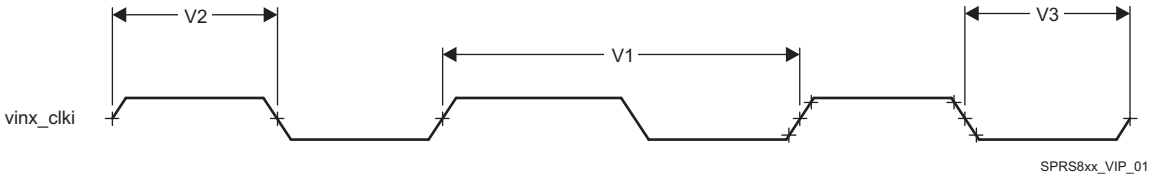


**Figure 7-4. Video Input Ports Clock Signal**


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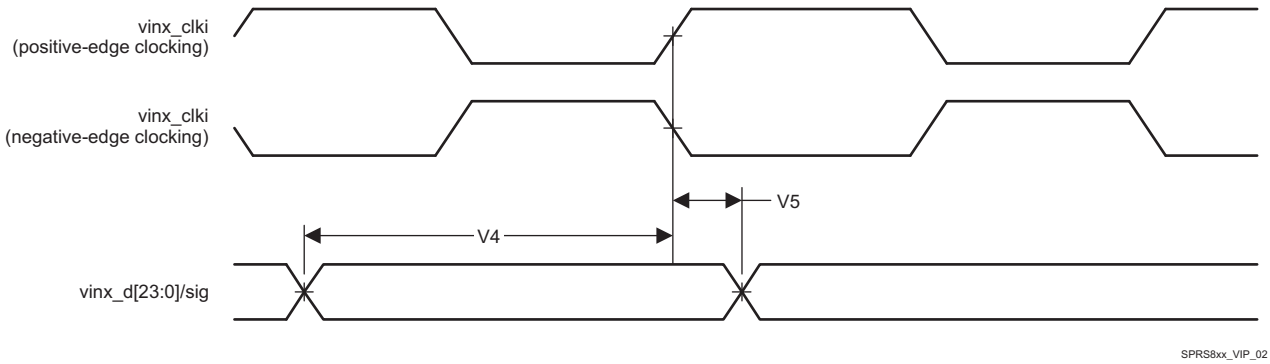


**Figure 7-5. Video Input Ports Timings**

In Table 7-4,Table 7-5 and Table 7-6 are presented the specific groupings of signals (IOSET) for use with vin2, vin3, and vin4.

**Table 7-4. VIN2 IOSETs**

| Signals | IOSET1 | | IOSET2 | | IOSET3 | |
|---|---|---|---|---|---|---|
| | BALL | MUX | BALL | MUX | BALL | MUX |
| **vin2a** | | | | | | |
| vin2a_d0 | F2 | 0 | F2 | 0 | U4 | 4 |
| vin2a_d1 | F3 | 0 | F3 | 0 | V2 | 4 |
| vin2a_d2 | D1 | 0 | D1 | 0 | Y1 | 4 |
| vin2a_d3 | E2 | 0 | E2 | 0 | W9 | 4 |
| vin2a_d4 | D2 | 0 | D2 | 0 | V9 | 4 |
| vin2a_d5 | F4 | 0 | F4 | 0 | U5 | 4 |
| vin2a_d6 | C1 | 0 | C1 | 0 | V5 | 4 |
| vin2a_d7 | E4 | 0 | E4 | 0 | V4 | 4 |
| vin2a_d8 | F5 | 0 | F5 | 0 | V3 | 4 |
| vin2a_d9 | E6 | 0 | E6 | 0 | Y2 | 4 |
| vin2a_d10 | D3 | 0 | D3 | 0 | U6 | 4 |
| vin2a_d11 | F6 | 0 | F6 | 0 | U3 | 4 |
| vin2a_d12 | D5 | 0 | D5 | 0 | - | - |
| vin2a_d13 | C2 | 0 | C2 | 0 | - | - |
| vin2a_d14 | C3 | 0 | C3 | 0 | - | - |
| vin2a_d15 | C4 | 0 | C4 | 0 | - | - |
| vin2a_d16 | B2 | 0 | B2 | 0 | - | - |
| vin2a_d17 | D6 | 0 | D6 | 0 | - | - |
| vin2a_d18 | C5 | 0 | C5 | 0 | - | - |
| vin2a_d19 | A3 | 0 | A3 | 0 | - | - |
| vin2a_d20 | B3 | 0 | B3 | 0 | - | - |
| vin2a_d21 | B4 | 0 | B4 | 0 | - | - |
| vin2a_d22 | B5 | 0 | B5 | 0 | - | - |
| vin2a_d23 | A4 | 0 | A4 | 0 | - | - |
| vin2a_hsync0 | G1 | 0 | G1 | 0 | U7 | 4 |
| vin2a_vsync0 | G6 | 0 | G6 | 0 | V6 | 4 |
| vin2a_de0 | G2 | 0 | - | - | V7 | 4 |
| vin2a_fld0 | H7 | 0 | G2 | 1 | W2 | 4 |
| vin2a_clk0 | E1 | 0 | E1 | 0 | V1 | 4 |
| **vin2b** | | | | | | |

### Table 7-4. VIN2 IOSETs (continued)

| Signals | IOSET1 | | IOSET2 | | IOSET3 | |
|---|---|---|---|---|---|---|
| | BALL | MUX | BALL | MUX | BALL | MUX |
| vin2b_clk1 | H7 | 2 | H7 | 2 | AB5 | 4 |
| vin2b_de1 | - | - | G2 | 3 | AB8 | 4 |
| vin2b_fld1 | G2 | 2 | - | - | - | - |
| vin2b_d0 | A4 | 2 | A4 | 2 | AD6 | 4 |
| vin2b_d1 | B5 | 2 | B5 | 2 | AC8 | 4 |
| vin2b_d2 | B4 | 2 | B4 | 2 | AC3 | 4 |
| vin2b_d3 | B3 | 2 | B3 | 2 | AC9 | 4 |
| vin2b_d4 | A3 | 2 | A3 | 2 | AC6 | 4 |
| vin2b_d5 | C5 | 2 | C5 | 2 | AC7 | 4 |
| vin2b_d6 | D6 | 2 | D6 | 2 | AC4 | 4 |
| vin2b_d7 | B2 | 2 | B2 | 2 | AD4 | 4 |
| vin2b_hsync1 | G1 | 3 | G1 | 3 | AC5 | 4 |
| vin2b_vsync1 | G6 | 3 | G6 | 3 | AB4 | 4 |

### Table 7-5. VIN3 IOSETs

| Signals | IOSET1 | | IOSET2 | | IOSET3 | | IOSET4 | |
|---|---|---|---|---|---|---|---|---|
| | BALL | MUX | BALL | MUX | BALL | MUX | BALL | MUX |
| **vin3a** | | | | | | | | |
| vin3a_d0 | M6 | 2 | AF1 | 6 | AF1 | 6 | B7 | 4 |
| vin3a_d1 | M2 | 2 | AE3 | 6 | AE3 | 6 | B8 | 4 |
| vin3a_d2 | L5 | 2 | AE5 | 6 | AE5 | 6 | A7 | 4 |
| vin3a_d3 | M1 | 2 | AE1 | 6 | AE1 | 6 | A8 | 4 |
| vin3a_d4 | L6 | 2 | AE2 | 6 | AE2 | 6 | C9 | 4 |
| vin3a_d5 | L4 | 2 | AE6 | 6 | AE6 | 6 | A9 | 4 |
| vin3a_d6 | L3 | 2 | AD2 | 6 | AD2 | 6 | B9 | 4 |
| vin3a_d7 | L2 | 2 | AD3 | 6 | AD3 | 6 | A10 | 4 |
| vin3a_d8 | L1 | 2 | B2 | 6 | B2 | 6 | E8 | 4 |
| vin3a_d9 | K2 | 2 | D6 | 6 | D6 | 6 | D9 | 4 |
| vin3a_d10 | J1 | 2 | C5 | 6 | C5 | 6 | D7 | 4 |
| vin3a_d11 | J2 | 2 | A3 | 6 | A3 | 6 | D8 | 4 |
| vin3a_d12 | H1 | 2 | B3 | 6 | - | - | A5 | 4 |
| vin3a_d13 | J3 | 2 | B4 | 6 | - | - | C6 | 4 |
| vin3a_d14 | H2 | 2 | B5 | 6 | - | - | C8 | 4 |
| vin3a_d15 | H3 | 2 | A4 | 6 | - | - | C7 | 4 |
| vin3a_d16 | R6 | 2 | - | - | - | - | F11 | 4 |
| vin3a_d17 | T9 | 2 | - | - | - | - | G10 | 4 |
| vin3a_d18 | T6 | 2 | - | - | - | - | F10 | 4 |
| vin3a_d19 | T7 | 2 | - | - | - | - | G11 | 4 |
| vin3a_d20 | P6 | 2 | - | - | - | - | E9 | 4 |
| vin3a_d21 | R9 | 2 | - | - | - | - | F9 | 4 |
| vin3a_d22 | R5 | 2 | - | - | - | - | F8 | 4 |
| vin3a_d23 | P5 | 2 | - | - | - | - | E7 | 4 |
| vin3a_hsync0 | N7 | 2 | N7 | 2 | B5 | 5 | C11 | 4 |
| vin3a_vsync0 | R4 | 2 | R4 | 2 | A4 | 5 | E11 | 4 |
| vin3a_de0 | N9 | 2 | N9 | 2 | B3 | 5 | B10 | 4 |
| vin3a_fld0 | P9 | 2 | P9 | 2 | B4 | 5 | D11 | 4 |


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### Table 7-5. VIN3 IOSETs (continued)

| Signals | IOSET1 | | IOSET2 | | IOSET3 | | IOSET4 | |
|---|---|---|---|---|---|---|---|---|
| | BALL | MUX | BALL | MUX | BALL | MUX | BALL | MUX |
| vin3a_clk0 | P1 | 2 | AH7 | 6 | AH7 | 6 | B11 | 4 |
| **vin3b** | | | | | | | | |
| vin3b_clk1 | P7 | 6 | M4 | 4 | - | - | - | - |
| vin3b_de1 | N6 | 6 | N6 | 6 | - | - | - | - |
| vin3b_fld1 | M4 | 6 | - | - | - | - | - | - |
| vin3b_d0 | K7 | 6 | K7 | 6 | - | - | - | - |
| vin3b_d1 | M7 | 6 | M7 | 6 | - | - | - | - |
| vin3b_d2 | J5 | 6 | J5 | 6 | - | - | - | - |
| vin3b_d3 | K6 | 6 | K6 | 6 | - | - | - | - |
| vin3b_d4 | J7 | 6 | J7 | 6 | - | - | - | - |
| vin3b_d5 | J4 | 6 | J4 | 6 | - | - | - | - |
| vin3b_d6 | J6 | 6 | J6 | 6 | - | - | - | - |
| vin3b_d7 | H4 | 6 | H4 | 6 | - | - | - | - |
| vin3b_hsync1 | H5 | 6 | H5 | 6 | - | - | - | - |
| vin3b_vsync1 | H6 | 6 | H6 | 6 | - | - | - | - |

### Table 7-6. VIN4 IOSETs

| Signals | IOSET1 | | IOSET2 | | IOSET3 | |
|---|---|---|---|---|---|---|
| | BALL | MUX | BALL | MUX | BALL | MUX |
| **vin4a** | | | | | | |
| vin4a_d0 | R6 | 4 | B7 | 3 | B14 | 8 |
| vin4a_d1 | T9 | 4 | B8 | 3 | J14 | 8 |
| vin4a_d2 | T6 | 4 | A7 | 3 | G13 | 8 |
| vin4a_d3 | T7 | 4 | A8 | 3 | J11 | 8 |
| vin4a_d4 | P6 | 4 | C9 | 3 | E12 | 8 |
| vin4a_d5 | R9 | 4 | A9 | 3 | F13 | 8 |
| vin4a_d6 | R5 | 4 | B9 | 3 | C12 | 8 |
| vin4a_d7 | P5 | 4 | A10 | 3 | D12 | 8 |
| vin4a_d8 | U2 | 4 | E8 | 3 | E15 | 8 |
| vin4a_d9 | U1 | 4 | D9 | 3 | A20 | 8 |
| vin4a_d10 | P3 | 4 | D7 | 3 | B15 | 8 |
| vin4a_d11 | R2 | 4 | D8 | 3 | A15 | 8 |
| vin4a_d12 | K7 | 4 | A5 | 3 | D15 | 8 |
| vin4a_d13 | M7 | 4 | C6 | 3 | B16 | 8 |
| vin4a_d14 | J5 | 4 | C8 | 3 | B17 | 8 |
| vin4a_d15 | K6 | 4 | C7 | 3 | A17 | 8 |
| vin4a_d16 | - | - | F11 | 3 | C18 | 8 |
| vin4a_d17 | - | - | G10 | 3 | A21 | 8 |
| vin4a_d18 | - | - | F10 | 3 | G16 | 8 |
| vin4a_d19 | - | - | G11 | 3 | D17 | 8 |
| vin4a_d20 | - | - | E9 | 3 | AA3 | 8 |
| vin4a_d21 | - | - | F9 | 3 | AB9 | 8 |
| vin4a_d22 | - | - | F8 | 3 | AB3 | 8 |
| vin4a_d23 | - | - | E7 | 3 | AA4 | 8 |
| vin4a_hsync0 | R3/ P7 | 4 / 4 | C11 | 3 | E21 | 8 |
| vin4a_vsync0 | T2/ N1 | 4 / 4 | E11 | 3 | F20 | 8 |

**Table 7-6. VIN4 IOSETs (continued)**

| Signals | IOSET1 | | IOSET2 | | IOSET3 | |
|---|---|---|---|---|---|---|
| | BALL | MUX | BALL | MUX | BALL | MUX |
| vin4a_de0 | H6/ P7 | 4 / 5 | B10 | 3 | C23 | 8 |
| vin4a_fld0 | P9/ J7 | 4 / 4 | D11 | 3 | F21 | 8 |
| vin4a_clk0 | P4 | 4 | B11 | 3 | B26 | 8 |
| **vin4b** | | | | | | |
| vin4b_clk1 | N9 | 6 | V1 | 5 | - | - |
| vin4b_de1 | P9 | 6 | V7 | 5 | - | - |
| vin4b_fld1 | P4 | 6 | W2 | 5 | - | - |
| vin4b_d0 | R6 | 6 | U4 | 5 | - | - |
| vin4b_d1 | T9 | 6 | V2 | 5 | - | - |
| vin4b_d2 | T6 | 6 | Y1 | 5 | - | - |
| vin4b_d3 | T7 | 6 | W9 | 5 | - | - |
| vin4b_d4 | P6 | 6 | V9 | 5 | - | - |
| vin4b_d5 | R9 | 6 | U5 | 5 | - | - |
| vin4b_d6 | R5 | 6 | V5 | 5 | - | - |
| vin4b_d7 | P5 | 6 | V4 | 5 | - | - |
| vin4b_hsync1 | N7 | 6 | U7 | 5 | - | - |
| vin4b_vsync1 | R4 | 6 | V6 | 5 | - | - |

**NOTE**

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the Control Module chapter in the Device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for VIP1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-7 *Manual Functions Mapping for VIP1* for a definition of the Manual modes.

Table 7-7 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.


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### Table 7-7. Manual Functions Mapping for VIP1

| BALL | BALL NAME | VIP1_MANUAL1 | | VIP1_MANUAL2 | | CFG REGISTER | MUXMODE | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 0 | 1 | 2 | 3 | 4 |
| U3 | RMII_MHZ_50_CLK | 1621 | 614 | 2018 | 279 | CFG_RMII_MHZ_50_CLK_IN | - | - | - | - | vin2a_d11 |
| N6 | gpmc_ben0 | 1756 | 1019 | 2235 | 494 | CFG_GPMC_BEN0_IN | - | - | - | vin1b_hsync1 | - |
| M4 | gpmc_ben1 | 1684 | 1107 | 2198 | 568 | CFG_GPMC_BEN1_IN | - | - | - | vin1b_de1 | - |
| U4 | mdio_d | 1594 | 417 | 2007 | 36 | CFG_MDIO_D_IN | - | - | - | - | vin2a_d0 |
| V1 | mdio_mclk | 0 | 0 | 0 | 0 | CFG_MDIO_MCLK_IN | - | - | - | - | vin2a_clk0 |
| U5 | rgmii0_rxc | 1005 | 935 | 1932 | 0 | CFG_RGMII0_RXC_IN | - | - | - | - | vin2a_d5 |
| V5 | rgmii0_rxctl | 1579 | 836 | 1982 | 485 | CFG_RGMII0_RXCTL_IN | - | - | - | - | vin2a_d6 |
| W2 | rgmii0_rxd0 | 1032 | 1033 | 1995 | 0 | CFG_RGMII0_RXD0_IN | - | - | - | - | vin2a_fld0 |
| Y2 | rgmii0_rxd1 | 950 | 1625 | 1993 | 673 | CFG_RGMII0_RXD1_IN | - | - | - | - | vin2a_d9 |
| V3 | rgmii0_rxd2 | 1578 | 832 | 1973 | 535 | CFG_RGMII0_RXD2_IN | - | - | - | - | vin2a_d8 |
| V4 | rgmii0_rxd3 | 1022 | 1648 | 2017 | 740 | CFG_RGMII0_RXD3_IN | - | - | - | - | vin2a_d7 |
| W9 | rgmii0_txc | 1604 | 769 | 2020 | 393 | CFG_RGMII0_TXC_IN | - | - | - | - | vin2a_d3 |
| V9 | rgmii0_txctl | 1060 | 1389 | 2074 | 396 | CFG_RGMII0_TXCTL_IN | - | - | - | - | vin2a_d4 |
| U6 | rgmii0_txd0 | 938 | 1242 | 2021 | 194 | CFG_RGMII0_TXD0_IN | - | - | - | - | vin2a_d10 |
| V6 | rgmii0_txd1 | 1013 | 1679 | 2036 | 730 | CFG_RGMII0_TXD1_IN | - | - | - | - | vin2a_vsync0 |
| U7 | rgmii0_txd2 | 1524 | 886 | 1933 | 526 | CFG_RGMII0_TXD2_IN | - | - | - | - | vin2a_hsync0 |
| V7 | rgmii0_txd3 | 1079 | 1504 | 2090 | 490 | CFG_RGMII0_TXD3_IN | - | - | - | - | vin2a_de0 |
| V2 | uart3_rxd | 1530 | 125 | 1586 | 0 | CFG_UART3_RXD_IN | - | - | - | - | vin2a_d1 |
| Y1 | uart3_txd | 1572 | 487 | 1980 | 16 | CFG_UART3_TXD_IN | - | - | - | - | vin2a_d2 |
| AG8 | vin1a_clk0 | 0 | 0 | 0 | 0 | CFG_VIN1A_CLK0_IN | vin1a_clk0 | - | - | - | - |
| AE8 | vin1a_d0 | 1697 | 1087 | 2105 | 619 | CFG_VIN1A_D0_IN | vin1a_d0 | - | - | - | - |
| AD8 | vin1a_d1 | 1589 | 1164 | 2017 | 757 | CFG_VIN1A_D1_IN | vin1a_d1 | - | - | - | - |
| AG3 | vin1a_d10 | 1733 | 1119 | 2107 | 739 | CFG_VIN1A_D10_IN | vin1a_d10 | vin1b_d5 | - | - | - |
| AG5 | vin1a_d11 | 1563 | 1210 | 2005 | 788 | CFG_VIN1A_D11_IN | vin1a_d11 | vin1b_d4 | - | - | - |
| AF2 | vin1a_d12 | 1705 | 1647 | 2059 | 1297 | CFG_VIN1A_D12_IN | vin1a_d12 | vin1b_d3 | - | - | - |
| AF6 | vin1a_d13 | 1624 | 1525 | 2027 | 1141 | CFG_VIN1A_D13_IN | vin1a_d13 | vin1b_d2 | - | - | - |
| AF3 | vin1a_d14 | 1730 | 1655 | 2071 | 1332 | CFG_VIN1A_D14_IN | vin1a_d14 | vin1b_d1 | - | - | - |
| AF4 | vin1a_d15 | 1681 | 2004 | 1995 | 1764 | CFG_VIN1A_D15_IN | vin1a_d15 | vin1b_d0 | - | - | - |
| AF1 | vin1a_d16 | 1659 | 1813 | 1999 | 1542 | CFG_VIN1A_D16_IN | vin1a_d16 | vin1b_d7 | - | - | - |
| AE3 | vin1a_d17 | 1715 | 1887 | 2072 | 1540 | CFG_VIN1A_D17_IN | vin1a_d17 | vin1b_d6 | - | - | - |

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### Table 7-7. Manual Functions Mapping for VIP1 (continued)

| BALL | BALL NAME | VIP1_MANUAL1 | | VIP1_MANUAL2 | | CFG REGISTER | MUXMODE | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 0 | 1 | 2 | 3 | 4 |
| AE5 | vin1a_d18 | 1728 | 1898 | 2034 | 1629 | CFG_VIN1A_D18_IN | vin1a_d18 | vin1b_d5 | - | - | - |
| AE1 | vin1a_d19 | 1707 | 2006 | 2026 | 1761 | CFG_VIN1A_D19_IN | vin1a_d19 | vin1b_d4 | - | - | - |
| AG7 | vin1a_d2 | 1557 | 1414 | 1996 | 962 | CFG_VIN1A_D2_IN | vin1a_d2 | - | - | - | - |
| AE2 | vin1a_d20 | 1695 | 1814 | 2037 | 1469 | CFG_VIN1A_D20_IN | vin1a_d20 | vin1b_d3 | - | - | - |
| AE6 | vin1a_d21 | 1757 | 1682 | 2077 | 1349 | CFG_VIN1A_D21_IN | vin1a_d21 | vin1b_d2 | - | - | - |
| AD2 | vin1a_d22 | 1683 | 1813 | 2022 | 1545 | CFG_VIN1A_D22_IN | vin1a_d22 | vin1b_d1 | - | - | - |
| AD3 | vin1a_d23 | 1833 | 1187 | 2168 | 784 | CFG_VIN1A_D23_IN | vin1a_d23 | vin1b_d0 | - | - | - |
| AH6 | vin1a_d3 | 1588 | 1289 | 1993 | 901 | CFG_VIN1A_D3_IN | vin1a_d3 | - | - | - | - |
| AH3 | vin1a_d4 | 1687 | 949 | 2098 | 499 | CFG_VIN1A_D4_IN | vin1a_d4 | - | - | - | - |
| AH5 | vin1a_d5 | 1616 | 1257 | 2038 | 844 | CFG_VIN1A_D5_IN | vin1a_d5 | - | - | - | - |
| AG6 | vin1a_d6 | 1582 | 1265 | 2002 | 863 | CFG_VIN1A_D6_IN | vin1a_d6 | - | - | - | - |
| AH4 | vin1a_d7 | 1659 | 1255 | 2063 | 873 | CFG_VIN1A_D7_IN | vin1a_d7 | - | - | - | - |
| AG4 | vin1a_d8 | 1681 | 1205 | 2088 | 759 | CFG_VIN1A_D8_IN | vin1a_d8 | vin1b_d7 | - | - | - |
| AG2 | vin1a_d9 | 1778 | 1168 | 2152 | 701 | CFG_VIN1A_D9_IN | vin1a_d9 | vin1b_d6 | - | - | - |
| AD9 | vin1a_de0 | 1468 | 1290 | 1926 | 728 | CFG_VIN1A_DE0_IN | vin1a_de0 | vin1b_hsync 1 | - | - | - |
| AF9 | vin1a_fld0 | 1633 | 1425 | 2043 | 937 | CFG_VIN1A_FLD0_IN | vin1a_fld0 | vin1b_vsync1 | - | - | - |
| AE9 | vin1a_hsync0 | 1561 | 1424 | 1978 | 909 | CFG_VIN1A_HSYNC0_IN | vin1a_hsync 0 | vin1b_fld1 | - | - | - |
| AF8 | vin1a_vsync0 | 1470 | 1369 | 1926 | 987 | CFG_VIN1A_VSYNC0_IN | vin1a_vsync0 | vin1b_de1 | - | - | - |
| AH7 | vin1b_clk1 | 69 | 150 | 242 | 0 | CFG_VIN1B_CLK1_IN | vin1b_clk1 | - | - | - | - |
| E1 | vin2a_clk0 | 0 | 0 | 0 | 0 | CFG_VIN2A_CLK0_IN | vin2a_clk0 | - | - | - | - |
| F2 | vin2a_d0 | 1597 | 561 | 2009 | 147 | CFG_VIN2A_D0_IN | vin2a_d0 | - | - | - | - |
| F3 | vin2a_d1 | 1598 | 801 | 2015 | 561 | CFG_VIN2A_D1_IN | vin2a_d1 | - | - | - | - |
| D3 | vin2a_d10 | 1576 | 655 | 2021 | 377 | CFG_VIN2A_D10_IN | vin2a_d10 | - | - | - | - |
| F6 | vin2a_d11 | 1488 | 340 | 1940 | 19 | CFG_VIN2A_D11_IN | vin2a_d11 | - | - | - | - |
| D5 | vin2a_d12 | 1399 | 612 | 1895 | 181 | CFG_VIN2A_D12_IN | vin2a_d12 | - | - | - | - |
| C2 | vin2a_d13 | 1595 | 439 | 2063 | 15 | CFG_VIN2A_D13_IN | vin2a_d13 | - | - | - | - |
| C3 | vin2a_d14 | 1480 | 243 | 1709 | 0 | CFG_VIN2A_D14_IN | vin2a_d14 | - | - | - | - |
| C4 | vin2a_d15 | 1415 | 755 | 1899 | 369 | CFG_VIN2A_D15_IN | vin2a_d15 | - | - | - | - |
| B2 | vin2a_d16 | 1341 | 653 | 1821 | 317 | CFG_VIN2A_D16_IN | vin2a_d16 | - | vin2b_d7 | - | - |
| D6 | vin2a_d17 | 1396 | 724 | 1880 | 349 | CFG_VIN2A_D17_IN | vin2a_d17 | - | vin2b_d6 | - | - |


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**Table 7-7. Manual Functions Mapping for VIP1 (continued)**

| BALL | BALL NAME | VIP1_MANUAL1 | | VIP1_MANUAL2 | | CFG REGISTER | MUXMODE | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 0 | 1 | 2 | 3 | 4 |
| C5 | vin2a_d18 | 1582 | 364 | 1963 | 0 | CFG_VIN2A_D18_IN | vin2a_d18 | - | vin2b_d5 | - | - |
| A3 | vin2a_d19 | 1308 | 289 | 1681 | 0 | CFG_VIN2A_D19_IN | vin2a_d19 | - | vin2b_d4 | - | - |
| D1 | vin2a_d2 | 1600 | 323 | 2021 | 0 | CFG_VIN2A_D2_IN | vin2a_d2 | - | - | - | - |
| B3 | vin2a_d20 | 1307 | 586 | 1772 | 299 | CFG_VIN2A_D20_IN | vin2a_d20 | - | vin2b_d3 | - | - |
| B4 | vin2a_d21 | 1301 | 640 | 1787 | 282 | CFG_VIN2A_D21_IN | vin2a_d21 | - | vin2b_d2 | - | - |
| B5 | vin2a_d22 | 1316 | 534 | 1789 | 223 | CFG_VIN2A_D22_IN | vin2a_d22 | - | vin2b_d1 | - | - |
| A4 | vin2a_d23 | 1311 | 613 | 1788 | 286 | CFG_VIN2A_D23_IN | vin2a_d23 | - | vin2b_d0 | - | - |
| E2 | vin2a_d3 | 1765 | 720 | 2142 | 492 | CFG_VIN2A_D3_IN | vin2a_d3 | - | - | - | - |
| D2 | vin2a_d4 | 1680 | 282 | 2071 | 0 | CFG_VIN2A_D4_IN | vin2a_d4 | - | - | - | - |
| F4 | vin2a_d5 | 1791 | 696 | 2155 | 461 | CFG_VIN2A_D5_IN | vin2a_d5 | - | - | - | - |
| C1 | vin2a_d6 | 1538 | 175 | 1849 | 0 | CFG_VIN2A_D6_IN | vin2a_d6 | - | - | - | - |
| E4 | vin2a_d7 | 1546 | 451 | 1977 | 192 | CFG_VIN2A_D7_IN | vin2a_d7 | - | - | - | - |
| F5 | vin2a_d8 | 1522 | 650 | 1966 | 391 | CFG_VIN2A_D8_IN | vin2a_d8 | - | - | - | - |
| E6 | vin2a_d9 | 1546 | 578 | 1996 | 270 | CFG_VIN2A_D9_IN | vin2a_d9 | - | - | - | - |
| G2 | vin2a_de0 | 1548 | 623 | 2036 | 213 | CFG_VIN2A_DE0_IN | vin2a_de0 | vin2a_fld0 | vin2b_fld1 | vin2b_de1 | - |
| H7 | vin2a_fld0 | 1771 | 815 | 2162 | 566 | CFG_VIN2A_FLD0_IN | vin2a_fld0 | - | vin2b_clk1 | - | - |
| G1 | vin2a_hsync0 | 1703 | 587 | 2071 | 225 | CFG_VIN2A_HSYNC0_IN | vin2a_hsync 0 | - | - | vin2b_hsync 1 | - |
| G6 | vin2a_vsync0 | 1486 | 464 | 1895 | 53 | CFG_VIN2A_VSYNC0_IN | vin2a_vsync0 | - | - | vin2b_vsync1 | - |

Manual IO Timings Modes must be used to ensure some IO timings for VIP1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-8 *Manual Functions Mapping for VIP1 2B* for a definition of the Manual modes.

Table 7-8 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-8. Manual Functions Mapping for VIP1 2B**

| BALL | BALL NAME | VIP1_2B_MANUAL1 | | VIP1_2B_MANUAL2 | | CFG REGISTER | MUXMODE | | |
|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 2 | 3 | 4 |
| AC5 | gpio6_10 | 1830 | 911 | 2136 | 593 | CFG_GPIO6_10_IN | - | - | vin2b_hsync1 |
| AB4 | gpio6_11 | 1797 | 1159 | 2088 | 926 | CFG_GPIO6_11_IN | - | - | vin2b_vsync1 |
| AD4 | mmc3_clk | (1) | (1) | (1) | (1) | CFG_MMC3_CLK_IN | - | - | vin2b_d7 |
| AC4 | mmc3_cmd | 1769 | 980 | 2092 | 650 | CFG_MMC3_CMD_IN | - | - | vin2b_d6 |
| AC7 | mmc3_dat0 | 1678 | 984 | 2027 | 691 | CFG_MMC3_DAT0_IN | - | - | vin2b_d5 |

**Table 7-8. Manual Functions Mapping for VIP1 2B (continued)**

| BALL | BALL NAME | VIP1_2B_MANUAL1 | | VIP1_2B_MANUAL2 | | CFG REGISTER | MUXMODE | | |
|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 2 | 3 | 4 |
| AC6 | mmc3_dat1 | 1664 | 883 | 2031 | 491 | CFG_MMC3_DAT1_IN | - | - | vin2b_d4 |
| AC9 | mmc3_dat2 | 1672 | 439 | 2065 | 0 | CFG_MMC3_DAT2_IN | - | - | vin2b_d3 |
| AC3 | mmc3_dat3 | 1762 | 1078 | 2089 | 799 | CFG_MMC3_DAT3_IN | - | - | vin2b_d2 |
| AC8 | mmc3_dat4 | 1766 | 583 | 2125 | 135 | CFG_MMC3_DAT4_IN | - | - | vin2b_d1 |
| AD6 | mmc3_dat5 | 1777 | 577 | 2072 | 362 | CFG_MMC3_DAT5_IN | - | - | vin2b_d0 |
| AB8 | mmc3_dat6 | 1675 | 808 | 2035 | 431 | CFG_MMC3_DAT6_IN | - | - | vin2b_de1 |
| AB5 | mmc3_dat7 | 0 | 0 | 0 | 0 | CFG_MMC3_DAT7_IN | - | - | vin2b_clk1 |
| B2 | vin2a_d16 | 1181 | 0 | 1424 | 0 | CFG_VIN2A_D16_IN | vin2b_d7 | - | - |
| D6 | vin2a_d17 | 1317 | 0 | 1545 | 0 | CFG_VIN2A_D17_IN | vin2b_d6 | - | - |
| C5 | vin2a_d18 | 1132 | 0 | 1240 | 0 | CFG_VIN2A_D18_IN | vin2b_d5 | - | - |
| A3 | vin2a_d19 | 749 | 0 | 919 | 0 | CFG_VIN2A_D19_IN | vin2b_d4 | - | - |
| B3 | vin2a_d20 | 1078 | 0 | 1320 | 0 | CFG_VIN2A_D20_IN | vin2b_d3 | - | - |
| B4 | vin2a_d21 | 1119 | 0 | 1357 | 0 | CFG_VIN2A_D21_IN | vin2b_d2 | - | - |
| B5 | vin2a_d22 | 1089 | 0 | 1306 | 0 | CFG_VIN2A_D22_IN | vin2b_d1 | - | - |
| A4 | vin2a_d23 | 1118 | 0 | 1362 | 0 | CFG_VIN2A_D23_IN | vin2b_d0 | - | - |
| G2 | vin2a_de0 | 1371 | 420 | 1813 | 86 | CFG_VIN2A_DE0_IN | vin2b_fld1 | vin2b_de1 | - |
| H7 | vin2a_fld0 | 0 | 0 | 0 | 0 | CFG_VIN2A_FLD0_IN | vin2b_clk1 | - | - |
| G1 | vin2a_hsync0 | 1605 | 0 | 1674 | 0 | CFG_VIN2A_HSYNC0_IN | - | vin2b_hsync1 | - |
| G6 | vin2a_vsync0 | 1231 | 0 | 1300 | 0 | CFG_VIN2A_VSYNC0_IN | - | vin2b_vsync1 | - |

(1) The CFG_MMC3_CLK_IN register should remain at its Default value, which is programmed automatically by hardware during the recalibration process.

Manual IO Timings Modes must be used to ensure some IO timings for VIP2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-9 *Manual Functions Mapping for VIP2* for a definition of the Manual modes.

Table 7-9 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-9. Manual Functions Mapping for VIP2**

| BALL | BALL NAME | VIP2_MANUAL 1 | | VIP2_MANUAL2 | | CFG REGISTER | MUXMODE | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 2 | 3 | 4 | 5 | 6 |
| R6 | gpmc_a0 | 2216 | 947 | 2519 | 702 | CFG_GPMC_A0_IN | vin3a_d16 | - | vin4a_d0 | - | - |
| T9 | gpmc_a1 | 2078 | 1022 | 2384 | 778 | CFG_GPMC_A1_IN | vin3a_d17 | - | vin4a_d1 | - | - |
| N9 | gpmc_a10 | 2108 | 823 | 2435 | 411 | CFG_GPMC_A10_IN | vin3a_de0 | - | - | - | - |
| P9 | gpmc_a11 | 2068 | 977 | 2379 | 755 | CFG_GPMC_A11_IN | vin3a_fld0 | - | vin4a_fld0 | - | - |


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**Table 7-9. Manual Functions Mapping for VIP2 (continued)**

| BALL | BALL NAME | VIP2_MANUAL 1 | | VIP2_MANUAL2 | | CFG REGISTER | MUXMODE | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 2 | 3 | 4 | 5 | 6 |
| K7 | gpmc_a19 | 1740 | 123 | 1743 | 0 | CFG_GPMC_A19_IN | - | - | vin4a_d12 | - | vin3b_d0 |
| T6 | gpmc_a2 | 2280 | 1298 | 2499 | 1127 | CFG_GPMC_A2_IN | vin3a_d18 | - | vin4a_d2 | - | - |
| M7 | gpmc_a20 | 1628 | 30 | 1529 | 0 | CFG_GPMC_A20_IN | - | - | vin4a_d13 | - | vin3b_d1 |
| J5 | gpmc_a21 | 1687 | 217 | 1779 | 0 | CFG_GPMC_A21_IN | - | - | vin4a_d14 | - | vin3b_d2 |
| K6 | gpmc_a22 | 1595 | 151 | 1620 | 0 | CFG_GPMC_A22_IN | - | - | vin4a_d15 | - | vin3b_d3 |
| J7 | gpmc_a23 | 1366 | 0 | 1363 | 0 | CFG_GPMC_A23_IN | - | - | vin4a_fld0 | - | vin3b_d4 |
| J4 | gpmc_a24 | 1554 | 343 | 1765 | 0 | CFG_GPMC_A24_IN | - | - | - | - | vin3b_d5 |
| J6 | gpmc_a25 | 1652 | 268 | 1808 | 0 | CFG_GPMC_A25_IN | - | - | - | - | vin3b_d6 |
| H4 | gpmc_a26 | 1546 | 281 | 1669 | 0 | CFG_GPMC_A26_IN | - | - | - | - | vin3b_d7 |
| H5 | gpmc_a27 | 1534 | 198 | 1611 | 0 | CFG_GPMC_A27_IN | - | - | - | - | vin3b_hsync1 |
| T7 | gpmc_a3 | 2246 | 1318 | 2455 | 1181 | CFG_GPMC_A3_IN | vin3a_d19 | - | vin4a_d3 | - | - |
| P6 | gpmc_a4 | 2266 | 1216 | 2486 | 1039 | CFG_GPMC_A4_IN | vin3a_d20 | - | vin4a_d4 | - | - |
| R9 | gpmc_a5 | 2185 | 1122 | 2456 | 938 | CFG_GPMC_A5_IN | vin3a_d21 | - | vin4a_d5 | - | - |
| R5 | gpmc_a6 | 2206 | 782 | 2463 | 573 | CFG_GPMC_A6_IN | vin3a_d22 | - | vin4a_d6 | - | - |
| P5 | gpmc_a7 | 2369 | 1025 | 2608 | 783 | CFG_GPMC_A7_IN | vin3a_d23 | - | vin4a_d7 | - | - |
| N7 | gpmc_a8 | 2154 | 978 | 2430 | 656 | CFG_GPMC_A8_IN | vin3a_hsync0 | - | - | - | - |
| R4 | gpmc_a9 | 2185 | 1152 | 2465 | 850 | CFG_GPMC_A9_IN | vin3a_vsync0 | - | - | - | - |
| M6 | gpmc_ad0 | 1908 | 620 | 2316 | 301 | CFG_GPMC_AD0_IN | vin3a_d0 | - | - | - | - |
| M2 | gpmc_ad1 | 2117 | 382 | 2440 | 70 | CFG_GPMC_AD1_IN | vin3a_d1 | - | - | - | - |
| J1 | gpmc_ad10 | 1968 | 686 | 2324 | 406 | CFG_GPMC_AD10_IN | vin3a_d10 | - | - | - | - |
| J2 | gpmc_ad11 | 1853 | 689 | 2278 | 352 | CFG_GPMC_AD11_IN | vin3a_d11 | - | - | - | - |
| H1 | gpmc_ad12 | 1910 | 497 | 2297 | 160 | CFG_GPMC_AD12_IN | vin3a_d12 | - | - | - | - |
| J3 | gpmc_ad13 | 1869 | 436 | 2278 | 108 | CFG_GPMC_AD13_IN | vin3a_d13 | - | - | - | - |
| H2 | gpmc_ad14 | 1895 | 147 | 2035 | 0 | CFG_GPMC_AD14_IN | vin3a_d14 | - | - | - | - |
| H3 | gpmc_ad15 | 1917 | 655 | 2279 | 378 | CFG_GPMC_AD15_IN | vin3a_d15 | - | - | - | - |
| L5 | gpmc_ad2 | 2097 | 666 | 2404 | 446 | CFG_GPMC_AD2_IN | vin3a_d2 | - | - | - | - |
| M1 | gpmc_ad3 | 1954 | 581 | 2343 | 212 | CFG_GPMC_AD3_IN | vin3a_d3 | - | - | - | - |
| L6 | gpmc_ad4 | 2034 | 610 | 2355 | 322 | CFG_GPMC_AD4_IN | vin3a_d4 | - | - | - | - |
| L4 | gpmc_ad5 | 1965 | 484 | 2337 | 192 | CFG_GPMC_AD5_IN | vin3a_d5 | - | - | - | - |
| L3 | gpmc_ad6 | 1861 | 635 | 2270 | 314 | CFG_GPMC_AD6_IN | vin3a_d6 | - | - | - | - |
| L2 | gpmc_ad7 | 2004 | 507 | 2339 | 259 | CFG_GPMC_AD7_IN | vin3a_d7 | - | - | - | - |
| L1 | gpmc_ad8 | 1945 | 853 | 2308 | 577 | CFG_GPMC_AD8_IN | vin3a_d8 | - | - | - | - |

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**Table 7-9. Manual Functions Mapping for VIP2 (continued)**

| BALL | BALL NAME | VIP2_MANUAL 1 | | VIP2_MANUAL2 | | CFG REGISTER | MUXMODE | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 2 | 3 | 4 | 5 | 6 |
| K2 | gpmc_ad9 | 1914 | 539 | 2334 | 166 | CFG_GPMC_AD9_IN | vin3a_d9 | - | - | - | - |
| N6 | gpmc_ben0 | 1806 | 0 | 1722 | 0 | CFG_GPMC_BEN0_IN | - | - | - | - | vin3b_de1 |
| M4 | gpmc_ben1 | 1879 | 20 | 1840 | 0 | CFG_GPMC_BEN1_IN | - | - | vin3b_clk1 | - | vin3b_fld1 |
| P7 | gpmc_clk | 0 | 0 | 0 | 0 | CFG_GPMC_CLK_IN | - | - | vin4a_hsync0 | vin4a_de0 | vin3b_clk1 |
| H6 | gpmc_cs1 | 1505 | 41 | 1388 | 0 | CFG_GPMC_CS1_IN | - | - | vin4a_de0 | - | vin3b_vsync1 |
| P1 | gpmc_cs3 | 0 | 0 | 0 | 0 | CFG_GPMC_CS3_IN | vin3a_clk0 | - | - | - | - |
| AF1 | vin1a_d16 | 1803 | 1679 | 2244 | 1202 | CFG_VIN1A_D16_IN | - | - | - | - | vin3a_d0 |
| AE3 | vin1a_d17 | 1871 | 1654 | 2321 | 1116 | CFG_VIN1A_D17_IN | - | - | - | - | vin3a_d1 |
| AE5 | vin1a_d18 | 1875 | 1742 | 2280 | 1288 | CFG_VIN1A_D18_IN | - | - | - | - | vin3a_d2 |
| AE1 | vin1a_d19 | 1844 | 1759 | 2282 | 1281 | CFG_VIN1A_D19_IN | - | - | - | - | vin3a_d3 |
| AE2 | vin1a_d20 | 1845 | 1624 | 2284 | 1090 | CFG_VIN1A_D20_IN | - | - | - | - | vin3a_d4 |
| AE6 | vin1a_d21 | 1906 | 1520 | 2324 | 1000 | CFG_VIN1A_D21_IN | - | - | - | - | vin3a_d5 |
| AD2 | vin1a_d22 | 1807 | 1437 | 2278 | 915 | CFG_VIN1A_D22_IN | - | - | - | - | vin3a_d6 |
| AD3 | vin1a_d23 | 1996 | 997 | 2423 | 398 | CFG_VIN1A_D23_IN | - | - | - | - | vin3a_d7 |
| AH7 | vin1b_clk1 | 0 | 0 | 0 | 0 | CFG_VIN1B_CLK1_IN | - | - | - | - | vin3a_clk0 |
| B2 | vin2a_d16 | 1329 | 528 | 1779 | 0 | CFG_VIN2A_D16_IN | - | - | - | - | vin3a_d8 |
| D6 | vin2a_d17 | 1270 | 677 | 1844 | 0 | CFG_VIN2A_D17_IN | - | - | - | - | vin3a_d9 |
| C5 | vin2a_d18 | 1494 | 411 | 1767 | 0 | CFG_VIN2A_D18_IN | - | - | - | - | vin3a_d10 |
| A3 | vin2a_d19 | 1225 | 154 | 1254 | 0 | CFG_VIN2A_D19_IN | - | - | - | - | vin3a_d11 |
| B3 | vin2a_d20 | 1212 | 450 | 1597 | 0 | CFG_VIN2A_D20_IN | - | - | - | vin3a_de0 | vin3a_d12 |
| B4 | vin2a_d21 | 1232 | 494 | 1662 | 0 | CFG_VIN2A_D21_IN | - | - | - | vin3a_fld0 | vin3a_d13 |
| B5 | vin2a_d22 | 1203 | 503 | 1641 | 0 | CFG_VIN2A_D22_IN | - | - | - | vin3a_hsync0 | vin3a_d14 |
| A4 | vin2a_d23 | 1214 | 599 | 1748 | 0 | CFG_VIN2A_D23_IN | - | - | - | vin3a_vsync0 | vin3a_d15 |
| D11 | vout1_clk | 2047 | 735 | 2391 | 637 | CFG_VOUT1_CLK_IN | - | vin4a_fld0 | vin3a_fld0 | - | - |
| F11 | vout1_d0 | 2135 | 987 | 2403 | 965 | CFG_VOUT1_D0_IN | - | vin4a_d16 | vin3a_d16 | - | - |
| G10 | vout1_d1 | 2048 | 955 | 2368 | 880 | CFG_VOUT1_D1_IN | - | vin4a_d17 | vin3a_d17 | - | - |
| D7 | vout1_d10 | 1970 | 855 | 2347 | 724 | CFG_VOUT1_D10_IN | - | vin4a_d10 | vin3a_d10 | - | - |
| D8 | vout1_d11 | 2111 | 893 | 2389 | 861 | CFG_VOUT1_D11_IN | - | vin4a_d11 | vin3a_d11 | - | - |
| A5 | vout1_d12 | 2018 | 841 | 2356 | 748 | CFG_VOUT1_D12_IN | - | vin4a_d12 | vin3a_d12 | - | - |
| C6 | vout1_d13 | 2073 | 805 | 2382 | 731 | CFG_VOUT1_D13_IN | - | vin4a_d13 | vin3a_d13 | - | - |
| C8 | vout1_d14 | 2112 | 770 | 2401 | 703 | CFG_VOUT1_D14_IN | - | vin4a_d14 | vin3a_d14 | - | - |
| C7 | vout1_d15 | 2132 | 831 | 2434 | 771 | CFG_VOUT1_D15_IN | - | vin4a_d15 | vin3a_d15 | - | - |


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**Table 7-9. Manual Functions Mapping for VIP2 (continued)**

| BALL | BALL NAME | VIP2_MANUAL 1 | | VIP2_MANUAL2 | | CFG REGISTER | MUXMODE | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 2 | 3 | 4 | 5 | 6 |
| B7 | vout1_d16 | 1996 | 632 | 2338 | 536 | CFG_VOUT1_D16_IN | - | vin4a_d0 | vin3a_d0 | - | - |
| B8 | vout1_d17 | 2190 | 790 | 2442 | 775 | CFG_VOUT1_D17_IN | - | vin4a_d1 | vin3a_d1 | - | - |
| A7 | vout1_d18 | 2100 | 604 | 2385 | 565 | CFG_VOUT1_D18_IN | - | vin4a_d2 | vin3a_d2 | - | - |
| A8 | vout1_d19 | 2108 | 286 | 2424 | 168 | CFG_VOUT1_D19_IN | - | vin4a_d3 | vin3a_d3 | - | - |
| F10 | vout1_d2 | 1979 | 1020 | 2335 | 909 | CFG_VOUT1_D2_IN | - | vin4a_d18 | vin3a_d18 | - | - |
| C9 | vout1_d20 | 2031 | 967 | 2362 | 881 | CFG_VOUT1_D20_IN | - | vin4a_d4 | vin3a_d4 | - | - |
| A9 | vout1_d21 | 2039 | 450 | 2350 | 384 | CFG_VOUT1_D21_IN | - | vin4a_d5 | vin3a_d5 | - | - |
| B9 | vout1_d22 | 2037 | 583 | 2369 | 497 | CFG_VOUT1_D22_IN | - | vin4a_d6 | vin3a_d6 | - | - |
| A10 | vout1_d23 | 1768 | 740 | 2246 | 508 | CFG_VOUT1_D23_IN | - | vin4a_d7 | vin3a_d7 | - | - |
| G11 | vout1_d3 | 2099 | 881 | 2382 | 844 | CFG_VOUT1_D3_IN | - | vin4a_d19 | vin3a_d19 | - | - |
| E9 | vout1_d4 | 2120 | 786 | 2387 | 756 | CFG_VOUT1_D4_IN | - | vin4a_d20 | vin3a_d20 | - | - |
| F9 | vout1_d5 | 1965 | 857 | 2299 | 769 | CFG_VOUT1_D5_IN | - | vin4a_d21 | vin3a_d21 | - | - |
| F8 | vout1_d6 | 2139 | 680 | 2366 | 699 | CFG_VOUT1_D6_IN | - | vin4a_d22 | vin3a_d22 | - | - |
| E7 | vout1_d7 | 2122 | 912 | 2360 | 920 | CFG_VOUT1_D7_IN | - | vin4a_d23 | vin3a_d23 | - | - |
| E8 | vout1_d8 | 2073 | 906 | 2372 | 853 | CFG_VOUT1_D8_IN | - | vin4a_d8 | vin3a_d8 | - | - |
| D9 | vout1_d9 | 2097 | 934 | 2386 | 879 | CFG_VOUT1_D9_IN | - | vin4a_d9 | vin3a_d9 | - | - |
| B10 | vout1_de | 2021 | 527 | 2366 | 428 | CFG_VOUT1_DE_IN | - | vin4a_de0 | vin3a_de0 | - | - |
| B11 | vout1_fld | 0 | 0 | 0 | 0 | CFG_VOUT1_FLD_IN | - | vin4a_clk0 | vin3a_clk0 | - | - |
| C11 | vout1_hsync | 1775 | 486 | 2272 | 164 | CFG_VOUT1_HSYNC_IN | - | vin4a_hsync0 | vin3a_hsync0 | - | - |
| E11 | vout1_vsync | 1917 | 314 | 2301 | 0 | CFG_VOUT1_VSYNC_IN | - | vin4a_vsync0 | vin3a_vsync0 | - | - |

Manual IO Timings Modes must be used to ensure some IO timings for VIP2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-10 *Manual Functions Mapping for VIP2 4A* for a definition of the Manual modes.

Table 7-10 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-10. Manual Functions Mapping for VIP2 4A**

| BALL | BALL NAME | VIP2_4A_MANUAL1 | | VIP2_4A_MANUAL2 | | CFG REGISTER | MUXMODE | | |
|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 3 | 4 | 5 |
| R6 | gpmc_a0 | 1801 | 521 | 2268 | 0 | CFG_GPMC_A0_IN | - | vin4a_d0 | - |
| T9 | gpmc_a1 | 1668 | 488 | 2135 | 0 | CFG_GPMC_A1_IN | - | vin4a_d1 | - |

### Table 7-10. Manual Functions Mapping for VIP2 4A (continued)

| BALL | BALL NAME | VIP2_4A_MANUAL1 | | VIP2_4A_MANUAL2 | | CFG REGISTER | MUXMODE | | |
|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 3 | 4 | 5 |
| P9 | gpmc_a11 | 1694 | 308 | 2026 | 0 | CFG_GPMC_A11_IN | - | vin4a_fld0 | - |
| P4 | gpmc_a12 | 0 | 0 | 0 | 0 | CFG_GPMC_A12_IN | - | vin4a_clk0 | - |
| R3 | gpmc_a13 | 1529 | 570 | 2029 | 38 | CFG_GPMC_A13_IN | - | vin4a_hsync0 | - |
| T2 | gpmc_a14 | 1747 | 753 | 2266 | 261 | CFG_GPMC_A14_IN | - | vin4a_vsync0 | - |
| U2 | gpmc_a15 | 1536 | 336 | 1882 | 0 | CFG_GPMC_A15_IN | - | vin4a_d8 | - |
| U1 | gpmc_a16 | 1662 | 293 | 1936 | 0 | CFG_GPMC_A16_IN | - | vin4a_d9 | - |
| P3 | gpmc_a17 | 1637 | 247 | 1851 | 0 | CFG_GPMC_A17_IN | - | vin4a_d10 | - |
| R2 | gpmc_a18 | 1454 | 0 | 1369 | 0 | CFG_GPMC_A18_IN | - | vin4a_d11 | - |
| K7 | gpmc_a19 | 1577 | 205 | 1634 | 0 | CFG_GPMC_A19_IN | - | vin4a_d12 | - |
| T6 | gpmc_a2 | 1891 | 747 | 2369 | 238 | CFG_GPMC_A2_IN | - | vin4a_d2 | - |
| M7 | gpmc_a20 | 1398 | 220 | 1450 | 0 | CFG_GPMC_A20_IN | - | vin4a_d13 | - |
| J5 | gpmc_a21 | 1521 | 329 | 1691 | 0 | CFG_GPMC_A21_IN | - | vin4a_d14 | - |
| K6 | gpmc_a22 | 1383 | 273 | 1488 | 0 | CFG_GPMC_A22_IN | - | vin4a_d15 | - |
| J7 | gpmc_a23 | 1163 | 0 | 1147 | 0 | CFG_GPMC_A23_IN | - | vin4a_fld0 | - |
| T7 | gpmc_a3 | 1820 | 786 | 2325 | 271 | CFG_GPMC_A3_IN | - | vin4a_d3 | - |
| P6 | gpmc_a4 | 1865 | 662 | 2359 | 126 | CFG_GPMC_A4_IN | - | vin4a_d4 | - |
| R9 | gpmc_a5 | 1722 | 629 | 2260 | 53 | CFG_GPMC_A5_IN | - | vin4a_d5 | - |
| R5 | gpmc_a6 | 1755 | 279 | 1990 | 0 | CFG_GPMC_A6_IN | - | vin4a_d6 | - |
| P5 | gpmc_a7 | 1979 | 506 | 2410 | 0 | CFG_GPMC_A7_IN | - | vin4a_d7 | - |
| N1 | gpmc_advn_ale | 1793 | 267 | 2045 | 0 | CFG_GPMC_ADVN_ALE_IN | - | vin4a_vsync0 | - |
| P7 | gpmc_clk | 1738 | 309 | 2040 | 0 | CFG_GPMC_CLK_IN | - | vin4a_hsync0 | vin4a_de0 |
| H6 | gpmc_cs1 | 1379 | 95 | 1361 | 0 | CFG_GPMC_CS1_IN | - | vin4a_de0 | - |
| D11 | vout1_clk | 2090 | 401 | 2409 | 357 | CFG_VOUT1_CLK_IN | vin4a_fld0 | - | - |
| F11 | vout1_d0 | 2139 | 961 | 2394 | 981 | CFG_VOUT1_D0_IN | vin4a_d16 | - | - |
| G10 | vout1_d1 | 1993 | 878 | 2347 | 799 | CFG_VOUT1_D1_IN | vin4a_d17 | - | - |
| D7 | vout1_d10 | 1976 | 678 | 2346 | 583 | CFG_VOUT1_D10_IN | vin4a_d10 | - | - |
| D8 | vout1_d11 | 2135 | 749 | 2393 | 767 | CFG_VOUT1_D11_IN | vin4a_d11 | - | - |
| A5 | vout1_d12 | 2014 | 696 | 2351 | 634 | CFG_VOUT1_D12_IN | vin4a_d12 | - | - |
| C6 | vout1_d13 | 2035 | 590 | 2370 | 531 | CFG_VOUT1_D13_IN | vin4a_d13 | - | - |
| C8 | vout1_d14 | 2108 | 861 | 2385 | 860 | CFG_VOUT1_D14_IN | vin4a_d14 | - | - |
| C7 | vout1_d15 | 2074 | 682 | 2423 | 609 | CFG_VOUT1_D15_IN | vin4a_d15 | - | - |
| B7 | vout1_d16 | 1976 | 579 | 2331 | 500 | CFG_VOUT1_D16_IN | vin4a_d0 | - | - |


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**Table 7-10. Manual Functions Mapping for VIP2 4A (continued)**

| BALL | BALL NAME | VIP2_4A_MANUAL1 | | VIP2_4A_MANUAL2 | | CFG REGISTER | MUXMODE | | |
|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 3 | 4 | 5 |
| B8 | vout1_d17 | 2203 | 505 | 2464 | 509 | CFG_VOUT1_D17_IN | vin4a_d1 | - | - |
| A7 | vout1_d18 | 2096 | 412 | 2394 | 390 | CFG_VOUT1_D18_IN | vin4a_d2 | - | - |
| A8 | vout1_d19 | 2106 | 72 | 2423 | 21 | CFG_VOUT1_D19_IN | vin4a_d3 | - | - |
| F10 | vout1_d2 | 2023 | 648 | 2374 | 572 | CFG_VOUT1_D2_IN | vin4a_d18 | - | - |
| C9 | vout1_d20 | 2027 | 767 | 2370 | 700 | CFG_VOUT1_D20_IN | vin4a_d4 | - | - |
| A9 | vout1_d21 | 2026 | 184 | 2354 | 128 | CFG_VOUT1_D21_IN | vin4a_d5 | - | - |
| B9 | vout1_d22 | 2061 | 195 | 2397 | 135 | CFG_VOUT1_D22_IN | vin4a_d6 | - | - |
| A10 | vout1_d23 | 1764 | 607 | 2251 | 396 | CFG_VOUT1_D23_IN | vin4a_d7 | - | - |
| G11 | vout1_d3 | 2053 | 757 | 2377 | 707 | CFG_VOUT1_D3_IN | vin4a_d19 | - | - |
| E9 | vout1_d4 | 2119 | 617 | 2392 | 619 | CFG_VOUT1_D4_IN | vin4a_d20 | - | - |
| F9 | vout1_d5 | 1951 | 712 | 2305 | 633 | CFG_VOUT1_D5_IN | vin4a_d21 | - | - |
| F8 | vout1_d6 | 2119 | 515 | 2365 | 543 | CFG_VOUT1_D6_IN | vin4a_d22 | - | - |
| E7 | vout1_d7 | 2119 | 779 | 2363 | 810 | CFG_VOUT1_D7_IN | vin4a_d23 | - | - |
| E8 | vout1_d8 | 2043 | 807 | 2357 | 768 | CFG_VOUT1_D8_IN | vin4a_d8 | - | - |
| D9 | vout1_d9 | 2166 | 643 | 2412 | 671 | CFG_VOUT1_D9_IN | vin4a_d9 | - | - |
| B10 | vout1_de | 1982 | 410 | 2353 | 314 | CFG_VOUT1_DE_IN | vin4a_de0 | - | - |
| B11 | vout1_fld | 0 | 0 | 0 | 0 | CFG_VOUT1_FLD_IN | vin4a_clk0 | - | - |
| C11 | vout1_hsync | 1755 | 305 | 2269 | 4 | CFG_VOUT1_HSYNC_IN | vin4a_hsync0 | - | - |
| E11 | vout1_vsync | 1924 | 8 | 2066 | 0 | CFG_VOUT1_VSYNC_IN | vin4a_vsync0 | - | - |

Manual IO Timings Modes must be used to ensure some IO timings for VIP2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-11 *Manual Functions Mapping for VIP2 4A IOSET3* for a definition of the Manual modes.

Table 7-11 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-11. Manual Functions Mapping for VIP2 4A IOSET3**

| BALL | BALL NAME | VIP2_4A_IOSET3_MANUAL1 | | VIP2_4A_IOSET3_MANUAL2 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 8 |
| E21 | gpio6_14 | 683 | 0 | 939 | 0 | CFG_GPIO6_14_IN | vin4a_hsync0 |
| F20 | gpio6_15 | 1065 | 0 | 1321 | 0 | CFG_GPIO6_15_IN | vin4a_vsync0 |
| F21 | gpio6_16 | 858 | 0 | 1114 | 0 | CFG_GPIO6_16_IN | vin4a_fld0 |
| B14 | mcasp1_aclkr | 1711 | 23 | 1990 | 0 | CFG_MCASP1_ACLKR_IN | vin4a_d0 |
| G13 | mcasp1_axr2 | 2131 | 1054 | 2423 | 1073 | CFG_MCASP1_AXR2_IN | vin4a_d2 |

**Table 7-11. Manual Functions Mapping for VIP2 4A IOSET3 (continued)**

| BALL | BALL NAME | VIP2_4A_IOSET3_MANUAL1 | | VIP2_4A_IOSET3_MANUAL2 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 8 |
| J11 | mcasp1_axr3 | 2267 | 691 | 2573 | 696 | CFG_MCASP1_AXR3_IN | vin4a_d3 |
| E12 | mcasp1_axr4 | 2089 | 813 | 2441 | 773 | CFG_MCASP1_AXR4_IN | vin4a_d4 |
| F13 | mcasp1_axr5 | 2061 | 858 | 2430 | 799 | CFG_MCASP1_AXR5_IN | vin4a_d5 |
| C12 | mcasp1_axr6 | 2151 | 595 | 2539 | 480 | CFG_MCASP1_AXR6_IN | vin4a_d6 |
| D12 | mcasp1_axr7 | 2112 | 931 | 2421 | 932 | CFG_MCASP1_AXR7_IN | vin4a_d7 |
| J14 | mcasp1_fsr | 1714 | 323 | 2248 | 44 | CFG_MCASP1_FSR_IN | vin4a_d1 |
| E15 | mcasp2_aclkr | 1462 | 76 | 1795 | 0 | CFG_MCASP2_ACLKR_IN | vin4a_d8 |
| B15 | mcasp2_axr0 | 1578 | 833 | 2113 | 554 | CFG_MCASP2_AXR0_IN | vin4a_d10 |
| A15 | mcasp2_axr1 | 1785 | 396 | 2279 | 212 | CFG_MCASP2_AXR1_IN | vin4a_d11 |
| D15 | mcasp2_axr4 | 1765 | 485 | 2299 | 206 | CFG_MCASP2_AXR4_IN | vin4a_d12 |
| B16 | mcasp2_axr5 | 1644 | 509 | 2179 | 230 | CFG_MCASP2_AXR5_IN | vin4a_d13 |
| B17 | mcasp2_axr6 | 1098 | 0 | 1354 | 0 | CFG_MCASP2_AXR6_IN | vin4a_d14 |
| A17 | mcasp2_axr7 | 1242 | 521 | 1777 | 243 | CFG_MCASP2_AXR7_IN | vin4a_d15 |
| A20 | mcasp2_fsr | 1328 | 130 | 1713 | 0 | CFG_MCASP2_FSR_IN | vin4a_d9 |
| C18 | mcasp4_aclkx | 1033 | 0 | 1166 | 0 | CFG_MCASP4_ACLKX_IN | vin4a_d16 |
| G16 | mcasp4_axr0 | 2147 | 358 | 2529 | 221 | CFG_MCASP4_AXR0_IN | vin4a_d18 |
| D17 | mcasp4_axr1 | 2140 | 676 | 2482 | 645 | CFG_MCASP4_AXR1_IN | vin4a_d19 |
| A21 | mcasp4_fsx | 2140 | 339 | 2554 | 165 | CFG_MCASP4_FSX_IN | vin4a_d17 |
| AA3 | mcasp5_aclkx | 2846 | 2620 | 3059 | 2547 | CFG_MCASP5_ACLKX_IN | vin4a_d20 |
| AB3 | mcasp5_axr0 | 2880 | 3301 | 3040 | 3417 | CFG_MCASP5_AXR0_IN | vin4a_d22 |
| AA4 | mcasp5_axr1 | 2851 | 3586 | 3042 | 3593 | CFG_MCASP5_AXR1_IN | vin4a_d23 |
| AB9 | mcasp5_fsx | 2847 | 2856 | 3031 | 2890 | CFG_MCASP5_FSX_IN | vin4a_d21 |
| B26 | xref_clk2 | 0 | 0 | 0 | 0 | CFG_XREF_CLK2_IN | vin4a_clk0 |
| C23 | xref_clk3 | 927 | 0 | 1183 | 0 | CFG_XREF_CLK3_IN | vin4a_de0 |

Manual IO Timings Modes must be used to ensure some IO timings for VIP2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-12 *Manual Functions Mapping for VIP2 4B* for a definition of the Manual modes.

Table 7-12 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.


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**Table 7-12. Manual Functions Mapping for VIP2 4B**

| BALL | BALL NAME | VIP2_4B_MANUAL1 | | VIP2_4B_MANUAL2 | | CFG REGISTER | MUXMODE | |
|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 5 | 6 |
| R6 | gpmc_a0 | 1861 | 901 | 2102 | 660 | CFG_GPMC_A0_IN | - | vin4b_d0 |
| T9 | gpmc_a1 | 1652 | 891 | 1955 | 583 | CFG_GPMC_A1_IN | - | vin4b_d1 |
| N9 | gpmc_a10 | 0 | 0 | 0 | 0 | CFG_GPMC_A10_IN | - | vin4b_clk1 |
| P9 | gpmc_a11 | 1783 | 1178 | 1975 | 1021 | CFG_GPMC_A11_IN | - | vin4b_de1 |
| P4 | gpmc_a12 | 1903 | 853 | 2076 | 664 | CFG_GPMC_A12_IN | - | vin4b_fld1 |
| T6 | gpmc_a2 | 1888 | 1212 | 2065 | 994 | CFG_GPMC_A2_IN | - | vin4b_d2 |
| T7 | gpmc_a3 | 1839 | 1274 | 2025 | 1075 | CFG_GPMC_A3_IN | - | vin4b_d3 |
| P6 | gpmc_a4 | 1868 | 1113 | 2058 | 869 | CFG_GPMC_A4_IN | - | vin4b_d4 |
| R9 | gpmc_a5 | 1757 | 1079 | 2028 | 802 | CFG_GPMC_A5_IN | - | vin4b_d5 |
| R5 | gpmc_a6 | 1800 | 670 | 2032 | 421 | CFG_GPMC_A6_IN | - | vin4b_d6 |
| P5 | gpmc_a7 | 1967 | 898 | 2179 | 597 | CFG_GPMC_A7_IN | - | vin4b_d7 |
| N7 | gpmc_a8 | 1731 | 959 | 1993 | 559 | CFG_GPMC_A8_IN | - | vin4b_hsync1 |
| R4 | gpmc_a9 | 1766 | 1150 | 2022 | 834 | CFG_GPMC_A9_IN | - | vin4b_vsync1 |
| U4 | mdio_d | 1602 | 506 | 1931 | 283 | CFG_MDIO_D_IN | vin4b_d0 | - |
| V1 | mdio_mclk | 0 | 0 | 0 | 0 | CFG_MDIO_MCLK_IN | vin4b_clk1 | - |
| U5 | rgmii0_rxc | 1678 | 887 | 1987 | 663 | CFG_RGMII0_RXC_IN | vin4b_d5 | - |
| V5 | rgmii0_rxctl | 1595 | 932 | 1903 | 748 | CFG_RGMII0_RXCTL_IN | vin4b_d6 | - |
| W2 | rgmii0_rxd0 | 1707 | 464 | 2010 | 160 | CFG_RGMII0_RXD0_IN | vin4b_fld1 | - |
| V4 | rgmii0_rxd3 | 1662 | 1146 | 1943 | 996 | CFG_RGMII0_RXD3_IN | vin4b_d7 | - |
| W9 | rgmii0_txc | 1639 | 1195 | 1970 | 1006 | CFG_RGMII0_TXC_IN | vin4b_d3 | - |
| V9 | rgmii0_txctl | 1695 | 1226 | 1952 | 1113 | CFG_RGMII0_TXCTL_IN | vin4b_d4 | - |
| V6 | rgmii0_txd1 | 1693 | 1118 | 1951 | 1003 | CFG_RGMII0_TXD1_IN | vin4b_vsync1 | - |
| U7 | rgmii0_txd2 | 1522 | 1004 | 1895 | 685 | CFG_RGMII0_TXD2_IN | vin4b_hsync1 | - |
| V7 | rgmii0_txd3 | 1777 | 957 | 2018 | 787 | CFG_RGMII0_TXD3_IN | vin4b_de1 | - |
| V2 | uart3_rxd | 1537 | 236 | 1762 | 0 | CFG_UART3_RXD_IN | vin4b_d1 | - |
| Y1 | uart3_txd | 1575 | 645 | 1933 | 276 | CFG_UART3_TXD_IN | vin4b_d2 | - |

Manual IO Timings Modes must be used to ensure some IO timings for VIP2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-13 *Manual Functions Mapping for VIP2 3B IOSET2* for a definition of the Manual modes.

Table 7-13 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

### Table 7-13. Manual Functions Mapping for VIP2 3B IOSET2

| BALL | BALL NAME | VIP2_3B_IOSET2_MANUAL1 | | VIP2_3B_IOSET2_MANUAL2 | | CFG REGISTER | MUXMODE | |
|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 4 | 6 |
| K7 | gpmc_a19 | 1505 | 1172 | 1854 | 799 | CFG_GPMC_A19_IN | vin4a_d12 | vin3b_d0 |
| M7 | gpmc_a20 | 1394 | 1074 | 1723 | 716 | CFG_GPMC_A20_IN | vin4a_d13 | vin3b_d1 |
| J5 | gpmc_a21 | 1452 | 1266 | 1789 | 900 | CFG_GPMC_A21_IN | vin4a_d14 | vin3b_d2 |
| K6 | gpmc_a22 | 1360 | 1200 | 1684 | 847 | CFG_GPMC_A22_IN | vin4a_d15 | vin3b_d3 |
| J7 | gpmc_a23 | 1446 | 735 | 1831 | 443 | CFG_GPMC_A23_IN | vin4a_fld0 | vin3b_d4 |
| J4 | gpmc_a24 | 1329 | 1360 | 1686 | 970 | CFG_GPMC_A24_IN | - | vin3b_d5 |
| J6 | gpmc_a25 | 1417 | 1318 | 1757 | 962 | CFG_GPMC_A25_IN | - | vin3b_d6 |
| H4 | gpmc_a26 | 1321 | 1298 | 1680 | 880 | CFG_GPMC_A26_IN | - | vin3b_d7 |
| H5 | gpmc_a27 | 1309 | 1215 | 1669 | 834 | CFG_GPMC_A27_IN | - | vin3b_hsync1 |
| N6 | gpmc_ben0 | 1677 | 944 | 1994 | 638 | CFG_GPMC_BEN0_IN | - | vin3b_de1 |
| M4 | gpmc_ben1 | 0 | 0 | 0 | 0 | CFG_GPMC_BEN1_IN | vin3b_clk1 | vin3b_fld1 |
| H6 | gpmc_cs1 | 1280 | 1058 | 1620 | 664 | CFG_GPMC_CS1_IN | vin4a_de0 | vin3b_vsync1 |


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Manual IO Timings Modes must be used to ensure some IO timings for VIP3. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-14 *Manual Functions Mapping for VIP3* for a definition of the Manual modes.

Table 7-14 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-14. Manual Functions Mapping for VIP3**

| BALL | BALL NAME | VIP3_MANUAL1 | | VIP3_MANUAL2 | | CFG REGISTER | MUXMODE | |
|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 7 | 9 |
| AC5 | gpio6_10 | 774 | 2462 | 765 | 2551 | CFG_GPIO6_10_IN | - | vin5a_clk0 |
| AB4 | gpio6_11 | 2453 | 3000 | 2863 | 2719 | CFG_GPIO6_11_IN | - | vin5a_de0 |
| C14 | mcasp1_aclkx | 1400 | 154 | 1698 | 0 | CFG_MCASP1_ACLKX_IN | vin6a_fld0 | - |
| G12 | mcasp1_axr0 | 2055 | 612 | 2459 | 381 | CFG_MCASP1_AXR0_IN | vin6a_vsync0 | - |
| F12 | mcasp1_axr1 | 1623 | 338 | 2098 | 0 | CFG_MCASP1_AXR1_IN | vin6a_hsync0 | - |
| B13 | mcasp1_axr10 | 1625 | 92 | 1681 | 0 | CFG_MCASP1_AXR10_IN | vin6a_d13 | - |
| A12 | mcasp1_axr11 | 1509 | 714 | 2048 | 317 | CFG_MCASP1_AXR11_IN | vin6a_d12 | - |
| E14 | mcasp1_axr12 | 1189 | 619 | 1729 | 222 | CFG_MCASP1_AXR12_IN | vin6a_d11 | - |
| A13 | mcasp1_axr13 | 1546 | 265 | 1954 | 0 | CFG_MCASP1_AXR13_IN | vin6a_d10 | - |
| G14 | mcasp1_axr14 | 1305 | 0 | 1448 | 0 | CFG_MCASP1_AXR14_IN | vin6a_d9 | - |
| F14 | mcasp1_axr15 | 1342 | 313 | 1798 | 0 | CFG_MCASP1_AXR15_IN | vin6a_d8 | - |
| B12 | mcasp1_axr8 | 1833 | 466 | 2264 | 0 | CFG_MCASP1_AXR8_IN | vin6a_d15 | - |
| A11 | mcasp1_axr9 | 1555 | 777 | 2029 | 352 | CFG_MCASP1_AXR9_IN | vin6a_d14 | - |
| D14 | mcasp1_fsx | 1549 | 281 | 1972 | 0 | CFG_MCASP1_FSX_IN | vin6a_de0 | - |
| A19 | mcasp2_aclkx | 1063 | 0 | 1206 | 0 | CFG_MCASP2_ACLKX_IN | vin6a_d7 | - |
| C15 | mcasp2_axr2 | 1134 | 0 | 1277 | 0 | CFG_MCASP2_AXR2_IN | vin6a_d5 | - |
| A16 | mcasp2_axr3 | 1348 | 487 | 1888 | 90 | CFG_MCASP2_AXR3_IN | vin6a_d4 | - |
| A18 | mcasp2_fsx | 1030 | 250 | 1424 | 0 | CFG_MCASP2_FSX_IN | vin6a_d6 | - |
| B18 | mcasp3_aclkx | 0 | 0 | 0 | 0 | CFG_MCASP3_ACLKX_IN | vin6a_d3 | - |
| B19 | mcasp3_axr0 | 888 | 485 | 1428 | 88 | CFG_MCASP3_AXR0_IN | vin6a_d1 | - |
| C17 | mcasp3_axr1 | 861 | 582 | 1331 | 254 | CFG_MCASP3_AXR1_IN | vin6a_d0 | vin5a_fld0 |
| F15 | mcasp3_fsx | 1093 | 451 | 1633 | 54 | CFG_MCASP3_FSX_IN | vin6a_d2 | - |
| C18 | mcasp4_aclkx | 557 | 0 | 541 | 0 | CFG_MCASP4_ACLKX_IN | - | vin5a_d15 |
| G16 | mcasp4_axr0 | 1027 | 989 | 1441 | 644 | CFG_MCASP4_AXR0_IN | - | vin5a_d13 |
| D17 | mcasp4_axr1 | 1140 | 1038 | 1601 | 740 | CFG_MCASP4_AXR1_IN | - | vin5a_d12 |
| A21 | mcasp4_fsx | 1140 | 885 | 700 | 1377 | CFG_MCASP4_FSX_IN | - | vin5a_d14 |
| AA3 | mcasp5_aclkx | 1633 | 3030 | 1658 | 2999 | CFG_MCASP5_ACLKX_IN | - | vin5a_d11 |
| AB3 | mcasp5_axr0 | 2392 | 3028 | 2816 | 2711 | CFG_MCASP5_AXR0_IN | - | vin5a_d9 |
| AA4 | mcasp5_axr1 | 2435 | 3026 | 2856 | 2723 | CFG_MCASP5_AXR1_IN | - | vin5a_d8 |
| AB9 | mcasp5_fsx | 2285 | 2660 | 2713 | 2288 | CFG_MCASP5_FSX_IN | - | vin5a_d10 |
| AD4 | mmc3_clk | 2501 | 2822 | 2915 | 2475 | CFG_MMC3_CLK_IN | - | vin5a_d7 |
| AC4 | mmc3_cmd | 2423 | 2826 | 2832 | 2485 | CFG_MMC3_CMD_IN | - | vin5a_d6 |
| AC7 | mmc3_dat0 | 2336 | 2820 | 2743 | 2526 | CFG_MMC3_DAT0_IN | - | vin5a_d5 |
| AC6 | mmc3_dat1 | 2332 | 2710 | 2749 | 2346 | CFG_MMC3_DAT1_IN | - | vin5a_d4 |
| AC9 | mmc3_dat2 | 1732 | 3048 | 1811 | 3012 | CFG_MMC3_DAT2_IN | - | vin5a_d3 |
| AC3 | mmc3_dat3 | 2459 | 2969 | 2872 | 2683 | CFG_MMC3_DAT3_IN | - | vin5a_d2 |
| AC8 | mmc3_dat4 | 2436 | 2662 | 2836 | 2271 | CFG_MMC3_DAT4_IN | - | vin5a_d1 |
| AD6 | mmc3_dat5 | 2450 | 2431 | 1771 | 3271 | CFG_MMC3_DAT5_IN | - | vin5a_d0 |
| AB8 | mmc3_dat6 | 2332 | 2640 | 2752 | 2255 | CFG_MMC3_DAT6_IN | - | vin5a_hsync0 |
| AB5 | mmc3_dat7 | 1799 | 2927 | 1881 | 2844 | CFG_MMC3_DAT7_IN | - | vin5a_vsync0 |

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**Table 7-14. Manual Functions Mapping for VIP3 (continued)**

| BALL | BALL NAME | VIP3_MANUAL1 | | VIP3_MANUAL2 | | CFG REGISTER | MUXMODE | |
|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 7 | 9 |
| D18 | xref_clk0 | 681 | 0 | 824 | 0 | CFG_XREF_CLK0_IN | vin6a_d0 | - |
| E17 | xref_clk1 | 21 | 0 | 0 | 0 | CFG_XREF_CLK1_IN | vin6a_clk0 | - |

## 7.7 Display Subsystem – Video Output Ports

Three Display Parallel Interfaces (DPI) channels are available in DSS named DPI Video Output 1, DPI Video Output 2 and DPI Video Output 3.

**NOTE**

The DPI Video Output i (i = 1 to 3) interface is also referred to as VOUTi.

Every VOUT interface consists of:

- 24-bit data bus (data[23:0])
- Horizontal synchronization signal (HSYNC)
- Vertical synchronization signal (VSYNC)
- Data enable (DE)
- Field ID (FID)
- Pixel clock (CLK)

**NOTE**

For more information, see the Display Subsystem chapter of the Device TRM.

**CAUTION**

The IO timings provided in this section are only valid if signals within a single IOSET are used. The IOSETs are defined in the Table 7-19 and Table 7-20.

**CAUTION**

The IO Timings provided in this section are only valid for some DSS usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

**CAUTION**

All pads/balls configured as vouti_* signals are recommended to use slow slew rate by setting the corresponding CTRL_CORE_PAD_*[SLEWCONTROL] register field to SLOW (0b1). FAST slew setting is allowed, but results in faster edge rates on the VOUTn bus, higher power/ground noise, and higher EMI emissions compared to SLOW slew rate.

Table 7-15, Table 7-16 and Figure 7-6 assume testing over the recommended operating conditions and electrical characteristic conditions

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### Table 7-15. DPI Video Output i (i = 1..3) Default Switching Characteristics

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| D1 | $t_{c(clk)}$ | Cycle time, output pixel clock vouti_clk | | 11.76 (2) | | ns |
| D2 | $t_{w(clkL)}$ | Pulse duration, output pixel clock vouti_clk low | DPI1, DPI2 (IOSET1), DPI3 | P*0.5-1 (1) | | ns |
| | | | DPI2 (IOSET2) | P*0.5-1.35 (1) | | ns |
| D3 | $t_{w(clkH)}$ | Pulse duration, output pixel clock vouti_clk high | DPI1, DPI2 (IOSET1), DPI3 | P*0.5-1 (1) | | ns |
| | | | DPI2 (IOSET2) | P*0.5-1.35 (1) | | ns |
| D5 | $t_{d(clk-dV)}$ | Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid | DPI1 | -2.5 | 2.5 | ns |
| | | | DPI2 (IOSET1) | -2.5 | 2.5 | ns |
| | | | DPI2 (IOSET2) | -2.5 | 2.5 | ns |
| | | | DPI3 (IOSET1) | -2.5 | 2.5 | ns |
| | | | DPI3 (IOSET2/3) | -2.5 | 2.5 | ns |
| D6 | $t_{d(clk-ctlV)}$ | Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid | DPI1 | -2.5 | 2.5 | ns |
| | | | DPI2 (IOSET1) | -2.5 | 2.5 | ns |
| | | | DPI2 (IOSET2) | -2.5 | 2.5 | ns |
| | | | DPI3 (IOSET1) | -2.5 | 2.5 | ns |
| | | | DPI3 (IOSET2/3) | -2.5 | 2.5 | ns |

(1) P = output vouti_clk period in ns.

(2) All pads/balls configured as vouti_* signals are recommended to use slow slew rate by setting the corresponding CTRL_CORE_PAD_*[SLEWCONTROL] register field to SLOW (0b1). FAST slew setting is allowed, but results in faster edge rates on the VOUTn bus, higher power/ground noise, and higher EMI emissions compared to SLOW slew rate.

(3) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. A clock jitter cleaner such as the CDCE813 may be needed to meet the required jitter masks of the SERDES transceiver. See Application Note **SPRAC62** for general reference on a similar device with the same interface.

### Table 7-16. DPI Video Output i (i = 1..3) Alternate Switching Characteristics

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| D1 | $t_{c(clk)}$ | Cycle time, output pixel clock vouti_clk | | 6.06 (2) | | ns |
| D2 | $t_{w(clkL)}$ | Pulse duration, output pixel clock vouti_clk low | | P*0.5-1 (1) | | ns |
| D3 | $t_{w(clkH)}$ | Pulse duration, output pixel clock vouti_clk high | | P*0.5-1 (1) | | ns |
| D5 | $t_{d(clk-ctlV)}$ | Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid | DPI1 | 1.51 | 4.55 | ns |
| | | | DPI2 (IOSET1) | 1.51 | 4.55 | ns |
| | | | DPI2 (IOSET2) | 1.51 | 4.55 | ns |
| | | | DPI3 | 1.51 | 4.55 | ns |
| D6 | $t_{d(clk-dV)}$ | Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid | DPI1 | 1.51 | 4.55 | ns |
| | | | DPI2 (IOSET1) | 1.51 | 4.55 | ns |
| | | | DPI2 (IOSET2) | 1.51 | 4.55 | ns |
| | | | DPI3 | 1.51 | 4.55 | ns |

(1) P = output vouti_clk period in ns.

(2) All pads/balls configured as vouti_* signals are recommended to use slow slew rate by setting the corresponding CTRL_CORE_PAD_*[SLEWCONTROL] register field to SLOW (0b1). FAST slew setting is allowed, but results in faster edge rates on the VOUTn bus, higher power/ground noise, and higher EMI emissions compared to SLOW slew rate.

(3) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. A clock jitter cleaner such as the CDCE813 may be needed to meet the required jitter masks of the SERDES transceiver. See Application Note **SPRAC62** for general reference on a similar device with the same interface.

### Table 7-17. DPI Video Output i (i = 1..3) MANUAL3 Switching Characteristics

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| D1 | $t_{c(clk)}$ | Cycle time, output pixel clock vouti_clk | | 6.06 (2) | | ns |
| D2 | $t_{w(clkL)}$ | Pulse duration, output pixel clock vouti_clk low | | P*0.5-1 (1) | | ns |
| D3 | $t_{w(clkH)}$ | Pulse duration, output pixel clock vouti_clk high | | P*0.5-1 (1) | | ns |
| D5 | $t_{d(clk-ctlV)}$ | Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid | DPI1 | 2.85 | 5.56 | ns |
| | | | DPI2, DPI3 | 2.78 | 5.91 | ns |
| D6 | $t_{d(clk-dV)}$ | Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid | DPI1 | 2.85 | 5.56 | ns |
| | | | DPI2, DPI3 | 2.78 | 5.91 | ns |

(1) P = output vouti_clk period in ns.

(2) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. A clock jitter cleaner such as the CDCE813 may be needed to meet the required jitter masks of the SERDES transceiver. See Application Note **SPRAC62** for general reference on a similar device with the same interface.

### Table 7-18. DPI Video Output i (i = 1..3) MANUAL4 Switching Characteristics

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| D1 | $t_{c(clk)}$ | Cycle time, output pixel clock vouti_clk | | 6.06 (2) | | ns |
| D2 | $t_{w(clkL)}$ | Pulse duration, output pixel clock vouti_clk low | | P*0.5-1 (1) | | ns |
| D3 | $t_{w(clkH)}$ | Pulse duration, output pixel clock vouti_clk high | | P*0.5-1 (1) | | ns |
| D5 | $t_{d(clk-ctlV)}$ | Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid | DPI1, DPI2, DPI3 | 3.55 | 6.61 | ns |
| D6 | $t_{d(clk-dV)}$ | Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid | DPI1, DPI2, DPI3 | 3.55 | 6.61 | ns |


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(1) P = output vouti_clk period in ns.

(2) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. A clock jitter cleaner such as the CDCE813 may be needed to meet the required jitter masks of the SERDES transceiver. See Application Note **SPRAC62** for general reference on a similar device with the same interface.

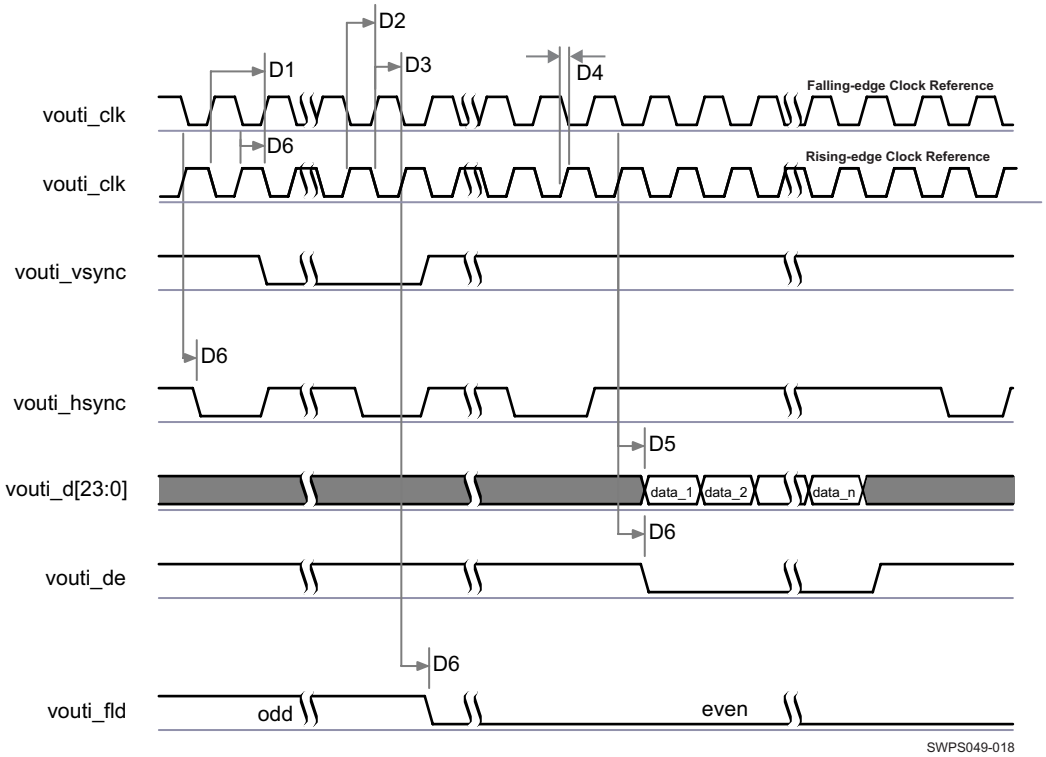


**Figure 7-6. DPI Video Output[(1)(2)(3)]**

(1) The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.

(2) The polarity and the pulse width of vouti_hsync and vouti_vsync are programmable, refer to the DSS section of the device TRM.

(3) The vouti_clk frequency can be configured, refer to the DSS section of the device TRM.

**NOTE**

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented in Table 4-3 and described in Control Module chapter of the Device TRM.

In Table 7-19 are presented the specific groupings of signals (IOSET) for use with VOUT2.

**Table 7-19. VOUT2 IOSETs**

| SIGNALS | IOSET1 | | IOSET2 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| vout2_d23 | F2 | 4 | AA4 | 6 |
| vout2_d22 | F3 | 4 | AB3 | 6 |
| vout2_d21 | D1 | 4 | AB9 | 6 |
| vout2_d20 | E2 | 4 | AA3 | 6 |
| vout2_d19 | D2 | 4 | D17 | 6 |
| vout2_d18 | F4 | 4 | G16 | 6 |
| vout2_d17 | C1 | 4 | A21 | 6 |
| vout2_d16 | E4 | 4 | C18 | 6 |

**Table 7-19. VOUT2 IOSETs (continued)**

| SIGNALS | IOSET1 | | IOSET2 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| vout2_d15 | F5 | 4 | A17 | 6 |
| vout2_d14 | E6 | 4 | B17 | 6 |
| vout2_d13 | D3 | 4 | B16 | 6 |
| vout2_d12 | F6 | 4 | D15 | 6 |
| vout2_d11 | D5 | 4 | A15 | 6 |
| vout2_d10 | C2 | 4 | B15 | 6 |
| vout2_d9 | C3 | 4 | A20 | 6 |
| vout2_d8 | C4 | 4 | E15 | 6 |
| vout2_d7 | B2 | 4 | D12 | 6 |
| vout2_d6 | D6 | 4 | C12 | 6 |
| vout2_d5 | C5 | 4 | F13 | 6 |
| vout2_d4 | A3 | 4 | E12 | 6 |
| vout2_d3 | B3 | 4 | J11 | 6 |
| vout2_d2 | B4 | 4 | G13 | 6 |
| vout2_d1 | B5 | 4 | J14 | 6 |
| vout2_d0 | A4 | 4 | B14 | 6 |
| vout2_vsync | G6 | 4 | F20 | 6 |
| vout2_hsync | G1 | 4 | E21 | 6 |
| vout2_clk | H7 | 4 | B26 | 6 |
| vout2_fld | E1 | 4 | F21 | 6 |
| vout2_de | G2 | 4 | C23 | 6 |

In Table 7-20 are presented the specific groupings of signals (IOSET) for use with VOUT3.

**Table 7-20. VOUT3 IOSETs**

| SIGNALS | IOSET1 | | IOSET2 (1) | | IOSET3 (1) | |
|---|---|---|---|---|---|---|
| | BALL | MUX | BALL | MUX | BALL | MUX |
| vout3_d23 | P5 | 3 | AE8 | 4 | | |
| vout3_d22 | R5 | 3 | AD8 | 4 | | |
| vout3_d21 | R9 | 3 | AG7 | 4 | | |
| vout3_d20 | P6 | 3 | AH6 | 4 | | |
| vout3_d19 | T7 | 3 | AH3 | 4 | | |
| vout3_d18 | T6 | 3 | AH5 | 4 | | |
| vout3_d17 | T9 | 3 | AG6 | 4 | AD9 | 3 |
| vout3_d16 | R6 | 3 | AH4 | 4 | AG8 | 3 |
| vout3_d15 | H3 | 3 | AG4 | 4 | AG4 | 4 |
| vout3_d14 | H2 | 3 | AG2 | 4 | AG2 | 4 |
| vout3_d13 | J3 | 3 | AG3 | 4 | AG3 | 4 |
| vout3_d12 | H1 | 3 | AG5 | 4 | AG5 | 4 |
| vout3_d11 | J2 | 3 | AF2 | 4 | AF2 | 4 |
| vout3_d10 | J1 | 3 | AF6 | 4 | AF6 | 4 |
| vout3_d9 | K2 | 3 | AF3 | 4 | AF3 | 4 |
| vout3_d8 | L1 | 3 | AF4 | 4 | AF4 | 4 |
| vout3_d7 | L2 | 3 | AF1 | 4 | AE8 | 3 |
| vout3_d6 | L3 | 3 | AE3 | 4 | AD8 | 3 |
| vout3_d5 | L4 | 3 | AE5 | 4 | AG7 | 3 |
| vout3_d4 | L6 | 3 | AE1 | 4 | AH6 | 3 |


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**Table 7-20. VOUT3 IOSETs (continued)**

| SIGNALS | IOSET1 | | IOSET2 (1) | | IOSET3 (1) | |
|---|---|---|---|---|---|---|
| | BALL | MUX | BALL | MUX | BALL | MUX |
| vout3_d3 | M1 | 3 | AE2 | 4 | AH3 | 3 |
| vout3_d2 | L5 | 3 | AE6 | 4 | AH5 | 3 |
| vout3_d1 | M2 | 3 | AD2 | 4 | AG6 | 3 |
| vout3_d0 | M6 | 3 | AD3 | 4 | AH4 | 3 |
| vout3_de | N9 | 3 | AD9 | 4 | | |
| vout3_vsync | R4 | 3 | AF8 | 4 | AF8 | 4 |
| vout3_clk | P1 | 3 | AF9 | 4 | AF9 | 4 |
| vout3_hsync | N7 | 3 | AE9 | 4 | AE9 | 4 |
| vout3_fld | P9 | 3 | AG8 | 4 | | |

(1) The VOUT3 interface when multiplexed onto balls mapped to the VDDSHV6 supply rail is restricted to operating in 1.8V mode only (VDDSHV6 must be supplied with 1.8V). 3.3V mode is not supported. This must be considered in the pin mux programming and VDDSHVx supply connections.

**NOTE**

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the Control Module chapter in the Device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for VOUT1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-21 *Manual Functions Mapping for DSS VOUT1* for a definition of the Manual modes.

Table 7-21 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

### Table 7-21. Manual Functions Mapping for DSS VOUT1

| BALL | BALL NAME | VOUT1_MANUAL1 | | VOUT1_MANUAL2 | | VOUT1_MANUAL3 | | VOUT1_MANUAL4 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 0 |
| D11 | vout1_clk | 0 | 706 | 1126 | 751 | 0 | 466 | 0 | 466 | CFG_VOUT1_CLK_OUT | vout1_clk |
| F11 | vout1_d0 | 2313 | 0 | 395 | 0 | 3436 | 0 | 4306 | 0 | CFG_VOUT1_D0_OUT | vout1_d0 |
| G10 | vout1_d1 | 2439 | 0 | 521 | 0 | 3562 | 0 | 4432 | 0 | CFG_VOUT1_D1_OUT | vout1_d1 |
| D7 | vout1_d10 | 2199 | 0 | 282 | 0 | 3323 | 0 | 3993 | 0 | CFG_VOUT1_D10_OUT | vout1_d10 |
| D8 | vout1_d11 | 2266 | 0 | 348 | 0 | 3390 | 0 | 4060 | 0 | CFG_VOUT1_D11_OUT | vout1_d11 |
| A5 | vout1_d12 | 3159 | 0 | 1240 | 0 | 4281 | 0 | 4951 | 0 | CFG_VOUT1_D12_OUT | vout1_d12 |
| C6 | vout1_d13 | 2100 | 0 | 182 | 0 | 3223 | 0 | 4093 | 0 | CFG_VOUT1_D13_OUT | vout1_d13 |
| C8 | vout1_d14 | 2229 | 0 | 311 | 0 | 3353 | 0 | 4223 | 0 | CFG_VOUT1_D14_OUT | vout1_d14 |
| C7 | vout1_d15 | 2202 | 0 | 285 | 0 | 3326 | 0 | 4196 | 0 | CFG_VOUT1_D15_OUT | vout1_d15 |
| B7 | vout1_d16 | 2084 | 0 | 166 | 0 | 3208 | 0 | 4078 | 0 | CFG_VOUT1_D16_OUT | vout1_d16 |
| B8 | vout1_d17 | 2195 | 0 | 278 | 0 | 3319 | 0 | 4189 | 0 | CFG_VOUT1_D17_OUT | vout1_d17 |
| A7 | vout1_d18 | 2342 | 0 | 425 | 0 | 3466 | 0 | 4136 | 0 | CFG_VOUT1_D18_OUT | vout1_d18 |
| A8 | vout1_d19 | 2463 | 0 | 516 | 0 | 3557 | 0 | 4227 | 0 | CFG_VOUT1_D19_OUT | vout1_d19 |
| F10 | vout1_d2 | 2200 | 0 | 282 | 0 | 3324 | 0 | 4194 | 0 | CFG_VOUT1_D2_OUT | vout1_d2 |
| C9 | vout1_d20 | 2304 | 0 | 386 | 0 | 3428 | 0 | 4298 | 0 | CFG_VOUT1_D20_OUT | vout1_d20 |
| A9 | vout1_d21 | 2103 | 0 | 111 | 0 | 3193 | 0 | 4063 | 0 | CFG_VOUT1_D21_OUT | vout1_d21 |
| B9 | vout1_d22 | 2145 | 0 | 227 | 0 | 3268 | 0 | 4138 | 0 | CFG_VOUT1_D22_OUT | vout1_d22 |
| A10 | vout1_d23 | 1932 | 0 | 0 | 0 | 3039 | 0 | 3909 | 0 | CFG_VOUT1_D23_OUT | vout1_d23 |
| G11 | vout1_d3 | 2355 | 0 | 438 | 0 | 3479 | 0 | 4349 | 0 | CFG_VOUT1_D3_OUT | vout1_d3 |
| E9 | vout1_d4 | 3215 | 0 | 1298 | 0 | 4339 | 0 | 5209 | 0 | CFG_VOUT1_D4_OUT | vout1_d4 |
| F9 | vout1_d5 | 2314 | 0 | 397 | 0 | 3438 | 0 | 4308 | 0 | CFG_VOUT1_D5_OUT | vout1_d5 |
| F8 | vout1_d6 | 2238 | 0 | 321 | 0 | 3362 | 0 | 4082 | 0 | CFG_VOUT1_D6_OUT | vout1_d6 |
| E7 | vout1_d7 | 2381 | 0 | 155 | 309 | 3505 | 0 | 4175 | 0 | CFG_VOUT1_D7_OUT | vout1_d7 |
| E8 | vout1_d8 | 2138 | 0 | 212 | 0 | 3253 | 0 | 4123 | 0 | CFG_VOUT1_D8_OUT | vout1_d8 |
| D9 | vout1_d9 | 2383 | 0 | 466 | 0 | 3507 | 0 | 4377 | 0 | CFG_VOUT1_D9_OUT | vout1_d9 |
| B10 | vout1_de | 1984 | 0 | 0 | 0 | 3085 | 0 | 3955 | 0 | CFG_VOUT1_DE_OUT | vout1_de |
| B11 | vout1_fld | 2265 | 0 | 236 | 0 | 3337 | 0 | 4207 | 0 | CFG_VOUT1_FLD_OUT | vout1_fld |
| C11 | vout1_hsync | 1947 | 0 | 0 | 0 | 3052 | 0 | 3922 | 0 | CFG_VOUT1_HSYNC_OUT | vout1_hsync |
| E11 | vout1_vsync | 2739 | 0 | 139 | 701 | 3863 | 0 | 4733 | 0 | CFG_VOUT1_VSYNC_OUT | vout1_vsync |


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Manual IO Timings Modes must be used to ensure some IO timings for VOUT2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-22 *Manual Functions Mapping for DSS VOUT2* for a definition of the Manual modes.

Table 7-22 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-22. Manual Functions Mapping for DSS VOUT2 IOSET1**

| BALL | BALL NAME | VOUT2_IOSET1_MANUAL 1 | | VOUT2_IOSET1_MANUAL 2 | | VOUT2_IOSET1_MANUAL 3 | | VOUT2_IOSET1_MANUAL 4 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 4 |
| E1 | vin2a_clk0 | 2718 | 0 | 819 | 0 | 3794 | 0 | 4664 | 0 | CFG_VIN2A_CLK0_OUT | vout2_fld |
| F2 | vin2a_d0 | 2680 | 0 | 485 | 296 | 3757 | 0 | 4627 | 0 | CFG_VIN2A_D0_OUT | vout2_d23 |
| F3 | vin2a_d1 | 2633 | 0 | 733 | 0 | 3710 | 0 | 4580 | 0 | CFG_VIN2A_D1_OUT | vout2_d22 |
| D3 | vin2a_d10 | 1867 | 0 | 0 | 0 | 2954 | 0 | 3824 | 0 | CFG_VIN2A_D10_OUT | vout2_d13 |
| F6 | vin2a_d11 | 2457 | 0 | 431 | 127 | 3534 | 0 | 4404 | 0 | CFG_VIN2A_D11_OUT | vout2_d12 |
| D5 | vin2a_d12 | 2683 | 1016 | 1286 | 514 | 3628 | 648 | 4498 | 648 | CFG_VIN2A_D12_OUT | vout2_d11 |
| C2 | vin2a_d13 | 2629 | 985 | 1229 | 486 | 3569 | 622 | 4439 | 622 | CFG_VIN2A_D13_OUT | vout2_d10 |
| C3 | vin2a_d14 | 2531 | 804 | 1126 | 309 | 3460 | 452 | 4530 | 452 | CFG_VIN2A_D14_OUT | vout2_d9 |
| C4 | vin2a_d15 | 2624 | 818 | 1227 | 315 | 3567 | 452 | 4537 | 452 | CFG_VIN2A_D15_OUT | vout2_d8 |
| B2 | vin2a_d16 | 2747 | 767 | 1357 | 256 | 3704 | 386 | 4574 | 386 | CFG_VIN2A_D16_OUT | vout2_d7 |
| D6 | vin2a_d17 | 2622 | 841 | 1226 | 337 | 3616 | 474 | 4686 | 474 | CFG_VIN2A_D17_OUT | vout2_d6 |
| C5 | vin2a_d18 | 2328 | 0 | 430 | 0 | 3406 | 0 | 4276 | 0 | CFG_VIN2A_D18_OUT | vout2_d5 |
| A3 | vin2a_d19 | 2300 | 0 | 401 | 0 | 3427 | 0 | 4197 | 0 | CFG_VIN2A_D19_OUT | vout2_d4 |
| D1 | vin2a_d2 | 2452 | 0 | 446 | 106 | 3528 | 0 | 4398 | 0 | CFG_VIN2A_D2_OUT | vout2_d21 |
| B3 | vin2a_d20 | 1998 | 0 | 98 | 0 | 3075 | 0 | 3845 | 0 | CFG_VIN2A_D20_OUT | vout2_d3 |
| B4 | vin2a_d21 | 1953 | 0 | 54 | 0 | 3030 | 0 | 3900 | 0 | CFG_VIN2A_D21_OUT | vout2_d2 |
| B5 | vin2a_d22 | 1893 | 0 | 0 | 0 | 3030 | 0 | 3900 | 0 | CFG_VIN2A_D22_OUT | vout2_d1 |
| A4 | vin2a_d23 | 1936 | 0 | 36 | 0 | 3013 | 0 | 3883 | 0 | CFG_VIN2A_D23_OUT | vout2_d0 |
| E2 | vin2a_d3 | 2494 | 0 | 595 | 0 | 3571 | 0 | 4441 | 0 | CFG_VIN2A_D3_OUT | vout2_d20 |
| D2 | vin2a_d4 | 3001 | 153 | 1254 | 0 | 4231 | 0 | 4901 | 0 | CFG_VIN2A_D4_OUT | vout2_d19 |
| F4 | vin2a_d5 | 2463 | 0 | 563 | 0 | 3539 | 0 | 4409 | 0 | CFG_VIN2A_D5_OUT | vout2_d18 |
| C1 | vin2a_d6 | 2456 | 0 | 558 | 0 | 3334 | 0 | 4404 | 0 | CFG_VIN2A_D6_OUT | vout2_d17 |
| E4 | vin2a_d7 | 2431 | 0 | 532 | 0 | 3509 | 0 | 4379 | 0 | CFG_VIN2A_D7_OUT | vout2_d16 |
| F5 | vin2a_d8 | 2262 | 0 | 363 | 0 | 3340 | 0 | 4210 | 0 | CFG_VIN2A_D8_OUT | vout2_d15 |
| E6 | vin2a_d9 | 2145 | 0 | 246 | 0 | 3222 | 0 | 4092 | 0 | CFG_VIN2A_D9_OUT | vout2_d14 |
| G2 | vin2a_de0 | 2597 | 0 | 550 | 149 | 3675 | 0 | 4545 | 0 | CFG_VIN2A_DE0_OUT | vout2_de |
| H7 | vin2a_fld0 | 0 | 957 | 1208 | 969 | 0 | 686 | 0 | 686 | CFG_VIN2A_FLD0_OUT | vout2_clk |

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**Table 7-22. Manual Functions Mapping for DSS VOUT2 IOSET1 (continued)**

| BALL | BALL NAME | VOUT2_IOSET1_MANUAL 1 | | VOUT2_IOSET1_MANUAL 2 | | VOUT2_IOSET1_MANUAL 3 | | VOUT2_IOSET1_MANUAL 4 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 4 |
| G1 | vin2a_hsync0 | 2958 | 0 | 1059 | 0 | 4035 | 0 | 4905 | 0 | CFG_VIN2A_HSYNC0_OUT | vout2_hsync |
| G6 | vin2a_vsync0 | 2752 | 0 | 853 | 0 | 3829 | 0 | 4699 | 0 | CFG_VIN2A_VSYNC0_OUT | vout2_vsync |

Manual IO Timings Modes must be used to ensure some IO timings for VOUT2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-23 *Manual Functions Mapping for DSS VOUT2 IOSET2* for a definition of the Manual modes.

Table 7-23 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-23. Manual Functions Mapping for DSS VOUT2 IOSET2**

| BALL | BALL NAME | VOUT2_IOSET2_MANUAL 1 | | VOUT2_IOSET2_MANUAL 2 | | VOUT2_IOSET2_MANUAL 3 | | VOUT2_IOSET2_MANUAL 4 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 6 |
| E21 | gpio6_14 | 1547 | 30 | 0 | 0 | 2298 | 0 | 3168 | 0 | CFG_GPIO6_14_OUT | vout2_hsync |
| F20 | gpio6_15 | 1773 | 31 | 209 | 0 | 2484 | 0 | 3354 | 0 | CFG_GPIO6_15_OUT | vout2_vsync |
| F21 | gpio6_16 | 1547 | 27 | 33 | 0 | 2345 | 0 | 3215 | 0 | CFG_GPIO6_16_OUT | vout2_fld |
| B14 | mcasp1_aclkr | 3738 | 2 | 2636 | 0 | 4925 | 0 | 5795 | 0 | CFG_MCASP1_ACLKR_OUT | vout2_d0 |
| G13 | mcasp1_axr2 | 2846 | 4 | 1730 | 0 | 4003 | 0 | 4873 | 0 | CFG_MCASP1_AXR2_OUT | vout2_d2 |
| J11 | mcasp1_axr3 | 2831 | 17 | 1498 | 0 | 3771 | 0 | 4541 | 0 | CFG_MCASP1_AXR3_OUT | vout2_d3 |
| E12 | mcasp1_axr4 | 3009 | 5 | 1879 | 0 | 4152 | 0 | 5022 | 0 | CFG_MCASP1_AXR4_OUT | vout2_d4 |
| F13 | mcasp1_axr5 | 3009 | 9 | 1802 | 0 | 4075 | 0 | 4945 | 0 | CFG_MCASP1_AXR5_OUT | vout2_d5 |
| C12 | mcasp1_axr6 | 2875 | 2 | 1792 | 0 | 4065 | 0 | 4935 | 0 | CFG_MCASP1_AXR6_OUT | vout2_d6 |
| D12 | mcasp1_axr7 | 2893 | 7 | 1717 | 0 | 3991 | 0 | 4861 | 0 | CFG_MCASP1_AXR7_OUT | vout2_d7 |
| J14 | mcasp1_fsr | 2729 | 13 | 1466 | 0 | 3739 | 0 | 4609 | 0 | CFG_MCASP1_FSR_OUT | vout2_d1 |
| E15 | mcasp2_aclkr | 3753 | 13 | 2488 | 0 | 4761 | 0 | 5631 | 0 | CFG_MCASP2_ACLKR_OUT | vout2_d8 |


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**Table 7-23. Manual Functions Mapping for DSS VOUT2 IOSET2 (continued)**

| BALL | BALL NAME | VOUT2_IOSET2_MANUAL 1 | | VOUT2_IOSET2_MANUAL 2 | | VOUT2_IOSET2_MANUAL 3 | | VOUT2_IOSET2_MANUAL 4 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 6 |
| B15 | mcasp2_axr0 | 2182 | 6 | 1022 | 0 | 3294 | 0 | 4164 | 0 | CFG_MCASP2_AXR0_OUT | vout2_d10 |
| A15 | mcasp2_axr1 | 2324 | 5 | 1179 | 0 | 3452 | 0 | 4322 | 0 | CFG_MCASP2_AXR1_OUT | vout2_d11 |
| D15 | mcasp2_axr4 | 2434 | 0 | 1374 | 0 | 3647 | 0 | 4517 | 0 | CFG_MCASP2_AXR4_OUT | vout2_d12 |
| B16 | mcasp2_axr5 | 2287 | 4 | 1164 | 0 | 3437 | 0 | 4307 | 0 | CFG_MCASP2_AXR5_OUT | vout2_d13 |
| B17 | mcasp2_axr6 | 3598 | 13 | 2339 | 0 | 4599 | 0 | 5469 | 0 | CFG_MCASP2_AXR6_OUT | vout2_d14 |
| A17 | mcasp2_axr7 | 2231 | 15 | 931 | 0 | 3204 | 0 | 4074 | 0 | CFG_MCASP2_AXR7_OUT | vout2_d15 |
| A20 | mcasp2_fsr | 1944 | 11 | 715 | 0 | 2988 | 0 | 3858 | 0 | CFG_MCASP2_FSR_OUT | vout2_d9 |
| C18 | mcasp4_aclkx | 3241 | 8 | 2051 | 0 | 4324 | 0 | 5194 | 0 | CFG_MCASP4_ACLKX_OUT | vout2_d16 |
| G16 | mcasp4_axr0 | 2236 | 22 | 830 | 0 | 3090 | 0 | 3960 | 0 | CFG_MCASP4_AXR0_OUT | vout2_d18 |
| D17 | mcasp4_axr1 | 1803 | 16 | 505 | 0 | 2766 | 0 | 3636 | 0 | CFG_MCASP4_AXR1_OUT | vout2_d19 |
| A21 | mcasp4_fsx | 1901 | 19 | 541 | 0 | 2801 | 0 | 3671 | 0 | CFG_MCASP4_FSX_OUT | vout2_d17 |
| AA3 | mcasp5_aclkx | 4582 | 2178 | 3499 | 1978 | 6020 | 1755 | 6890 | 1755 | CFG_MCASP5_ACLKX_OUT | vout2_d20 |
| AB3 | mcasp5_axr0 | 4628 | 1604 | 3505 | 1402 | 6025 | 1178 | 6895 | 1178 | CFG_MCASP5_AXR0_OUT | vout2_d22 |
| AA4 | mcasp5_axr1 | 4757 | 1237 | 3457 | 1063 | 5987 | 806 | 6857 | 806 | CFG_MCASP5_AXR1_OUT | vout2_d23 |
| AB9 | mcasp5_fsx | 4683 | 1485 | 3443 | 1280 | 5961 | 1059 | 6831 | 1059 | CFG_MCASP5_FSX_OUT | vout2_d21 |
| B26 | xref_clk2 | 0 | 850 | 1900 | 1150 | 0 | 730 | 0 | 730 | CFG_XREF_CLK2_OUT | vout2_clk |
| C23 | xref_clk3 | 3075 | 19 | 1752 | 0 | 4012 | 0 | 4882 | 0 | CFG_XREF_CLK3_OUT | vout2_de |

Manual IO Timings Modes must be used to ensure some IO timings for VOUT3. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-24 *Manual Functions Mapping for DSS VOUT3* for a definition of the Manual modes.

Table 7-24 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

### Table 7-24. Manual Functions Mapping for DSS VOUT3

| BALL | BALL NAME | VOUT3_MANUAL1 | | VOUT3_MANUAL2 | | VOUT3_MANUAL3 | | VOUT3_MANUAL4 | | CFG REGISTER | MUXMODE | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 3 | 4 |
| R6 | gpmc_a0 | 3069 | 0 | 565 | 267 | 3365 | 0 | 4235 | 0 | CFG_GPMC_A0_OUT | vout3_d16 | - |
| T9 | gpmc_a1 | 2888 | 0 | 650 | 0 | 3183 | 0 | 4053 | 0 | CFG_GPMC_A1_OUT | vout3_d17 | - |
| N9 | gpmc_a10 | 3595 | 0 | 1157 | 0 | 3690 | 0 | 4560 | 0 | CFG_GPMC_A10_OUT | vout3_de | - |
| P9 | gpmc_a11 | 3891 | 14 | 669 | 970 | 4170 | 0 | 5040 | 0 | CFG_GPMC_A11_OUT | vout3_fld | - |
| T6 | gpmc_a2 | 2934 | 0 | 705 | 0 | 3238 | 0 | 4108 | 0 | CFG_GPMC_A2_OUT | vout3_d18 | - |
| T7 | gpmc_a3 | 3944 | 4 | 1521 | 0 | 4054 | 0 | 4924 | 0 | CFG_GPMC_A3_OUT | vout3_d19 | - |
| P6 | gpmc_a4 | 4456 | 261 | 1837 | 0 | 4370 | 0 | 5240 | 0 | CFG_GPMC_A4_OUT | vout3_d20 | - |
| R9 | gpmc_a5 | 2915 | 0 | 739 | 0 | 3273 | 0 | 4143 | 0 | CFG_GPMC_A5_OUT | vout3_d21 | - |
| R5 | gpmc_a6 | 3192 | 0 | 937 | 0 | 3471 | 0 | 4341 | 0 | CFG_GPMC_A6_OUT | vout3_d22 | - |
| P5 | gpmc_a7 | 3182 | 0 | 944 | 0 | 3477 | 0 | 4347 | 0 | CFG_GPMC_A7_OUT | vout3_d23 | - |
| N7 | gpmc_a8 | 4124 | 75 | 1843 | 0 | 4375 | 0 | 5245 | 0 | CFG_GPMC_A8_OUT | vout3_hsync | - |
| R4 | gpmc_a9 | 4252 | 0 | 998 | 0 | 3530 | 0 | 4400 | 0 | CFG_GPMC_A9_OUT | vout3_vsync | - |
| M6 | gpmc_ad0 | 3501 | 52 | 1151 | 0 | 3684 | 0 | 4534 | 0 | CFG_GPMC_AD0_OUT | vout3_d0 | - |
| M2 | gpmc_ad1 | 3163 | 0 | 956 | 0 | 3489 | 0 | 4339 | 0 | CFG_GPMC_AD1_OUT | vout3_d1 | - |
| J1 | gpmc_ad10 | 3130 | 0 | 1064 | 0 | 3598 | 0 | 4148 | 0 | CFG_GPMC_AD10_OUT | vout3_d10 | - |
| J2 | gpmc_ad11 | 2821 | 0 | 809 | 0 | 3344 | 0 | 3894 | 0 | CFG_GPMC_AD11_OUT | vout3_d11 | - |
| H1 | gpmc_ad12 | 3290 | 0 | 1161 | 0 | 3694 | 0 | 4244 | 0 | CFG_GPMC_AD12_OUT | vout3_d12 | - |
| J3 | gpmc_ad13 | 2573 | 0 | 524 | 0 | 3058 | 0 | 3908 | 0 | CFG_GPMC_AD13_OUT | vout3_d13 | - |
| H2 | gpmc_ad14 | 2540 | 0 | 632 | 0 | 3165 | 0 | 3715 | 0 | CFG_GPMC_AD14_OUT | vout3_d14 | - |
| H3 | gpmc_ad15 | 3181 | 0 | 1012 | 0 | 3545 | 0 | 4295 | 0 | CFG_GPMC_AD15_OUT | vout3_d15 | - |
| L5 | gpmc_ad2 | 3550 | 45 | 1222 | 0 | 3756 | 0 | 4506 | 0 | CFG_GPMC_AD2_OUT | vout3_d2 | - |
| M1 | gpmc_ad3 | 2922 | 0 | 875 | 0 | 3408 | 0 | 4158 | 0 | CFG_GPMC_AD3_OUT | vout3_d3 | - |
| L6 | gpmc_ad4 | 3463 | 36 | 1170 | 0 | 3703 | 0 | 4453 | 0 | CFG_GPMC_AD4_OUT | vout3_d4 | - |
| L4 | gpmc_ad5 | 2299 | 17 | 358 | 0 | 2930 | 0 | 3780 | 0 | CFG_GPMC_AD5_OUT | vout3_d5 | - |
| L3 | gpmc_ad6 | 3346 | 0 | 1184 | 0 | 3717 | 0 | 4267 | 0 | CFG_GPMC_AD6_OUT | vout3_d6 | - |
| L2 | gpmc_ad7 | 2971 | 0 | 908 | 0 | 3441 | 0 | 3991 | 0 | CFG_GPMC_AD7_OUT | vout3_d7 | - |
| L1 | gpmc_ad8 | 874 | 234 | 0 | 0 | 1923 | 0 | 2873 | 0 | CFG_GPMC_AD8_OUT | vout3_d8 | - |
| K2 | gpmc_ad9 | 1160 | 221 | 0 | 0 | 2402 | 0 | 3252 | 0 | CFG_GPMC_AD9_OUT | vout3_d9 | - |
| P1 | gpmc_cs3 | 0 | 600 | 1505 | 1379 | 0 | 947 | 0 | 947 | CFG_GPMC_CS3_OUT | vout3_clk | - |
| AG8 | vin1a_clk0 | 2670 | 0 | 1280 | 0 | 3511 | 0 | 4381 | 0 | CFG_VIN1A_CLK0_OUT | vout3_d16 | vout3_fld |
| AE8 | vin1a_d0 | 2750 | 196 | 1286 | 0 | 3820 | 0 | 4690 | 0 | CFG_VIN1A_D0_OUT | vout3_d7 | vout3_d23 |
| AD8 | vin1a_d1 | 2409 | 240 | 1282 | 0 | 3816 | 0 | 4686 | 0 | CFG_VIN1A_D1_OUT | vout3_d6 | vout3_d22 |


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**Table 7-24. Manual Functions Mapping for DSS VOUT3 (continued)**

| BALL | BALL NAME | VOUT3_MANUAL1 | | VOUT3_MANUAL2 | | VOUT3_MANUAL3 | | VOUT3_MANUAL4 | | CFG REGISTER | MUXMODE | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 3 | 4 |
| AG3 | vin1a_d10 | 3026 | 270 | 1038 | 622 | 4228 | 0 | 5098 | 0 | CFG_VIN1A_D10_OUT | - | vout3_d13 |
| AG5 | vin1a_d11 | 2711 | 203 | 1141 | 0 | 3867 | 0 | 4737 | 0 | CFG_VIN1A_D11_OUT | - | vout3_d12 |
| AF2 | vin1a_d12 | 2924 | 539 | 1154 | 0 | 4422 | 0 | 5292 | 0 | CFG_VIN1A_D12_OUT | - | vout3_d11 |
| AF6 | vin1a_d13 | 2861 | 235 | 1339 | 0 | 3815 | 0 | 4685 | 0 | CFG_VIN1A_D13_OUT | - | vout3_d10 |
| AF3 | vin1a_d14 | 3176 | 377 | 892 | 0 | 4559 | 0 | 5429 | 0 | CFG_VIN1A_D14_OUT | - | vout3_d9 |
| AF4 | vin1a_d15 | 2806 | 232 | 1221 | 89 | 3755 | 0 | 4625 | 0 | CFG_VIN1A_D15_OUT | - | vout3_d8 |
| AF1 | vin1a_d16 | 2402 | 396 | 692 | 0 | 3873 | 0 | 4743 | 0 | CFG_VIN1A_D16_OUT | - | vout3_d7 |
| AE3 | vin1a_d17 | 2132 | 374 | 353 | 0 | 3860 | 0 | 4730 | 0 | CFG_VIN1A_D17_OUT | - | vout3_d6 |
| AE5 | vin1a_d18 | 2547 | 284 | 1109 | 0 | 3857 | 0 | 4727 | 0 | CFG_VIN1A_D18_OUT | - | vout3_d5 |
| AE1 | vin1a_d19 | 2095 | 575 | 640 | 180 | 3929 | 0 | 4799 | 0 | CFG_VIN1A_D19_OUT | - | vout3_d4 |
| AG7 | vin1a_d2 | 2546 | 189 | 1273 | 0 | 3806 | 0 | 4476 | 0 | CFG_VIN1A_D2_OUT | vout3_d5 | vout3_d21 |
| AE2 | vin1a_d20 | 1825 | 735 | 628 | 0 | 3552 | 0 | 4622 | 0 | CFG_VIN1A_D20_OUT | - | vout3_d3 |
| AE6 | vin1a_d21 | 2720 | 210 | 1322 | 0 | 4021 | 0 | 4891 | 0 | CFG_VIN1A_D21_OUT | - | vout3_d2 |
| AD2 | vin1a_d22 | 2361 | 413 | 746 | 0 | 3659 | 0 | 4729 | 0 | CFG_VIN1A_D22_OUT | - | vout3_d1 |
| AD3 | vin1a_d23 | 2731 | 273 | 1547 | 0 | 3775 | 0 | 4845 | 0 | CFG_VIN1A_D23_OUT | - | vout3_d0 |
| AH6 | vin1a_d3 | 2534 | 219 | 1357 | 0 | 3890 | 0 | 4760 | 0 | CFG_VIN1A_D3_OUT | vout3_d4 | vout3_d20 |
| AH3 | vin1a_d4 | 3015 | 538 | 2033 | 19 | 4585 | 0 | 5455 | 0 | CFG_VIN1A_D4_OUT | vout3_d3 | vout3_d19 |
| AH5 | vin1a_d5 | 2451 | 237 | 1039 | 0 | 3572 | 0 | 4442 | 0 | CFG_VIN1A_D5_OUT | vout3_d2 | vout3_d18 |
| AG6 | vin1a_d6 | 2505 | 191 | 1230 | 0 | 3763 | 0 | 4433 | 0 | CFG_VIN1A_D6_OUT | vout3_d1 | vout3_d17 |
| AH4 | vin1a_d7 | 2550 | 170 | 1235 | 0 | 3768 | 0 | 4638 | 0 | CFG_VIN1A_D7_OUT | vout3_d0 | vout3_d16 |
| AG4 | vin1a_d8 | 2847 | 285 | 1219 | 0 | 3850 | 0 | 4720 | 0 | CFG_VIN1A_D8_OUT | - | vout3_d15 |
| AG2 | vin1a_d9 | 2857 | 247 | 1113 | 256 | 3900 | 0 | 4770 | 0 | CFG_VIN1A_D9_OUT | - | vout3_d14 |
| AD9 | vin1a_de0 | 3164 | 0 | 1494 | 0 | 3728 | 0 | 4848 | 0 | CFG_VIN1A_DE0_OUT | vout3_d17 | vout3_de |
| AF9 | vin1a_fld0 | 0 | 1100 | 1718 | 869 | 261 | 384 | 261 | 384 | CFG_VIN1A_FLD0_OUT | - | vout3_clk |
| AE9 | vin1a_hsync0 | 3171 | 41 | 1439 | 0 | 3798 | 0 | 4668 | 0 | CFG_VIN1A_HSYNC0_OUT | - | vout3_hsync |
| AF8 | vin1a_vsync0 | 2956 | 110 | 1268 | 88 | 3610 | 0 | 4480 | 0 | CFG_VIN1A_VSYNC0_OUT | - | vout3_vsync |

## 7.8 Display Subsystem – High-Definition Multimedia Interface (HDMI)

The High-Definition Multimedia Interface is provided for transmitting digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. The HDMI interface is aligned with the HDMI TMDS single stream standard v1.4a (720p @60Hz to 1080p @24Hz) and the HDMI v1.3 (1080p @60Hz): 3 data channels, plus 1 clock channel is supported (differential).

**NOTE**

For more information, see the High-Definition Multimedia Interface section of the device TRM.

## 7.9 External Memory Interface (EMIF)

The device has a dedicated interface to DDR3 SDRAM. It supports JEDEC standard compliant DDR3 SDRAM devices with the following features:

- 16-bit or 32-bit data path to external SDRAM memory
- Memory device capacity: 128Mb, 256Mb, 512Mb, 1Gb, 2Gb, 4Gb and 8Gb devices (Single die only)
- One interface with associated DDR3 PHYs

**NOTE**

For more information, see the EMIF Controller section of the Device TRM.

## 7.10 General-Purpose Memory Controller (GPMC)

The GPMC is the unified memory controller that interfaces external memory devices such as:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous page mode and synchronous burst NOR flash
- NAND flash

**NOTE**

For more information, see the General-Purpose Memory Controller section of the Device TRM.

### *7.10.1 GPMC/NOR Flash Interface Synchronous Timing*

**CAUTION**

The IO Timings provided in this section are only valid for some GPMC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-25 and Table 7-26 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 7-7, Figure 7-8, Figure 7-9, Figure 7-10, Figure 7-11, and Figure 7-12).

**Table 7-25. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - Default**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| F12 | $t_{su(dV-clkH)}$ | Setup time, read gpmc_ad[15:0] valid before gpmc_clk high | 2.69 | | ns |
| F13 | $t_{h(clkH-dV)}$ | Hold time, read gpmc_ad[15:0] valid after gpmc_clk high | 1.53 | | ns |


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### Table 7-25. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - Default (continued)

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| F21 | $t_{su(waitV-clkH)}$ | Setup time, gpmc_wait[1:0] valid before gpmc_clk high | 2.23 | | ns |
| F22 | $t_{h(clkH-waitV)}$ | Hold Time, gpmc_wait[1:0] valid after gpmc_clk high | 1.52 | | ns |

**NOTE**

Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see General-Purpose Memory Controller section in the Device TRM.

### Table 7-26. GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Default

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| F0 | $t_{c(clk)}$ | Cycle time, output clock gpmc_clk period | 11.3 | | ns |
| F2 | $t_{d(clkH-nCSV)}$ | Delay time, gpmc_clk rising edge to gpmc_cs[7:0] transition | F-1.48(6) | F+3.84(6) | ns |
| F3 | $t_{d(clkH-nCSIV)}$ | Delay time, gpmc_clk rising edge to gpmc_cs[7:0] invalid | E-1.48(5) | E +3.84(5) | ns |
| F4 | $t_{d(ADDV-clk)}$ | Delay time, gpmc_a[27:0] address bus valid to gpmc_clk first edge | B-1.69(2) | B+3.76(2) | ns |
| F5 | $t_{d(clkH-ADDIV)}$ | Delay time, gpmc_clk rising edge to gpmc_a[27:0] gpmc address bus invalid | -1.69 | | ns |
| F6 | $t_{d(nBEV-clk)}$ | Delay time, gpmc_ben[1:0] valid to gpmc_clk rising edge | B-3.8(2) | B+2.37(2) | ns |
| F7 | $t_{d(clkH-nBEIV)}$ | Delay time, gpmc_clk rising edge to gpmc_ben[1:0] invalid | D-0.4(4) | D+1.1(4) | ns |
| F8 | $t_{d(clkH-nADV)}$ | Delay time, gpmc_clk rising edge to gpmc_advn_ale transition | G-1.48 (7) | G+3.84 (7) | ns |
| F9 | $t_{d(clkH-nADVIV)}$ | Delay time, gpmc_clk rising edge to gpmc_advn_ale invalid | D-1.48 (4) | G+3.84 (7) | ns |
| F10 | $t_{d(clkH-nOE)}$ | Delay time, gpmc_clk rising edge to gpmc_oen_ren transition | H-1.41 (8) | H+2.45 (8) | ns |
| F11 | $t_{d(clkH-nOEIV)}$ | Delay time, gpmc_clk rising edge to gpmc_oen_ren invalid | E-1.41 (5) | E+2.1 (5) | ns |
| F14 | $t_{d(clkH-nWE)}$ | Delay time, gpmc_clk rising edge to gpmc_wen transition | I-1.18 (9) | I+3.68 (9) | ns |
| F15 | $t_{d(clkH-Data)}$ | Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition | J-1.89 (10) | J+4.89 (10) | ns |
| F17 | $t_{d(clkH-nBE)}$ | Delay time, gpmc_clk rising edge to gpmc_ben[1:0] transition | J-1.3 (10) | J+3.8 (10) | ns |
| F18 | $t_{w(nCSV)}$ | Pulse duration, gpmc_cs[7:0] low | A (1) | | ns |
| F19 | $t_{w(nBEV)}$ | Pulse duration, gpmc_ben[1:0] low | C (3) | | ns |
| F20 | $t_{w(nADVV)}$ | Pulse duration, gpmc_advn_ale low | K (11) | | ns |
| F23 | $t_{d(CLK-GPIO)}$ | Delay time, gpmc_clk transition to gpio6_16.clkout1 transition | 1.2 | 6.1 | ns |

### Table 7-27. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - Alternate

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| F12 | $t_{su(dV-clkH)}$ | Setup time, read gpmc_ad[15:0] valid before gpmc_clk high | 3.56 | | ns |
| F13 | $t_{h(clkH-dV)}$ | Hold time, read gpmc_ad[15:0] valid after gpmc_clk high | 1.9 | | ns |
| F21 | $t_{su(waitV-clkH)}$ | Setup time, gpmc_wait[1:0] valid before gpmc_clk high | 3.1 | | ns |
| F22 | $t_{h(clkH-waitV)}$ | Hold Time, gpmc_wait[1:0] valid after gpmc_clk high | 1.9 | | ns |

### Table 7-28. GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| F0 | $t_{c(clk)}$ | Cycle time, output clock gpmc_clk period (12) | 15.04 | | ns |
| F2 | $t_{d(clkH-nCSV)}$ | Delay time, gpmc_clk rising edge to gpmc_cs[7:0] transition | F-0.84 (6) | F+6.73 (6) | ns |

### Table 7-28. GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate (continued)

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| F3 | $t_{d(clkH-nCSIV)}$ | Delay time, gpmc_clk rising edge to gpmc_cs[7:0] invalid | E-0.84 (5) | E+6.73 (5) | ns |
| F4 | $t_{d(ADDV-clk)}$ | Delay time, gpmc_a[27:0] address bus valid to gpmc_clk first edge | B-1.36 (2) | B+6.73 (2) | ns |
| F5 | $t_{d(clkH-ADDIV)}$ | Delay time, gpmc_clk rising edge to gpmc_a[27:0] gpmc address bus invalid | -1.36 | | ns |
| F6 | $t_{d(nBEV-clk)}$ | Delay time, gpmc_ben[1:0] valid to gpmc_clk rising edge | B-6.34 (2) | B+0.6 (2) | ns |
| F7 | $t_{d(clkH-nBEIV)}$ | Delay time, gpmc_clk rising edge to gpmc_ben[1:0] invalid | D-0.4 (4) | D+4.9 (4) | ns |
| F8 | $t_{d(clkH-nADV)}$ | Delay time, gpmc_clk rising edge to gpmc_advn_ale transition | G-0.67 (7) | G+6.1 (7) | ns |
| F9 | $t_{d(clkH-nADVIV)}$ | Delay time, gpmc_clk rising edge to gpmc_advn_ale invalid | D-0.67 (4) | D+6.1 (4) | ns |
| F10 | $t_{d(clkH-nOE)}$ | Delay time, gpmc_clk rising edge to gpmc_oen_ren transition | H-0.67 (8) | H+5.65 (8) | ns |
| F11 | $t_{d(clkH-nOEIV)}$ | Delay time, gpmc_clk rising edge to gpmc_oen_ren invalid | E-0.67 (5) | E+5.65 (5) | ns |
| F14 | $t_{d(clkH-nWE)}$ | Delay time, gpmc_clk rising edge to gpmc_wen transition | I-0.6 (9) | I+6.1 (9) | ns |
| F15 | $t_{d(clkH-Data)}$ | Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition | J-1.76 (10) | J+6.39 (10) | ns |
| F17 | $t_{d(clkH-nBE)}$ | Delay time, gpmc_clk rising edge to gpmc_ben[1:0] transition | J-0.6 (10) | J+6.34 (10) | ns |
| F18 | $t_{w(nCSV)}$ | Pulse duration, gpmc_cs[7:0] low | A (10) | | ns |
| F19 | $t_{w(nBEV)}$ | Pulse duration, gpmc_ben[1:0] low | C (3) | | ns |
| F20 | $t_{w(nADVV)}$ | Pulse duration, gpmc_advn_ale low | K (11) | | ns |
| F23 | $t_{d(CLK-GPIO)}$ | Delay time, gpmc_clk transition to gpio6_16.clkout1 transition (13) | 0.96 | 6.1 | ns |

(1) For single read: A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
with n the page burst access number.

(2) B = ClkActivationTime * GPMC_FCLK

(3) For single read: C = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: C = (RdCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For Burst write: C = (WrCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n the page burst access number.

(4) For single read: D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: D = (WrCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(5) For single read: E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: E = (CSWrOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(6) For nCS falling edge (CS activated):
Case GpmcFCLKDivider = 0 :
F = 0.5 * CSExtraDelay * GPMC_FCLK Case GpmcFCLKDivider = 1:
F = 0.5 * CSExtraDelay * GPMC_FCLK if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
F = 0.5 * CSExtraDelay * GPMC_FCLK if ((CSOnTime – ClkActivationTime) is a multiple of 3)
F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime – ClkActivationTime – 1) is a multiple of 3)
F = (2 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
F = 0.5 * CSExtraDelay * GPMC_FCLK if ((CSOnTime - ClkActivationTime) is a multiple of 4)
F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime - ClkActivationTime - 1) is a multiple of 4)
F = (2 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime - ClkActivationTime - 2) is a multiple of 4)
F = (3 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime - ClkActivationTime - 3) is a multiple of 4)

(7) For ADV falling edge (ADV activated):
Case GpmcFCLKDivider = 0 :
G = 0.5 * ADVExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise


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Case GpmcFCLKDivider = 2:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)
For ADV rising edge (ADV deactivated) in Reading mode:
Case GpmcFCLKDivider = 0:
G = 0.5 * ADVExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime) is a multiple of 4)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 4)
G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 4)
G = (3 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 3) is a multiple of 4)
For ADV rising edge (ADV deactivated) in Writing mode:
Case GpmcFCLKDivider = 0:
G = 0.5 * ADVExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime) is a multiple of 4)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 4)
G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 4)
G = (3 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 3) is a multiple of 4)

(8) For OE falling edge (OE activated):
Case GpmcFCLKDivider = 0:
- H = 0.5 * OEExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOnTime – ClkActivationTime) is a multiple of 3)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
- H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOnTime - ClkActivationTime) is a multiple of 4)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime - ClkActivationTime - 1) is a multiple of 4)
- H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime - ClkActivationTime - 2) is a multiple of 4)
- H = (3 + 0.5 * OEExtraDelay)) * GPMC_FCLK if ((OEOnTime - ClkActivationTime - 3) is a multiple of 4)
For OE rising edge (OE deactivated):
Case GpmcFCLKDivider = 0:
- H = 0.5 * OEExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOffTime – ClkActivationTime) is a multiple of 3)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
- H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOffTime – ClkActivationTime) is a multiple of 4)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 1) is a multiple of 4)
- H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 2) is a multiple of 4)
- H = (3 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 3) is a multiple of 4)

(9) For WE falling edge (WE activated):
Case GpmcFCLKDivider = 0:
- I = 0.5 * WEExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)

- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOnTime – ClkActivationTime) is a multiple of 3)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 1) is a multiple of 3)
- I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOnTime - ClkActivationTime) is a multiple of 4)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime - ClkActivationTime - 1) is a multiple of 4)
- I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime - ClkActivationTime - 2) is a multiple of 4)
- I = (3 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime - ClkActivationTime - 3) is a multiple of 4)
For WE rising edge (WE deactivated):
Case GpmcFCLKDivider = 0:
- I = 0.5 * WEExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOffTime – ClkActivationTime) is a multiple of 3)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 1) is a multiple of 3)
- I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOffTime - ClkActivationTime) is a multiple of 4)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime - ClkActivationTime - 1) is a multiple of 4)
- I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime - ClkActivationTime - 2) is a multiple of 4)
- I = (3 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime - ClkActivationTime - 3) is a multiple of 4)

(10) J = GPMC_FCLK period, where GPMC_FCLK is the General Purpose Memory Controller internal functional clock

(11) For read:
K = (ADVRdOffTime – ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For write: K = (ADVWrOffTime – ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(12) The gpmc_clk output clock maximum and minimum frequency is programmable in the I/F module by setting the GPMC_CONFIG1_CSx configuration register bit fields GpmcFCLKDivider

(13) gpio6_16 programmed to MUXMODE=9 (clkout1), CM_CLKSEL_CLKOUTMUX1 programmed to 7 (CORE_DPLL_OUT_DCLK), CM_CLKSEL_CORE_DPLL_OUT_CLK_CLKOUTMUX programmed to 1.

(14) CSEXTRADELAY = 0, ADVEXTRADELAY = 0, WEEXTRADELAY = 0, OEEXTRADELAY = 0. Extra half-GPMC_FCLK cycle delay mode is not timed.


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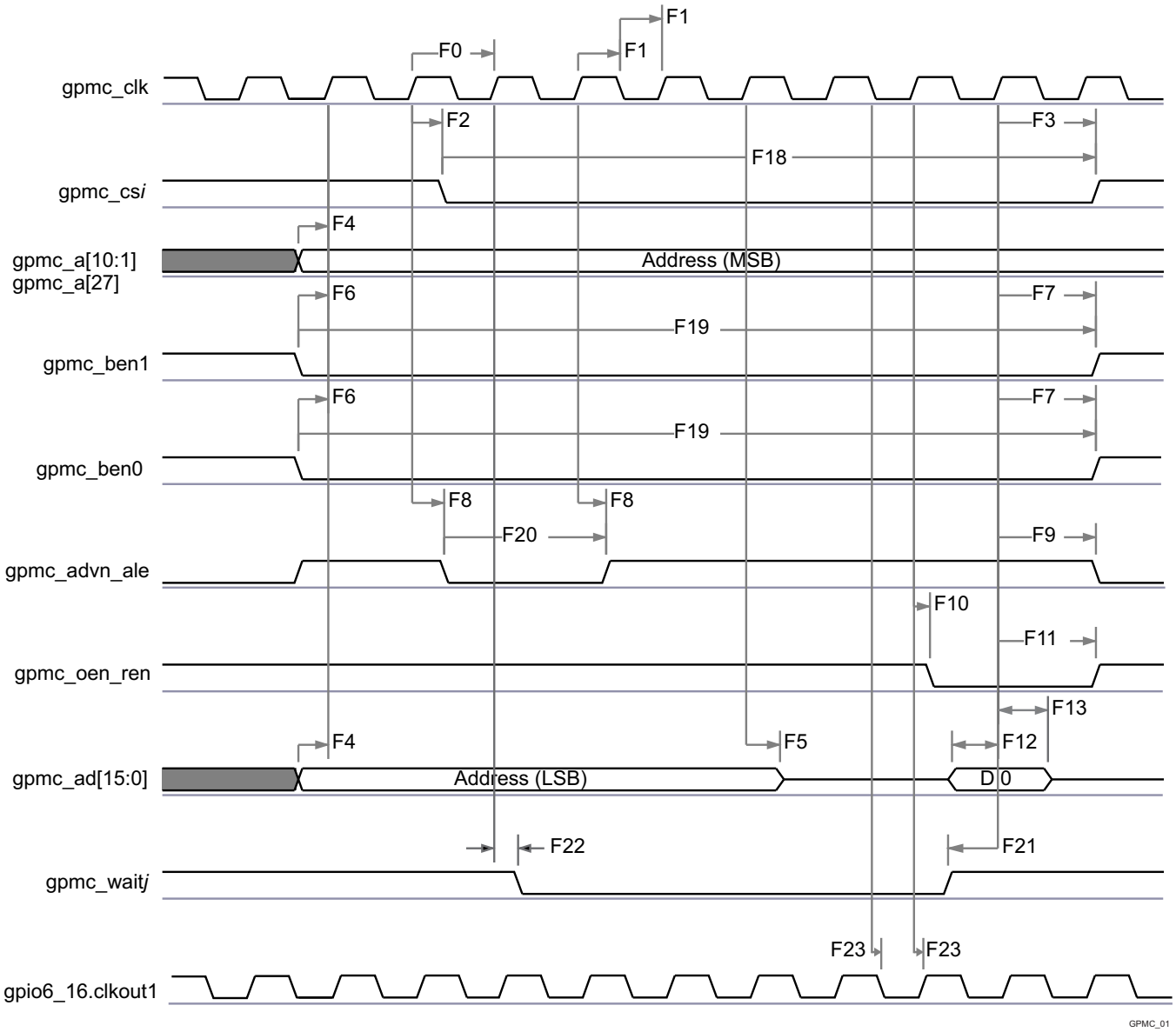


**Figure 7-7. GPMC / Multiplexed 16bits NOR Flash - Synchronous Single Read - (GpmcFCLKDivider = 0)[(1)(2)]**

(1) In gpmc_cs*i*, i = 0 to 7.

(2) In gpmc_waitj, j = 0 to 1.

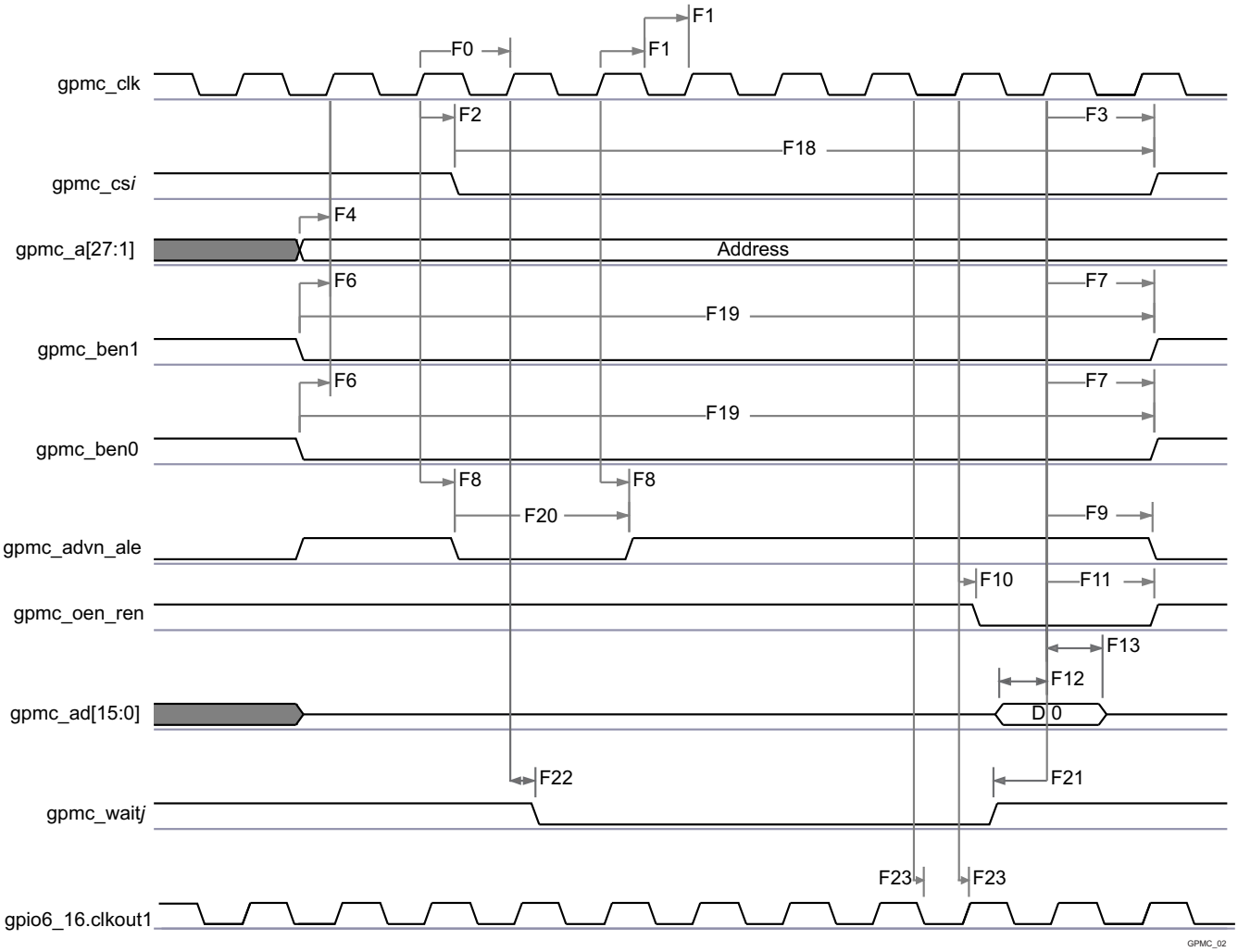


**Figure 7-8. GPMC / Nonmultiplexed 16bits NOR Flash - Synchronous Single Read - (GpmcFCLKDivider = 0)[(1)(2)]**

(1) In gpmc_cs*i*, i = 0 to 7.

(2) In gpmc_waitj, j = 0 to 1.


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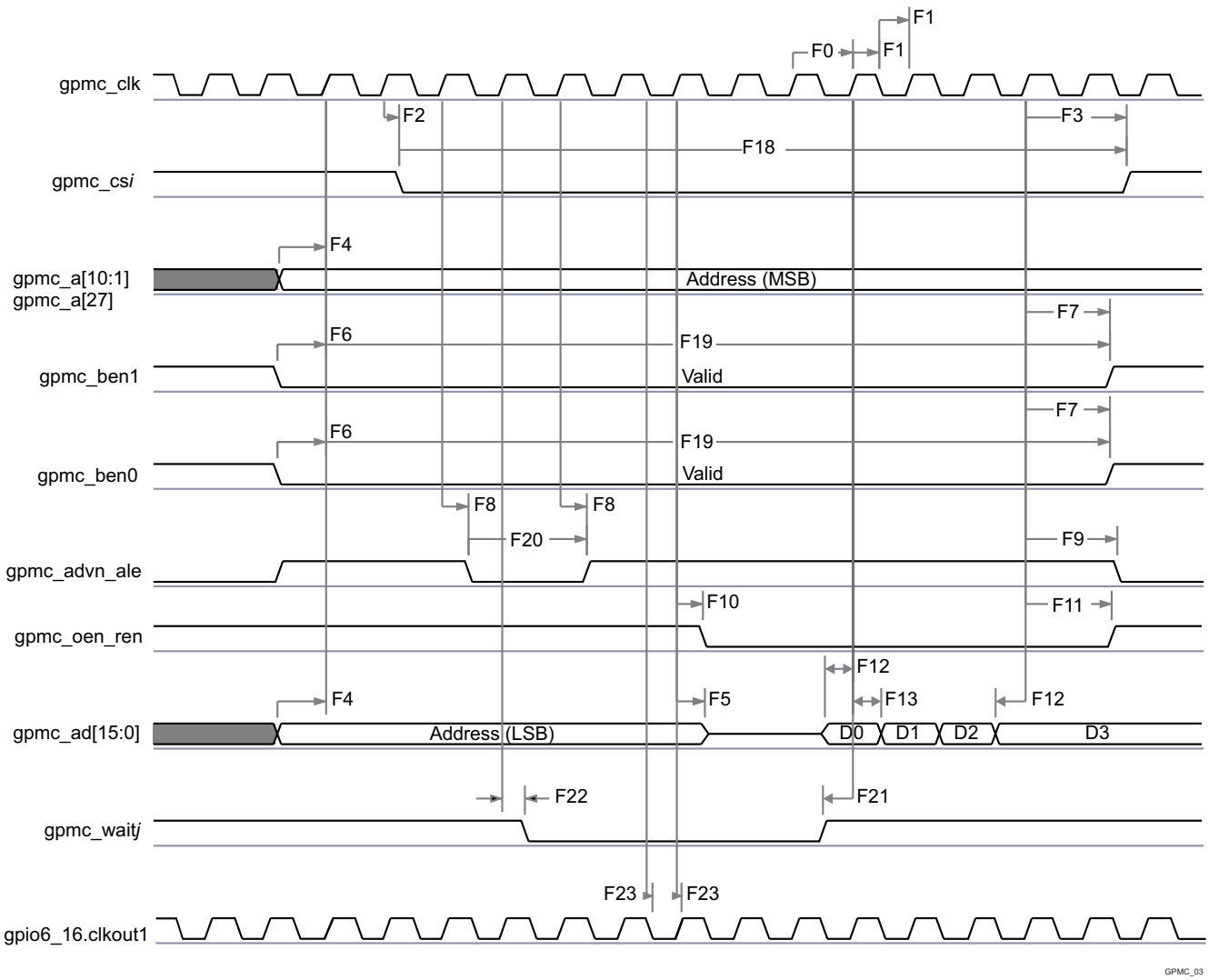


**Figure 7-9. GPMC / Multiplexed 16bits NOR Flash - Synchronous Burst Read 4x16 bits - (GpmcFCLKDivider = 0)[(1)(2)]**

(1) In gpmc_cs*i*, i= 0 to 7.

(2) In gpmc_waitj, j = 0 to 1.

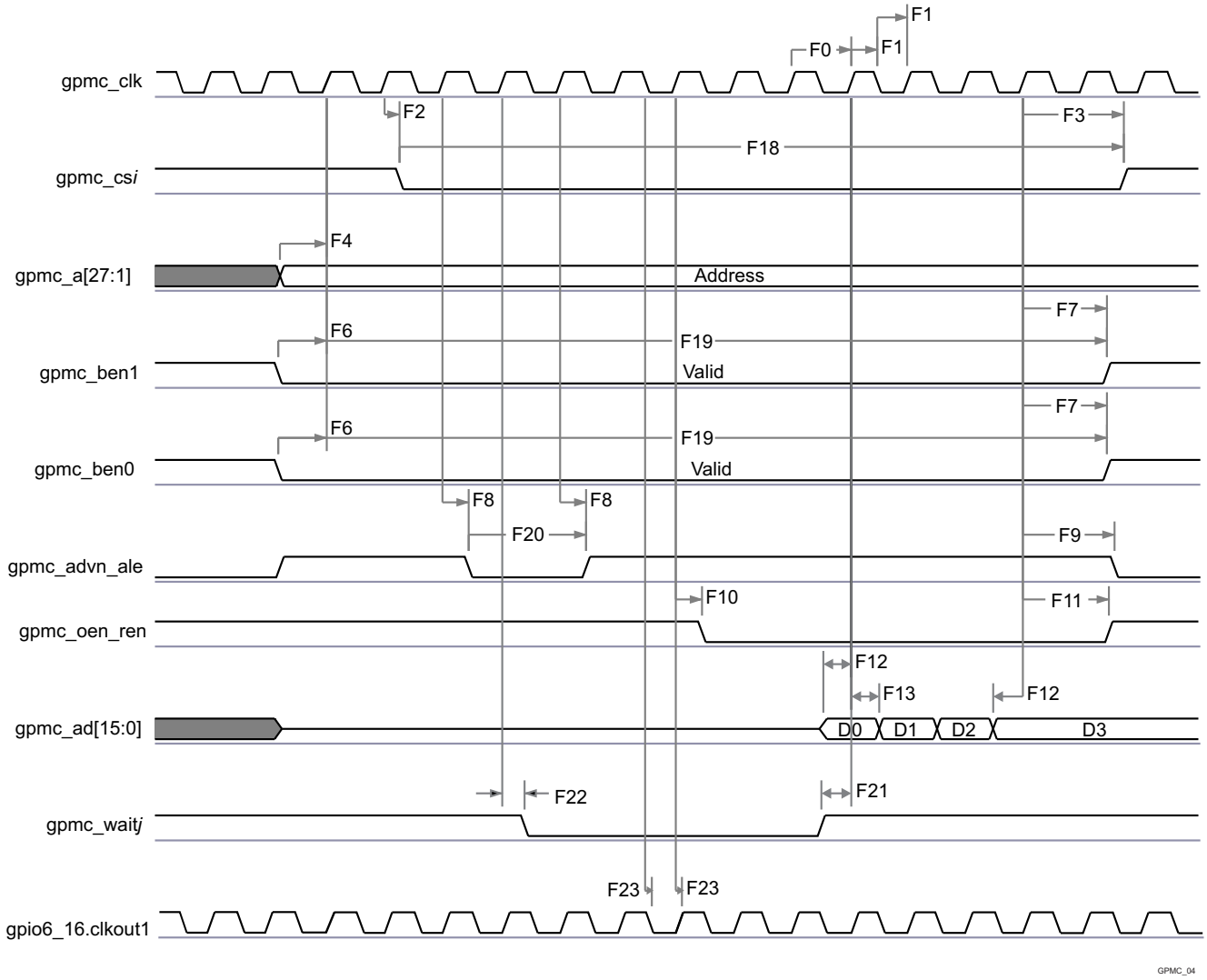


**Figure 7-10. GPMC / Nonmultiplexed 16bits NOR Flash - Synchronous Burst Read 4x16 bits - (GpmcFCLKDivider = 0)[(1)(2)]**

(1) In gpmc_cs*i*, i = 0 to 7.

(2) In gpmc_waitj, j = 0 to 1.


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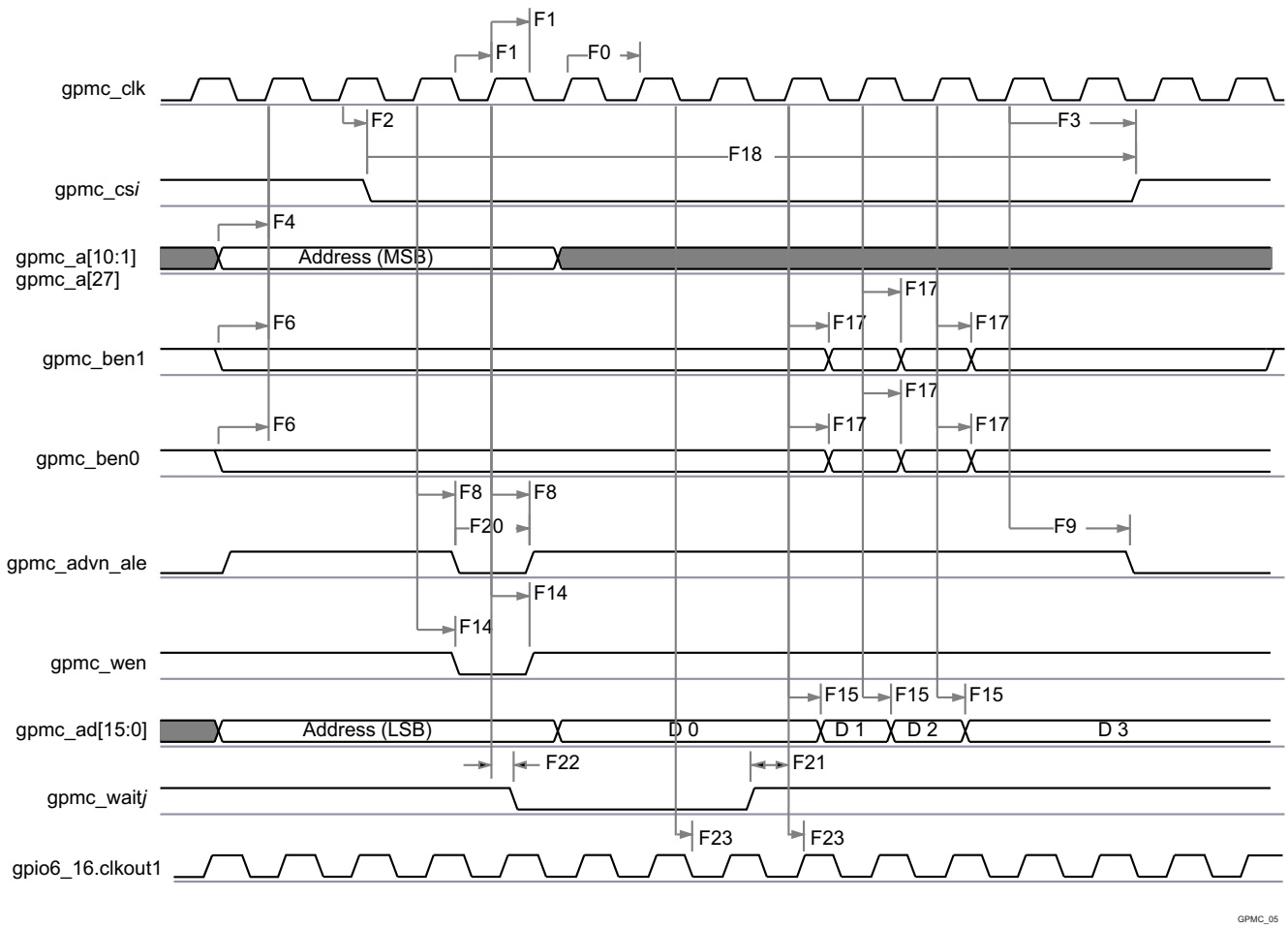


**Figure 7-11. GPMC / Multiplexed 16bits NOR Flash - Synchronous Burst Write 4x16bits - (GpmcFCLKDivider = 0)[(1)(2)]**

(1) In gpmc_cs*i*, i = 0 to 7.

(2) In gpmc_waitj, j = 0 to 1.

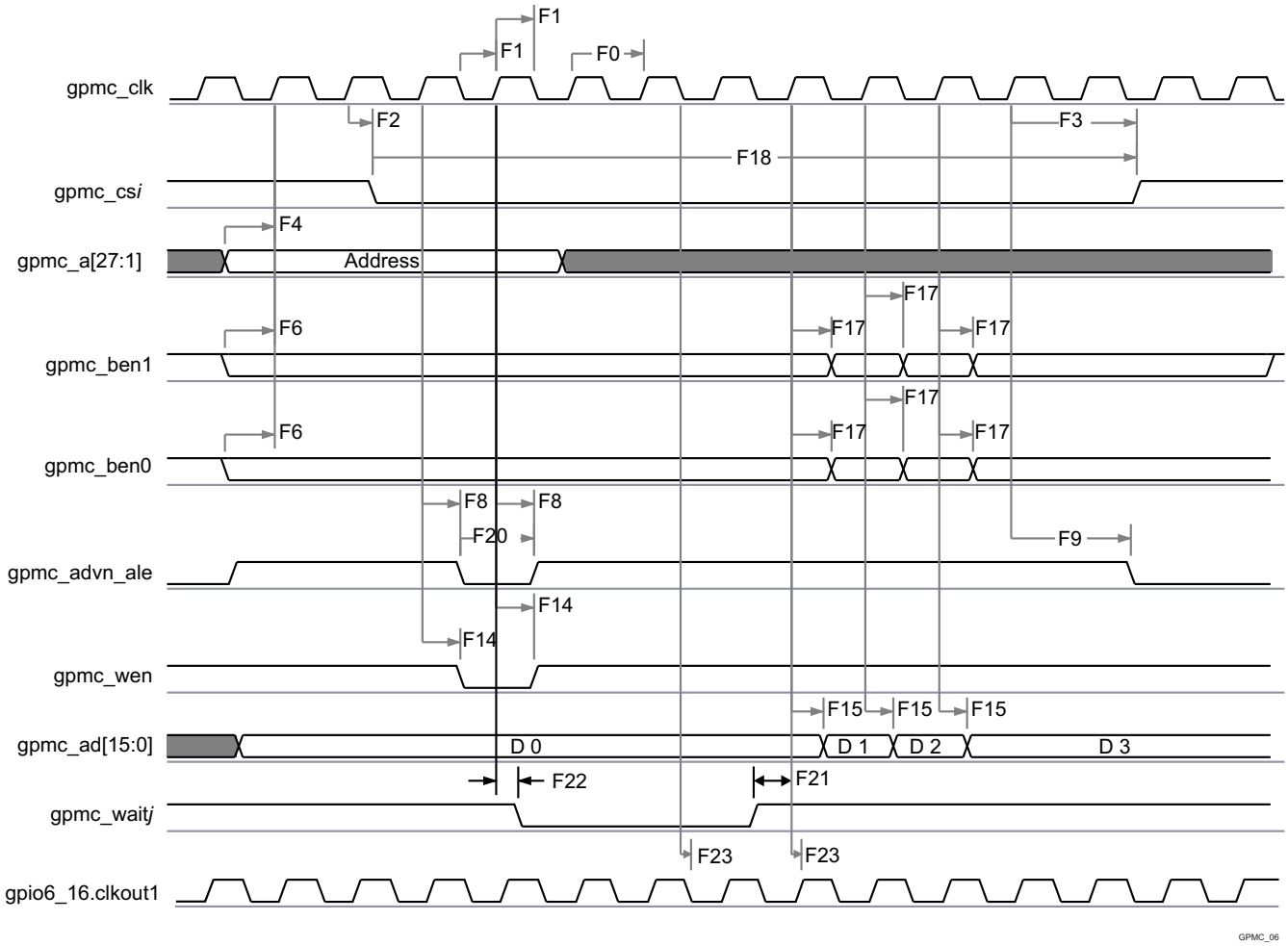


**Figure 7-12. GPMC / Nonmultiplexed 16bits NOR Flash - Synchronous Burst Write 4x16bits - (GpmcFCLKDivider = 0)[(1)(2)]**

(1) In gpmc_cs*i*, i = 1 to 7.

(2) In gpmc_waitj, j = 0 to 1.

### *7.10.2 GPMC/NOR Flash Interface Asynchronous Timing*

**CAUTION**

The IO Timings provided in this section are only valid for some GPMC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-29 and Table 7-30 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 7-13, Figure 7-14, Figure 7-15, Figure 7-16, Figure 7-17, and Figure 7-18).

**Table 7-29. GPMC/NOR Flash Interface Timing Requirements - Asynchronous Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| FA5 | $t_{acc(DAT)}$ | Data Maximum Access Time (GPMC_FCLK cycles) | | H [(1)] | cycles |


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### Table 7-29. GPMC/NOR Flash Interface Timing Requirements - Asynchronous Mode (continued)

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| FA20 | $t_{acc1\text{-}pgmode(DAT)}$ | Page Mode Successive Data Maximum Access Time (GPMC_FCLK cycles) | | P (2) | cycles |
| FA21 | $t_{acc2\text{-}pgmode(DAT)}$ | Page Mode First Data Maximum Access Time (GPMC_FCLK cycles) | | H (1) | cycles |
| - | $t_{su(DV\text{-}OEH)}$ | Setup time, read gpmc_ad[15:0] valid before gpmc_oen_ren high | 1.9 | | ns |
| - | $t_{h(OEH\text{-}DV)}$ | Hold time, read gpmc_ad[15:0] valid after gpmc_oen_ren high | 1 | | ns |

(1) H = Access Time * (TimeParaGranularity + 1)

(2) P = PageBurstAccessTime * (TimeParaGranularity + 1)

### Table 7-30. GPMC/NOR Flash Interface Switching Characteristics - Asynchronous Mode

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| - | $t_{r(DO)}$ | Rising time, gpmc_ad[15:0] output data | 0.447 | 4.067 | ns |
| - | $t_{f(DO)}$ | Fallling time, gpmc_ad[15:0] output data | 0.43 | 4.463 | ns |
| FA0 | $t_{w(nBEV)}$ | Pulse duration, gpmc_ben[1:0] valid time | | N (1) | ns |
| FA1 | $t_{w(nCSV)}$ | Pulse duration, gpmc_cs[7:0] low | | A (2) | ns |
| FA3 | $t_{d(nCSV\text{-}nADVIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_advn_ale invalid | B - 2 (3) | B + 4 (3) | ns |
| FA4 | $t_{d(nCSV\text{-}nOEIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren invalid (Single read) | C - 2 (4) | C + 4 (4) | ns |
| FA9 | $t_{d(AV\text{-}nCSV)}$ | Delay time, address bus valid to gpmc_cs[7:0] valid | J - 2 (5) | J + 4 (5) | ns |
| FA10 | $t_{d(nBEV\text{-}nCSV)}$ | Delay time, gpmc_ben[1:0] valid to gpmc_cs[7:0] valid | J - 2 (5) | J + 4 (5) | ns |
| FA12 | $t_{d(nCSV\text{-}nADVV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_advn_ale valid | K - 2 (6) | K + 4 (6) | ns |
| FA13 | $t_{d(nCSV\text{-}nOEV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren valid | L - 2 (7) | L + 4 (7) | ns |
| FA16 | $t_{w(AIV)}$ | Pulse duration, address invalid between 2 successive R/W accesses | G (8) | | ns |
| FA18 | $t_{d(nCSV\text{-}nOEIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren invalid (Burst read) | I - 2 (9) | I + 4 (9) | ns |
| FA20 | $t_{w(AV)}$ | Pulse duration, address valid : 2nd, 3rd and 4th accesses | D (10) | | ns |
| FA25 | $t_{d(nCSV\text{-}nWEV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_wen valid | E - 2 (11) | E + 4 (11) | ns |
| FA27 | $t_{d(nCSV\text{-}nWEIV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_wen invalid | F - 2 (12) | F + 4 (12) | ns |
| FA28 | $t_{d(nWEV\text{-}DV)}$ | Delay time, gpmc_ wen valid to data bus valid | | 2 | ns |
| FA29 | $t_{d(DV\text{-}nCSV)}$ | Delay time, data bus valid to gpmc_cs[7:0] valid | J - 2 (5) | J + 4 (5) | ns |
| FA37 | $t_{d(nOEV\text{-}AIV)}$ | Delay time, gpmc_oen_ren valid to gpmc_ad[15:0] multiplexed address bus phase end | | 2 | ns |

(1) For single read: N = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: N = WrCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: N = (RdCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: N = (WrCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(2) For single read: A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: A = (CSWrOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(3) For reading: B = ((ADVRdOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK
For writing: B = ((ADVWrOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK

(4) C = ((OEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK

(5) J = (CSOnTime * (TimeParaGranularity + 1) + 0.5 * CSExtraDelay) * GPMC_FCLK

(6) K = ((ADVOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK

(7) L = ((OEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK

(8) G = Cycle2CycleDelay * GPMC_FCLK * (TimeParaGranularity +1)

(9) I = ((OEOffTime + (n - 1) * PageBurstAccessTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK

(10) D = PageBurstAccessTime * (TimeParaGranularity + 1) * GPMC_FCLK

(11) E = ((WEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK

(12) F = ((WEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK

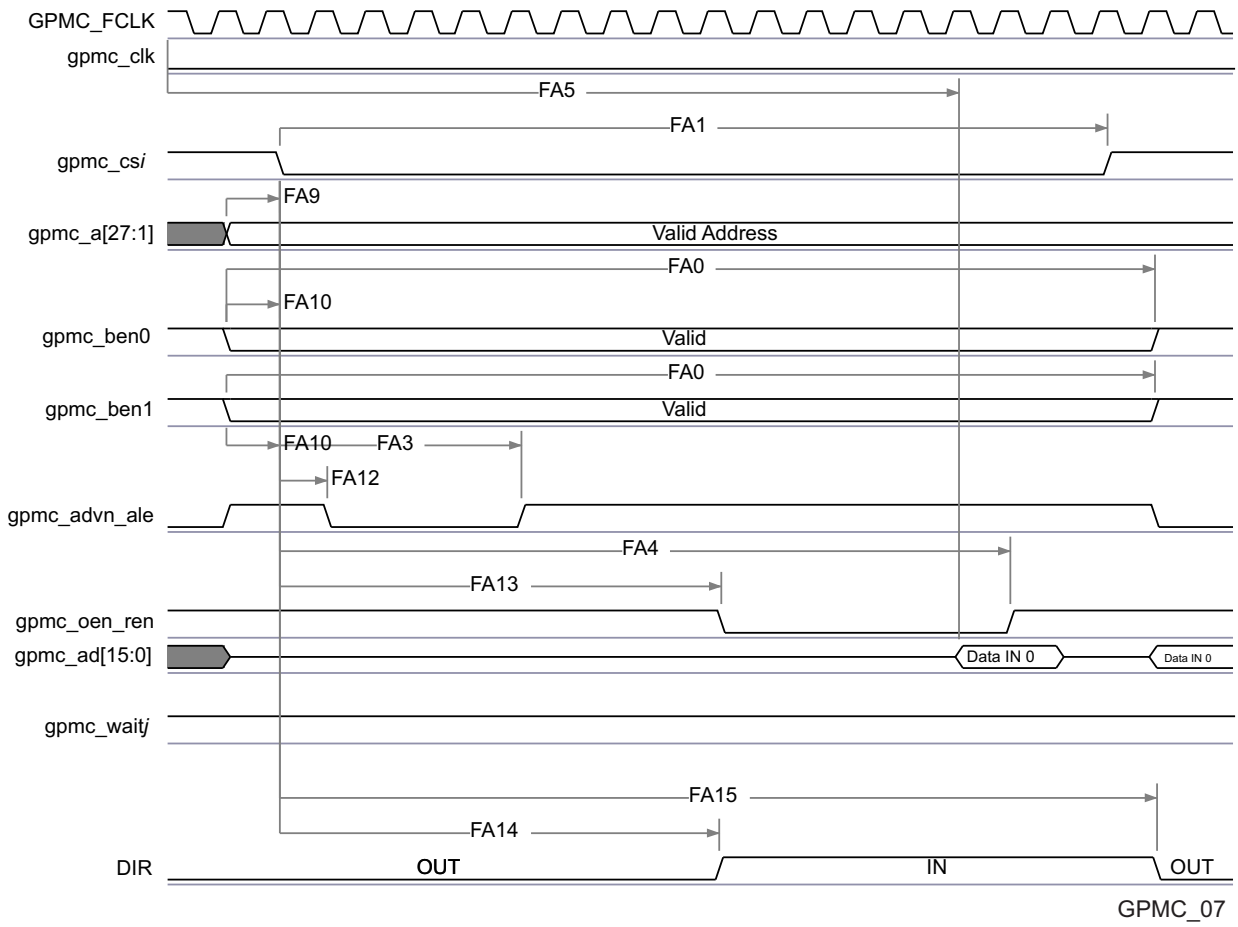


**Figure 7-13. GPMC / NOR Flash - Asynchronous Read - Single Word Timing[(1)(2)(3)]**

(1) In gpmc_cs*i*, i = 0 to 7. In gpmc_waitj, j = 0 to 1.

(2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.


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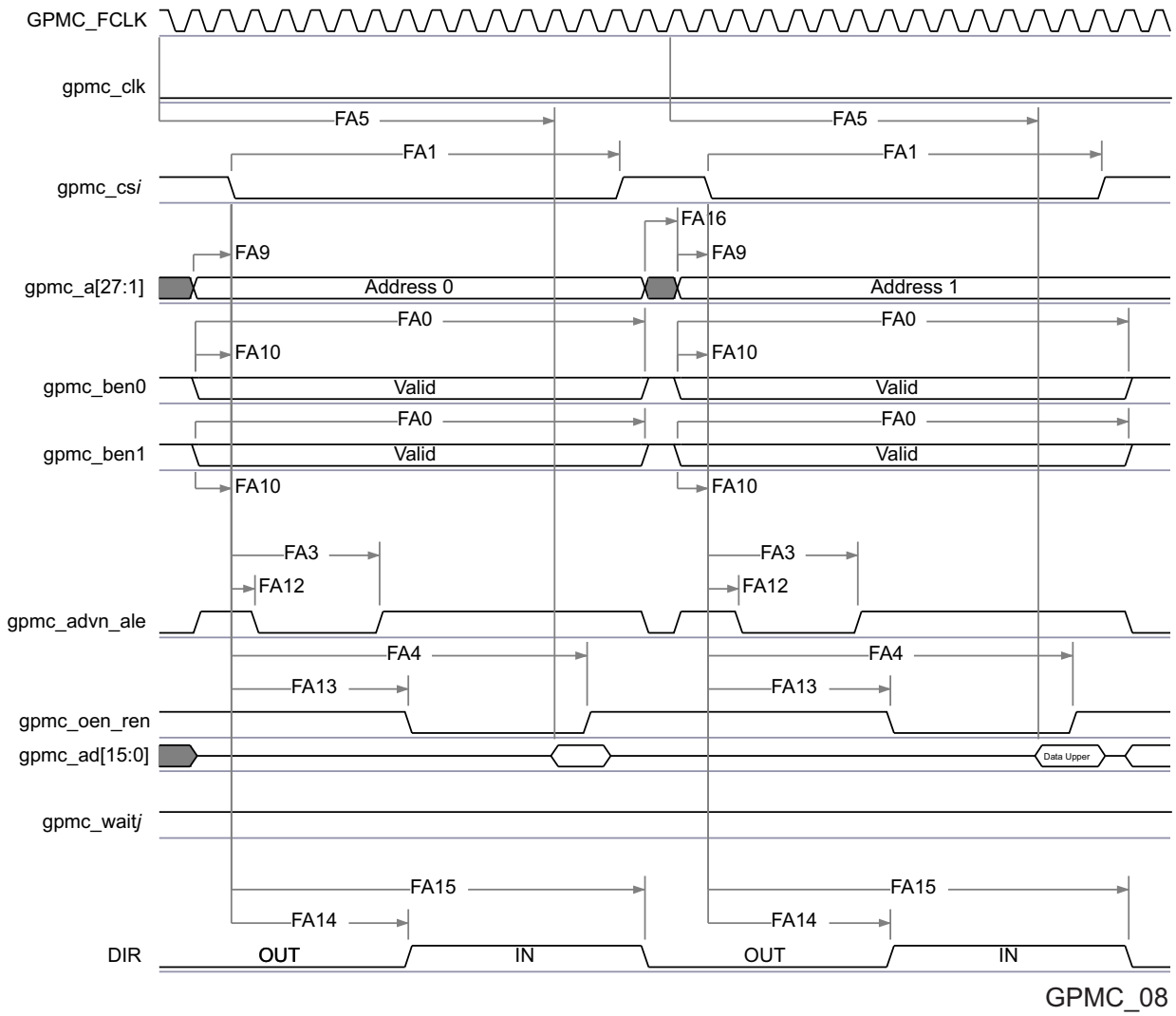


**Figure 7-14. GPMC / NOR Flash - Asynchronous Read - 32-bit Timing[(1)(2)(3)]**

(1) In gpmc_cs*i*, i = 0 to 7. In gpmc_waitj, j = 0 to 1.

(2) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value should be stored inside AccessTime register bits field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

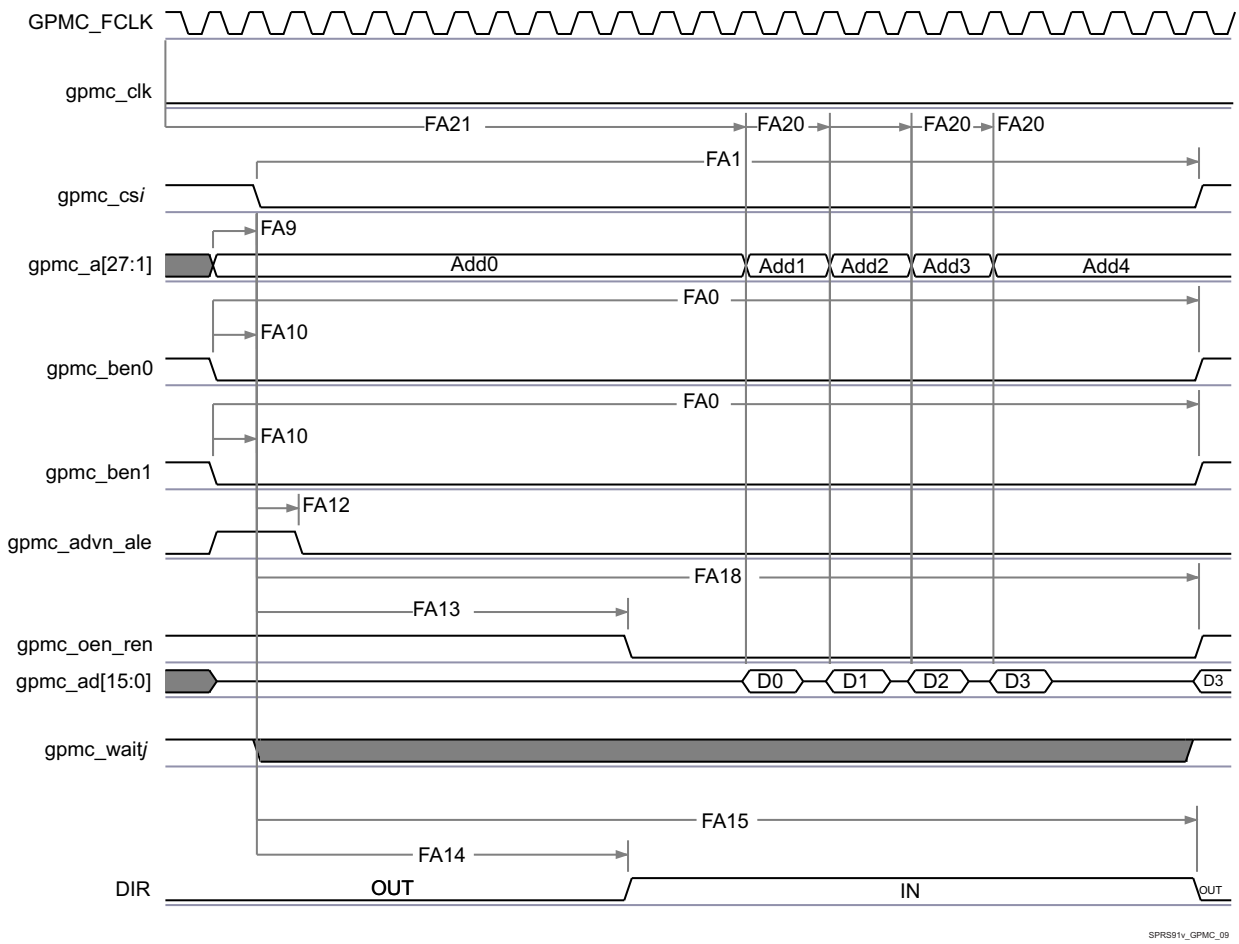


**Figure 7-15. GPMC / NOR Flash - Asynchronous Read - Page Mode 4x16-bit Timing[(1)(2)(3)(4)]**

(1) In gpmc_cs*i*, i = 0 to 7. In gpmc_waitj, j = 0 to 1.

(2) FA21 parameter illustrates amount of time required to internally sample first input Page Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, First input Page Data will be internally sampled by active functional clock edge. FA21 calculation is detailled in a separated application note and should be stored inside AccessTime register bits field.

(3) FA20 parameter illustrates amount of time required to internally sample successive input Page Data. It is expressed in number of GPMC functional clock cycles. After each access to input Page Data, next input Page Data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input Page Data (excluding first input Page Data). FA20 value should be stored in PageBurstAccessTime register bits field.

(4) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(5) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.


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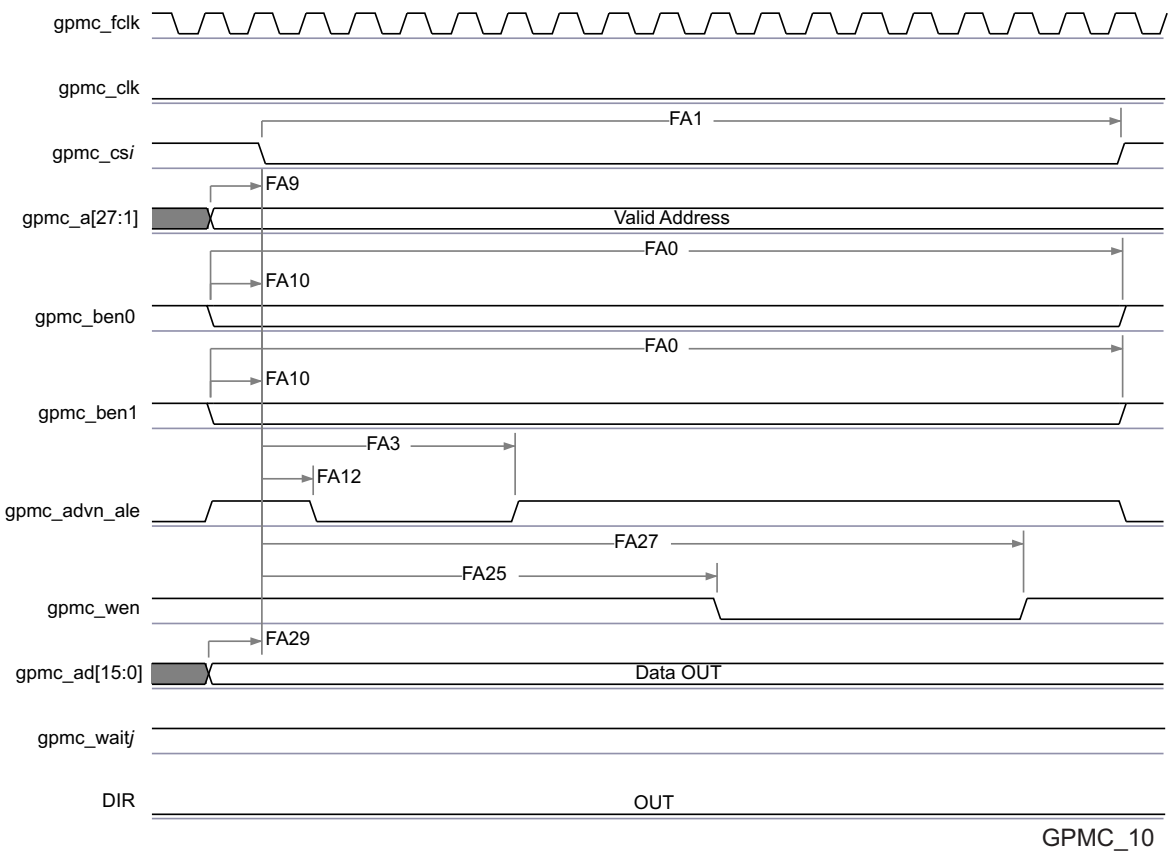


**Figure 7-16. GPMC / NOR Flash - Asynchronous Write - Single Word Timing[(1)]**

(1) In gpmc_cs*i*, i = 0 to 7. In gpmc_waitj, j = 0 to 1.

(2) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

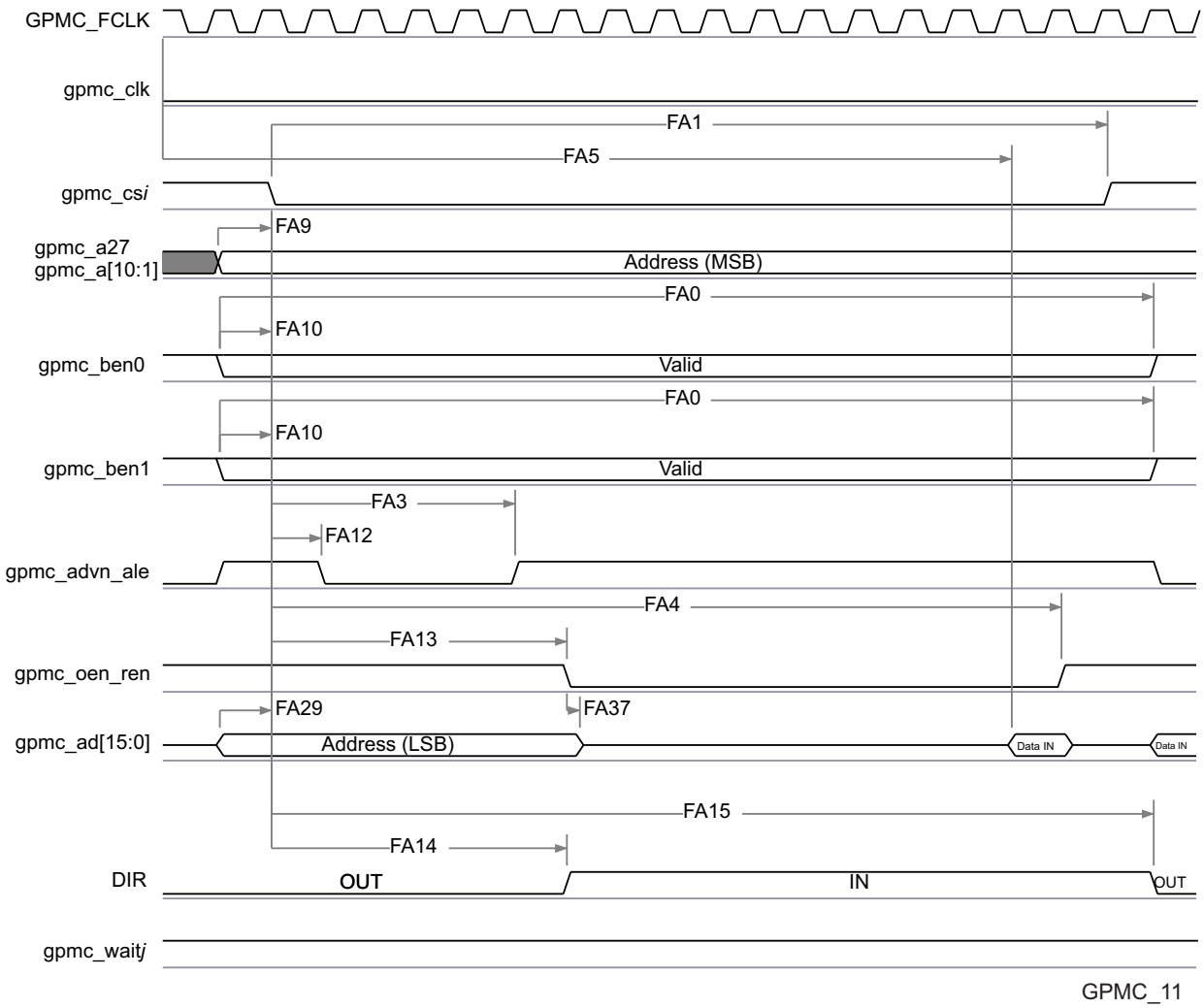


**Figure 7-17. GPMC / Multiplexed NOR Flash - Asynchronous Read - Single Word Timing[(1)(2)(3)]**

(1) In gpmc_cs*i*, i = 0 to 7. In gpmc_wait*j*, j = 0 to 1

(2) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value should be stored inside AccessTime register bits field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally

(4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.


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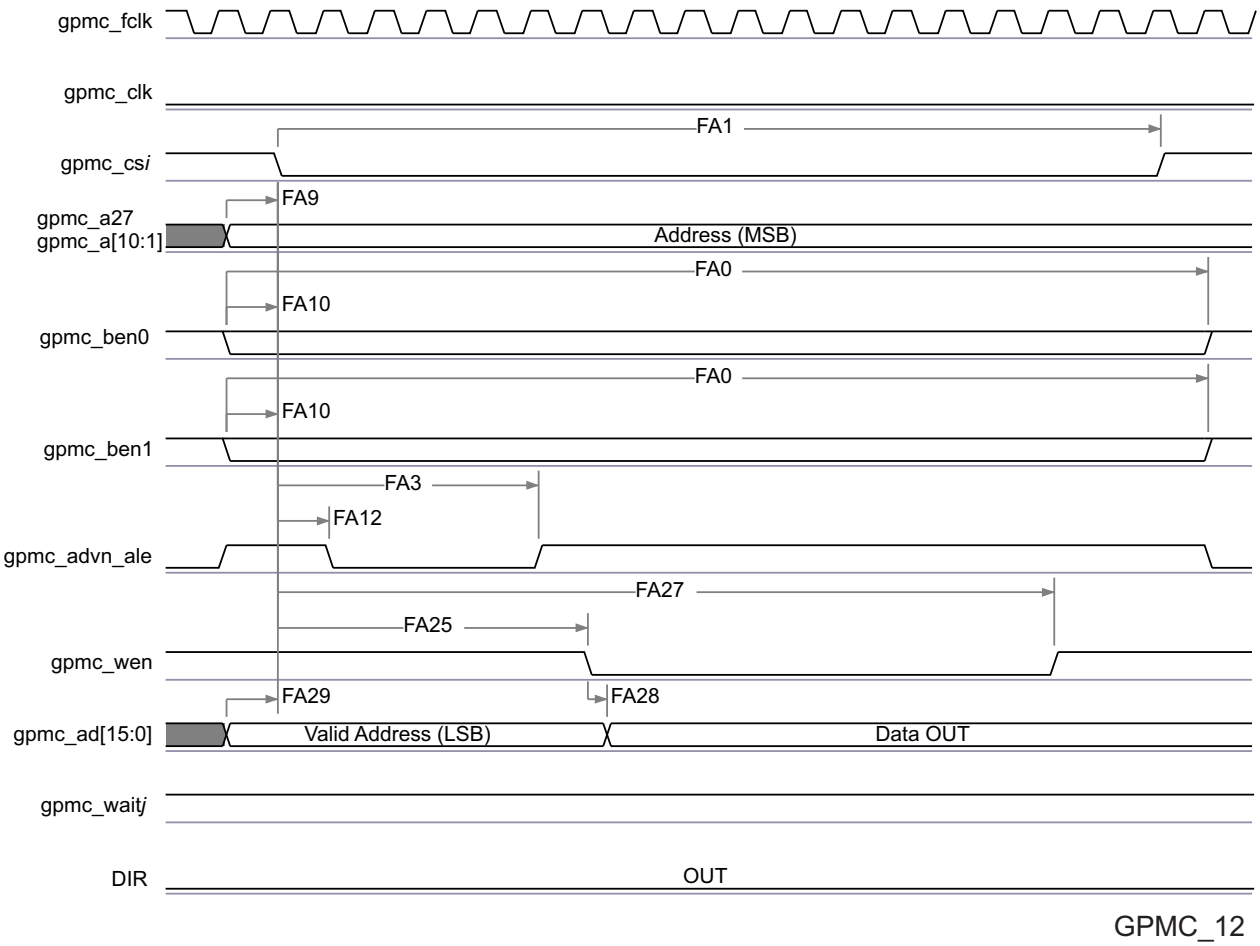


**Figure 7-18. GPMC / Multiplexed NOR Flash - Asynchronous Write - Single Word Timing[(1)]**

(1) In gpmc_cs*i*, i = 0 to 7. In gpmc_waitj, j = 0 to 1.

(2) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

### *7.10.3 GPMC/NAND Flash Interface Asynchronous Timing*

**CAUTION**

The IO Timings provided in this section are only valid for some GPMC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-31 and Table 7-32 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 7-19, Figure 7-20, Figure 7-21, and Figure 7-22).

**Table 7-31. GPMC/NAND Flash Interface Timing Requirements**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| GNF12 | $t_{acc(DAT)}$ | Data maximum access time (GPMC_FCLK Cycles) | | J [(1)] | cycles |
| - | $t_{su(DV-OEH)}$ | Setup time, read gpmc_ad[15:0] valid before gpmc_oen_ren high | 1.9 | | ns |
| - | $t_{h(OEH-DV)}$ | Hold time, read gpmc_ad[15:0] valid after gpmc_oen_ren high | 1 | | ns |

(1) J = AccessTime * (TimeParaGranularity + 1)

### Table 7-32. GPMC/NAND Flash Interface Switching Characteristics

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| - | $t_{r(DO)}$ | Rising time, gpmc_ad[15:0] output data | 0.447 | 4.067 | ns |
| - | $t_{f(DO)}$ | Fallling time, gpmc_ad[15:0] output data | 0.43 | 4.463 | ns |
| GNF0 | $t_{w(nWEV)}$ | Pulse duration, gpmc_wen valid time | | A (1) | ns |
| GNF1 | $t_{d(nCSV-nWEV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_wen valid | B - 2 (2) | B + 4 (2) | ns |
| GNF2 | $t_{d(CLEH-nWEV)}$ | Delay time, gpmc_ben[1:0] high to gpmc_wen valid | C - 2 (3) | C + 4 (3) | ns |
| GNF3 | $t_{d(nWEV-DV)}$ | Delay time, gpmc_ad[15:0] valid to gpmc_wen valid | D - 2 (4) | D + 4 (4) | ns |
| GNF4 | $t_{d(nWEIV-DIV)}$ | Delay time, gpmc_wen invalid to gpmc_ad[15:0] invalid | E - 2 (5) | E + 4 (5) | ns |
| GNF5 | $t_{d(nWEIV-CLEIV)}$ | Delay time, gpmc_wen invalid to gpmc_ben[1:0] invalid | F - 2 (6) | F + 4 (6) | ns |
| GNF6 | $t_{d(nWEIV-nCSIV)}$ | Delay time, gpmc_wen invalid to gpmc_cs[7:0] invalid | G - 2 (7) | G + 4 (7) | ns |
| GNF7 | $t_{d(ALEH-nWEV)}$ | Delay time, gpmc_advn_ale high to gpmc_wen valid | C - 2 (3) | C + 4 (3) | ns |
| GNF8 | $t_{d(nWEIV-ALEIV)}$ | Delay time, gpmc_wen invalid to gpmc_advn_ale invalid | F - 2 (6) | F + 4 (6) | ns |
| GNF9 | $t_{c(nWE)}$ | Cycle time, write cycle time | | H (8) | ns |
| GNF10 | $t_{d(nCSV-nOEV)}$ | Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren valid | I - 2 (9) | I + 4 (9) | ns |
| GNF13 | $t_{w(nOEV)}$ | Pulse duration, gpmc_oen_ren valid time | | K (10) | ns |
| GNF14 | $t_{c(nOE)}$ | Cycle time, read cycle time | | L (11) | ns |
| GNF15 | $t_{d(nOEIV-nCSIV)}$ | Delay time, gpmc_oen_ren invalid to gpmc_cs[7:0] invalid | M - 2 (12) | M + 4 (12) | ns |

(1) A = (WEOffTime – WEOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(2) B = ((WEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK
(3) C = ((WEOnTime – ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – ADVExtraDelay)) * GPMC_FCLK
(4) D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEExtraDelay ) * GPMC_FCLK
(5) E = (WrCycleTime – WEOffTime * (TimeParaGranularity + 1) – 0.5 * WEExtraDelay ) * GPMC_FCLK
(6) F = (ADVWrOffTime – WEOffTime * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – WEExtraDelay) * GPMC_FCLK
(7) G = (CSWrOffTime – WEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay – WEExtraDelay) * GPMC_FCLK
(8) H = WrCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK
(9) I = ((OEOffTime + (n – 1) * PageBurstAccessTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK
(10) K = (OEOffTime – OEOnTime) * (1 + TimeParaGranularity) * GPMC_FCLK
(11) L = RdCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK
(12) M = (CSRdOffTime – OEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay – OEExtraDelay) * GPMC_FCLK


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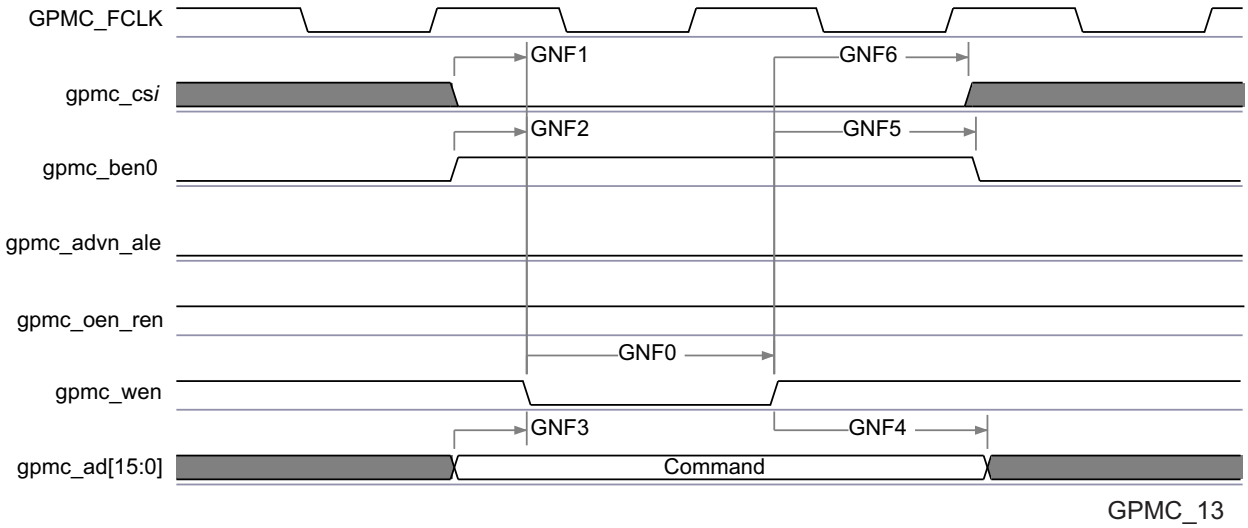


**Figure 7-19. GPMC / NAND Flash - Command Latch Cycle Timing[(1)]**

(1) In gpmc_cs*i*, i = 0 to 7.

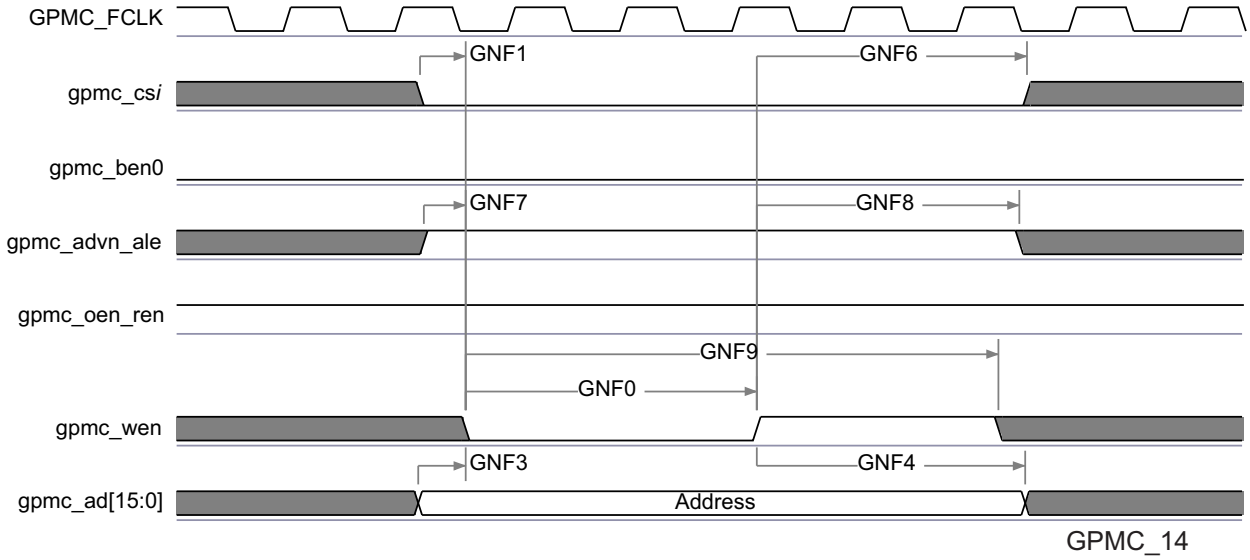


**Figure 7-20. GPMC / NAND Flash - Address Latch Cycle Timing[(1)]**

(1) In gpmc_cs*i*, i = 0 to 7.

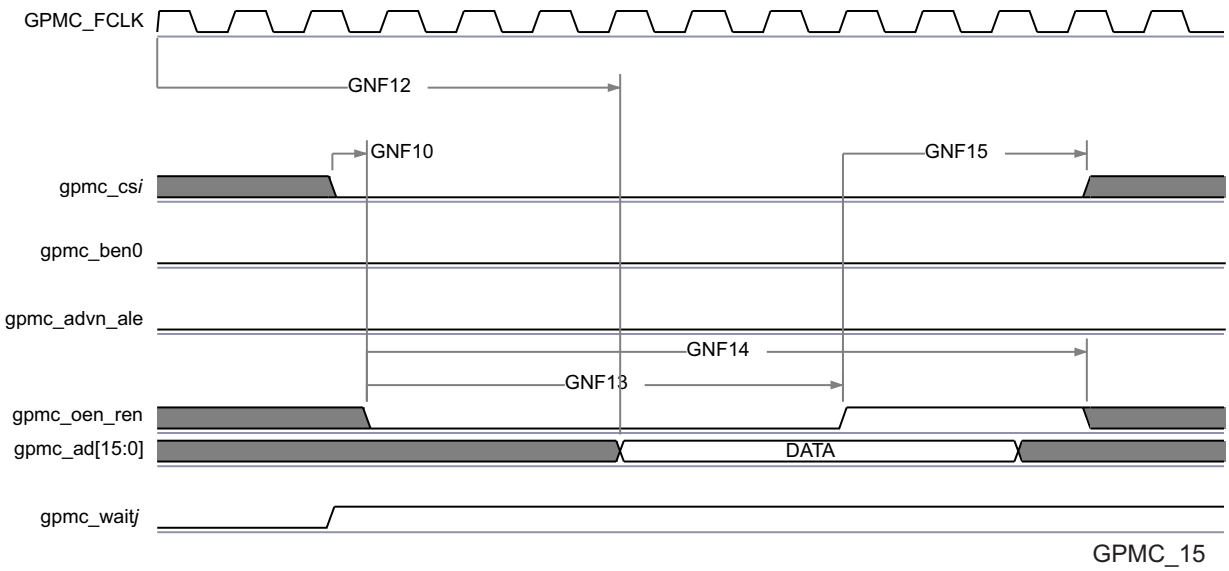


**Figure 7-21. GPMC / NAND Flash - Data Read Cycle Timing[(1)(2)(3)]**

(1) GNF12 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.

(2) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(3) In gpmc_cs*i*, i = 0 to 7. In gpmc_waitj, j = 0 to 1.

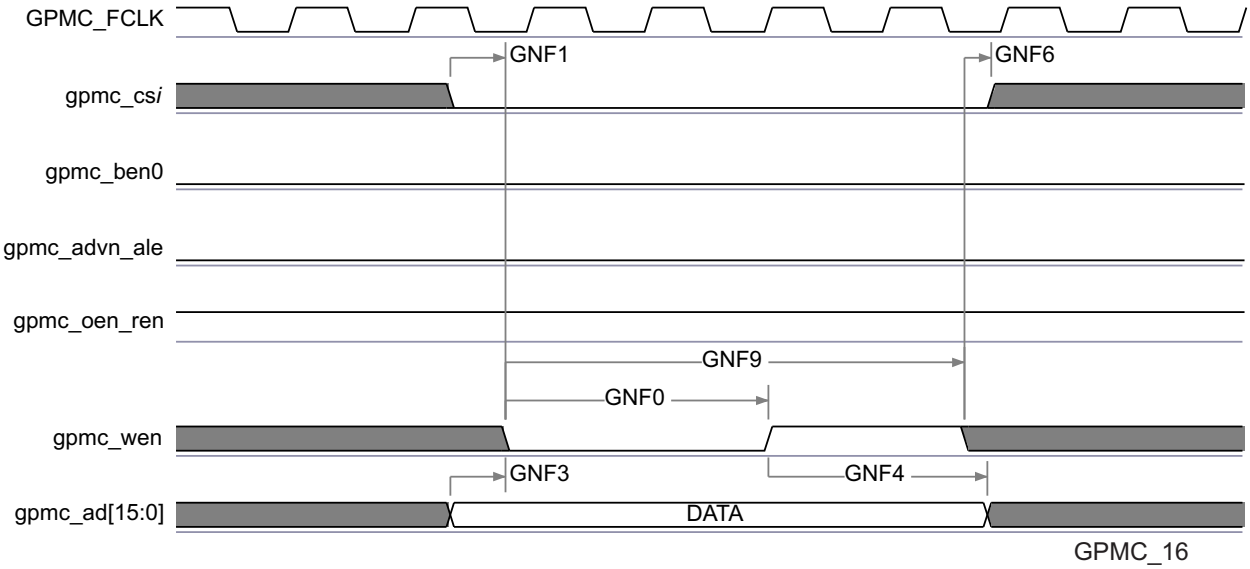


**Figure 7-22. GPMC / NAND Flash - Data Write Cycle Timing[(1)]**

(1) In gpmc_cs*i*, i = 0 to 7.

---

**NOTE**

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented in Table 4-3 and described in Device TRM, *Chapter 18 - Control Module*.

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Virtual IO Timings Modes must be used to ensure some IO timings for GPMC. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 7-33 *Virtual Functions Mapping for GPMC* for a definition of the Virtual modes.

Table 7-33 presents the values for DELAYMODE bitfield.

**Table 7-33. Virtual Functions Mapping for GPMC**

| BALL NUMBER | BALL NAME | Delay Mode Value | MUXMODE[15:0] | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | GPMC_VIRTUAL 1 | 0 | 1 | 2 | 3 | 5 | 6 |
| M6 | gpmc_ad0 | 11 | gpmc_ad0 | | | | | |
| M2 | gpmc_ad1 | 11 | gpmc_ad1 | | | | | |
| L5 | gpmc_ad2 | 11 | gpmc_ad2 | | | | | |
| M1 | gpmc_ad3 | 11 | gpmc_ad3 | | | | | |
| L6 | gpmc_ad4 | 11 | gpmc_ad4 | | | | | |
| L4 | gpmc_ad5 | 11 | gpmc_ad5 | | | | | |
| L3 | gpmc_ad6 | 11 | gpmc_ad6 | | | | | |
| L2 | gpmc_ad7 | 11 | gpmc_ad7 | | | | | |
| L1 | gpmc_ad8 | 11 | gpmc_ad8 | | | | | |
| K2 | gpmc_ad9 | 11 | gpmc_ad9 | | | | | |
| J1 | gpmc_ad10 | 11 | gpmc_ad10 | | | | | |
| J2 | gpmc_ad11 | 11 | gpmc_ad11 | | | | | |
| H1 | gpmc_ad12 | 11 | gpmc_ad12 | | | | | |
| J3 | gpmc_ad13 | 11 | gpmc_ad13 | | | | | |
| H2 | gpmc_ad14 | 11 | gpmc_ad14 | | | | | |
| H3 | gpmc_ad15 | 11 | gpmc_ad15 | | | | | |
| R6 | gpmc_a0 | 11 | gpmc_a0 | | | | | |
| T9 | gpmc_a1 | 11 | gpmc_a1 | | | | | |
| T6 | gpmc_a2 | 11 | gpmc_a2 | | | | | |
| T7 | gpmc_a3 | 10 | gpmc_a3 | | | | | |
| P6 | gpmc_a4 | 10 | gpmc_a4 | | | | | |
| R9 | gpmc_a5 | 11 | gpmc_a5 | | | | | |
| R5 | gpmc_a6 | 11 | gpmc_a6 | | | | | |
| P5 | gpmc_a7 | 11 | gpmc_a7 | | | | | |
| N7 | gpmc_a8 | 12 | gpmc_a8 | | | | | |
| R4 | gpmc_a9 | 12 | gpmc_a9 | | | | | |
| N9 | gpmc_a10 | 12 | gpmc_a10 | | | | | |
| P9 | gpmc_a11 | 11 | gpmc_a11 | | | | | |
| P4 | gpmc_a12 | 13 | gpmc_a12 | | | | gpmc_a0 | |
| R3 | gpmc_a13 | 12 | gpmc_a13 | | | | | |
| T2 | gpmc_a14 | 12 | gpmc_a14 | | | | | |
| U2 | gpmc_a15 | 12 | gpmc_a15 | | | | | |
| U1 | gpmc_a16 | 12 | gpmc_a16 | | | | | |
| P3 | gpmc_a17 | 12 | gpmc_a17 | | | | | |
| R2 | gpmc_a18 | 12 | gpmc_a18 | | | | | |
| K7 | gpmc_a19 | 11 | gpmc_a19 | | gpmc_a13 | | | |
| M7 | gpmc_a20 | 11 | gpmc_a20 | | gpmc_a14 | | | |
| J5 | gpmc_a21 | 11 | gpmc_a21 | | gpmc_a15 | | | |
| K6 | gpmc_a22 | 11 | gpmc_a22 | | gpmc_a16 | | | |
| J7 | gpmc_a23 | 11 | gpmc_a23 | | gpmc_a17 | | | |

**Table 7-33. Virtual Functions Mapping for GPMC (continued)**

| BALL NUMBER | BALL NAME | Delay Mode Value | MUXMODE[15:0] | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | GPMC_VIRTUAL 1 | 0 | 1 | 2 | 3 | 5 | 6 |
| J4 | gpmc_a24 | 11 | gpmc_a24 | | gpmc_a18 | | | |
| J6 | gpmc_a25 | 11 | gpmc_a25 | | gpmc_a19 | | | |
| H4 | gpmc_a26 | 11 | gpmc_a26 | | gpmc_a20 | | | |
| H5 | gpmc_a27 | 11 | gpmc_a27 | | gpmc_a21 | | | |
| H6 | gpmc_cs1 | 11 | gpmc_cs1 | | gpmc_a22 | | | |
| T1 | gpmc_cs0 | 14 | gpmc_cs0 | | | | | |
| P2 | gpmc_cs2 | 12 | gpmc_cs2 | | | | | |
| P1 | gpmc_cs3 | 10 | gpmc_cs3 | | | | gpmc_a1 | |
| P7 | gpmc_clk | 12 | gpmc_clk | gpmc_cs7 | | gpmc_wait1 | | |
| N1 | gpmc_advn_ale | 13 | gpmc_advn_ale | gpmc_cs6 | | gpmc_wait1 | gpmc_a2 | gpmc_a23 |
| M5 | gpmc_oen_ren | 14 | gpmc_oen_ren | | | | | |
| M3 | gpmc_wen | 14 | gpmc_wen | | | | | |
| N6 | gpmc_ben0 | 11 | gpmc_ben0 | gpmc_cs4 | | | | |
| M4 | gpmc_ben1 | 11 | gpmc_ben1 | gpmc_cs5 | | | gpmc_a3 | |
| N2 | gpmc_wait0 | 14 | gpmc_wait0 | | | | | |
| AG5 | vin1a_d11 | 9 | | | | | gpmc_a23 | |
| AF2 | vin1a_d12 | 9 | | | | | gpmc_a24 | |
| AF6 | vin1a_d13 | 9 | | | | | gpmc_a25 | |
| AF3 | vin1a_d14 | 9 | | | | | gpmc_a26 | |
| AF4 | vin1a_d15 | 9 | | | | | gpmc_a27 | |

## 7.11 Timers

The device has 16 general-purpose (GP) timers (TIMER1 - TIMER16), two watchdog timers, and a 32-kHz synchronized timer (COUNTER_32K) that have the following features:

- Dedicated input trigger for capture mode and dedicated output trigger/pulse width modulation (PWM) signal
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Supported modes:
  - Compare and capture modes
  - Auto-reload mode
  - Start-stop mode
- On-the-fly read/write register (while counting)

The device has two system watchdog timer (WD_TIMER1 and WD_TIMER2) that have the following features:

- Free-running 32-bit upward counter
- On-the-fly read/write register (while counting)
- Reset upon occurrence of a timer overflow condition

The device includes one instance of the 32-bit watchdog timer: WD_TIMER2, also called the MPU watchdog timer.

The watchdog timer is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.


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**NOTE**

For additional information on the Timer Module, see Timers chapter in the Device TRM.

## 7.12 Inter-Integrated Circuit Interface (I2C)

The device includes 5 inter-integrated circuit (I2C) modules which provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive 8-bit data to/from the device through the I2C module.

**NOTE**

Note that, on I2C1 and I2C2, due to characteristics of the open drain IO cells, HS mode is not supported.

**NOTE**

Inter-integrated circuit i (i=1 to 5) module is also referred to as I2Ci.

**NOTE**

For more information, see the Multimaster High-Speed I2C Controller section of the Device TRM.

Table 7-34, Table 7-35 and Figure 7-23 assume testing over the recommended operating conditions and electrical characteristic conditions below.

**Table 7-34. Timing Requirements for I2C Input Timings[(1)]**

| NO. | PARAMETER | DESCRIPTION | STANDARD MODE | | FAST MODE | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | µs |
| 2 | $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | µs |
| 3 | $t_{h(SDAL-SCLL)}$ | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | µs |
| 4 | $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | µs |
| 5 | $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | µs |
| 6 | $t_{su(SDAV-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100[(2)] | | ns |
| 7 | $t_{h(SCLL-SDAV)}$ | Hold time, SDA valid after SCL low | 0[(3)] | 3.45[(4)] | 0[(3)] | 0.9[(4)] | µs |
| 8 | $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | µs |
| 9 | $t_{r(SDA)}$ | Rise time, SDA | | 1000 | $20 + 0.1C_b$[(5)] | 300[(3)] | ns |
| 10 | $t_{r(SCL)}$ | Rise time, SCL | | 1000 | $20 + 0.1C_b$[(5)] | 300[(3)] | ns |
| 11 | $t_{f(SDA)}$ | Fall time, SDA | | 300 | $20 + 0.1C_b$[(5)] | 300[(3)] | ns |
| 12 | $t_{f(SCL)}$ | Fall time, SCL | | 300 | $20 + 0.1C_b$[(5)] | 300[(3)] | ns |
| 13 | $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4 | | 0.6 | | µs |
| 14 | $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | | | 0 | 50 | ns |
| 15 | $C_b$ [(5)] | Capacitive load for each bus line | | 400 | | 400 | pF |

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

(2) A Fast-mode $I^2C$-bus™ device can be used in a Standard-mode $I^2C$-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_r$ max + $t_{su(SDA-SCLH)}$= 1000 + 250 = 1250 ns (according to the Standard-mode $I^2C$-Bus Specification) before the SCL line is released.

(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IHmin}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

(4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.

(5) $C_b$ = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

### Table 7-35. Timing Requirements for $I^2C$ HS-Mode ($I^2C$3/4/5 Only)(1)

| NO. | PARAMETER | DESCRIPTION | $C_b$ = 100 pF MAX | | $C_b$ = 400 pF (2) | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SCL)}$ | Cycle time, SCL | 0.294 | | 0.588 | | µs |
| 2 | $t_{su(SCLH-SDAL)}$ | Set-up time, SCL high before SDA low (for a repeated START condition) | 160 | | 160 | | ns |
| 3 | $t_{h(SDAL-SCLL)}$ | Hold time, SCL low after SDA low (for a repeated START condition) | 160 | | 160 | | ns |
| 4 | $t_{w(SCLL)}$ | LOW period of the SCLH clock | 160 | | 320 | | ns |
| 5 | $t_{w(SCLH)}$ | HIGH period of the SCLH clock | 60 | | 120 | | ns |
| 6 | $t_{su(SDAV-SCLH)}$ | Setup time, SDA valid vefore SCL high | 10 | | 10 | | ns |
| 7 | $t_{h(SCLL-SDAV)}$ | Hold time, SDA valid after SCL low | 0 (3) | 70 | 0 (3) | 150 | ns |
| 13 | $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for a STOP condition) | 160 | | 160 | | ns |
| 14 | $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | 0 | 10 | 0 | 10 | ns |
| 15 | $C_b$ (2) | Capacitive load for SDAH and SCLH lines | | 100 | | 400 | pF |
| 16 | $C_b$ | Capacitive load for SDAH + SDA line and SCLH + SCL line | | 400 | | 400 | pF |

(1) $I^2C$ HS-Mode is only supported on $I^2C$3/4/5. I2C HS-Mode is not supported on $I^2C$1/2.

(2) For bus line loads $C_b$ between 100 and 400 pF the timing parameters must be linearly interpolated.

(3) A device must internally provide a Data hold time to bridge the undefined part between $V_{IH}$ and $V_{IL}$ of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

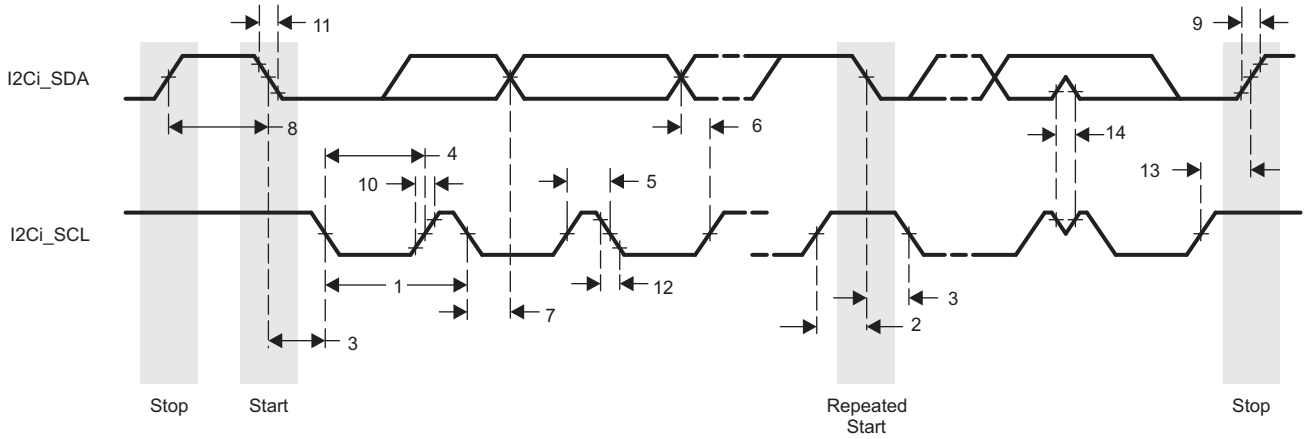


**Figure 7-23. I2C Receive Timing**


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Table 7-36 and Figure 7-24 assume testing over the recommended operating conditions and electrical characteristic conditions below.

**Table 7-36. Switching Characteristics Over Recommended Operating Conditions for I2C Output Timings[(2)]**

| NO. | PARAMETER | DESCRIPTION | STANDARD MODE | | FAST MODE | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 16 | $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | µs |
| 17 | $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | µs |
| 18 | $t_{h(SDAL-SCLL)}$ | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | µs |
| 19 | $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | µs |
| 20 | $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | µs |
| 21 | $t_{su(SDAV-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100 | | ns |
| 22 | $t_{h(SCLL-SDAV)}$ | Hold time, SDA valid after SCL low (for I2C bus devices) | 0 | 3.45 | 0 | 0.9 | µs |
| 23 | $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | µs |
| 24 | $t_{r(SDA)}$ | Rise time, SDA | | 1000 | $20 + 0.1C_b$ [(1) (3)] | 300[(3)] | ns |
| 25 | $t_{r(SCL)}$ | Rise time, SCL | | 1000 | $20 + 0.1C_b$ [(1) (3)] | 300[(3)] | ns |
| 26 | $t_{f(SDA)}$ | Fall time, SDA | | 300 | $20 + 0.1C_b$ [(1) (3)] | 300[(3)] | ns |
| 27 | $t_{f(SCL)}$ | Fall time, SCL | | 300 | $20 + 0.1C_b$ [(1) (3)] | 300[(3)] | ns |
| 28 | $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4 | | 0.6 | | µs |
| 29 | $C_p$ | Capacitance for each I2C pin | | 10 | | 10 | pF |

(1) $C_b$ = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

(2) Software must properly configure the I2C module registers to achieve the timings shown in this table. See the Device TRM for details.

(3) These timings apply only to I2C1 and I2C2. I2C3, I2C4, and I2C5 use standard LVCMOS buffers to emulate open-drain buffers and their rise/fall times should be referenced in the device IBIS model.

**NOTE**

I2C emulation is achieved by configuring the LVCMOS buffers to output Hi-Z instead of driving high when transmitting logic-1.

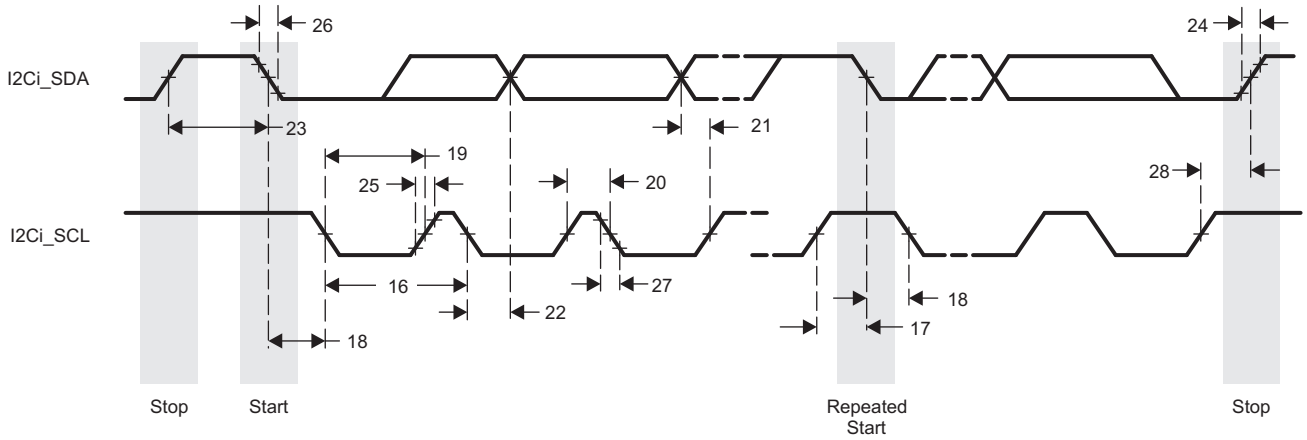


**Figure 7-24. I2C Transmit Timing**

## 7.13 HDQ / 1-Wire Interface (HDQ1W)

The module is intended to work with both HDQ and 1-Wire protocols. The protocols use a single wire to communicate between the master and the slave. The protocols employ an asynchronous return to one mechanism where, after any command, the line is pulled high.

**NOTE**

For more information, see the HDQ / 1-Wire section of the Device TRM.

### *7.13.1 HDQ / 1-Wire — HDQ Mode*

Table 7-37 and Table 7-38 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 7-25, Figure 7-26, Figure 7-27, and Figure 7-28).

**Table 7-37. HDQ/1-Wire Timing Requirements—HDQ Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{CYCH}$ | Read bit window timing | 190 | 250 | µs |
| 2 | $t_{HW1}$ | Read one data valid after HDQ low | 32(2) | 66(2) | µs |
| 3 | $t_{HW0}$ | Read zero data hold after HDQ low | 70(2) | 145(2) | µs |
| 4 | $t_{RSPS}$ | Response time from HDQ slave device(1) | 190 | 320 | µs |

(1) Defined by software.

(2) If the HDQ slave device drives a logic-low state after tHW0 maximum, it can be interpreted as a break pulse. For more information see Table 7-38 and the HDQ/1-Wire chapter of the TRM.

**Table 7-38. HDQ / 1-Wire Switching Characteristics - HDQ Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 5 | $t_B$ | Break timing | 190 | | µs |
| 6 | $t_{BR}$ | Break recovery time | 40 | | µs |
| 7 | $t_{CYCD}$ | Write bit windows timing | 190 | | µs |
| 8 | $t_{DW1}$ | Write one data valid after HDQ low | 0.5 | 50 | µs |
| 9 | $t_{DW0}$ | Write zero data hold after HDQ low | 86 | 145 | µs |

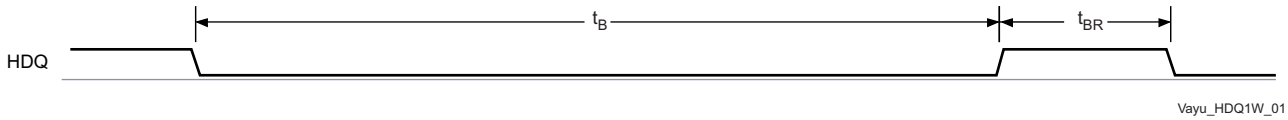


**Figure 7-25. HDQ Break and Break Recovery Timing — HDQ Interface Writing to Slave**

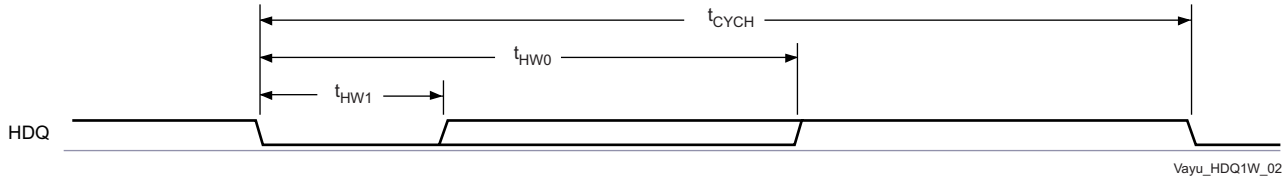


**Figure 7-26. Device HDQ Interface Bit Read Timing (Data)**


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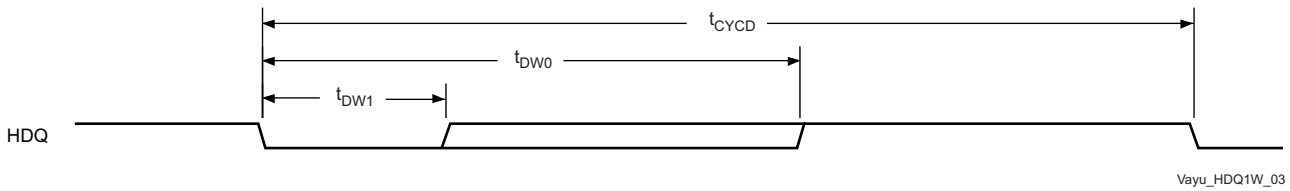


**Figure 7-27. Device HDQ Interface Bit Write Timing (Command / Address or Data)**

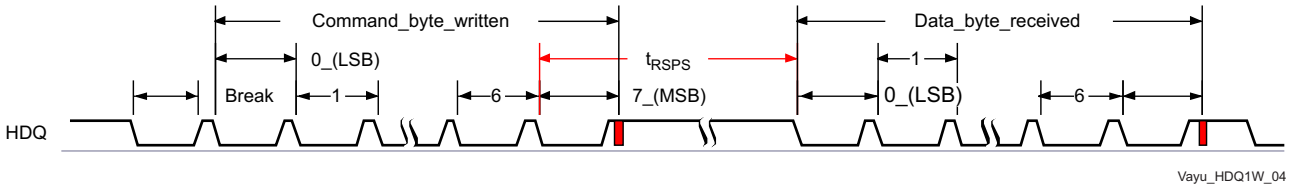


**Figure 7-28. HDQ Communication Timing**

### *7.13.2 HDQ/1-Wire—1-Wire Mode*

Table 7-39 and Table 7-40 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 7-29, Figure 7-30, and Figure 7-31).

**Table 7-39. HDQ / 1-Wire Timing Requirements - 1-Wire Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 10 | $t_{PDH}$ | Presence pulse delay high | 15 | 60 | µs |
| 11 | $t_{PDL}$ | Presence pulse delay low | 60 | 240 | µs |
| 12 | $t_{RDV}$ | Read data valid time | $t_{LOWR}$ | 15 | µs |
| 13 | $t_{REL}$ | Read data release time | 0 | 45 | µs |

**Table 7-40. HDQ / 1-Wire Switching Characteristics - 1-Wire Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 14 | $t_{RSTL}$ | Reset time low | 480 | 960 | µs |
| 15 | $t_{RSTH}$ | Reset time high | 480 | | µs |
| 16 | $t_{SLOT}$ | Bit cycle time | 60 | 120 | µs |
| 17 | $t_{LOW1}$ | Write bit-one time | 1 | 15 | µs |
| 18 | $t_{LOW0}$ | Write bit-zero time(2) | 60 | 120 | µs |
| 19 | $t_{REC}$ | Recovery time | 1 | | µs |
| 20 | $t_{LOWR}$ | Read bit strobe time(1) | 1 | 15 | µs |

(1) $t_{LOWR}$ (low pulse sent by the master) must be short as possible to maximize the master sampling window.

(2) $t_{LOW0}$ must be less than $t_{SLOT}$.

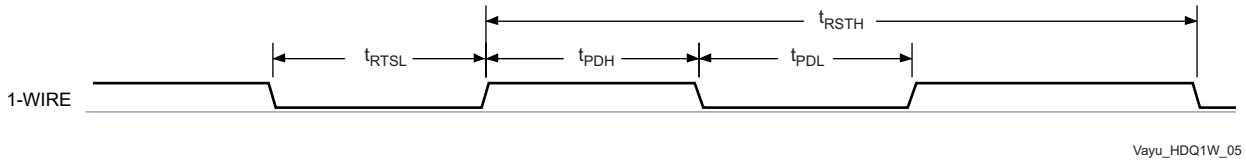


**Figure 7-29. 1-Wire—Break (Reset)**

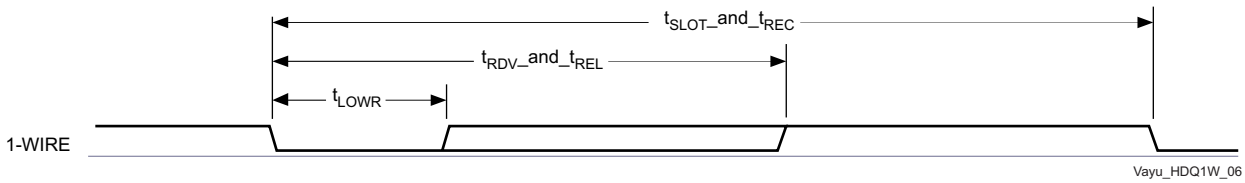


**Figure 7-30. 1-Wire—Read Bit (Data)**

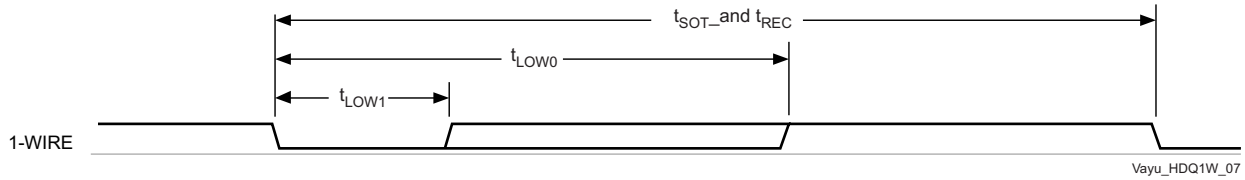


**Figure 7-31. 1-Wire—Write Bit-One Timing (Command / Address or Data)**

## 7.14 Universal Asynchronous Receiver Transmitter (UART)

The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. There are 10 UART modules in the device. Only one UART supports IrDA features. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices

The UARTi (where i = 1 to 10) include the following features:

- 16C750 compatibility
- 64-byte FIFO buffer for receiver and 64-byte FIFO for transmitter
- Baud generation based on programmable divisors N (where N = 1…16 384) operating from a fixed functional clock of 48 MHz or 192 MHz
- Break character detection and generation
- Configurable data format:
  - Data bit: 5, 6, 7, or 8 bits
  - Parity bit: Even, odd, none
  - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)
- Only UART1 module has extended modem control signals (DCD, RI, DTR, DSR)
- Only UART3 supports IrDA

**NOTE**

For more information, see the UART/IrDA/CIR section of the Device TRM.

Table 7-41, Table 7-42 and Figure 7-32 assume testing over the recommended operating conditions and electrical characteristic conditions below.

**Table 7-41. Timing Requirements for UART**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 4 | $t_{w(RX)}$ | Pulse width, receive data bit, 15/30/100pF high or low | 0.96U(1) | 1.05U(1) | ns |
| 5 | $t_{w(CTS)}$ | Pulse width, receive start bit, 15/30/100pF high or low | 0.96U(1) | 1.05U(1) | ns |
| | $t_{d(RTS-TX)}$ | Delay time, transmit start bit to transmit data | P(2) | | ns |
| | $t_{d(CTS-TX)}$ | Delay time, receive start bit to transmit data | P(2) | | ns |


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(1) U = UART baud time = 1/programmed baud rate
(2) P = Clock period of the reference clock (FCLK, usually 48 MHz or 192MHz).

**Table 7-42. Switching Characteristics Over Recommended Operating Conditions for UART**

| NO. | PARAMETER | DESCRIPTION | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| | $f_{(baud)}$ | Maximum programmable baud rate | 15 pF | | 12 | MHz |
| | | | 30 pF | | 0.23 | |
| | | | 100 pF | | 0.115 | |
| 2 | $t_{w(TX)}$ | Pulse width, transmit data bit, 15/30/100 pF high or low | | U - 2[(1)] | U + 2[(1)] | ns |
| 3 | $t_{w(RTS)}$ | Pulse width, transmit start bit, 15/30/100 pF high or low | | U - 2[(1)] | U + 2[(1)] | ns |

(1) U = UART baud time = 1/programmed baud rate

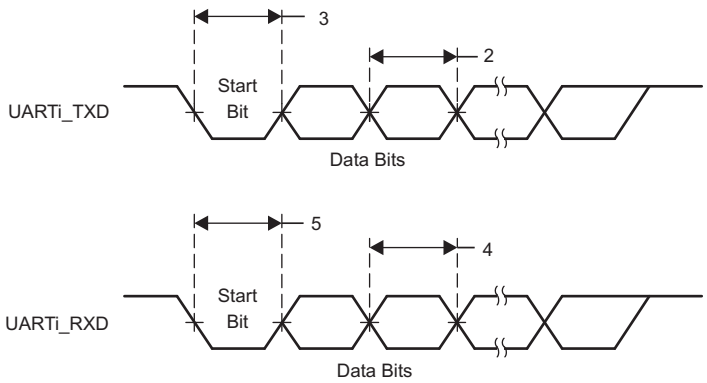


**Figure 7-32. UART Timing**

## 7.15 Multichannel Serial Peripheral Interface (McSPI)

The McSPI is a master/slave synchronous serial bus. There are four separate McSPI modules (SPI1, SPI2, SPI3, and SPI4) in the device. All these four modules support up to four external devices (four chip selects) and are able to work as both master and slave.

The McSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four master channels, or single channel in slave mode
- Master multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible input/output (I/O) port controls per channel
  - Programmable clock granularity
  - SPI configuration per channel. This means, clock definition, polarity enabling and word width
- Power management through wake-up capabilities
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel.
- Each SPI module supports multiple chip select pins spim_cs[i], where i = 1 to 4.

**NOTE**

For more information, see the Serial Communication Interface section of the device TRM.

**NOTE**

The McSPIm module (m = 1 to 4) is also referred to as SPIm.

**CAUTION**

The IO timings provided in this section are applicable for all combinations of signals for SPI1 and SPI2. However, the timings are only valid for SPI3 and SPI4 if signals within a single IOSET are used. The IOSETS are defined in the Table 7-45.

Table 7-43, Figure 7-33 and Figure 7-34 present Timing Requirements for McSPI - Master Mode.

**Table 7-43. Timing Requirements for SPI - Master Mode (1)(8)**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| SM1 | $t_{c(SPICLK)}$ | Cycle time, spi_sclk (1) (2) | SPI1/2/3/4 | 20.8 (3) | | ns |
| SM2 | $t_{w(SPICLKL)}$ | Typical Pulse duration, spi_sclk low (1) | | 0.5*P-1 (4) | | ns |
| SM3 | $t_{w(SPICLKH)}$ | Typical Pulse duration, spi_sclk high (1) | | 0.5*P-1 (4) | | ns |
| SM4 | $t_{su(MISO-SPICLK)}$ | Setup time, spi_d[x] valid before spi_sclk active edge (1) | | 4.4 | | ns |
| SM5 | $t_{h(SPICLK-MISO)}$ | Hold time, spi_d[x] valid after spi_sclk active edge (1) | | 3.9 | | ns |
| SM6 | $t_{d(SPICLK-SIMO)}$ | Delay time, spi_sclk active edge to spi_d[x] transition (1) | SPI1 | -4.27 | 4.27 | ns |
| | | | SPI2 | -4.32 | 4.32 | ns |
| | | | SPI3 | -5.37 | 4.23 | ns |
| | | | SPI4 | -3.81 | 4..41 | ns |
| SM7 | $t_{d(CS-SIMO)}$ | Delay time, spi_cs[x] active edge to spi_d[x] transition | | | 5 | ns |
| SM8 | $t_{d(CS-SPICLK)}$ | Delay time, spi_cs[x] active to spi_sclk first edge (1) | MASTER_PHA0 (5) | B-4.6 (6) | | ns |
| | | | MASTER_PHA1 (5) | A-4.6 (7) | | ns |
| SM9 | $t_{d(SPICLK-CS)}$ | Delay time, spi_sclk last edge to spi_cs[x] inactive (1) | MASTER_PHA0 (5) | A-4.6 (7) | | ns |
| | | | MASTER_PHA1 (5) | B-4.6 (6) | | ns |

(1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.

(2) Related to the SPI_CLK maximum frequency.

(3) 20.8ns cycle time = 48MHz, 26ns cycle time = 38.4MHz

(4) P = SPICLK period.

(5) SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.

(6) B = (TCS + 0.5) * TSPICLKREF * Fratio, where TCS is a bit field of the SPI_CH(i)CONF register and Fratio = Even ≥2.

(7) When P = 20.8 ns, A = (TCS + 1) * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register. When P > 20.8 ns, A = (TCS + 0.5) * Fratio * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register.

(8) The IO timings provided in this section are applicable for all combinations of signals for spi1 and spi2. However, the timings are only valid for spi3 and spi4 if signals within a single IOSET are used. The IOSETs are defined in the following tables.


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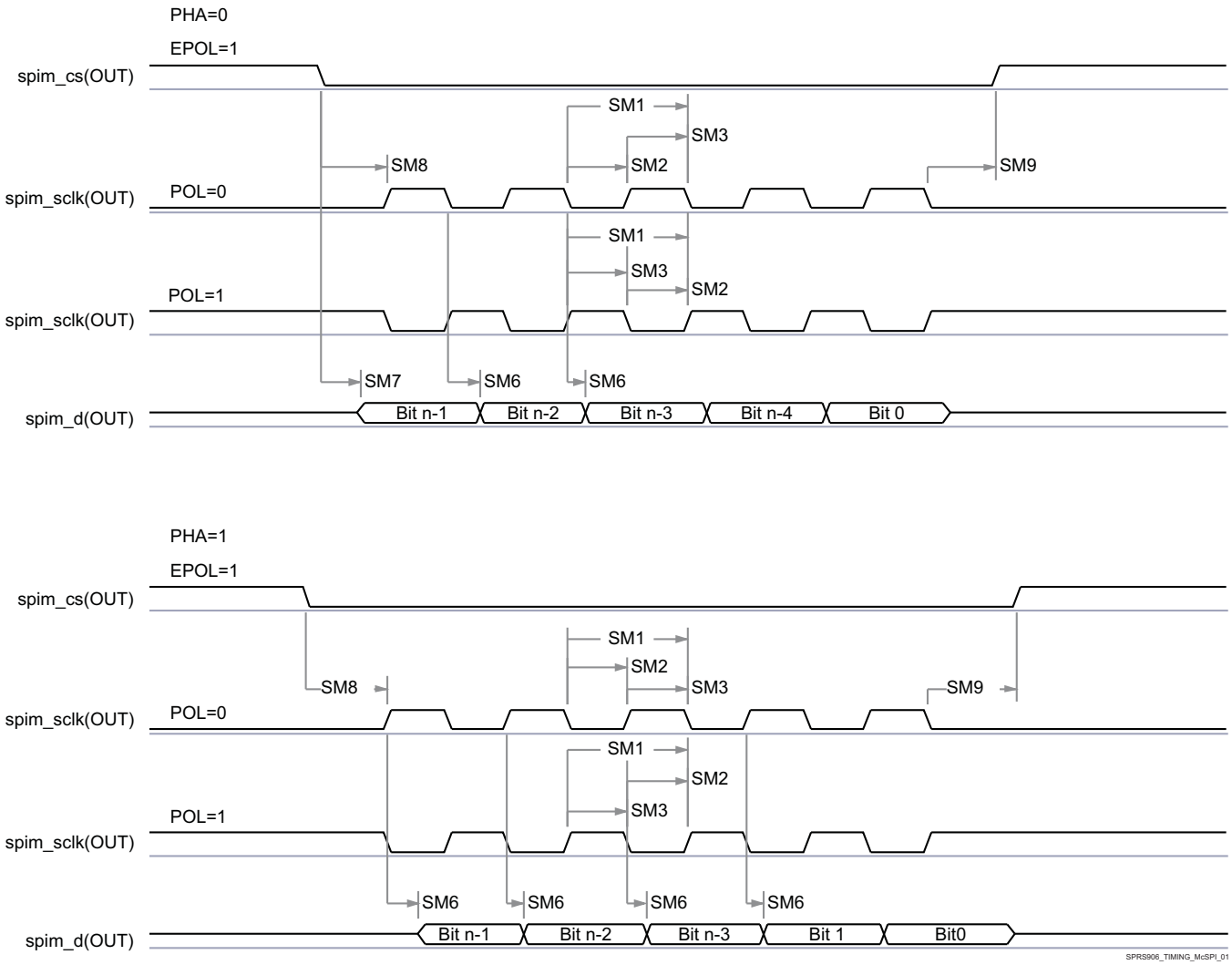


**Figure 7-33. McSPI - Master Mode Transmit**

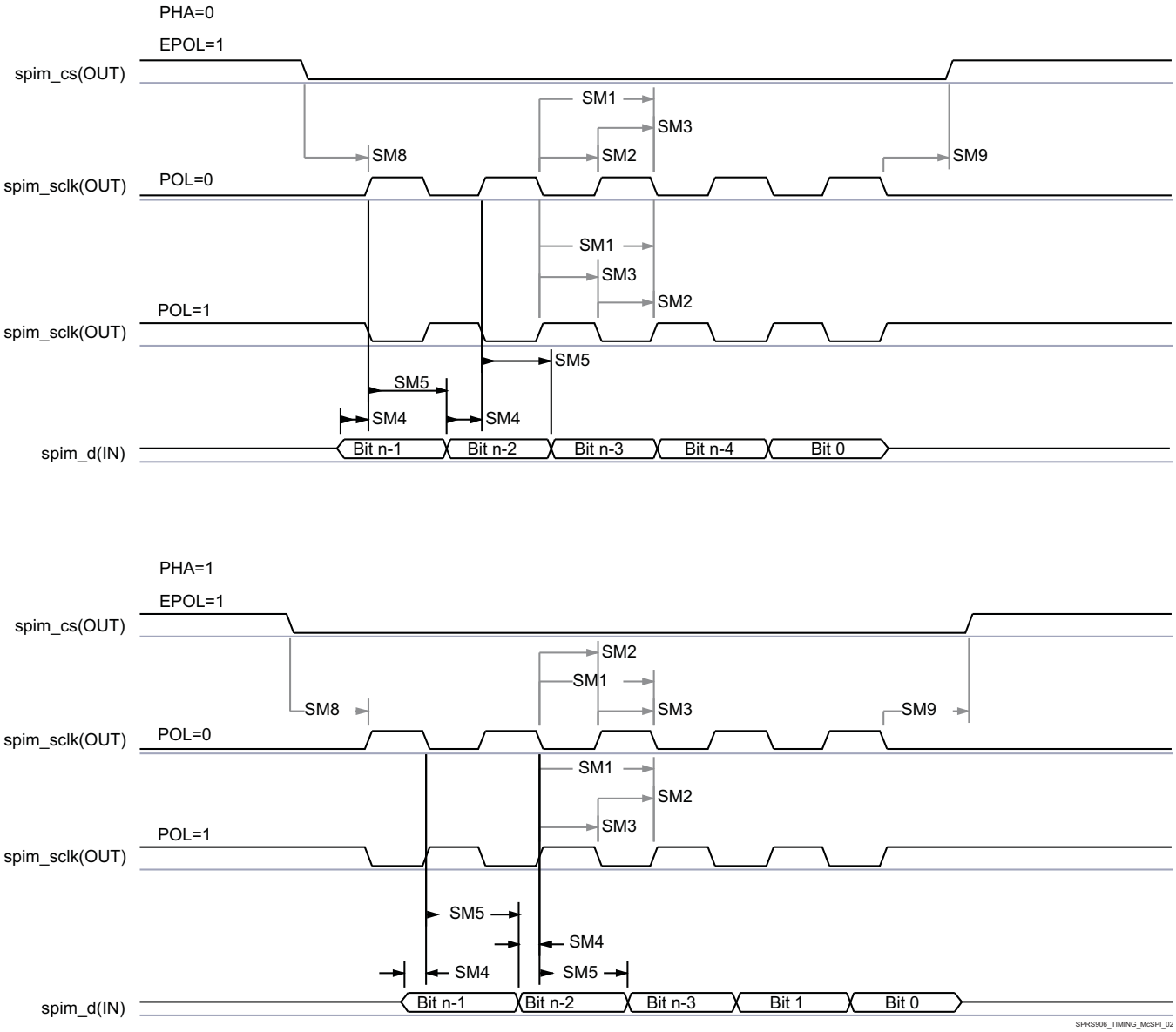


**Figure 7-34. McSPI - Master Mode Receive**

Table 7-44, Figure 7-35 and Figure 7-36 present Timing Requirements for McSPI - Slave Mode.

**Table 7-44. Timing Requirements for SPI - Slave Mode**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| SS1 | $t_{c(SPICLK)}$ | Cycle time, spi_sclk (1) (2) | (3) | 62.5 | | ns |
| SS2 | $t_{w(SPICLKL)}$ | Typical Pulse duration, spi_sclk low (1) | | 0.45*P (4) | | ns |
| SS3 | $t_{w(SPICLKH)}$ | Typical Pulse duration, spi_sclk high (1) | | 0.45*P (4) | | ns |
| SS4 | $t_{su(SIMO-SPICLK)}$ | Setup time, spi_d[x] valid before spi_sclk active edge (1) | | 5 | | ns |
| SS5 | $t_{h(SPICLK-SIMO)}$ | Hold time, spi_d[x] valid after spi_sclk active edge (1) | | 5 | | ns |
| SS6 | $t_{d(SPICLK-SOMI)}$ | Delay time, spi_sclk active edge to mcspi_somi transition (1) | SPI1/2/3 | 2 | 26.1 | ns |
| | | | SPI4 | 2 | 18 | ns |
| SS7 | $t_{d(CS-SOMI)}$ | Delay time, spi_cs[x] active edge to mcspi_somi transition (1) | | | 20.95 | ns |
| SS8 | $t_{su(CS-SPICLK)}$ | Setup time, spi_cs[x] valid before spi_sclk first edge (1) | | 5 | | ns |
| SS9 | $t_{h(SPICLK-CS)}$ | Hold time, spi_cs[x] valid after spi_sclk last edge (1) | | 5 | | ns |


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(1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.

(2) When operating the SPI interface in RX-only mode, the minimum Cycle time is 26ns (38.4MHz)

(3) 62.5ns Cycle time = 16 MHz

(4) P = SPICLK period.

(5) PHA = 0; SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.

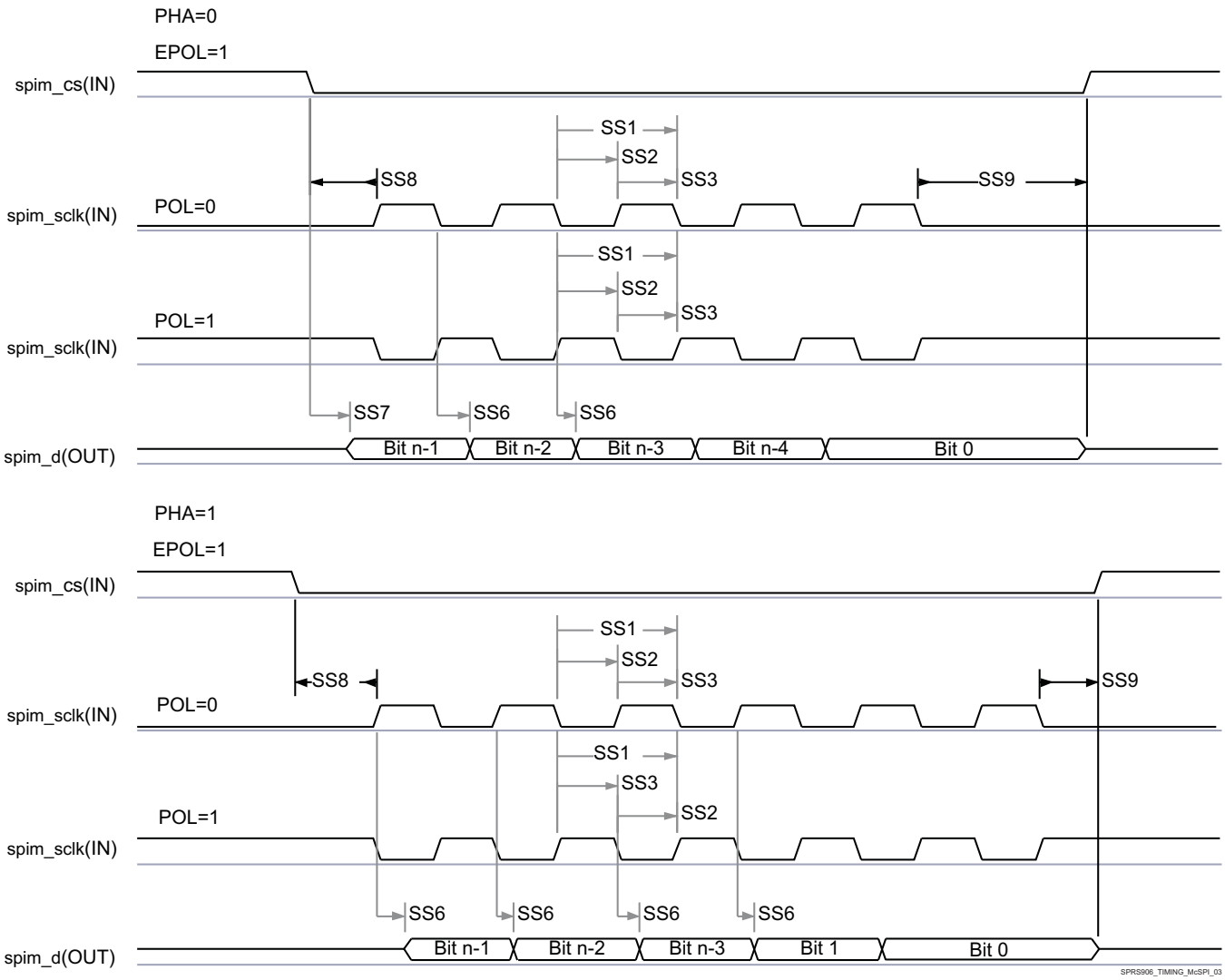


**Figure 7-35. McSPI - Slave Mode Transmit**

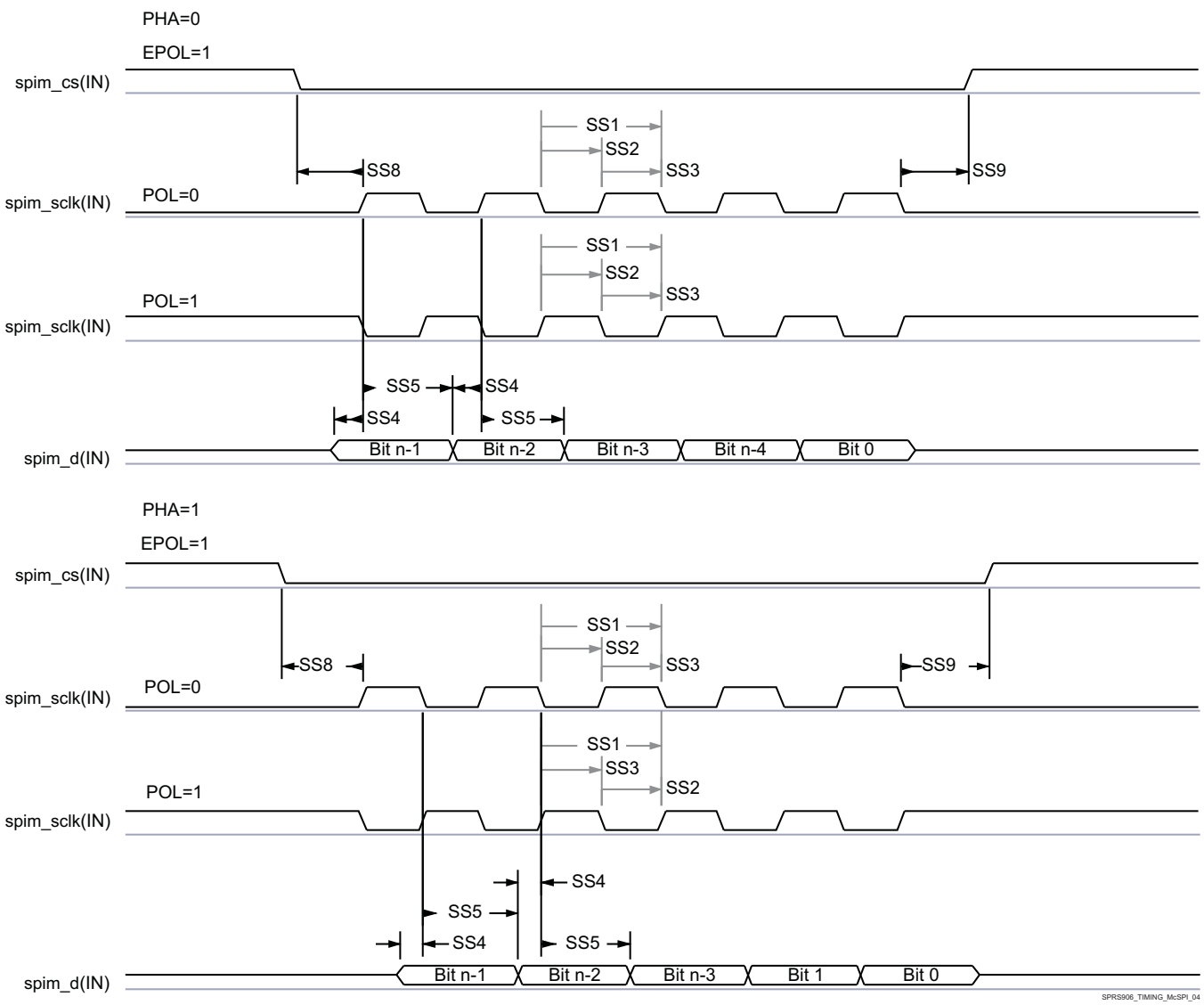


**Figure 7-36. McSPI - Slave Mode Receive**

In Table 7-45 are presented the specific groupings of signals (IOSET) for use with SPI3 and SPI4.

**Table 7-45. McSPI3/4 IOSETs**

| Signal | IOSET1 | | IOSET2 | | IOSET3 | | IOSET4 | | IOSET5 | | IOSET6 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | BALL | MUX | BALL | MUX | BALL | MUX | BALL | MUX | BALL | MUX | BALL | MUX |
| **SPI3** | | | | | | | | | | | | |
| spi3_sclk | AD9 | 8 | E11 | 8 | V2 | 7 | B12 | 3 | C18 | 2 | AC4 | 1 |
| spi3_d1 | AF9 | 8 | B10 | 8 | Y1 | 7 | A11 | 3 | A21 | 2 | AC7 | 1 |
| spi3_d0 | AE9 | 8 | C11 | 8 | W9 | 7 | B13 | 3 | G16 | 2 | AC6 | 1 |
| spi3_cs0 | AF8 | 8 | D11 | 8 | V9 | 7 | A12 | 3 | D17 | 2 | AC9 | 1 |
| spi3_cs1 | AC3 | 1 | B11 | 8 | AC3 | 1 | E14 | 3 | B11 | 8 | AC3 | 1 |
| spi3_cs2 | - | - | F11 | 8 | - | - | F11 | 8 | F11 | 8 | - | - |
| spi3_cs3 | - | - | A10 | 8 | - | - | A10 | 8 | A10 | 8 | - | - |
| **SPI4** | | | | | | | | | | | | |
| spi4_sclk | N7 | 8 | G1 | 8 | V7 | 7 | AA3 | 2 | AC8 | 1 | - | - |


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**Table 7-45. McSPI3/4 IOSETs (continued)**

| Signal | IOSET1 | | IOSET2 | | IOSET3 | | IOSET4 | | IOSET5 | | IOSET6 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | BALL | MUX | BALL | MUX | BALL | MUX | BALL | MUX | BALL | MUX | BALL | MUX |
| spi4_d1 | R4 | 8 | G6 | 8 | U7 | 7 | AB9 | 2 | AD6 | 1 | - | - |
| spi4_d0 | N9 | 8 | F2 | 8 | V6 | 7 | AB3 | 2 | AB8 | 1 | - | - |
| spi4_cs0 | P9 | 8 | F3 | 8 | U6 | 7 | AA4 | 2 | AB5 | 1 | - | - |
| spi4_cs1 | P4 | 8 | P4 | 8 | Y1 | 8 | Y1 | 8 | Y1 | 8 | - | - |
| spi4_cs2 | R3 | 8 | R3 | 8 | W9 | 8 | W9 | 8 | W9 | 8 | - | - |
| spi4_cs3 | T2 | 8 | T2 | 8 | V9 | 8 | V9 | 8 | V9 | 8 | - | - |

## 7.16 Quad Serial Peripheral Interface (QSPI)

The Quad SPI (QSPI) module is a type of SPI module that allows single, dual or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. It works as a master only. There is one QSPI module in the device and it is primary intended for fast booting from quad-SPI flash memories.

General SPI features:

- Programmable clock divider
- Six pin interface (DCLK, CS_N, DOUT, DIN, QDIN1, QDIN2)
- 4 external chip select signals
- Support for 3-, 4- or 6-pin SPI interface
- Programmable CS_N to DOUT delay from 0 to 3 DCLKs
- Programmable signal polarities
- Programmable active clock edge
- Software controllable interface allowing for any type of SPI transfer

**NOTE**

For more information, see the Quad Serial Peripheral Interface section of the Device TRM.

**CAUTION**

The IO Timings provided in this section are only valid for some QSPI usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

**CAUTION**

The IO Timings provided in this section are only valid when all QSPI Chip Selects used in a system are configured to use the same Clock Mode (either Clock Mode 0 or Clock Mode3).

Table 7-46 and Table 7-47 present Timing and Switching Characteristics for Quad SPI Interface.

### Table 7-46. Switching Characteristics for QSPI

| No | PARAMETER | DESCRIPTION | Mode | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| Q1 | $t_{c(SCLK)}$ | Cycle time, sclk | Default Timing Mode, Clock Mode 0 | 13.02 | | ns |
| | | | Default Timing Mode, Clock Mode 3 | 20.8 | | ns |
| Q2 | $t_{w(SCLKL)}$ | Pulse duration, sclk low | | Y*P-1 (1) | | ns |
| Q3 | $t_{w(SCLKH)}$ | Pulse duration, sclk high | | Y*P-1 (1) | | ns |
| Q4 | $t_{d(CS-SCLK)}$ | Delay time, sclk falling edge to cs active edge, CS3:0 | Default Timing Mode | -M*P-2.0 (2) (3) | -M*P+2.0 (2) (3) | ns |
| Q5 | $t_{d(SCLK-CS)}$ | Delay time, sclk falling edge to cs inactive edge, CS3:0 | Default Timing Mode | N*P-2.0 (2) (3) | N*P+2.0 (2) (3) | ns |
| Q6 | $t_{d(SCLK-D1)}$ | Delay time, sclk falling edge to d[0] transition | Default Timing Mode | -2 | 2 | ns |
| Q7 | $t_{ena(CS-D1LZ)}$ | Enable time, cs active edge to d[0] driven (lo-z) | | -P-3.5 | -P+2.5 | ns |
| Q8 | $t_{dis(CS-D1Z)}$ | Disable time, cs active edge to d[0] tri-stated (hi-z) | | -P-2.5 | -P+2.0 | ns |
| Q9 | $t_{d(SCLK-D0)}$ | Delay time, sclk first falling edge to first d[0] transition | PHA=0 Only, Default Timing Mode | -2.45 - P | 1 .45 - P | ns |

(1) The Y parameter is defined as follows:
If DCLK_DIV is 0 or ODD then, Y equals 0.5.
If DCLK_DIV is EVEN then, Y equals (DCLK_DIV/2) / (DCLK_DIV+1).
For best performance, it is recommended to use a DCLK_DIV of 0 or ODD to minimize the duty cycle distortion. The HSDIVIDER on CLKOUTX2_H13 output of DPLL_PER can be used to achieve the desired clock divider ratio. All required details about clock division factor DCLK_DIV can be found in the device TRM.

(2) P = SCLK period.

(3) M=QSPI_SPI_DC_REG.DDx + 1 when Clock Mode 0.
M=QSPI_SPI_DC_REG.DDx when Clock Mode 3.
N = 2 when Clock Mode 0.
N = 3 when Clock Mode 3.


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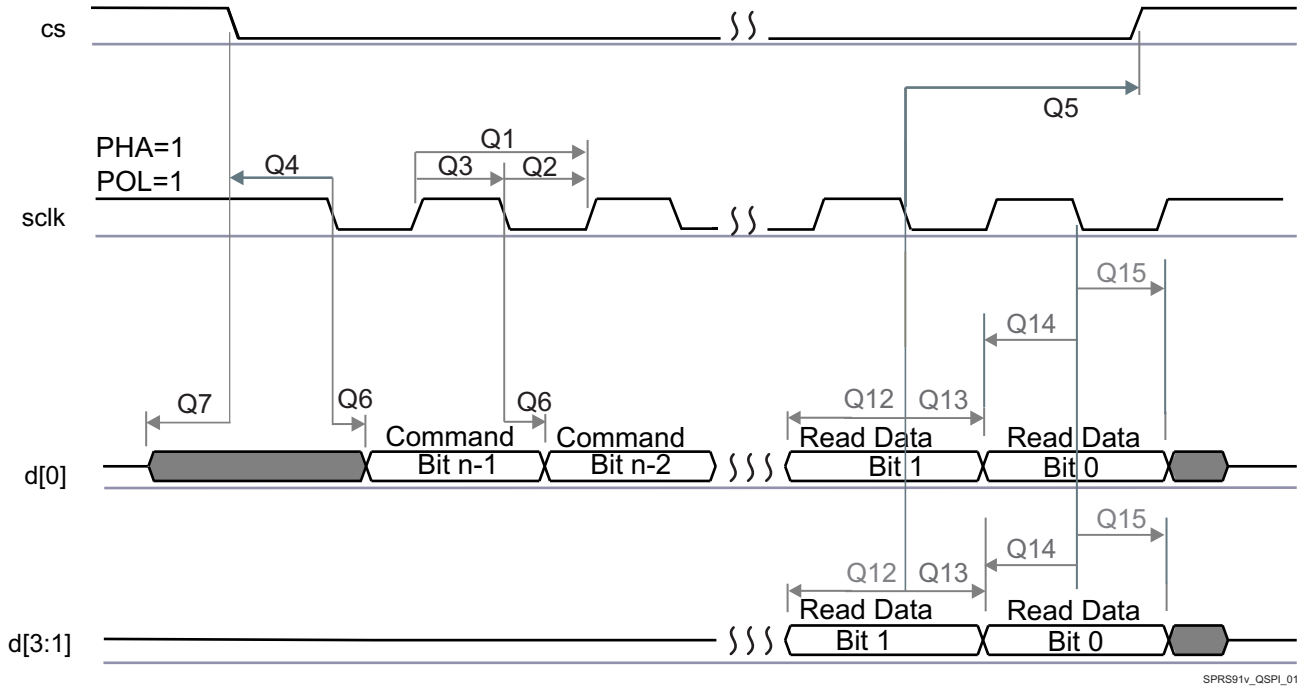


**Figure 7-37. QSPI Read (Clock Mode 3)**

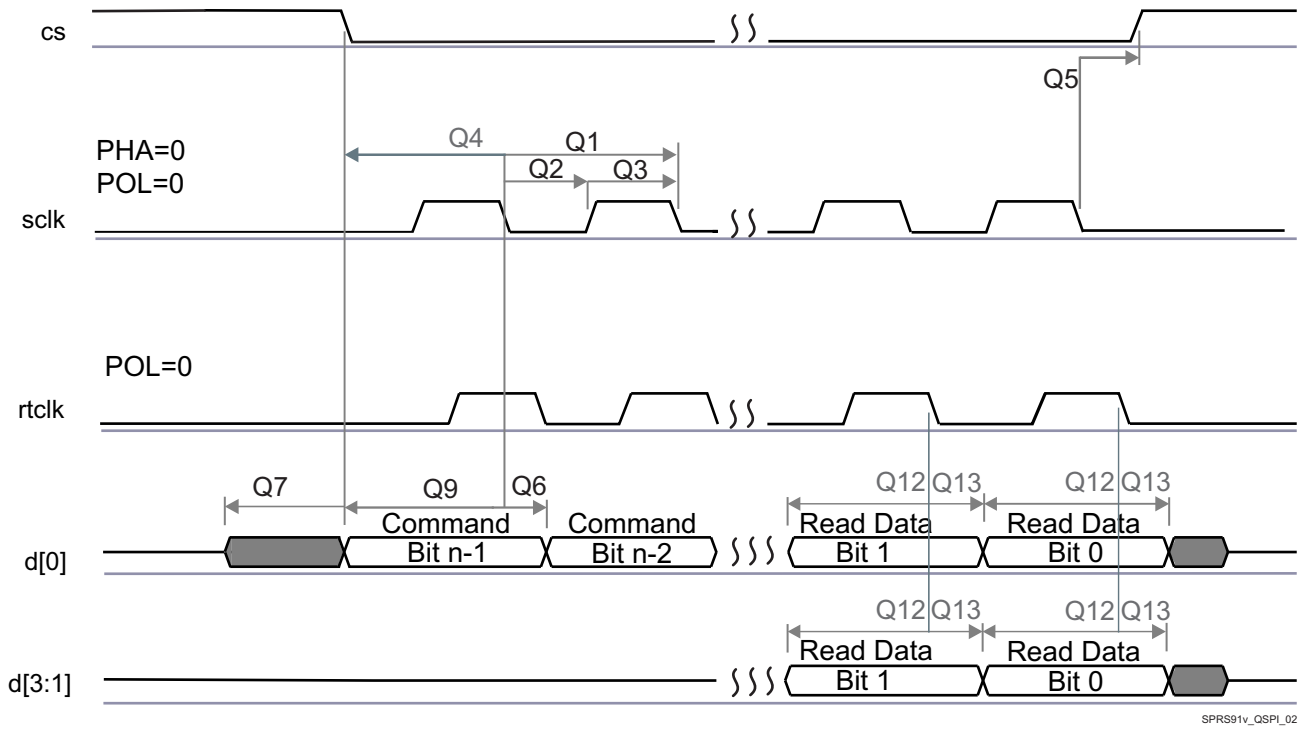


**Figure 7-38. QSPI Read (Clock Mode 0)**

**CAUTION**

The IO Timings provided in this section are only valid for some QSPI usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

**Table 7-47. Timing Requirements for QSPI**

| No | PARAMETER | DESCRIPTION | Mode | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| Q12 | $t_{su(D-RTCLK)}$ | Setup time, d[3:0] valid before falling rtclk edge | Default Timing Mode, Clock Mode 0 | 5.1 | | ns |
| | $t_{su(D-SCLK)}$ | Setup time, d[3:0] valid before falling sclk edge | Default Timing Mode, Clock Mode 3 | 12.3 | | ns |
| Q13 | $t_{h(RTCLK-D)}$ | Hold time, d[3:0] valid after falling rtclk edge | Default Timing Mode, Clock Mode 0 | -0.1 | | ns |
| | $t_{h(SCLK-D)}$ | Hold time, d[3:0] valid after falling sclk edge | Default Timing Mode, Clock Mode 3 | 0 | | ns |
| Q14 | $t_{su(D-SCLK)}$ | Setup time, final d[3:0] bit valid before final falling sclk edge | Default Timing Mode, Clock Mode 3 | 12.3-P (1) | | ns |
| Q15 | $t_{h(SCLK-D)}$ | Hold time, final d[3:0] bit valid after final falling sclk edge | Default Timing Mode, Clock Mode 3 | 0+P (1) | | ns |

(1) P = SCLK period.

(2) Clock Modes 1 and 2 are not supported.

(3) The Device captures data on the falling clock edge in Clock Mode 0 and 3, as opposed to the traditional rising clock edge. Although nonstandard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Modes 0 and 3.

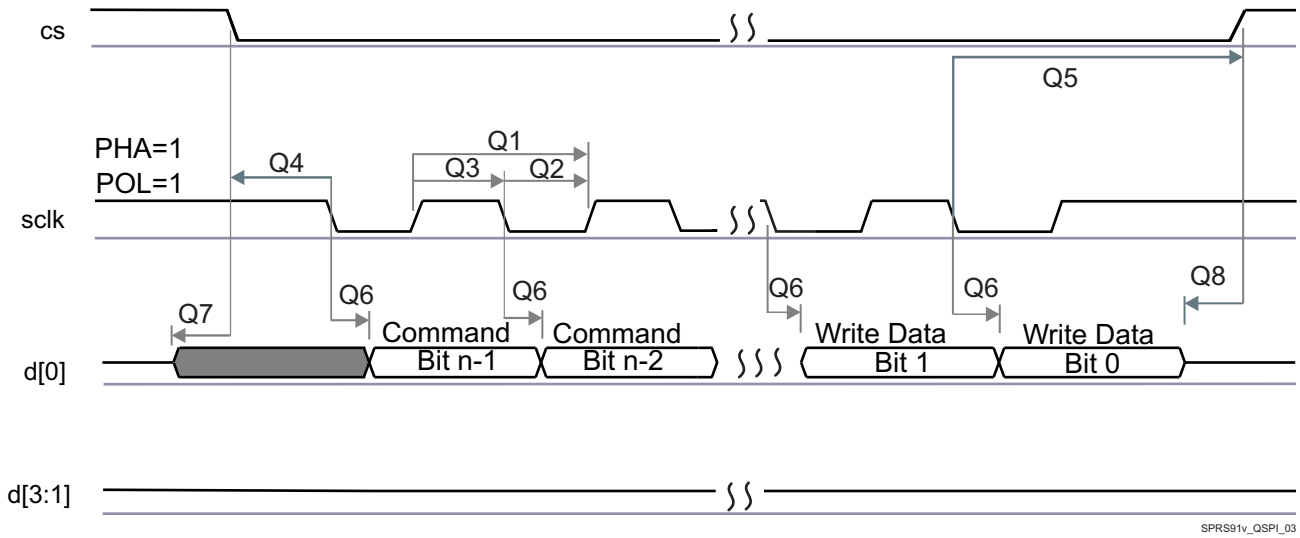


**Figure 7-39. QSPI Write (Clock Mode 3)**


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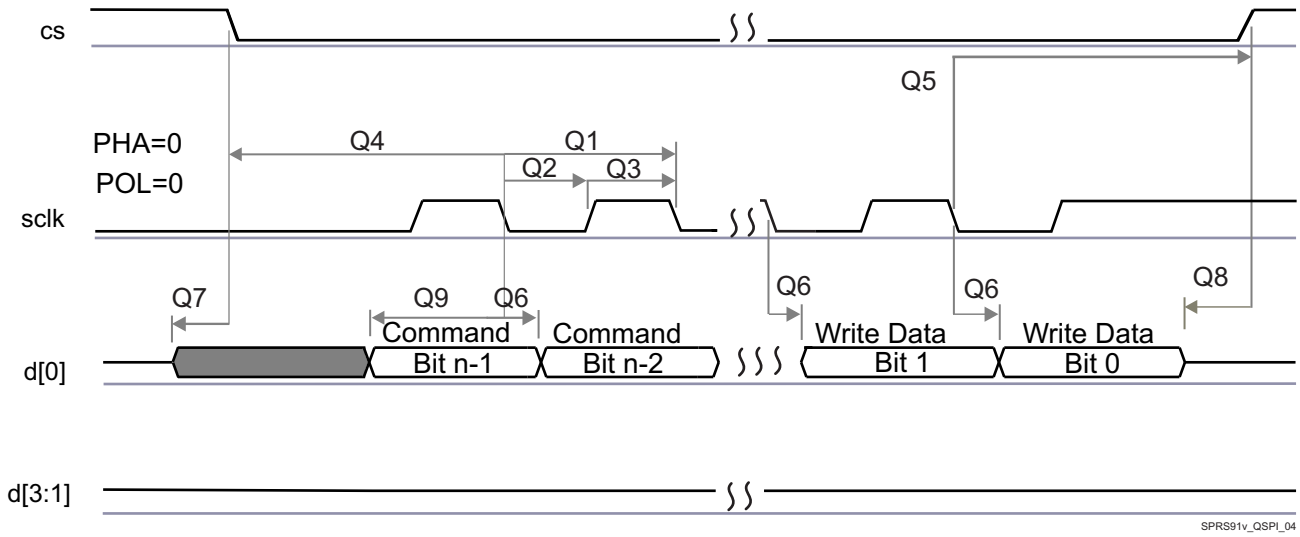


**Figure 7-40. QSPI Write (Clock Mode 0)**

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**NOTE**

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the Control Module chapter in the Device TRM.

---

Manual IO Timings Modes must be used to ensure some IO timings for QSPI. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-48 *Manual Functions Mapping for QSPI* for a definition of the Manual modes.

Table 7-48 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-48. Manual Functions Mapping for QSPI**

| BALL | BALL NAME | QSPI_MODE0_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 1 |
| T7 | gpmc_a3 | 114 | 0 | CFG_GPMC_A3_OUT | qspi1_cs2 |
| P6 | gpmc_a4 | 91 | 0 | CFG_GPMC_A4_OUT | qspi1_cs3 |
| R3 | gpmc_a13 | 0 | 0 | CFG_GPMC_A13_IN | qspi1_rtclk |
| T2 | gpmc_a14 | 2575 | 966 | CFG_GPMC_A14_IN | qspi1_d3 |
| U2 | gpmc_a15 | 2503 | 889 | CFG_GPMC_A15_IN | qspi1_d2 |
| U1 | gpmc_a16 | 2528 | 1007 | CFG_GPMC_A16_IN | qspi1_d0 |
| U1 | gpmc_a16 | 0 | 0 | CFG_GPMC_A16_OUT | qspi1_d0 |
| P3 | gpmc_a17 | 2533 | 980 | CFG_GPMC_A17_IN | qspi1_d1 |
| R2 | gpmc_a18 | 590 | 0 | CFG_GPMC_A18_OUT | qspi1_sclk |
| P2 | gpmc_cs2 | 0 | 0 | CFG_GPMC_CS2_OUT | qspi1_cs0 |
| P1 | gpmc_cs3 | 70 | 0 | CFG_GPMC_CS3_OUT | qspi1_cs1 |

## 7.17 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and inter-component digital audio interface transmission (DIT).

The device have integrated 8 McASP modules (McASP1-McASP8) with:

- McASP1 and McASP2 modules supporting 16 channels with independent TX/RX clock/sync domain
- McASP3 through McASP8 modules supporting 4 channels with independent TX/RX clock/sync domain

**NOTE**

For more information, see the Multichannel Audio Serial Port section of the Device TRM.

**CAUTION**

The IO Timings provided in this section are only valid for some McASP usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-49, Table 7-50, Table 7-51 and Figure 7-41 present Timing Requirements for McASP1 to McASP8.


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### Table 7-49. Timing Requirements for McASP1 (1)

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 20 | | ns |
| 2 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | 0.35P (2) | | ns |
| 3 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | | 20 | | ns |
| 4 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/X high or low | | 0.5R - 3 (3) | | ns |
| 5 | $t_{su(AFSRX-ACLK)}$ | Setup time, AFSR/X input valid before ACLKR/X | ACLKR/X int | 20 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 4 | | ns |
| 6 | $t_{h(ACLK-AFSRX)}$ | Hold time, AFSR/X input valid after ACLKR/X | ACLKR/X int | -1 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 2.21 | | ns |
| 7 | $t_{su(AXR-ACLK)}$ | Setup time, AXR input valid before ACLKR/X | ACLKR/X int | 21.9 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 4.42 | | ns |
| 8 | $t_{h(ACLK-AXR)}$ | Hold time, AXR input valid after ACLKR/X | ACLKR/X int | -1 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 2.52 | | ns |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKR/X period in ns.

(3) R = ACLKR/X period in ns.

### Table 7-50. Timing Requirements for McASP2 (1)

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 20 | | ns |
| 2 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | 0.35P (2) | | ns |
| 3 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | Any Other Conditions | 20 | | ns |
| | | | ACLKX/AFSX (In Sync Mode), ACLKR/AFSR (In Async Mode), and AXR are all inputs "80M" Virtual IO Timing Mode | 12.5 | | ns |
| 4 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/X high or low | Any Other Conditions | 0.5R - 3 (3) | | ns |
| | | | ACLKX/AFSX (In Sync Mode), ACLKR/AFSR (In Async Mode), and AXR are all inputs "80M" Virtual IO Timing Modes | 0.38R (3) | | ns |
| 5 | $t_{su(AFSRX-ACLK)}$ | Setup time, AFSR/X input valid before ACLKR/X | ACLKR/X int | 20.7 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 3.9 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes | 3 | | ns |

### Table 7-50. Timing Requirements for McASP2 (1) (continued)

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 6 | $t_{h(ACLK-AFSRX)}$ | Hold time, AFSR/X input valid after ACLKR/X | ACLKR/X int | -1 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 3.2 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes | 3 | | ns |
| 7 | $t_{su(AXR-ACLK)}$ | Setup time, AXR input valid before ACLKR/X | ACLKR/X int | 21.4 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 3.9 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes | 3 | | ns |
| 8 | $t_{h(ACLK-AXR)}$ | Hold time, AXR input valid after ACLKR/X | ACLKR/X int | -1 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 3.2 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes | 3 | | ns |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKR/X period in ns.

(3) R = ACLKR/X period in ns.

### Table 7-51. Timing Requirements for McASP3/4/5/6/7/8 (1)

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 20 | | ns |
| 2 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | 0.35P (2) | | ns |
| 3 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | | 20 | | ns |
| 4 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/X high or low | | 0.5R - 3 (3) | | ns |
| 5 | $t_{su(AFSRX-ACLK)}$ | Setup time, AFSR/X input valid before ACLKR/X | ACLKR/X int | 20.2 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 4.9 | | ns |
| 6 | $t_{h(ACLK-AFSRX)}$ | Hold time, AFSR/X input valid after ACLKR/X | ACLKR/X int | -1 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 2.26 | | ns |
| | $t_{su(AXR-ACLK)}$ | Setup time, AXR input valid before ACLKX | ACLKX int (ASYNC=0) | 20.8 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 5.75 | | ns |
| 8 | $t_{h(ACLK-AXR)}$ | Hold time, AXR input valid after ACLKX | ACLKX int (ASYNC=0) | -0.9 | | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 2.87 | | ns |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1 (NOT SUPPORTED)
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKR/X period in ns.


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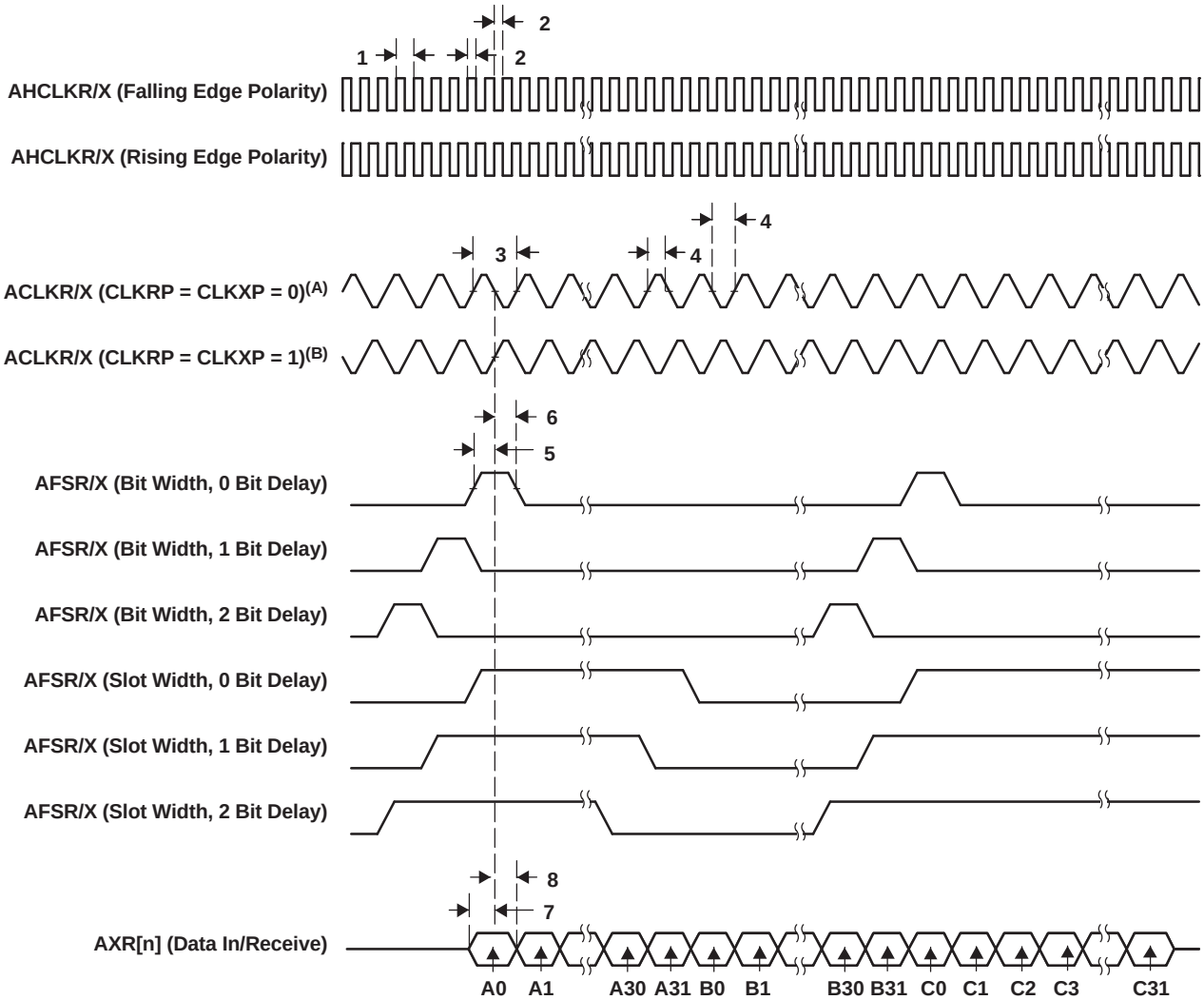
(3) R = ACLKR/X period in ns.




A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

**Figure 7-41. McASP Input Timing**

**CAUTION**

The IO Timings provided in this section are only valid for some McASP usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-52, Table 7-53, Table 7-54 and Figure 7-42 present Switching Characteristics Over Recommended Operating Conditions for McASP1 to McASP8.

**Table 7-52. Switching Characteristics Over Recommended Operating Conditions for McASP1 (1)**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 9 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 20 | | ns |

### Table 7-52. Switching Characteristics Over Recommended Operating Conditions for McASP1 [(1)] (continued)

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 10 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | 0.5P - 2.5 [(2)] | | ns |
| 11 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | | 20 | | ns |
| 12 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/X high or low | | 0.5P - 2.5 [(3)] | | ns |
| 13 | $t_{d(ACLK-AFSXR)}$ | Delay time, ACLKR/X transmit edge to AFSX/R output valid | ACLKR/X int | -0.21 | 6 | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 2 | 23.9 | ns |
| 14 | $t_{d(ACLK-AXR)}$ | Delay time, ACLKR/X transmit edge to AXR output valid | ACLKR/X int | -1.8 | 6.9 | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 2 | 25.6 | ns |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKR/X period in ns.

(3) R = ACLKR/X period in ns.

### Table 7-53. Switching Characteristics Over Recommended Operating Conditions for McASP2 [(1)]

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 9 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 20 | | ns |
| 10 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | 0.5P - 2.5 [(2)] | | ns |
| 11 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | | 20 | | ns |
| 12 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/X high or low | | 0.5P - 2.5 [(3)] | | ns |
| 13 | $t_{d(ACLK-AFSXR)}$ | Delay time, ACLKR/X transmit edge to AFSX/R output valid | ACLKR/X int | 0 | 6 | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 2 | 25.2 | ns |
| 14 | $t_{d(ACLK-AXR)}$ | Delay time, ACLKR/X transmit edge to AXR output valid | ACLKR/X int | -1.29 | 6.11 | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 2 | 24.8 | ns |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKR/X period in ns.

(3) R = ACLKR/X period in ns.

### Table 7-54. Switching Characteristics Over Recommended Operating Conditions for McASP3/4/5/6/7/8 [(1)]

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 9 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 20 | | ns |
| 10 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | 0.5P - 2.5 [(2)] | | ns |
| 11 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | | 20 | | ns |
| 12 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/X high or low | | 0.5P - 2.5 [(3)] | | ns |


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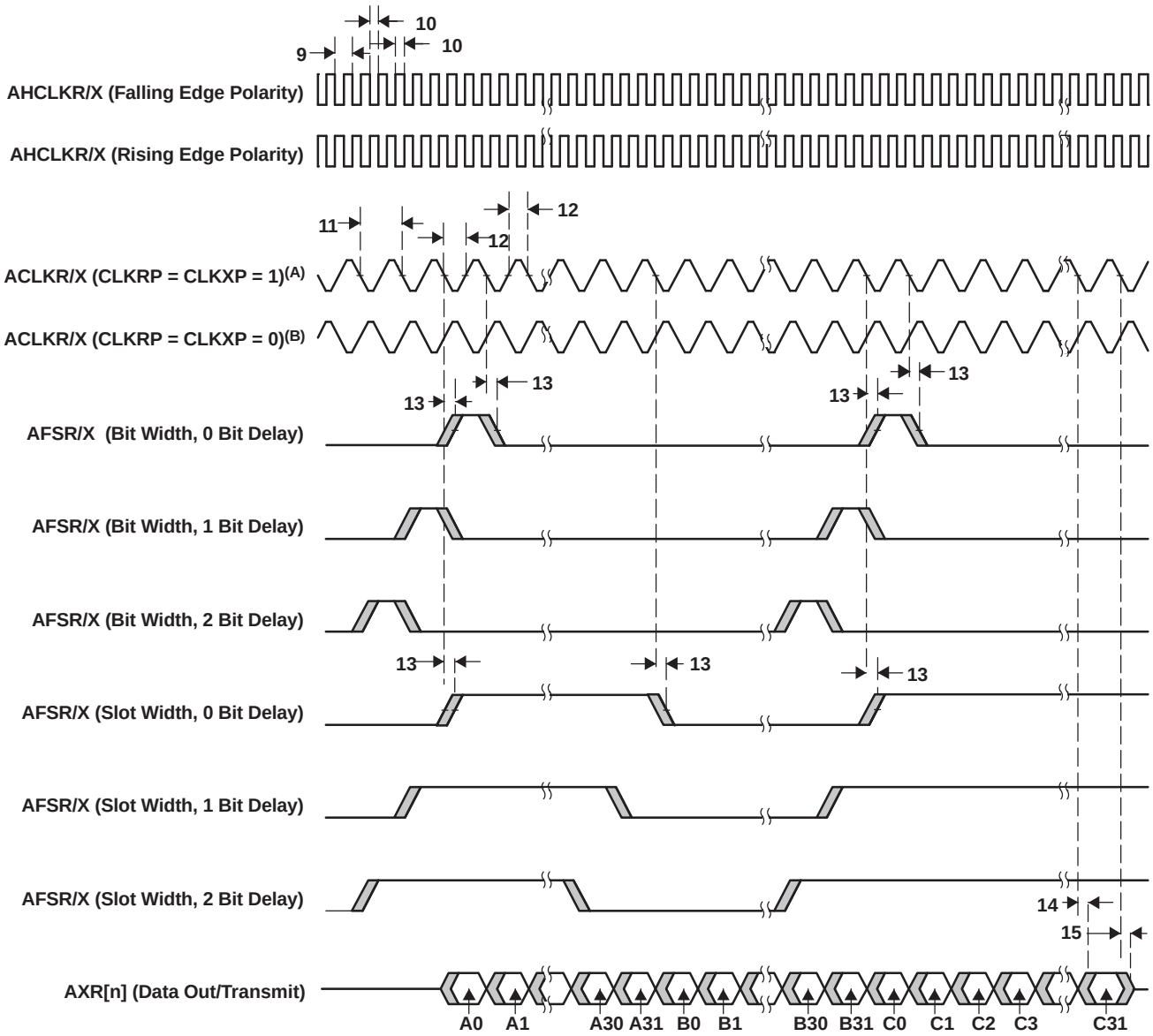
**Table 7-54. Switching Characteristics Over Recommended Operating Conditions for McASP3/4/5/6/7/8 [(1)] (continued)**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 13 | $t_{d(ACLK-AFSXR)}$ | Delay time, ACLKR/X transmit edge to AFSX/R output valid | ACLKR/X int | -0.74 | 6 | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 2 | 26.4 | ns |
| 14 | $t_{d(ACLK-AXR)}$ | Delay time, ACLKR/X transmit edge to AXR output valid | ACLKR/X int | -1.68 | 6.97 | ns |
| | | | ACLKR/X ext in ACLKR/X ext out | 1.07 | 25.9 | ns |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKR/X period in ns.

(3) R = ACLKR/X period in ns.




A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

**Figure 7-42. McASP Output Timing**

---

**NOTE**

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented in Table 4-3 and described in Device TRM, *Chapter 18 - Control Module*.

---

Table 7-55 through Table 7-62 explain all cases with Virtual Mode Details for McASP1/2/3/4/5/6/7/8 (see Figure 7-43 through Figure 7-50).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### Table 7-55. Virtual Mode Case Details for McASP1

| No. | CASE | CASE Description | Virtual Mode Settings | | Notes |
|---|---|---|---|---|---|
| | | | Signals | Virtual Mode Value | |
| **IP Mode : ASYNC** | | | | | |
| 1 | COIFOI | CLKX / FSX: Output CLKR / FSR: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-43 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP1_VIRTUAL3_ASYNC_RX | |
| 2 | COIFIO | CLKX / FSR: Output CLKR / FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-44 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP1_VIRTUAL3_ASYNC_RX | |
| 3 | CIOFIO | CLKR / FSR: Output CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP1_VIRTUAL3_ASYNC_RX | See Figure 7-45 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP1_VIRTUAL1_ASYNC_TX | |
| 4 | CIOFOI | CLKR / FSX: Output CLKX / FSR: Input | AXR(Outputs)/CLKX/FSX | MCASP1_VIRTUAL3_ASYNC_RX | See Figure 7-46 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP1_VIRTUAL1_ASYNC_TX | |
| **IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)** | | | | | |
| 5 | CO-FO- | CLKX / FSX: Output | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-47 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |
| 6 | CI-FO- | FSX: Output CLKX: Input | AXR(Outputs)/CLKX/FSX | MCASP1_VIRTUAL2_SYNC_RX | See Figure 7-48 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP1_VIRTUAL2_SYNC_RX | |
| 7 | CI-FI- | CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP1_VIRTUAL2_SYNC_RX | See Figure 7-49 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP1_VIRTUAL2_SYNC_RX | |
| 8 | CO-FI- | CLKX: Output FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-50 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |

### Table 7-56. Virtual Mode Case Details for McASP2

| No. | CASE | CASE Description | Virtual Mode Settings | | Notes |
|---|---|---|---|---|---|
| | | | Signals | Virtual Mode Value | |
| **IP Mode : ASYNC** | | | | | |
| 1 | COIFOI | CLKX / FSX: Output CLKR / FSR: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode)(1) | See Figure 7-43 |
| | | | AXR(Inputs)/CLKR/FSR | Default (No Virtual Mode)(1) | |
| | | | AXR(Inputs)/CLKR/FSR | MCASP2_VIRTUAL4_ASYNC_RX_80M (2) | |
| 2 | COIFIO | CLKX / FSR: Output CLKR / FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-44 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP2_VIRTUAL2_ASYNC_RX | |
| 3 | CIOFIO | CLKR / FSR: Output CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP2_VIRTUAL2_ASYNC_RX | See Figure 7-45 |
| | | | AXR(Inputs)/CLKR/FSR | Default (No Virtual Mode) | |
| 4 | CIOFOI | CLKR / FSX: Output CLKX / FSR: Input | AXR(Outputs)/CLKX/FSX | MCASP2_VIRTUAL2_ASYNC_RX | See Figure 7-46 |
| | | | AXR(Inputs)/CLKR/FSR | Default (No Virtual Mode) | |
| **IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)** | | | | | |
| 5 | CO-FO- | CLKX / FSX: Output | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-47 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |
| 6 | CI-FO- | FSX: Output CLKX: Input | AXR(Outputs)/CLKX/FSX | MCASP2_VIRTUAL3_SYNC_RX | See Figure 7-48 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP2_VIRTUAL3_SYNC_RX | |
| 7 | CI-FI- | CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP2_VIRTUAL3_SYNC_RX(1) | See Figure 7-49 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP2_VIRTUAL3_SYNC_RX(1) | |
| | | | AXR(Inputs)/CLKX/FSX | MCASP2_VIRTUAL1_SYNC_RX_80M(2) | |
| 8 | CO-FI- | CLKX: Output FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-50 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |

(1) Used up to 50MHz. Should also be used in a CI-FI- mixed case where AXR operate as both inputs and outputs (that is, AXR are bidirectional).

(2) Used in 80MHz input only mode when AXR, CLKX and FSX are all inputs.

### Table 7-57. Virtual Mode Case Details for McASP3

| No. | CASE | CASE Description | Virtual Mode Settings | | Notes |
|---|---|---|---|---|---|
| | | | Signals | Virtual Mode Value | |
| **IP Mode : ASYNC** | | | | | |
| 1 | COIFOI | CLKX / FSX: Output<br>CLKR / FSR: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-43 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP3_VIRTUAL2_SYNC_RX | |
| 2 | COIFIO | CLKX / FSR: Output<br>CLKR / FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-44 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP3_VIRTUAL2_SYNC_RX | |
| 3 | CIOFIO | CLKR / FSR: Output<br>CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP3_VIRTUAL2_SYNC_RX | See Figure 7-45 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP3_VIRTUAL2_SYNC_RX | |
| 4 | CIOFOI | CLKR / FSX: Output<br>CLKX / FSR: Input | AXR(Outputs)/CLKX/FSX | MCASP3_VIRTUAL2_SYNC_RX | See Figure 7-46 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP3_VIRTUAL2_SYNC_RX | |
| **IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)** | | | | | |
| 5 | CO-FO- | CLKX / FSX: Output | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-47 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |
| 6 | CI-FO- | FSX: Output CLKX: Input | AXR(Outputs)/CLKX/FSX | MCASP3_VIRTUAL2_SYNC_RX | See Figure 7-48 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP3_VIRTUAL2_SYNC_RX | |
| 7 | CI-FI- | CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP3_VIRTUAL2_SYNC_RX | See Figure 7-49 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP3_VIRTUAL2_SYNC_RX | |
| 8 | CO-FI- | CLKX: Output FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-50 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |

### Table 7-58. Virtual Mode Case Details for McASP4

| No. | CASE | CASE Description | Virtual Mode Settings | | Notes |
|---|---|---|---|---|---|
| | | | Signals | Virtual Mode Value | |
| **IP Mode : ASYNC** | | | | | |
| 1 | COIFOI | CLKX / FSX: Output<br>CLKR / FSR: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-43 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP4_VIRTUAL1_SYNC_RX | |
| 2 | COIFIO | CLKX / FSR: Output<br>CLKR / FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-44 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP4_VIRTUAL1_SYNC_RX | |
| 3 | CIOFIO | CLKR / FSR: Output<br>CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP4_VIRTUAL1_SYNC_RX | See Figure 7-45 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP4_VIRTUAL1_SYNC_RX | |
| 4 | CIOFOI | CLKR / FSX: Output<br>CLKX / FSR: Input | AXR(Outputs)/CLKX/FSX | MCASP4_VIRTUAL1_SYNC_RX | See Figure 7-46 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP4_VIRTUAL1_SYNC_RX | |
| **IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)** | | | | | |
| 5 | CO-FO- | CLKX / FSX: Output | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-47 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |
| 6 | CI-FO- | FSX: Output CLKX: Input | AXR(Outputs)/CLKX/FSX | MCASP4_VIRTUAL1_SYNC_RX | See Figure 7-48 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP4_VIRTUAL1_SYNC_RX | |
| 7 | CI-FI- | CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP4_VIRTUAL1_SYNC_RX | See Figure 7-49 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP4_VIRTUAL1_SYNC_RX | |
| 8 | CO-FI- | CLKX: Output FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-50 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |


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### Table 7-59. Virtual Mode Case Details for McASP5

| No. | CASE | CASE Description | Virtual Mode Settings | | Notes |
|---|---|---|---|---|---|
| | | | Signals | Virtual Mode Value | |
| **IP Mode : ASYNC** | | | | | |
| 1 | COIFOI | CLKX / FSX: Output<br>CLKR / FSR: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-43 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP5_VIRTUAL1_SYNC_RX | |
| 2 | COIFIO | CLKX / FSR: Output<br>CLKR / FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-44 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP5_VIRTUAL1_SYNC_RX | |
| 3 | CIOFIO | CLKR / FSR: Output<br>CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP5_VIRTUAL1_SYNC_RX | See Figure 7-45 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP5_VIRTUAL1_SYNC_RX | |
| 4 | CIOFOI | CLKR / FSX: Output<br>CLKX / FSR: Input | AXR(Outputs)/CLKX/FSX | MCASP5_VIRTUAL1_SYNC_RX | See Figure 7-46 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP5_VIRTUAL1_SYNC_RX | |
| **IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)** | | | | | |
| 5 | CO-FO- | CLKX / FSX: Output | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-47 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |
| 6 | CI-FO- | FSX: Output CLKX: Input | AXR(Outputs)/CLKX/FSX | MCASP5_VIRTUAL1_SYNC_RX | See Figure 7-48 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP5_VIRTUAL1_SYNC_RX | |
| 7 | CI-FI- | CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP5_VIRTUAL1_SYNC_RX | See Figure 7-49 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP5_VIRTUAL1_SYNC_RX | |
| 8 | CO-FI- | CLKX: Output FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-50 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |

### Table 7-60. Virtual Mode Case Details for McASP6

| No. | CASE | CASE Description | Virtual Mode Settings | | Notes |
|---|---|---|---|---|---|
| | | | Signals | Virtual Mode Value | |
| **IP Mode : ASYNC** | | | | | |
| 1 | COIFOI | CLKX / FSX: Output<br>CLKR / FSR: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-43 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP6_VIRTUAL1_SYNC_RX | |
| 2 | COIFIO | CLKX / FSR: Output<br>CLKR / FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-44 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP6_VIRTUAL1_SYNC_RX | |
| 3 | CIOFIO | CLKR / FSR: Output<br>CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP6_VIRTUAL1_SYNC_RX | See Figure 7-45 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP6_VIRTUAL1_SYNC_RX | |
| 4 | CIOFOI | CLKR / FSX: Output<br>CLKX / FSR: Input | AXR(Outputs)/CLKX/FSX | MCASP6_VIRTUAL1_SYNC_RX | See Figure 7-46 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP6_VIRTUAL1_SYNC_RX | |
| **IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)** | | | | | |
| 5 | CO-FO- | CLKX / FSX: Output | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-47 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |
| 6 | CI-FO- | FSX: Output CLKX: Input | AXR(Outputs)/CLKX/FSX | MCASP6_VIRTUAL1_SYNC_RX | See Figure 7-48 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP6_VIRTUAL1_SYNC_RX | |
| 7 | CI-FI- | CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP6_VIRTUAL1_SYNC_RX | See Figure 7-49 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP6_VIRTUAL1_SYNC_RX | |
| 8 | CO-FI- | CLKX: Output FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-50 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |

### Table 7-61. Virtual Mode Case Details for McASP7

| No. | CASE | CASE Description | Virtual Mode Settings | | Notes |
|---|---|---|---|---|---|
| | | | Signals | Virtual Mode Value | |
| **IP Mode : ASYNC** | | | | | |
| 1 | COIFOI | CLKX / FSX: Output CLKR / FSR: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-43 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP7_VIRTUAL2_SYNC_RX | |
| 2 | COIFIO | CLKX / FSR: Output CLKR / FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-44 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP7_VIRTUAL2_SYNC_RX | |
| 3 | CIOFIO | CLKR / FSR: Output CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP7_VIRTUAL2_SYNC_RX | See Figure 7-45 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP7_VIRTUAL2_SYNC_RX | |
| 4 | CIOFOI | CLKR / FSX: Output CLKX / FSR: Input | AXR(Outputs)/CLKX/FSX | MCASP7_VIRTUAL2_SYNC_RX | See Figure 7-46 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP7_VIRTUAL2_SYNC_RX | |
| **IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)** | | | | | |
| 5 | CO-FO- | CLKX / FSX: Output | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-47 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |
| 6 | CI-FO- | FSX: Output CLKX: Input | AXR(Outputs)/CLKX/FSX | MCASP7_VIRTUAL2_SYNC_RX | See Figure 7-48 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP7_VIRTUAL2_SYNC_RX | |
| 7 | CI-FI- | CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP7_VIRTUAL2_SYNC_RX | See Figure 7-49 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP7_VIRTUAL2_SYNC_RX | |
| 8 | CO-FI- | CLKX: Output FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-50 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |

### Table 7-62. Virtual Mode Case Details for McASP8

| No. | CASE | CASE Description | Virtual Mode Settings | | Notes |
|---|---|---|---|---|---|
| | | | Signals | Virtual Mode Value | |
| **IP Mode : ASYNC** | | | | | |
| 1 | COIFOI | CLKX / FSX: Output CLKR / FSR: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-43 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP8_VIRTUAL1_SYNC_RX | |
| 2 | COIFIO | CLKX / FSR: Output CLKR / FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-44 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP8_VIRTUAL1_SYNC_RX | |
| 3 | CIOFIO | CLKR / FSR: Output CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP8_VIRTUAL1_SYNC_RX | See Figure 7-45 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP8_VIRTUAL1_SYNC_RX | |
| 4 | CIOFOI | CLKR / FSX: Output CLKX / FSR: Input | AXR(Outputs)/CLKX/FSX | MCASP8_VIRTUAL1_SYNC_RX | See Figure 7-46 |
| | | | AXR(Inputs)/CLKR/FSR | MCASP8_VIRTUAL1_SYNC_RX | |
| **IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)** | | | | | |
| 5 | CO-FO- | CLKX / FSX: Output | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-47 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |
| 6 | CI-FO- | FSX: Output CLKX: Input | AXR(Outputs)/CLKX/FSX | MCASP8_VIRTUAL1_SYNC_RX | See Figure 7-48 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP8_VIRTUAL1_SYNC_RX | |
| 7 | CI-FI- | CLKX / FSX: Input | AXR(Outputs)/CLKX/FSX | MCASP8_VIRTUAL1_SYNC_RX | See Figure 7-49 |
| | | | AXR(Inputs)/CLKX/FSX | MCASP8_VIRTUAL1_SYNC_RX | |
| 8 | CO-FI- | CLKX: Output FSX: Input | AXR(Outputs)/CLKX/FSX | Default (No Virtual Mode) | See Figure 7-50 |
| | | | AXR(Inputs)/CLKX/FSX | Default (No Virtual Mode) | |


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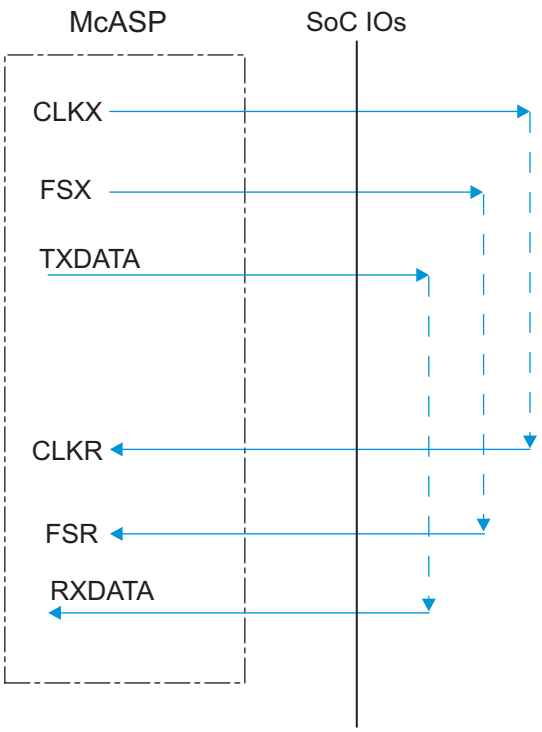


**Figure 7-43. McASP1-8 COIFOI – ASYNC Mode**

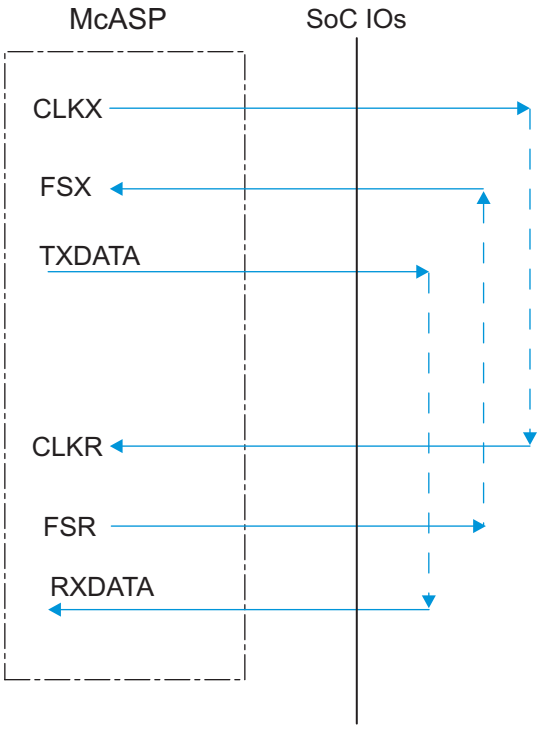


**Figure 7-44. McASP1-8 COIFIO – ASYNC Mode**

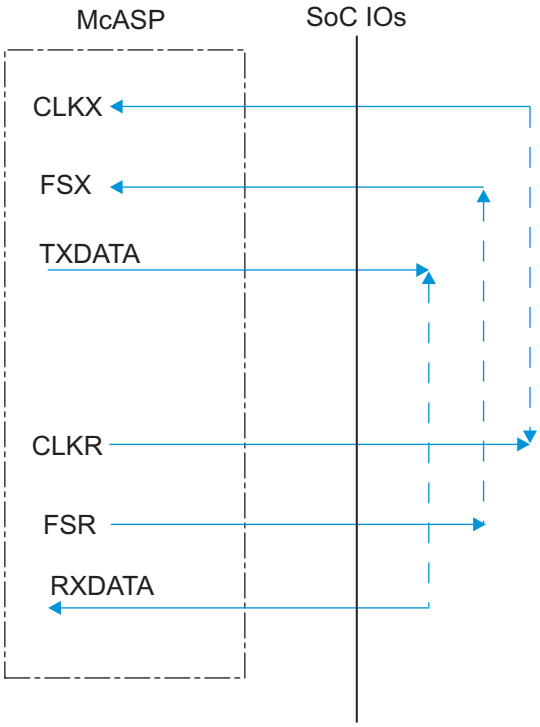


**Figure 7-45. McASP1-8 CIOFIO – ASYNC Mode**

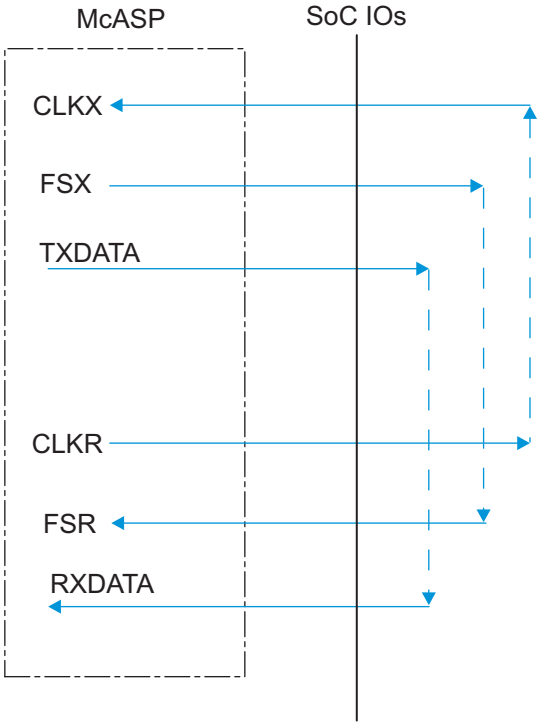


**Figure 7-46. McASP1-8 CIOFOI – ASYNC Mode**


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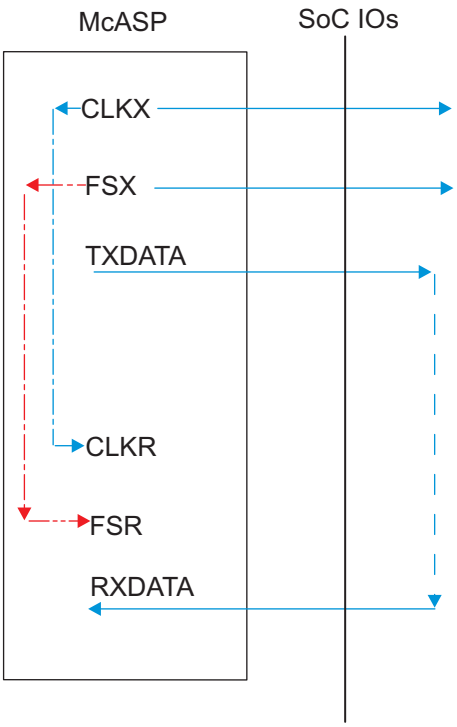


**Figure 7-47. McASP1-8 CO-FO- – SYNC Mode**

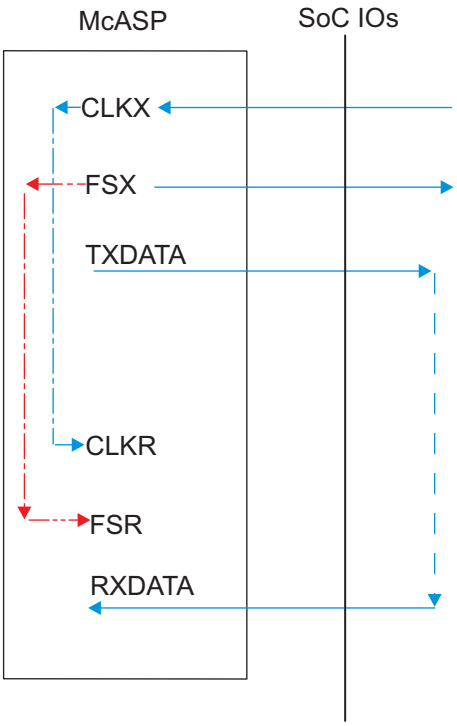


**Figure 7-48. McASP1-8 CI-FO- – SYNC Mode**

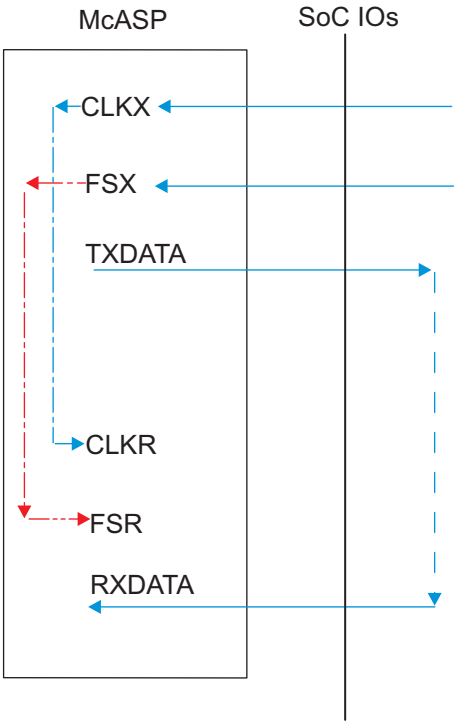


**Figure 7-49. McASP1-8 CI-FI- – SYNC Mode**

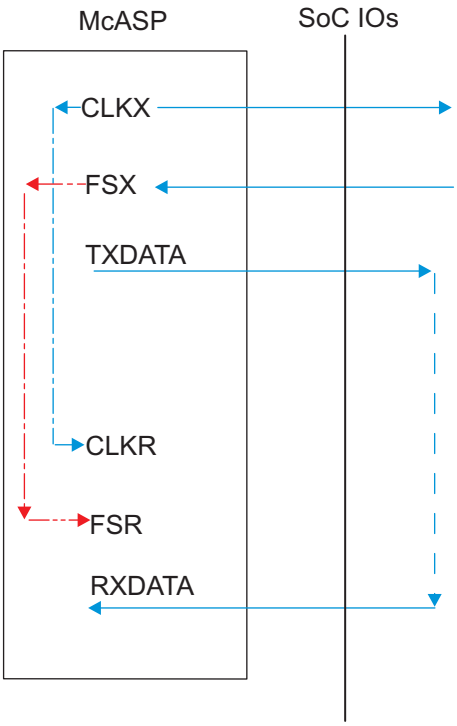


**Figure 7-50. McASP1-8 CO-FI- – SYNC Mode**

Virtual IO Timings Modes must be used to ensure some IO timings for McASP1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 7-63 *Virtual Functions Mapping for McASP1* for a definition of the Virtual modes.

Table 7-63 presents the values for DELAYMODE bitfield.


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**Table 7-63. Virtual Functions Mapping for McASP1**

| BALL | BALL NAME | Delay Mode Value | | | MUXMODE[15:0] | | |
|---|---|---|---|---|---|---|---|
| | | MCASP1_VIRTUAL1_ASYNC_TX | MCASP1_VIRTUAL2_SYNC_RX | MCASP1_VIRTUAL3_ASYNC_RX | 0 | 1 | 2 |
| E21 | gpio6_14 | 11 | 15 | 14 | | mcasp1_axr8 | |
| F20 | gpio6_15 | 11 | 15 | 14 | | mcasp1_axr9 | |
| F21 | gpio6_16 | 11 | 15 | 14 | | mcasp1_axr10 | |
| D18 | xref_clk0 | 0 | 15 | 14 | | | mcasp1_axr4 |
| E17 | xref_clk1 | 0 | 15 | 14 | | | mcasp1_axr5 |
| B26 | xref_clk2 | 5 | 15 | 14 | | | mcasp1_axr6 |
| C23 | xref_clk3 | 5 | 15 | 14 | | | mcasp1_axr7 |
| C14 | mcasp1_aclkx | 8 | 15 | 14 | mcasp1_aclkx | | |
| D14 | mcasp1_fsx | 12 | 15 | 14 | mcasp1_fsx | | |
| B14 | mcasp1_aclkr | 11 | N/A | 15 | mcasp1_aclkr | | |
| J14 | mcasp1_fsr | 11 | N/A | 15 | mcasp1_fsr | | |
| G12 | mcasp1_axr0 | 8 | 15 | 14 | mcasp1_axr0 | | |
| F12 | mcasp1_axr1 | 8 | 15 | 14 | mcasp1_axr1 | | |
| G13 | mcasp1_axr2 | 10 | 15 | 14 | mcasp1_axr2 | | |
| J11 | mcasp1_axr3 | 10 | 15 | 14 | mcasp1_axr3 | | |
| E12 | mcasp1_axr4 | 10 | 15 | 14 | mcasp1_axr4 | | |
| F13 | mcasp1_axr5 | 10 | 15 | 14 | mcasp1_axr5 | | |
| C12 | mcasp1_axr6 | 10 | 15 | 14 | mcasp1_axr6 | | |
| D12 | mcasp1_axr7 | 10 | 15 | 14 | mcasp1_axr7 | | |
| B12 | mcasp1_axr8 | 6 | 15 | 14 | mcasp1_axr8 | | |
| A11 | mcasp1_axr9 | 6 | 15 | 14 | mcasp1_axr9 | | |
| B13 | mcasp1_axr10 | 6 | 15 | 14 | mcasp1_axr10 | | |
| A12 | mcasp1_axr11 | 6 | 15 | 14 | mcasp1_axr11 | | |
| E14 | mcasp1_axr12 | 6 | 15 | 14 | mcasp1_axr12 | | |
| A13 | mcasp1_axr13 | 6 | 15 | 14 | mcasp1_axr13 | | |
| G14 | mcasp1_axr14 | 6 | 15 | 14 | mcasp1_axr14 | | |
| F14 | mcasp1_axr15 | 6 | 15 | 14 | mcasp1_axr15 | | |

1. NA in this table stands for Not Applicable.

Virtual IO Timings Modes must be used to ensure some IO timings for McASP2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 7-64 *Virtual Functions Mapping for McASP2* for a definition of the Virtual modes.

Table 7-64 presents the values for DELAYMODE bitfield.

**Table 7-64. Virtual Functions Mapping for McASP2**

| BALL | BALL NAME | Delay Mode Value | | | | | MUXMODE[15:0] | | |
|---|---|---|---|---|---|---|---|---|---|
| | | MCASP2_VIRTUAL1_ASYNC_RX_80M | MCASP2_VIRTUAL2_ASYNC_RX | MCASP2_VIRTUAL3_ASYNC_TX | MCASP2_VIRTUAL4_SYNC_RX | MCASP2_VIRTUAL5_SYNC_RX_80M | 0 | 1 | 2 |
| D18 | xref_clk0 | 10 | 9 | 4 | 8 | 6 | | mcasp2_axr8 | |
| E17 | xref_clk1 | 10 | 9 | 4 | 8 | 6 | | mcasp2_axr9 | |
| B26 | xref_clk2 | 13 | 12 | 0 | 11 | 10 | | mcasp2_axr10 | |
| C23 | xref_clk3 | 13 | 12 | 0 | 11 | 10 | | mcasp2_axr11 | |
| A19 | mcasp2_aclkx | 15 | 14 | 5 | 10 | 9 | mcasp2_aclkx | | |
| A18 | mcasp2_fsx | 15 | 14 | 5 | 10 | 9 | mcasp2_fsx | | |
| E15 | mcasp2_aclkr | 15 | 14 | 10 | N/A | N/A | mcasp2_aclkr | | |
| A20 | mcasp2_fsr | 15 | 14 | 10 | N/A | N/A | mcasp2_fsr | | |
| B15 | mcasp2_axr0 | 15 | 14 | 9 | 13 | 12 | mcasp2_axr0 | | |
| A15 | mcasp2_axr1 | 15 | 14 | 9 | 13 | 12 | mcasp2_axr1 | | |
| C15 | mcasp2_axr2 | 15 | 14 | 4 | 10 | 9 | mcasp2_axr2 | | |
| A16 | mcasp2_axr3 | 15 | 14 | 4 | 10 | 9 | mcasp2_axr3 | | |
| D15 | mcasp2_axr4 | 15 | 14 | 7 | 13 | 12 | mcasp2_axr4 | | |
| B16 | mcasp2_axr5 | 15 | 14 | 7 | 13 | 12 | mcasp2_axr5 | | |
| B17 | mcasp2_axr6 | 15 | 14 | 7 | 13 | 12 | mcasp2_axr6 | | |
| A17 | mcasp2_axr7 | 15 | 14 | 7 | 13 | 12 | mcasp2_axr7 | | |
| B18 | mcasp3_aclkx | 15 | 14 | 5 | 10 | 9 | | | mcasp2_axr12 |
| F15 | mcasp3_fsx | 15 | 14 | 4 | 10 | 9 | | | mcasp2_axr13 |
| B19 | mcasp3_axr0 | 15 | 14 | 4 | 10 | 9 | | | mcasp2_axr14 |
| C17 | mcasp3_axr1 | 15 | 14 | 3 | 10 | 8 | | | mcasp2_axr15 |

1. NA in this table stands for Not Applicable.

Virtual IO Timings Modes must be used to ensure some IO timings for McASP3/4/5/6/7/8. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 7-65 *Virtual Functions Mapping for McASP3/4/5/6/7/8* for a definition of the Virtual modes.

Table 7-65 presents the values for DELAYMODE bitfield.


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### Table 7-65. Virtual Functions Mapping for McASP3/4/5/6/7/8

| BALL NUMBER | BALL NAME | Delay Mode Value | MUXMODE[15:0] | | |
|---|---|---|---|---|---|
| | | | 0 | 1 | 2 |
| **MCASP3_VIRTUAL2_SYNC_RX** | | | | | |
| C15 | mcasp2_axr2 | 8 | | mcasp3_axr2 | |
| A16 | mcasp2_axr3 | 8 | | mcasp3_axr3 | |
| B18 | mcasp3_aclkx | 8 | mcasp3_aclkx | mcasp3_aclkr | |
| F15 | mcasp3_fsx | 8 | mcasp3_fsx | mcasp3_fsr | |
| B19 | mcasp3_axr0 | 8 | mcasp3_axr0 | | |
| C17 | mcasp3_axr1 | 6 | mcasp3_axr1 | | |
| **MCASP4_VIRTUAL1_SYNC_RX** | | | | | |
| E12 | mcasp1_axr4 | 13 | | mcasp4_axr2 | |
| F13 | mcasp1_axr5 | 13 | | mcasp4_axr3 | |
| C18 | mcasp4_aclkx | 15 | mcasp4_aclkx | mcasp4_aclkr | |
| A21 | mcasp4_fsx | 15 | mcasp4_fsx | mcasp4_fsr | |
| G16 | mcasp4_axr0 | 15 | mcasp4_axr0 | | |
| D17 | mcasp4_axr1 | 15 | mcasp4_axr1 | | |
| **MCASP5_VIRTUAL1_SYNC_RX** | | | | | |
| C12 | mcasp1_axr6 | 13 | | mcasp5_axr2 | |
| D12 | mcasp1_axr7 | 13 | | mcasp5_axr3 | |
| AA3 | mcasp5_aclkx | 15 | mcasp5_aclkx | mcasp5_aclkr | |
| AB9 | mcasp5_fsx | 15 | mcasp5_fsx | mcasp5_fsr | |
| AB3 | mcasp5_axr0 | 15 | mcasp5_axr0 | | |
| AA4 | mcasp5_axr1 | 15 | mcasp5_axr1 | | |
| **MCASP6_VIRTUAL1_SYNC_RX** | | | | | |
| G13 | mcasp1_axr2 | 13 | | mcasp6_axr2 | |
| J11 | mcasp1_axr3 | 13 | | mcasp6_axr3 | |
| B12 | mcasp1_axr8 | 10 | | mcasp6_axr0 | |
| A11 | mcasp1_axr9 | 10 | | mcasp6_axr1 | |
| B13 | mcasp1_axr10 | 10 | | mcasp6_aclkx | mcasp6_aclkr |
| A12 | mcasp1_axr11 | 10 | | mcasp6_fsx | mcasp6_fsr |
| **MCASP7_VIRTUAL2_SYNC_RX** | | | | | |
| B14 | mcasp1_aclkr | 14 | | mcasp7_axr2 | |
| J14 | mcasp1_fsr | 14 | | mcasp7_axr3 | |
| E14 | mcasp1_axr12 | 10 | | mcasp7_axr0 | |

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### Table 7-65. Virtual Functions Mapping for McASP3/4/5/6/7/8 (continued)

| BALL NUMBER | BALL NAME | Delay Mode Value | MUXMODE[15:0] | | |
|---|---|---|---|---|---|
| | | | 0 | 1 | 2 |
| A13 | mcasp1_axr13 | 10 | | mcasp7_axr1 | |
| G14 | mcasp1_axr14 | 10 | | mcasp7_aclkx | mcasp7_aclkr |
| F14 | mcasp1_axr15 | 10 | | mcasp7_fsx | mcasp7_fsr |
| **MCASP8_VIRTUAL1_SYNC_RX** | | | | | |
| E15 | mcasp2_aclkr | 13 | | mcasp8_axr2 | |
| A20 | mcasp2_fsr | 13 | | mcasp8_axr3 | |
| D15 | mcasp2_axr4 | 11 | | mcasp8_axr0 | |
| B16 | mcasp2_axr5 | 11 | | mcasp8_axr1 | |
| B17 | mcasp2_axr6 | 11 | | mcasp8_aclkx | mcasp8_aclkr |
| A17 | mcasp2_axr7 | 11 | | mcasp8_fsx | mcasp8_fsr |


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## 7.18 Universal Serial Bus (USB)

SuperSpeed USB DRD Subsystem has two instances in the device providing the following functions:

- USB1: SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem with integrated SS (USB3.0) PHY and HS/FS (USB2.0) PHY.
- USB2: High-Speed (HS) USB 2.0 Dual-Role-Device (DRD) subsystem with integrated HS/FS PHY.

**NOTE**

For more information, see the SuperSpeed USB DRD section of the Device TRM.

### *7.18.1 USB1 DRD PHY*

The USB1 DRD interface supports the following applications:

- USB2.0 High-Speed PHY port (1.8 V and 3.3 V): this asynchronous high-speed interface is compliant with the USB2.0 PHY standard with an internal transceiver (USB2.0 standard v2.0), for a maximum data rate of 480 Mbps.
- USB3.0 Super-Speed PHY port (1.8 V): this asynchronous differential super-speed interface is compliant with the USB3.0 RX/TX PHY standard (USB3.0 standard v1.0) for a maximum data bit rate of 5Gbps.

### *7.18.2 USB2 PHY*

The USB2 interface supports the following applications:

- USB2.0 High-Speed PHY port (1.8 V and 3.3 V): this asynchronous high-speed interface is compliant with the USB2.0 PHY standard with an internal transceiver (USB2.0 standard v2.0), for a maximum data rate of 480 Mbps.

## 7.19 Serial Advanced Technology Attachment (SATA)

The SATA RX/TX PHY interface is compliant with the SATA standard v2.6 for a maximum data rate:

- Gen2i, Gen2m, Gen2x: 3Gbps.
- Gen1i, Gen1m, Gen1x: 1.5Gbps.

**NOTE**

For more information, see the SATA Controller section of the Device TRM.

## 7.20 Peripheral Component Interconnect Express (PCIe)

The device supports connections to PCIe-compliant devices via the integrated PCIe master/slave bus interface. The PCIe module is comprised of a dual-mode PCIe core and a SerDes PHY. Each PCIe subsystem controller has support for PCIe Gen-II mode (5 Gbps per lane) and Gen-I mode (2.5 Gbps per lane) (Single Lane and Flexible dual lane configuration).

The device PCIe supports the following features:

- 16-bit operation @250 MHz on PIPE interface (per 16-bit lane)
- Supports 2 ports x 1 lane or 1 port x 2 lanes configuration
- Single virtual channel (VC0), single traffic class (TC0)
- Single function in end-point mode
- Automatic width and speed negotiation
- Max payload: 128 byte outbound, 256 byte inbound
- Automatic credit management

- ECRC generation and checking
- Configurable BAR filtering
- Legacy interrupt reception (RC) and generation (EP)
- MSI generation and reception
- PCI Express Active State Power Management (ASPM) state L0s and L1 (with exceptions)
- All PCI Device Power Management D-states with the exception of $D3_{cold}$ / L2 state

The PCIe controller on this device conforms to the PCI Express Base 3.0 Specification, revision 1.0 and the PCI Local Bus Specification, revision 3.0.

**NOTE**
For more information, see the PCIe Controller section of the Device TRM.

## 7.21 Controller Area Network Interface (DCAN)

The device provides two DCAN interfaces for supporting distributed realtime control with a high level of security. The DCAN interfaces implement the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- 64 message objects
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Direct access to Message RAM during test mode
- CAN Rx/Tx pins are configurable as general-purpose IO pins
- Two interrupt lines (plus additional parity-error interrupts line)
- RAM initialization
- DMA support

**NOTE**
For more information, see the DCAN section of the Device TRM.

**NOTE**
The Controller Area Network Interface x (x = 1 to 2) is also referred to as DCANx.

**NOTE**
Refer to the CAN Specification for calculations necessary to validate timing compliance. Jitter tolerance calculations must be performed to validate the implementation.

Table 7-66 and Table 7-67 present timing and switching characteristics for DCANx Interface.

**Table 7-66. Timing Requirements for DCANx Receive**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| - | f(baud) | Maximum programmable baud rate | | 1 | Mbps |


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**Table 7-66. Timing Requirements for DCANx Receive (continued)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| - | $t_{d(DCANRX)}$ | Delay time, DCANx_RX pin to receive shift register | | 15 | ns |

**Table 7-67. Switching Characteristics Over Recommended Operating Conditions for DCANx Transmit**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| - | f(baud) | Maximum programmable baud rate | | 1 | Mbps |
| - | $t_{d(DCANTX)}$ | Delay time, Transmit shift register to DCANx_TX pin(1) | | 15 | ns |

(1) These values do not include rise/fall times of the output buffer.

## 7.22 Ethernet Interface (GMAC_SW)

The three-port gigabit ethernet switch subsystem (GMAC_SW) provides ethernet packet communication and can be configured as an ethernet switch. It provides the Gigabit Media Independent Interface (G/MII) in MII mode, Reduced Gigabit Media Independent Interface (RGMII), Reduced Media Independent Interface (RMII), and the Management Data Input/Output (MDIO) for physical layer device (PHY) management.

**NOTE**

For more information, see the Gigabit Ethernet Switch (GMAC_SW) section of the Device TRM.

**NOTE**

The Gigabit, Reduced and Media Independent Interface n (n = 0 to 1) are also referred to as MIIn, RMIIn and RGMIIn.

**CAUTION**

The IO timings provided in this section are only valid if signals within a single IOSET are used. The IOSETs are defined in the Table 7-72, Table 7-75, Table 7-80 and Table 7-87.

**CAUTION**

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-68 and Figure 7-51 present timing requirements for MIIn in receive operation.

### *7.22.1 GMAC MII Timings*

**Table 7-68. Timing Requirements for miin_rxclk - MII Operation**

| NO. | PARAMETER | DESCRIPTION | SPEED | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(RX_CLK)}$ | Cycle time, miin_rxclk | 10 Mbps | 400 | | ns |
| | | | 100 Mbps | 40 | | ns |
| 2 | $t_{w(RX_CLKH)}$ | Pulse duration, miin_rxclk high | 10 Mbps | 140 | 260 | ns |
| | | | 100 Mbps | 14 | 26 | ns |

**Table 7-68. Timing Requirements for miin_rxclk - MII Operation (continued)**

| NO. | PARAMETER | DESCRIPTION | SPEED | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 3 | $t_{w(RX_CLKL)}$ | Pulse duration, miin_rxclk low | 10 Mbps | 140 | 260 | ns |
| | | | 100 Mbps | 14 | 26 | ns |
| 4 | $t_{t(RX_CLK)}$ | Transition time, miin_rxclk | 10 Mbps | | 3 | ns |
| | | | 100 Mbps | | 3 | ns |

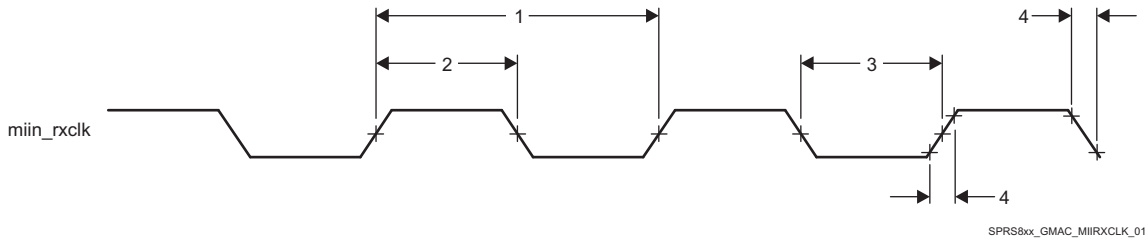


**Figure 7-51. Clock Timing (GMAC Receive) - MIIn operation**

Table 7-69 and Figure 7-52 present timing requirements for MIIn in transmit operation.

**Table 7-69. Timing Requirements for miin_txclk - MII Operation**

| NO. | PARAMETER | DESCRIPTION | SPEED | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(TX_CLK)}$ | Cycle time, miin_txclk | 10 Mbps | 400 | | ns |
| | | | 100 Mbps | 40 | | ns |
| 2 | $t_{w(TX_CLKH)}$ | Pulse duration, miin_txclk high | 10 Mbps | 140 | 260 | ns |
| | | | 100 Mbps | 14 | 26 | ns |
| 3 | $t_{w(TX_CLKL)}$ | Pulse duration, miin_txclk low | 10 Mbps | 140 | 260 | ns |
| | | | 100 Mbps | 14 | 26 | ns |
| 4 | $t_{t(TX_CLK)}$ | Transition time, miin_txclk | 10 Mbps | | 3 | ns |
| | | | 100 Mbps | | 3 | ns |

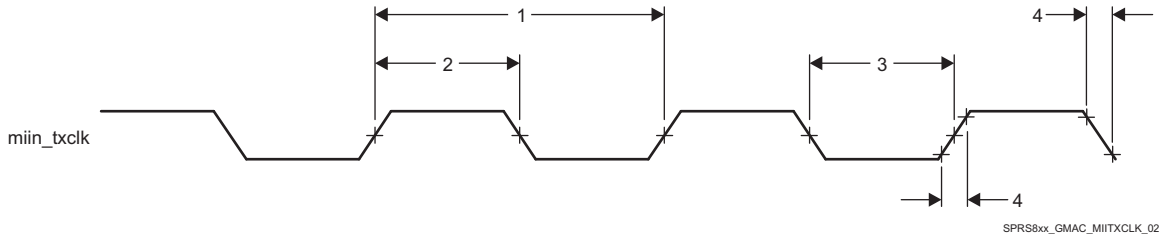


**Figure 7-52. Clock Timing (GMAC Transmit) - MIIn operation**

Table 7-70 and Figure 7-53 present timing requirements for GMAC MIIn Receive 10/100Mbit/s.

**Table 7-70. Timing Requirements for GMAC MIIn Receive 10/100 Mbit/s**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{su(RXD\text{-}RX_CLK)}$ | Setup time, receive selected signals valid before miin_rxclk | 8 | | ns |
| | $t_{su(RX_DV\text{-}RX_CLK)}$ | | | | |
| | $t_{su(RX_ER\text{-}RX_CLK)}$ | | | | |
| 2 | $t_{h(RX_CLK\text{-}RXD)}$ | Hold time, receive selected signals valid after miin_rxclk | 8 | | ns |
| | $t_{h(RX_CLK\text{-}RX_DV)}$ | | | | |
| | $t_{h(RX_CLK\text{-}RX_ER)}$ | | | | |


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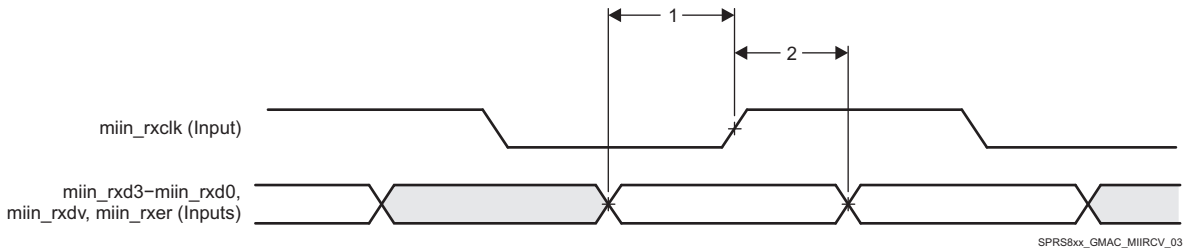


**Figure 7-53. GMAC Receive Interface Timing MIIn operation**

Table 7-71 and Figure 7-54 present timing requirements for GMAC MIIn Transmit 10/100Mbit/s.

**Table 7-71. Switching Characteristics Over Recommended Operating Conditions for GMAC MIIn Transmit 10/100 Mbits/s**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{d(TX_CLK-TXD)}$ | Delay time, miin_txclk to transmit selected signals valid | 0 | 25 | ns |
| | $t_{d(TX_CLK-TX_EN)}$ | | | | |
| | $t_{d(TX_CLK-TX_ER)}$ | | | | |

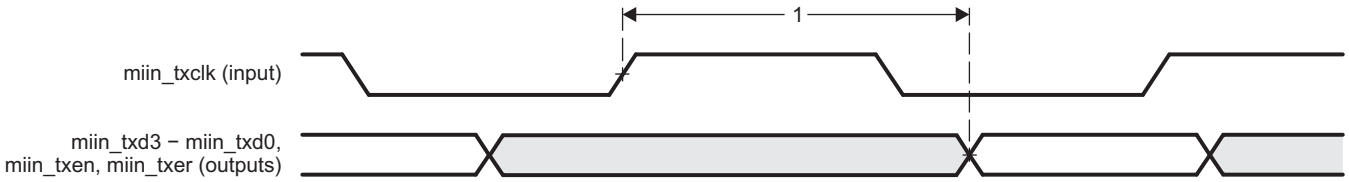


**Figure 7-54. GMAC Transmit Interface Timing MIIn operation**

In Table 7-72 are presented the specific groupings of signals (IOSET) for use with GMAC MII signals.

**Table 7-72. GMAC MII IOSETs**

| SIGNALS | IOSET5 | | IOSET6 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| **GMAC MII1** | | | | |
| mii1_txd3 | C5 | 8 | | |
| mii1_txd2 | D6 | 8 | | |
| mii1_txd1 | B2 | 8 | | |
| mii1_txd0 | C4 | 8 | | |
| mii1_rxd3 | F5 | 8 | | |
| mii1_rxd2 | E4 | 8 | | |
| mii1_rxd1 | C1 | 8 | | |
| mii1_rxd0 | E6 | 8 | | |
| mii1_col | B4 | 8 | | |
| mii1_rxer | B3 | 8 | | |
| mii1_txer | A3 | 8 | | |
| mii1_txen | A4 | 8 | | |
| mii1_crs | B5 | 8 | | |
| mii1_rxclk | D5 | 8 | | |
| mii1_txclk | C3 | 8 | | |
| mii1_rxdv | C2 | 8 | | |
| **GMAC MII0** | | | | |
| mii0_txd3 | | | V5 | 3 |

**Table 7-72. GMAC MII IOSETs (continued)**

| SIGNALS | IOSET5 | | IOSET6 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| mii0_txd2 | | | V4 | 3 |
| mii0_txd1 | | | Y2 | 3 |
| mii0_txd0 | | | W2 | 3 |
| mii0_rxd3 | | | W9 | 3 |
| mii0_rxd2 | | | V9 | 3 |
| mii0_rxd1 | | | V6 | 3 |
| mii0_rxd0 | | | U6 | 3 |
| mii0_txclk | | | U5 | 3 |
| mii0_txer | | | U4 | 3 |
| mii0_rxer | | | U7 | 3 |
| mii0_rxdv | | | V2 | 3 |
| mii0_crs | | | V7 | 3 |
| mii0_col | | | V1 | 3 |
| mii0_rxclk | | | Y1 | 3 |
| mii0_txen | | | V3 | 3 |

### *7.22.2 GMAC MDIO Interface Timings*

**CAUTION**

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-73, Table 7-73 and Figure 7-55 present timing requirements for MDIO.

**Table 7-73. Timing Requirements for MDIO Input**

| No | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| MDIO1 | $t_{c(MDC)}$ | Cycle time, MDC | 400 | | ns |
| MDIO2 | $t_{w(MDCH)}$ | Pulse Duration, MDC High | 160 | | ns |
| MDIO3 | $t_{w(MDCL)}$ | Pulse Duration, MDC Low | 160 | | ns |
| MDIO4 | $t_{su(MDIO-MDC)}$ | Setup time, MDIO valid before MDC High | 90 | | ns |
| MDIO5 | $t_{h(MDIO_MDC)}$ | Hold time, MDIO valid from MDC High | 0 | | ns |

**Table 7-74. Switching Characteristics Over Recommended Operating Conditions for MDIO Output**

| NO | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| MDIO6 | $t_{t(MDC)}$ | Transition time, MDC | | 5 | ns |
| MDIO7 | $t_{d(MDC-MDIO)}$ | Delay time, MDC low to MDIO valid | -150 | 150 | ns |


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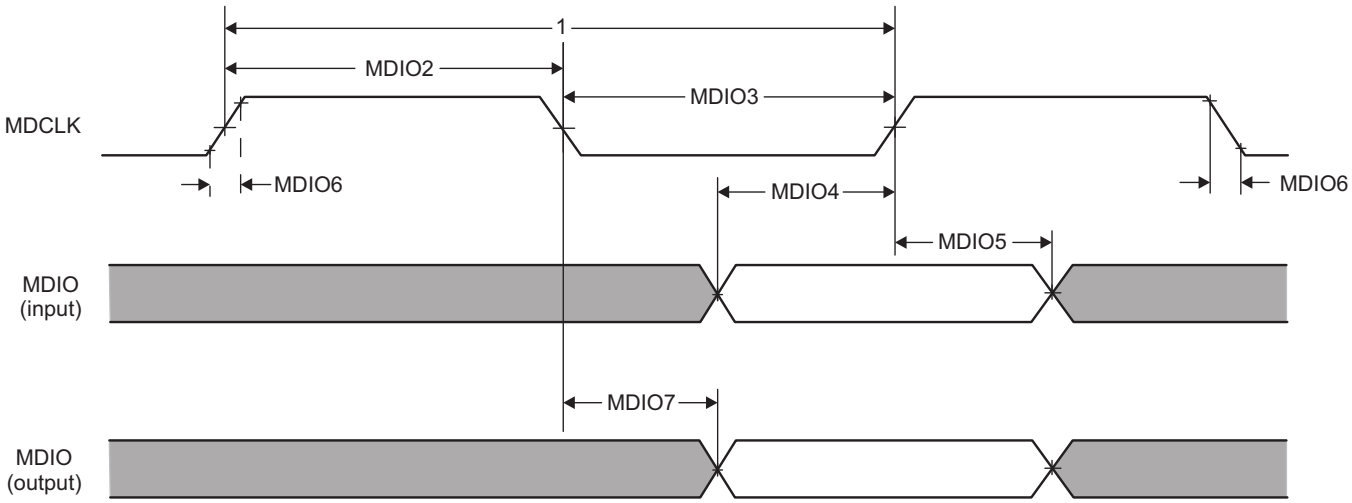


**Figure 7-55. GMAC MDIO diagrams**

In Table 7-75 are presented the specific groupings of signals (IOSET) for use with GMAC MDIO signals.

**Table 7-75. GMAC MDIO IOSETs**

| SIGNALS | IOSET7 | | IOSET8 | | IOSET9 | | IOSET10 | |
|---|---|---|---|---|---|---|---|---|
| | BALL | MUX | BALL | MUX | BALL | MUX | BALL | MUX |
| mdio_d | F6 | 3 | U4 | 0 | AB4 | 1 | B20 | 5 |
| mdio_mclk | D3 | 3 | V1 | 0 | AC5 | 1 | B21 | 5 |

### *7.22.3 GMAC RMII Timings*

The main reference clock REF_CLK (RMII_50MHZ_CLK) of RMII interface is internally supplied from PRCM. The source of this clock could be either externally sourced from the RMII_MHZ_50_CLK pin of the device or internally generated from DPLL_GMAC output clock GMAC_RMII_HS_CLK. See the PRCM chapter of the device TRM for full details about RMII reference clock.

**CAUTION**

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-76, Table 7-77 and Figure 7-56 present timing requirements for GMAC RMIIn Receive.

**Table 7-76. Timing Requirements for GMAC REF_CLK - RMII Operation**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| RMII1 | $t_{c(REF_CLK)}$ | Cycle time, REF_CLK | 20 | | ns |
| RMII2 | $t_{w(REF_CLKH)}$ | Pulse duration, REF_CLK high | 7 | 13 | ns |
| RMII3 | $t_{w(REF_CLKL)}$ | Pulse duration, REF_CLK low | 7 | 13 | ns |
| RMII4 | $t_{tt(REF_CLK)}$ | Transistion time, REF_CLK | | 3 | ns |

**Table 7-77. Timing Requirements for GMAC RMIIn Receive**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| RMII5 | $t_{su(RXD-REF_CLK)}$ | Setup time, receive selected signals valid before REF_CLK | 4 | | ns |
| | $t_{su(CRS_DV-REF_CLK)}$ | | | | |
| | $t_{su(RX_ER-REF_CLK)}$ | | | | |
| RMII6 | $t_{h(REF_CLK-RXD)}$ | Hold time, receive selected signals valid after REF_CLK | 2 | | ns |
| | $t_{h(REF_CLK-CRS_DV)}$ | | | | |
| | $t_{h(REF_CLK-RX_ER)}$ | | | | |

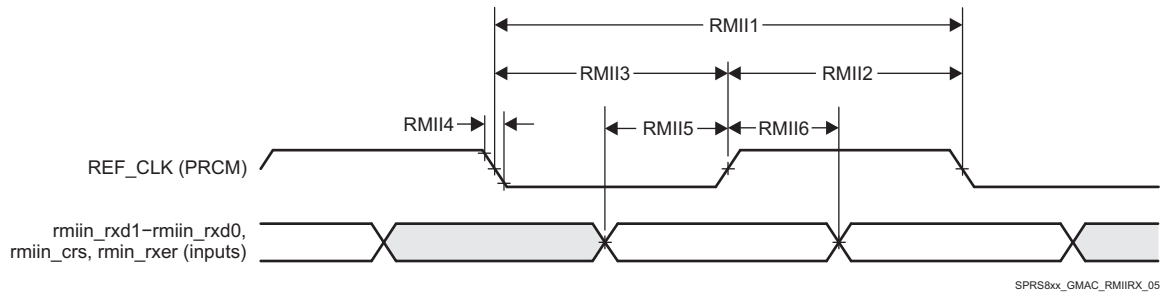


**Figure 7-56. GMAC Receive Interface Timing RMIIn operation**

Table 7-78, Table 7-78 and Figure 7-57 present switching characteristics for GMAC RMIIn Transmit 10/100Mbit/s.

**Table 7-78. Switching Characteristics Over Recommended Operating Conditions for GMAC REF_CLK - RMII Operation**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| RMII7 | $t_{c(REF_CLK)}$ | Cycle time, REF_CLK | 20 | | ns |
| RMII8 | $t_{w(REF_CLKH)}$ | Pulse duration, REF_CLK high | 7 | 13 | ns |
| RMII9 | $t_{w(REF_CLKL)}$ | Pulse duration, REF_CLK low | 7 | 13 | ns |
| RMII10 | $t_{t(REF_CLK)}$ | Transistion time, REF_CLK | | 3 | ns |

**Table 7-79. Switching Characteristics Over Recommended Operating Conditions for GMAC RMIIn Transmit 10/100 Mbits/s**

| NO. | PARAMETER | DESCRIPTION | RMIIn | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| RMII11 | $t_{d(REF_CLK-TXD)}$ | Delay time, REF_CLK high to selected transmit signals valid | RMII0 | 2 | 13.5 | ns |
| | $t_{dd(REF_CLK-TXEN)}$ | | | | | |
| | $t_{d(REF_CLK-TXD)}$ | | RMII1 | 2 | 13.8 | ns |
| | $t_{dd(REF_CLK-TXEN)}$ | | | | | |

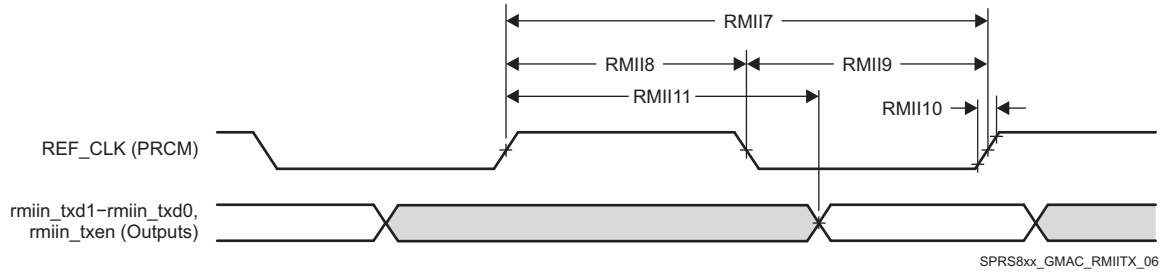


**Figure 7-57. GMAC Transmit Interface Timing RMIIn Operation**

In Table 7-80 are presented the specific groupings of signals (IOSET) for use with GMAC RMII signals.


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**Table 7-80. GMAC RMII IOSETs**

| SIGNALS | IOSET1 | | IOSET2 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| **GMAC RMII1** | | | | |
| RMII_MHZ_50_CLK | U3 | 0 | | |
| rmii1_txd1 | V5 | 2 | | |
| rmii1_txd0 | V4 | 2 | | |
| rmii1_rxd1 | W9 | 2 | | |
| rmii1_rxd0 | V9 | 2 | | |
| rmii1_rxer | Y1 | 2 | | |
| rmii1_txen | U5 | 2 | | |
| rmii1_crs | V2 | 2 | | |
| **GMAC RMII0** | | | | |
| RMII_MHZ_50_CLK | | | U3 | 0 |
| rmii0_txd1 | | | Y2 | 1 |
| rmii0_txd0 | | | W2 | 1 |
| rmii0_rxd1 | | | V6 | 1 |
| rmii0_rxd0 | | | U6 | 1 |
| rmii0_txen | | | V3 | 1 |
| rmii0_rxer | | | U7 | 1 |
| rmii0_crs | | | V7 | 1 |

Manual IO Timings Modes must be used to ensure some IO timings for GMAC. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-81 *Manual Functions Mapping for GMAC RMII0* for a definition of the Manual modes.

Table 7-81 list the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-81. Manual Functions Mapping for GMAC RMII0**

| BALL | BALL NAME | GMAC_RMII0_MANUAL1 | | CFG REGISTER | MUXMODE | |
|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 0 | 1 |
| U3 | RMII_MHZ_50_CLK | 0 | 0 | CFG_RMII_MHZ_50_CLK_IN | RMII_MHZ_50_CLK | |
| U6 | rgmii0_txd0 | 500 | 500 | CFG_RGMII0_TXD0_IN | | rmii0_rxd0 |
| V6 | rgmii0_txd1 | 840 | 1000 | CFG_RGMII0_TXD1_IN | | rmii0_rxd1 |
| U7 | rgmii0_txd2 | 360 | 840 | CFG_RGMII0_TXD2_IN | | rmii0_rxer |
| V7 | rgmii0_txd3 | 600 | 1000 | CFG_RGMII0_TXD3_IN | | rmii0_crs |

Manual IO Timings Modes must be used to ensure some IO timings for GMAC. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-82 *Manual Functions Mapping for GMAC RMII1* for a definition of the Manual modes.

Table 7-82 list the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-82. Manual Functions Mapping for GMAC RMII1**

| BALL | BALL NAME | GMAC_RMII1_MANUAL1 | | CFG REGISTER | MUXMODE | |
|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 0 | 2 |
| U3 | RMII_MHZ_50_CLK | 0 | 0 | CFG_RMII_MHZ_50_CLK_IN | RMII_MHZ_50_CLK | |
| V9 | rgmii0_txctl | 300 | 1000 | CFG_RGMII0_TXCTL_IN | | rmii1_rxd0 |

**Table 7-82. Manual Functions Mapping for GMAC RMII1 (continued)**

| BALL | BALL NAME | GMAC_RMII1_MANUAL1 | | CFG REGISTER | MUXMODE | |
|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 0 | 2 |
| W9 | rgmii0_txc | 300 | 1200 | CFG_RGMII0_TXC_IN | | rmii1_rxd1 |
| Y1 | uart3_txd | 300 | 500 | CFG_UART3_TXD_IN | | rmii1_rxer |
| V2 | uart3_rxd | 400 | 700 | CFG_UART3_RXD_IN | | rmii1_crs |

### *7.22.4 GMAC RGMII Timings*

**CAUTION**

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-83, Table 7-84 and Figure 7-58 present timing requirements for receive RGMIIn operation.

**Table 7-83. Timing Requirements for rgmiin_rxc - RGMIIn Operation**

| NO. | PARAMETER | DESCRIPTION | SPEED | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(RXC)}$ | Cycle time, rgmiin_rxc | 10 Mbps | 360 | 440 | ns |
| | | | 100 Mbps | 36 | 44 | ns |
| | | | 1000 Mbps | 7.2 | 8.8 | ns |
| 2 | $t_{w(RXCH)}$ | Pulse duration, rgmiin_rxc high | 10 Mbps | 160 | 240 | ns |
| | | | 100 Mbps | 16 | 24 | ns |
| | | | 1000 Mbps | 3.6 | 4.4 | ns |
| 3 | $t_{w(RXCL)}$ | Pulse duration, rgmiin_rxc low | 10 Mbps | 160 | 240 | ns |
| | | | 100 Mbps | 16 | 24 | ns |
| | | | 1000 Mbps | 3.6 | 4.4 | ns |
| 4 | $t_{t(RXC)}$ | Transition time, rgmiin_rxc | 10 Mbps | | 0.75 | ns |
| | | | 100 Mbps | | 0.75 | ns |
| | | | 1000 Mbps | | 0.75 | ns |

**Table 7-84. Timing Requirements for GMAC RGMIIn Input Receive for 10/100/1000 Mbps (1)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 5 | $t_{su(RXD-RXCH)}$ | Setup time, receive selected signals valid before rgmiin_rxc high/low | 1 | | ns |
| 6 | $t_{h(RXCH-RXD)}$ | Hold time, receive selected signals valid after rgmiin_rxc high/low | 1 | | ns |


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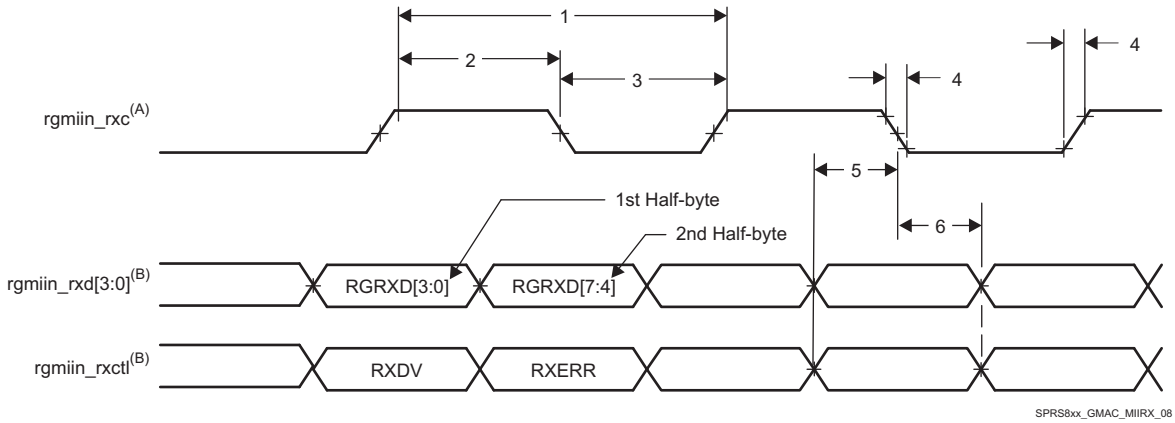
(1) For RGMII, receive selected signals include: rgmiin_rxd[3:0] and rgmiin_rxctl.




A. rgmiin_rxc must be externally delayed relative to the data and control pins.
B. Data and control information is received using both edges of the clocks. rgmiin_rxd[3:0] carries data bits 3-0 on the rising edge of rgmiin_rxc and data bits 7-4 on the falling edge ofrgmiin_rxc. Similarly, rgmiin_rxctl carries RXDV on rising edge of rgmiin_rxc and RXERR on falling edge of rgmiin_rxc.

**Figure 7-58. GMAC Receive Interface Timing, RGMIIn operation**

Table 7-85, Table 7-86 and Figure 7-59 present switching characteristics for transmit - RGMIIn for 10/100/1000Mbit/s.

**Table 7-85. Switching Characteristics Over Recommended Operating Conditions for rgmiin_txctl - RGMIIn Operation for 10/100/1000 Mbit/s**

| NO. | PARAMETER | DESCRIPTION | SPEED | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(TXC)}$ | Cycle time, rgmiin_txc | 10 Mbps | 360 | 440 | ns |
| | | | 100 Mbps | 36 | 44 | ns |
| | | | 1000 Mbps | 7.2 | 8.8 | ns |
| 2 | $t_{w(TXCH)}$ | Pulse duration, rgmiin_txc high | 10 Mbps | 160 | 240 | ns |
| | | | 100 Mbps | 16 | 24 | ns |
| | | | 1000 Mbps | 3.6 | 4.4 | ns |
| 3 | $t_{w(TXCL)}$ | Pulse duration, rgmiin_txc low | 10 Mbps | 160 | 240 | ns |
| | | | 100 Mbps | 16 | 24 | ns |
| | | | 1000 Mbps | 3.6 | 4.4 | ns |
| 4 | $t_{t(TXC)}$ | Transition time, rgmiin_txc | 10 Mbps | | 0.75 | ns |
| | | | 100 Mbps | | 0.75 | ns |
| | | | 1000 Mbps | | 0.75 | ns |

**Table 7-86. Switching Characteristics for GMAC RGMIIn Output Transmit for 10/100/1000 Mbps (1)**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 5 | $t_{osu(TXD-TXC)}$ | Output Setup time, transmit selected signals valid to rgmiin_txc high/low | RGMII0, Internal Delay Enabled, 1000 Mbps | 1.05 (2) | | ns |
| | | | RGMII0, Internal Delay Enabled, 10/100 Mbps | 1.2 | | ns |
| | | | RGMII1, Internal Delay Enabled, 1000 Mbps | 1.05 (3) | | ns |
| | | | RGMII1, Internal Delay Enabled, 10/100 Mbps | 1.2 | | ns |

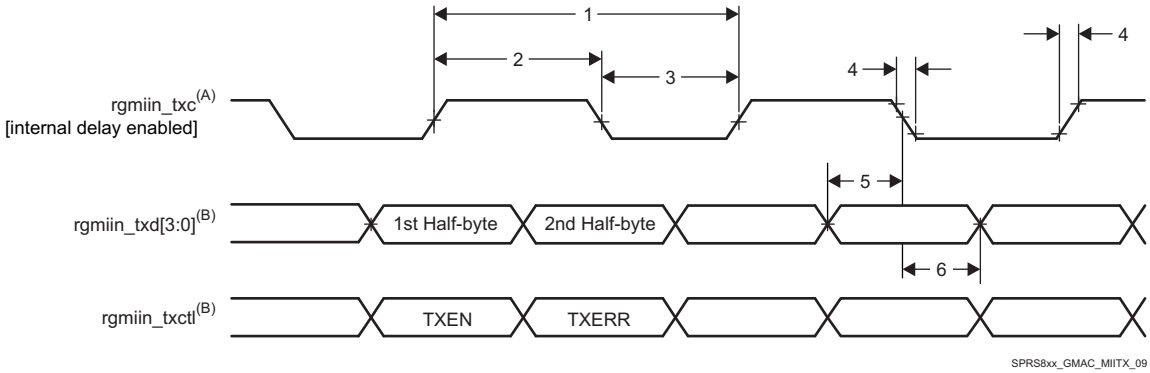
### Table 7-86. Switching Characteristics for GMAC RGMIIn Output Transmit for 10/100/1000 Mbps (1) (continued)

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 6 | $t_{oh(TXC-TXD)}$ | Output Hold time, transmit selected signals valid after rgmiin_txc high/low | RGMII0, Internal Delay Enabled, 1000 Mbps | 1.05 (2) | | ns |
| | | | RGMII0, Internal Delay Enabled, 10/100 Mbps | 1.2 | | ns |
| | | | RGMII1, Internal Delay Enabled, 1000 Mbps | 1.05 (3) | | ns |
| | | | RGMII1, Internal Delay Enabled, 10/100 Mbps | 1.2 | | ns |

(1) For RGMII, transmit selected signals include: rgmiin_txd[3:0] and rgmiin_txctl.

(2) RGMII0 1000Mbps operation requires that the 4 data pins rgmii0_txd[3:0] and rgmii0_txctl have their board propagation delays matched within 50pS of rgmii0_txc.

(3) RGMII1 1000Mbps operation requires that the 4 data pins rgmii1_txd[3:0] and rgmii1_txctl have their board propagation delays matched within 50pS of rgmii1_txc.




A. TXC is delayed internally before being driven to the rgmiin_txc pin. This internal delay is always enabled.

B. Data and control information is transmitted using both edges of the clocks. rgmiin_txd[3:0] carries data bits 3-0 on the rising edge of rgmiin_txc and data bits 7-4 on the falling edge of rgmiin_txc. Similarly, rgmiin_txctl carries TXEN on rising edge of rgmiin_txc and TXERR of falling edge of rgmiin_txc.

**Figure 7-59. GMAC Transmit Interface Timing RGMIIn operation**

In Table 7-87 are presented the specific groupings of signals (IOSET) for use with GMAC RGMII signals.

### Table 7-87. GMAC RGMII IOSETs

| SIGNALS | IOSET3 | | IOSET4 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| **GMAC RGMII1** | | | | |
| rgmii1_txd3 | C3 | 3 | | |
| rgmii1_txd2 | C4 | 3 | | |
| rgmii1_txd1 | B2 | 3 | | |
| rgmii1_txd0 | D6 | 3 | | |
| rgmii1_rxd3 | B3 | 3 | | |
| rgmii1_rxd2 | B4 | 3 | | |
| rgmii1_rxd1 | B5 | 3 | | |
| rgmii1_rxd0 | A4 | 3 | | |
| rgmii1_rxctl | A3 | 3 | | |
| rgmii1_txc | D5 | 3 | | |
| rgmii1_txctl | C2 | 3 | | |
| rgmii1_rxc | C5 | 3 | | |
| **GMAC RGMII0** | | | | |


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**Table 7-87. GMAC RGMII IOSETs (continued)**

| SIGNALS | IOSET3 | | IOSET4 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| rgmii0_txd3 | | | V7 | 0 |
| rgmii0_txd2 | | | U7 | 0 |
| rgmii0_txd1 | | | V6 | 0 |
| rgmii0_txd0 | | | U6 | 0 |
| rgmii0_rxd3 | | | V4 | 0 |
| rgmii0_rxd2 | | | V3 | 0 |
| rgmii0_rxd1 | | | Y2 | 0 |
| rgmii0_rxd0 | | | W2 | 0 |
| rgmii0_txc | | | W9 | 0 |
| rgmii0_rxctl | | | V5 | 0 |
| rgmii0_rxc | | | U5 | 0 |
| rgmii0_txctl | | | V9 | 0 |

**NOTE**

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the Control Module chapter in the Device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for GMAC. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-88 *Manual Functions Mapping for GMAC RGMII0* for a definition of the Manual modes.

Table 7-88 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-88. Manual Functions Mapping for GMAC RGMII0**

| BALL | BALL NAME | GMAC_RGMII0_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 0 |
| U5 | rgmii0_rxc | 260 | 0 | CFG_RGMII0_RXC_IN | rgmii0_rxc |
| V5 | rgmii0_rxctl | 0 | 1412 | CFG_RGMII0_RXCTL_IN | rgmii0_rxctl |
| W2 | rgmii0_rxd0 | 123 | 1047 | CFG_RGMII0_RXD0_IN | rgmii0_rxd0 |
| Y2 | rgmii0_rxd1 | 139 | 1081 | CFG_RGMII0_RXD1_IN | rgmii0_rxd1 |
| V3 | rgmii0_rxd2 | 195 | 1100 | CFG_RGMII0_RXD2_IN | rgmii0_rxd2 |
| V4 | rgmii0_rxd3 | 239 | 1216 | CFG_RGMII0_RXD3_IN | rgmii0_rxd3 |
| W9 | rgmii0_txc | 89 | 0 | CFG_RGMII0_TXC_OUT | rgmii0_txc |
| V9 | rgmii0_txctl | 15 | 125 | CFG_RGMII0_TXCTL_OUT | rgmii0_txctl |
| U6 | rgmii0_txd0 | 339 | 162 | CFG_RGMII0_TXD0_OUT | rgmii0_txd0 |
| V6 | rgmii0_txd1 | 146 | 94 | CFG_RGMII0_TXD1_OUT | rgmii0_txd1 |
| U7 | rgmii0_txd2 | 0 | 27 | CFG_RGMII0_TXD2_OUT | rgmii0_txd2 |
| V7 | rgmii0_txd3 | 291 | 205 | CFG_RGMII0_TXD3_OUT | rgmii0_txd3 |

Manual IO Timings Modes must be used to ensure some IO timings for GMAC. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-89 *Manual Functions Mapping for GMAC RGMII1* for a definition of the Manual modes.

Table 7-89 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-89. Manual Functions Mapping for GMAC RGMII1**

| BALL | BALL NAME | GMAC_RGMII1_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 3 |
| C5 | vin2a_d18 | 411 | 0 | CFG_VIN2A_D18_IN | rgmii1_rxc |
| A3 | vin2a_d19 | 0 | 382 | CFG_VIN2A_D19_IN | rgmii1_rxctl |
| B3 | vin2a_d20 | 320 | 750 | CFG_VIN2A_D20_IN | rgmii1_rxd3 |
| B4 | vin2a_d21 | 192 | 836 | CFG_VIN2A_D21_IN | rgmii1_rxd2 |
| B5 | vin2a_d22 | 294 | 669 | CFG_VIN2A_D22_IN | rgmii1_rxd1 |
| A4 | vin2a_d23 | 50 | 700 | CFG_VIN2A_D23_IN | rgmii1_rxd0 |
| | | | | | |
| D5 | vin2a_d12 | 0 | 0 | CFG_VIN2A_D12_OUT | rgmii1_txc |
| C2 | vin2a_d13 | 219 | 101 | CFG_VIN2A_D13_OUT | rgmii1_txctl |
| C3 | vin2a_d14 | 92 | 58 | CFG_VIN2A_D14_OUT | rgmii1_txd3 |
| C4 | vin2a_d15 | 135 | 100 | CFG_VIN2A_D15_OUT | rgmii1_txd2 |
| B2 | vin2a_d16 | 154 | 101 | CFG_VIN2A_D16_OUT | rgmii1_txd1 |
| D6 | vin2a_d17 | 78 | 27 | CFG_VIN2A_D17_OUT | rgmii1_txd0 |

## 7.23 eMMC/SD/SDIO

The Device includes the following external memory interfaces 4 MultiMedia Card/Secure Digital/Secure Digital Input Output Interface (MMC/SD/SDIO).

**NOTE**

The eMMC/SD/SDIOi (i = 1 to 4) controller is also referred to as MMCi.

### *7.23.1 MMC1—SD Card Interface*

MMC1 interface is compliant with the SD Standard v3.01 and it supports the following SD Card applications:

- Default speed, 4-bit data, SDR, half-cycle
- High speed, 4-bit data, SDR, half-cycle
- SDR12, 4-bit data, half-cycle
- SDR25, 4-bit data, half-cycle
- UHS-I SDR50, 4-bit data, half-cycle
- UHS-I SDR104, 4-bit data, half-cycle
- UHS-I DDR50, 4-bit data

**NOTE**

For more information, see the eMMC/SD/SDIO chapter of the Device TRM.

#### 7.23.1.1 Default speed, 4-bit data, SDR, half-cycle

Table 7-90 and Table 7-91 present Timing requirements and Switching characteristics for MMC1 - Default Speed in receiver and transmitter mode (see Figure 7-60 and Figure 7-61)

**Table 7-90. Timing Requirements for MMC1 - SD Card Default Speed Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| DSSD5 | $t_{su(cmdV-clkH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 5.11 | | ns |
| DSSD6 | $t_{h(clkH-cmdV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | 20.46 | | ns |
| DSSD7 | $t_{su(dV-clkH)}$ | Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge | 5.11 | | ns |


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**Table 7-90. Timing Requirements for MMC1 - SD Card Default Speed Mode (continued)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| DSSD8 | $t_{h(clkH-dV)}$ | Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge | 20.46 | | ns |

**Table 7-91. Switching Characteristics for MMC1 - SD Card Default Speed Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| DSSD0 | fop(clk) | Operating frequency, mmc1_clk | | 24 | MHz |
| DSSD1 | $t_{w(clkH)}$ | Pulse duration, mmc1_clk high | 0.5*P-0.185 | (1) | ns |
| DSSD2 | $t_{w(clkL)}$ | Pulse duration, mmc1_clk low | 0.5*P-0.185 | (1) | ns |
| DSSD3 | $t_{d(clkL-cmdV)}$ | Delay time, mmc1_clk falling clock edge to mmc1_cmd transition | -14.93 | 14.93 | ns |
| DSSD4 | $t_{d(clkL-dV)}$ | Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition | -14.93 | 14.93 | ns |

(1) P = output mmc1_clk period in ns

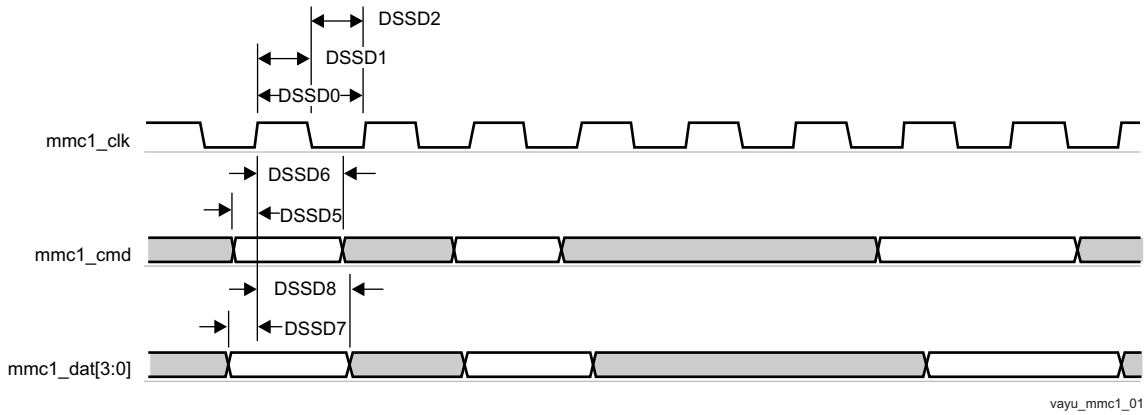


**Figure 7-60. MMC/SD/SDIO in - Default Speed - Receiver Mode**

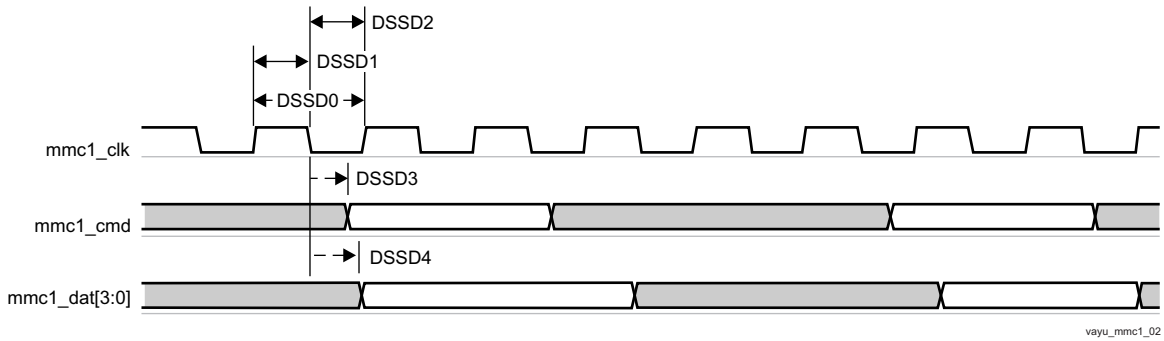


**Figure 7-61. MMC/SD/SDIO in - Default Speed - Transmitter Mode**

### 7.23.1.2 High speed, 4-bit data, SDR, half-cycle

Table 7-92 and Table 7-93 present Timing requirements and Switching characteristics for MMC1 - High Speed in receiver and transmitter mode (see Figure 7-62 and Figure 7-63)

**Table 7-92. Timing Requirements for MMC1 - SD Card High Speed Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| HSSD3 | $t_{su(cmdV-clkH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 5.3 | | ns |
| HSSD4 | $t_{h(clkH-cmdV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | 2.6 | | ns |
| HSSD7 | $t_{su(dV-clkH)}$ | Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge | 5.3 | | ns |

**Table 7-92. Timing Requirements for MMC1 - SD Card High Speed Mode (continued)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| HSSD8 | $t_{h(clkH-dV)}$ | Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge | 2.6 | | ns |

**Table 7-93. Switching Characteristics for MMC1 - SD Card High Speed Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| HSSD1 | fop(clk) | Operating frequency, mmc1_clk | | 48 | MHz |
| HSSD2H | $t_{w(clkH)}$ | Pulse duration, mmc1_clk high | 0.5*P-0.185 | (1) | ns |
| HSSD2L | $t_{w(clkL)}$ | Pulse duration, mmc1_clk low | 0.5*P-0.185 | (1) | ns |
| HSSD5 | $t_{d(clkL-cmdV)}$ | Delay time, mmc1_clk falling clock edge to mmc1_cmd transition | -7.6 | 3.6 | ns |
| HSSD6 | $t_{d(clkL-dV)}$ | Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition | -7.6 | 3.6 | ns |

(1) P = output mmc1_clk period in ns

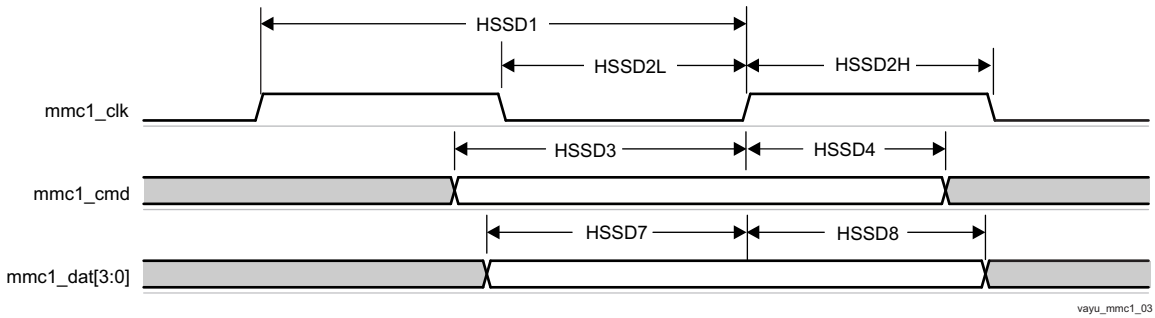


**Figure 7-62. MMC/SD/SDIO in - High Speed - Receiver Mode**

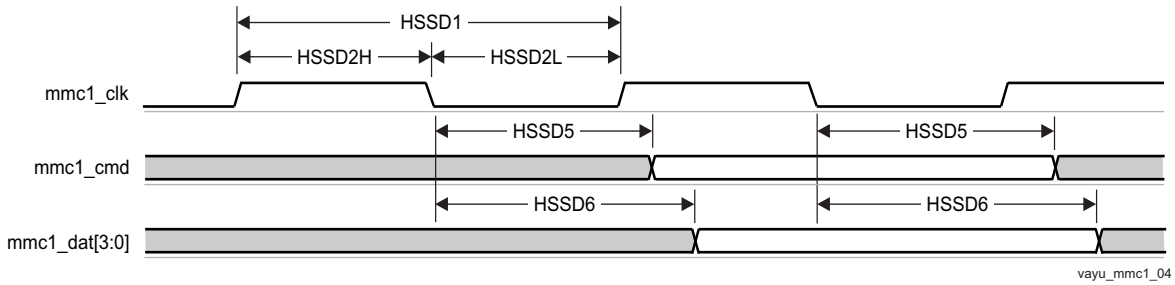


**Figure 7-63. MMC/SD/SDIO in - High Speed - Transmitter Mode**

### 7.23.1.3 SDR12, 4-bit data, half-cycle

Table 7-94 and Table 7-95 present Timing requirements and Switching characteristics for MMC1 - SDR12 in receiver and transmitter mode(see Figure 7-64 and Figure 7-65).

**Table 7-94. Timing Requirements for MMC1 - SD Card SDR12 Mode**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| SDR125 | $t_{su(cmdV-clkH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | | 25.99 | | ns |
| SDR126 | $t_{h(clkH-cmdV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | Pad Loopback Clock | 1.6 | | ns |
| | | | Internal Loopback Clock | 1.6 | | ns |


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**Table 7-94. Timing Requirements for MMC1 - SD Card SDR12 Mode (continued)**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| SDR127 | $t_{su(dV-clkH)}$ | Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge | | 25.99 | | ns |
| SDR128 | $t_{h(clkH-dV)}$ | Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge | Pad Loopback Clock | 1.6 | | ns |
| | | | Internal Loopback Clock | 1.6 | | ns |

**Table 7-95. Switching Characteristics for MMC1 - SD Card SDR12 Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR120 | fop(clk) | Operating frequency, mmc1_clk | | 24 | MHz |
| SDR121 | $t_{w(clkH)}$ | Pulse duration, mmc1_clk high | 0.5*P-0.185 | (1) | ns |
| SDR122 | $t_{w(clkL)}$ | Pulse duration, mmc1_clk low | 0.5*P-0.185 | (1) | ns |
| SDR123 | $t_{d(clkL-cmdV)}$ | Delay time, mmc1_clk falling clock edge to mmc1_cmd transition | -19.13 | 16.93 | ns |
| SDR124 | $t_{d(clkL-dV)}$ | Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition | -19.13 | 16.93 | ns |

(1) P = output mmc1_clk period in ns

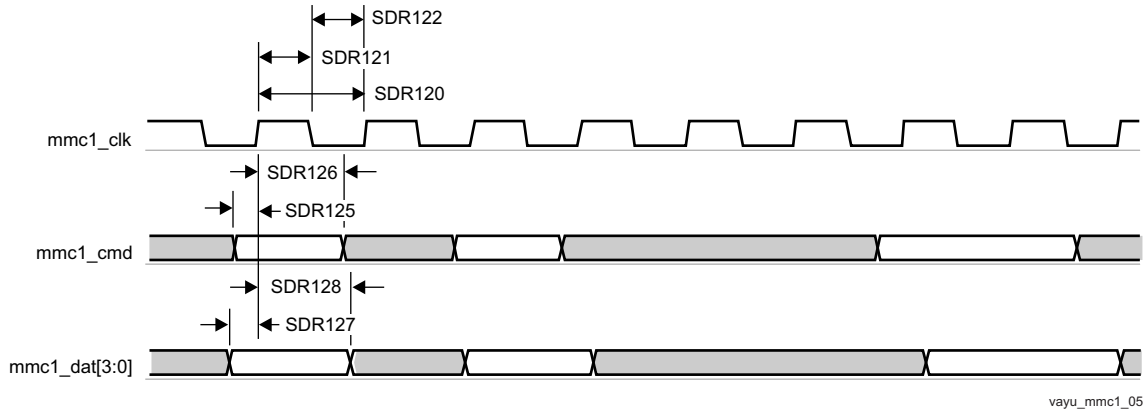


**Figure 7-64. MMC/SD/SDIO in - High Speed SDR12 - Receiver Mode**

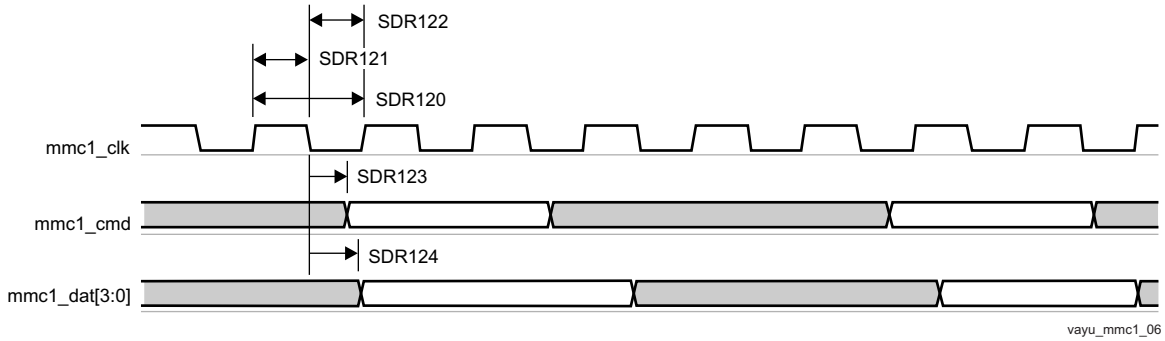


**Figure 7-65. MMC/SD/SDIO in - High Speed SDR12 - Transmitter Mode**

### 7.23.1.4 SDR25, 4-bit data, half-cycle

Table 7-96 and Table 7-97 present Timing requirements and Switching characteristics for MMC1 - SDR25 in receiver and transmitter mode (see Figure 7-66 and Figure 7-67).

**Table 7-96. Timing Requirements for MMC1 - SD Card SDR25 Mode**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| SDR253 | $t_{su(cmdV-clkH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | | 5.3 | | ns |
| SDR254 | $t_{h(clkH-cmdV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | | 1.6 | | ns |
| SDR257 | $t_{su(dV-clkH)}$ | Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge | | 5.3 | | ns |
| SDR258 | $t_{h(clkH-dV)}$ | Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge | Pad Loopback Clock | 1.6 | | ns |
| | | | Internal Loopback Clock | 1.6 | | ns |

**Table 7-97. Switching Characteristics for MMC1 - SD Card SDR25 Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR251 | fop(clk) | Operating frequency, mmc1_clk | | 48 | MHz |
| SDR252H | $t_{w(clkH)}$ | Pulse duration, mmc1_clk high | 0.5*P-0.185 | (1) | ns |
| SDR252L | $t_{w(clkL)}$ | Pulse duration, mmc1_clk low | 0.5*P-0.185 | (1) | ns |
| SDR255 | $t_{d(clkL-cmdV)}$ | Delay time, mmc1_clk falling clock edge to mmc1_cmd transition | -8.8 | 6.6 | ns |
| SDR256 | $t_{d(clkL-dV)}$ | Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition | -8.8 | 6.6 | ns |

(1) P = output mmc1_clk period in ns

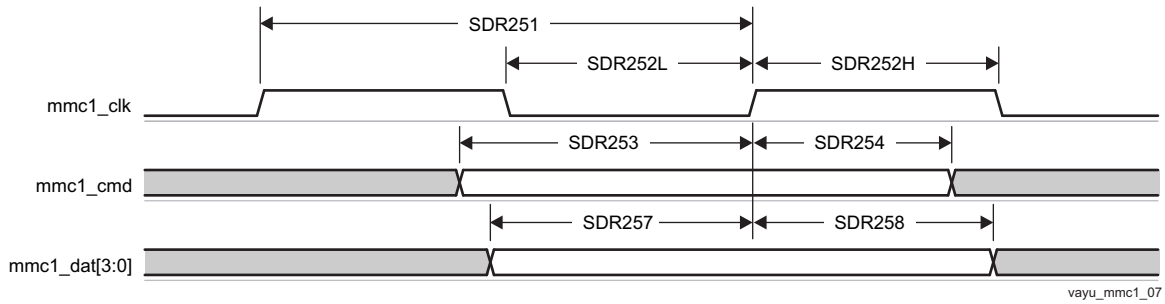


**Figure 7-66. MMC/SD/SDIO in - High Speed SDR25 - Receiver Mode**

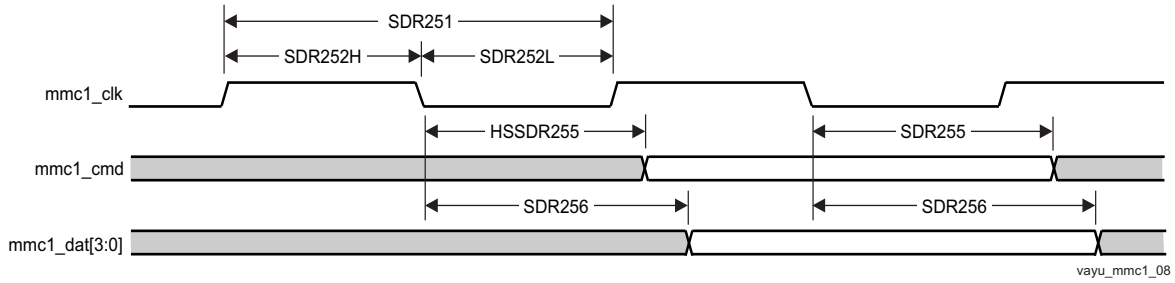


**Figure 7-67. MMC/SD/SDIO in - High Speed SDR25 - Transmitter Mode**

### 7.23.1.5 UHS-I SDR50, 4-bit data, half-cycle

Table 7-98 and Table 7-99 present Timing requirements and Switching characteristics for MMC1 - SDR50 in receiver and transmitter mode (see Figure 7-68 and Figure 7-69).


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**Table 7-98. Timing Requirements for MMC1 - SD Card SDR50 Mode**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| SDR503 | $t_{su(cmdV-clkH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | | 1.72 | | ns |
| SDR504 | $t_{h(clkH-cmdV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | | 1.6 | | ns |
| SDR507 | $t_{su(dV-clkH)}$ | Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge | | 1.72 | | ns |
| SDR508 | $t_{h(clkH-dV)}$ | Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge | Pad Loopback Clock | 1.6 | | ns |
| | | | Internal Loopback Clock | 1.6 | | ns |

**Table 7-99. Switching Characteristics for MMC1 - SD Card SDR50 Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR501 | fop(clk) | Operating frequency, mmc1_clk | | 96 | MHz |
| SDR502H | $t_{w(clkH)}$ | Pulse duration, mmc1_clk high | 0.5*P-0.185 | (1) | ns |
| SDR502L | $t_{w(clkL)}$ | Pulse duration, mmc1_clk low | 0.5*P-0.185 | (1) | ns |
| SDR505 | $t_{d(clkL-cmdV)}$ | Delay time, mmc1_clk falling clock edge to mmc1_cmd transition | -3.66 | 1.46 | ns |
| SDR506 | $t_{d(clkL-dV)}$ | Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition | -3.66 | 1.46 | ns |

(1) P = output mmc1_clk period in ns

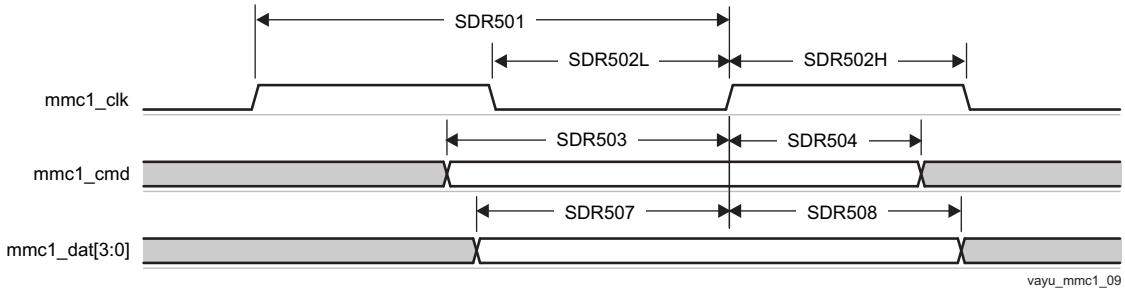


**Figure 7-68. MMC/SD/SDIO in - High Speed SDR50 - Receiver Mode**

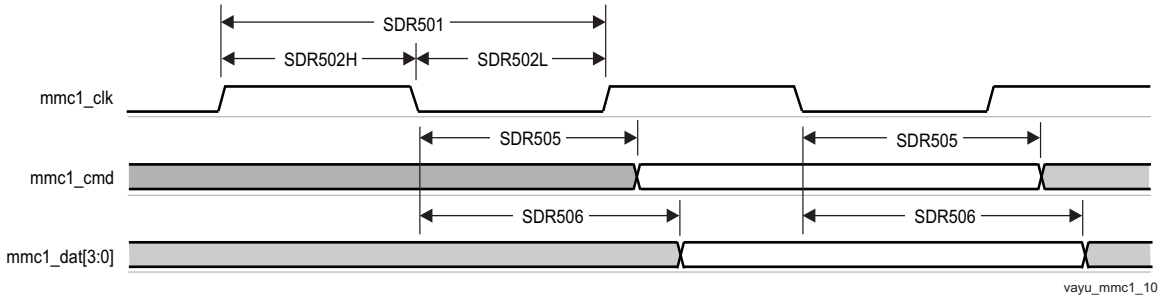


**Figure 7-69. MMC/SD/SDIO in - High Speed SDR50 - Transmitter Mode**

### 7.23.1.6 UHS-I SDR104, 4-bit data, half-cycle

Table 7-100 presents Timing requirements and Switching characteristics for MMC1 - SDR104 in receiver and transmitter mode (see Figure 7-70 and Figure 7-71)

**Table 7-100. Switching Characteristics for MMC1 - SD Card SDR104 Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR1041 | fop(clk) | Operating frequency, mmc1_clk | | 192 | MHz |
| SDR1042 H | $t_{w(clkH)}$ | Pulse duration, mmc1_clk high | 0.5*P-0.185 | (1) | ns |
| SDR1042 L | $t_{w(clkL)}$ | Pulse duration, mmc1_clk low | 0.5*P-0.185 | (1) | ns |
| SDR1045 | $t_{d(clkL-cmdV)}$ | Delay time, mmc1_clk falling clock edge to mmc1_cmd transition | -1.09 | 0.49 | ns |
| SDR1046 | $t_{d(clkL-dV)}$ | Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition | -1.09 | 0.49 | ns |

(1) P = output mmc1_clk period in ns

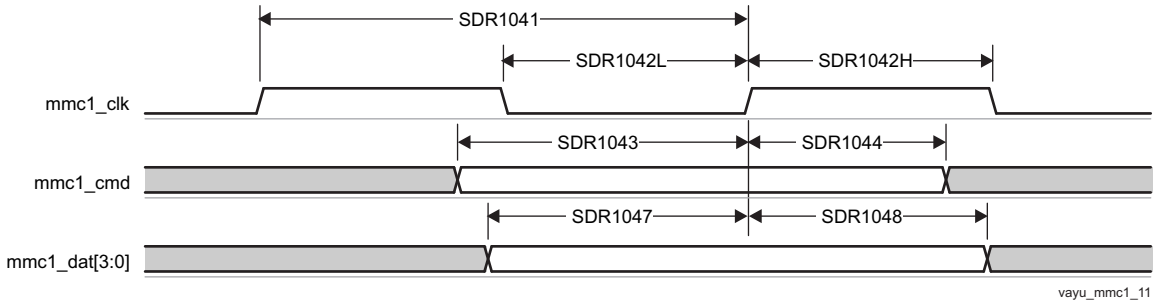


**Figure 7-70. MMC/SD/SDIO in - High Speed SDR104 - Receiver Mode**

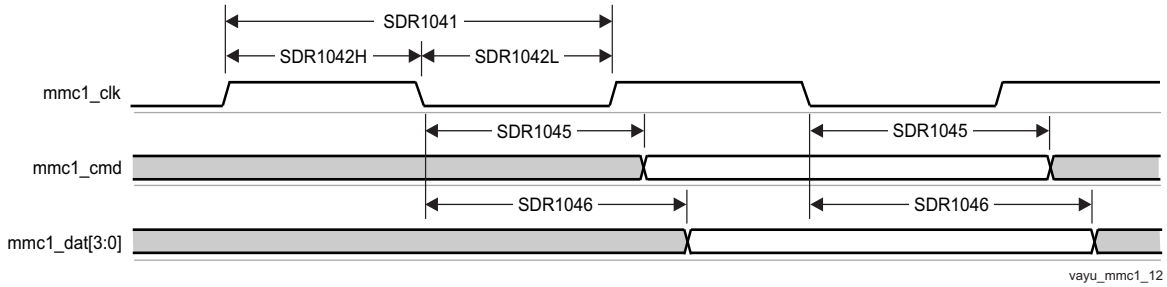


**Figure 7-71. MMC/SD/SDIO in - High Speed SDR104 - Transmitter Mode**

### 7.23.1.7 UHS-I DDR50, 4-bit data

Table 7-101 and Table 7-102 present Timing requirements and Switching characteristics for MMC1 - DDR50 in receiver and transmitter mode (see Figure 7-72 and Figure 7-73).

**Table 7-101. Timing Requirements for MMC1 - SD Card DDR50 Mode**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| DDR505 | $t_{su(cmdV-clk)}$ | Setup time, mmc1_cmd valid before mmc1_clk transition | | 1.79 | | ns |
| DDR506 | $t_{h(clk-cmdV)}$ | Hold time, mmc1_cmd valid after mmc1_clk transition | | 1.6 | | ns |
| DDR507 | $t_{su(dV-clk)}$ | Setup time, mmc1_dat[3:0] valid before mmc1_clk transition | Pad Loopback | 1.79 | | ns |
| | | | Internal Loopback | 1.79 | | ns |
| DDR508 | $t_{h(clk-dV)}$ | Hold time, mmc1_dat[3:0] valid after mmc1_clk transition | Pad Loopback | 1.6 | | ns |
| | | | Internal Loopback | 1.6 | | ns |


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**Table 7-102. Switching Characteristics for MMC1 - SD Card DDR50 Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| DDR500 | fop(clk) | Operating frequency, mmc1_clk | | 48 | MHz |
| DDR501 | $t_{w(clkH)}$ | Pulse duration, mmc1_clk high | 0.5*P-0.185 | (1) | ns |
| DDR502 | $t_{w(clkL)}$ | Pulse duration, mmc1_clk low | 0.5*P-0.185 | (1) | ns |
| DDR503 | $t_{d(clk-cmdV)}$ | Delay time, mmc1_clk transition to mmc1_cmd transition | 1.225 | 6.6 | ns |
| DDR504 | $t_{d(clk-dV)}$ | Delay time, mmc1_clk transition to mmc1_dat[3:0] transition | 1.225 | 6.6 | ns |

(1) P = output mmc1_clk period in ns

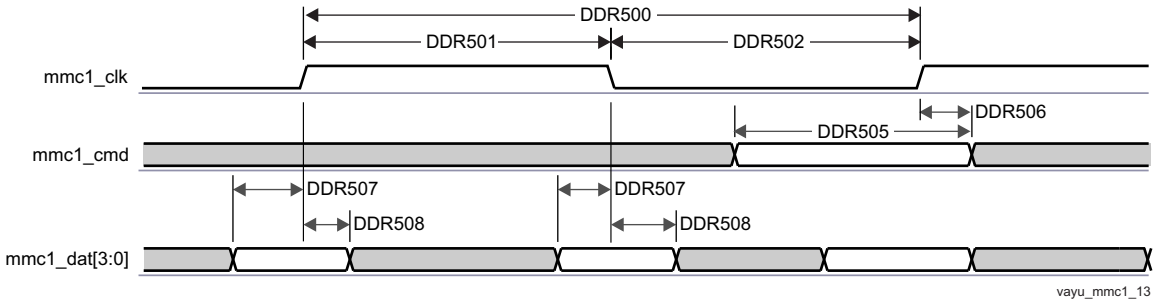


**Figure 7-72. SDMMC - High Speed SD - DDR - Data/Command Receive**

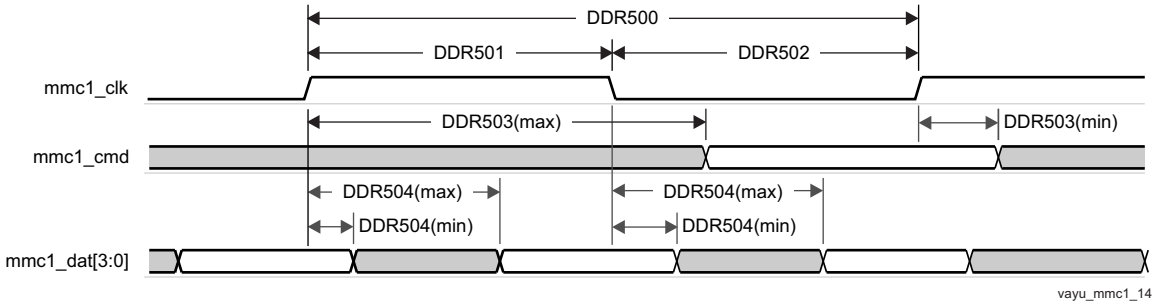


**Figure 7-73. SDMMC - High Speed SD - DDR - Data/Command Transmit**

**NOTE**

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented in Table 4-3 and described in Device TRM, *Control Module Chapter*.

Virtual IO Timings Modes must be used to ensure some IO timings for MMC1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 7-103 *Virtual Functions Mapping for MMC1* for a definition of the Virtual modes.

Table 7-103 presents the values for DELAYMODE bitfield.

**Table 7-103. Virtual Functions Mapping for MMC1**

| BALL | BALL NAME | Delay Mode Value | | | | | MUXMODE[15:0] |
|---|---|---|---|---|---|---|---|
| | | MMC1_VIRTUAL1 | MMC1_VIRTUAL2 | MMC1_VIRTUAL5 | MMC1_VIRTUAL6 | MMC1_VIRTUAL7 | 0 |
| W6 | mmc1_clk | 11 | 10 | 7 | 6 | 5 | mmc1_clk |

**Table 7-103. Virtual Functions Mapping for MMC1 (continued)**

| BALL | BALL NAME | Delay Mode Value | | | | | MUXMODE[15:0] |
|---|---|---|---|---|---|---|---|
| | | MMC1_VIRTUAL1 | MMC1_VIRTUAL2 | MMC1_VIRTUAL5 | MMC1_VIRTUAL6 | MMC1_VIRTUAL7 | 0 |
| Y6 | mmc1_cmd | 11 | 10 | 7 | 6 | 5 | mmc1_cmd |
| AA6 | mmc1_dat0 | 11 | 10 | 7 | 6 | 5 | mmc1_dat0 |
| Y4 | mmc1_dat1 | 11 | 10 | 7 | 6 | 5 | mmc1_dat1 |
| AA5 | mmc1_dat2 | 11 | 10 | 7 | 6 | 5 | mmc1_dat2 |
| Y3 | mmc1_dat3 | 11 | 10 | 7 | 6 | 5 | mmc1_dat3 |

**NOTE**

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the Control Module chapter in the Device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for MMC1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-104 *Manual Functions Mapping for MMC1* for a definition of the Manual modes.

Table 7-104 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.


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**Table 7-104. Manual Functions Mapping for MMC1**

| BALL | BALL NAME | MMC1_DDR_MANUAL1 | | MMC1_SDR104_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 0 |
| W6 | mmc1_clk | 1076 | 330 | - | - | CFG_MMC1_CLK_IN | mmc1_clk |
| W6 | mmc1_clk | 1271 | 0 | 600 | 400 | CFG_MMC1_CLK_OUT | mmc1_clk |
| Y6 | mmc1_cmd | 722 | 0 | - | - | CFG_MMC1_CMD_IN | mmc1_cmd |
| Y6 | mmc1_cmd | 0 | 0 | 0 | 0 | CFG_MMC1_CMD_OEN | mmc1_cmd |
| Y6 | mmc1_cmd | 0 | 0 | 0 | 0 | CFG_MMC1_CMD_OUT | mmc1_cmd |
| AA6 | mmc1_dat0 | 751 | 0 | - | - | CFG_MMC1_DAT0_IN | mmc1_dat0 |
| AA6 | mmc1_dat0 | 0 | 0 | 0 | 0 | CFG_MMC1_DAT0_OEN | mmc1_dat0 |
| AA6 | mmc1_dat0 | 20 | 0 | 30 | 0 | CFG_MMC1_DAT0_OUT | mmc1_dat0 |
| Y4 | mmc1_dat1 | 256 | 0 | - | - | CFG_MMC1_DAT1_IN | mmc1_dat1 |
| Y4 | mmc1_dat1 | 0 | 0 | 0 | 0 | CFG_MMC1_DAT1_OEN | mmc1_dat1 |
| Y4 | mmc1_dat1 | 0 | 0 | 0 | 0 | CFG_MMC1_DAT1_OUT | mmc1_dat1 |
| AA5 | mmc1_dat2 | 263 | 0 | - | - | CFG_MMC1_DAT2_IN | mmc1_dat2 |
| AA5 | mmc1_dat2 | 0 | 0 | 0 | 0 | CFG_MMC1_DAT2_OEN | mmc1_dat2 |
| AA5 | mmc1_dat2 | 0 | 0 | 0 | 0 | CFG_MMC1_DAT2_OUT | mmc1_dat2 |
| Y3 | mmc1_dat3 | 0 | 0 | - | - | CFG_MMC1_DAT3_IN | mmc1_dat3 |
| Y3 | mmc1_dat3 | 0 | 0 | 0 | 0 | CFG_MMC1_DAT3_OEN | mmc1_dat3 |
| Y3 | mmc1_dat3 | 0 | 0 | 0 | 0 | CFG_MMC1_DAT3_OUT | mmc1_dat3 |

### *7.23.2 MMC2 — eMMC*

MMC2 interface is compliant with the JC64 eMMC Standard v4.5 and it supports the following eMMC applications:

- Standard JC64 SDR, 8-bit data, half cycle
- High-speed JC64 SDR, 8-bit data, half cycle
- High-speed JC64 DDR, 8-bit data
- High-speed HS200 JC64 SDR, 8-bit data, half cycle

**NOTE**

For more information, see the eMMC/SD/SDIO chapter of the Device TRM.

#### 7.23.2.1 Standard JC64 SDR, 8-bit data, half cycle

Table 7-105 and Table 7-106 present Timing requirements and Switching characteristics for MMC2 - Standard SDR in receiver and transmitter mode (see Figure 7-74 and Figure 7-75).

### Table 7-105. Timing Requirements for MMC2 - JC64 Standard SDR Mode

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SSDR5 | $t_{su(cmdV-clkH)}$ | Setup time, mmc2_cmd valid before mmc2_clk rising clock edge | 13.19 | | ns |
| SSDR6 | $t_{h(clkH-cmdV)}$ | Hold time, mmc2_cmd valid after mmc2_clk rising clock edge | 8.4 | | ns |
| SSDR7 | $t_{su(dV-clkH)}$ | Setup time, mmc2_dat[7:0] valid before mmc2_clk rising clock edge | 13.19 | | ns |
| SSDR8 | $t_{h(clkH-dV)}$ | Hold time, mmc2_dat[7:0] valid after mmc2_clk rising clock edge | 8.4 | | ns |


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**Table 7-106. Switching Characteristics for MMC2 - JC64 Standard SDR Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SSDR1 | fop(clk) | Operating frequency, mmc2_clk | | 24 | MHz |
| SSDR2H | $t_{w(clkH)}$ | Pulse duration, mmc2_clk high | 0.5*P-0.172 | (1) | ns |
| SSDR2L | $t_{w(clkL)}$ | Pulse duration, mmc2_clk low | 0.5*P-0.172 | (1) | ns |
| SSDR3 | $t_{d(clkL-cmdV)}$ | Delay time, mmc2_clk falling clock edge to mmc2_cmd transition | -16.96 | 16.96 | ns |
| SSDR4 | $t_{d(clkL-dV)}$ | Delay time, mmc2_clk falling clock edge to mmc2_dat[7:0] transition | -16.96 | 16.96 | ns |

(1) P = output mmc2_clk period in ns

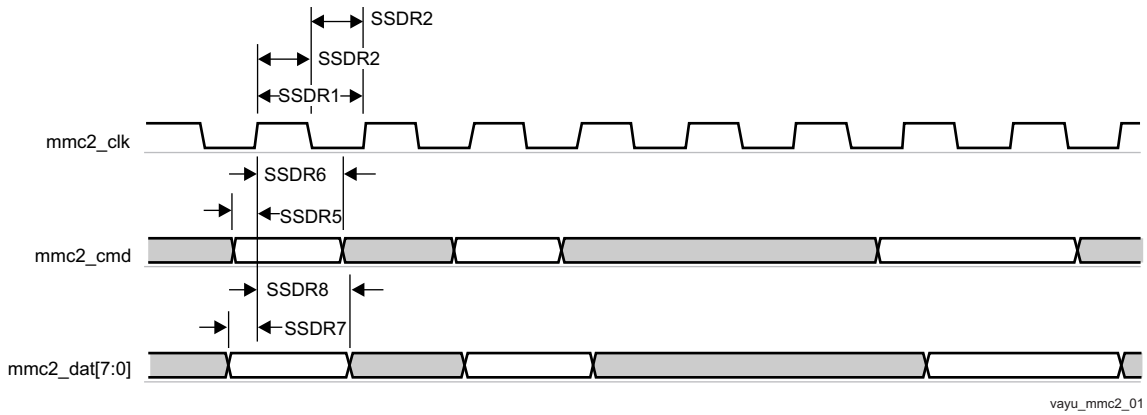


**Figure 7-74. MMC/SD/SDIO in - Standard JC64 - Receiver Mode**

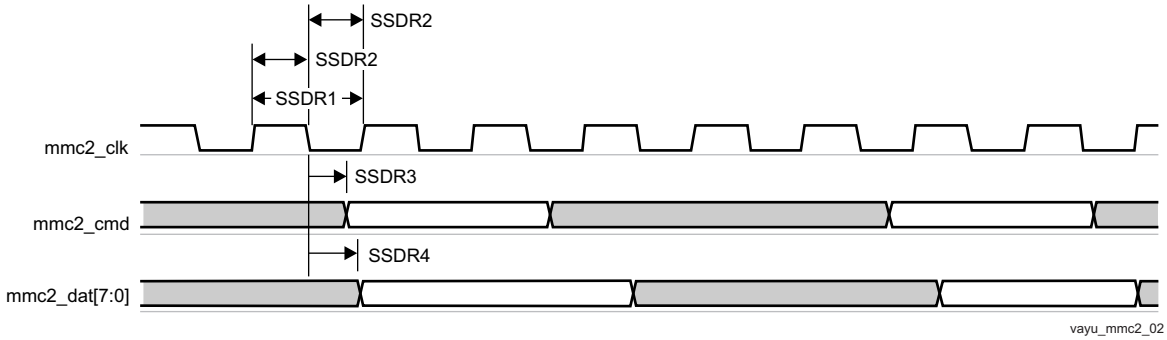


**Figure 7-75. MMC/SD/SDIO in - Standard JC64 - Transmitter Mode**

### 7.23.2.2 High-speed JC64 SDR, 8-bit data, half cycle

Table 7-107 and Table 7-108 present Timing requirements and Switching characteristics for MMC2 - High speed SDR in receiver and transmitter mode (see Figure 7-76 and Figure 7-77).

**Table 7-107. Timing Requirements for MMC2 - JC64 High Speed SDR Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| JC643 | $t_{su(cmdV-clkH)}$ | Setup time, mmc2_cmd valid before mmc2_clk rising clock edge | 5.6 | | ns |
| JC644 | $t_{h(clkH-cmdV)}$ | Hold time, mmc2_cmd valid after mmc2_clk rising clock edge | 2.6 | | ns |
| JC647 | $t_{su(dV-clkH)}$ | Setup time, mmc2_dat[7:0] valid before mmc2_clk rising clock edge | 5.6 | | ns |
| JC648 | $t_{h(clkH-dV)}$ | Hold time, mmc2_dat[7:0] valid after mmc2_clk rising clock edge | 2.6 | | ns |

**Table 7-108. Switching Characteristics for MMC2 - JC64 High Speed SDR Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| JC641 | fop(clk) | Operating frequency, mmc2_clk | | 48 | MHz |
| JC642H | $t_{w(clkH)}$ | Pulse duration, mmc2_clk high | 0.5*P-0.172 | (1) | ns |
| JC642L | $t_{w(clkL)}$ | Pulse duration, mmc2_clk low | 0.5*P-0.172 | (1) | ns |
| JC645 | $t_{d(clkL-cmdV)}$ | Delay time, mmc2_clk falling clock edge to mmc2_cmd transition | -6.64 | 6.64 | ns |
| JC646 | $t_{d(clkL-dV)}$ | Delay time, mmc2_clk falling clock edge to mmc2_dat[7:0] transition | -6.64 | 6.64 | ns |

(1) P = output mmc2_clk period in ns

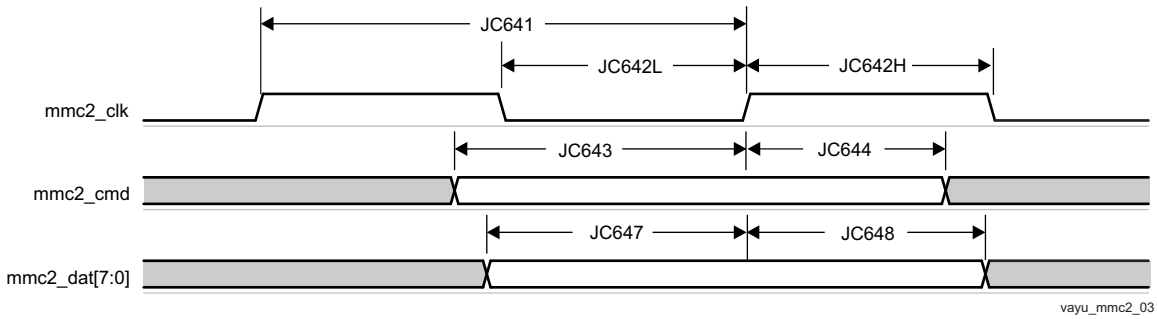


**Figure 7-76. MMC/SD/SDIO in - High Speed JC64 - Receiver Mode**

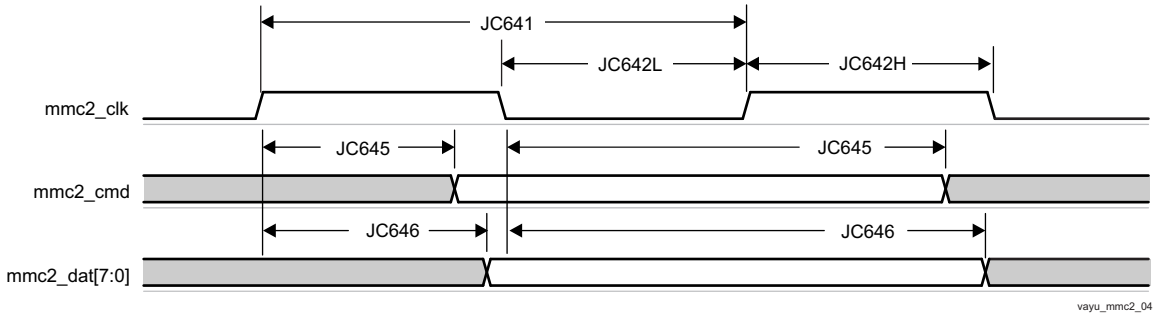


**Figure 7-77. MMC/SD/SDIO in - High Speed JC64 - Transmitter Mode**

### 7.23.2.3 High-speed HS200 JC64 SDR, 8-bit data, half cycle

Table 7-109 presents Timing requirements and Switching characteristics for MMC2 - HS200 in receiver and transmitter mode (see Figure 7-78).

**Table 7-109. Switching Characteristics for MMC2 - JEDS84 HS200 Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| HS2001 | fop(clk) | Operating frequency, mmc2_clk | | 192 | MHz |
| HS2002H | $t_{w(clkH)}$ | Pulse duration, mmc2_clk high | 0.5*P-0.172 | (1) | ns |
| HS2002L | $t_{w(clkL)}$ | Pulse duration, mmc2_clk low | 0.5*P-0.172 | (1) | ns |
| HS2005 | $t_{d(clkL-cmdV)}$ | Delay time, mmc2_clk falling clock edge to mmc2_cmd transition | -1.136 | 0.536 | ns |
| HS2006 | $t_{d(clkL-dV)}$ | Delay time, mmc2_clk falling clock edge to mmc2_dat[7:0] transition | -1.136 | 0.536 | ns |


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(1) P = output mmc2_clk period in ns

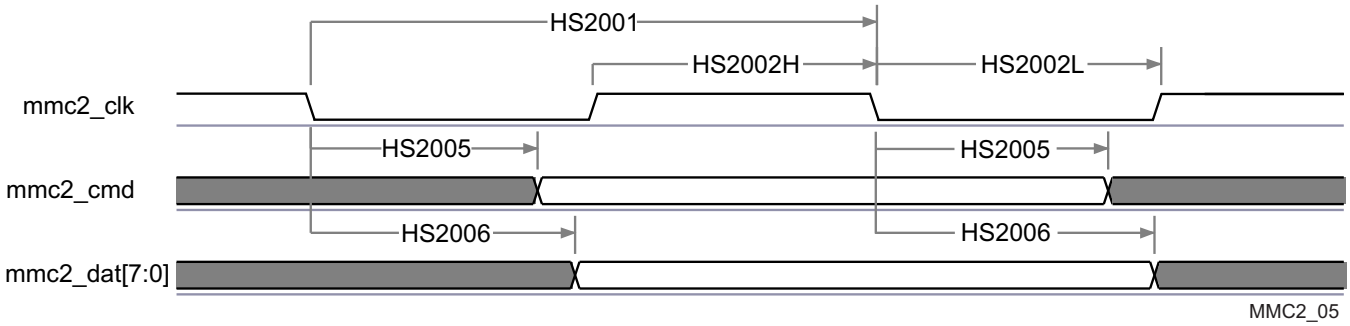


**Figure 7-78. eMMC in - HS200 SDR - Transmitter Mode**

### 7.23.2.4 High-speed JC64 DDR, 8-bit data

Table 7-110 and Table 7-111 present Timing requirements and Switching characteristics for MMC2 - High speed DDR in receiver and transmitter mode (see Figure 7-79 and Figure 7-80).

**Table 7-110. Timing Requirements for MMC2 - JC64 High Speed DDR Mode**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| DDR3 | $t_{su(cmdV-clk)}$ | Setup time, mmc2_cmd valid before mmc2_clk transition | | 1.8 | | ns |
| DDR4 | $t_{h(clk-cmdV)}$ | Hold time, mmc2_cmd valid after mmc2_clk transition | | 1.8 | | ns |
| DDR7 | $t_{su(dV-clk)}$ | Setup time, mmc2_dat[7:0] valid before mmc2_clk transition | | 1.8 | | ns |
| DDR8 | $t_{h(clk-dV)}$ | Hold time, mmc2_dat[7:0] valid after mmc2_clk transition | Pad Loopback (1.8V) | 1.8 (1) | | ns |
| | | | Pad Loopback (3.3V) | 1.8 | | ns |
| | | | Internal Loopback | 1.8 (1) | | ns |

(1) This Hold time requirement is larger than the Hold time provided by a typical eMMC component. Therefore, the trace length between the Device and eMMC component must be sufficiently long enough to ensure that the Hold time is met at the Device.

**Table 7-111. Switching Characteristics for MMC2 - JC64 High Speed DDR Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| DDR1 | fop(clk) | Operating frequency, mmc2_clk | | 48 | MHz |
| DDR2H | $t_{w(clkH)}$ | Pulse duration, mmc2_clk high | 0.5*P-0.172 | (1) | ns |
| DDR2L | $t_{w(clkL)}$ | Pulse duration, mmc2_clk low | 0.5*P-0.172 | (1) | ns |
| DDR5 | $t_{d(clk-cmdV)}$ | Delay time, mmc2_clk transition to mmc2_cmd transition | 2.9 | 7.14 | ns |
| DDR6 | $t_{d(clk-dV)}$ | Delay time, mmc2_clk transition to mmc2_dat[7:0] transition | 2.9 | 7.14 | ns |

(1) P = output mmc2_clk period in ns

Table 7-112 and Table 7-113 present Timing requirements and Switching characteristics for MMC2 - High speed DDR in receiver and transmitter mode During Boot (see Figure 7-79 and Figure 7-80).

**Table 7-112. Timing Requirements for MMC2 - JC64 High Speed DDR Mode During Boot**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| DDR3 | $t_{su(cmdV-clk)}$ | Setup time, mmc2_cmd valid before mmc2_clk transition | Boot (1.8V) | 1.8 | | ns |
| | | | Boot (3.3V) | 1.8 | | ns |
| DDR4 | $t_{h(clk-cmdV)}$ | Hold time, mmc2_cmd valid after mmc2_clk transition | Boot (1.8V) | 1.8 (1) | | ns |
| | | | Boot (3.3V) | 1.8 (1) | | ns |
| DDR7 | $t_{su(dV-clk)}$ | Setup time, mmc2_dat[7:0] valid before mmc2_clk transition | Boot (1.8V) | 1.8 | | ns |
| | | | Boot (3.3V) | 1.8 | | ns |
| DDR8 | $t_{h(clk-dV)}$ | Hold time, mmc2_dat[7:0] valid after mmc2_clk transition | Boot (1.8V) | 1.8 (1) | | ns |
| | | | Boot (3.3V) | 1.8 (1) | | ns |

(1) This Hold time requirement is larger than the Hold time provided by a typical eMMC component. Therefore, the trace length between the Device and eMMC component must be sufficiently long enough to ensure that the Hold time is met at the Device.

**Table 7-113. Switching Characteristics for MMC2 - JC64 High Speed DDR Mode During Boot**

| NO. | PARAMETER | DESCRIPTION | MODE | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| DDR1 | fop(clk) | Operating frequency, mmc2_clk | | | 48 | MHz |
| DDR2H | $t_{w(clkH)}$ | Pulse duration, mmc2_clk high | | 0.5*P-0.172 (1) | | ns |
| DDR2L | $t_{w(clkL)}$ | Pulse duration, mmc2_clk low | | 0.5*P-0.172 (1) | | ns |
| DDR5 | $t_{d(clk-cmdV)}$ | Delay time, mmc2_clk transition to mmc2_cmd transition | Boot (1.8V) | 2.9 | 7.14 | ns |
| | | | Boot (3.3V) | 2.9 | 7.14 | ns |
| DDR6 | $t_{d(clk-dV)}$ | Delay time, mmc2_clk transition to mmc2_dat[7:0] transition | Boot (1.8V) | 2.9 | 7.14 | ns |
| | | | Boot (3.3V) | 2.9 | 7.14 | ns |

(1) P = output mmc2_clk period in ns

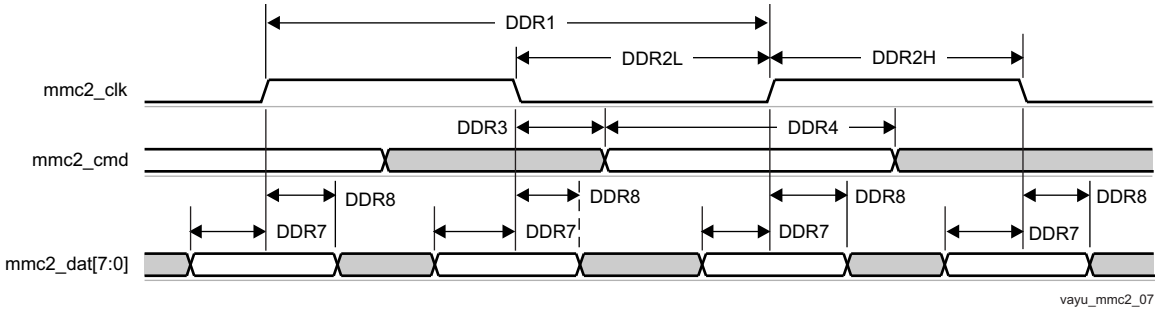


**Figure 7-79. MMC/SD/SDIO in - High Speed DDR JC64 - Receiver Mode**


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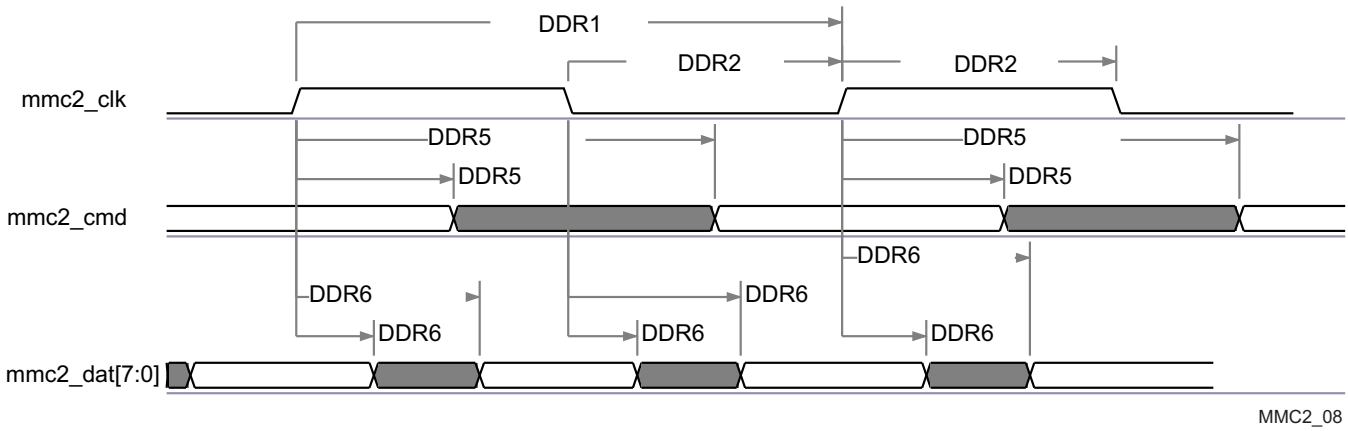


**Figure 7-80. MMC/SD/SDIO in - High Speed DDR JC64 - Transmitter Mode**

**NOTE**

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the Control Module chapter in the Device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for MMC2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-114 *Manual Functions Mapping for MMC2 With Internal Loopback Clock and for HS200* for a definition of the Manual modes.

Table 7-114 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

### Table 7-114. Manual Functions Mapping for MMC2 With Internal Loopback Clock and for HS200

| BALL | BALL NAME | MMC2_DDR_LB_MANUAL1 | | MMC2_STD_HS_LB_MANUAL1 | | MMC2_HS200_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 1 |
| K7 | gpmc_a19 | 49 | 0 | 850 | 0 | - | - | CFG_GPMC_A19_IN | mmc2_dat4 |
| K7 | gpmc_a19 | 0 | 0 | 0 | 0 | 274 | 0 | CFG_GPMC_A19_OEN | mmc2_dat4 |
| K7 | gpmc_a19 | 170 | 0 | 0 | 0 | 162 | 0 | CFG_GPMC_A19_OUT | mmc2_dat4 |
| M7 | gpmc_a20 | 463 | 0 | 1264 | 0 | - | - | CFG_GPMC_A20_IN | mmc2_dat5 |
| M7 | gpmc_a20 | 0 | 0 | 0 | 0 | 401 | 0 | CFG_GPMC_A20_OEN | mmc2_dat5 |
| M7 | gpmc_a20 | 81 | 0 | 0 | 0 | 73 | 0 | CFG_GPMC_A20_OUT | mmc2_dat5 |
| J5 | gpmc_a21 | 8 | 0 | 786 | 0 | - | - | CFG_GPMC_A21_IN | mmc2_dat6 |
| J5 | gpmc_a21 | 0 | 0 | 0 | 0 | 465 | 0 | CFG_GPMC_A21_OEN | mmc2_dat6 |
| J5 | gpmc_a21 | 123 | 0 | 0 | 0 | 115 | 0 | CFG_GPMC_A21_OUT | mmc2_dat6 |
| K6 | gpmc_a22 | 0 | 102 | 902 | 0 | - | - | CFG_GPMC_A22_IN | mmc2_dat7 |
| K6 | gpmc_a22 | 0 | 0 | 0 | 0 | 633 | 0 | CFG_GPMC_A22_OEN | mmc2_dat7 |
| K6 | gpmc_a22 | 55 | 0 | 0 | 0 | 47 | 0 | CFG_GPMC_A22_OUT | mmc2_dat7 |
| J7 | gpmc_a23 | 592 | 2815 | 0 | 2764 | - | - | CFG_GPMC_A23_IN | mmc2_clk |
| J7 | gpmc_a23 | 422 | 0 | 0 | 0 | 935 | 280 | CFG_GPMC_A23_OUT | mmc2_clk |
| J4 | gpmc_a24 | 384 | 0 | 1185 | 0 | - | - | CFG_GPMC_A24_IN | mmc2_dat0 |
| J4 | gpmc_a24 | 0 | 0 | 0 | 0 | 621 | 0 | CFG_GPMC_A24_OEN | mmc2_dat0 |
| J4 | gpmc_a24 | 0 | 0 | 0 | 0 | 0 | 0 | CFG_GPMC_A24_OUT | mmc2_dat0 |
| J6 | gpmc_a25 | 0 | 0 | 670 | 0 | - | - | CFG_GPMC_A25_IN | mmc2_dat1 |
| J6 | gpmc_a25 | 0 | 0 | 0 | 0 | 183 | 0 | CFG_GPMC_A25_OEN | mmc2_dat1 |
| J6 | gpmc_a25 | 0 | 0 | 0 | 0 | 0 | 0 | CFG_GPMC_A25_OUT | mmc2_dat1 |
| H4 | gpmc_a26 | 171 | 0 | 972 | 0 | - | - | CFG_GPMC_A26_IN | mmc2_dat2 |
| H4 | gpmc_a26 | 0 | 0 | 0 | 0 | 467 | 0 | CFG_GPMC_A26_OEN | mmc2_dat2 |
| H4 | gpmc_a26 | 0 | 0 | 0 | 0 | 0 | 0 | CFG_GPMC_A26_OUT | mmc2_dat2 |
| H5 | gpmc_a27 | 315 | 0 | 1116 | 0 | - | - | CFG_GPMC_A27_IN | mmc2_dat3 |
| H5 | gpmc_a27 | 0 | 0 | 0 | 0 | 262 | 0 | CFG_GPMC_A27_OEN | mmc2_dat3 |
| H5 | gpmc_a27 | 54 | 0 | 0 | 0 | 46 | 0 | CFG_GPMC_A27_OUT | mmc2_dat3 |
| H6 | gpmc_cs1 | 0 | 0 | 250 | 0 | - | - | CFG_GPMC_CS1_IN | mmc2_cmd |
| H6 | gpmc_cs1 | 0 | 0 | 0 | 0 | 684 | 0 | CFG_GPMC_CS1_OEN | mmc2_cmd |
| H6 | gpmc_cs1 | 0 | 0 | 0 | 0 | 76 | 0 | CFG_GPMC_CS1_OUT | mmc2_cmd |


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### 7.23.3 MMC3 and MMC4—SDIO/SD

MMC3 and MMC4 interfaces are compliant with the SDIO3.0 standard v1.0, SD Part E1 and for generic SDIO devices, it supports the following applications:

- MMC3 8-bit data and MMC4 4-bit data, SD Default speed, SDR
- MMC3 8-bit data and MMC4 4-bit data, SD High speed, SDR
- MMC3 8-bit data and MMC4 4-bit data, UHS-1 SDR12 (SD Standard v3.01), 4-bit data, SDR, half cycle
- MMC3 8-bit data and MMC4 4-bit data, UHS-I SDR25 (SD Standard v3.01), 4-bit data, SDR, half cycle
- MMC3 8-bit data, UHS-I SDR50

**NOTE**

The eMMC/SD/SDIOj (j = 3 to 4) controller is also referred to as MMCj.

**NOTE**

For more information, see the MMC/SDIO chapter of the Device TRM.

#### 7.23.3.1 MMC3 and MMC4, SD Default Speed

Figure 7-81, Figure 7-82, and Table 7-115 through Table 7-118 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD Default speed in receiver and transmitter mode.

**Table 7-115. Timing Requirements for MMC3 - Default Speed Mode (1)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| DS5 | $t_{su(cmdV-clkH)}$ | Setup time, mmc3_cmd valid before mmc3_clk rising clock edge | 5.11 | | ns |
| DS6 | $t_{h(clkH-cmdV)}$ | Hold time, mmc3_cmd valid after mmc3_clk rising clock edge | 20.46 | | ns |
| DS7 | $t_{su(dV-clkH)}$ | Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge | 5.11 | | ns |
| DS8 | $t_{h(clkH-dV)}$ | Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge | 20.46 | | ns |

(1) i in [i:0] = 7

**Table 7-116. Switching Characteristics for MMC3 - SD/SDIO Default Speed Mode (2)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| DS0 | fop(clk) | Operating frequency, mmc3_clk | | 24 | MHz |
| DS1 | $t_{w(clkH)}$ | Pulse duration, mmc3_clk high | 0.5*P-0.270 | (1) | ns |
| DS2 | $t_{w(clkL)}$ | Pulse duration, mmc3_clk low | 0.5*P-0.270 | (1) | ns |
| DS3 | $t_{d(clkL-cmdV)}$ | Delay time, mmc3_clk falling clock edge to mmc3_cmd transition | -14.93 | 14.93 | ns |
| DS4 | $t_{d(clkL-dV)}$ | Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition | -14.93 | 14.93 | ns |

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

**Table 7-117. Timing Requirements for MMC4 - Default Speed Mode (1)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| DS5 | $t_{su(cmdV-clkH)}$ | Setup time, mmc4_cmd valid before mmc4_clk rising clock edge | 5.11 | | ns |
| DS6 | $t_{h(clkH-cmdV)}$ | Hold time, mmc4_cmd valid after mmc4_clk rising clock edge | 20.46 | | ns |
| DS7 | $t_{su(dV-clkH)}$ | Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge | 5.11 | | ns |
| DS8 | $t_{h(clkH-dV)}$ | Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge | 20.46 | | ns |


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(1) i in [i:0] = 3

**Table 7-118. Switching Characteristics for MMC4 - Default Speed Mode (2)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| DS0 | fop(clk) | Operating frequency, mmc4_clk | | 24 | MHz |
| DS1 | $t_{w(clkH)}$ | Pulse duration, mmc4_clk high | 0.5*P-0.270 | (1) | ns |
| DS2 | $t_{w(clkL)}$ | Pulse duration, mmc4_clk low | 0.5*P-0.270 | (1) | ns |
| DS3 | $t_{d(clkL-cmdV)}$ | Delay time, mmc4_clk falling clock edge to mmc4_cmd transition | -14.93 | 14.93 | ns |
| DS4 | $t_{d(clkL-dV)}$ | Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition | -14.93 | 14.93 | ns |

(1) P = output mmc4_clk period in ns
(2) i in [i:0] = 3

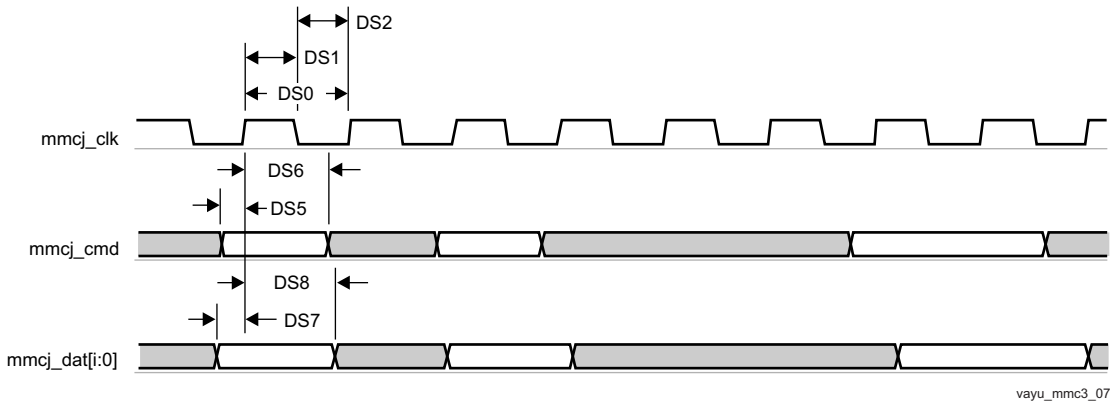


**Figure 7-81. MMC/SD/SDIOj in - Default Speed - Receiver Mode**

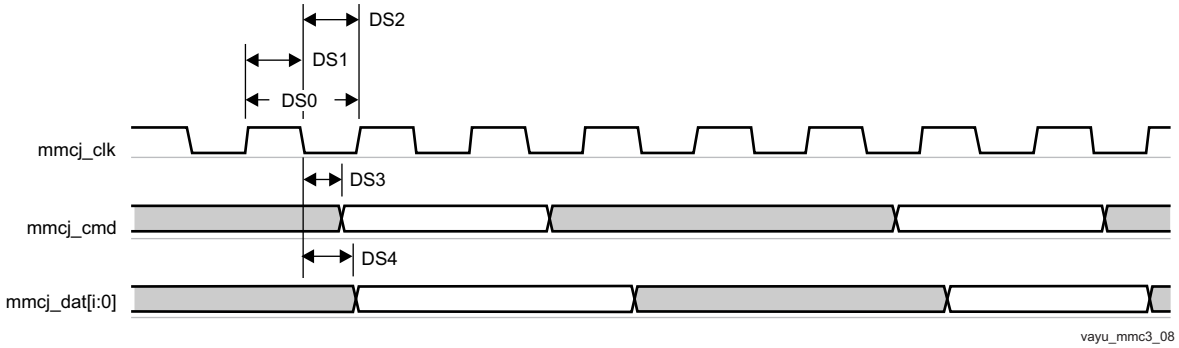


**Figure 7-82. MMC/SD/SDIOj in - Default Speed - Transmitter Mode**

### 7.23.3.2 MMC3 and MMC4, SD High Speed

Figure 7-83, Figure 7-84, and Table 7-119 through Table 7-122 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD and SDIO High speed in receiver and transmitter mode.

**Table 7-119. Timing Requirements for MMC3 - SD/SDIO High Speed Mode (1)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| HS3 | $t_{su(cmdV-clkH)}$ | Setup time, mmc3_cmd valid before mmc3_clk rising clock edge | 5.3 | | ns |
| HS4 | $t_{h(clkH-cmdV)}$ | Hold time, mmc3_cmd valid after mmc3_clk rising clock edge | 2.6 | | ns |
| HS7 | $t_{su(dV-clkH)}$ | Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge | 5.3 | | ns |

### Table 7-119. Timing Requirements for MMC3 - SD/SDIO High Speed Mode (1) (continued)

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| HS8 | $t_{h(clkH-dV)}$ | Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge | 2.6 | | ns |

(1) i in [i:0] = 7

### Table 7-120. Switching Characteristics for MMC3 - SD/SDIO High Speed Mode (2)

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| HS1 | fop(clk) | Operating frequency, mmc3_clk | | 48 | MHz |
| HS2H | $t_{w(clkH)}$ | Pulse duration, mmc3_clk high | 0.5*P-0.270 | (1) | ns |
| HS2L | $t_{w(clkL)}$ | Pulse duration, mmc3_clk low | 0.5*P-0.270 | (1) | ns |
| HS5 | $t_{d(clkL-cmdV)}$ | Delay time, mmc3_clk falling clock edge to mmc3_cmd transition | -7.6 | 3.6 | ns |
| HS6 | $t_{d(clkL-dV)}$ | Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition | -7.6 | 3.6 | ns |

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

### Table 7-121. Timing Requirements for MMC4 - High Speed Mode (1)

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| HS3 | $t_{su(cmdV-clkH)}$ | Setup time, mmc4_cmd valid before mmc4_clk rising clock edge | 5.3 | | ns |
| HS4 | $t_{h(clkH-cmdV)}$ | Hold time, mmc4_cmd valid after mmc4_clk rising clock edge | 1.6 | | ns |
| HS7 | $t_{su(dV-clkH)}$ | Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge | 5.3 | | ns |
| HS8 | $t_{h(clkH-dV)}$ | Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge | 1.6 | | ns |

(1) i in [i:0] = 3

### Table 7-122. Switching Characteristics for MMC4 - High Speed Mode (2)

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| HS1 | fop(clk) | Operating frequency, mmc4_clk | | 48 | MHz |
| HS2H | $t_{w(clkH)}$ | Pulse duration, mmc4_clk high | 0.5*P-0.270 | (1) | ns |
| HS2L | $t_{w(clkL)}$ | Pulse duration, mmc4_clk low | 0.5*P-0.270 | (1) | ns |
| HS5 | $t_{d(clkL-cmdV)}$ | Delay time, mmc4_clk falling clock edge to mmc4_cmd transition | -8.8 | 6.6 | ns |
| HS6 | $t_{d(clkL-dV)}$ | Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition | -8.8 | 6.6 | ns |

(1) P = output mmc4_clk period in ns

(2) i in [i:0] = 3

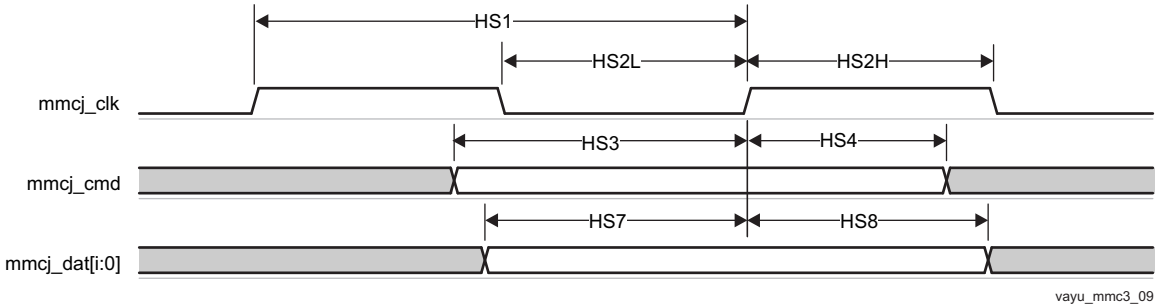


**Figure 7-83. MMC/SD/SDIOj in - High Speed - Receiver Mode**


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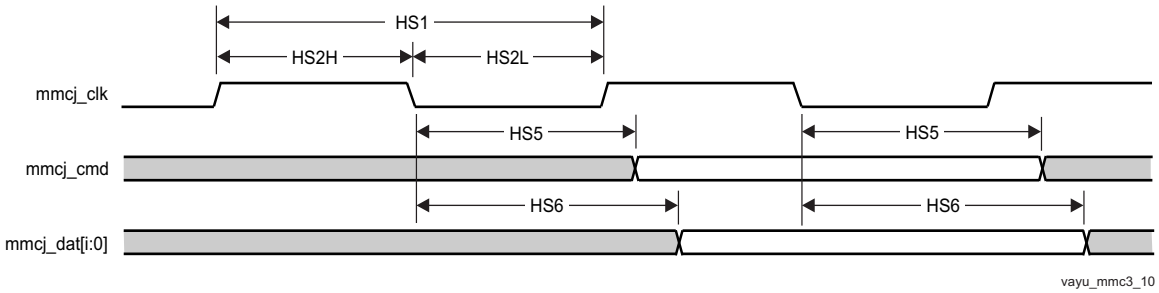


**Figure 7-84. MMC/SD/SDIOj in - High Speed - Transmitter Mode**

### 7.23.3.3 MMC3 and MMC4, SD and SDIO SDR12 Mode

Figure 7-85, Figure 7-86, and Table 7-123, through Table 7-126 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD and SDIO SDR12 in receiver and transmitter mode.

**Table 7-123. Timing Requirements for MMC3 - SDR12 Mode (1)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR125 | $t_{su(cmdV-clkH)}$ | Setup time, mmc3_cmd valid before mmc3_clk rising clock edge | 25.99 | | ns |
| SDR126 | $t_{h(clkH-cmdV)}$ | Hold time, mmc3_cmd valid after mmc3_clk rising clock edge | 1.6 | | ns |
| SDR127 | $t_{su(dV-clkH)}$ | Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge | 25.99 | | ns |
| SDR128 | $t_{h(clkH-dV)}$ | Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge | 1.6 | | ns |

(1) i in [i:0] = 7

**Table 7-124. Switching Characteristics for MMC3 - SDR12 Mode (2)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR120 | fop(clk) | Operating frequency, mmc3_clk | | 24 | MHz |
| SDR121 | $t_{w(clkH)}$ | Pulse duration, mmc3_clk high | 0.5*P-0.270 | (1) | ns |
| SDR122 | $t_{w(clkL)}$ | Pulse duration, mmc3_clk low | 0.5*P-0.270 | (1) | ns |
| SDR123 | $t_{d(clkL-cmdV)}$ | Delay time, mmc3_clk falling clock edge to mmc3_cmd transition | -19.13 | 16.93 | ns |
| SDR124 | $t_{d(clkL-dV)}$ | Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition | -19.13 | 16.93 | ns |

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

**Table 7-125. Timing Requirements for MMC4 - SDR12 Mode (1)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR125 | $t_{su(cmdV-clkH)}$ | Setup time, mmc4_cmd valid before mmc4_clk rising clock edge | 25.99 | | ns |
| SDR126 | $t_{h(clkH-cmdV)}$ | Hold time, mmc4_cmd valid after mmc4_clk rising clock edge | 1.6 | | ns |
| SDR127 | $t_{su(dV-clkH)}$ | Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge | 25.99 | | ns |
| SDR128 | $t_{h(clkH-dV)}$ | Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge | 1.6 | | ns |

(1) j in [i:0] = 3

**Table 7-126. Switching Characteristics for MMC4 - SDR12 Mode (2)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR120 | fop(clk) | Operating frequency, mmc4_clk | | 24 | MHz |
| SDR121 | $t_{w(clkH)}$ | Pulse duration, mmc4_clk high | 0.5*P-0.270 | (1) | ns |
| SDR122 | $t_{w(clkL)}$ | Pulse duration, mmc4_clk low | 0.5*P-0.270 | (1) | ns |
| SDR125 | $t_{d(clkL-cmdV)}$ | Delay time, mmc4_clk falling clock edge to mmc4_cmd transition | -19.13 | 16.93 | ns |

**Table 7-126. Switching Characteristics for MMC4 - SDR12 Mode (2) (continued)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR126 | $t_{d(clkL-dV)}$ | Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition | -19.13 | 16.93 | ns |

(1) P = output mmc4_clk period in ns
(2) j in [i:0] = 3

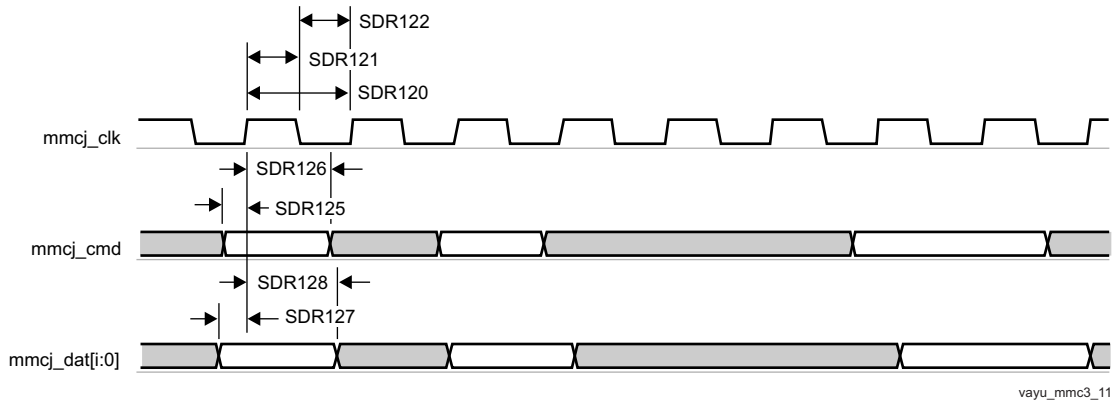


**Figure 7-85. MMC/SD/SDIOj in - SDR12 - Receiver Mode**

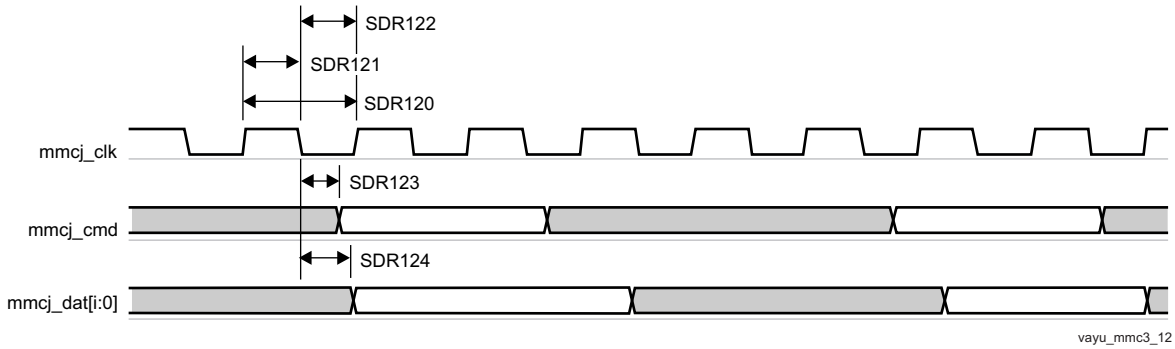


**Figure 7-86. MMC/SD/SDIOj in - SDR12 - Transmitter Mode**

### 7.23.3.4 MMC3 and MMC4, SD SDR25 Mode

Figure 7-87, Figure 7-88, and Table 7-127 through Table 7-130 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD and SDIO SDR25 in receiver and transmitter mode.

**Table 7-127. Timing Requirements for MMC3 - SDR25 Mode (1)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR253 | $t_{su(cmdV-clkH)}$ | Setup time, mmc3_cmd valid before mmc3_clk rising clock edge | 5.3 | | ns |
| SDR254 | $t_{h(clkH-cmdV)}$ | Hold time, mmc3_cmd valid after mmc3_clk rising clock edge | 1.6 | | ns |
| SDR257 | $t_{su(dV-clkH)}$ | Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge | 5.3 | | ns |
| SDR258 | $t_{h(clkH-dV)}$ | Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge | 1.6 | | ns |

(1) i in [i:0] = 7

**Table 7-128. Switching Characteristics for MMC3 - SDR25 Mode (2)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR251 | fop(clk) | Operating frequency, mmc3_clk | | 48 | MHz |
| SDR252 H | $t_{w(clkH)}$ | Pulse duration, mmc3_clk high | 0.5*P-0.270 | (1) | ns |


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### Table 7-128. Switching Characteristics for MMC3 - SDR25 Mode [2] (continued)

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR252L | $t_{w(clkL)}$ | Pulse duration, mmc3_clk low | 0.5*P-0.270 | [1] | ns |
| SDR255 | $t_{d(clkL-cmdV)}$ | Delay time, mmc3_clk falling clock edge to mmc3_cmd transition | -8.8 | 6.6 | ns |
| SDR256 | $t_{d(clkL-dV)}$ | Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition | -8.8 | 6.6 | ns |

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

### Table 7-129. Timing Requirements for MMC4 - SDR25 Mode [1]

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR255 | $t_{su(cmdV-clkH)}$ | Setup time, mmc4_cmd valid before mmc4_clk rising clock edge | 5.3 | | ns |
| SDR256 | $t_{h(clkH-cmdV)}$ | Hold time, mmc4_cmd valid after mmc4_clk rising clock edge | 1.6 | | ns |
| SDR257 | $t_{su(dV-clkH)}$ | Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge | 5.3 | | ns |
| SDR258 | $t_{h(clkH-dV)}$ | Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge | 1.6 | | ns |

(1) i in [i:0] = 3

### Table 7-130. Switching Characteristics for MMC4 - SDR25 Mode [2]

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR251 | fop(clk) | Operating frequency, mmc4_clk | | 48 | MHz |
| SDR252H | $t_{w(clkH)}$ | Pulse duration, mmc4_clk high | 0.5*P-0.270 | [1] | ns |
| SDR252L | $t_{w(clkL)}$ | Pulse duration, mmc4_clk low | 0.5*P-0.270 | [1] | ns |
| SDR255 | $t_{d(clkL-cmdV)}$ | Delay time, mmc4_clk falling clock edge to mmc4_cmd transition | -8.8 | 6.6 | ns |
| SDR256 | $t_{d(clkL-dV)}$ | Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition | -8.8 | 6.6 | ns |

(1) P = output mmc4_clk period in ns

(2) i in [i:0] = 3

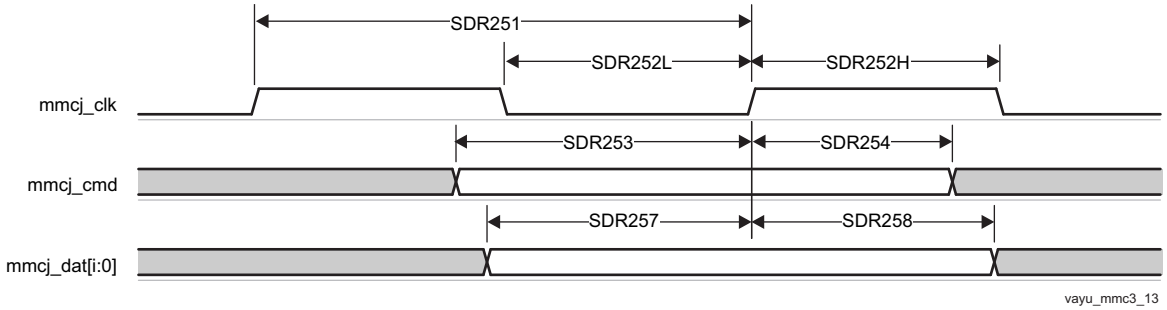


**Figure 7-87. MMC/SD/SDIOj in - SDR25 - Receiver Mode**

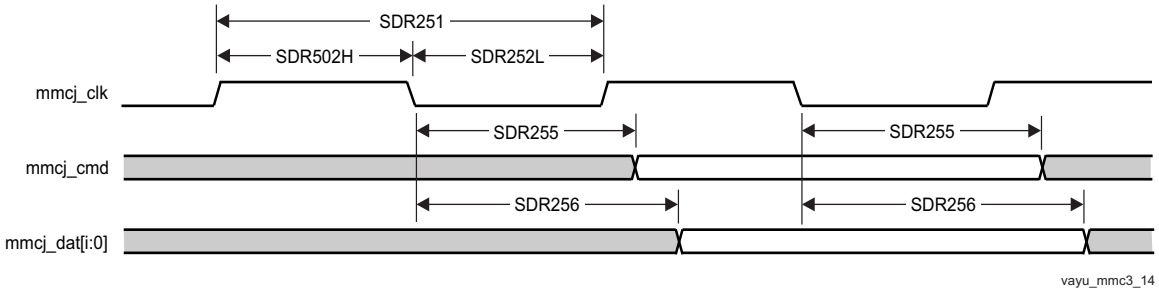


**Figure 7-88. MMC/SD/SDIOj in - SDR25 - Transmitter Mode**

### 7.23.3.5 MMC3 SDIO High-Speed UHS-I SDR50 Mode, Half Cycle

Figure 7-89, Figure 7-90, Table 7-131, and Table 7-132 present Timing requirements and Switching characteristics for MMC3 - SDIO High speed SDR50 in receiver and transmitter mode.

**Table 7-131. Timing Requirements for MMC3 - SDR50 Mode (1)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR503 | $t_{su(cmdV-clkH)}$ | Setup time, mmc3_cmd valid before mmc3_clk rising clock edge | 1.48 | | ns |
| SDR504 | $t_{h(clkH-cmdV)}$ | Hold time, mmc3_cmd valid after mmc3_clk rising clock edge | 1.6 | | ns |
| SDR507 | $t_{su(dV-clkH)}$ | Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge | 1.48 | | ns |
| SDR508 | $t_{h(clkH-dV)}$ | Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge | 1.6 | | ns |

(1) i in [i:0] = 7

**Table 7-132. Switching Characteristics for MMC3 - SDR50 Mode (2)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SDR501 | fop(clk) | Operating frequency, mmc3_clk | | 64 | MHz |
| SDR502H | $t_{w(clkH)}$ | Pulse duration, mmc3_clk high | 0.5*P-0.270 | (1) | ns |
| SDR502L | $t_{w(clkL)}$ | Pulse duration, mmc3_clk low | 0.5*P-0.270 | (1) | ns |
| SDR505 | $t_{d(clkL-cmdV)}$ | Delay time, mmc3_clk falling clock edge to mmc3_cmd transition | -3.66 | 1.46 | ns |
| SDR506 | $t_{d(clkL-dV)}$ | Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition | -3.66 | 1.46 | ns |

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

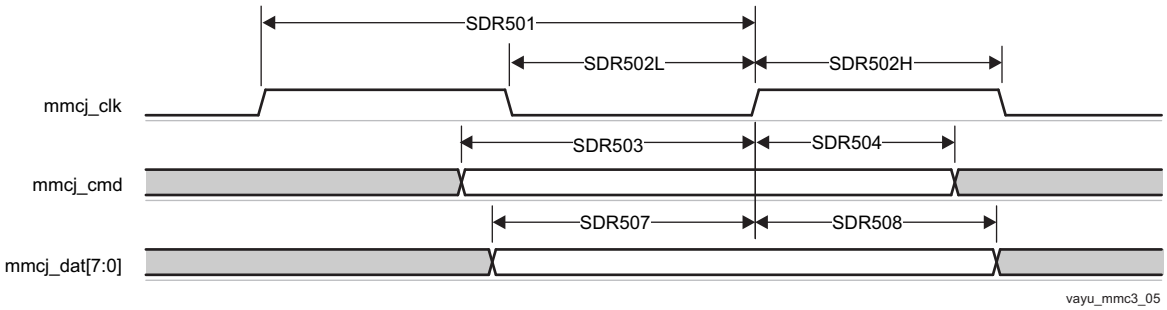


**Figure 7-89. MMC/SD/SDIOj in - High Speed SDR50 - Receiver Mode**

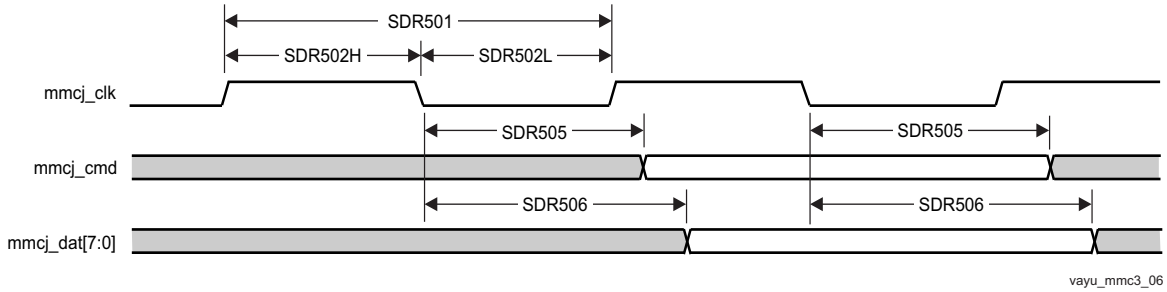


**Figure 7-90. MMC/SD/SDIOj in - High Speed SDR50 - Transmitter Mode**


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**NOTE**

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the Control Module chapter in the Device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for MMC3. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-133 *Manual Functions Mapping for MMC3* for a definition of the Manual modes.

Table 7-133 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-133. Manual Functions Mapping for MMC3**

| BALL | BALL NAME | MMC3_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 0 |
| AD4 | mmc3_clk | 0 | 386 | CFG_MMC3_CLK_IN | mmc3_clk |
| AD4 | mmc3_clk | 605 | 0 | CFG_MMC3_CLK_OUT | mmc3_clk |
| AC4 | mmc3_cmd | 0 | 0 | CFG_MMC3_CMD_IN | mmc3_cmd |
| AC4 | mmc3_cmd | 0 | 0 | CFG_MMC3_CMD_OEN | mmc3_cmd |
| AC4 | mmc3_cmd | 0 | 0 | CFG_MMC3_CMD_OUT | mmc3_cmd |
| AC7 | mmc3_dat0 | 171 | 0 | CFG_MMC3_DAT0_IN | mmc3_dat0 |
| AC7 | mmc3_dat0 | 0 | 0 | CFG_MMC3_DAT0_OEN | mmc3_dat0 |
| AC7 | mmc3_dat0 | 0 | 0 | CFG_MMC3_DAT0_OUT | mmc3_dat0 |
| AC6 | mmc3_dat1 | 221 | 0 | CFG_MMC3_DAT1_IN | mmc3_dat1 |
| AC6 | mmc3_dat1 | 0 | 0 | CFG_MMC3_DAT1_OEN | mmc3_dat1 |
| AC6 | mmc3_dat1 | 0 | 0 | CFG_MMC3_DAT1_OUT | mmc3_dat1 |
| AC9 | mmc3_dat2 | 0 | 0 | CFG_MMC3_DAT2_IN | mmc3_dat2 |
| AC9 | mmc3_dat2 | 0 | 0 | CFG_MMC3_DAT2_OEN | mmc3_dat2 |
| AC9 | mmc3_dat2 | 0 | 0 | CFG_MMC3_DAT2_OUT | mmc3_dat2 |
| AC3 | mmc3_dat3 | 474 | 0 | CFG_MMC3_DAT3_IN | mmc3_dat3 |
| AC3 | mmc3_dat3 | 0 | 0 | CFG_MMC3_DAT3_OEN | mmc3_dat3 |
| AC3 | mmc3_dat3 | 0 | 0 | CFG_MMC3_DAT3_OUT | mmc3_dat3 |
| AC8 | mmc3_dat4 | 792 | 0 | CFG_MMC3_DAT4_IN | mmc3_dat4 |
| AC8 | mmc3_dat4 | 0 | 0 | CFG_MMC3_DAT4_OEN | mmc3_dat4 |
| AC8 | mmc3_dat4 | 0 | 0 | CFG_MMC3_DAT4_OUT | mmc3_dat4 |
| AD6 | mmc3_dat5 | 782 | 0 | CFG_MMC3_DAT5_IN | mmc3_dat5 |
| AD6 | mmc3_dat5 | 0 | 0 | CFG_MMC3_DAT5_OEN | mmc3_dat5 |
| AD6 | mmc3_dat5 | 0 | 0 | CFG_MMC3_DAT5_OUT | mmc3_dat5 |
| AB8 | mmc3_dat6 | 942 | 0 | CFG_MMC3_DAT6_IN | mmc3_dat6 |
| AB8 | mmc3_dat6 | 0 | 0 | CFG_MMC3_DAT6_OEN | mmc3_dat6 |
| AB8 | mmc3_dat6 | 0 | 0 | CFG_MMC3_DAT6_OUT | mmc3_dat6 |
| AB5 | mmc3_dat7 | 636 | 0 | CFG_MMC3_DAT7_IN | mmc3_dat7 |
| AB5 | mmc3_dat7 | 0 | 0 | CFG_MMC3_DAT7_OEN | mmc3_dat7 |
| AB5 | mmc3_dat7 | 0 | 0 | CFG_MMC3_DAT7_OUT | mmc3_dat7 |

Manual IO Timings Modes must be used to ensure some IO timings for MMC4. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-134 *Manual Functions Mapping for MMC4* for a definition of the Manual modes.

Table 7-134 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-134. Manual Functions Mapping for MMC4**

| BALL | BALL NAME | MMC4_MANUAL1 | | MMC4_DS_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | A_DELAY (ps) | G_DELAY (ps) | | 3 |
| E25 | uart1_ctsn | 0 | 0 | 0 | 0 | CFG_UART1_CTSN_IN | mmc4_clk |
| E25 | uart1_ctsn | 1147 | 0 | 0 | 0 | CFG_UART1_CTSN_OUT | mmc4_clk |
| C27 | uart1_rtsn | 1834 | 0 | 307 | 0 | CFG_UART1_RTSN_IN | mmc4_cmd |
| C27 | uart1_rtsn | 0 | 0 | 0 | 0 | CFG_UART1_RTSN_OEN | mmc4_cmd |
| C27 | uart1_rtsn | 0 | 0 | 0 | 0 | CFG_UART1_RTSN_OUT | mmc4_cmd |
| D27 | uart2_ctsn | 2165 | 0 | 785 | 0 | CFG_UART2_CTSN_IN | mmc4_dat2 |
| D27 | uart2_ctsn | 0 | 0 | 0 | 0 | CFG_UART2_CTSN_OEN | mmc4_dat2 |
| D27 | uart2_ctsn | 0 | 0 | 0 | 0 | CFG_UART2_CTSN_OUT | mmc4_dat2 |
| C28 | uart2_rtsn | 1929 | 64 | 613 | 0 | CFG_UART2_RTSN_IN | mmc4_dat3 |
| C28 | uart2_rtsn | 0 | 0 | 0 | 0 | CFG_UART2_RTSN_OEN | mmc4_dat3 |
| C28 | uart2_rtsn | 0 | 0 | 0 | 0 | CFG_UART2_RTSN_OUT | mmc4_dat3 |
| D28 | uart2_rxd | 1935 | 128 | 683 | 0 | CFG_UART2_RXD_IN | mmc4_dat0 |
| D28 | uart2_rxd | 0 | 0 | 0 | 0 | CFG_UART2_RXD_OEN | mmc4_dat0 |
| D28 | uart2_rxd | 0 | 0 | 0 | 0 | CFG_UART2_RXD_OUT | mmc4_dat0 |
| D26 | uart2_txd | 2172 | 44 | 835 | 0 | CFG_UART2_TXD_IN | mmc4_dat1 |
| D26 | uart2_txd | 0 | 0 | 0 | 0 | CFG_UART2_TXD_OEN | mmc4_dat1 |
| D26 | uart2_txd | 0 | 0 | 0 | 0 | CFG_UART2_TXD_OUT | mmc4_dat1 |

## 7.24 General-Purpose Interface (GPIO)

The general-purpose interface combines eight general-purpose input/output (GPIO) banks. Each GPIO module provides 32 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 247 pins.

These pins can be configured for the following applications:

- Data input (capture)/output (drive)
- Keyboard interface with a debounce cell
- Interrupt generation in active mode upon the detection of external events. Detected events are processed by two parallel independent interrupt-generation submodules to support biprocessor operations
- Wake-up request generation in idle mode upon the detection of external events

**NOTE**

For more information, see the General-Purpose Interface chapter of the Device TRM.

**NOTE**

The general-purpose input/output i (i = 1 to 8) bank is also referred to as GPIOi.

## 7.25 Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)


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The device Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS) consists of dual 32-bit Load / Store RISC CPU cores - Programmable Real-Time Units (PRU0 and PRU1), shared, data, and instruction memories, internal peripheral modules, and an interrupt controller (PRU-ICSS_INTC). The programmable nature of the PRUs, along with their access to pins, events and all SoC resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, customer peripheral interfaces, and in off-loading tasks from the other processor cores of the system-on-chip (SoC).

The each PRU-ICSS includes the following main features:

- 21x Enhanced GPIs (EGPIs) and 21x Enhanced GPOs (EGPOs) with asynchronous capture and serial support per each PRU CPU core
- One Ethernet MII_RT module (PRU-ICSS_MII_RT) with two MII ports and configurable connections to PRUs
- 1 MDIO Port (PRU-ICSS_MII_MDIO)
- One Industrial Ethernet Peripheral (IEP) to manage/generate Industrial Ethernet functions
- 1 x 16550-compatible UART with a dedicated 192 MHz clock to support 12Mbps Profibus
- 1 Industrial Ethernet timer with 7/9 capture and 8 compare events
- 1 Enhanced Capture Module (ECAP)
- 1 Interrupt Controller (PRU-ICSS_INTC)
- A flexible power management support
- Integrated switched central resource with programmable priority
- Parity control supported by all memories

**CAUTION**

The IO timings provided in this section are only valid if signals within a single IOSET are used. The IOSETs are defined in the Table 7-154 and Table 7-155.

**NOTE**

For more information about PRU-ICSS subsystems interfaces, see the device TRM.

**NOTE**

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented in Table 4-3 and described in Device TRM, *Chapter 18 - Control Module*.

## 7.25.1 Programmable Real-Time Unit (PRU-ICSS PRU)

### 7.25.1.1 PRU-ICSS PRU Direct Input/Output Mode Electrical Data and Timing

**Table 7-135. PRU-ICSS PRU Timing Requirements - Direct Input Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(GPI)}$ | Pulse width, GPI | 2*P (1) | | ns |
| 2 | $t_{sk(GPI)}$ | Skew between GPI[20:0] signals | | 4.5 | ns |

(1) PRUSS_GICLK clock period

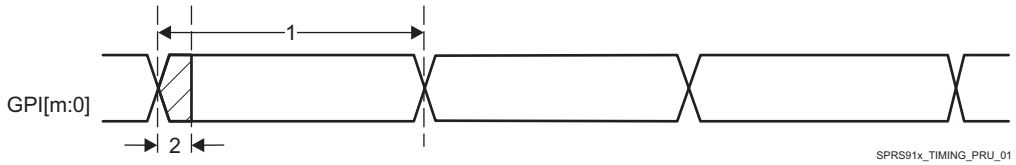


**Figure 7-91. PRU-ICSS PRU Direct Input Timing**

(1) m in GPI[m:0] = 20

**Table 7-136. PRU-ICSS PRU Switching Requirements – Direct Output Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(GPO)}$ | Pulse width, GPO | 2*P (1) | | ns |
| 2 | $t_{sk(GPO)}$ | Skew between GPO[20:0] signals | | 4.5 | ns |

(1) PRUSS_GICLK clock period

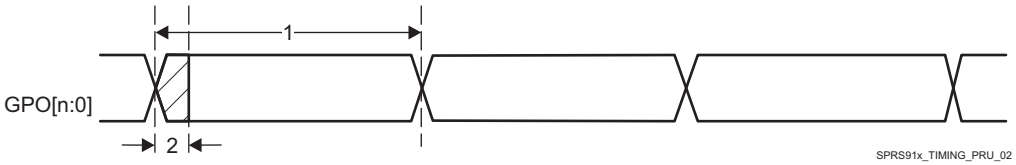


**Figure 7-92. PRU-ICSS PRU Direct Output Timing**

(1) n in GPO[n:0] = 20

### 7.25.1.2 PRU-ICSS PRU Parallel Capture Mode Electrical Data and Timing

**Table 7-137. PRU-ICSS PRU Timing Requirements - Parallel Capture Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(CLOCKIN)}$ | Cyle time, CLOCKIN | 20 | | ns |
| 2 | $t_{w(CLOCKIN_L)}$ | Pulse duration, CLOCKIN low | 9 | 11 | ns |
| 3 | $t_{w(CLOCKIN_H)}$ | Pulse duration, CLOCKIN high | 9 | 11 | ns |
| 4 | $t_{su(DATAIN-CLOCKIN)}$ | Setup time, DATAIN valid before CLOCKIN | 4.5 | | ns |
| 5 | $t_{h(CLOCKIN-DATAIN)}$ | Hold time, DATAIN valid after CLOCKIN | 0 | | ns |

(1) PRUSS_GICLK clock period

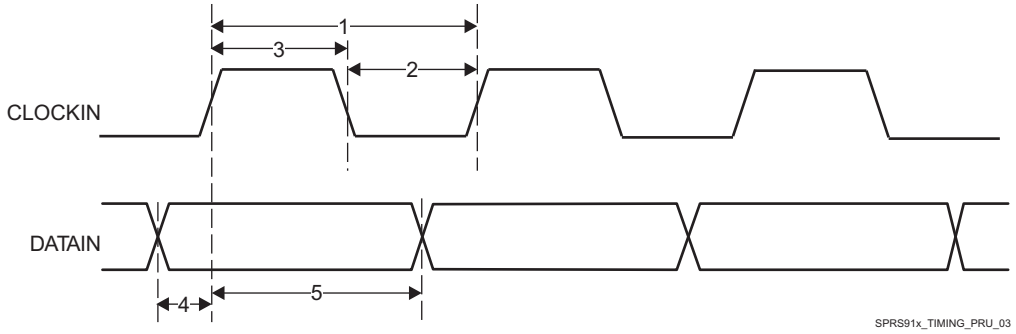


**Figure 7-93. PRU-ICSS PRU Parallel Capture Timing - Rising Edge Mode**


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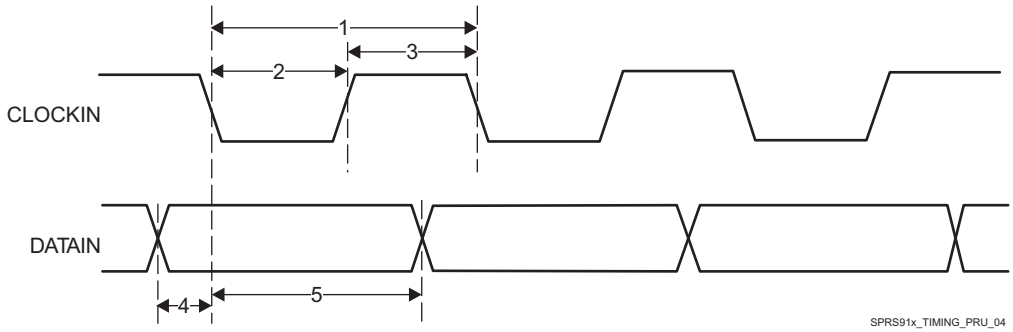


**Figure 7-94. PRU-ICSS PRU Parallel Capture Timing - Falling Edge Mode**

#### 7.25.1.3 PRU-ICSS PRU Shift Mode Electrical Data and Timing

**Table 7-138. PRU-ICSS PRU Timing Requirements – Shift In Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(DATAIN)}$ | Cycle time, DATAIN | 10.00 | | ns |
| 2 | $t_{w(DATAIN)}$ | Pulse width, DATAIN | 0.45*P (1) | 0.55*P (1) | ns |

(1) P = 10.00ns

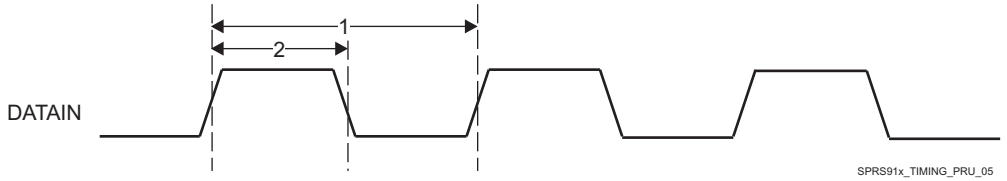


**Figure 7-95. PRU-ICSS PRU Shift In Timing**

**Table 7-139. PRU-ICSS PRU Switching Requirements - Shift Out Mode**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(CLOCKOUT)}$ | Cycle time, CLOCKOUT | 10.00 | | ns |
| 2 | $t_{w(CLOCKOUT)}$ | Pulse width, CLOCKOUT | 0.45*P (1) | 0.55*P (1) | ns |
| 3 | $t_{d(CLOCKOUT-DATAOUT)}$ | Delay time, CLOCKOUT to DATAOUT Valid | -3.00 | 3.60 | ns |

(1) P = 10.00ns

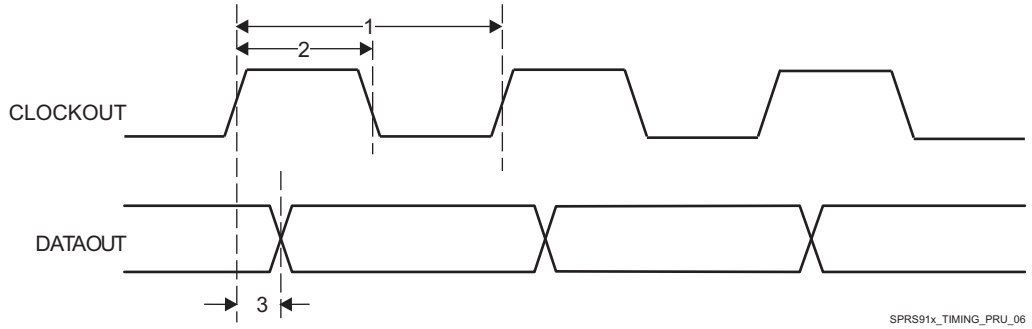


**Figure 7-96. PRU-ICSS PRU Shift Out Timing**

### *7.25.2 PRU-ICSS EtherCAT (PRU-ICSS ECAT)*

#### 7.25.2.1 PRU-ICSS ECAT Electrical Data and Timing

**Table 7-140. PRU-ICSS ECAT Timing Requirements – Input Validated With LATCH_IN**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(EDIO_LATCH_IN)}$ | Pulse width, EDIO_LATCH_IN | 100.00 | | ns |
| 2 | $t_{su(EDIO_DATA_IN-EDIO_LATCH_IN)}$ | Setup time, EDIO_DATA_IN valid before EDIO_LATCH_IN active edge | 20.00 | | ns |
| 3 | $t_{h(EDIO_LATCH_IN-EDIO_DATA_IN)}$ | Hold time, EDIO_DATA_IN valid after EDIO_LATCH_IN active edge | 20.00 | | ns |

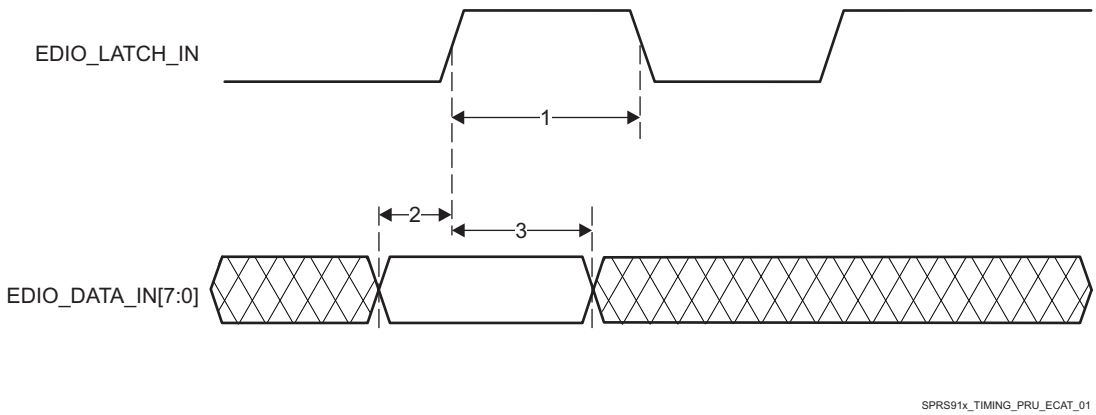


**Figure 7-97. PRU-ICSS ECAT Input Validated with LATCH_IN Timing**

**Table 7-141. PRU-ICSS ECAT Timing Requirements – Input Validated With SYNCx**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(EDC_SYNCx_OUT)}$ | Pulse width, EDC_SYNCx_OUT | 100.00 | | ns |
| 2 | $t_{su(EDIO_DATA_IN-EDC_SYNCx_OUT)}$ | Setup time, EDIO_DATA_IN valid before EDC_SYNCx_OUT active edge | 20.00 | | ns |
| 3 | $t_{h(EDC_SYNCx_OUT-EDIO_DATA_IN)}$ | Hold time, EDIO_DATA_IN valid after EDC_SYNCx_OUT active edge | 20.00 | | ns |

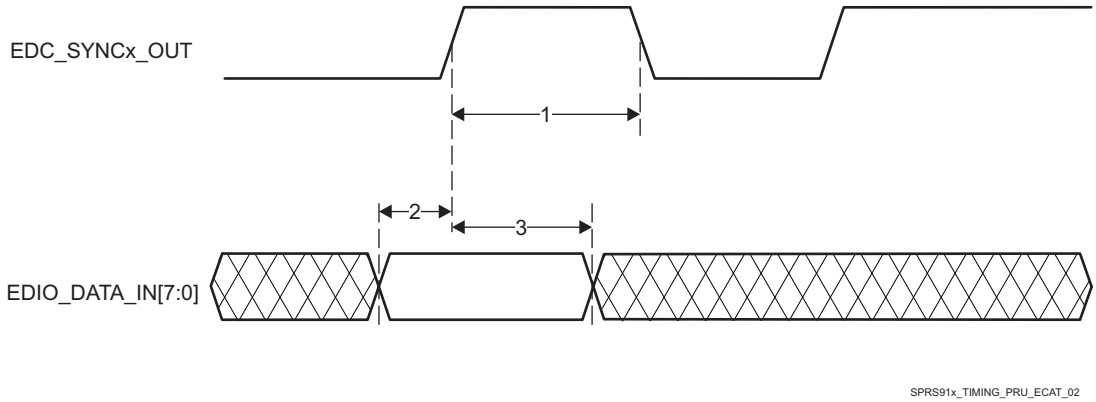


**Figure 7-98. PRU-ICSS ECAT Input Validated With SYNCx Timing**

**Table 7-142. PRU-ICSS ECAT Timing Requirements – Input Validated With Start of Frame (SOF)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(EDIO_SOF)}$ | Pulse duration, EDIO_SOF | 4*P (1) | 5*P (1) | ns |
| 2 | $t_{su(EDIO_DATA_IN-EDIO_SOF)}$ | Setup time, EDIO_DATA_IN valid before EDIO_SOF active edge | 20.00 | | ns |
| 3 | $t_{h(EDIO_SOF-EDIO_DATA_IN)}$ | Hold time, EDIO_DATA_IN valid after EDIO_SOF active edge | 20.00 | | ns |


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(1) PRUSS_IEP_CLK clock period

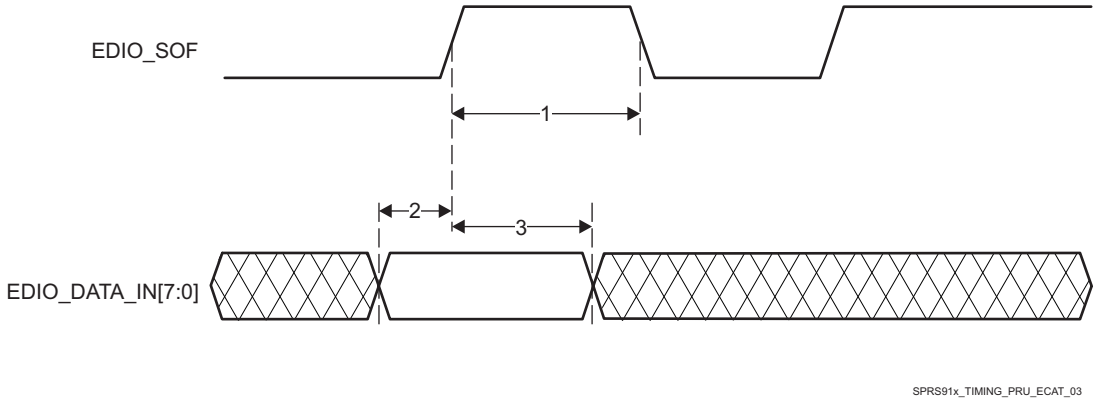


**Figure 7-99. PRU-ICSS ECAT Input Validated With SOF**

**Table 7-143. PRU-ICSS ECAT Timing Requirements - LATCHx_IN**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(EDC_LATCHx_IN)}$ | Pulse duration, EDC_LATCHx_IN | 3*P (1) | | ns |

(1) PRUSS_IEP_CLK clock period

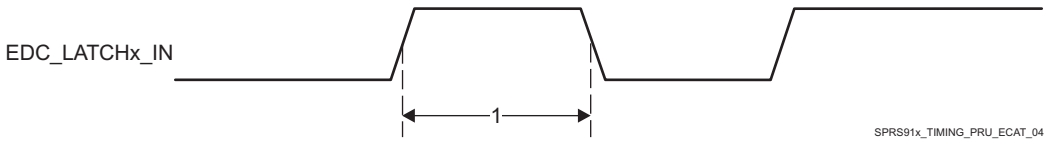


**Figure 7-100. PRU-ICSS ECAT LATCHx_IN Timing**

**Table 7-144. PRU-ICSS ECAT Switching Requirements - Digital IOs**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{sk(EDIO_DATA_OUT)}$ | EDIO_DATA_OUT skew | | 8 | ns |

## *7.25.3 PRU-ICSS MII_RT and Switch*

### 7.25.3.1 PRU-ICSS MDIO Electrical Data and Timing

**Table 7-145. PRU-ICSS MDIO Timing Requirements – MDIO_DATA**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{su(MDIO-MDC)}$ | Setup time, MDIO valid before MDC high | 90 | | ns |
| 2 | $t_{h(MDIO-MDC)}$ | Hold time, MDIO valid from MDC high | 0 | | ns |

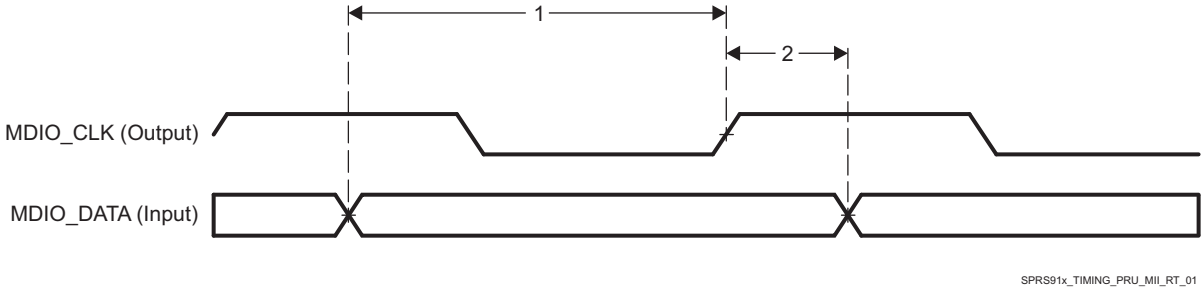


**Figure 7-101. PRU-ICSS MDIO_DATA Timing - Input Mode**

**Table 7-146. PRU-ICSS MDIO Switching Characteristics - MDIO_CLK**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(MDC)}$ | Cycle time, MDC | 400 | | ns |
| 2 | $t_{w(MDCH)}$ | Pulse duration, MDC high | 160 | | ns |
| 3 | $t_{w(MDCL)}$ | Pulse duration, MDC low | 160 | | ns |
| 4 | $t_{t(MDC)}$ | Transition time, MDC | | 5 | ns |

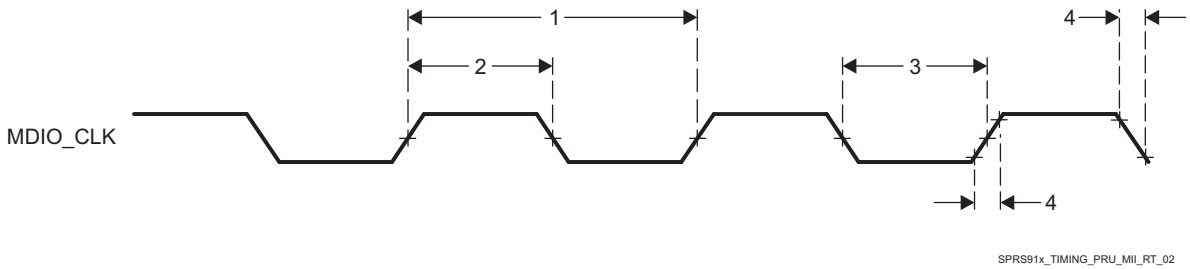


**Figure 7-102. PRU-ICSS MDIO_CLK Timing**

**Table 7-147. PRU-ICSS MDIO Switching Characteristics – MDIO_DATA**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{d(MDC-MDIO)}$ | Delay time, MDC high to MDIO valid | 0 | 390 | ns |

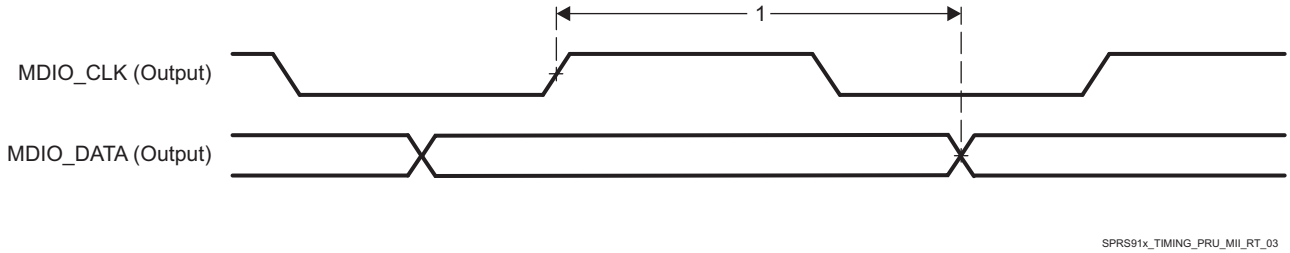


**Figure 7-103. PRU-ICSS MDIO_DATA Timing – Output Mode**

### 7.25.3.2 PRU-ICSS MII_RT Electrical Data and Timing

**NOTE**

In order to ensure the MII_RT IO timing values published in the device data manual, the PRUSS_GICLK clock must be configured for 200MHz (default value) and the TX_CLK_DELAY bitfield in the PRUSS_MII_RT_TXCFG0/1 register must be configured as follows:

- 100 Mbps mode: 6h (non-default value)
- 10 Mbps mode: 0h (default value)

**Table 7-148. PRU-ICSS MII_RT Timing Requirements – MII[x]_RXCLK**

| NO. | PARAMETER | DESCRIPTION | SPEED | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(RX_CLK)}$ | Cycle time, RX_CLK | 10 Mbps | 399.96 | 400.04 | ns |
| | | | 100 Mbps | 39.996 | 40.004 | ns |
| 2 | $t_{w(RX_CLKH)}$ | Pulse duration, RX_CLK high | 10 Mbps | 140 | 260 | ns |
| | | | 100 Mbps | 14 | 26 | ns |
| 3 | $t_{w(RX_CLKL)}$ | Pulse duration, RX_CLK low | 10 Mbps | 140 | 260 | ns |
| | | | 100 Mbps | 14 | 26 | ns |


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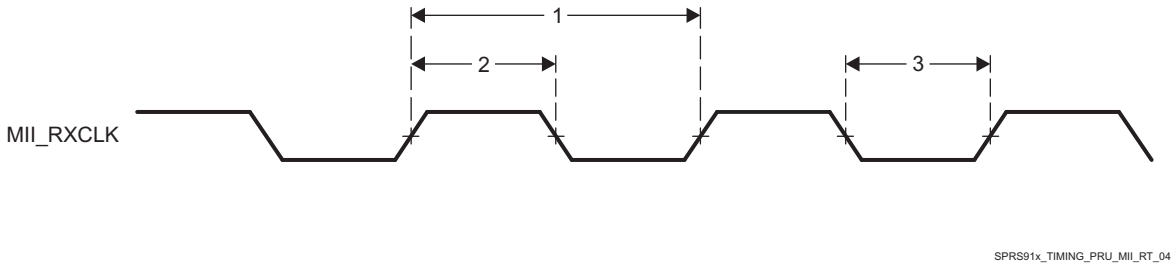


**Figure 7-104. PRU-ICSS MII[x]_RXCLK Timing**

**Table 7-149. PRU-ICSS MII_RT Timing Requirements - MII[x]_TXCLK**

| NO. | PARAMETER | DESCRIPTION | SPEED | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(TX_CLK)}$ | Cycle time, TX_CLK | 10 Mbps | 399.96 | 400.04 | ns |
| | | | 100 Mbps | 39.996 | 40.004 | ns |
| 2 | $t_{w(TX_CLKH)}$ | Pulse duration, TX_CLK high | 10 Mbps | 140 | 260 | ns |
| | | | 100 Mbps | 14 | 26 | ns |
| 3 | $t_{w(TX_CLKL)}$ | Pulse duration, TX_CLK low | 10 Mbps | 140 | 260 | ns |
| | | | 100 Mbps | 14 | 26 | ns |
| 4 | $t_{t(TX_CLK)}$ | Transition time, TX_CLK | 10 Mbps | | 3 | ns |
| | | | 100 Mbps | | 3 | ns |

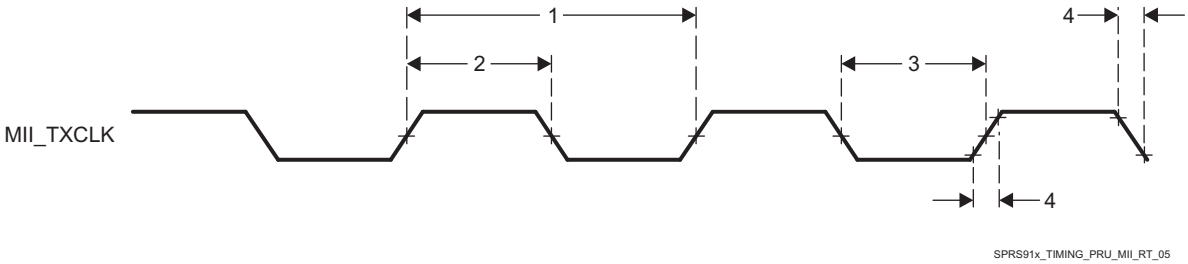


**Figure 7-105. PRU-ICSS MII[x]_TXCLK Timing**

**Table 7-150. PRU-ICSS MII_RT Timing Requirements - MII_RXD[3:0], MII_RXDV, and MII_RXER**

| NO. | PARAMETER | DESCRIPTION | SPEED | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{su(RXD\text{-}RX_CLK)}$ | Setup time, RXD[3:0] valid before RX_CLK | 10 Mbps | 8 | | ns |
| | $t_{su(RX_DV\text{-}RX_CLK)}$ | Setup time, RX_DV valid before RX_CLK | | | | |
| | $t_{su(RX_ER\text{-}RX_CLK)}$ | Setup time, RX_ER valid before RX_CLK | | | | |
| | $t_{su(RXD\text{-}RX_CLK)}$ | Setup time, RXD[3:0] valid before RX_CLK | 100 Mbps | 8 | | ns |
| | $t_{su(RX_DV\text{-}RX_CLK)}$ | Setup time, RX_DV valid before RX_CLK | | | | |
| | $t_{su(RX_ER\text{-}RX_CLK)}$ | Setup time, RX_ER valid before RX_CLK | | | | |
| 2 | $t_{h(RX_CLK\text{-}RXD)}$ | Hold time RXD[3:0] valid after RX_CLK | 10 Mbps | 8 | | ns |
| | $t_{h(RX_CLK\text{-}RX_DV)}$ | Hold time RX_DV valid after RX_CLK | | | | |
| | $t_{h(RX_CLK\text{-}RX_ER)}$ | Hold time RX_ER valid after RX_CLK | | | | |
| | $t_{h(RX_CLK\text{-}RXD)}$ | Hold time RXD[3:0] valid after RX_CLK | 100 Mbps | 8 | | ns |
| | $t_{h(RX_CLK\text{-}RX_DV)}$ | Hold time RX_DV valid after RX_CLK | | | | |
| | $t_{h(RX_CLK\text{-}RX_ER)}$ | Hold time RX_ER valid after RX_CLK | | | | |

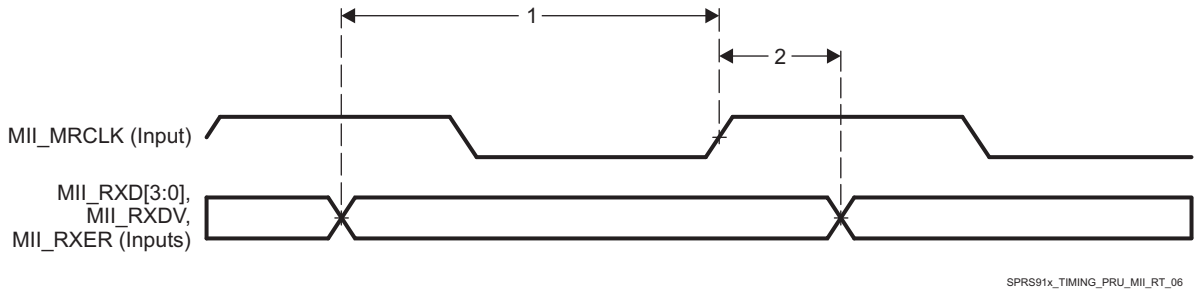


**Figure 7-106. PRU-ICSS MII_RXD[3:0], MII_RXDV, and MII_RXER Timing**

**Table 7-151. PRU-ICSS MII_RT Switching Characteristics - MII_TXD[3:0] and MII_TXEN**

| NO. | PARAMETER | DESCRIPTION | SPEED | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{d(TX_CLK-TXD)}$ | Delay time, TX_CLK high to TXD[3:0] valid | 10 Mbps | 5 | 33 | ns |
| | $t_{d(TX_CLK-TX_EN)}$ | Delay time, TX_CLK to TX_EN valid | | | | |
| | $t_{d(TX_CLK-TXD)}$ | Delay time, TX_CLK high to TXD[3:0] valid | 100 Mbps | 5 | 25 | ns |
| | $t_{d(TX_CLK-TX_EN)}$ | Delay time, TX_CLK to TX_EN valid | | | | |

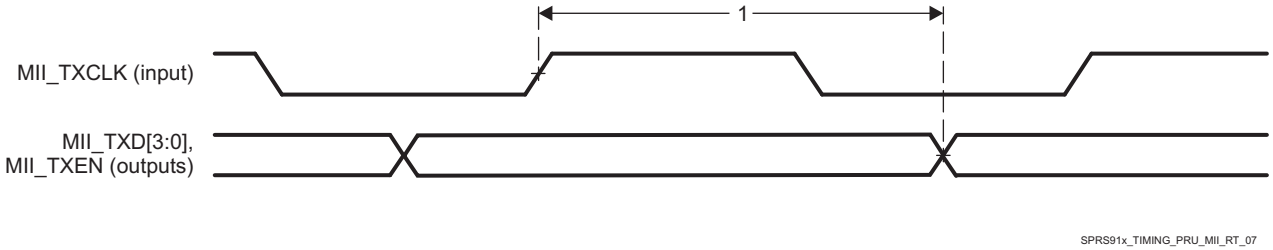


**Figure 7-107. PRU-ICSS MII_TXD[3:0], MII_TXEN Timing**

### *7.25.4 PRU-ICSS Universal Asynchronous Receiver Transmitter (PRU-ICSS UART)*

**Table 7-152. Timing Requirements for PRU-ICSS UART Receive**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 3 | $t_{w(RX)}$ | Pulse duration, receive start, stop, data bit | 0.96U (1) | 1.05U | ns |

(1) U = UART baud time = 1/programmed baud rate.

**Table 7-153. Switching Characteristics Over Recommended Operating Conditions for PRU-ICSS UART Transmit**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $f$baud(baud) | Maximum programmable baud rate | 0 | 12 | MHz |
| 2 | $t_{w(TX)}$ | Pulse duration, transmit start, stop, data bit | U - 2 (1) | U + 2 | ns |


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(1) U = UART baud time = 1/programmed baud rate.

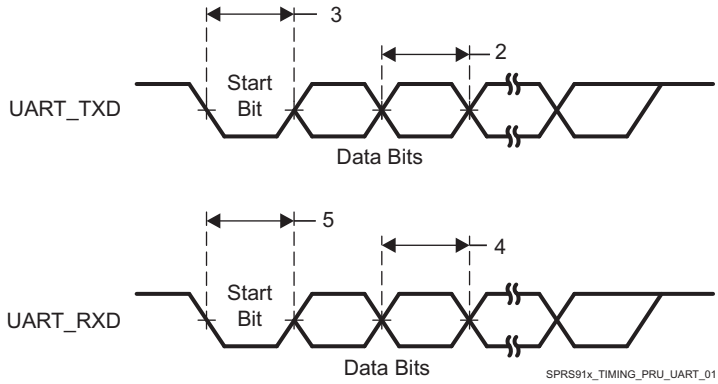


**Figure 7-108. PRU-ICSS UART Timing**

### *7.25.5 PRU-ICSS IOSETs*

In Table 7-154 and Table 7-155 are presented the specific groupings of signals (IOSET) for use with PRU-ICSS1 and PRU-ICSS2.

**Table 7-154. PRU-ICSS1 IOSETs**

| SIGNALS | IOSET1 | | IOSET2 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| PRU-ICSS1 | | | | |
| pr1_pru1_gpi20 | A4 | 12 | | |
| pr1_pru1_gpi19 | B5 | 12 | | |
| pr1_pru1_gpi18 | B4 | 12 | | |
| pr1_pru1_gpi17 | B3 | 12 | | |
| pr1_pru1_gpi16 | A3 | 12 | | |
| pr1_pru1_gpi15 | C5 | 12 | | |
| pr1_pru1_gpi14 | D6 | 12 | | |
| pr1_pru1_gpi13 | B2 | 12 | | |
| pr1_pru1_gpi12 | C4 | 12 | | |
| pr1_pru1_gpi11 | C3 | 12 | | |
| pr1_pru1_gpi10 | C2 | 12 | | |
| pr1_pru1_gpo20 | A4 | 13 | | |
| pr1_pru1_gpo19 | B5 | 13 | | |
| pr1_pru1_gpo18 | B4 | 13 | | |
| pr1_pru1_gpo17 | B3 | 13 | | |
| pr1_pru1_gpo16 | A3 | 13 | | |
| pr1_pru1_gpo15 | C5 | 13 | | |
| pr1_pru1_gpo14 | D6 | 13 | | |
| pr1_pru1_gpo13 | B2 | 13 | | |
| pr1_pru1_gpo12 | C4 | 13 | | |
| pr1_pru1_gpo11 | C3 | 13 | | |
| pr1_pru1_gpo10 | C2 | 13 | | |
| pr1_pru1_gpi9 | D5 | 12 | | |
| pr1_pru1_gpi8 | F6 | 12 | | |
| pr1_pru1_gpi7 | D3 | 12 | | |
| pr1_pru1_gpi6 | E6 | 12 | | |

**Table 7-154. PRU-ICSS1 IOSETs (continued)**

| SIGNALS | IOSET1 | | IOSET2 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| pr1_pru1_gpi5 | F5 | 12 | | |
| pr1_pru1_gpi4 | E4 | 12 | | |
| pr1_pru1_gpi3 | C1 | 12 | | |
| pr1_pru1_gpi2 | F4 | 12 | | |
| pr1_pru1_gpi1 | D2 | 12 | | |
| pr1_pru1_gpi0 | E2 | 12 | | |
| pr1_pru1_gpo9 | D5 | 13 | | |
| pr1_pru1_gpo8 | F6 | 13 | | |
| pr1_pru1_gpo7 | D3 | 13 | | |
| pr1_pru1_gpo6 | E6 | 13 | | |
| pr1_pru1_gpo5 | F5 | 13 | | |
| pr1_pru1_gpo4 | E4 | 13 | | |
| pr1_pru1_gpo3 | C1 | 13 | | |
| pr1_pru1_gpo2 | F4 | 13 | | |
| pr1_pru1_gpo1 | D2 | 13 | | |
| pr1_pru1_gpo0 | E2 | 13 | | |
| pr1_pru0_gpi20 | AD3 | 12 | | |
| pr1_pru0_gpi19 | AD2 | 12 | | |
| pr1_pru0_gpi18 | AE6 | 12 | | |
| pr1_pru0_gpi17 | AE2 | 12 | | |
| pr1_pru0_gpi16 | AE1 | 12 | | |
| pr1_pru0_gpi15 | AE5 | 12 | | |
| pr1_pru0_gpi14 | AE3 | 12 | | |
| pr1_pru0_gpi13 | AF1 | 12 | | |
| pr1_pru0_gpi12 | AF4 | 12 | | |
| pr1_pru0_gpi11 | AF3 | 12 | | |
| pr1_pru0_gpi10 | AF6 | 12 | | |
| pr1_pru0_gpo20 | AD3 | 13 | | |
| pr1_pru0_gpo19 | AD2 | 13 | | |
| pr1_pru0_gpo18 | AE6 | 13 | | |
| pr1_pru0_gpo17 | AE2 | 13 | | |
| pr1_pru0_gpo16 | AE1 | 13 | | |
| pr1_pru0_gpo15 | AE5 | 13 | | |
| pr1_pru0_gpo14 | AE3 | 13 | | |
| pr1_pru0_gpo13 | AF1 | 13 | | |
| pr1_pru0_gpo12 | AF4 | 13 | | |
| pr1_pru0_gpo11 | AF3 | 13 | | |
| pr1_pru0_gpo10 | AF6 | 13 | | |
| pr1_pru0_gpi9 | AF2 | 12 | | |
| pr1_pru0_gpi8 | AG5 | 12 | | |
| pr1_pru0_gpi7 | AG3 | 12 | | |
| pr1_pru0_gpi6 | AG2 | 12 | | |
| pr1_pru0_gpi5 | AG4 | 12 | | |
| pr1_pru0_gpi4 | AH4 | 12 | | |
| pr1_pru0_gpi3 | AG6 | 12 | | |
| pr1_pru0_gpi2 | AH5 | 12 | | |


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**Table 7-154. PRU-ICSS1 IOSETs (continued)**

| SIGNALS | IOSET1 | | IOSET2 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| pr1_pru0_gpi1 | AH3 | 12 | | |
| pr1_pru0_gpi0 | AH6 | 12 | | |
| pr1_pru0_gpo9 | AF2 | 13 | | |
| pr1_pru0_gpo8 | AG5 | 13 | | |
| pr1_pru0_gpo7 | AG3 | 13 | | |
| pr1_pru0_gpo6 | AG2 | 13 | | |
| pr1_pru0_gpo5 | AG4 | 13 | | |
| pr1_pru0_gpo4 | AH4 | 13 | | |
| pr1_pru0_gpo3 | AG6 | 13 | | |
| pr1_pru0_gpo2 | AH5 | 13 | | |
| pr1_pru0_gpo1 | AH3 | 13 | | |
| pr1_pru0_gpo0 | AH6 | 13 | | |
| pr1_mii1_crs | A4 | 11 | | |
| pr1_mii1_rxlink | B4 | 11 | | |
| pr1_mii1_col | B5 | 11 | | |
| pr1_mii0_col | V1 | 11 | | |
| pr1_mii0_rxlink | U4 | 11 | | |
| pr1_mii0_crs | V7 | 11 | | |
| pr1_edio_data_out7 | AD3 | 11 | D1 | 13 |
| pr1_edio_data_out6 | AD2 | 11 | F3 | 13 |
| pr1_edio_data_out5 | AE6 | 11 | F2 | 13 |
| pr1_edio_data_out4 | AE2 | 11 | G6 | 13 |
| pr1_edio_data_out3 | AE1 | 11 | G1 | 13 |
| pr1_edio_data_out2 | AE5 | 11 | H7 | 13 |
| pr1_edio_data_out1 | AE3 | 11 | G2 | 13 |
| pr1_edio_data_out0 | AF1 | 11 | E1 | 13 |
| pr1_edio_data_in7 | AD3 | 10 | D1 | 12 |
| pr1_edio_data_in6 | AD2 | 10 | F3 | 12 |
| pr1_edio_data_in5 | AE6 | 10 | F2 | 12 |
| pr1_edio_data_in4 | AE2 | 10 | G6 | 12 |
| pr1_edio_data_in3 | AE1 | 10 | G1 | 12 |
| pr1_edio_data_in2 | AE5 | 10 | H7 | 12 |
| pr1_edio_data_in1 | AE3 | 10 | G2 | 12 |
| pr1_edio_data_in0 | AF1 | 10 | E1 | 12 |
| pr1_edio_sof | AF4 | 10 | F4 | 11 |
| pr1_edc_latch0_in | AG3 | 10 | E2 | 11 |
| pr1_edc_latch1_in | AG5 | 10 | | |
| pr1_edc_sync1_out | AF6 | 10 | | |
| pr1_edc_sync0_out | AF2 | 10 | D2 | 11 |
| pr1_edio_latch_in | AF3 | 10 | | |
| pr1_uart0_cts_n | G1 | 11 | F11 | 10 |
| pr1_uart0_rts_n | G6 | 11 | G10 | 10 |
| pr1_uart0_txd | F3 | 11 | G11 | 10 |
| pr1_uart0_rxd | F2 | 11 | F10 | 10 |
| pr1_ecap0_ecap_capin_apwm_o | D1 | 11 | E9 | 10 |
| **PRU-ICSS1 MII** | | | | |

### Table 7-154. PRU-ICSS1 IOSETs (continued)

| SIGNALS | IOSET1 | | IOSET2 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| pr1_mii1_txd3 | F5 | 11 | | |
| pr1_mii1_txd2 | E6 | 11 | | |
| pr1_mii1_txd1 | D5 | 11 | | |
| pr1_mii1_txd0 | C2 | 11 | | |
| pr1_mii1_rxd3 | B2 | 11 | | |
| pr1_mii1_rxd2 | D6 | 11 | | |
| pr1_mii1_rxd1 | C5 | 11 | | |
| pr1_mii1_rxd0 | A3 | 11 | | |
| pr1_mii1_rxdv | C4 | 11 | | |
| pr1_mii1_txen | E4 | 11 | | |
| pr1_mii1_rxer | B3 | 11 | | |
| pr1_mii_mr1_clk | C3 | 11 | | |
| pr1_mii_mt1_clk | C1 | 11 | | |
| pr1_mii0_txd3 | V5 | 11 | | |
| pr1_mii0_txd2 | V4 | 11 | | |
| pr1_mii0_txd1 | Y2 | 11 | | |
| pr1_mii0_txd0 | W2 | 11 | | |
| pr1_mii0_rxd3 | W9 | 11 | | |
| pr1_mii0_rxd2 | V9 | 11 | | |
| pr1_mii0_rxd1 | V6 | 11 | | |
| pr1_mii0_rxd0 | U6 | 11 | | |
| pr1_mii0_rxdv | V2 | 11 | | |
| pr1_mii0_txen | V3 | 11 | | |
| pr1_mii0_rxer | U7 | 11 | | |
| pr1_mii_mt0_clk | U5 | 11 | | |
| pr1_mii_mr0_clk | Y1 | 11 | | |
| pr1_mdio_mdclk | D3 | 11 | | |
| pr1_mdio_data | F6 | 11 | | |

### Table 7-155. PRU-ICSS2 IOSETs

| SIGNALS | IOSET1 | | IOSET2 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| PRU-ICSS2 | | | | |
| pr2_pru1_gpi20 | F10 | 12 | F10 | 12 |
| pr2_pru1_gpi19 | G10 | 12 | G10 | 12 |
| pr2_pru1_gpi18 | F11 | 12 | F11 | 12 |
| pr2_pru1_gpi17 | E11 | 12 | E11 | 12 |
| pr2_pru1_gpi16 | W2 | 12 | G14 | 12 |
| pr2_pru1_gpi15 | Y2 | 12 | A13 | 12 |
| pr2_pru1_gpi14 | V3 | 12 | E14 | 12 |
| pr2_pru1_gpi13 | V4 | 12 | A12 | 12 |
| pr2_pru1_gpi12 | V5 | 12 | B13 | 12 |
| pr2_pru1_gpi11 | U5 | 12 | A11 | 12 |
| pr2_pru1_gpi10 | U6 | 12 | B12 | 12 |
| pr2_pru1_gpi9 | V6 | 12 | F12 | 12 |
| pr2_pru1_gpi8 | U7 | 12 | G12 | 12 |


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**Table 7-155. PRU-ICSS2 IOSETs (continued)**

| SIGNALS | IOSET1 | | IOSET2 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| pr2_pru1_gpi7 | V7 | 12 | C14 | 12 |
| pr2_pru1_gpi6 | V9 | 12 | E17 | 12 |
| pr2_pru1_gpi5 | W9 | 12 | D18 | 12 |
| pr2_pru1_gpi4 | Y1 | 12 | AA4 | 12 |
| pr2_pru1_gpi3 | V2 | 12 | AB3 | 12 |
| pr2_pru1_gpi2 | U3 | 12 | AB9 | 12 |
| pr2_pru1_gpi1 | U4 | 12 | AA3 | 12 |
| pr2_pru1_gpi0 | V1 | 12 | D17 | 12 |
| pr2_pru1_gpo20 | F10 | 13 | F10 | 13 |
| pr2_pru1_gpo19 | G10 | 13 | G10 | 13 |
| pr2_pru1_gpo18 | F11 | 13 | F11 | 13 |
| pr2_pru1_gpo17 | E11 | 13 | E11 | 13 |
| pr2_pru1_gpo16 | W2 | 13 | G14 | 13 |
| pr2_pru1_gpo15 | Y2 | 13 | A13 | 13 |
| pr2_pru1_gpo14 | V3 | 13 | E14 | 13 |
| pr2_pru1_gpo13 | V4 | 13 | A12 | 13 |
| pr2_pru1_gpo12 | V5 | 13 | B13 | 13 |
| pr2_pru1_gpo11 | U5 | 13 | A11 | 13 |
| pr2_pru1_gpo10 | U6 | 13 | B12 | 13 |
| pr2_pru1_gpo9 | V6 | 13 | F12 | 13 |
| pr2_pru1_gpo8 | U7 | 13 | G12 | 13 |
| pr2_pru1_gpo7 | V7 | 13 | C14 | 13 |
| pr2_pru1_gpo6 | V9 | 13 | E17 | 13 |
| pr2_pru1_gpo5 | W9 | 13 | D18 | 13 |
| pr2_pru1_gpo4 | Y1 | 13 | AA4 | 13 |
| pr2_pru1_gpo3 | V2 | 13 | AB3 | 13 |
| pr2_pru1_gpo2 | U3 | 13 | AB9 | 13 |
| pr2_pru1_gpo1 | U4 | 13 | AA3 | 13 |
| pr2_pru1_gpo0 | V1 | 13 | D17 | 13 |
| pr2_pru0_gpi20 | A10 | 12 | F14 | 12 |
| pr2_pru0_gpi19 | B9 | 12 | A18 | 12 |
| pr2_pru0_gpi18 | A9 | 12 | A19 | 12 |
| pr2_pru0_gpi17 | C9 | 12 | A16 | 12 |
| pr2_pru0_gpi16 | A8 | 12 | C15 | 12 |
| pr2_pru0_gpi15 | A7 | 12 | C17 | 12 |
| pr2_pru0_gpi14 | B8 | 12 | B19 | 12 |
| pr2_pru0_gpi13 | B7 | 12 | F15 | 12 |
| pr2_pru0_gpi12 | C7 | 12 | B18 | 12 |
| pr2_pru0_gpi11 | C8 | 12 | AB5 | 12 |
| pr2_pru0_gpi10 | C6 | 12 | AB8 | 12 |
| pr2_pru0_gpi9 | A5 | 12 | AD6 | 12 |
| pr2_pru0_gpi8 | D8 | 12 | AC8 | 12 |
| pr2_pru0_gpi7 | D7 | 12 | AC3 | 12 |
| pr2_pru0_gpi6 | D9 | 12 | AC9 | 12 |
| pr2_pru0_gpi5 | E8 | 12 | AC6 | 12 |
| pr2_pru0_gpi4 | E7 | 12 | AC7 | 12 |

**Table 7-155. PRU-ICSS2 IOSETs (continued)**

| SIGNALS | IOSET1 | | IOSET2 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| pr2_pru0_gpi3 | F8 | 12 | AC4 | 12 |
| pr2_pru0_gpi2 | F9 | 12 | AD4 | 12 |
| pr2_pru0_gpi1 | E9 | 12 | AB4 | 12 |
| pr2_pru0_gpi0 | G11 | 12 | AC5 | 12 |
| pr2_pru0_gpo20 | A10 | 13 | F14 | 13 |
| pr2_pru0_gpo19 | B9 | 13 | A18 | 13 |
| pr2_pru0_gpo18 | A9 | 13 | A19 | 13 |
| pr2_pru0_gpo17 | C9 | 13 | A16 | 13 |
| pr2_pru0_gpo16 | A8 | 13 | C15 | 13 |
| pr2_pru0_gpo15 | A7 | 13 | C17 | 13 |
| pr2_pru0_gpo14 | B8 | 13 | B19 | 13 |
| pr2_pru0_gpo13 | B7 | 13 | F15 | 13 |
| pr2_pru0_gpo12 | C7 | 13 | B18 | 13 |
| pr2_pru0_gpo11 | C8 | 13 | AB5 | 13 |
| pr2_pru0_gpo10 | C6 | 13 | AB8 | 13 |
| pr2_pru0_gpo9 | A5 | 13 | AD6 | 13 |
| pr2_pru0_gpo8 | D8 | 13 | AC8 | 13 |
| pr2_pru0_gpo7 | D7 | 13 | AC3 | 13 |
| pr2_pru0_gpo6 | D9 | 13 | AC9 | 13 |
| pr2_pru0_gpo5 | E8 | 13 | AC6 | 13 |
| pr2_pru0_gpo4 | E7 | 13 | AC7 | 13 |
| pr2_pru0_gpo3 | F8 | 13 | AC4 | 13 |
| pr2_pru0_gpo2 | F9 | 13 | AD4 | 13 |
| pr2_pru0_gpo1 | E9 | 13 | AB4 | 13 |
| pr2_pru0_gpo0 | G11 | 13 | AC5 | 13 |
| pr2_mii1_crs | E17 | 11 | | |
| pr2_mii1_rxlink | C17 | 11 | | |
| pr2_mii0_crs | B18 | 11 | | |
| pr2_mii0_rxlink | A16 | 11 | | |
| pr2_mii0_col | F15 | 11 | | |
| pr2_mii1_col | D18 | 11 | | |
| pr2_edio_data_out7 | A10 | 11 | | |
| pr2_edio_data_out6 | B9 | 11 | | |
| pr2_edio_data_out5 | A9 | 11 | | |
| pr2_edio_data_out4 | C9 | 11 | | |
| pr2_edio_data_out3 | A8 | 11 | | |
| pr2_edio_data_out2 | A7 | 11 | | |
| pr2_edio_data_out1 | B8 | 11 | | |
| pr2_edio_data_out0 | B7 | 11 | | |
| pr2_edio_data_in7 | A10 | 10 | | |
| pr2_edio_data_in6 | B9 | 10 | | |
| pr2_edio_data_in5 | A9 | 10 | | |
| pr2_edio_data_in4 | C9 | 10 | | |
| pr2_edio_data_in3 | A8 | 10 | | |
| pr2_edio_data_in2 | A7 | 10 | | |
| pr2_edio_data_in1 | B8 | 10 | | |


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**Table 7-155. PRU-ICSS2 IOSETs (continued)**

| SIGNALS | IOSET1 | | IOSET2 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| pr2_edio_data_in0 | B7 | 10 | | |
| pr2_edio_latch_in | D9 | 10 | | |
| pr2_edio_sof | D7 | 10 | | |
| pr2_edc_sync0_out | E7 | 10 | | |
| pr2_edc_sync1_out | E8 | 10 | | |
| pr2_edc_latch0_in | F9 | 10 | | |
| pr2_edc_latch1_in | F8 | 10 | | |
| pr2_uart0_rxd | C6 | 10 | | |
| pr2_uart0_txd | C8 | 10 | | |
| pr2_uart0_cts_n | D8 | 10 | | |
| pr2_uart0_rts_n | A5 | 10 | | |
| pr2_ecap0_ecap_capin_apwm_o | C7 | 10 | | |
| **PRU-ICSS2 MII** | | | | |
| pr2_mii1_txd3 | AD4 | 11 | | |
| pr2_mii1_txd2 | AC4 | 11 | | |
| pr2_mii1_txd1 | AC7 | 11 | | |
| pr2_mii1_txd0 | AC6 | 11 | | |
| pr2_mii1_rxd3 | AC8 | 11 | | |
| pr2_mii1_rxd2 | AD6 | 11 | | |
| pr2_mii1_rxd1 | AB8 | 11 | | |
| pr2_mii1_rxd0 | AB5 | 11 | | |
| pr2_mii_mr1_clk | AC9 | 11 | | |
| pr2_mii1_rxer | B19 | 11 | | |
| pr2_mii_mt1_clk | AC5 | 11 | | |
| pr2_mii1_rxdv | AC3 | 11 | | |
| pr2_mii1_txen | AB4 | 11 | | |
| pr2_mii0_txd3 | A11 | 11 | | |
| pr2_mii0_txd2 | B13 | 11 | | |
| pr2_mii0_txd1 | A12 | 11 | | |
| pr2_mii0_txd0 | E14 | 11 | | |
| pr2_mii0_rxd3 | F14 | 11 | | |
| pr2_mii0_rxd2 | A19 | 11 | | |
| pr2_mii0_rxd1 | A18 | 11 | | |
| pr2_mii0_rxd0 | C15 | 11 | | |
| pr2_mii_mr0_clk | A13 | 11 | | |
| pr2_mii0_rxer | G12 | 11 | | |
| pr2_mii_mt0_clk | F12 | 11 | | |
| pr2_mii0_rxdv | G14 | 11 | | |
| pr2_mii0_txen | B12 | 11 | | |
| pr2_mdio_mdclk | C14 | 11 | AB3 | 11 |
| pr2_mdio_data | D14 | 11 | AA4 | 11 |

### 7.25.6 PRU-ICSS Manual Functional Mapping

**NOTE**

To configure the desired Manual IO Timing Mode the user must follow the steps described in section "*Manual IO Timing Modes*" of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the *Control Module Chapter* in the Device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS1 PRU0 Direct Output mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-156 *Manual Functions Mapping for PRU-ICSS1 PRU0 Direct Output mode* for a definition of the Manual modes.

Table 7-156 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-156. Manual Functions Mapping for PRU-ICSS1 PRU0 Direct Output mode**

| BALL | BALL NAME | PR1_PRU0_DIR_OUT_MANUAL | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 13 |
| AG3 | vin1a_d10 | 0 | 600 | CFG_VIN1A_D10_OUT | pr1_pru0_gpo7 |
| AG5 | vin1a_d11 | 0 | 0 | CFG_VIN1A_D11_OUT | pr1_pru0_gpo8 |
| AF2 | vin1a_d12 | 0 | 2700 | CFG_VIN1A_D12_OUT | pr1_pru0_gpo9 |
| AF6 | vin1a_d13 | 0 | 200 | CFG_VIN1A_D13_OUT | pr1_pru0_gpo10 |
| AF3 | vin1a_d14 | 0 | 800 | CFG_VIN1A_D14_OUT | pr1_pru0_gpo11 |
| AF4 | vin1a_d15 | 0 | 0 | CFG_VIN1A_D15_OUT | pr1_pru0_gpo12 |
| AF1 | vin1a_d16 | 0 | 100 | CFG_VIN1A_D16_OUT | pr1_pru0_gpo13 |
| AE3 | vin1a_d17 | 0 | 300 | CFG_VIN1A_D17_OUT | pr1_pru0_gpo14 |
| AE5 | vin1a_d18 | 0 | 0 | CFG_VIN1A_D18_OUT | pr1_pru0_gpo15 |
| AE1 | vin1a_d19 | 0 | 400 | CFG_VIN1A_D19_OUT | pr1_pru0_gpo16 |
| AE2 | vin1a_d20 | 0 | 300 | CFG_VIN1A_D20_OUT | pr1_pru0_gpo17 |
| AE6 | vin1a_d21 | 0 | 500 | CFG_VIN1A_D21_OUT | pr1_pru0_gpo18 |
| AD2 | vin1a_d22 | 0 | 0 | CFG_VIN1A_D22_OUT | pr1_pru0_gpo19 |
| AD3 | vin1a_d23 | 0 | 500 | CFG_VIN1A_D23_OUT | pr1_pru0_gpo20 |
| AH6 | vin1a_d3 | 0 | 1600 | CFG_VIN1A_D3_OUT | pr1_pru0_gpo0 |
| AH3 | vin1a_d4 | 0 | 2800 | CFG_VIN1A_D4_OUT | pr1_pru0_gpo1 |
| AH5 | vin1a_d5 | 0 | 0 | CFG_VIN1A_D5_OUT | pr1_pru0_gpo2 |
| AG6 | vin1a_d6 | 0 | 0 | CFG_VIN1A_D6_OUT | pr1_pru0_gpo3 |
| AH4 | vin1a_d7 | 0 | 0 | CFG_VIN1A_D7_OUT | pr1_pru0_gpo4 |
| AG4 | vin1a_d8 | 0 | 0 | CFG_VIN1A_D8_OUT | pr1_pru0_gpo5 |
| AG2 | vin1a_d9 | 0 | 0 | CFG_VIN1A_D9_OUT | pr1_pru0_gpo6 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS1 PRU1 Direct Output mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-157 *Manual Functions Mapping for PRU-ICSS1 PRU1 Direct Output mode* for a definition of the Manual modes.

Table 7-157 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.


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**Table 7-157. Manual Functions Mapping for PRU-ICSS1 PRU1 Direct Output mode**

| BALL | BALL NAME | PR1_PRU1_DIR_OUT_MANUAL | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 13 |
| D3 | vin2a_d10 | 0 | 1900 | CFG_VIN2A_D10_OUT | pr1_pru1_gpo7 |
| F6 | vin2a_d11 | 0 | 2700 | CFG_VIN2A_D11_OUT | pr1_pru1_gpo8 |
| D5 | vin2a_d12 | 0 | 3400 | CFG_VIN2A_D12_OUT | pr1_pru1_gpo9 |
| C2 | vin2a_d13 | 0 | 3200 | CFG_VIN2A_D13_OUT | pr1_pru1_gpo10 |
| C3 | vin2a_d14 | 0 | 3000 | CFG_VIN2A_D14_OUT | pr1_pru1_gpo11 |
| C4 | vin2a_d15 | 0 | 2900 | CFG_VIN2A_D15_OUT | pr1_pru1_gpo12 |
| B2 | vin2a_d16 | 0 | 2700 | CFG_VIN2A_D16_OUT | pr1_pru1_gpo13 |
| D6 | vin2a_d17 | 0 | 3000 | CFG_VIN2A_D17_OUT | pr1_pru1_gpo14 |
| C5 | vin2a_d18 | 0 | 2200 | CFG_VIN2A_D18_OUT | pr1_pru1_gpo15 |
| A3 | vin2a_d19 | 0 | 2300 | CFG_VIN2A_D19_OUT | pr1_pru1_gpo16 |
| B3 | vin2a_d20 | 0 | 1800 | CFG_VIN2A_D20_OUT | pr1_pru1_gpo17 |
| B4 | vin2a_d21 | 0 | 1900 | CFG_VIN2A_D21_OUT | pr1_pru1_gpo18 |
| B5 | vin2a_d22 | 0 | 1400 | CFG_VIN2A_D22_OUT | pr1_pru1_gpo19 |
| A4 | vin2a_d23 | 0 | 1900 | CFG_VIN2A_D23_OUT | pr1_pru1_gpo20 |
| E2 | vin2a_d3 | 0 | 3900 | CFG_VIN2A_D3_OUT | pr1_pru1_gpo0 |
| D2 | vin2a_d4 | 0 | 5100 | CFG_VIN2A_D4_OUT | pr1_pru1_gpo1 |
| F4 | vin2a_d5 | 0 | 0 | CFG_VIN2A_D5_OUT | pr1_pru1_gpo2 |
| C1 | vin2a_d6 | 0 | 2700 | CFG_VIN2A_D6_OUT | pr1_pru1_gpo3 |
| E4 | vin2a_d7 | 0 | 2600 | CFG_VIN2A_D7_OUT | pr1_pru1_gpo4 |
| F5 | vin2a_d8 | 0 | 2500 | CFG_VIN2A_D8_OUT | pr1_pru1_gpo5 |
| E6 | vin2a_d9 | 0 | 1900 | CFG_VIN2A_D9_OUT | pr1_pru1_gpo6 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS1 PRU0 Direct Input mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-158 *Manual Functions Mapping for PRU-ICSS1 PRU0 Direct Input mode* for a definition of the Manual modes.

Table 7-158 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-158. Manual Functions Mapping for PRU-ICSS1 PRU0 Direct Input mode**

| BALL | BALL NAME | PR1_PRU0_DIR_IN_MANUAL | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| AG3 | vin1a_d10 | 0 | 0 | CFG_VIN1A_D10_IN | pr1_pru0_gpi7 |
| AG5 | vin1a_d11 | 0 | 300 | CFG_VIN1A_D11_IN | pr1_pru0_gpi8 |
| AF2 | vin1a_d12 | 0 | 800 | CFG_VIN1A_D12_IN | pr1_pru0_gpi9 |
| AF6 | vin1a_d13 | 0 | 0 | CFG_VIN1A_D13_IN | pr1_pru0_gpi10 |
| AF3 | vin1a_d14 | 0 | 600 | CFG_VIN1A_D14_IN | pr1_pru0_gpi11 |
| AF4 | vin1a_d15 | 0 | 1100 | CFG_VIN1A_D15_IN | pr1_pru0_gpi12 |
| AF1 | vin1a_d16 | 0 | 800 | CFG_VIN1A_D16_IN | pr1_pru0_gpi13 |
| AE3 | vin1a_d17 | 0 | 1000 | CFG_VIN1A_D17_IN | pr1_pru0_gpi14 |
| AE5 | vin1a_d18 | 0 | 1100 | CFG_VIN1A_D18_IN | pr1_pru0_gpi15 |
| AE1 | vin1a_d19 | 0 | 2800 | CFG_VIN1A_D19_IN | pr1_pru0_gpi16 |
| AE2 | vin1a_d20 | 0 | 900 | CFG_VIN1A_D20_IN | pr1_pru0_gpi17 |
| AE6 | vin1a_d21 | 0 | 800 | CFG_VIN1A_D21_IN | pr1_pru0_gpi18 |
| AD2 | vin1a_d22 | 0 | 1400 | CFG_VIN1A_D22_IN | pr1_pru0_gpi19 |
| AD3 | vin1a_d23 | 0 | 1001 | CFG_VIN1A_D23_IN | pr1_pru0_gpi20 |

**Table 7-158. Manual Functions Mapping for PRU-ICSS1 PRU0 Direct Input mode (continued)**

| BALL | BALL NAME | PR1_PRU0_DIR_IN_MANUAL | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| AH6 | vin1a_d3 | 0 | 600 | CFG_VIN1A_D3_IN | pr1_pru0_gpi0 |
| AH3 | vin1a_d4 | 0 | 0 | CFG_VIN1A_D4_IN | pr1_pru0_gpi1 |
| AH5 | vin1a_d5 | 0 | 900 | CFG_VIN1A_D5_IN | pr1_pru0_gpi2 |
| AG6 | vin1a_d6 | 0 | 400 | CFG_VIN1A_D6_IN | pr1_pru0_gpi3 |
| AH4 | vin1a_d7 | 0 | 500 | CFG_VIN1A_D7_IN | pr1_pru0_gpi4 |
| AG4 | vin1a_d8 | 0 | 0 | CFG_VIN1A_D8_IN | pr1_pru0_gpi5 |
| AG2 | vin1a_d9 | 0 | 0 | CFG_VIN1A_D9_IN | pr1_pru0_gpi6 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS1 PRU1 Direct Input mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-159 *Manual Functions Mapping for PRU-ICSS1 PRU1 Direct Input mode* for a definition of the Manual modes.

Table 7-159 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-159. Manual Functions Mapping for PRU-ICSS1 PRU1 Direct Input mode**

| BALL | BALL NAME | PR1_PRU1_DIR_IN_MANUAL | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| D3 | vin2a_d10 | 0 | 1600 | CFG_VIN2A_D10_IN | pr1_pru1_gpi7 |
| F6 | vin2a_d11 | 0 | 1000 | CFG_VIN2A_D11_IN | pr1_pru1_gpi8 |
| D5 | vin2a_d12 | 0 | 1400 | CFG_VIN2A_D12_IN | pr1_pru1_gpi9 |
| C2 | vin2a_d13 | 0 | 800 | CFG_VIN2A_D13_IN | pr1_pru1_gpi10 |
| C3 | vin2a_d14 | 0 | 0 | CFG_VIN2A_D14_IN | pr1_pru1_gpi11 |
| C4 | vin2a_d15 | 0 | 1600 | CFG_VIN2A_D15_IN | pr1_pru1_gpi12 |
| B2 | vin2a_d16 | 0 | 1200 | CFG_VIN2A_D16_IN | pr1_pru1_gpi13 |
| D6 | vin2a_d17 | 0 | 1500 | CFG_VIN2A_D17_IN | pr1_pru1_gpi14 |
| C5 | vin2a_d18 | 0 | 1000 | CFG_VIN2A_D18_IN | pr1_pru1_gpi15 |
| A3 | vin2a_d19 | 0 | 1100 | CFG_VIN2A_D19_IN | pr1_pru1_gpi16 |
| B3 | vin2a_d20 | 0 | 700 | CFG_VIN2A_D20_IN | pr1_pru1_gpi17 |
| B4 | vin2a_d21 | 0 | 1300 | CFG_VIN2A_D21_IN | pr1_pru1_gpi18 |
| B5 | vin2a_d22 | 0 | 1400 | CFG_VIN2A_D22_IN | pr1_pru1_gpi19 |
| A4 | vin2a_d23 | 0 | 1300 | CFG_VIN2A_D23_IN | pr1_pru1_gpi20 |
| E2 | vin2a_d3 | 0 | 2100 | CFG_VIN2A_D3_IN | pr1_pru1_gpi0 |
| D2 | vin2a_d4 | 0 | 1000 | CFG_VIN2A_D4_IN | pr1_pru1_gpi1 |
| F4 | vin2a_d5 | 0 | 1700 | CFG_VIN2A_D5_IN | pr1_pru1_gpi2 |
| C1 | vin2a_d6 | 0 | 700 | CFG_VIN2A_D6_IN | pr1_pru1_gpi3 |
| E4 | vin2a_d7 | 0 | 1300 | CFG_VIN2A_D7_IN | pr1_pru1_gpi4 |
| F5 | vin2a_d8 | 0 | 1700 | CFG_VIN2A_D8_IN | pr1_pru1_gpi5 |
| E6 | vin2a_d9 | 0 | 1600 | CFG_VIN2A_D9_IN | pr1_pru1_gpi6 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS1 PRU0 Parallel Capture mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-160 *Manual Functions Mapping for PRU-ICSS1 PRU0 Parallel Capture mode* for a definition of the Manual modes.

Table 7-160 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.


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**Table 7-160. Manual Functions Mapping for PRU-ICSS1 PRU0 Parallel Capture mode**

| BALL | BALL NAME | PR1_PRU0_PAR_CAP_MANUAL | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| AG3 | vin1a_d10 | 637 | 0 | CFG_VIN1A_D10_IN | pr1_pru0_gpi7 |
| AG5 | vin1a_d11 | 419 | 0 | CFG_VIN1A_D11_IN | pr1_pru0_gpi8 |
| AF2 | vin1a_d12 | 714 | 0 | CFG_VIN1A_D12_IN | pr1_pru0_gpi9 |
| AF6 | vin1a_d13 | 405 | 0 | CFG_VIN1A_D13_IN | pr1_pru0_gpi10 |
| AF3 | vin1a_d14 | 761 | 0 | CFG_VIN1A_D14_IN | pr1_pru0_gpi11 |
| AF4 | vin1a_d15 | 714 | 0 | CFG_VIN1A_D15_IN | pr1_pru0_gpi12 |
| AF1 | vin1a_d16 | 608 | 0 | CFG_VIN1A_D16_IN | pr1_pru0_gpi13 |
| AE3 | vin1a_d17 | 733 | 0 | CFG_VIN1A_D17_IN | pr1_pru0_gpi14 |
| AE5 | vin1a_d18 | 743 | 0 | CFG_VIN1A_D18_IN | pr1_pru0_gpi15 |
| AE1 | vin1a_d19 | 0 | 166 | CFG_VIN1A_D19_IN | pr1_pru0_gpi16 |
| AH6 | vin1a_d3 | 435 | 0 | CFG_VIN1A_D3_IN | pr1_pru0_gpi0 |
| AH3 | vin1a_d4 | 449 | 0 | CFG_VIN1A_D4_IN | pr1_pru0_gpi1 |
| AH5 | vin1a_d5 | 501 | 0 | CFG_VIN1A_D5_IN | pr1_pru0_gpi2 |
| AG6 | vin1a_d6 | 362 | 0 | CFG_VIN1A_D6_IN | pr1_pru0_gpi3 |
| AH4 | vin1a_d7 | 382 | 0 | CFG_VIN1A_D7_IN | pr1_pru0_gpi4 |
| AG4 | vin1a_d8 | 488 | 0 | CFG_VIN1A_D8_IN | pr1_pru0_gpi5 |
| AG2 | vin1a_d9 | 649 | 0 | CFG_VIN1A_D9_IN | pr1_pru0_gpi6 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS1 PRU1 Parallel Capture mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-161 *Manual Functions Mapping for PRU-ICSS1 PRU1 Parallel Capture mode* for a definition of the Manual modes.

Table 7-161 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-161. Manual Functions Mapping for PRU-ICSS1 PRU1 Parallel Capture mode**

| BALL | BALL NAME | PR1_PRU1_PAR_CAP_MANUAL | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| D3 | vin2a_d10 | 2693 | 441 | CFG_VIN2A_D10_IN | pr1_pru1_gpi7 |
| F6 | vin2a_d11 | 2580 | 0 | CFG_VIN2A_D11_IN | pr1_pru1_gpi8 |
| D5 | vin2a_d12 | 2531 | 348 | CFG_VIN2A_D12_IN | pr1_pru1_gpi9 |
| C2 | vin2a_d13 | 2409 | 0 | CFG_VIN2A_D13_IN | pr1_pru1_gpi10 |
| C3 | vin2a_d14 | 1792 | 0 | CFG_VIN2A_D14_IN | pr1_pru1_gpi11 |
| C4 | vin2a_d15 | 2644 | 121 | CFG_VIN2A_D15_IN | pr1_pru1_gpi12 |
| B2 | vin2a_d16 | 2478 | 146 | CFG_VIN2A_D16_IN | pr1_pru1_gpi13 |
| D6 | vin2a_d17 | 2542 | 350 | CFG_VIN2A_D17_IN | pr1_pru1_gpi14 |
| C5 | vin2a_d18 | 2728 | 64 | CFG_VIN2A_D18_IN | pr1_pru1_gpi15 |
| A3 | vin2a_d19 | 0 | 0 | CFG_VIN2A_D19_IN | pr1_pru1_gpi16 |
| E2 | vin2a_d3 | 2908 | 562 | CFG_VIN2A_D3_IN | pr1_pru1_gpi0 |
| D2 | vin2a_d4 | 2684 | 0 | CFG_VIN2A_D4_IN | pr1_pru1_gpi1 |
| F4 | vin2a_d5 | 2904 | 234 | CFG_VIN2A_D5_IN | pr1_pru1_gpi2 |
| C1 | vin2a_d6 | 2488 | 0 | CFG_VIN2A_D6_IN | pr1_pru1_gpi3 |
| E4 | vin2a_d7 | 2600 | 124 | CFG_VIN2A_D7_IN | pr1_pru1_gpi4 |
| F5 | vin2a_d8 | 2590 | 547 | CFG_VIN2A_D8_IN | pr1_pru1_gpi5 |
| E6 | vin2a_d9 | 2690 | 248 | CFG_VIN2A_D9_IN | pr1_pru1_gpi6 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS2 PRU0 IOSET1 Direct Input mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-162 *Manual Functions Mapping for PRU-ICSS2 PRU0 IOSET1 Direct Input mode* for a definition of the Manual modes.

Table 7-162 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-162. Manual Functions Mapping for PRU-ICSS2 PRU0 IOSET1 Direct Input mode**

| BALL | BALL NAME | PR2_PRU0_DIR_IN_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| D7 | vout1_d10 | 0 | 0 | CFG_VOUT1_D10_IN | pr2_pru0_gpi7 |
| D8 | vout1_d11 | 0 | 756 | CFG_VOUT1_D11_IN | pr2_pru0_gpi8 |
| A5 | vout1_d12 | 0 | 531 | CFG_VOUT1_D12_IN | pr2_pru0_gpi9 |
| C6 | vout1_d13 | 0 | 180 | CFG_VOUT1_D13_IN | pr2_pru0_gpi10 |
| C8 | vout1_d14 | 0 | 334 | CFG_VOUT1_D14_IN | pr2_pru0_gpi11 |
| C7 | vout1_d15 | 0 | 1361 | CFG_VOUT1_D15_IN | pr2_pru0_gpi12 |
| B7 | vout1_d16 | 0 | 488 | CFG_VOUT1_D16_IN | pr2_pru0_gpi13 |
| B8 | vout1_d17 | 0 | 321 | CFG_VOUT1_D17_IN | pr2_pru0_gpi14 |
| A7 | vout1_d18 | 0 | 254 | CFG_VOUT1_D18_IN | pr2_pru0_gpi15 |
| A8 | vout1_d19 | 0 | 500 | CFG_VOUT1_D19_IN | pr2_pru0_gpi16 |
| C9 | vout1_d20 | 0 | 716 | CFG_VOUT1_D20_IN | pr2_pru0_gpi17 |
| A9 | vout1_d21 | 0 | 0 | CFG_VOUT1_D21_IN | pr2_pru0_gpi18 |
| B9 | vout1_d22 | 0 | 404 | CFG_VOUT1_D22_IN | pr2_pru0_gpi19 |
| A10 | vout1_d23 | 0 | 290 | CFG_VOUT1_D23_IN | pr2_pru0_gpi20 |
| G11 | vout1_d3 | 0 | 226 | CFG_VOUT1_D3_IN | pr2_pru0_gpi0 |
| E9 | vout1_d4 | 0 | 0 | CFG_VOUT1_D4_IN | pr2_pru0_gpi1 |
| F9 | vout1_d5 | 0 | 365 | CFG_VOUT1_D5_IN | pr2_pru0_gpi2 |
| F8 | vout1_d6 | 0 | 0 | CFG_VOUT1_D6_IN | pr2_pru0_gpi3 |
| E7 | vout1_d7 | 0 | 218 | CFG_VOUT1_D7_IN | pr2_pru0_gpi4 |
| E8 | vout1_d8 | 0 | 186 | CFG_VOUT1_D8_IN | pr2_pru0_gpi5 |
| D9 | vout1_d9 | 0 | 308 | CFG_VOUT1_D9_IN | pr2_pru0_gpi6 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS2 PRU0 IOSET2 Direct Input mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-163 *Manual Functions Mapping for PRU-ICSS2 PRU0 IOSET2 Direct Input mode* for a definition of the Manual modes.

Table 7-163 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-163. Manual Functions Mapping for PRU-ICSS2 PRU0 IOSET2 Direct Input mode**

| BALL | BALL NAME | PR2_PRU0_DIR_IN_MANUAL2 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| AC5 | gpio6_10 | 1000 | 3900 | CFG_GPIO6_10_IN | pr2_pru0_gpi0 |
| AB4 | gpio6_11 | 1000 | 4500 | CFG_GPIO6_11_IN | pr2_pru0_gpi1 |
| F14 | mcasp1_axr15 | 0 | 1800 | CFG_MCASP1_AXR15_IN | pr2_pru0_gpi20 |
| A19 | mcasp2_aclkx | 0 | 700 | CFG_MCASP2_ACLKX_IN | pr2_pru0_gpi18 |
| C15 | mcasp2_axr2 | 0 | 1700 | CFG_MCASP2_AXR2_IN | pr2_pru0_gpi16 |
| A16 | mcasp2_axr3 | 0 | 1800 | CFG_MCASP2_AXR3_IN | pr2_pru0_gpi17 |
| A18 | mcasp2_fsx | 0 | 1100 | CFG_MCASP2_FSX_IN | pr2_pru0_gpi19 |
| B19 | mcasp3_axr0 | 0 | 1100 | CFG_MCASP3_AXR0_IN | pr2_pru0_gpi14 |


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**Table 7-163. Manual Functions Mapping for PRU-ICSS2 PRU0 IOSET2 Direct Input mode (continued)**

| BALL | BALL NAME | PR2_PRU0_DIR_IN_MANUAL2 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| C17 | mcasp3_axr1 | 0 | 1200 | CFG_MCASP3_AXR1_IN | pr2_pru0_gpi15 |
| F15 | mcasp3_fsx | 0 | 1400 | CFG_MCASP3_FSX_IN | pr2_pru0_gpi13 |
| AD4 | mmc3_clk | 1000 | 4500 | CFG_MMC3_CLK_IN | pr2_pru0_gpi2 |
| AC4 | mmc3_cmd | 1000 | 4000 | CFG_MMC3_CMD_IN | pr2_pru0_gpi3 |
| AC7 | mmc3_dat0 | 1000 | 4200 | CFG_MMC3_DAT0_IN | pr2_pru0_gpi4 |
| AC6 | mmc3_dat1 | 1000 | 3800 | CFG_MMC3_DAT1_IN | pr2_pru0_gpi5 |
| AC9 | mmc3_dat2 | 1000 | 3800 | CFG_MMC3_DAT2_IN | pr2_pru0_gpi6 |
| AC3 | mmc3_dat3 | 1000 | 4400 | CFG_MMC3_DAT3_IN | pr2_pru0_gpi7 |
| AC8 | mmc3_dat4 | 1000 | 4100 | CFG_MMC3_DAT4_IN | pr2_pru0_gpi8 |
| AD6 | mmc3_dat5 | 1000 | 4000 | CFG_MMC3_DAT5_IN | pr2_pru0_gpi9 |
| AB8 | mmc3_dat6 | 1000 | 3900 | CFG_MMC3_DAT6_IN | pr2_pru0_gpi10 |
| AB5 | mmc3_dat7 | 1000 | 3500 | CFG_MMC3_DAT7_IN | pr2_pru0_gpi11 |
| B18 | mcasp3_aclkx | 0 | 0 | CFG_MCASP3_ACLKX_IN | pr2_pru0_gpi12 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS2 PRU0 IOSET1 Direct Output mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-164 *Manual Functions Mapping for PRU-ICSS2 PRU0 IOSET1 Direct Output mode* for a definition of the Manual modes.

Table 7-164 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-164. Manual Functions Mapping for PRU-ICSS2 PRU0 IOSET1 Direct Output mode**

| BALL | BALL NAME | PR2_PRU0_DIR_OUT_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 13 |
| D7 | vout1_d10 | 0 | 0 | CFG_VOUT1_D10_OUT | pr2_pru0_gpo7 |
| D8 | vout1_d11 | 0 | 200 | CFG_VOUT1_D11_OUT | pr2_pru0_gpo8 |
| A5 | vout1_d12 | 0 | 2300 | CFG_VOUT1_D12_OUT | pr2_pru0_gpo9 |
| C6 | vout1_d13 | 0 | 450 | CFG_VOUT1_D13_OUT | pr2_pru0_gpo10 |
| C8 | vout1_d14 | 0 | 600 | CFG_VOUT1_D14_OUT | pr2_pru0_gpo11 |
| C7 | vout1_d15 | 0 | 500 | CFG_VOUT1_D15_OUT | pr2_pru0_gpo12 |
| B7 | vout1_d16 | 0 | 100 | CFG_VOUT1_D16_OUT | pr2_pru0_gpo13 |
| B8 | vout1_d17 | 0 | 300 | CFG_VOUT1_D17_OUT | pr2_pru0_gpo14 |
| A7 | vout1_d18 | 0 | 700 | CFG_VOUT1_D18_OUT | pr2_pru0_gpo15 |
| A8 | vout1_d19 | 0 | 700 | CFG_VOUT1_D19_OUT | pr2_pru0_gpo16 |
| C9 | vout1_d20 | 0 | 900 | CFG_VOUT1_D20_OUT | pr2_pru0_gpo17 |
| A9 | vout1_d21 | 0 | 900 | CFG_VOUT1_D21_OUT | pr2_pru0_gpo18 |
| B9 | vout1_d22 | 0 | 300 | CFG_VOUT1_D22_OUT | pr2_pru0_gpo19 |
| A10 | vout1_d23 | 0 | 300 | CFG_VOUT1_D23_OUT | pr2_pru0_gpo20 |
| G11 | vout1_d3 | 0 | 1300 | CFG_VOUT1_D3_OUT | pr2_pru0_gpo0 |
| E9 | vout1_d4 | 0 | 2500 | CFG_VOUT1_D4_OUT | pr2_pru0_gpo1 |
| F9 | vout1_d5 | 0 | 950 | CFG_VOUT1_D5_OUT | pr2_pru0_gpo2 |
| F8 | vout1_d6 | 0 | 800 | CFG_VOUT1_D6_OUT | pr2_pru0_gpo3 |
| E7 | vout1_d7 | 0 | 600 | CFG_VOUT1_D7_OUT | pr2_pru0_gpo4 |
| E8 | vout1_d8 | 0 | 500 | CFG_VOUT1_D8_OUT | pr2_pru0_gpo5 |
| D9 | vout1_d9 | 0 | 500 | CFG_VOUT1_D9_OUT | pr2_pru0_gpo6 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS2 PRU0 IOSET2 Direct Output mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-165 *Manual Functions Mapping for PRU-ICSS2 PRU0 IOSET2 Direct Output mode* for a definition of the Manual modes.

Table 7-165 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-165. Manual Functions Mapping for PRU-ICSS2 PRU0 IOSET2 Direct Output mode**

| BALL | BALL NAME | PR2_PRU0_DIR_OUT_MANUAL2 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 13 |
| AC5 | gpio6_10 | 1000 | 4100 | CFG_GPIO6_10_OUT | pr2_pru0_gpo0 |
| AB4 | gpio6_11 | 1000 | 4700 | CFG_GPIO6_11_OUT | pr2_pru0_gpo1 |
| F14 | mcasp1_axr15 | 0 | 1600 | CFG_MCASP1_AXR15_OUT | pr2_pru0_gpo20 |
| A19 | mcasp2_aclkx | 0 | 2600 | CFG_MCASP2_ACLKX_OUT | pr2_pru0_gpo18 |
| C15 | mcasp2_axr2 | 0 | 1800 | CFG_MCASP2_AXR2_OUT | pr2_pru0_gpo16 |
| A16 | mcasp2_axr3 | 0 | 1200 | CFG_MCASP2_AXR3_OUT | pr2_pru0_gpo17 |
| A18 | mcasp2_fsx | 0 | 0 | CFG_MCASP2_FSX_OUT | pr2_pru0_gpo19 |
| B18 | mcasp3_aclkx | 0 | 2300 | CFG_MCASP3_ACLKX_OUT | pr2_pru0_gpo12 |
| B19 | mcasp3_axr0 | 0 | 300 | CFG_MCASP3_AXR0_OUT | pr2_pru0_gpo14 |
| C17 | mcasp3_axr1 | 0 | 600 | CFG_MCASP3_AXR1_OUT | pr2_pru0_gpo15 |
| F15 | mcasp3_fsx | 0 | 500 | CFG_MCASP3_FSX_OUT | pr2_pru0_gpo13 |
| AD4 | mmc3_clk | 1000 | 4400 | CFG_MMC3_CLK_OUT | pr2_pru0_gpo2 |
| AC4 | mmc3_cmd | 1000 | 4300 | CFG_MMC3_CMD_OUT | pr2_pru0_gpo3 |
| AC7 | mmc3_dat0 | 1000 | 3400 | CFG_MMC3_DAT0_OUT | pr2_pru0_gpo4 |
| AC6 | mmc3_dat1 | 1000 | 3600 | CFG_MMC3_DAT1_OUT | pr2_pru0_gpo5 |
| AC9 | mmc3_dat2 | 1000 | 3400 | CFG_MMC3_DAT2_OUT | pr2_pru0_gpo6 |
| AC3 | mmc3_dat3 | 1000 | 3300 | CFG_MMC3_DAT3_OUT | pr2_pru0_gpo7 |
| AC8 | mmc3_dat4 | 1000 | 4300 | CFG_MMC3_DAT4_OUT | pr2_pru0_gpo8 |
| AD6 | mmc3_dat5 | 1000 | 4800 | CFG_MMC3_DAT5_OUT | pr2_pru0_gpo9 |
| AB8 | mmc3_dat6 | 1000 | 3900 | CFG_MMC3_DAT6_OUT | pr2_pru0_gpo10 |
| AB5 | mmc3_dat7 | 1000 | 4000 | CFG_MMC3_DAT7_OUT | pr2_pru0_gpo11 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS2 PRU1 IOSET1 Direct Input mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-166 *Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET1 Direct Input mode* for a definition of the Manual modes.

Table 7-166 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-166. Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET1 Direct Input mode**

| BALL | BALL NAME | PR2_PRU1_DIR_IN_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| U3 | RMII_MHZ_50_CLK | 0 | 2100 | CFG_RMII_MHZ_50_CLK_IN | pr2_pru1_gpi2 |
| U4 | mdio_d | 0 | 3200 | CFG_MDIO_D_IN | pr2_pru1_gpi1 |
| V1 | mdio_mclk | 0 | 2422 | CFG_MDIO_MCLK_IN | pr2_pru1_gpi0 |
| U5 | rgmii0_rxc | 0 | 1904 | CFG_RGMII0_RXC_IN | pr2_pru1_gpi11 |
| V5 | rgmii0_rxctl | 0 | 3629 | CFG_RGMII0_RXCTL_IN | pr2_pru1_gpi12 |
| W2 | rgmii0_rxd0 | 0 | 2800 | CFG_RGMII0_RXD0_IN | pr2_pru1_gpi16 |
| Y2 | rgmii0_rxd1 | 0 | 3100 | CFG_RGMII0_RXD1_IN | pr2_pru1_gpi15 |


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**Table 7-166. Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET1 Direct Input mode (continued)**

| BALL | BALL NAME | PR2_PRU1_DIR_IN_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| V3 | rgmii0_rxd2 | 0 | 2900 | CFG_RGMII0_RXD2_IN | pr2_pru1_gpi14 |
| V4 | rgmii0_rxd3 | 0 | 3363 | CFG_RGMII0_RXD3_IN | pr2_pru1_gpi13 |
| W9 | rgmii0_txc | 0 | 2488 | CFG_RGMII0_TXC_IN | pr2_pru1_gpi5 |
| V9 | rgmii0_txctl | 0 | 2263 | CFG_RGMII0_TXCTL_IN | pr2_pru1_gpi6 |
| U6 | rgmii0_txd0 | 0 | 2292 | CFG_RGMII0_TXD0_IN | pr2_pru1_gpi10 |
| V6 | rgmii0_txd1 | 0 | 2900 | CFG_RGMII0_TXD1_IN | pr2_pru1_gpi9 |
| U7 | rgmii0_txd2 | 0 | 2800 | CFG_RGMII0_TXD2_IN | pr2_pru1_gpi8 |
| V7 | rgmii0_txd3 | 0 | 2400 | CFG_RGMII0_TXD3_IN | pr2_pru1_gpi7 |
| V2 | uart3_rxd | 0 | 1900 | CFG_UART3_RXD_IN | pr2_pru1_gpi3 |
| Y1 | uart3_txd | 0 | 1900 | CFG_UART3_TXD_IN | pr2_pru1_gpi4 |
| E11 | vout1_vsync | 0 | 0 | CFG_VOUT1_VSYNC_IN | pr2_pru1_gpi17 |
| F11 | vout1_d0 | 0 | 1020 | CFG_VOUT1_D0_IN | pr2_pru1_gpi18 |
| G10 | vout1_d1 | 0 | 976 | CFG_VOUT1_D1_IN | pr2_pru1_gpi19 |
| F10 | vout1_d2 | 0 | 946 | CFG_VOUT1_D2_IN | pr2_pru1_gpi20 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS2 PRU1 IOSET2 Direct Input mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-167 *Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET2 Direct Input mode* for a definition of the Manual modes.

Table 7-167 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-167. Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET2 Direct Input mode**

| BALL | BALL NAME | PR2_PRU1_DIR_IN_MANUAL2 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| C14 | mcasp1_aclkx | 0 | 700 | CFG_MCASP1_ACLKX_IN | pr2_pru1_gpi7 |
| G12 | mcasp1_axr0 | 0 | 2100 | CFG_MCASP1_AXR0_IN | pr2_pru1_gpi8 |
| F12 | mcasp1_axr1 | 0 | 1250 | CFG_MCASP1_AXR1_IN | pr2_pru1_gpi9 |
| B13 | mcasp1_axr10 | 0 | 1800 | CFG_MCASP1_AXR10_IN | pr2_pru1_gpi12 |
| A12 | mcasp1_axr11 | 0 | 1700 | CFG_MCASP1_AXR11_IN | pr2_pru1_gpi13 |
| E14 | mcasp1_axr12 | 0 | 1000 | CFG_MCASP1_AXR12_IN | pr2_pru1_gpi14 |
| A13 | mcasp1_axr13 | 0 | 1300 | CFG_MCASP1_AXR13_IN | pr2_pru1_gpi15 |
| G14 | mcasp1_axr14 | 0 | 1200 | CFG_MCASP1_AXR14_IN | pr2_pru1_gpi16 |
| E11 | vout1_vsync | 0 | 0 | CFG_VOUT1_VSYNC_IN | pr2_pru1_gpi17 |
| F11 | vout1_d0 | 0 | 0 | CFG_VOUT1_D0_IN | pr2_pru1_gpi18 |
| G10 | vout1_d1 | 0 | 0 | CFG_VOUT1_D1_IN | pr2_pru1_gpi19 |
| F10 | vout1_d2 | 0 | 0 | CFG_VOUT1_D2_IN | pr2_pru1_gpi20 |
| B12 | mcasp1_axr8 | 0 | 1450 | CFG_MCASP1_AXR8_IN | pr2_pru1_gpi10 |
| A11 | mcasp1_axr9 | 0 | 1600 | CFG_MCASP1_AXR9_IN | pr2_pru1_gpi11 |
| D17 | mcasp4_axr1 | 0 | 1200 | CFG_MCASP4_AXR1_IN | pr2_pru1_gpi0 |
| AA3 | mcasp5_aclkx | 800 | 4100 | CFG_MCASP5_ACLKX_IN | pr2_pru1_gpi1 |
| AB3 | mcasp5_axr0 | 900 | 4100 | CFG_MCASP5_AXR0_IN | pr2_pru1_gpi3 |
| AA4 | mcasp5_axr1 | 1000 | 4100 | CFG_MCASP5_AXR1_IN | pr2_pru1_gpi4 |
| AB9 | mcasp5_fsx | 800 | 3800 | CFG_MCASP5_FSX_IN | pr2_pru1_gpi2 |
| D18 | xref_clk0 | 0 | 0 | CFG_XREF_CLK0_IN | pr2_pru1_gpi5 |
| E17 | xref_clk1 | 0 | 400 | CFG_XREF_CLK1_IN | pr2_pru1_gpi6 |

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Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS2 PRU1 IOSET1 Direct Output mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-168 *Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET1 Direct Output mode* for a definition of the Manual modes.

Table 7-168 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-168. Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET1 Direct Output mode**

| BALL | BALL NAME | PR2_PRU1_DIR_OUT_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 13 |
| U3 | RMII_MHZ_50_CLK | 0 | 2500 | CFG_RMII_MHZ_50_CLK_OUT | pr2_pru1_gpo2 |
| U4 | mdio_d | 0 | 3900 | CFG_MDIO_D_OUT | pr2_pru1_gpo1 |
| V1 | mdio_mclk | 0 | 3200 | CFG_MDIO_MCLK_OUT | pr2_pru1_gpo0 |
| U5 | rgmii0_rxc | 0 | 2600 | CFG_RGMII0_RXC_OUT | pr2_pru1_gpo11 |
| V5 | rgmii0_rxctl | 0 | 2800 | CFG_RGMII0_RXCTL_OUT | pr2_pru1_gpo12 |
| W2 | rgmii0_rxd0 | 0 | 2800 | CFG_RGMII0_RXD0_OUT | pr2_pru1_gpo16 |
| Y2 | rgmii0_rxd1 | 0 | 2700 | CFG_RGMII0_RXD1_OUT | pr2_pru1_gpo15 |
| V3 | rgmii0_rxd2 | 0 | 2600 | CFG_RGMII0_RXD2_OUT | pr2_pru1_gpo14 |
| V4 | rgmii0_rxd3 | 0 | 2700 | CFG_RGMII0_RXD3_OUT | pr2_pru1_gpo13 |
| W9 | rgmii0_txc | 0 | 3300 | CFG_RGMII0_TXC_OUT | pr2_pru1_gpo5 |
| V9 | rgmii0_txctl | 0 | 2700 | CFG_RGMII0_TXCTL_OUT | pr2_pru1_gpo6 |
| U6 | rgmii0_txd0 | 0 | 2900 | CFG_RGMII0_TXD0_OUT | pr2_pru1_gpo10 |
| V6 | rgmii0_txd1 | 0 | 2500 | CFG_RGMII0_TXD1_OUT | pr2_pru1_gpo9 |
| U7 | rgmii0_txd2 | 0 | 3000 | CFG_RGMII0_TXD2_OUT | pr2_pru1_gpo8 |
| V7 | rgmii0_txd3 | 0 | 3200 | CFG_RGMII0_TXD3_OUT | pr2_pru1_gpo7 |
| V2 | uart3_rxd | 0 | 3400 | CFG_UART3_RXD_OUT | pr2_pru1_gpo3 |
| Y1 | uart3_txd | 0 | 3000 | CFG_UART3_TXD_OUT | pr2_pru1_gpo4 |
| F11 | vout1_d0 | 0 | 600 | CFG_VOUT1_D0_OUT | pr2_pru1_gpo18 |
| G10 | vout1_d1 | 0 | 0 | CFG_VOUT1_D1_OUT | pr2_pru1_gpo19 |
| F10 | vout1_d2 | 0 | 300 | CFG_VOUT1_D2_OUT | pr2_pru1_gpo20 |
| E11 | vout1_vsync | 0 | 1200 | CFG_VOUT1_VSYNC_OUT | pr2_pru1_gpo17 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS2 PRU1 IOSET2 Direct Output mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-169 *Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET2 Direct Output mode* for a definition of the Manual modes.

Table 7-169 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-169. Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET2 Direct Output mode**

| BALL | BALL NAME | PR2_PRU1_DIR_OUT_MANUAL2 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 13 |
| C14 | mcasp1_aclkx | 0 | 1800 | CFG_MCASP1_ACLKX_OUT | pr2_pru1_gpo7 |
| G12 | mcasp1_axr0 | 0 | 800 | CFG_MCASP1_AXR0_OUT | pr2_pru1_gpo8 |
| F12 | mcasp1_axr1 | 0 | 1400 | CFG_MCASP1_AXR1_OUT | pr2_pru1_gpo9 |
| B13 | mcasp1_axr10 | 0 | 2300 | CFG_MCASP1_AXR10_OUT | pr2_pru1_gpo12 |
| A12 | mcasp1_axr11 | 0 | 600 | CFG_MCASP1_AXR11_OUT | pr2_pru1_gpo13 |
| E14 | mcasp1_axr12 | 0 | 700 | CFG_MCASP1_AXR12_OUT | pr2_pru1_gpo14 |
| A13 | mcasp1_axr13 | 0 | 1500 | CFG_MCASP1_AXR13_OUT | pr2_pru1_gpo15 |
| G14 | mcasp1_axr14 | 0 | 2000 | CFG_MCASP1_AXR14_OUT | pr2_pru1_gpo16 |


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**Table 7-169. Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET2 Direct Output mode (continued)**

| BALL | BALL NAME | PR2_PRU1_DIR_OUT_MANUAL2 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 13 |
| E11 | vout1_vsync | 0 | 0 | CFG_VOUT1_VSYNC_OUT | pr2_pru1_gpo17 |
| F11 | vout1_d0 | 0 | 0 | CFG_VOUT1_D0_OUT | pr2_pru1_gpo18 |
| G10 | vout1_d1 | 0 | 0 | CFG_VOUT1_D1_OUT | pr2_pru1_gpo19 |
| F10 | vout1_d2 | 0 | 0 | CFG_VOUT1_D2_OUT | pr2_pru1_gpo20 |
| B12 | mcasp1_axr8 | 0 | 2000 | CFG_MCASP1_AXR8_OUT | pr2_pru1_gpo10 |
| A11 | mcasp1_axr9 | 0 | 800 | CFG_MCASP1_AXR9_OUT | pr2_pru1_gpo11 |
| D17 | mcasp4_axr1 | 0 | 0 | CFG_MCASP4_AXR1_OUT | pr2_pru1_gpo0 |
| AA3 | mcasp5_aclkx | 1000 | 4200 | CFG_MCASP5_ACLKX_OUT | pr2_pru1_gpo1 |
| AB3 | mcasp5_axr0 | 1000 | 3100 | CFG_MCASP5_AXR0_OUT | pr2_pru1_gpo3 |
| AA4 | mcasp5_axr1 | 1000 | 2700 | CFG_MCASP5_AXR1_OUT | pr2_pru1_gpo4 |
| AB9 | mcasp5_fsx | 1000 | 2800 | CFG_MCASP5_FSX_OUT | pr2_pru1_gpo2 |
| D18 | xref_clk0 | 0 | 1600 | CFG_XREF_CLK0_OUT | pr2_pru1_gpo5 |
| E17 | xref_clk1 | 0 | 1500 | CFG_XREF_CLK1_OUT | pr2_pru1_gpo6 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS2 PRU0 IOSET1 Parallel Capture mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-170 *Manual Functions Mapping for PRU-ICSS2 PRU0 IOSET1 Parallel Capture mode* for a definition of the Manual modes.

Table 7-170 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-170. Manual Functions Mapping for PRU-ICSS2 PRU0 IOSET1 Parallel Capture mode**

| BALL | BALL NAME | PR2_PRU0_PAR_CAP_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| D7 | vout1_d10 | 1554 | 0 | CFG_VOUT1_D10_IN | pr2_pru0_gpi7 |
| D8 | vout1_d11 | 1711 | 0 | CFG_VOUT1_D11_IN | pr2_pru0_gpi8 |
| A5 | vout1_d12 | 1562 | 0 | CFG_VOUT1_D12_IN | pr2_pru0_gpi9 |
| C6 | vout1_d13 | 1350 | 0 | CFG_VOUT1_D13_IN | pr2_pru0_gpi10 |
| C8 | vout1_d14 | 1552 | 0 | CFG_VOUT1_D14_IN | pr2_pru0_gpi11 |
| C7 | vout1_d15 | 1882 | 0 | CFG_VOUT1_D15_IN | pr2_pru0_gpi12 |
| B7 | vout1_d16 | 1525 | 0 | CFG_VOUT1_D16_IN | pr2_pru0_gpi13 |
| B8 | vout1_d17 | 1431 | 0 | CFG_VOUT1_D17_IN | pr2_pru0_gpi14 |
| A7 | vout1_d18 | 1240 | 0 | CFG_VOUT1_D18_IN | pr2_pru0_gpi15 |
| A8 | vout1_d19 | 0 | 0 | CFG_VOUT1_D19_IN | pr2_pru0_gpi16 |
| G11 | vout1_d3 | 1231 | 0 | CFG_VOUT1_D3_IN | pr2_pru0_gpi0 |
| E9 | vout1_d4 | 1355 | 0 | CFG_VOUT1_D4_IN | pr2_pru0_gpi1 |
| F9 | vout1_d5 | 1261 | 0 | CFG_VOUT1_D5_IN | pr2_pru0_gpi2 |
| F8 | vout1_d6 | 1016 | 0 | CFG_VOUT1_D6_IN | pr2_pru0_gpi3 |
| E7 | vout1_d7 | 1297 | 0 | CFG_VOUT1_D7_IN | pr2_pru0_gpi4 |
| E8 | vout1_d8 | 1390 | 0 | CFG_VOUT1_D8_IN | pr2_pru0_gpi5 |
| D9 | vout1_d9 | 1685 | 0 | CFG_VOUT1_D9_IN | pr2_pru0_gpi6 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS2 PRU0 IOSET2 Parallel Capture mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-171 *Manual Functions Mapping for PRU-ICSS2 PRU0 IOSET2 Parallel Capture mode* for a definition of the Manual modes.

Table 7-171 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-171. Manual Functions Mapping for PRU-ICSS2 PRU0 IOSET2 Parallel Capture mode**

| BALL | BALL NAME | PR2_PRU0_PAR_CAP_MANUAL2 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| AC5 | gpio6_10 | 3800 | 1785 | CFG_GPIO6_10_IN | pr2_pru0_gpi0 |
| AB4 | gpio6_11 | 3747 | 2246 | CFG_GPIO6_11_IN | pr2_pru0_gpi1 |
| C15 | mcasp2_axr2 | 0 | 0 | CFG_MCASP2_AXR2_IN | pr2_pru0_gpi16 |
| B18 | mcasp3_aclkx | 271 | 0 | CFG_MCASP3_ACLKX_IN | pr2_pru0_gpi12 |
| B19 | mcasp3_axr0 | 1215 | 0 | CFG_MCASP3_AXR0_IN | pr2_pru0_gpi14 |
| C17 | mcasp3_axr1 | 1678 | 0 | CFG_MCASP3_AXR1_IN | pr2_pru0_gpi15 |
| F15 | mcasp3_fsx | 1862 | 0 | CFG_MCASP3_FSX_IN | pr2_pru0_gpi13 |
| AD4 | mmc3_clk | 3888 | 1913 | CFG_MMC3_CLK_IN | pr2_pru0_gpi2 |
| AC4 | mmc3_cmd | 3804 | 1690 | CFG_MMC3_CMD_IN | pr2_pru0_gpi3 |
| AC7 | mmc3_dat0 | 3771 | 1681 | CFG_MMC3_DAT0_IN | pr2_pru0_gpi4 |
| AC6 | mmc3_dat1 | 3689 | 1591 | CFG_MMC3_DAT1_IN | pr2_pru0_gpi5 |
| AC9 | mmc3_dat2 | 3807 | 1441 | CFG_MMC3_DAT2_IN | pr2_pru0_gpi6 |
| AC3 | mmc3_dat3 | 3680 | 2415 | CFG_MMC3_DAT3_IN | pr2_pru0_gpi7 |
| AC8 | mmc3_dat4 | 3846 | 1455 | CFG_MMC3_DAT4_IN | pr2_pru0_gpi8 |
| AD6 | mmc3_dat5 | 3747 | 1673 | CFG_MMC3_DAT5_IN | pr2_pru0_gpi9 |
| AB8 | mmc3_dat6 | 3777 | 1557 | CFG_MMC3_DAT6_IN | pr2_pru0_gpi10 |
| AB5 | mmc3_dat7 | 3775 | 1320 | CFG_MMC3_DAT7_IN | pr2_pru0_gpi11 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS2 PRU1 IOSET1 Parallel Capture mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-172 *Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET1 Parallel Capture mode* for a definition of the Manual modes.

Table 7-171 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-172. Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET1 Parallel Capture mode**

| BALL | BALL NAME | PR2_PRU1_PAR_CAP_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| U3 | RMII_MHZ_50_CLK | 1234 | 0 | CFG_RMII_MHZ_50_CLK_IN | pr2_pru1_gpi2 |
| U4 | mdio_d | 1693 | 0 | CFG_MDIO_D_IN | pr2_pru1_gpi1 |
| V1 | mdio_mclk | 1045 | 0 | CFG_MDIO_MCLK_IN | pr2_pru1_gpi0 |
| U5 | rgmii0_rxc | 1028 | 0 | CFG_RGMII0_RXC_IN | pr2_pru1_gpi11 |
| V5 | rgmii0_rxctl | 1896 | 0 | CFG_RGMII0_RXCTL_IN | pr2_pru1_gpi12 |
| W2 | rgmii0_rxd0 | 0 | 0 | CFG_RGMII0_RXD0_IN | pr2_pru1_gpi16 |
| Y2 | rgmii0_rxd1 | 1659 | 0 | CFG_RGMII0_RXD1_IN | pr2_pru1_gpi15 |
| V3 | rgmii0_rxd2 | 1448 | 0 | CFG_RGMII0_RXD2_IN | pr2_pru1_gpi14 |
| V4 | rgmii0_rxd3 | 1762 | 0 | CFG_RGMII0_RXD3_IN | pr2_pru1_gpi13 |
| W9 | rgmii0_txc | 1384 | 0 | CFG_RGMII0_TXC_IN | pr2_pru1_gpi5 |
| V9 | rgmii0_txctl | 953 | 0 | CFG_RGMII0_TXCTL_IN | pr2_pru1_gpi6 |
| U6 | rgmii0_txd0 | 1170 | 0 | CFG_RGMII0_TXD0_IN | pr2_pru1_gpi10 |


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**Table 7-172. Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET1 Parallel Capture mode (continued)**

| BALL | BALL NAME | PR2_PRU1_PAR_CAP_MANUAL1 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| V6 | rgmii0_txd1 | 1749 | 0 | CFG_RGMII0_TXD1_IN | pr2_pru1_gpi9 |
| U7 | rgmii0_txd2 | 1410 | 0 | CFG_RGMII0_TXD2_IN | pr2_pru1_gpi8 |
| V7 | rgmii0_txd3 | 1479 | 0 | CFG_RGMII0_TXD3_IN | pr2_pru1_gpi7 |
| V2 | uart3_rxd | 1124 | 0 | CFG_UART3_RXD_IN | pr2_pru1_gpi3 |
| Y1 | uart3_txd | 765 | 0 | CFG_UART3_TXD_IN | pr2_pru1_gpi4 |

Manual IO Timings Modes must be used to ensure some IO timings for PRU-ICSS2 PRU1 IOSET2 Parallel Capture mode. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-173 *Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET2 Parallel Capture mode* for a definition of the Manual modes.

Table 7-173 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

**Table 7-173. Manual Functions Mapping for PRU-ICSS2 PRU1 IOSET2 Parallel Capture mode**

| BALL | BALL NAME | PR2_PRU1_PAR_CAP_MANUAL2 | | CFG REGISTER | MUXMODE |
|---|---|---|---|---|---|
| | | A_DELAY (ps) | G_DELAY (ps) | | 12 |
| C14 | mcasp1_aclkx | 1959 | 0 | CFG_MCASP1_ACLKX_IN | pr2_pru1_gpi7 |
| G12 | mcasp1_axr0 | 3142 | 0 | CFG_MCASP1_AXR0_IN | pr2_pru1_gpi8 |
| F12 | mcasp1_axr1 | 2361 | 0 | CFG_MCASP1_AXR1_IN | pr2_pru1_gpi9 |
| B13 | mcasp1_axr10 | 2488 | 0 | CFG_MCASP1_AXR10_IN | pr2_pru1_gpi12 |
| A12 | mcasp1_axr11 | 2652 | 0 | CFG_MCASP1_AXR11_IN | pr2_pru1_gpi13 |
| E14 | mcasp1_axr12 | 2036 | 0 | CFG_MCASP1_AXR12_IN | pr2_pru1_gpi14 |
| A13 | mcasp1_axr13 | 2301 | 0 | CFG_MCASP1_AXR13_IN | pr2_pru1_gpi15 |
| G14 | mcasp1_axr14 | 0 | 0 | CFG_MCASP1_AXR14_IN | pr2_pru1_gpi16 |
| B12 | mcasp1_axr8 | 2581 | 0 | CFG_MCASP1_AXR8_IN | pr2_pru1_gpi10 |
| A11 | mcasp1_axr9 | 2565 | 0 | CFG_MCASP1_AXR9_IN | pr2_pru1_gpi11 |
| D17 | mcasp4_axr1 | 2580 | 0 | CFG_MCASP4_AXR1_IN | pr2_pru1_gpi0 |
| AA3 | mcasp5_aclkx | 3533 | 2482 | CFG_MCASP5_ACLKX_IN | pr2_pru1_gpi1 |
| AB3 | mcasp5_axr0 | 3568 | 2725 | CFG_MCASP5_AXR0_IN | pr2_pru1_gpi3 |
| AA4 | mcasp5_axr1 | 3679 | 2464 | CFG_MCASP5_AXR1_IN | pr2_pru1_gpi4 |
| AB9 | mcasp5_fsx | 3604 | 2091 | CFG_MCASP5_FSX_IN | pr2_pru1_gpi2 |
| D18 | xref_clk0 | 851 | 0 | CFG_XREF_CLK0_IN | pr2_pru1_gpi5 |
| E17 | xref_clk1 | 1966 | 0 | CFG_XREF_CLK1_IN | pr2_pru1_gpi6 |

## 7.26 System and Miscellaneous interfaces

The Device includes the following System and Miscellaneous interfaces:

- Sysboot Interface
- System DMA Interface
- Interrupt Controllers (INTC) Interface
- Observability Signal (OBS) Interface

## 7.27 Test Interfaces

The Device includes the following Test interfaces:

- IEEE 1149.1 Standard-Test-Access Port (JTAG)
- Trace Port Interface Unit (TPIU)
- Advanced Event Triggering Interface (AET)

### 7.27.1 IEEE 1149.1 Standard-Test-Access Port (JTAG)

The JTAG (IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture) interface is used for BSDL testing and emulation of the device. The trstn pin only needs to be released when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality. For maximum reliability, the device includes an internal Pulldown (IPD) on the trstn pin to ensure that trstn is always asserted upon power up and the device's internal emulation logic is always properly initialized. JTAG controllers from Texas Instruments actively drive trstn high. However, some third-party JTAG controllers may not drive trstn high but expect the use of a pullup resistor on trstn. When using this type of JTAG controller, assert trstn to initialize the device after powerup and externally drive trstn high before attempting any emulation or boundary-scan operations.

The main JTAG features include:

- 32KB Embedded Trace Buffer (ETB™)
- 5-pin system trace interface for debug
- Supports Advanced Event Triggering (AET)
- All processors can be emulated via JTAG ports
- All functions on EMU pins of the device:
  - EMU[1:0] - cross-triggering, boot mode (WIR), STM trace
  - EMU[4:2] - STM trace only (single direction)

#### 7.27.1.1 JTAG Electrical Data/Timing

Table 7-174, Table 7-175 and Figure 7-109 assume testing over the recommended operating conditions and electrical characteristic conditions below.

**Table 7-174. Timing Requirements for IEEE 1149.1 JTAG**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(TCK)}$ | Cycle time, TCK | 62.29 | | ns |
| 1a | $t_{w(TCKH)}$ | Pulse duration, TCK high (40% of $t_c$) | 24.92 | | ns |
| 1b | $t_{w(TCKL)}$ | Pulse duration, TCK low (40% of $t_c$) | 24.92 | | ns |
| 3 | $t_{su(TDI-TCK)}$ | Input setup time, TDI valid to TCK high | 6.23 | | ns |
| | $t_{su(TMS-TCK)}$ | Input setup time, TMS valid to TCK high | 6.23 | | ns |
| 4 | $t_{h(TCK-TDI)}$ | Input hold time, TDI valid from TCK high | 31.15 | | ns |
| | $t_{h(TCK-TMS)}$ | Input hold time, TMS valid from TCK high | 31.15 | | ns |

**Table 7-175. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 2 | $t_{d(TCKL-TDOV)}$ | Delay time, TCK low to TDO valid | 0 | 30.5 | ns |

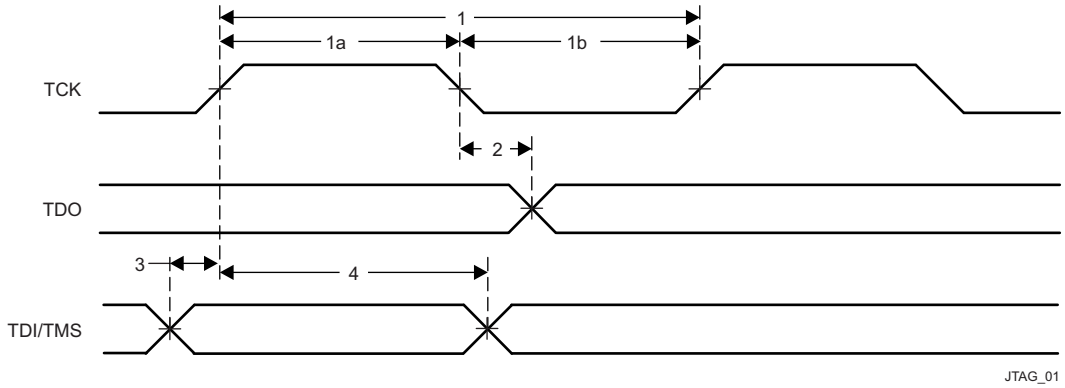


**Figure 7-109. JTAG Timing**


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Table 7-176, Table 7-177 and Figure 7-110 assume testing over the recommended operating conditions and electrical characteristic conditions below.

**Table 7-176. Timing Requirements for IEEE 1149.1 JTAG With RTCK**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(TCK)}$ | Cycle time, TCK | 62.29 | | ns |
| 1a | $t_{w(TCKH)}$ | Pulse duration, TCK high (40% of $t_c$) | 24.92 | | ns |
| 1b | $t_{w(TCKL)}$ | Pulse duration, TCK low (40% of $t_c$) | 24.92 | | ns |
| 3 | $t_{su(TDI-TCK)}$ | Input setup time, TDI valid to TCK high | 6.23 | | ns |
| | $t_{su(TMS-TCK)}$ | Input setup time, TMS valid to TCK high | 6.23 | | ns |
| 4 | $t_{h(TCK-TDI)}$ | Input hold time, TDI valid from TCK high | 31.15 | | ns |
| | $t_{h(TCK-TMS)}$ | Input hold time, TMS valid from TCK high | 31.15 | | ns |

**Table 7-177. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG With RTCK**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 5 | $t_{d(TCK-RTCK)}$ | Delay time, TCK to RTCK with no selected subpaths (ICEPick is the only tap selected - when the Arm is in the scan chain, the delay time is a function of the Arm functional clock). | 0 | 27 | ns |
| 6 | $t_{c(RTCK)}$ | Cycle time, RTCK | 62.29 | | ns |
| 7 | $t_{w(RTCKH)}$ | Pulse duration, RTCK high (40% of $t_c$) | 24.92 | | ns |
| 8 | $t_{w(RTCKL)}$ | Pulse duration, RTCK low (40% of $t_c$) | 24.92 | | ns |

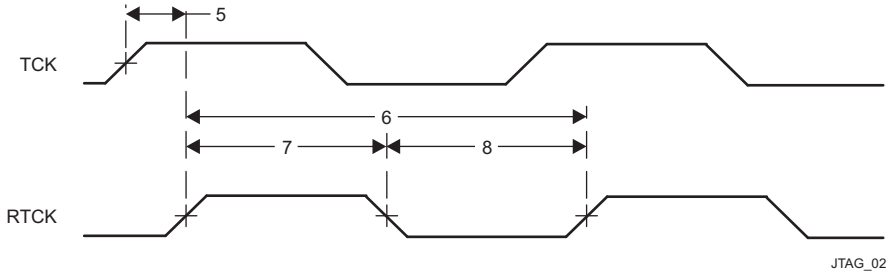


**Figure 7-110. JTAG With RTCK Timing**

## 7.27.2 *Trace Port Interface Unit (TPIU)*

**CAUTION**

The I/O timings provided in this section are valid only if signals within a single IOSET are used. The IOSETs are defined in Table 7-179.

### 7.27.2.1 TPIU PLL DDR Mode

Table 7-178 and Figure 7-111 assume testing over the recommended operating conditions and electrical characteristic conditions below.

**Table 7-178. Switching Characteristics for TPIU**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| TPIU1 | $t_{c(clk)}$ | Cycle time, TRACECLK period | 5.56 | | ns |
| TPIU4 | $t_{d(clk-ctlV)}$ | Skew time, TRACECLK transition to TRACECTL transition | -0.96 | 0.96 | ns |

**Table 7-178. Switching Characteristics for TPIU (continued)**

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| TPIU5 | $t_{d(clk\text{-}dataV)}$ | Skew time, TRACECLK transition to TRACEDATA[17:0] | -0.96 | 0.96 | ns |

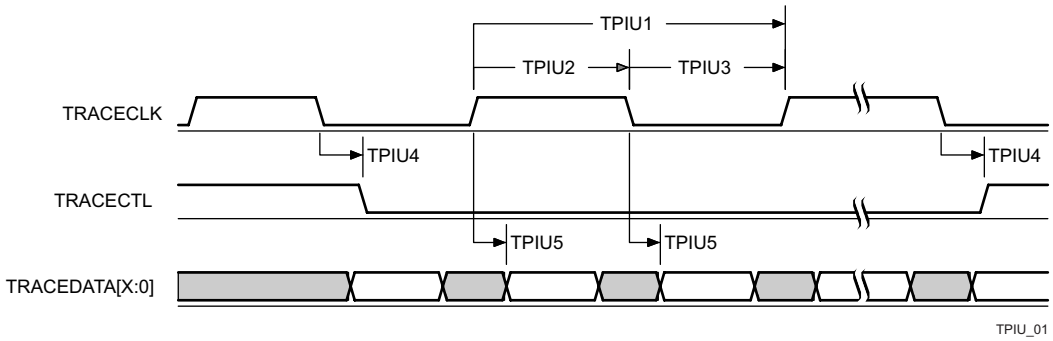


**Figure 7-111. TPIU—PLL DDR Transmit Mode[(1)]**

(1) In d[X:0], X is equal to 15 or 17.

In Table 7-179 are presented the specific groupings of signals (IOSET) for use with TPIU signals.

**Table 7-179. TPIU IOSETs**

| SIGNALS | IOSET1 | | IOSET2 | |
|---|---|---|---|---|
| | BALL | MUX | BALL | MUX |
| emu0 | G21 | 0 | G21 | 0 |
| emu1 | D24 | 0 | D24 | 0 |
| emu2 | F10 | 2 | F10 | 2 |
| emu3 | D7 | 2 | D7 | 2 |
| emu4 | A7 | 2 | A7 | 2 |
| emu5 | E1 | 5 | G11 | 2 |
| emu6 | G2 | 5 | E9 | 2 |
| emu7 | H7 | 5 | F9 | 2 |
| emu8 | G1 | 5 | F8 | 2 |
| emu9 | G6 | 5 | E7 | 2 |
| emu10 | F2 | 5 | D8 | 2 |
| emu11 | F3 | 5 | A5 | 2 |
| emu12 | D1 | 5 | C6 | 2 |
| emu13 | E2 | 5 | C8 | 2 |
| emu14 | D2 | 5 | C7 | 2 |
| emu15 | F4 | 5 | A8 | 2 |
| emu16 | C1 | 5 | C9 | 2 |
| emu17 | E4 | 5 | A9 | 2 |
| emu18 | F5 | 5 | B9 | 2 |
| emu19 | E6 | 5 | A10 | 2 |


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# 8 Applications, Implementation, and Layout

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test design implementation to confirm system functionality.

## 8.1 Power Supply Mapping

TPS659037 is the Power Management IC (PMIC) that should be used for the Device designs. TI requires use of this PMIC for the following reasons:

- TI has validated its use with the Device
- Board level margins including transient response and output accuracy are analyzed and optimized for the entire system
- Support for power sequencing requirements (refer to Section 5.9 *Power Supply Sequences*)
- Support for Adaptive Voltage Scaling (AVS) Class 0 requirements, including TI provided software

Whenever we allow for combining of rails mapped on any of the SMPSes, the PDN guidelines that are the most stringent of the rails combined should be implemented for the particular supply rail.

It is possible that some voltage domains on the device are unused in some systems. In such cases, to ensure device reliability, it is still required that the supply pins for the specific voltage domains are connected to some core power supply output.

These unused supplies though can be combined with any of the core supplies that are used (active) in the system. e.g. if IVA and GPU domains are not used, they can be combined with the CORE domain, thereby having a single power supply driving the combined CORE, IVA and GPU domains.

For the combined rail, the following relaxations do apply:

- The AVS voltage of active rail in the combined rail needs to be used to set the power supply
- The decoupling capacitance should be set according to the active rail in the combined rail

Table 8-1 illustrates the approved and validated power supply connections to the Device for the SMPS outputs of the TPS659037 PMIC.

**Table 8-1. TPS659037 Power Supply Connections[(1)]**

| TPS659037 Power Supply | Valid Combination 1 | Valid Combination 2 |
|---|---|---|
| SMPS1/2[(2)] | vdd_mpu | vdd_mpu |
| SMPS3 | vdds_ddr1, vdds_ddr2 | vdds_ddr1, vdds_ddr2 |
| SMPS4/5 | vdd_dspeve, vdd_gpu, vdd_iva | vdd_dspeve |
| SMPS6 | vdd | vdd_gpu |
| SMPS7 | SW configuration after boot | vdd |
| SMPS8 | vdds18v | vdd_iva |
| SMPS9 | SW configuration after boot 3.3V | vddshvx |
| LDO1 | vddshv8 | vddshv8 |
| LDO2 | vddshv5 | vdds18v |
| LDO3 | vdda_usb1, vdda_usb2, vdda_usb3, vdda_sata | vdda_usb1, vdda_usb2, vdda_usb3, vdda_sata |
| LDO4 | vdda_hdmi, vdda_pcie, vdda_pcie0, vdda_pcie1 | vdda_hdmi, vdda_pcie, vdda_pcie0, vdda_pcie1 |
| LDO9 | vdd_rtc | vdd_rtc |
| LDOLN | 1.8V PLLs | 1.8V PLLs |
| LDOUSB | vdda_usb3v3 | vdda_usb3v3 |

(1) Power consumption is highly application-specific. Separate analysis must be performed to ensure output current ratings (average and peak) is within the limits of the PMIC for all rails of the device.

(2) Refer to the PMIC data manual for the latest TPS659037 specifications

(3) For more information on connectivity with the TPS659037 PMIC, see the TPS659037 User's Guide to Power AM572x (SLIU011).

(4) A product's maximum ambient temperature, thermal system design & heat spreading performance could limit the maximum power dissipation below the full PMIC capacity in order to not exceed recommended SoC max Tj

## 8.2 DDR3 Board Design and Layout Guidelines

### *8.2.1 DDR3 General Board Layout Guidelines*

To help ensure good signaling performance, consider the following board design guidelines:

- Avoid crossing splits in the power plane.
- Minimize Vref noise.
- Use the widest trace that is practical between decoupling capacitors and memory module.
- Maintain a single reference.
- Minimize ISI by keeping impedances matched.
- Minimize crosstalk by isolating sensitive bits, such as strobes, and avoiding return path discontinuities.
- Use proper low-pass filtering on the Vref pins.
- Keep the stub length as short as possible.
- Add additional spacing for on-clock and strobe nets to eliminate crosstalk.
- Maintain a common ground reference for all bypass and decoupling capacitors.
- Take into account the differences in propagation delays between microstrip and stripline nets when evaluating timing constraints.

### *8.2.2 DDR3 Board Design and Layout Guidelines*

#### 8.2.2.1 Board Designs

TI only supports board designs using DDR3 memory that follow the guidelines in this document. The switching characteristics and timing diagram for the DDR3 memory controller are shown in Table 8-2 and Figure 8-1.

**Table 8-2. Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller**

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(DDR_CLK)}$ | Cycle time, DDR_CLK | 1.875 | 2.5[(1)] | ns |

(1) This is the absolute maximum the clock period can be. Actual maximum clock period may be limited by DDR3 speed grade and operating frequency (see the DDR3 memory device data sheet).

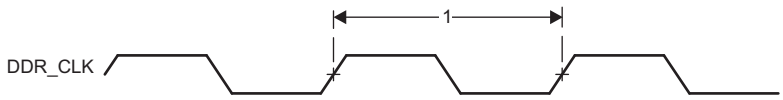


**Figure 8-1. DDR3 Memory Controller Clock Timing**

#### 8.2.2.2 DDR3 EMIFs

The processor contains two separate DDR3 EMIFs. This specification covers one of these EMIFs (ddr1_*) and, thus, needs to be implemented twice, once for each EMIF. The PCB layout generally turns out to be a semi-mirror with ddr2_* being a flipped version of ddr1_*; the only exception being the DDR3 devices themselves are not flipped unless mounted on opposite sides of the PCB. Requirements are identical between the two EMIFs.


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#### 8.2.2.3 DDR3 Device Combinations

Because there are several possible combinations of device counts and single- or dual-side mounting, Table 8-3 summarizes the supported device configurations.

**Table 8-3. Supported DDR3 Device Combinations[(1)]**

| NUMBER OF DDR3 DEVICES | DDR3 DATA DEVICE WIDTH (BITS) | MIRRORED? | DDR3 EMIF WIDTH (BITS) |
|---|---|---|---|
| 1 | 16 | N | 16 |
| 2 | 8 | Y[(2)] | 16 |
| 2 | 16 | N | 32 |
| 2 | 16 | Y[(2)] | 32 |
| 3 | 16 | N[(4)] | 32 |
| 4 | 8 | N | 32 |
| 4 | 8 | Y[(3)] | 32 |
| 5 | 8 | N[(4)] | 32 |

(1) This table is per EMIF.

(2) Two DDR3 devices are mirrored when one device is placed on the top of the board and the second device is placed on the bottom of the board.

(3) This is two mirrored pairs of DDR3 devices.

(4) The DDR memory connected to the DDR ECC bus does NOT need to be the same part number as the DDR memories connected to the DDR data bus. However, some constraints do apply. When selecting a memory for the DDR ECC bus, the following restrictions must be adhered to as compared to the DDR memories on the data bus:

- Match the same DDR3 speed grade
- Have an equal number of internal banks
- Have an equal number of columns
- Have a greater or equal number of rows

#### 8.2.2.4 DDR3 Interface Schematic

##### *8.2.2.4.1 32-Bit DDR3 Interface*

The DDR3 interface schematic varies, depending upon the width of the DDR3 devices used and the width of the bus used (16 or 32 bits). General connectivity is straightforward and very similar. 16-bit DDR devices look like two 8-bit devices. Figure 8-2 and Figure 8-3 show the schematic connections for 32-bit interfaces using x16 devices.

##### *8.2.2.4.2 16-Bit DDR3 Interface*

Note that the 16-bit wide interface schematic is practically identical to the 32-bit interface (see Figure 8-2 and Figure 8-3); only the high-word DDR memories are removed and the unused DQS inputs are tied off.

When not using all or part of a DDR interface, the proper method of handling the unused pins is to tie off the ddrx_dqs*i* pins to ground via a 1k-Ω resistor and to tie off the ddrx_dqsn*i* pins to the corresponding vdds_ddr*x* supply via a 1k-Ω resistor. This needs to be done for each byte not used. Although these signals have internal pullups and pulldowns, external pullups and pulldowns provide additional protection against external electrical noise causing activity on the signals.

The vdds_ddr*x* and ddrx_vref0 power supply pins need to be connected to their respective power supplies even if ddrx is not being used. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32-bits wide, 16-bits wide, or not used.

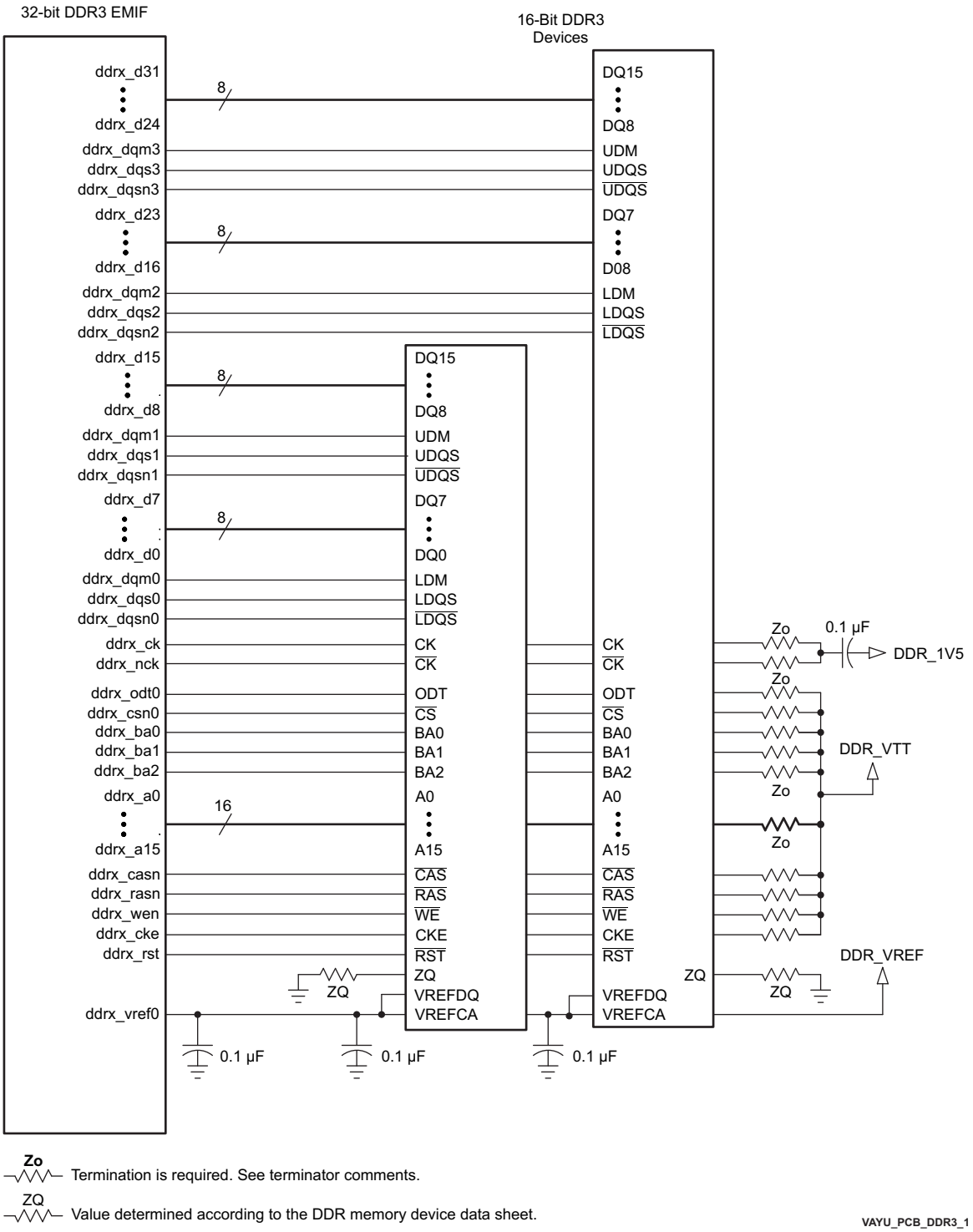


**Figure 8-2. 32-Bit, One-Bank DDR3 Interface Schematic Using Two 16-Bit DDR3 Devices**


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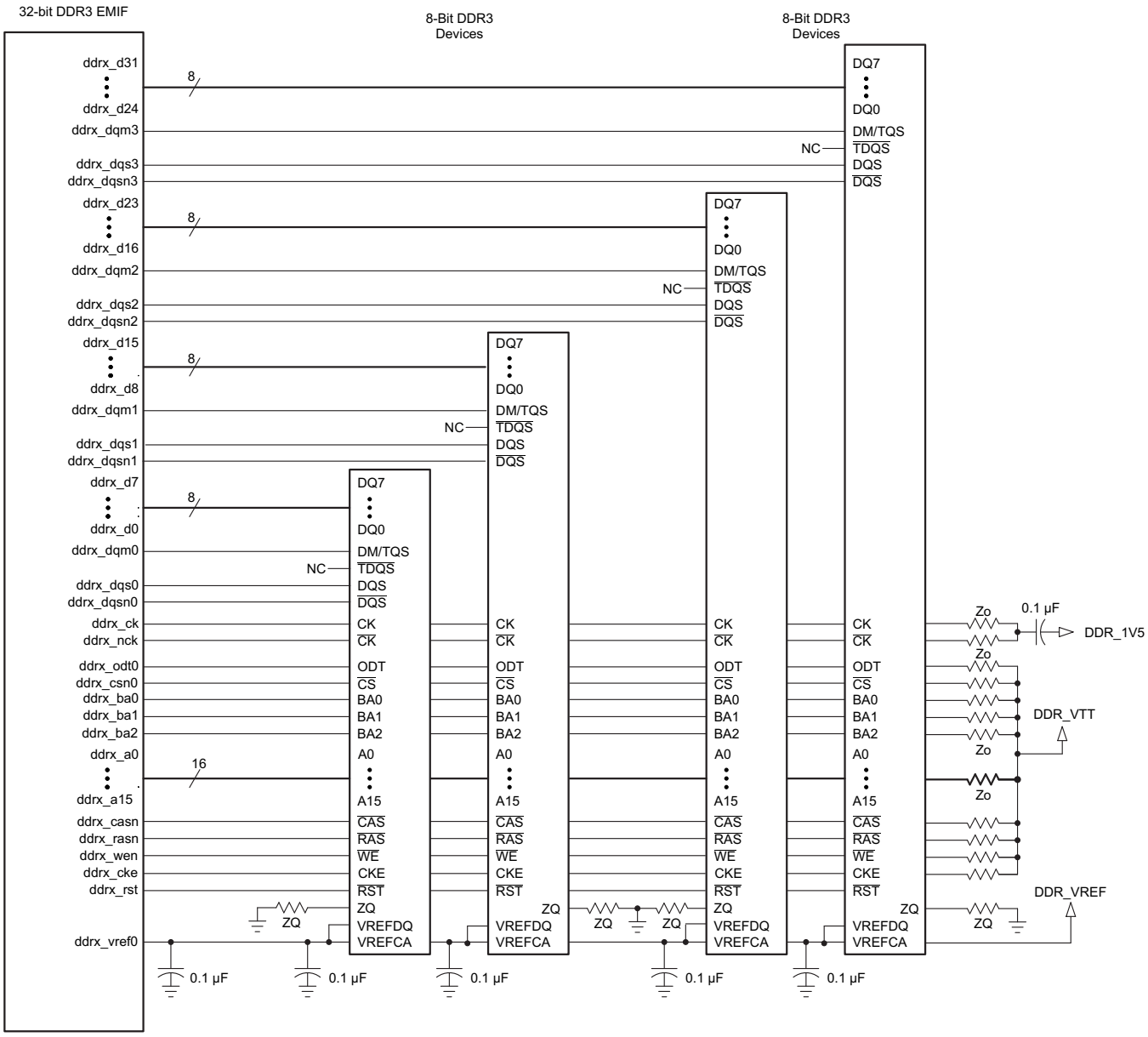


Zo — Termination is required. See terminator comments.

ZQ — Value determined according to the DDR memory device data sheet.

**Figure 8-3. 32-Bit, One-Bank DDR3 Interface Schematic Using Four 8-Bit DDR3 Devices**

#### 8.2.2.5 Compatible JEDEC DDR3 Devices

Table 8-4 shows the parameters of the JEDEC DDR3 devices that are compatible with this interface. Generally, the DDR3 interface is compatible with DDR3-1066 devices in the x8 or x16 widths.

**Table 8-4. Compatible JEDEC DDR3 Devices (Per Interface)**

| NO. | PARAMETER | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | JEDEC DDR3 device speed grade(1) | DDR clock rate = 400MHz | DDR3-800 | DDR3-1600 | |
| | | 400MHz< DDR clock rate ≤ 533MHz | DDR3-1066 | DDR3-1600 | |
| 2 | JEDEC DDR3 device bit width | | x8 | x16 | Bits |
| 3 | JEDEC DDR3 device count(2) | | 2 | 4 | Devices |

(1) Refer to Table 8-2 Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller for the range of supported DDR clock rates.

(2) For valid DDR3 device configurations and device counts, see Section 8.2.2.4, Figure 8-2, and Figure 8-3.

#### 8.2.2.6 PCB Stackup

The minimum stackup for routing the DDR3 interface is a six-layer stack up as shown in Table 8-5. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance SI/EMI performance, or to reduce the size of the PCB footprint. Complete stackup specifications are provided in Table 8-6.

**Table 8-5. Six-Layer PCB Stackup Suggestion**

| LAYER | TYPE | DESCRIPTION |
|---|---|---|
| 1 | Signal | Top routing mostly vertical |
| 2 | Plane | Ground |
| 3 | Plane | Split power plane |
| 4 | Plane | Split power plane or Internal routing |
| 5 | Plane | Ground |
| 6 | Signal | Bottom routing mostly horizontal |


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**Table 8-6. PCB Stackup Specifications**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| PS1 | PCB routing/plane layers | 6 | | | |
| PS2 | Signal routing layers | 3 | | | |
| PS3 | Full ground reference layers under DDR3 routing region(1) | 1 | | | |
| PS4 | Full 1.5-V power reference layers under the DDR3 routing region(1) | 1 | | | |
| PS5 | Number of reference plane cuts allowed within DDR routing region(2) | | | 0 | |
| PS6 | Number of layers between DDR3 routing layer and reference plane(3) | | | 0 | |
| PS7 | PCB routing feature size | | 4 | | Mils |
| PS8 | PCB trace width, w | | 4 | | Mils |
| PS9 | Single-ended impedance, Zo | 50 | | 75 | Ω |
| PS10 | Impedance control(5) | Z-5 | Z | Z+5 | Ω |

(1) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers.

(2) No traces should cross reference plane cuts within the DDR routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.

(3) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.

(4) An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.

(5) Z is the nominal singled-ended impedance selected for the PCB specified by PS9.

#### 8.2.2.7 Placement

Figure 8-4 shows the required placement for the processor as well as the DDR3 devices. The dimensions for this figure are defined in Table 8-7. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR3 devices are omitted from the placement.

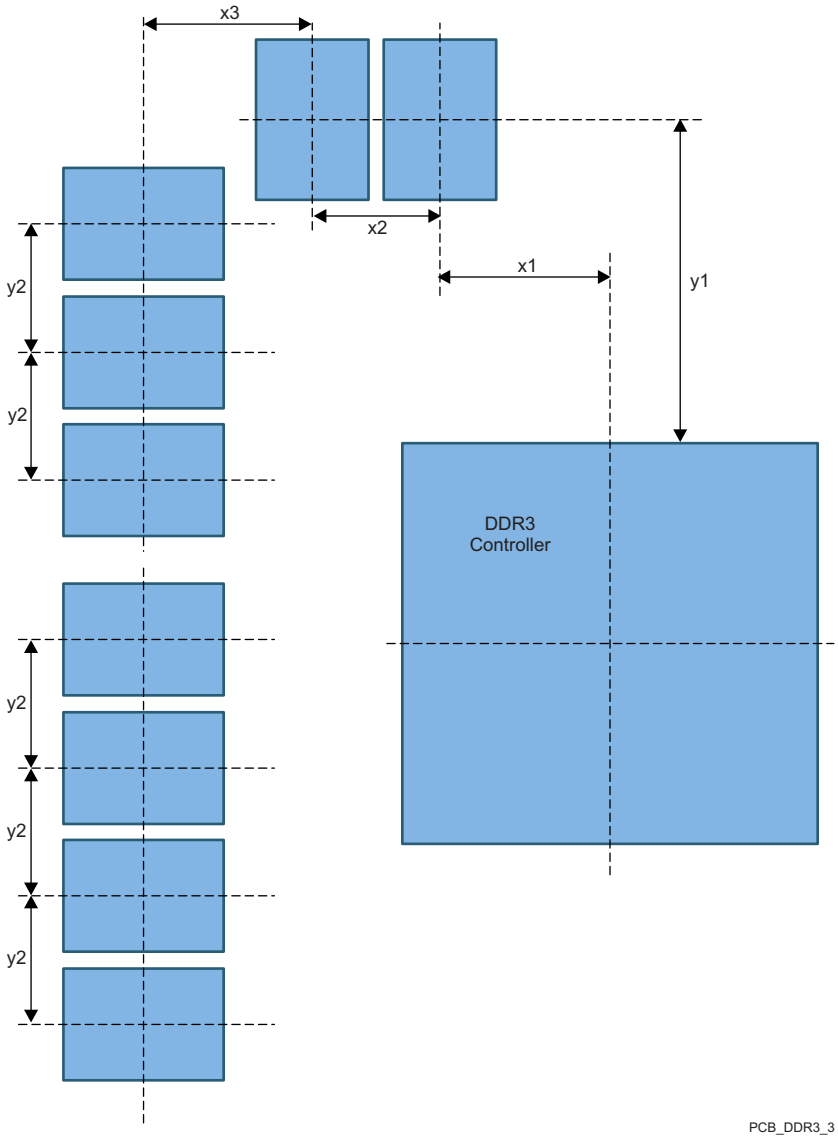


**Figure 8-4. Placement Specifications**

**Table 8-7. Placement Specifications DDR3**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| KOD31 | X1 | | 500 | Mils |
| KOD32 | X2 | | 600 | Mils |
| KOD33 | X3 | | 600 | Mils |
| KOD34 | Y1 | | 1800 | Mils |
| KOD35 | Y2 | | 600 | Mils |
| KOD36 | DDR3 keepout region (1) | | | |
| KOD37 | Clearance from non-DDR3 signal to DDR3 keepout region (2) (3) | 4 | | W |


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(1) DDR3 keepout region to encompass entire DDR3 routing area.

(2) Non-DDR3 signals allowed within DDR3 keepout region provided they are separated from DDR3 routing layers by a ground plane.

(3) If a device has more than one DDR controller, the signals from the other controller(s) are considered non-DDR3 and should be separated by this specification.

#### 8.2.2.8 DDR3 Keepout Region

The region of the PCB used for DDR3 circuitry must be isolated from other signals. The DDR3 keepout region is defined for this purpose and is shown in Figure 8-5. The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in Table 8-7. Non-DDR3 signals should not be routed on the DDR signal layers within the DDR3 keepout region. Non-DDR3 signals may be routed in the region, provided they are routed on layers separated from the DDR signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.5-V DDR3 power plane should cover the entire keepout region. Also note that the two signals from the DDR3 controller should be separated from each other by the specification in Table 8-7, (see KOD37).

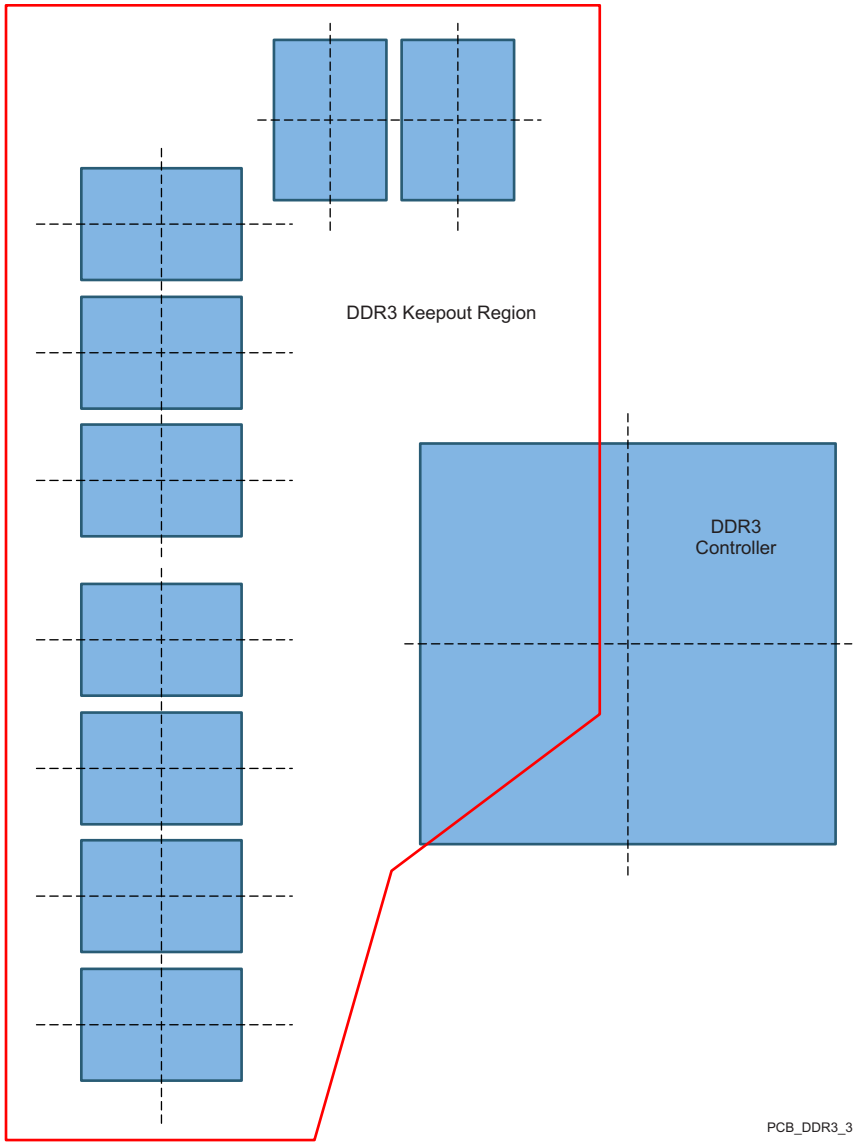


**Figure 8-5. DDR3 Keepout Region**

#### 8.2.2.9 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR3 and other circuitry. Table 8-8 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR3 controllers and DDR3 devices. Additional bulk bypass capacitance may be needed for other circuitry.

**Table 8-8. Bulk Bypass Capacitors**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | vdds_ddrx bulk bypass capacitor count(1) | 1 | | Devices |
| 2 | vdds_ddrx bulk bypass total capacitance | 22 | | µF |

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR3 signal routing.

#### 8.2.2.10 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critcal for proper DDR3 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor/DDR power, and processor/DDR ground connections. Table 8-9 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

1. Fit as many HS bypass capacitors as possible.
2. Minimize the distance from the bypass cap to the pins/balls being bypassed.
3. Use the smallest physical sized capacitors possible with the highest capacitance readily available.
4. Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
5. Minimize via sharing. Note the limites on via sharing shown in Table 8-9.

**Table 8-9. High-Speed Bypass Capacitors**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | HS bypass capacitor package size(1) | | 0201 | 0402 | 10 Mils |
| 2 | Distance, HS bypass capacitor to processor being bypassed(2)(3)(4) | | | 400 | Mils |
| 3 | processor HS bypass capacitor count per vdds_ddrx rail (12) | See Section 8.4 and (11) | | | Devices |
| 4 | processor HS bypass capacitor total capacitance per vdds_ddrx rail (12) | See Section 8.4 and (11) | | | µF |
| 5 | Number of connection vias for each device power/ground ball(5) | | | | Vias |
| 6 | Trace length from device power/ground ball to connection via(2) | | 35 | 70 | Mils |
| 7 | Distance, HS bypass capacitor to DDR device being bypassed(6) | | | 150 | Mils |
| 8 | DDR3 device HS bypass capacitor count(7) | 12 | | | Devices |
| 9 | DDR3 device HS bypass capacitor total capacitance(7) | 0.85 | | | µF |
| 10 | Number of connection vias for each HS capacitor(8)(9) | 2 | | | Vias |
| 11 | Trace length from bypass capacitor connect to connection via(2)(9) | | 35 | 100 | Mils |
| 12 | Number of connection vias for each DDR3 device power/ground ball(10) | 1 | | | Vias |
| 13 | Trace length from DDR3 device power/ground ball to connection via(2)(8) | | 35 | 60 | Mils |

(1) LxW, 10-mil units, that is, a 0402 is a 40x20-mil surface-mount capacitor.

(2) Closer/shorter is better.

(3) Measured from the nearest processor power/ground ball to the center of the capacitor package.

(4) Three of these capacitors should be located underneath the processor, between the cluster of DDR_1V5 balls and ground balls, between the DDR interfaces on the package.

(5) See the Via Channel™ escape for the processor package.

(6) Measured from the DDR3 device power/ground ball to the center of the capacitor package.

(7) Per DDR3 device.

(8) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of


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vias is permitted on the same side of the board.

(9) An HS bypass capacitor may share a via with a DDR device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR device pad should be less than 150 mils.

(10) Up to a total of two pairs of DDR power/ground balls may share a via.

(11) The capacitor recommendations in this data manual reflect only the needs of this processor. Please see the memory vendor's guidelines for determining the appropriate decoupling capacitor arrangement for the memory device itself.

(12) For more information, see , *Core Power Domains*

#### *8.2.2.10.1 Return Current Bypass Capacitors*

Use additional bypass capacitors if the return current reference plane changes due to DDR3 signals hopping from one signal layer to another. The bypass capacitor here provides a path for the return current to hop planes along with the signal. As many of these return current bypass capacitors should be used as possible. Because these are returns for signal current, the signal via size may be used for these capacitors.

### 8.2.2.11 Net Classes

Table 8-10 lists the clock net classes for the DDR3 interface. Table 8-11 lists the signal net classes, and associated clock net classes, for signals in the DDR3 interface. These net classes are used for the termination and routing rules that follow.

**Table 8-10. Clock Net Class Definitions**

| CLOCK NET CLASS | processor PIN NAMES |
|---|---|
| CK | ddrx_ck / ddrx_nck |
| DQS0 | ddrx_dqs0 / ddrx_dqsn0 |
| DQS1 | ddrx_dqs1 / ddrx_dqsn1 |
| DQS2(1) | ddrx_dqs2 / ddrx_dqsn2 |
| DQS3(1) | ddrx_dqs3 / ddrx_dqsn3 |

(1) Only used on 32-bit wide DDR3 memory systems.

**Table 8-11. Signal Net Class Definitions**

| SIGNAL NET CLASS | ASSOCIATED CLOCK NET CLASS | processor PIN NAMES |
|---|---|---|
| ADDR_CTRL | CK | ddrx_ba[2:0], ddrx_a[14:0], ddrx_csn*j*, ddrx_casn, ddrx_rasn, ddrx_wen, ddrx_cke, ddrx_odt*i* |
| DQ0 | DQS0 | ddrx_d[7:0], ddrx_dqm0 |
| DQ1 | DQS1 | ddrx_d[15:8], ddrx_dqm1 |
| DQ2(1) | DQS2 | ddrx_d[23:16], ddrx_dqm2 |
| DQ3(1) | DQS3 | ddrx_d[31:24], ddrx_dqm3 |

(1) Only used on 32-bit wide DDR3 memory systems.

### 8.2.2.12 DDR3 Signal Termination

Signal terminators are required for the CK and ADDR_CTRL net classes. The data lines are terminated by ODT and, thus, the PCB traces should be unterminated. Detailed termination specifications are covered in the routing rules in the following sections.

### 8.2.2.13 VREF_DDR Routing

ddrx_vref0 (VREF) is used as a reference by the input buffers of the DDR3 memories as well as the processor. VREF is intended to be half the DDR3 power supply voltage and is typically generated with the DDR3 VDDS and VTT power supply. It should be routed as a nominal 20-mil wide trace with 0.1 µF bypass capacitors near each device connection. Narrowing of VREF is allowed to accommodate routing congestion.

#### 8.2.2.14 VTT

Like VREF, the nominal value of the VTT supply is half the DDR3 supply voltage. Unlike VREF, VTT is expected to source and sink current, specifically the termination current for the ADDR_CTRL net class Thevinen terminators. VTT is needed at the end of the address bus and it should be routed as a power sub-plane. VTT should be bypassed near the terminator resistors.

#### 8.2.2.15 CK and ADDR_CTRL Topologies and Routing Definition

The CK and ADDR_CTRL net classes are routed in a fly-by topology. They are routed in a similar manner and are length matched to minimize skew between them. CK is a bit more complicated because it runs at a higher transition rate and is differential. The following subsections show the topology and routing for various DDR3 configurations for CK and ADDR_CTRL. The figures in the following subsections define the terms for the routing specification detailed in Table 8-12. Balanced-T routing is not recommended.

##### *8.2.2.15.1 Four DDR3 Devices*

Four DDR3 devices are supported on the DDR EMIF consisting of four x8 DDR3 devices arranged as one bank (CS). These four devices may be mounted on a single side of the PCB, or may be mirrored in two pairs to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

###### *8.2.2.15.1.1 CK and ADDR_CTRL Topologies, Four DDR3 Devices*

Figure 8-6 shows the topology of the CK net classes and Figure 8-7 shows the topology for the corresponding ADDR_CTRL net classes.

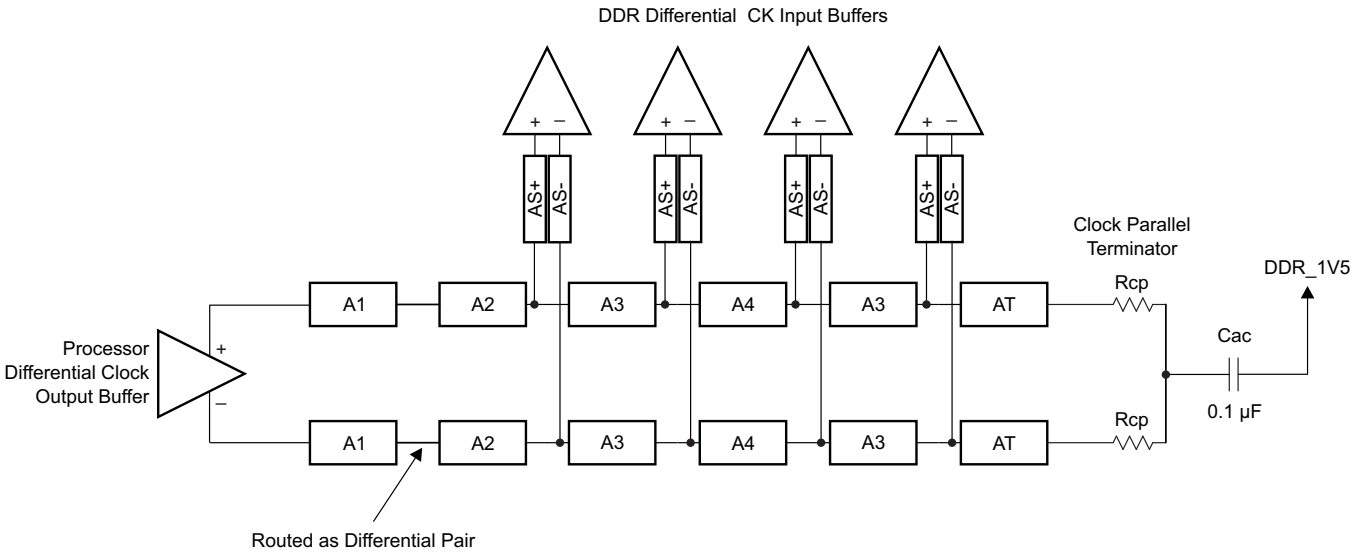


**Figure 8-6. CK Topology for Four x8 DDR3 Devices**


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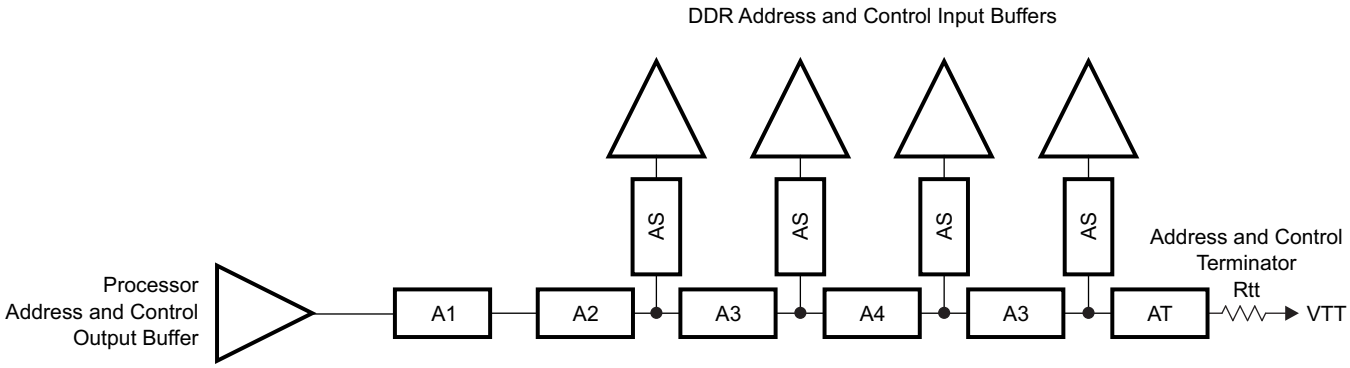


**Figure 8-7. ADDR_CTRL Topology for Four x8 DDR3 Devices**

#### *8.2.2.15.1.2 CK and ADDR_CTRL Routing, Four DDR3 Devices*

Figure 8-8 shows the CK routing for four DDR3 devices placed on the same side of the PCB. Figure 8-9 shows the corresponding ADDR_CTRL routing.

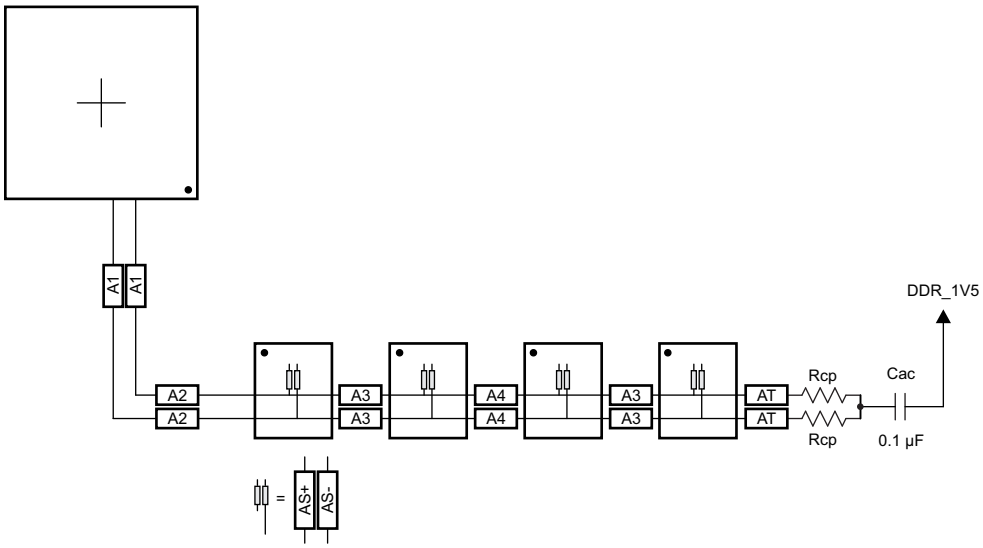


**Figure 8-8. CK Routing for Four Single-Side DDR3 Devices**

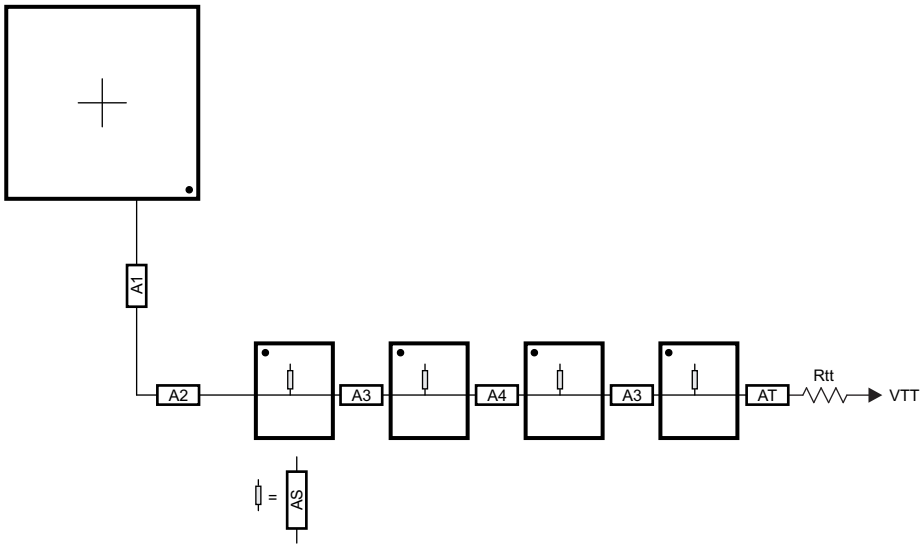


**Figure 8-9. ADDR_CTRL Routing for Four Single-Side DDR3 Devices**

To save PCB space, the four DDR3 memories may be mounted as two mirrored pairs at a cost of increased routing and assembly complexity. Figure 8-10 and Figure 8-11 show the routing for CK and ADDR_CTRL, respectively, for four DDR3 devices mirrored in a two-pair configuration.

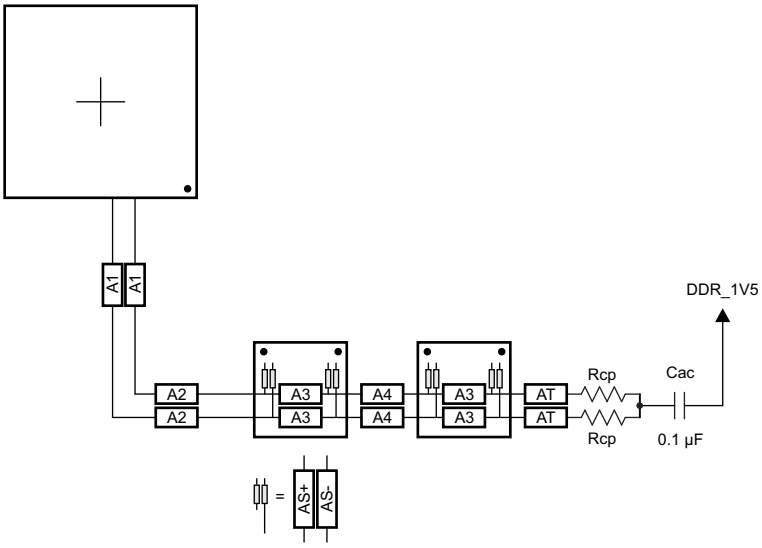


**Figure 8-10. CK Routing for Four Mirrored DDR3 Devices**


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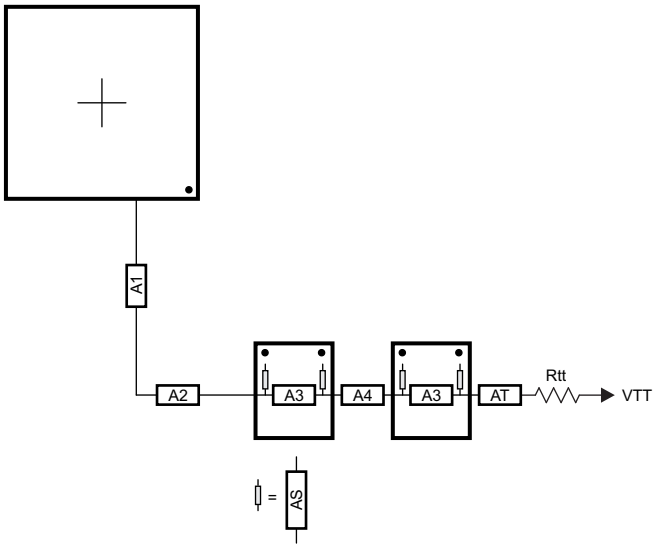


**Figure 8-11. ADDR_CTRL Routing for Four Mirrored DDR3 Devices**

#### *8.2.2.15.2 Two DDR3 Devices*

Two DDR3 devices are supported on the DDR EMIF consisting of two x8 DDR3 devices arranged as one bank (CS), 16 bits wide, or two x16 DDR3 devices arranged as one bank (CS), 32 bits wide. These two devices may be mounted on a single side of the PCB, or may be mirrored in a pair to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

##### *8.2.2.15.2.1 CK and ADDR_CTRL Topologies, Two DDR3 Devices*

Figure 8-12 shows the topology of the CK net classes and Figure 8-13 shows the topology for the corresponding ADDR_CTRL net classes.

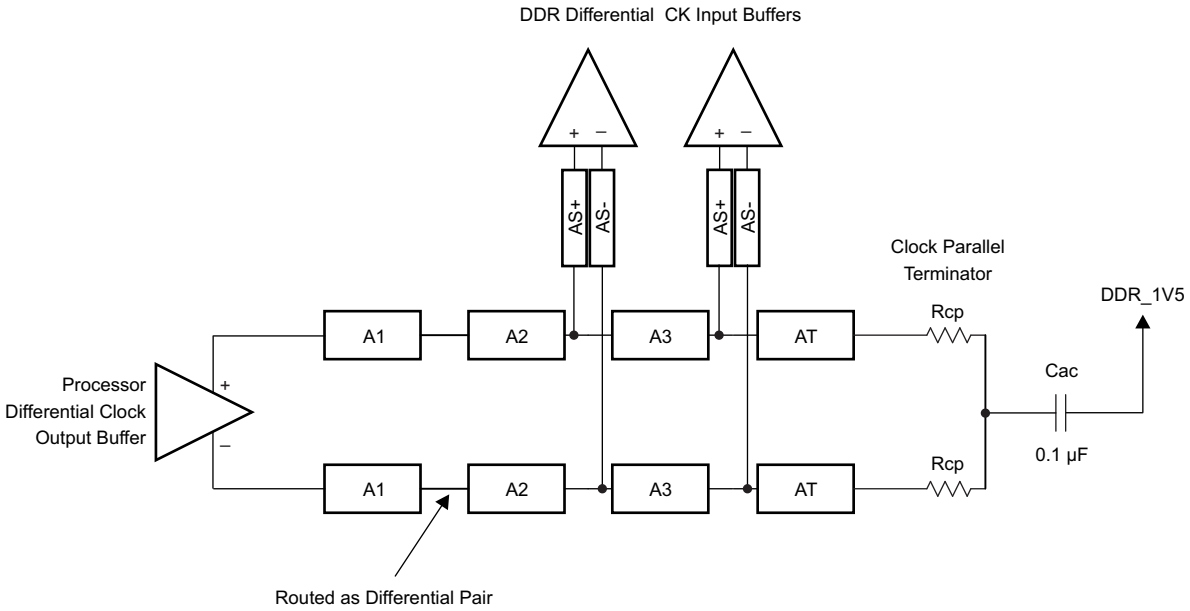


**Figure 8-12. CK Topology for Two DDR3 Devices**

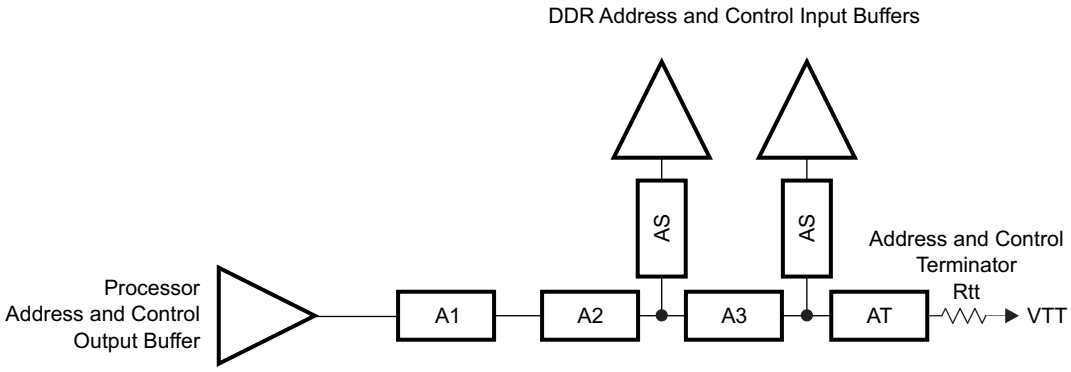


**Figure 8-13. ADDR_CTRL Topology for Two DDR3 Devices**

#### *8.2.2.15.2.2 CK and ADDR_CTRL Routing, Two DDR3 Devices*

Figure 8-14 shows the CK routing for two DDR3 devices placed on the same side of the PCB. Figure 8-15 shows the corresponding ADDR_CTRL routing.

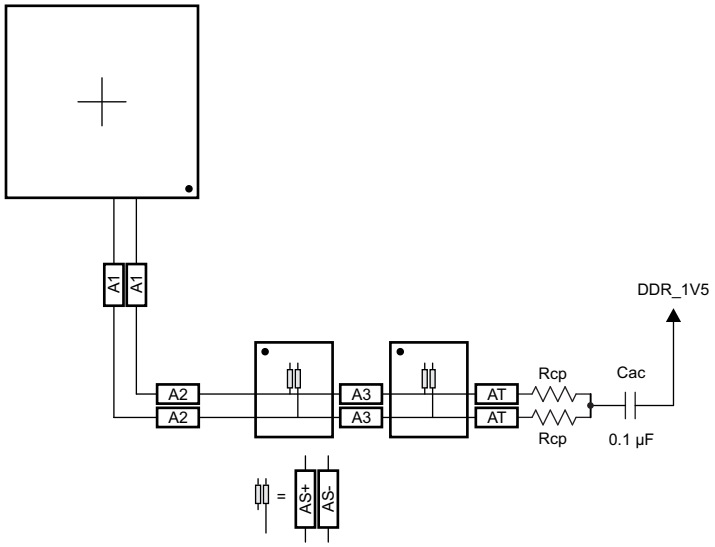


**Figure 8-14. CK Routing for Two Single-Side DDR3 Devices**


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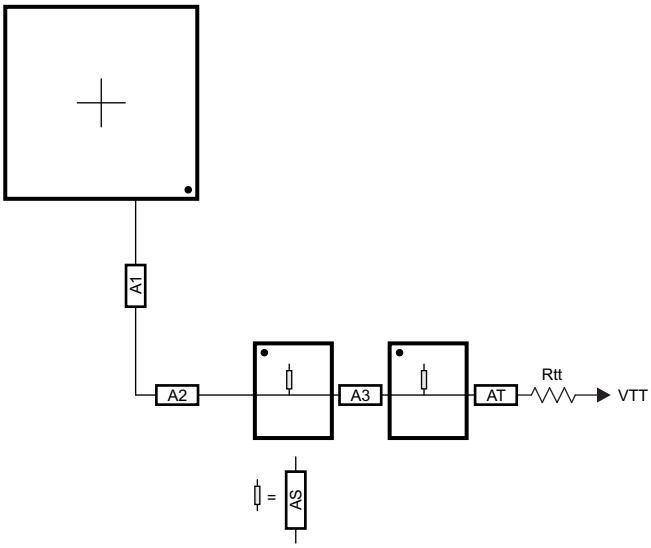


**Figure 8-15. ADDR_CTRL Routing for Two Single-Side DDR3 Devices**

To save PCB space, the two DDR3 memories may be mounted as a mirrored pair at a cost of increased routing and assembly complexity. Figure 8-16 and Figure 8-17 show the routing for CK and ADDR_CTRL, respectively, for two DDR3 devices mirrored in a single-pair configuration.

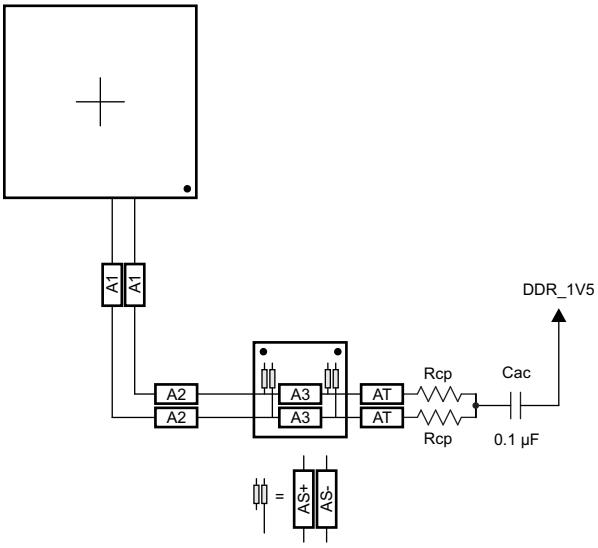


**Figure 8-16. CK Routing for Two Mirrored DDR3 Devices**

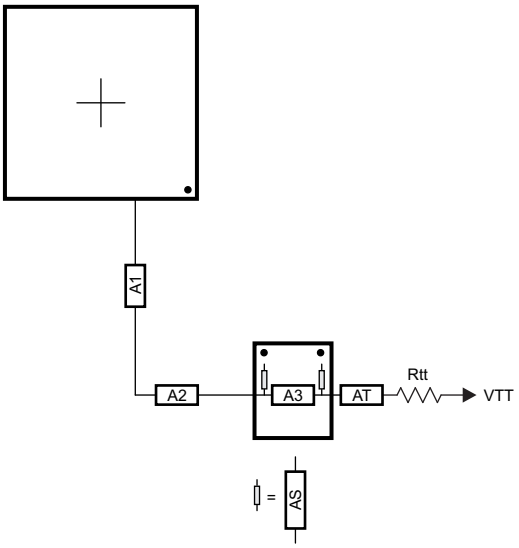


**Figure 8-17. ADDR_CTRL Routing for Two Mirrored DDR3 Devices**

#### *8.2.2.15.3 One DDR3 Device*

A single DDR3 device is supported on the DDR EMIF consisting of one x16 DDR3 device arranged as one bank (CS), 16 bits wide.

##### *8.2.2.15.3.1 CK and ADDR_CTRL Topologies, One DDR3 Device*

Figure 8-18 shows the topology of the CK net classes and Figure 8-19 shows the topology for the corresponding ADDR_CTRL net classes.

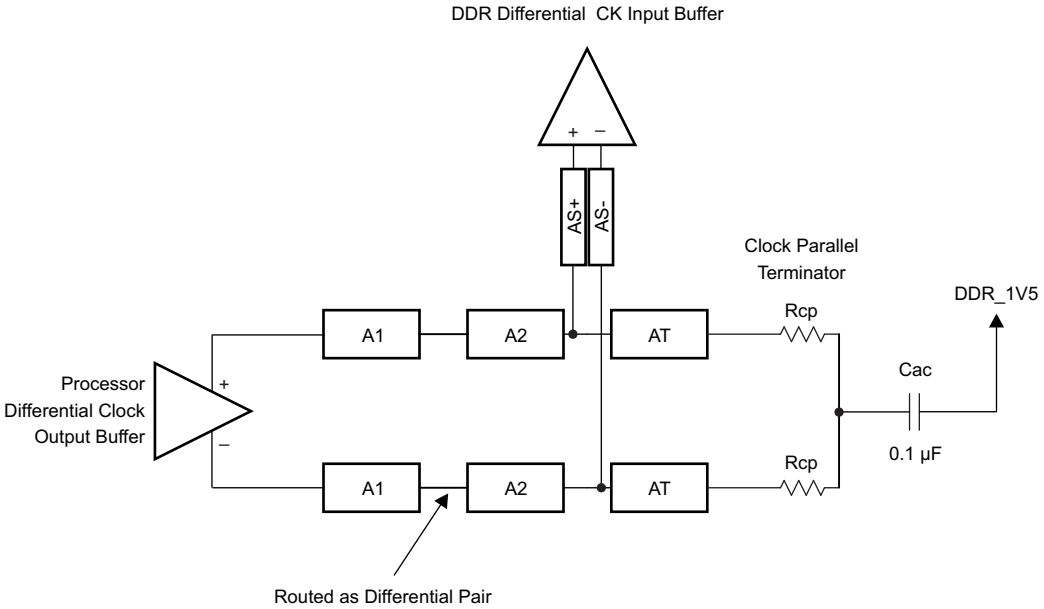


**Figure 8-18. CK Topology for One DDR3 Device**


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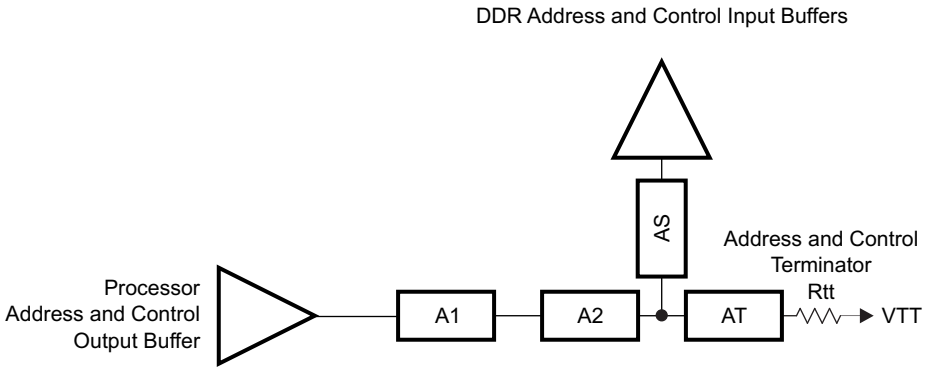


**Figure 8-19. ADDR_CTRL Topology for One DDR3 Device**

#### *8.2.2.15.3.2 CK and ADDR/CTRL Routing, One DDR3 Device*

Figure 8-20 shows the CK routing for one DDR3 device placed on the same side of the PCB. Figure 8-21 shows the corresponding ADDR_CTRL routing.

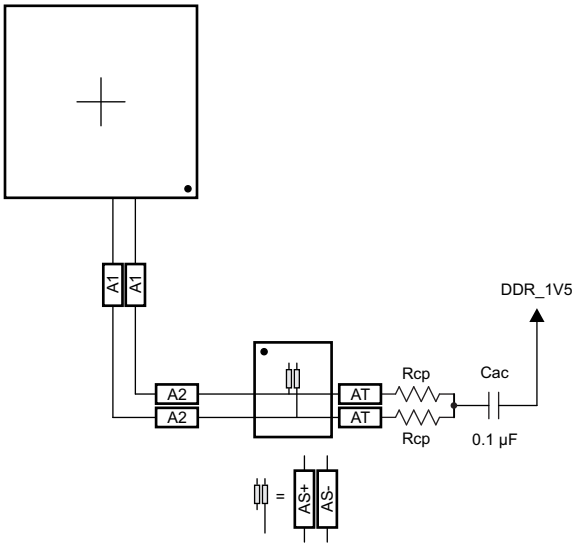


**Figure 8-20. CK Routing for One DDR3 Device**

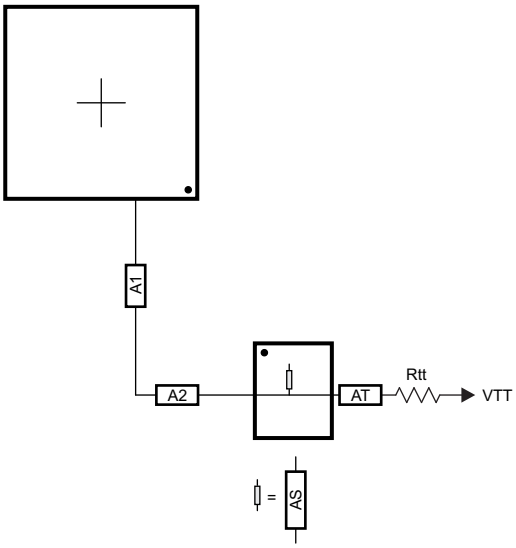


**Figure 8-21. ADDR_CTRL Routing for One DDR3 Device**

#### 8.2.2.16 Data Topologies and Routing Definition

No matter the number of DDR3 devices used, the data line topology is always point to point, so its definition is simple.

Care should be taken to minimize layer transitions during routing. If a layer transition is necessary, it is better to transition to a layer using the same reference plane. If this cannot be accommodated, ensure there are nearby ground vias to allow the return currents to transition between reference planes if both reference planes are ground or vdds_ddr. Ensure there are nearby bypass capacitors to allow the return currents to transition between reference planes if one of the reference planes is ground. The goal is to minimize the size of the return current loops.

##### *8.2.2.16.1 DQS and DQ/DM Topologies, Any Number of Allowed DDR3 Devices*

DQS lines are point-to-point differential, and DQ/DM lines are point-to-point singled ended. Figure 8-22 and Figure 8-23 show these topologies.

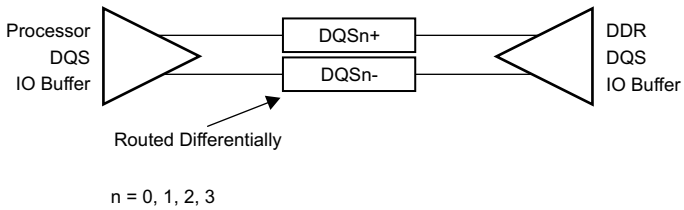


**Figure 8-22. DQS Topology**

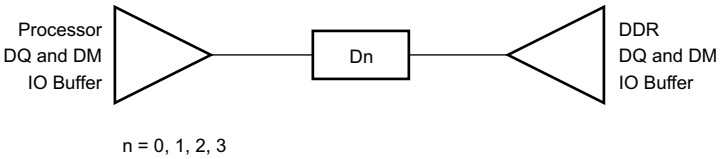


**Figure 8-23. DQ/DM Topology**

##### *8.2.2.16.2 DQS and DQ/DM Routing, Any Number of Allowed DDR3 Devices*

Figure 8-24 and Figure 8-25 show the DQS and DQ/DM routing.


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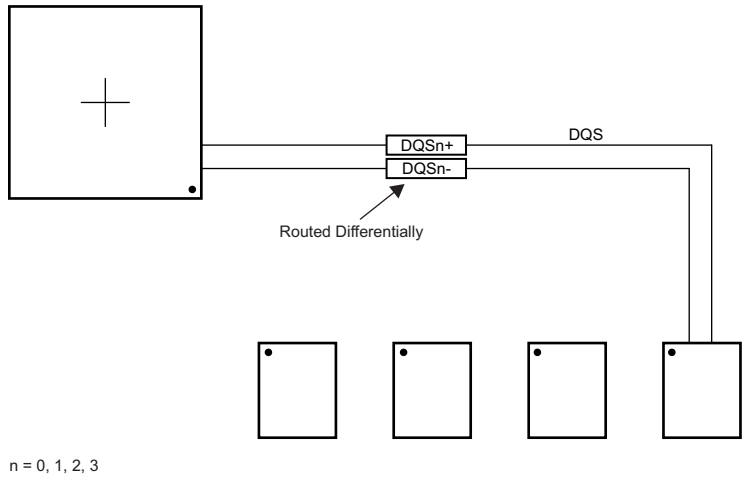



**Figure 8-24. DQS Routing With Any Number of Allowed DDR3 Devices**

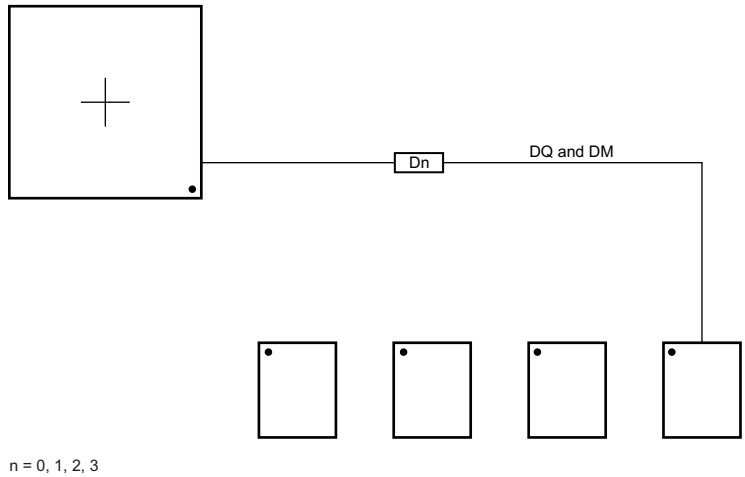


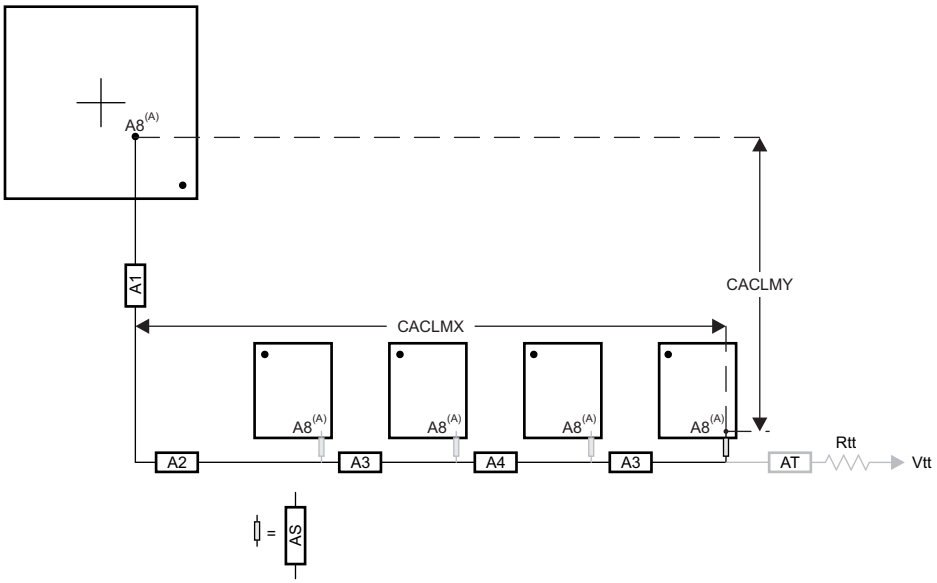

**Figure 8-25. DQ/DM Routing With Any Number of Allowed DDR3 Devices**

### 8.2.2.17 Routing Specification

#### *8.2.2.17.1 CK and ADDR_CTRL Routing Specification*

Skew within the CK and ADDR_CTRL net classes directly reduces setup and hold margin and, thus, this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. A metric to establish this maximum length is Manhattan distance. The Manhattan distance between two points on a PCB is the length between the points when connecting them only with horizontal or vertical segments. A reasonable trace route length is to within a percentage of its Manhattan distance. CACLM is defined as Clock Address Control Longest Manhattan distance.

Given the clock and address pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 8-26 and Figure 8-27 show this distance for four loads and two loads, respectively. It is from this distance that the specifications on the lengths of the transmission lines for the address bus are determined. CACLM is determined similarly for other address bus configurations; that is, it is based on the longest net of the CK/ADDR_CTRL net class. For CK and ADDR_CTRL routing, these specifications are contained in Table 8-12.

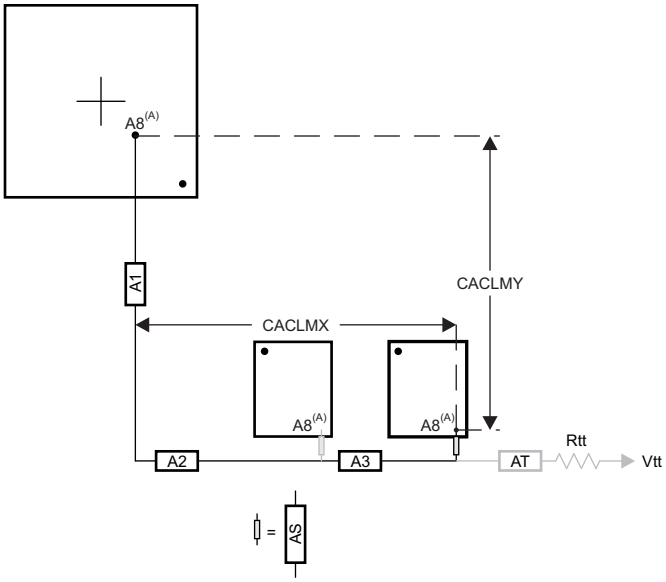



A. It is very likely that the longest CK/ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR_CTRL skew matching and length control.

The length of shorter CK/ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Nonincluded lengths are grayed out in the figure.

Assuming A8 is the longest, CACLM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

**Figure 8-26. CACLM for Four Address Loads on One Side of PCB**




A. It is very likely that the longest CK/ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR_CTRL skew matching and length control.

The length of shorter CK/ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Nonincluded lengths are grayed out in the figure.

Assuming A8 is the longest, CACLM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

**Figure 8-27. CACLM for Two Address Loads on One Side of PCB**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### Table 8-12. CK and ADDR_CTRL Routing Specification[2][3]

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| CARS31 | A1+A2 length | | | 500[1] | ps |
| CARS32 | A1+A2 skew | | | 29 | ps |
| CARS33 | A3 length | | | 125 | ps |
| CARS34 | A3 skew[4] | | | 6 | ps |
| CARS35 | A3 skew[5] | | | 6 | ps |
| CARS36 | A4 length | | | 125 | ps |
| CARS37 | A4 skew | | | 6 | ps |
| CARS38 | AS length | | 5[1] | 17 | ps |
| CARS39 | AS skew | | 1.3[1] | 14 | ps |
| CARS310 | AS+/AS- length | | 5 | 12 | ps |
| CARS311 | AS+/AS- skew | | | 1 | ps |
| CARS312 | AT length[6] | | 75 | | ps |
| CARS313 | AT skew[7] | | 14 | | ps |
| CARS314 | AT skew[8] | | | 1 | ps |
| CARS315 | CK/ADDR_CTRL trace length | | | 1020 | ps |
| CARS316 | Vias per trace | | | 3[1] | vias |
| CARS317 | Via count difference | | | 1[15] | vias |
| CARS318 | Center-to-center CK to other DDR3 trace spacing[9] | 4w | | | |
| CARS319 | Center-to-center ADDR_CTRL to other DDR3 trace spacing[9][10] | 4w | | | |
| CARS320 | Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing[9] | 3w | | | |
| CARS321 | CK center-to-center spacing [11][12] | | | | |
| CARS322 | CK spacing to other net[9] | 4w | | | |
| CARS323 | Rcp[13] | Zo-1 | Zo | Zo+1 | Ω |
| CARS324 | Rtt[13][14] | Zo-5 | Zo | Zo+5 | Ω |

(1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.

(2) The use of vias should be minimized.

(3) Additional bypass capacitors are required when using the DDR_1V5 plane as the reference plane to allow the return current to jump between the DDR_1V5 plane and the ground plane when the net class switches layers at a via.

(4) Non-mirrored configuration (all DDR3 memories on same side of PCB).

(5) Mirrored configuration (one DDR3 device on top of the board and one DDR3 device on the bottom).

(6) While this length can be increased for convenience, its length should be minimized.

(7) ADDR_CTRL net class only (not CK net class). Minimizing this skew is recommended, but not required.

(8) CK net class only.

(9) Center-to-center spacing is allowed to fall to minimum 2w for up to 1250 mils of routed length.

(10) The ADDR_CTRL net class of the other DDR EMIF is considered *other DDR3 trace spacing*.

(11) CK spacing set to ensure proper differential impedance.

(12) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the singleended impedance, Zo.

(13) Source termination (series resistor at driver) is specifically not allowed.

(14) Termination values should be uniform across the net class.

(15) Via count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure all segment skew maximums are not exceeded.

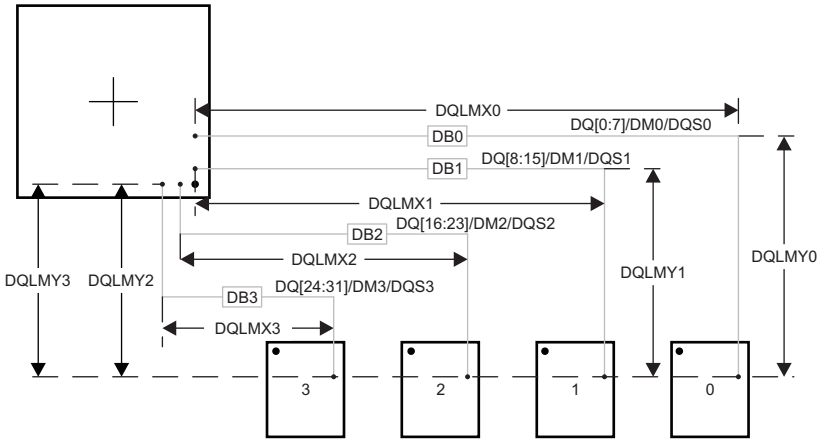
#### 8.2.2.17.2 DQS and DQ Routing Specification

Skew within the DQS and DQ/DM net classes directly reduces setup and hold margin and thus this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. As with CK and ADDR_CTRL, a reasonable trace route length is to within a percentage of its Manhattan distance. DQLMn is defined as DQ Longest Manhattan distance n, where n is the byte number. For a 32-bit interface, there are four DQLMs, DQLM0-DQLM3. Likewise, for a 16-bit interface, there are two DQLMs, DQLM0-DQLM1.

**NOTE**

It is not required, nor is it recommended, to match the lengths across all bytes. Length matching is only required within each byte.

Given the DQS and DQ/DM pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 8-28 shows this distance for four loads. It is from this distance that the specifications on the lengths of the transmission lines for the data bus are determined. For DQS and DQ/DM routing, these specifications are contained in Table 8-13.




DB0 - DB3 represent data bytes 0 - 3.

There are four DQLMs, one for each byte (32-bit interface). Each DQLM is the longest Manhattan distance of the byte; therefore:
DQLM0 = DQLMX0 + DQLMY0
DQLM1 = DQLMX1 + DQLMY1
DQLM2 = DQLMX2 + DQLMY2
DQLM3 = DQLMX3 + DQLMY3

**Figure 8-28. DQLM for Any Number of Allowed DDR3 Devices**

**Table 8-13. Data Routing Specification(2)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| DRS31 | DB0 length | | | 340 | ps |
| DRS32 | DB1 length | | | 340 | ps |
| DRS33 | DB2 length | | | 340 | ps |
| DRS34 | DB3 length | | | 340 | ps |
| DRS35 | DBn skew(3) | | | 5 | ps |
| DRS36 | DQSn+ to DQSn- skew | | | 1 | ps |
| DRS37 | DQSn to DBn skew(3)(4) | | | 5(10) | ps |
| DRS38 | Vias per trace | | | 2(1) | vias |
| DRS39 | Via count difference | | | 0(10) | vias |
| DRS310 | Center-to-center DBn to other DDR3 trace spacing(6) | 4 | | | w(5) |
| DRS311 | Center-to-center DBn to other DBn trace spacing(7) | 3 | | | w(5) |


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**Table 8-13. Data Routing Specification[2] (continued)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| DRS312 | DQSn center-to-center spacing [8] [9] | | | | |
| DRS313 | DQSn center-to-center spacing to other net | 4 | | | w[5] |

(1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.

(2) External termination disallowed. Data termination should use built-in ODT functionality.

(3) Length matching is only done within a byte. Length matching across bytes is neither required nor recommended.

(4) Each DQS pair is length matched to its associated byte.

(5) Center-to-center spacing is allowed to fall to minimum 2w for up to 1250 mils of routed length.

(6) Other DDR3 trace spacing means other DDR3 net classes not within the byte.

(7) This applies to spacing within the net classes of a byte.

(8) DQS pair spacing is set to ensure proper differential impedance.

(9) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the singleended impedance, Zo.

(10) Via count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure DBn skew and DQSn to DBn skew maximums are not exceeded.

## 8.3 High Speed Differential Signal Routing Guidance

The *High-Speed Interface Layout Guidelines Application Report (SPRAAR7)* available from http://www.ti.com/lit/pdf/spraar7 provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application report.

## 8.4 Power Distribution Network Implementation Guidance

The *Sitara Processor Power Distribution Networks: Implementation and Analysis (SPRAC76)* available from http://www.ti.com/lit/pdf/sprac76 provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI supports *only* designs that follow the board design guidelines contained in the application report.

## 8.5 Thermal Solution Guidance

The *Thermal Design Guide for DSP and Arm Application Processors Application Report (SPRABI3)* available from http://www.ti.com/lit/pdf/sprabi3 and the *AM572x Thermal Considerations Application Report (SPRAC53)* available from http://www.ti.com/lit/pdf/sprac53 provide guidance for successful implementation of a thermal solution for system designs that contain an AM57xx application processor. They provide background information on common terms and methods related to thermal solutions. Test data and thermal calculations are also provided for a sample design. TI supports only designs that follow the system design guidelines contained in the application reports. Devices must be operated within their rated temperature ranges at all times to maintain proper function and rated Power On Hours.

## 8.6 Single-Ended Interfaces

### *8.6.1 General Routing Guidelines*

The following paragraphs detail the routing guidelines that must be observed when routing the various functional LVCMOS interfaces.

- Line spacing:
  - For a line width equal to W, the spacing between two lines must be 2W, at least. This minimizes the crosstalk between switching signals between the different lines. On the PCB, this is not achievable everywhere (for example, when breaking signals out from the device package), but it is recommended to follow this rule as much as possible. When violating this guideline, minimize the length of the traces running parallel to each other (see Figure 8-29).

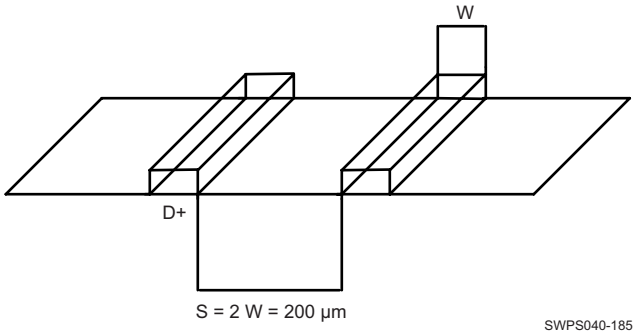


**Figure 8-29. Ground Guard Illustration**

- Length matching (unless otherwise specified):
  - For bus or traces at frequencies less than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 25 mm.
  - For bus or traces at frequencies greater than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 2.5 mm.
- Characteristic impedance
  - Unless otherwise specified, the characteristic impedance for single-ended interfaces is recommended to be between 35-Ω and 65-Ω.
- Multiple peripheral support
  - For interfaces where multiple peripherals have to be supported in the star topology, the length of each branch has to be balanced. Before closing the PCB design, it is highly recommended to verify signal integrity based on simulations including actual PCB extraction.

### *8.6.2 QSPI Board Design and Layout Guidelines*

The following section details the routing guidelines that must be observed when routing the QSPI interfaces.

- The qspi1_sclk output signal must be looped back into the qspi1_rtclk input.
- The signal propagation delay from the qspi1_sclk ball to the QSPI device CLK input pin (A to C) must be approximately equal to the signal propagation delay from the QSPI device CLK pin to the qspi1_rtclk ball (C to D).
- The signal propagation delay from the QSPI device CLK pin to the qspi1_rtclk ball (C to D) must be approximately equal to the signal propagation delay of the control and data signals between the QSPI device and the SoC device (E to F, or F to E).
- The signal propagation delay from the qspi1_sclk signal to the series terminators (R2 = 10 Ω) near the QSPI device must be < 450pS (~7cm as stripline or ~8cm as microstrip)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 8-30.
- Propagation delays and matching:
  - A to C = C to D = E to F.
  - Matching skew: < 60pS
  - A to B < 450pS
  - B to C = as small as possible (<60pS)


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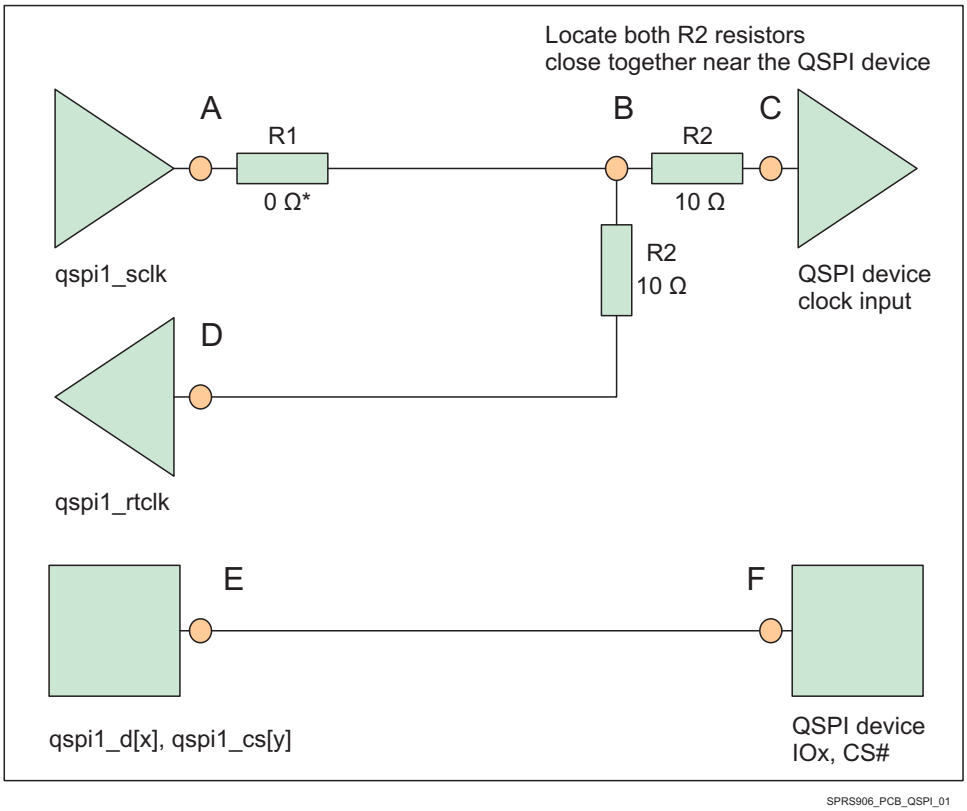


**Figure 8-30. QSPI Interface High Level Schematic**

(1) 0 Ω resistor (R1), located as close as possible to the qspi1_sclk pin, is placeholder for fine-tuning if needed.

## 8.7 LJCB_REFN/P Connections

A Common Refclk Rx Architecture is required to be used for the device PCIe interface. Specifically, two modes of Common Refclk Rx Architecture are supported:

- **External REFCLK Mode**: An common external 100MHz clock source is distributed to both the Device and the link partner
- **Output REFCLK Mode**: A 100MHz HCSL clock source is output by the device and used by the link partner

In **External REFCLK Mode**, a high-quality, low-jitter, differential HCSL 100MHz clock source compliant to the PCIe REFCLK AC Specifications should be provided on the Device's ljcb_clkn / ljcb_clkp inputs.

Alternatively, an LVDS clock source can be used with the following additional requirements:

- External AC coupling capacitors described in Table 8-14 should be populated at the ljcb_clkn / ljcb_clkp inputs.
- All termination requirements (ex. parallel 100ohm termination) from the clock source manufacturer should be followed.

In **Output REFCLK Mode**, the 100MHz clock from the Device's DPLL_PCIE_REF should be output on the Device's ljcb_clkn / ljcb_clkp pins and used as the HCSL REFCLK by the link partner. External near-side termination to ground described in Table 8-15 is required on both of the ljcb_clkn / ljcb_clkp outputs in this mode.

**Table 8-14. LJCB_REFN/P Requirements in External LVDS REFCLK Mode**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| ljcb_clkn / ljcb_clkp AC coupling capacitor value | | 100 | | nF |

**Table 8-14. LJCB_REFN/P Requirements in External LVDS REFCLK Mode (continued)**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| ljcb_clkn / ljcb_clkp AC coupling capacitor package size | | 0402 | 0603 | EIA[(1)(2)] |

(1) EIA LxW units, that is, a 0402 is a 40x20 mils surface mount capacitor.

(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

**Table 8-15. LJCB_REFN/P Requirements in Output REFCLK Mode**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| ljcb_clkn / ljcb_clkp near-side termination to ground value | 47.5 | 50 | 52.5 | Ohms |

## 8.8 Clock Routing Guidelines

### *8.8.1 32-kHz Oscillator Routing*

When designing the printed-circuit board:

- Keep the crystal as close as possible to the crystal pins X1 and X2.
- Keep the trace lengths short and small to reduce capacitor loading and prevent unwanted noise pickup.
- Place a guard ring around the crystal and tie the ring to ground to help isolate the crystal from unwanted noise pickup.
- Keep all signals out from beneath the crystal and the X1 and X2 pins to prevent noise coupling.
- Finally, an additional local ground plane on an adjacent PCB layer can be added under the crystal to shield it from unwanted pickup from traces on other layers of the board. This plane must be isolated from the regular PCB ground plane and tied to the GND pin of the RTC. The plane must not be any larger than the perimeter of the guard ring. Make sure that this ground plane does not contribute to significant capacitance (a few pF) between the signal line and ground on the connections that run from X1 and X2 to the crystal.

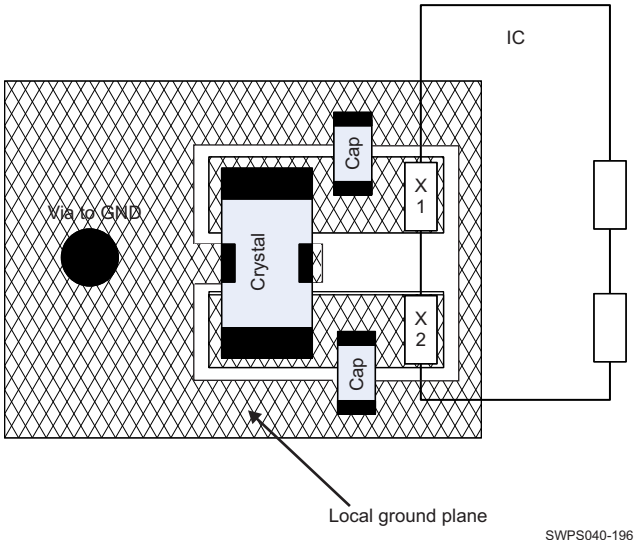


**Figure 8-31. Slow Clock PCB Requirements**

### *8.8.2 Oscillator Ground Connection*

Although the impedance of a ground plane is low it is, of course, not zero. Therefore, any noise current in the ground plane causes a voltage drop in the ground. Figure 8-32 shows the grounding scheme for slow (low frequency) clock generated from the internal oscillator.


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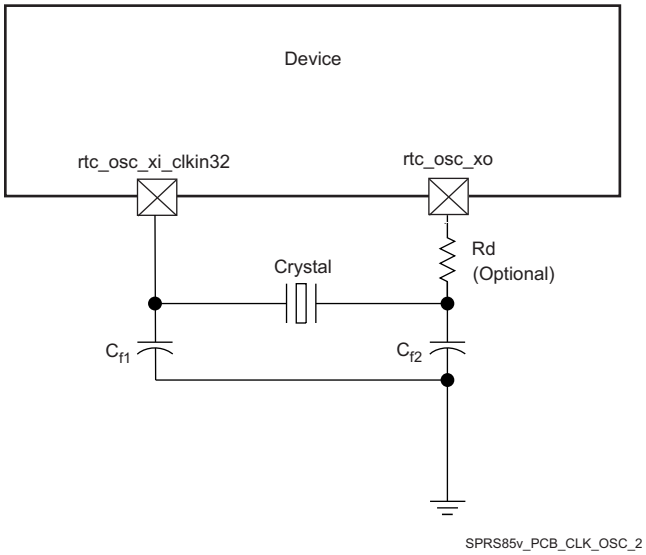
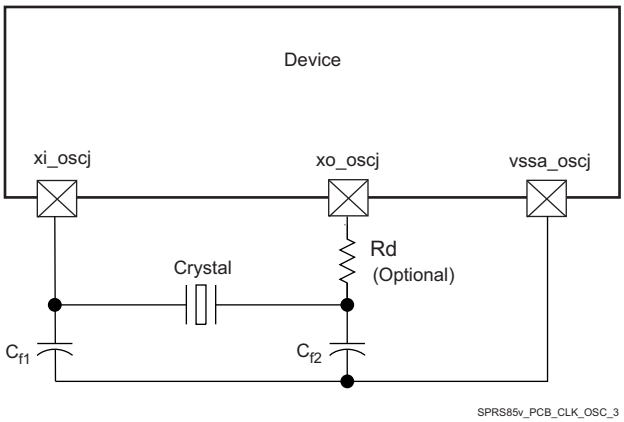



**Figure 8-32. Grounding Scheme for Low-Frequency Clock**

Figure 8-33 shows the grounding scheme for high-frequency clock.




(1) j in *_osc = 0 or 1

**Figure 8-33. Grounding Scheme for High-Frequency Clock**

# 9 Device and Documentation Support

TI offers an extensive line of development tools, including methods to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules as listed below.

## 9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, AM572x). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

**X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

**P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

**null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

**TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.

**TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM572x devices in the ABC package type, see the Package Option Addendum of this document, the TI website (ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the Silicon Errata (literature number SPRZ429).

### *9.1.1 Standard Package Symbolization*

**NOTE**

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.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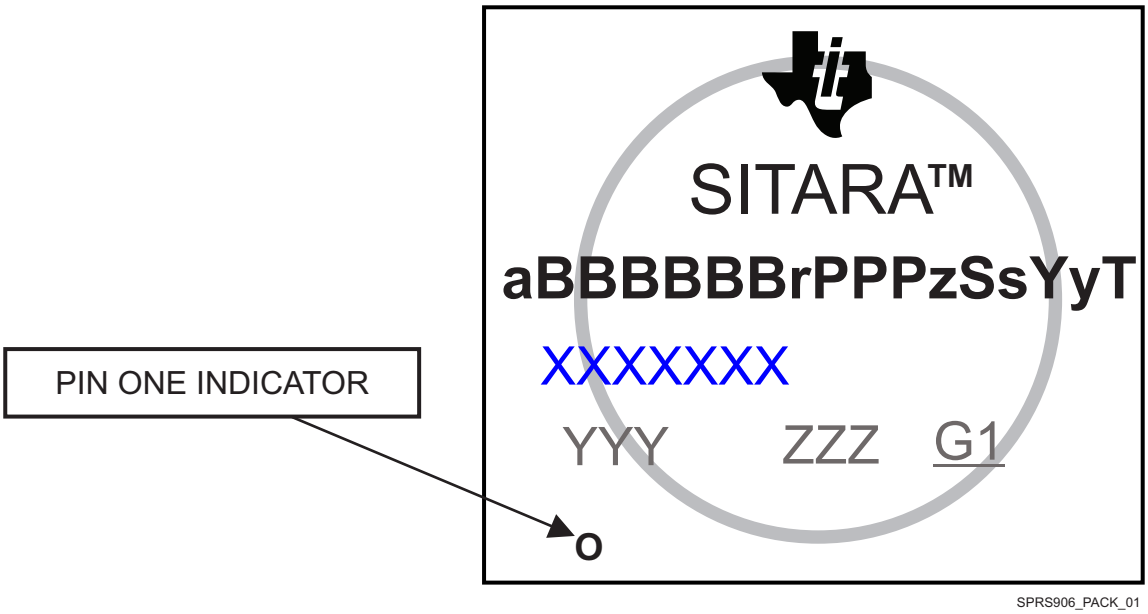


**Figure 9-1. Printed Device Reference**

### *9.1.2 Device Naming Convention*

**Table 9-1. Nomenclature Description**

| FIELD PARAMETER | FIELD DESCRIPTION | VALUE | DESCRIPTION |
|---|---|---|---|
| a | Device evolution stage | X | Prototype |
| | | P | Preproduction (production test flow, no reliability data) |
| | | BLANK | Production |
| BBBBBB | Base production part number | AM5729 | Super Tier (See Table 3-1, *Device Comparison*) |
| | | AM5728 | High Tier (See Table 3-1, *Device Comparison*) |
| | | AM5726 | Low Tier (See Table 3-1, *Device Comparison*) |
| r | Device revision | BLANK | SR 1.0 |
| | | A | SR 1.1 |
| | | B | SR 2.0 |
| PPP | Package Designator | ABC | ABC S-PBGA-N760 (23mm × 23mm) Package |
| z | Device Speed | X | High speed grade (see Table 5-5, *Speed Grade Maximum Frequency*) |
| | | OTHER | Alternate speed grade |
| Ss | Security Identifier | TU | Dummy key secure device |
| | | BLANK | General purpose device |
| Yy | Device type | E | All industrial protocols enabled (basic protocols plus EtherCAT slave and POWERLINK slave) |
| | | BLANK | Basic Industrial protocols enabled |
| | | Yn | Letter followed by number indicates HS device with customer key |
| T | Temperature [(2)] | A | Extended (see Table 5-4, *Recommended Operating Conditions*) |
| | | BLANK | Commercial (see Table 5-4, *Recommended Operating Conditions*) |
| XXXXXXX | Lot Trace Code (LTC) | | |
| YYY | Production Code; For TI use only | | |
| ZZZ | Production Code; For TI use only | | |
| O | Pin one designator | | |
| G1 | ECAT—Green package designator | | |

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.
Prototype devices are shipped against the following disclaimer:
"This product is still in development and is intended for internal evaluation purposes."
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

(2) Applies to device max junction temperature.

**NOTE**

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

## 9.2 Tools and Software

The following products support development for AM572x platforms:

### Design Kits and Evaluation Modules

#### AM572x Evaluation Module

The AM572x Evaluation Module provides an affordable platform to quickly start evaluation of Sitara™ Arm® Cortex®-A15 AM57x Processors (AM5728, AM5726, AM5718, AM5716) and accelerate development for HMI, machine vision, networking, medical imaging and many other industrial applications. It is a development platform based on the dual Arm® Cortex®-A15, dual C66x DSP processor that is integrated with tons of connectivity such as PCIe, SATA, HDMI, USB 3.0/2.0, Dual Gigabit Ethernet, and more. The AM572x Evaluation Module also integrates video and 3D/2D graphics acceleration, as well as a dual-core Programmable Real-time Unit (PRU) and dual Arm® Cortex®-M4 cores.

#### AM572x Industrial Development Kit (IDK)

The AM572x Industrial Development Kit (IDK) is a development platform for evaluating the industrial communication and control capabilities of Sitara AM572x processors for applications in factory automation, drives, robotics, grid infrastructure, and more. AM572x processors include dual PRU-ICSS (Programmable Real-time Unit for Industrial Communications) sub-systems which can be used for industrial Ethernet protocols such as Profinet, EtherCAT, Ethernet/IP, and others. The TMDXIDK5728 breaks out six ports of Ethernet, four of which can be used concurrently: 2x Gb Ethernet ports and 2x 10/100 Ethernet ports from the PRU-ICSS subsystems.

### Development Tools

#### Code Composer Studio (CCS) Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

#### Pin mux tool

The Pin MUX Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs. Results are output as C header/code files that can be imported into software development kits (SDKs) or used to configure customer's custom software. Version 4 of the Pin Mux utility adds the capability of automatically selecting a mux configuration that satisfies the entered requirements.

#### Power Estimation Tool (PET)

Power Estimation Tool (PET) provides users the ability to gain insight in to the power consumption of select TI processors. The tool includes the ability for the user to choose multiple application scenarios and understand the power consumption as well as how advanced power saving techniques can be applied to further reduce overall power consumption.

### Models


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**AM572x BSDL Model** BSDL Model

**AM572x IBIS Model** IBIS Model

**AM572x 23 mm Thermal Models** Thermal Model

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

## 9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the AM572x devices.

**Technical Reference Manual**

**AM572x Sitara™ Processors Silicon Revision 2.0, 1.1**
Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM572x family of devices.

**Errata**

**AM572x Sitara™ Processors Silicon Revision 2.0, 1.1**
Describes the known exceptions to the functional specifications for the device.

## 9.4 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 9-2. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| AM5729 | Click here | Click here | Click here | Click here | Click here |
| AM5728 | Click here | Click here | Click here | Click here | Click here |
| AM5726 | Click here | Click here | Click here | Click here | Click here |

## 9.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 9.6 Trademarks

Sitara, E2E are trademarks of Texas Instruments.
Arm, Cortex are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
HDQ is a trademark of Benchmarq.
1-Wire is a registered trademark of Dallas Semiconductor.
HDMI is a registered trademark of HDMI Licensing, LLC.
PowerVR is a registered trademark of Imagination Technologies Limited.
MMC, eMMC are trademarks of MultiMediaCard Association.

I$^2$C is a trademark of NXP Semiconductors.
PCI-Express is a registered trademark of PCI-SIG.
SD is a registered trademark of SD Card Association.
Vivante is a registered trademark of Vivante Corporation.
All other trademarks are the property of their respective owners.

## 9.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.8 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.


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# 10 Mechanical, Packaging, and Orderable Information

## 10.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AM5726BABCX | ACTIVE | FCBGA | ABC | 760 | 60 | Green (RoHS & no Sb/Br) | Call TI \| SNAGCU | Level-3-250C-168 HR | 0 to 90 | AM5726BABCX SITARATM | Samples |
| AM5726BABCXA | ACTIVE | FCBGA | ABC | 760 | 60 | Green (RoHS & no Sb/Br) | Call TI \| SNAGCU | Level-3-250C-168 HR | -40 to 105 | AM5726BABCXA SITARATM | Samples |
| AM5726BABCXAR | ACTIVE | FCBGA | ABC | 760 | 250 | Green (RoHS & no Sb/Br) | Call TI \| SNAGCU | Level-3-250C-168 HR | -40 to 105 | AM5726BABCXA SITARATM | Samples |
| AM5726BABCXEA | ACTIVE | FCBGA | ABC | 760 | 60 | Green (RoHS & no Sb/Br) | Call TI \| SNAGCU | Level-3-250C-168 HR | -40 to 105 | AM5726BABCXEA SITARATM | Samples |
| AM5728BABCX | ACTIVE | FCBGA | ABC | 760 | 60 | Green (RoHS & no Sb/Br) | Call TI \| SNAGCU | Level-3-250C-168 HR | 0 to 90 | AM5728BABCX SITARATM | Samples |
| AM5728BABCXA | ACTIVE | FCBGA | ABC | 760 | 60 | Green (RoHS & no Sb/Br) | Call TI \| SNAGCU | Level-3-250C-168 HR | -40 to 105 | AM5728BABCXA SITARATM | Samples |
| AM5728BABCXEA | ACTIVE | FCBGA | ABC | 760 | 60 | Green (RoHS & no Sb/Br) | Call TI \| SNAGCU | Level-3-250C-168 HR | -40 to 105 | AM5728BABCXEA SITARATM | Samples |
| AM5729BABCX | PREVIEW | FCBGA | ABC | 760 | 60 | Green (RoHS & no Sb/Br) | Call TI \| SNAGCU | Level-3-250C-168 HR | 0 to 90 | AM5729BABCX SITARATM | |
| AM5729BABCXA | PREVIEW | FCBGA | ABC | 760 | 60 | Green (RoHS & no Sb/Br) | Call TI \| SNAGCU | Level-3-250C-168 HR | -40 to 105 | AM5729BABCXA SITARATM | |
| AM5729BABCXEA | PREVIEW | FCBGA | ABC | 760 | 60 | Green (RoHS & no Sb/Br) | Call TI \| SNAGCU | Level-3-250C-168 HR | -40 to 105 | AM5729BABCXEA SITARATM | |
| AM5729BABCXEAR | PREVIEW | FCBGA | ABC | 760 | 250 | Green (RoHS & no Sb/Br) | Call TI \| SNAGCU | Level-3-250C-168 HR | -40 to 105 | AM5729BABCXEA SITARATM | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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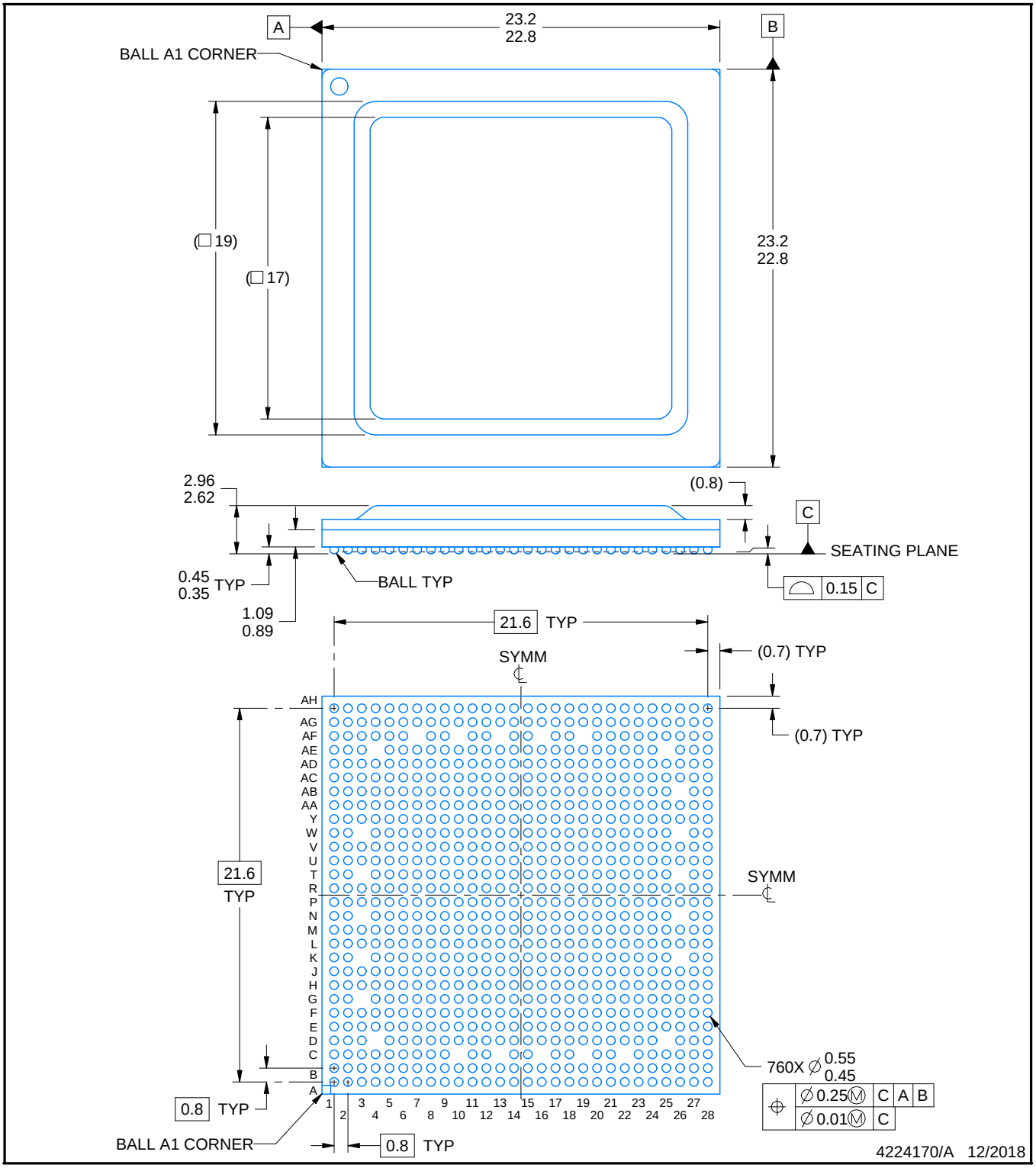
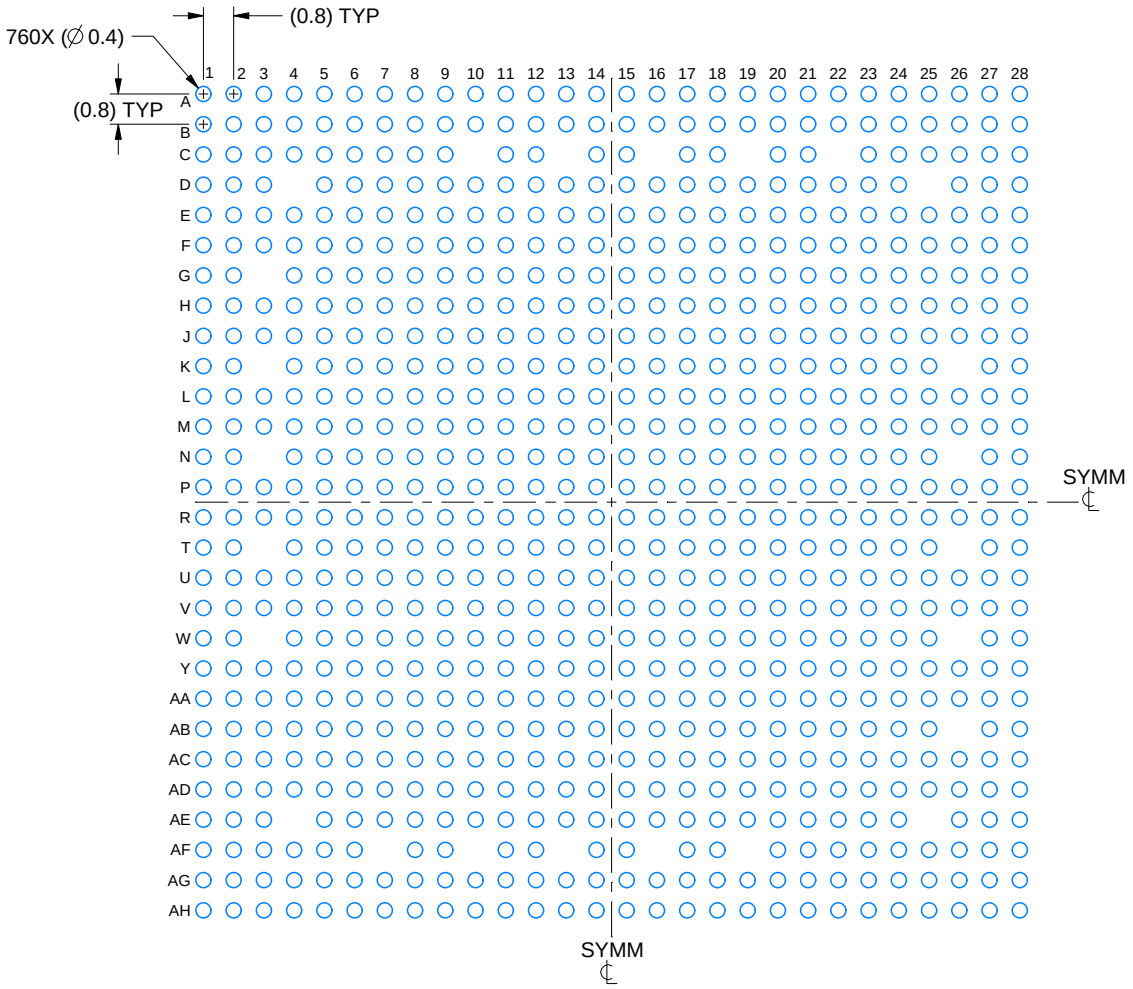
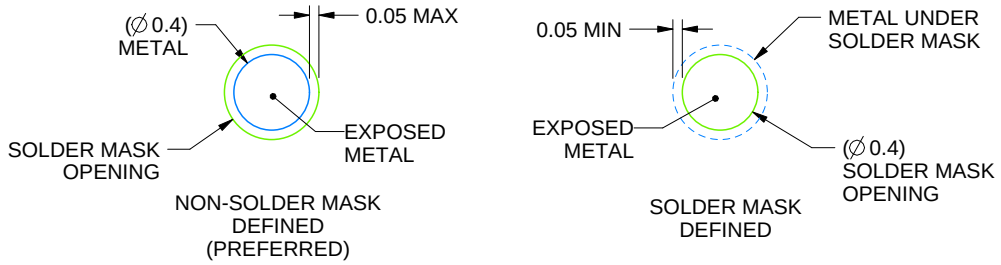



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X




SOLDER MASK DETAILS
NOT TO SCALE

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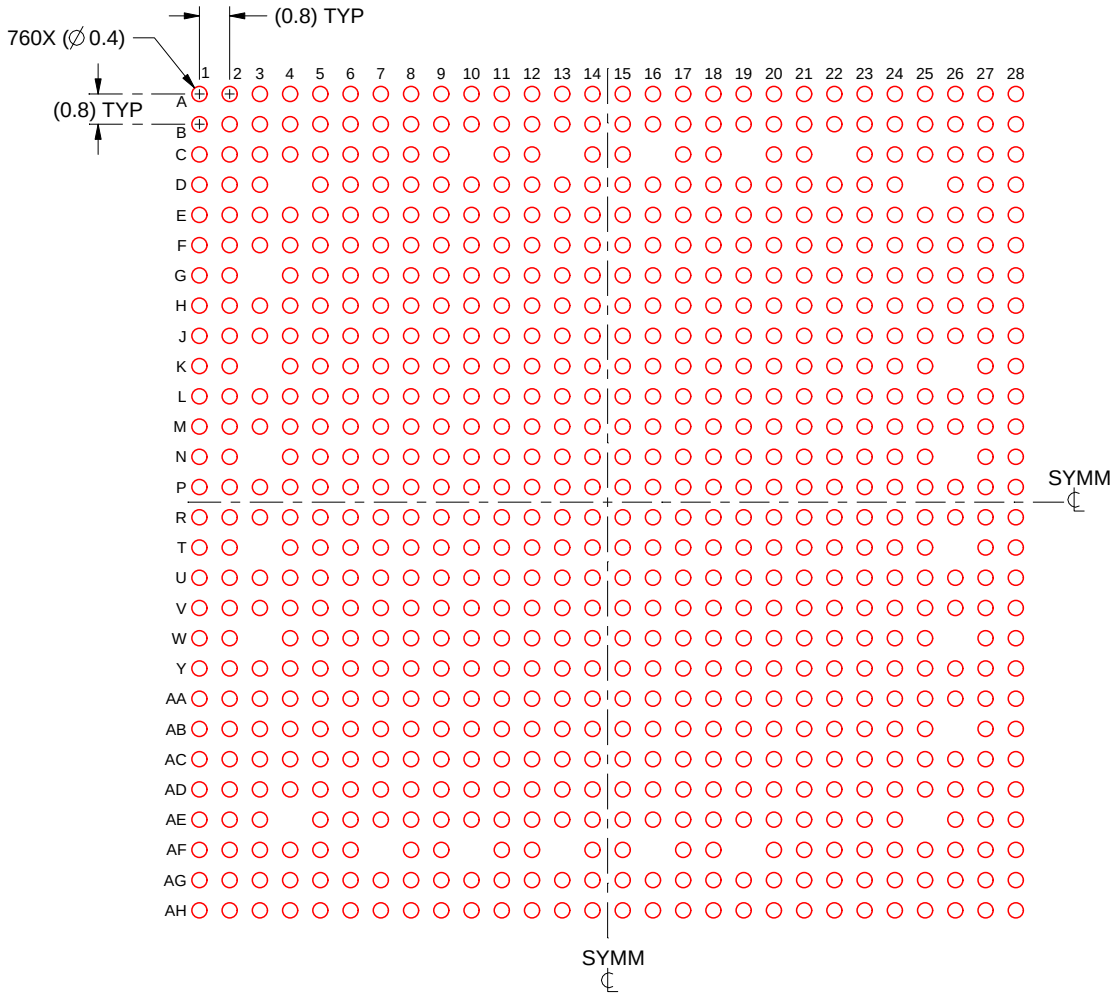
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).




SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:5X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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