VECTRON INTERNATIONAL
A DOVER COMPANY

VS-700
Voltage Controlled SAW Oscillator

Description

The VS-700 is a SAW based voltage controlled oscillator that operates at the fundamental frequency of the internal SAW filter. The SAW filter is a high-Q quartz device that enables the circuit to achieve low phase jitter performance over a wide operating temperature range. The oscillator is housed in a hermetically sealed leadless surface mount package offered on tape and reel. It has an output disable to facilitate on-board testing.

Features

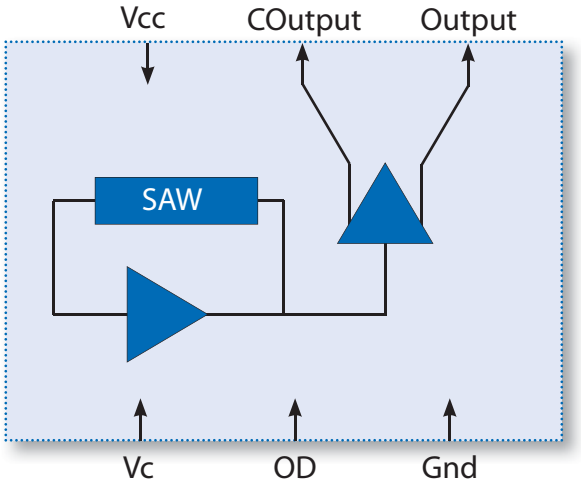
- Industry Standard Package, 5.0 x 7.5 x 2.5 mm
- Output Frequencies from 500 MHz to 850 MHz
- 3.3 V Operation
- Low Jitter < 0.25 ps-rms across 50 kHz to 80 MHz
- LV-PECL Configuration with Fast Transition Times
- Complementary Outputs
- Output Disable Feature
- Product is free of lead and compliant to EC RoHS Directive

Applications

PLL circuits for clock smoothing and frequency translation

Description	Standard
1-2-4 Gigabit Fibre Channel	INCITS 352-2002
10 Gigabit Fibre Channel	INCITS 364-2003
10GbE LAN / WAN	IEEE 802.3ae
OC-192	ITU-T G.709
SONET / SDH	GR-253-CORE Issue4
WiMax	IEEE 802.16

Block Diagram



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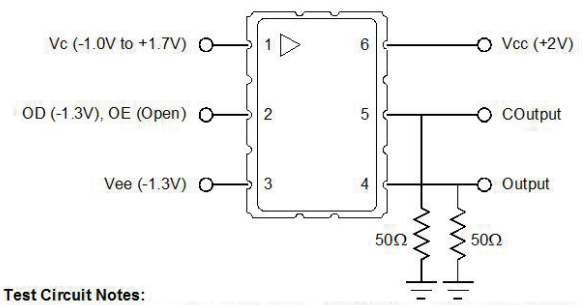
Rev: 08Dec2009

Performance Specifications

Electrical Performance						
Parameter	Symbol	Min	Typical	Maximum	Units	Notes
Supply						
Voltage	V_{CC}	2.97	3.3	3.63	V	2,3
Current (No Load)	I_{CC}		55	70	mA	3
Frequency						
Nominal Frequency	f_N		500 - 850		MHz	1,2,3
Absolute Pull Range	APR	±50			ppm	1,2,3,8
Linearity	Lin		±5		%	2,4,8
Gain Transfer (See pg 5)	K_V		+390		ppm/V	2,8
Temperature Stability	f_{STAB}		±100		ppm	1,6
Outputs						
Mid Level		V_{CC}-1.5	V_{CC}-1.3	V_{CC}-1.1	V	2,3
Swing		500	650	800	mV-pp	2,3
Current	I_{OUT}			20	mA	6
Rise Time	t_R		250	400	ps	5,6
Fall Time	t_F		250	400	ps	5,6
Symmetry	SYM	45	50	55	%	2,3
Spurious Suppression		50	60		dBc	6
Jitter (See pg 5)	ϕJ		0.120	0.250	ps-rms	6,7
Control Voltage						
Input Impedance	Z_C		100		kΩ	6
Modulation Bandwidth	BW		500		kHz	6
Operating Temperature	T_{OP}	-40		+85	°C	1,3
Package Size		5.0 x 7.5 x 2.5			mm	

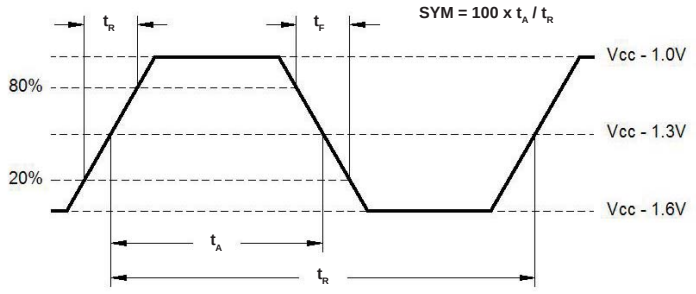
1] See Standard Frequencies and Ordering Information (Pg 7).
2] Parameters are tested with production test circuit below (Fig 1).
3] Parameters are tested at ambient temperature with test limits guardbanded for specified operating temperature.
4] Measured as the maximum deviation from the best straight-line fit, per MIL-0-55310.
5] Measured from 20% to 80% of a full output swing (Fig 2).
6] Not tested in production, guaranteed by design, verified at qualification.
7] Integrated across 50 kHz to 80 MHz, per GR-253-CORE Issue4.
8] Tested with Vc = 0.3V to 3.0V.

Fig 1: Test Circuit



Test Circuit Notes:
1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased Down 1.3V.
2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.
3) 50Ω Terminations are Within Test Equipment.

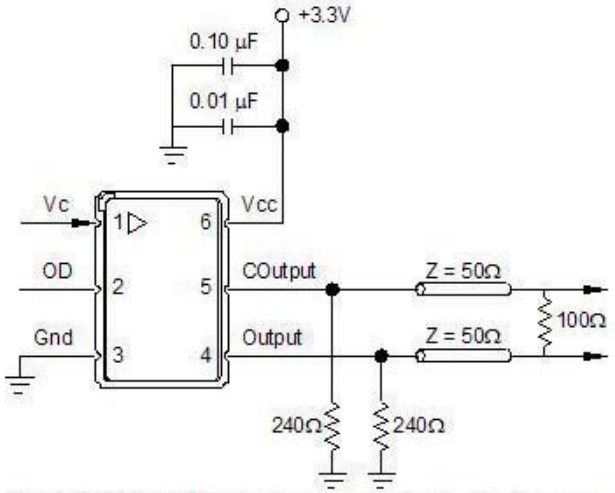
Fig 2: 10K LV-PECL Waveform



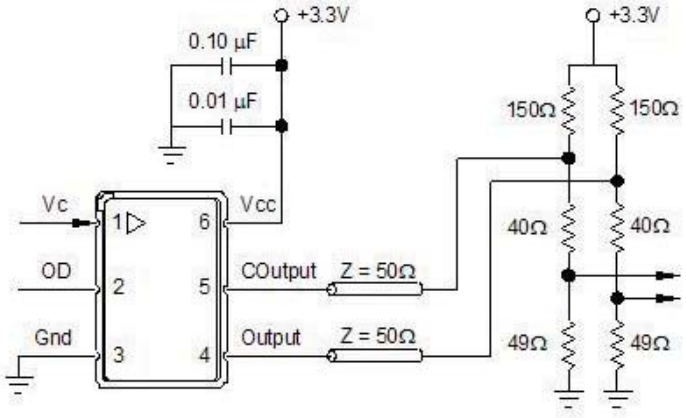
Absolute Maximum Ratings			
Parameter	**Symbol**	**Ratings**	**Unit**
Power Supply	V_{CC}	0 to 6	V
Input Current	I_{IN}	100	mA
Output Current	I_{OUT}	25	mA
Voltage Control Range	V_C	0 to V_{CC}	V
Storage Temperature	T_{STR}	-55 to 125	°C
Soldering Temperature / Duration	T_{PEAK} / t_P	260 / 40	°C / sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Also, exposure to these absolute maximum ratings for extended periods may adversely affect device reliability. Functional operation is not implied at these or any other conditions in excess of those represented in the operational sections of this datasheet. Permanent damage is also possible if any device input (Vc or OD) draws >100 mA.

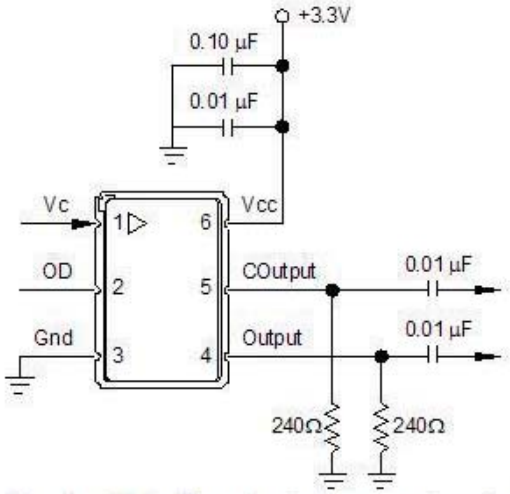
Suggested Output Load Configuration



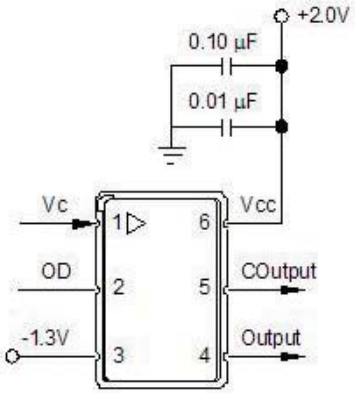
LV-PECL to LV-PECL: For short transmission lengths, the power consumption could be reduced by removing the 100Ω resistor and doubling the value of the pull down resistors.



LV-PECL to LVDS: Restricted for short transmission lengths. Configuration may require modification depending on LVDS receiver.

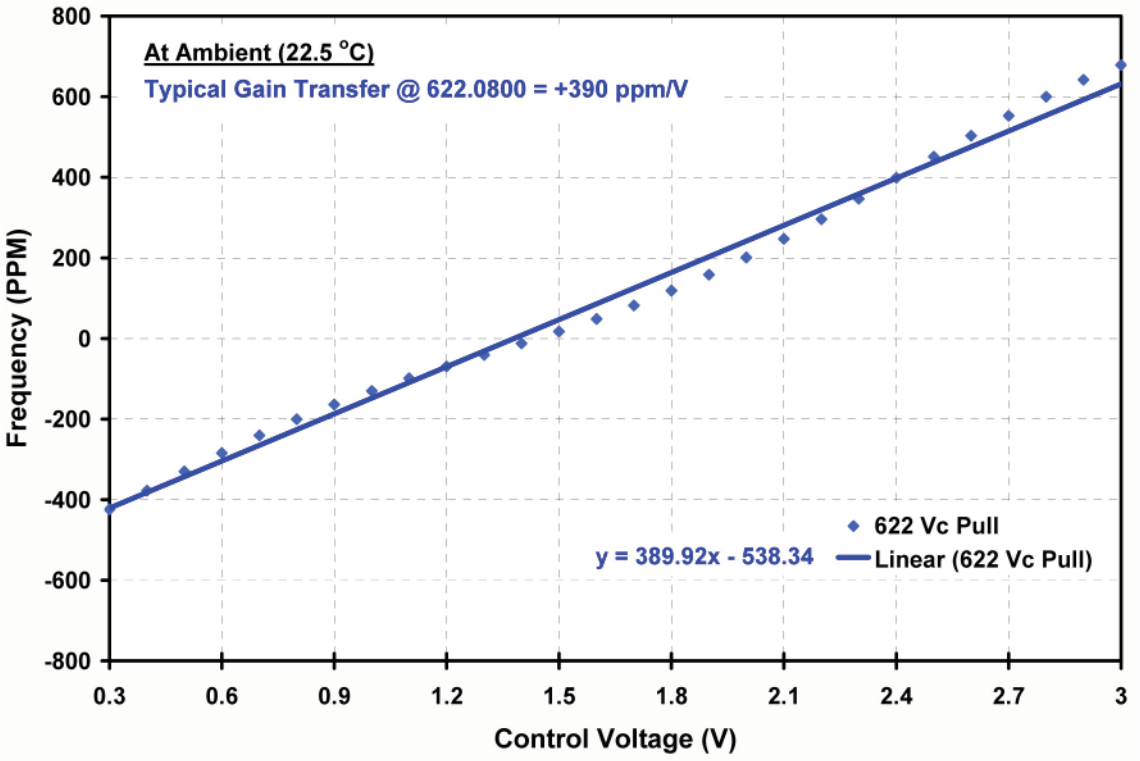


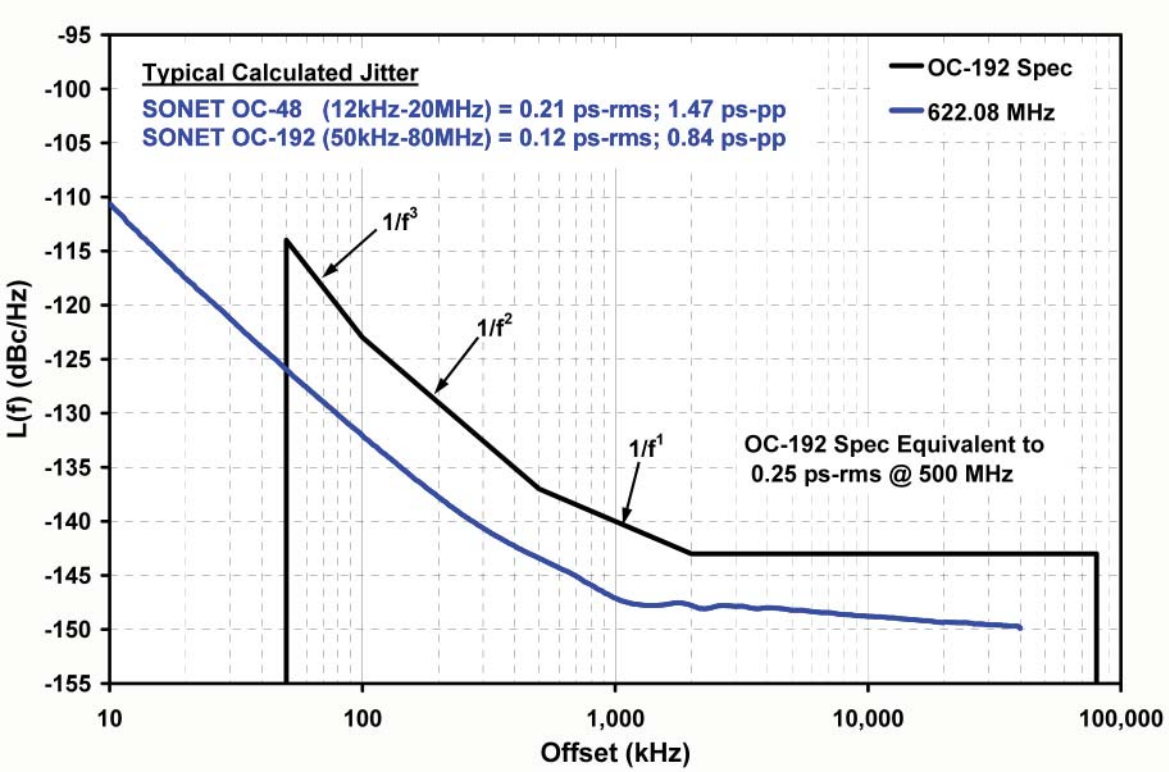
Functional Test: Allows standard power supply configuration. Since AC coupled, the LV-PECL levels cannot be measured.



Production Test: Allows direct DC coupling into 50Ω measurement equipment. Must bias the power supplys as shown. Similiar to figure 1.

Typical Characteristics





Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VS-700 family is capable of meeting the following qualification tests:

Environmental Compliance	
Parameter	**Conditions**
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

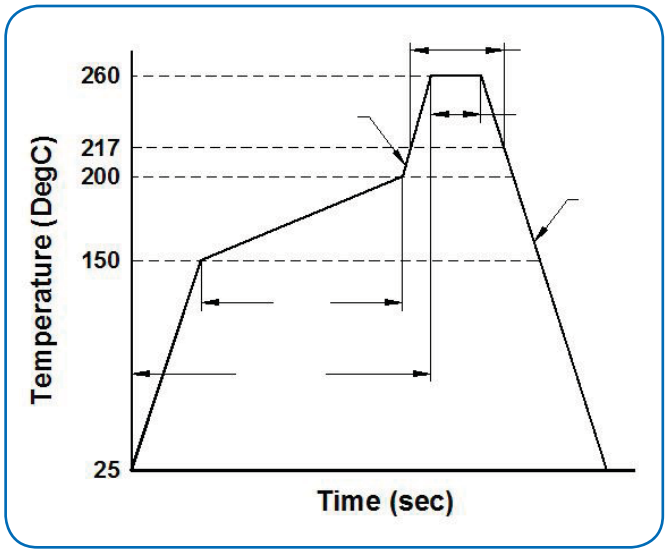
Handling Precautions

Although ESD protection circuitry has been designed into the VS-700 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

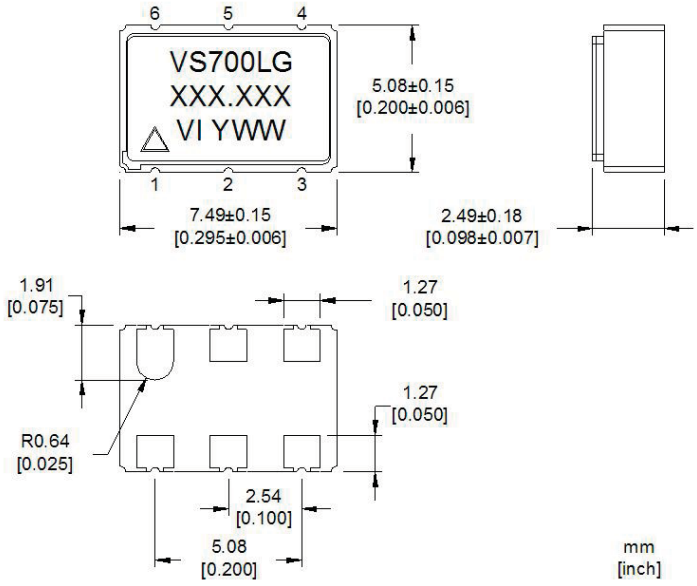
ESD Ratings		
Model	**Minimum**	**Conditions**
Human Body Model	1500V	MIL-STD-883, Method 3015
Charged Device Model	1000V	JEDEC, JESD22-C101

Reflow Profile (IPC/JEDEC J-STD-020C)		
Parameter	**Symbol**	**Value**
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	T_{AMB-P}	480 sec Max
Time at 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The device has been qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The VS-700 device is hermetically sealed so an aqueous wash is not an issue.

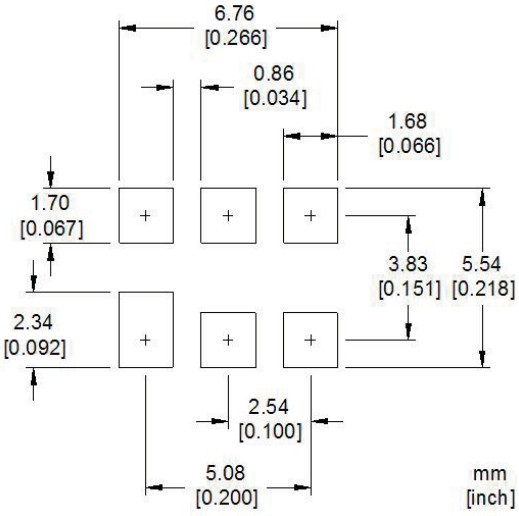


Outline Drawing



Suggested Pad Layout

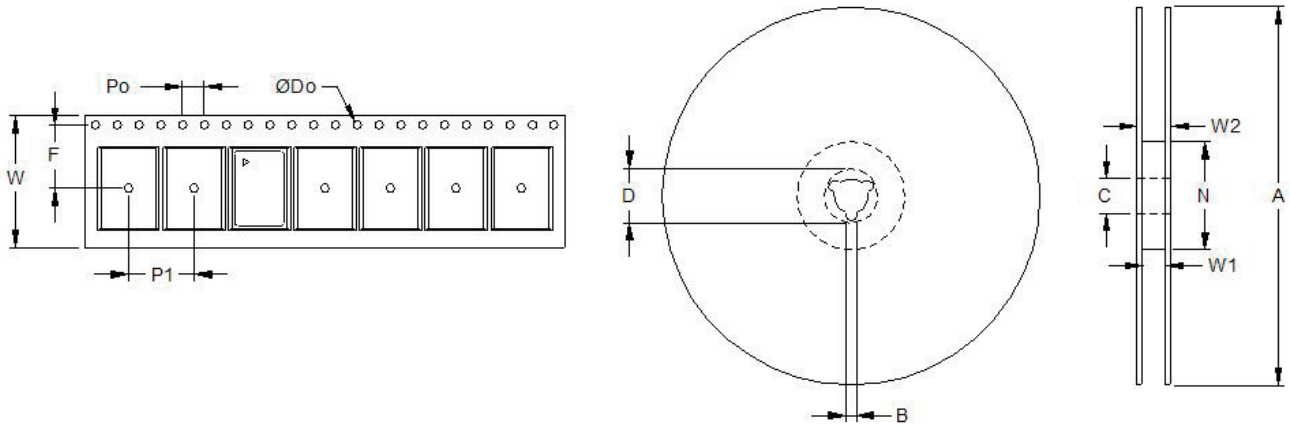
Dimensions in inches (mm)



Pin Out		
Pin	**Symbol**	**Function**
1	V_C	Control Voltage
2	OD	Output Disable Disabled = LV-CMOS Logic 0 (or Gnd) Enabled = LV-CMOS Logic 1 (or Open)
3	GND	Case and Electrical Ground
4	Output	VCSO Output
5	COutput	Complementary Output
6	V_{CC}	Power Supply Voltage (3.3V ±10%)

Marking Key	
Position 6	**Position 7**
L = LFF	G = GNN
	H = HNN

Tape & Reel (EIA-481-2-A)



Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	**W**	**F**	**Do**	**Po**	**P1**	**A**	**B**	**C**	**D**	**N**	**W1**	**W2**	**# Per Reel**
Tolerance	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Min**	**Typ**	**Min**	**Min**	**Typ**	**Max**	
VS-700	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

Standard Frequencies (MHz)							
500.000000	531.250000	552.960000	569.196400	595.056000	622.080000	624.693800	625.000000
627.329600	629.987800	637.500000	639.120000	640.000000	644.531300	647.239400	648.806400
657.421900	660.184200	666.514300	669.326582	669.642900	670.838600	672.162700	673.456600
674.278800	690.569200	693.483000	693.750000	704.380600	707.352700	709.375000	716.573200
718.750000	719.734400	737.280000	748.070900	750.000000	777.600000	779.568600	780.881000
781.250000	796.875000	800.000000	805.664100	809.063500	838.860800		

Other Frequencies Available Upon Request.

Ordering Information

VS - 700 - L F F - G N N - xxxMxxxxxx

Product Family
VS: VCSO

Package
700: 5 x 7.5 x 2.5 mm

Input
L: 3.3 V

Output
F: LV-PECL

Operating Temperature
F: -40 to 85 °C

Absolute Pull Range
G: ± 50 ppm
H: ± 100 ppm

Other (Future Use)
N: N/A

Other (Future Use)
N: N/A

Frequency (See Above)
500M000000 - 850M000000

Example: VS-700-LFF-GNN-622M080000

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