19-4093; Rev 0; 5/08

EVALUATION KIT AVAILABLE

300MHz to 450MHz Frequency-Programmable ASK/FSK Transmitter

General Description

The MAX7057 frequency-programmable UHF transmitter is designed to transmit ASK/FSK data at a wide range of frequencies from 300MHz to 450MHz. The MAX7057 has internal tuning capacitors at the output of the power amplifier that are programmable for matching to an antenna or load. This allows the user to change to a new frequency and match the antenna at the new frequency simultaneously. The MAX7057 transmits at a data rate up to 100kbps nonreturn-to-zero (NRZ) (50kbps Manchester coded). Typical transmitted power into a 50Ω load is +9.2dBm with a +2.7V supply. The device operates from +2.1V to +3.6V and typically draws under 12.5mA of current in FSK mode (8.5mA in ASK mode) when the antenna-matching network is designed to operate over the 315MHz to 433.92MHz frequency range. For narrower operating frequency ranges, the matching network can be redesigned to improve efficiency. The standby current is less than 1µA at room temperature.

The MAX7057 reference frequency from the crystal oscillator is multiplied by a fully integrated fractional-N phase-locked loop (PLL). The multiplying factor of the PLL is set by a 16-bit number, with 4 bits for integer and 12 bits for fraction; the multiplying factor can be anywhere between 19 and 28. The 12-bit fraction in the synthesizer sets a tuning resolution equal to the reference frequency divided by 4096; frequency deviation can be set as low as ±2kHz and as high as ±100kHz. The fractional-N synthesizer eliminates the problems associated with oscillator-pulling FSK signal generation. The MAX7057 has a serial peripheral interface (SPI™) for selecting all the necessary settings.

The MAX7057 is available in a 16-pin SO package and is specified to operate in the -40°C to +125°C automotive temperature range.

Applications

RF Remote Controls
Garage Door Openers
Home Automation
Automotive
Wireless Sensors
Wireless Game Consoles
Wireless Computer Peripherals
Security Systems

Features

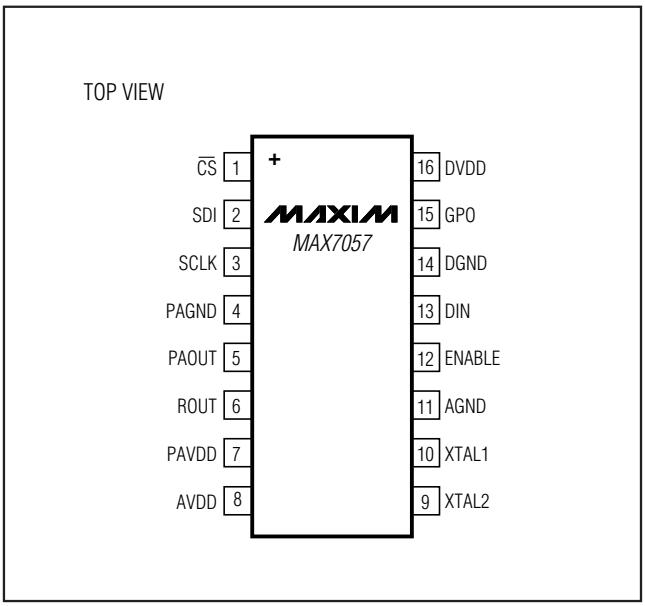
- **Programmable Frequency Operation with Single Crystal**
- **Internal Variable Capacitor for Antenna Tuning with Single-Matching Network**
- **100kbps Data Rate (NRZ)**
- **+2.1V to +3.6V Single-Supply Operation**
- **< 12.5mA (FSK), < 8.5mA (ASK) DC Current Drain**
- **< 1µA Standby Current**
- **ASK/FSK Modulation**
- **47% Carrier Tuning Range Using One Crystal**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7057ASE+	-40°C to +125°C	16 SO

+Denotes a lead-free package.

Pin Configuration



Typical Application Circuit and Functional Diagram appear at end of data sheet.

SPI is a trademark of Motorola, Inc.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

300MHz to 450MHz Frequency-Programmable ASK/FSK Transmitter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, PAVDD, AVDD, DVDD to AGND, DGND, PAGND .....-0.3V to +4.0V
All Other Pins....._GND - 0.3V to _V_{DD} + 0.3V
Continuous Power Dissipation (T_A = +70°C)
16-Pin SO (derate 8.7mW/°C above +70°C).....695.7mW
Operating Temperature .....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, 50Ω system impedance, tuned for 315MHz to 433.92MHz operation, AVDD = DVDD = PAVDD = +2.1V to +3.6V, f_{RF} = 300MHz to 450MHz, $f_{CRYSTAL}$ = 16MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at AVDD = DVDD = PAVDD = +2.7V, T_A = +25°C, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C, and guaranteed by design and characterization over temperature, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	PAVDD, AVDD, and DVDD connected to power supply, V_{DD}		2.1	2.7	3.6	V
Supply Current	I_{DD}	PA off, V_{DIN} at 0% duty cycle (ASK)	f_{RF} = 315MHz		3.9	6.5	mA
			f_{RF} = 433.92MHz		4.5	7.5	
		V_{DIN} at 50% duty cycle (ASK) (Notes 1, 2, 3)	f_{RF} = 315MHz		8.1	15.1	
			f_{RF} = 433.92MHz		8.5	15.0	
		V_{DIN} at 100% duty cycle (FSK) (Note 1)	f_{RF} = 315MHz		12.2	23.7	
			f_{RF} = 433.92MHz		12.4	22.4	
Standby Current	I_{STDBY}	V_{ENABLE} < V_{IL}	T_A = +25°C (Note 3)		0.8		µA
			T_A < +85°C (Note 3)		1	6.4	
			T_A < +125°C		6.2	20.1	
DIGITAL I/O							
Input High Threshold	V_{IH}			0.9 x DV_{DD}			V
Input Low Threshold	V_{IL}					0.1 x DV_{DD}	V
Input Pulldown Sink Current					13		µA
Input Pullup Source Current					9		µA
Output-Voltage High	V_{OH}	I_{SINK} = 500µA (GPO)			V_{DD} - 0.37		V
Output-Voltage Low	V_{OL}	I_{SOURCE} = 500µA (GPO)			0.36		V

AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, 50Ω system impedance, tuned for 315MHz to 433.92MHz operation, AVDD = DVDD = PAVDD = +2.1V to +3.6V, f_{RF} = 300MHz to 450MHz, $f_{CRYSTAL}$ = 16MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at AVDD = DVDD = PAVDD = +2.7V, T_A = +25°C, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C, and guaranteed by design and characterization over temperature, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Frequency Range				300		450	MHz
Power-On Time	t_{ON}	ENABLE transition low-to-high, frequency settled to within 50kHz of the desired carrier			120		µs
		ENABLE transition low-to-high, frequency settled to within 5kHz of the desired carrier			260		
Maximum Data Rate		ASK mode	Manchester encoded		50		kbps
			Nonreturn-to-Zero		100		
		FSK mode	Manchester encoded		50		
			Nonreturn-to-Zero		100		
Frequency Switching Time		Time from end of SPI write to frequency settled to within 5kHz of desired carrier			70		µs
PHASE-LOCKED LOOP (PLL)							
VCO Gain	K_{VCO}				320		MHz/V
PLL Phase Noise		f_{RF} = 315MHz	10kHz offset		-78		dBc/Hz
			1MHz offset		-98		
		f_{RF} = 433.92MHz	10kHz offset		-73		
			1MHz offset		-98		
Loop Bandwidth					300		kHz
Reference Frequency Input Level					500		mV_{P-P}
Frequency-Divider Range				19		28	
Frequency Deviation (FSK)				±2		±100	kHz
CRYSTAL OSCILLATOR							
Crystal Frequency	f_{XTAL}			10.71	16	23.68	MHz
Frequency Pulling by V_{DD}					4		ppm/V
Crystal Load Capacitance		(Note 4)			10		pF
POWER AMPLIFIER (PA)							
Output Power (Note 1)	P_{OUT}	T_A = +25°C (Note 3)		3.8	9.2	16.4	dBm
		T_A = +125°C, AVDD = DVDD = PAVDD = +2.1V		2.4	5.2		
		T_A = -40°C, AVDD = DVDD = PAVDD = +3.6V (Note 3)			12.6	17.0	
Modulation Depth					71		dB
Maximum Carrier Harmonics		With output matching network	f_{RF} = 315MHz		-29		dBc
			f_{RF} = 433.92MHz		-44		
Reference Spur					-45		dBc

300MHz to 450MHz Frequency-Programmable ASK/FSK Transmitter

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, 50Ω system impedance, tuned for 315MHz to 433.92MHz operation, AVDD = DVDD = PAVDD = +2.1V to +3.6V, f_{RF} = 300MHz to 450MHz, $f_{CRYSTAL}$ = 16MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at AVDD = DVDD = PAVDD = +2.7V, T_A = +25°C, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C, and guaranteed by design and characterization over temperature, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE (SPI) TIMING CHARACTERISTICS (Figure 1)						
Minimum SCLK Low to Falling-Edge of $\overline{CS}$ Setup Time	t_{SC}			10		ns
Minimum $\overline{CS}$ Low to Rising-Edge of SCLK Setup Time	t_{CSS}			5		ns
Minimum SCLK Low to Rising-Edge of $\overline{CS}$ Setup Time	t_{HCS}			20		ns
Minimum SCLK Low After Rising-Edge of $\overline{CS}$ Hold Time	t_{HS}			5		ns
Minimum Data Valid to SCLK Rising-Edge Setup Time	t_{DS}			10		ns
Minimum Data Valid to SCLK Rising-Edge Hold Time	t_{DH}			5		ns
Minimum SCLK High Pulse Width	t_{CH}			40		ns
Minimum SCLK Low Pulse Width	t_{CL}			40		ns
Minimum $\overline{CS}$ High Pulse Width	t_{CSH}			40		ns
Maximum Transition Time from Falling-Edge of $\overline{CS}$ to Valid GPO	t_{CSG}	C_L = 10pF load capacitance from GPO to DGND		50		ns
Maximum Transition Time from Falling-Edge of SCLK to Valid GPO	t_{CG}	C_L = 10pF load capacitance from GPO to DGND		50		ns

Note 1: Supply current and output power are greatly dependent on board layout and PAOUT match.
Note 2: 50% duty cycle at 10kHz ASK data (Manchester coded).
Note 3: Guaranteed by design and characterization, not production tested.
Note 4: Dependent on PCB trace capacitance.

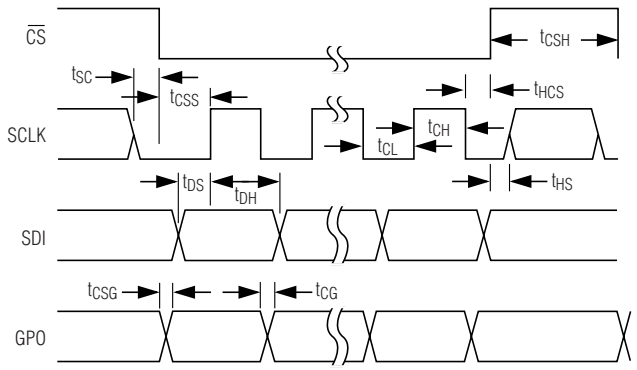
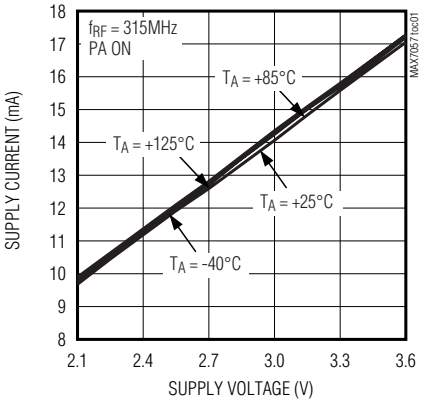


Figure 1. SPI Timing Diagram

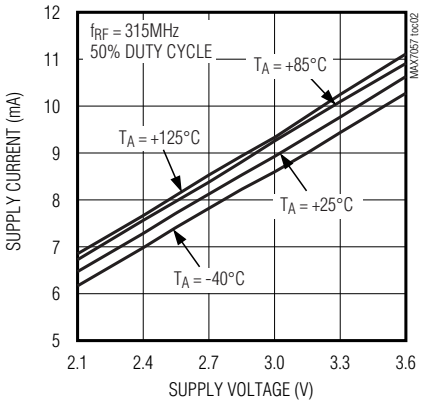
Typical Operating Characteristics

(50Ω system impedance, AVDD = DVDD = PAVDD = +2.1V to +3.6V, f_{RF} = 300MHz to 450MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at AVDD = DVDD = PAVDD = +2.7V, T_A = +25°C, unless otherwise noted.)

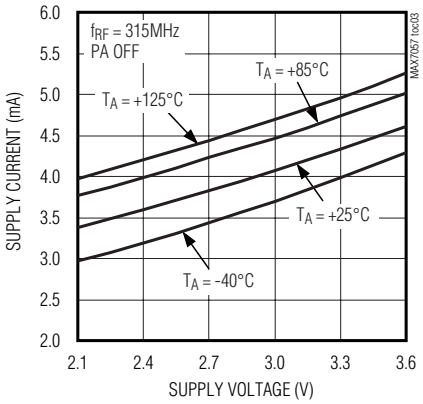
SUPPLY CURRENT vs. SUPPLY VOLTAGE



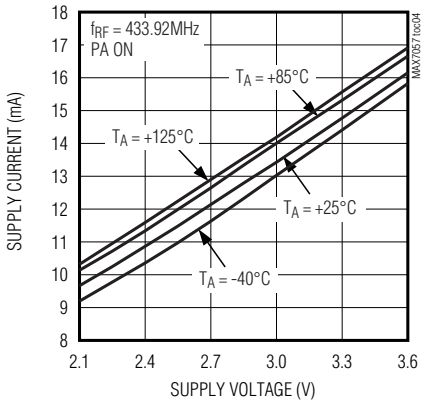
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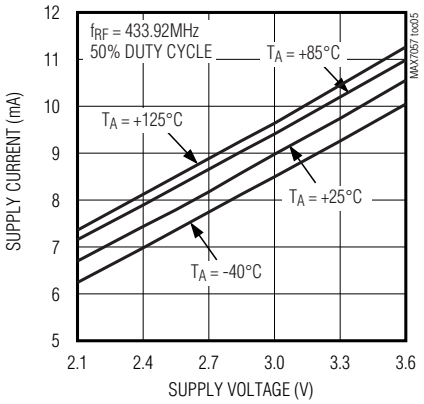
SUPPLY CURRENT vs. SUPPLY VOLTAGE



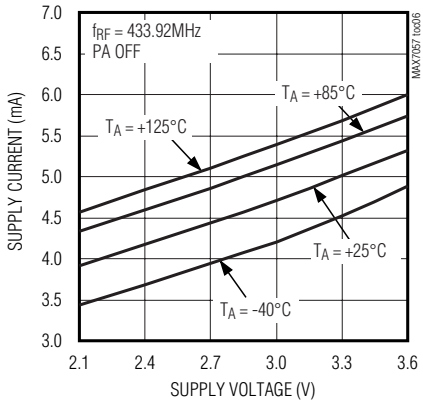
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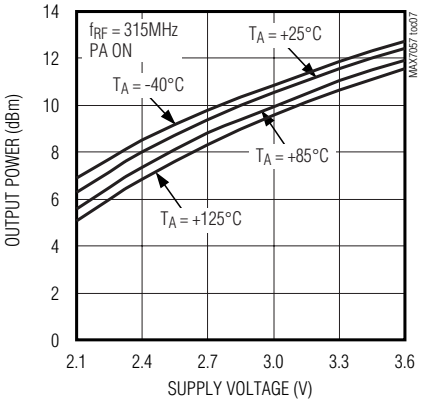
SUPPLY CURRENT vs. SUPPLY VOLTAGE



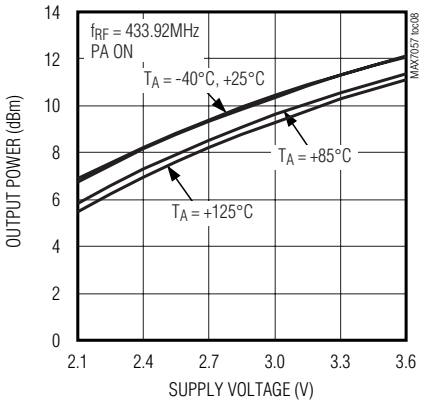
SUPPLY CURRENT vs. SUPPLY VOLTAGE



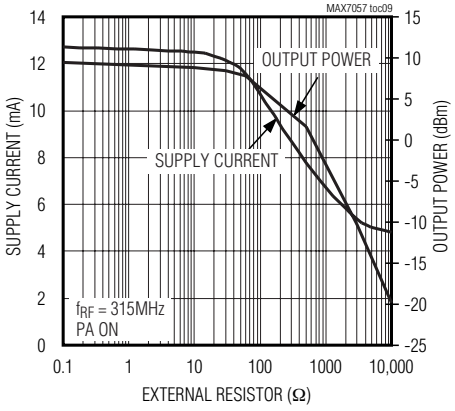
OUTPUT POWER vs. SUPPLY VOLTAGE



OUTPUT POWER vs. SUPPLY VOLTAGE



SUPPLY CURRENT AND OUTPUT POWER vs. EXTERNAL RESISTOR

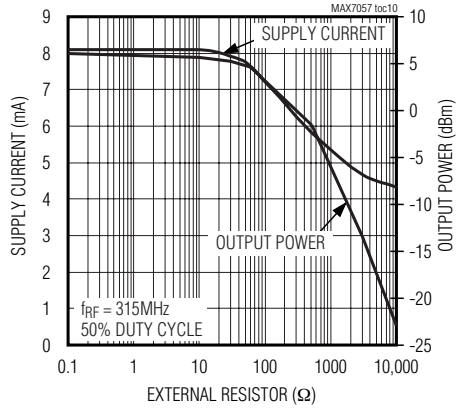


300MHz to 450MHz Frequency-Programmable ASK/FSK Transmitter

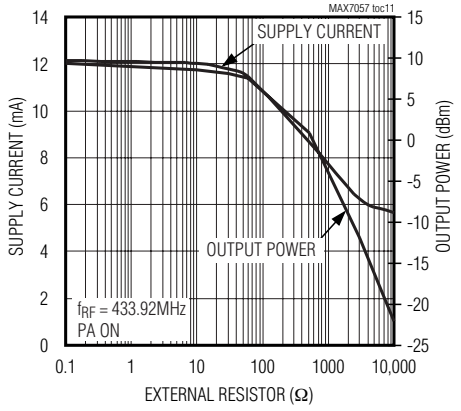
Typical Operating Characteristics (continued)

(50Ω system impedance, AVDD = DVDD = PAVDD = +2.1V to +3.6V, f_{RF} = 300MHz to 450MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at AVDD = DVDD = PAVDD = +2.7V, T_A = +25°C, unless otherwise noted.)

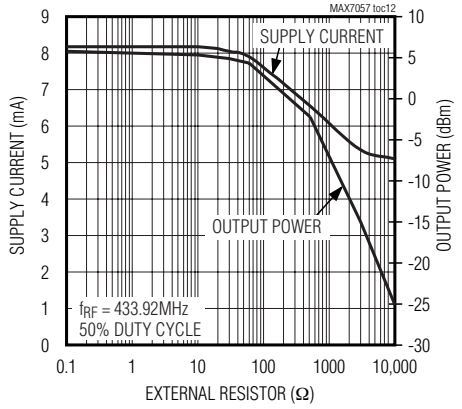
SUPPLY CURRENT AND OUTPUT POWER vs. EXTERNAL RESISTOR



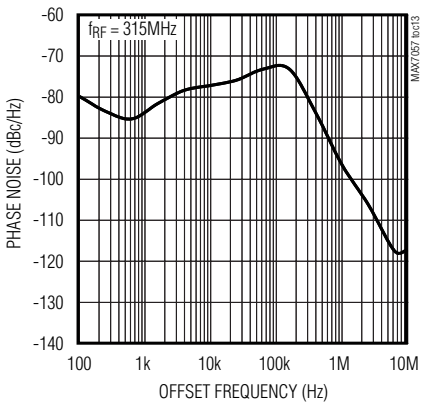
SUPPLY CURRENT AND OUTPUT POWER vs. EXTERNAL RESISTOR



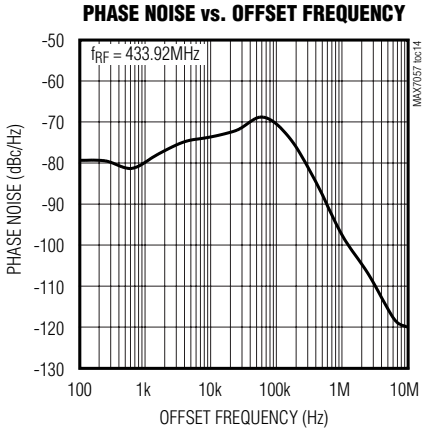
SUPPLY CURRENT AND OUTPUT POWER vs. EXTERNAL RESISTOR



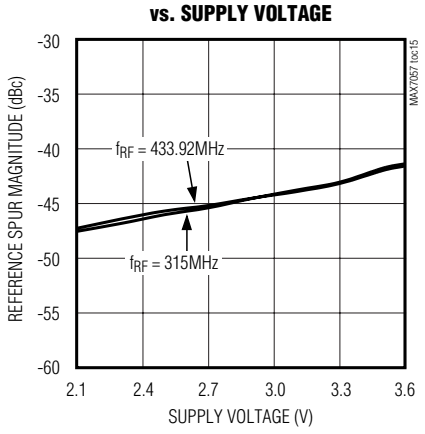
PHASE NOISE vs. OFFSET FREQUENCY



PHASE NOISE vs. OFFSET FREQUENCY



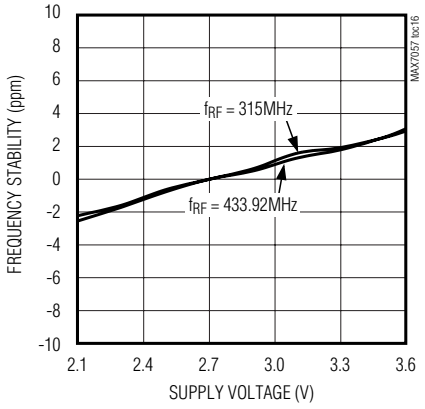
REFERENCE SPUR MAGNITUDE vs. SUPPLY VOLTAGE



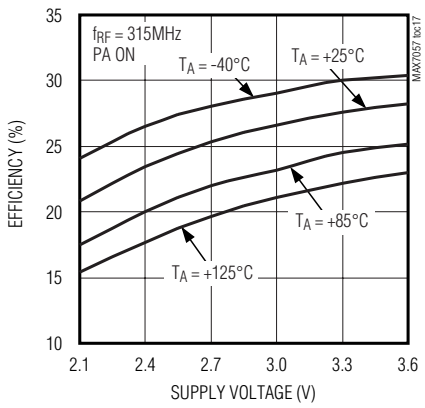
Typical Operating Characteristics (continued)

(50Ω system impedance, AVDD = DVDD = PAVDD = +2.1V to +3.6V, f_{RF} = 300MHz to 450MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at AVDD = DVDD = PAVDD = +2.7V, T_A = +25°C, unless otherwise noted.)

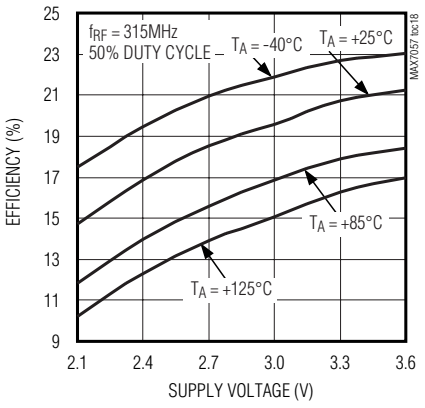
FREQUENCY STABILITY vs. SUPPLY VOLTAGE



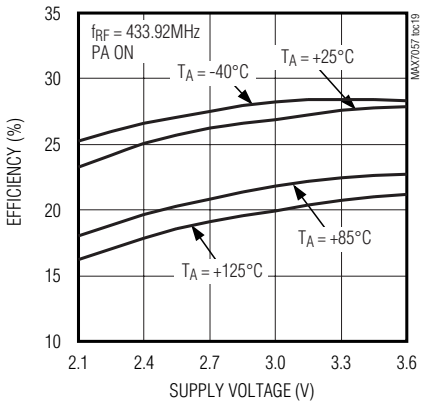
EFFICIENCY vs. SUPPLY VOLTAGE



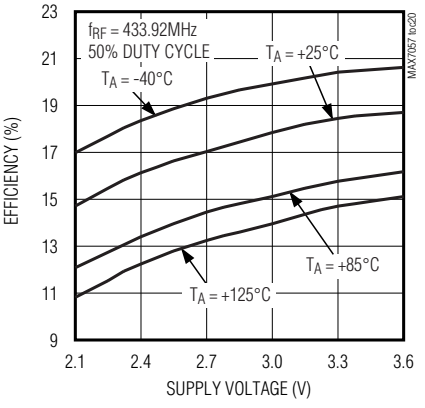
EFFICIENCY vs. SUPPLY VOLTAGE



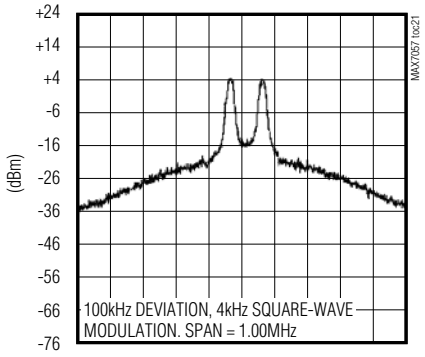
EFFICIENCY vs. SUPPLY VOLTAGE



EFFICIENCY vs. SUPPLY VOLTAGE



FSK SPECTRUM



300MHz to 450MHz Frequency-Programmable ASK/FSK Transmitter

Pin Description

PIN	NAME	FUNCTION
1	$\overline{CS}$	Serial Interface Active-Low Chip Select. Internally pulled up to DVDD.
2	SDI	Serial Interface Data Input. Internally pulled down to GND.
3	SCLK	Serial Interface Clock Input. Internally pulled down to GND.
4	PAGND	Power Amplifier Ground
5	PAOUT	Power Amplifier Output. Requires a pullup inductor to the supply voltage or ROUT. The pullup inductor can be part of the output-matching network.
6	ROUT	Envelope-Shaping Output. ROUT controls the power amplifier envelope's rise and fall times. Connect ROUT to the PA pullup inductor or to an optional power-adjust resistor. Bypass the inductor to GND as close as possible to the inductor with 680pF and 220pF capacitors.
7	PAVDD	Power Amplifier Supply Voltage. Bypass to ground with 0.01µF and 220pF capacitors placed as close as possible to the pin.
8	AVDD	Analog Positive Supply Voltage. Bypass to ground with 0.1µF and 0.01µF capacitors placed as close as possible to the pin.
9	XTAL2	Crystal Input 2. XTAL2 can be driven from an AC-coupled external reference.
10	XTAL1	Crystal Input 1. Bypass to ground if XTAL2 is driven from an AC-coupled external reference.
11	AGND	Analog Ground
12	ENABLE	Enable Pin. Drive high for normal operation; drive low or leave unconnected to put the device in standby mode. Internally pulled down to GND.
13	DIN	ASK/FSK Data Input. Use the control register (address: 0x00) to select the type of modulation. Internally pulled down to GND.
14	DGND	Digital Ground
15	GPO	General-Purpose Output. Can be configured to output various digital signals (SPI serial data output—SDO, CLKOUT—reference oscillator frequency divided by 1, 2, 4, or 8 for microprocessor clock, etc).
16	DVDD	Digital positive supply voltage. Bypass to ground with 0.1µF and 0.01µF capacitors placed as close as possible to the pin.

Detailed Description

The MAX7057 is frequency programmable from 300MHz to 450MHz, by using a fractional-N phase-locked loop (PLL), and transmits data using either ASK or FSK modulation. The MAX7057 has integrated tuning capacitors at the output of the power amplifier (PA) to ensure high-power efficiency at various programmable frequencies with a single-matching network.

The crystal-based architecture of the MAX7057 eliminates many of the common problems with SAW transmitters by providing greater modulation depth, faster frequency settling, tighter transmit frequency tolerance, and reduced temperature dependence. In particular, the tighter transmit frequency tolerance means that a superheterodyne receiver with a narrower IF bandwidth (therefore lower noise bandwidth) can be used. The payoff is better overall receiver performance when using a superheterodyne receiver such as the MAX1471, MAX1473, MAX7033, MAX7034, or MAX7042.

Frequency Programming

The MAX7057 is a crystal-referenced phased-locked loop (PLL) VHF/UHF transmitter that transmits data over the frequency range of 300MHz to 450MHz in ASK or FSK mode. The transmit frequency is set by the crystal frequency and the programmable divider in the PLL; the programmable-divide ratios can be set anywhere from 19 to 28, which means that with a crystal frequency of 16MHz, the output frequency range can be from 304MHz to 448MHz.

The fractional-N architecture of the PLL in the MAX7057 allows the FSK signal to be programmed for exact frequency deviations and rapid, transient-free frequency settling time. This modulation method completely elimi-

nates the problems associated with crystal-pulling FSK signal generation. The multiplying factor of the PLL is set by a 16-bit number, with 4 bits for integer and 12 bits for fraction. The 12-bit fraction in the synthesizer results in a tuning resolution that is equal to the reference frequency divided by 4096.

The MAX7057 has an internal variable shunt capacitor connected at the PA output. This capacitor is controlled using the SPI to maintain highly efficient transmission at any frequency within a 1.47 to 1 (28/19) tuning range. This means that it is possible to change the frequency and retune the antenna to the new frequency in a very short time. The combination of rapid-antenna tuning ability with rapid-synthesizer tuning makes the MAX7057 a true frequency-agile transmitter. The tuning capacitor has a resolution of 0.25pF. The MAX7057 also features adjustable output power through an external resistor to nearly +10dBm into a 50Ω load at +2.7V.

The MAX7057 supports data rates up to 100kbps NRZ in both ASK and FSK modes. In FSK mode, the frequency deviation can be programmed as low as ±2kHz and as high as ±100kHz.

Power Amplifier (PA)

The PA of the MAX7057 is a high-efficiency, open-drain switching-mode amplifier. In a switching-mode amplifier, the gate of the final-stage FET is driven with a very sharp 25% duty-cycle square wave at the transmit frequency. This square wave is derived from the synthesizer circuit. When the matching network is tuned correctly, the output FET resonates the attached matching circuit with a minimum amount of power dissipated in the FET. With a proper output-matching network, the PA can drive a wide range of antenna impedances, which include a small-loop PCB trace and a 50Ω antenna. The output-matching network suppresses the carrier harmonics and transforms the antenna impedance to an optimal impedance at PAOUT, which is from 125Ω to 250Ω.

When the output-matching network is properly tuned, the PA transmits power with a high overall efficiency of up to 25%. The efficiency of the PA itself is more than 39%. The output power can be adjusted by changing the impedance seen by the PA or by adjusting the value of an external resistor at PAOUT.

Envelope Shaping

The MAX7057 features an internal envelope-shaping resistor for ASK modulation, which connects between PAVDD and ROUT. When connected to the PA pullup inductor, the envelope-shaping resistor slows the turn-on/-off time of the PA and results in a smaller spectral width of the modulated PA output signal.

Variable Capacitor

The MAX7057 has a set of internal variable shunt capacitors that can be switched in and out to present different capacitor values at the PA output. The capacitors are connected from the PA output to ground. This allows changing the tuning network along with the synthesizer divide ratio each time the transmitted frequency changes, making it possible to maintain maximum transmitter power while moving rapidly from one frequency to another.

When the particular capacitance control bit is high, the corresponding amount of shunt capacitance is added at PAOUT. The 32 capacitor values are selected using the SPI; the capacitance resolution is 0.25pF. The total capacitance can vary from 0 to 7.75pF. For example, if cap[1] and cap[3] are high, and cap[4], cap[2], and cap[0] are low, this circuit will add 2.5pF at PAOUT. See Table 1 for variable capacitor values and control bits.

Fractional-N Phase-Locked Loop (PLL)

The MAX7057 utilizes a fully integrated fractional-N PLL for its transmit frequency synthesizer. All PLL components, including the loop filter, are included on-chip. The loop bandwidth is programmable to either 300kHz or 600kHz. See Tables 2, 3, and 4 for “pllbw” bit description. The 16-bit fractional-N topology allows the transmit frequency to be adjusted in increments of $f_{XTAL}/4096$. The allowable range of the f_{RF}/f_{XTAL} ratio is approximately 19 to 28.

The fractional-N topology also allows exact FSK frequency deviations to be programmed, completely eliminating the problems associated with generating frequency deviations by crystal oscillator pulling.

The integer and fractional portions of the PLL divider ratio set the transmit frequency. The following example shows how to determine the correct values to be loaded to registers HIFREQ1, HIFREQ0, LOFREQ1, and LOFREQ0. See Tables 2, 3, and 7–10 for a detailed description of these registers.

Table 1. Variable Capacitor Values and Control Bits

SPI REGISTER BITS	INCREMENTAL SHUNT CAPACITANCE (pF)
cap[0]	0.25
cap[1]	0.5
cap[2]	1.0
cap[3]	2.0
cap[4]	4.0

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Due to the nature of the transmit PLL frequency divider, a fixed offset of 16 must be subtracted from the transmit PLL divider ratio for programming the MAX7057's transmit frequency registers. To determine the value to program the MAX7057's transmit frequency registers, convert the decimal value of the following equation to the nearest hexadecimal value:

$$\left(\frac{f_{RF}}{f_{XTAL}} - 16\right) \times 4096 = \text{Decimal value to program transmit frequency registers}$$

Assume that the ASK transmit frequency = 315MHz and f_{XTAL} = 16MHz. In this example, the rounded decimal value is 15,104, or 0x3B00 hexadecimal. The upper 2 bytes (0x3B) are loaded into the LOFREQ1 register, and the low 2 bytes (0x00) are loaded into the LOFREQ0 register. In ASK mode, the transmit frequency equals the lower frequency programmed into the MAX7057's transmit frequency registers (see Tables 2, 3, and 9–12).

In FSK mode, the transmit frequencies equal the upper (HIFREQ1 and HIFREQ0) and lower (LOFREQ1 and LOFREQ0) frequencies programmed into the MAX7057's transmit frequency registers. Calculate the upper and lower frequency in the same way as shown above. FSK deviations as low as ±2kHz and as high as ±100kHz are programmable (see Tables 2, 3, and 8–12).

The exact min and max values for the transmit frequency registers (HIFREQ1/0, LOFREQ1/0) are 2.9596 (0x2F42) and 12.0220 (0xC05A), yielding a synthesizer ratio of 18.9596 and 28.0220, respectively. These limits **MUST** be followed to prevent the delta-sigma modulator from overflowing.

Whenever all of the fractional bits in the HIFREQ1/0 and LOFREQ1/0 registers are zero (fhi[11:0] and flo[11:0]), only an integer divider is used, and the delta-sigma modulator is not in operation. This allows lower current operation. The 600kHz PLL bandwidth should be used in this mode to reduce phase noise.

Any change to the transmit frequency registers must be followed by writing a "1" to the self-reset frequency load register (see Tables 2, 3, and 12).

Crystal (XTAL) Oscillator

The crystal (XTAL) oscillator in the MAX7057 is designed to present a capacitance of approximately 6pF between XTAL1 and XTAL2. In most cases, this corresponds to an 8pF load capacitance applied to the external crystal when typical PCB parasitics are added. The MAX7057 is designed to operate with a typical 10pF load capacitance crystal. **It is very important to use a crystal with a load capacitance that is equal to the capacitance of the MAX7057 crystal oscillator plus PCB parasitics and optional external load capacitors.** If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its stated operating frequency, introducing an error in the reference frequency. A crystal designed to operate at a higher load capacitance than the value specified for the oscillator is always pulled higher in frequency. Adding capacitance to increase the load capacitance on the crystal increases the start-up time and can prevent oscillation altogether.

In actuality, the oscillator pulls every crystal. The crystal's natural frequency is below its specified frequency, but when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance.

Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_p = \frac{C_m}{2}\left(\frac{1}{C_{case} + C_{load}} - \frac{1}{C_{case} + C_{spec}}\right) \times 10^6$$

where:

fp is the amount the crystal frequency is pulled in ppm
C_m is the motional capacitance of the crystal
C_{case} is the case capacitance
C_{spec} is the specified load capacitance
C_{load} is the actual load capacitance

When the crystal is loaded as specified (i.e., $C_{load} = C_{spec}$), the frequency pulling equals zero.

Communication Protocol

The MAX7057 registers are programmed through an SPI interface. Figure 2 shows the timing diagram of the SPI. The GPO must be properly configured to act as an SPI data output (SDO) by setting the configuration 1 register (see Tables 2, 3, 15, and 16).

The SPI operates on a byte format, according to Figure 2.

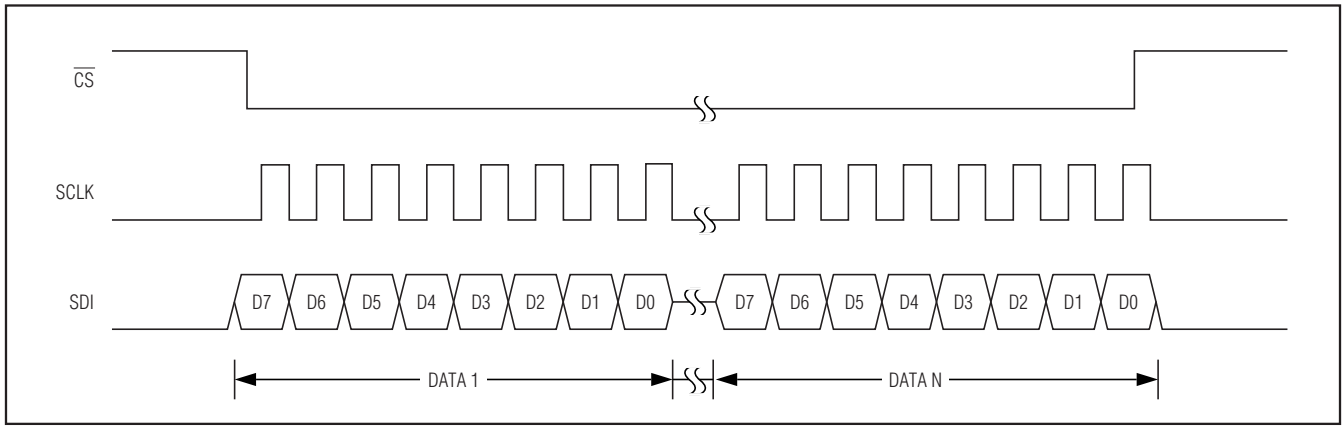


Figure 2. SPI Format

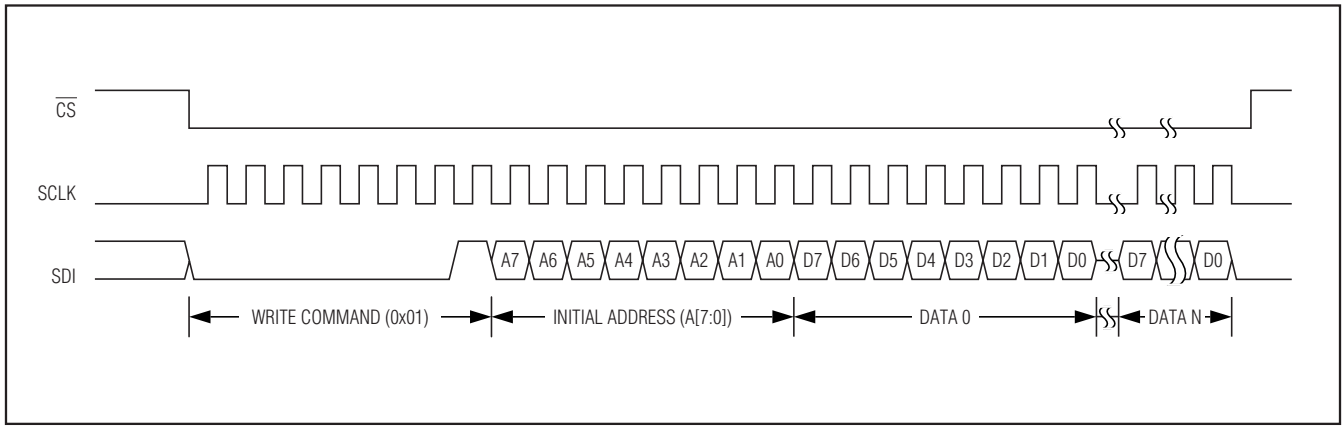


Figure 3. SPI Write Command Format

Depending on the command, byte 1 through byte N may assume different functions. They may either be a direct command (write, read, read all, reset), or an address or data contents. The commands available in the MAX7057 SPI are described in detail below:

Write: The write command (0x01) is used to program the MAX7057 registers (see Tables 2 and 3). The format shown in Figure 3 must be followed, allowing all the registers to be programmed within one $\overline{CS}$ cycle.

Using a byte descriptive notation, the write command can be viewed as the following sequence:

SDI: <0x01> <Initial Address> <Data 0> <Data 1> … <Data N>

Data 0 is then written to the register addressed by <Initial Address>, Data 1 is written to <Initial Address + 1>, and so on.

Read: To execute an SPI read operation, the general-purpose output (GPO) pin must be configured to either a CKOUT_SDO or SDO function (see Tables 15 and 16 for details).

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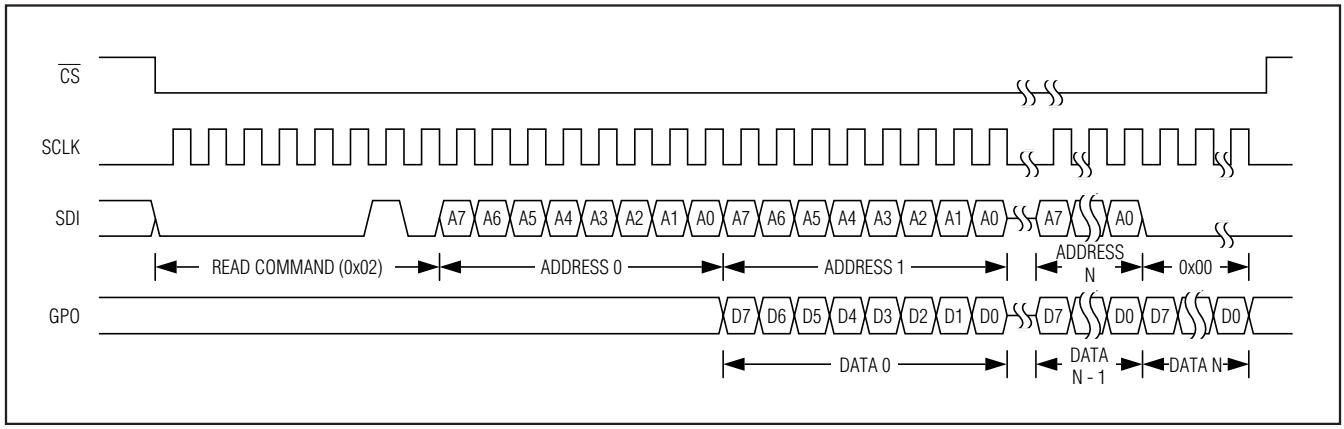


Figure 4. SPI Read Command Format

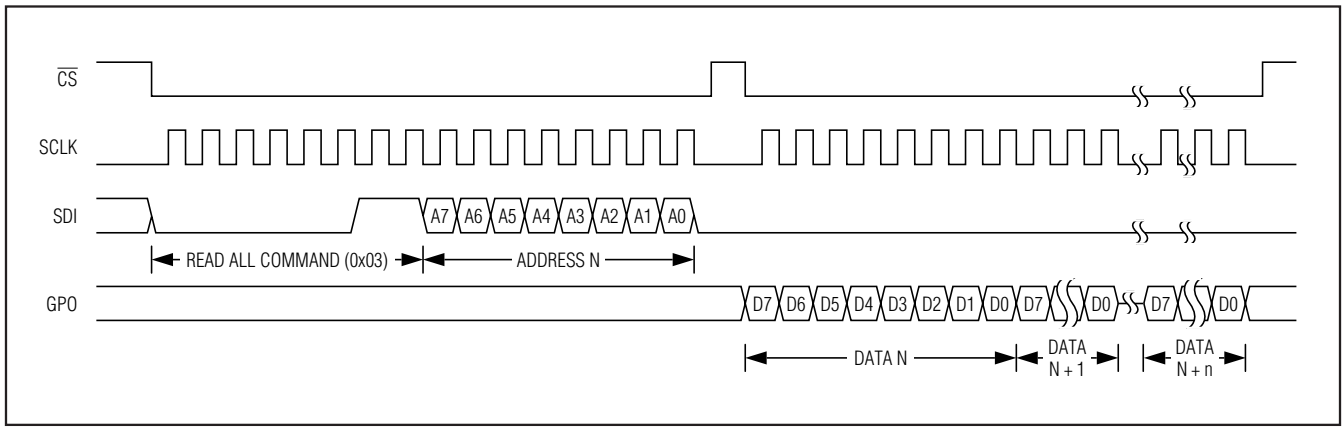


Figure 5. SPI Read-All Command Format

Using a byte descriptive notation, the read command can be viewed as the following sequence, within the same $\overline{CS}$ cycle:

SDI : <0x02> <Address 0> <Address 1> <Address2> … < Address N > < 0x00 >
GPO: < XX > < XX > < Data 0 > < Data 1 > … < Data N - 1 > <Data N>

With this command, all the registers can be read within the same cycle of $\overline{CS}$. The addresses can be given in any order.

Read-All: To execute an SPI read-all operation, GPO must be configured to either a CKOUT_SDO or SDO function (see Tables 15 and 17 for details).

Using a byte descriptive notation, the read command can be viewed as the following sequence, within two $\overline{CS}$ cycles:

	$\overline{CS}$ cycle 1	$\overline{CS}$ cycle 2
SDI :	<0x03> <Address N>	< XX > < XX > < XX >…< XX >
GPO:		<Data N> <DataN + 1> <DataN + 2>…<Data N + n>

Reset: The MAX7057 can be reset to its power-up state through the reset command.

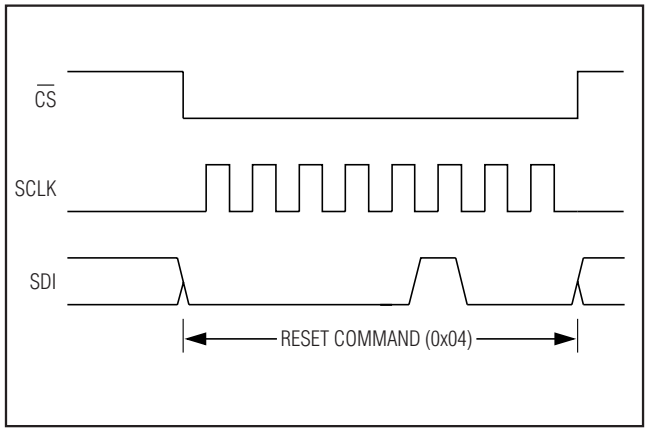


Figure 6. Reset Command Format

Using a byte descriptive notation, the reset command can be viewed as the following sequence, within the same $\overline{CS}$ cycle:

SDI: <0x04>

Features and Settings

Values and parameters are set through registers in the MAX7057 that are addressable through the SPI. These registers contain bits that either turn functions on and off or program numerical settings. The following settings are controlled through the SPI.

Variable Capacitor

The internal variable shunt capacitor, which is instrumental in matching the PA to the antenna, is controlled by setting 5 bits in the configuration 0 register. This allows for 32 levels of shunt capacitance control. Since the control of these 5 bits is independent of the other settings, any capacitance value can be chosen at any frequency, making it possible to maintain maximum transmitter efficiency while moving rapidly from one frequency to another.

Clock Output

The MAX7057 has a buffered clock output that can serve as a clock for a microprocessor. The divide ratio is set through the configuration 0 register (see Tables 5 and 6). The divide settings are 1 (no division), 2, 4, 8, or 16; the original undivided frequency is based on the reference frequency generated by the external crystal. The buffered clock output is available at GPO when enabled by setting the configuration 1 register (see Tables 2, 3, 15, and 16).

Mode Select and Crystal Shutdown

The transmission mode is selected by writing to a register. The default mode is ASK and the mode can be changed to FSK by writing a 1 to the mode bit in the control register. This register is also used to keep the crystal circuit powered up in the shutdown mode.

Registers

The following tables provide information on the MAX7057 registers.

Table 2. Register Summary

ADDRESS	REGISTER NAME	DESCRIPTION
0x00	CONTRL	Control register. Controls the mode (ASK/FSK), crystal clock output, envelope-shaping, PLL bandwidth, and SPI enable.
0x01	CONFIG0	Configuration 0 register. Controls the capacitance at the PA output and clock output frequency divider.
0x02	HIFREQ1	High-frequency 1 register (upper byte). Sets the high frequency in FSK transmission.
0x03	HIFREQ0	High-frequency 0 register (lower byte). Sets the high frequency in FSK transmission.
0x04	LOFREQ1	Low-frequency 1 register (upper byte). Sets the low frequency in FSK transmission, or carrier frequency in ASK transmission.
0x05	LOFREQ0	Low-frequency 0 register (lower byte). Sets the low frequency in FSK transmission, or carrier frequency in ASK transmission.
0x06	FLOAD	Frequency load register. Performs the frequency load function.
0x07	DATAIN	Data in register. SPI equivalent of DIN pin.
0x08	EN	Enable register. SPI equivalent of ENABLE pin.
0x09	CONFIG1	Configuration 1 register. GPO selector.
0x0C	STATUS	Status register.

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Table 3. Register Configuration

NAME	ADDRESS	DATA								
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	MODE
CONTRL	0x00	0	0	spioffsht	pllbw	shape	ckouts	ckouton	mode	R/W
CONFIG0	0x01	ckdiv[2]	ckdiv[1]	ckdiv[0]	cap[4]	cap[3]	cap[2]	cap[1]	cap[0]	R/W
HIFREQ1	0x02	fhi[15]	fhi[14]	fhi[13]	fhi[12]	fhi[11]	fhi[10]	fhi[9]	fhi[8]	R/W
HIFREQ0	0x03	fhi[7]	fhi[6]	fhi[5]	fhi[4]	fhi[3]	fhi[2]	fhi[1]	fhi[0]	R/W
LOFREQ1	0x04	flo[15]	flo[14]	flo[13]	flo[12]	flo[11]	flo[10]	flo[9]	flo[8]	R/W
LOFREQ0	0x05	flo[7]	flo[6]	flo[5]	flo[4]	flo[3]	flo[2]	flo[1]	flo[0]	R/W
FLOAD	0x06	—	—	—	—	—	—	—	fload	R/W
DATAIN	0x07	—	—	—	—	—	—	—	datain_bit	R/W
EN	0x08	—	—	—	—	—	—	—	enable_bit	R/W
CONFIG1	0x09	0	0	0	0	0	gposel[2]	gposel[1]	gposel[0]	R/W
STATUS	0x0C	fhi/lo[15]	fhi/lo[14]	fhi/lo[13]	fhi/lo[12]	X	0	TxREADY	NoXTAL	R

Table 4. Control Register (Address: 0x00)

BIT	NAME	FUNCTION
0	mode	ASK(0) or FSK(1)
1	ckouton	Crystal clock output enable(1) on GPO output
2	ckouts	Crystal clock output enable(1) while part is in shutdown mode
3	shape	Disable(0) or enable(1) transmitter envelope-shaping resistor
4	pllbw	PLL bandwidth setting, low(0) = 300kHz or high(1) = 600kHz; 300kHz is recommended for fractional-N and 600kHz for fixed-N
5	spioffsht	Enable(0) or disable(1) SPI communication during shutdown

Table 5. Configuration 0 Register (Address: 0x01)

BIT	NAME	FUNCTION
4-0	cap[4:0]	5-bit capacitor setting
7-5	ckdiv[2:0]	3-bit clock output frequency divider

Table 6. ckdiv[2:0] of Configuration 0 Register (Address: 0x01)

DECIMAL	BINARY	CRYSTAL FREQUENCY DIVIDED BY
0	000	1
1	001	2
2	010	4
3	011	8
4-7	1XX	16

Table 7. High-Frequency 1 Register (Address: 0x02)

BIT	NAME	FUNCTION
7-0	fhi[15:8]	8-bit upper byte of high-frequency divider for FSK

The 4 MSBs of HIFREQ1 (fhi[15:12]) are the integer portion of the divider, excluding offset of 16. The 12 LSBs (fhi[11:0]) are the fractional part of the divider.

Table 8. High-Frequency 0 Register (Address: 0x03)

BIT	NAME	FUNCTION
7-0	fhi[7:0]	8-bit lower byte of high-frequency divider for FSK

Table 9. Low-Frequency 1 Register (Address: 0x04)

BIT	NAME	FUNCTION
7-0	flo[15:8]	8-bit upper byte of low-frequency divider for FSK/ASK

The 4 MSBs of LOFREQ1 (flo[15:12]) are the integer portion of the divider, excluding offset of 16. The 12 LSBs (flo[11:0]) are the fractional part of the divider.

Valid values for the divider are shown in Table 11.

Table 10. Low-Frequency 0 Register (Address: 0x05)

BIT	NAME	FUNCTION
7-0	flo[7:0]	8-bit lower byte of low-frequency divider for FSK/ASK

Table 11. Maximum and Minimum Values for Frequency Divide

DECIMAL VALUE	fhi[15:12], flo[15:12]	fhi[11:0], flo[11:0]
12.0220	0xC	0x05A
2.9536	0x2	0xF42

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These values are internally summed with 16, and thus, the min and max divider becomes approximately 19 and 28. These limits **MUST** be followed, to prevent the delta-sigma number generator from overflowing.

Whenever all of the fhi[11:0] and flo[11:0] are zero, only an integer divider is used, and the delta-sigma modulator is not in operation. This allows lower current operation. The 600kHz PLL bandwidth could be used in this mode to reduce phase noise.

Table 12. Frequency Load Register (Address: 0x06)

BIT	NAME	FUNCTION
0	fload	Effectively changes the PLL frequency to the ones written in registers 2–5. This is a self-reset bit, and is reset to zero after the operation is completed.

Table 13. Data In Register (Address: 0x07)

BIT	NAME	FUNCTION
0	datain_bit	SPI equivalent of DIN, where the transmitted data can be controlled through the SPI interface. It should be kept low (0) if only the external DIN pin is used. The external DIN pin should also be kept low (0) if the SPI datain_bit is used.

Table 14. Enable Register (Address: 0x08)

BIT	NAME	FUNCTION
0	enable_bit	SPI equivalent of ENABLE. It should be kept low (0) if the external ENABLE pin is used. The external ENABLE pin should also be kept low (0) if the SPI enable_bit is used.

Table 15. Configuration 1 Register (Address: 0x09)

BIT	NAME	FUNCTION
2-0	gposel[2:0]	3-bit GPO selector
7-3	RESERVED “0”	RESERVED. Set to 0 for normal operation.

Table 16. General-Purpose Output Selector (gposel[2:0]) for Configuration 1 Register

DECIMAL	BINARY	GPO	DESCRIPTION
0	000	CKOUT_SDO	Clock/SDO Output. Outputs clock when $\overline{CS}$ is high and clock output is enabled; outputs SDO when $\overline{CS}$ is low.
1	001	SDO	SPI Serial Data Output (SDO)
2	010	CKOUT	Clock Output
3	011	RESERVED	RESERVED
4	100	RESERVED	RESERVED
5	101	NoXTAL	Internal Crystal Oscillator Status. High means oscillator is NOT in operation.
6	110	TxREADY	Transmitter Ready Status. High means PLL is locked and MAX7057 is ready to transmit data.
7	111	datain_bit	A copy of datain_bit

Table 17. Status Register (Address: 0x0C)

BIT	NAME	FUNCTION
0	NoXTAL	Internal Crystal Oscillator Status. High means oscillator is not in operation.
1	TxREADY	Transmitter Ready Status. High means PLL is locked and MAX7057 is ready to transmit data.
2	RESERVED "0"	RESERVED. Set to 0 for normal operation.
3	X	RESERVED
7-4	fhi/lo[15]–fhi/lo[12]	ASK mode: Outputs flo[15:12]. FSK mode: when datain pin/bit is high, outputs fhi[15:12]; when datain pin/bit is low, outputs flo[15:12].

Applications Information

Output Matching to 50Ω

When matched to a 50Ω system, the MAX7057's PA is capable of delivering +9.2dBm of output power at PAVDD = +2.7V with a broadband match. The output of the PA is an open-drain transistor, which has internal selectable shunt tuning capacitors (see the *Variable Capacitor* section) for impedance matching. It is connected to PAVDD or ROUT through a pullup inductor for proper biasing. The internal selectable shunt capacitors make it easy for tuning when changing the output frequency. The pullup inductor from the PA to PAVDD or ROUT serves three main purposes: resonating the capacitive PA output, providing biasing for the PA, and acting as a high-frequency choke to prevent RF energy from coupling onto the supply voltage. The pi network between the PA output and the antenna also forms a lowpass filter that provides attenuation for the higher-order harmonics.

Output Matching to PCB Loop Antenna

In many applications, the MAX7057 must be impedance-matched to a small-loop antenna. The antenna is usually fabricated out of a copper trace on a PCB in a rectangular, circular, or square pattern. The antenna has an impedance that consists of a lossy component and a radiative component. To achieve high radiating efficiency, the radiative component should be as high as possible, while minimizing the lossy component. In addition, a loop antenna has an inherent loop inductance associated with it (assuming the antenna is terminated to ground). In a typical application, the inductance of the loop antenna is approximately 50nH to 100nH. The radiative and lossy impedances can be anywhere from a few tenths of an ohm to 5Ω or 10Ω.

Layout Considerations

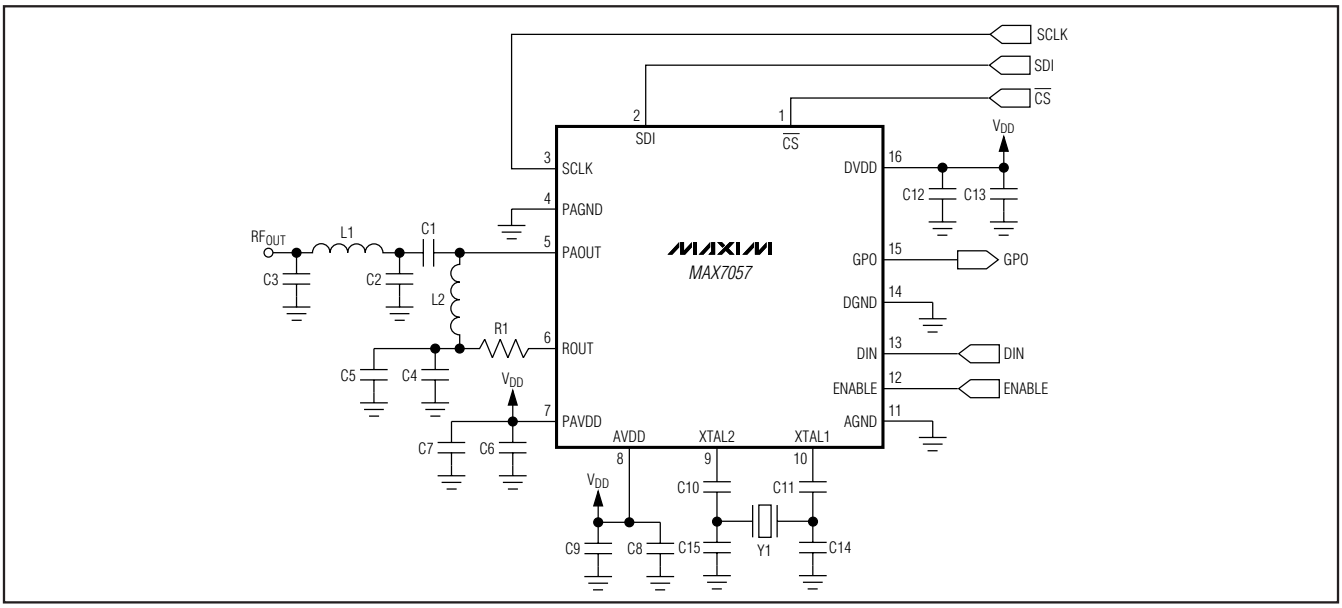
A properly designed PCB is an essential part of any RF/microwave circuit. At high-frequency inputs and outputs, use controlled-impedance lines and keep them as short as possible to minimize losses and radiation. At high frequencies, trace lengths that are in the order of λ/10 or longer act as antennas, where λ is the wavelength.

Keeping the traces short also reduces parasitic inductance. Generally, 1in of PCB trace adds about 20nH of parasitic inductance. The parasitic inductance can have a dramatic effect on the effective inductance of a passive component. For example, a 0.5in trace connecting to a 100nH inductor adds an extra 10nH of inductance, or 10%.

To reduce parasitic inductance, use wider traces and a solid ground or power plane below the signal traces. Using a solid ground plane can reduce the parasitic inductance from approximately 20nH/in to 7nH/in. Also, use low-inductance connections to the ground plane, and place decoupling capacitors as close as possible to all V_{DD} pins.

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Typical Application Circuit

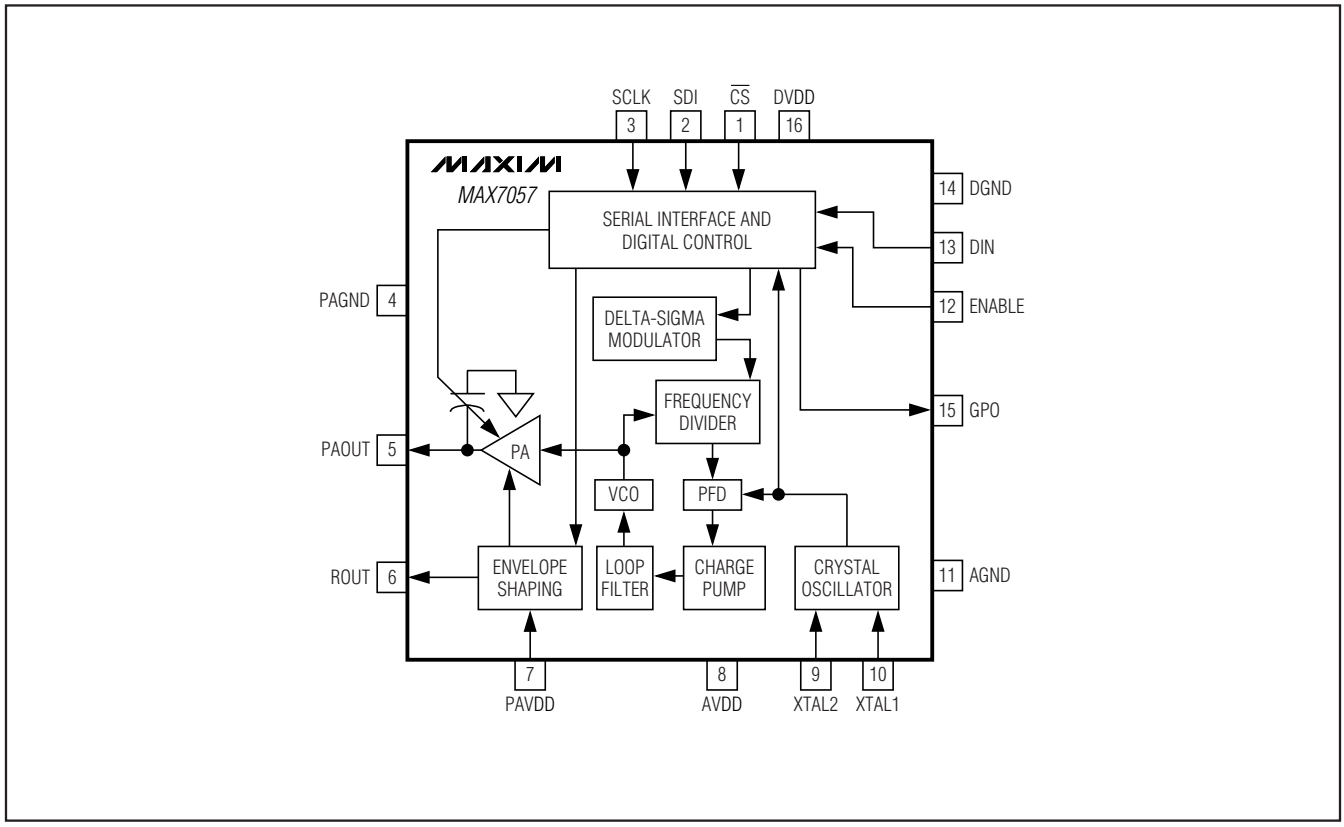


Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2	1	10pF ±5%, 50V C0G ceramic capacitor (0603) Murata GRM1885C1H100J
C3	1	6.8pF ±5%, 50V C0G ceramic capacitor (0603) Murata GRM1885C1H6R8J
C4, C7	2	220pF ±5%, 50V C0G ceramic capacitors (0603) Murata GRM1885C1H221J
C5	1	680pF ±5%, 50V C0G ceramic capacitor (0603) Murata GRM1885C1H681J
C6, C9, C12	3	10nF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H103K
C8, C13	2	100nF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H104K
C10, C11	2	100pF ±5%, 50V C0G ceramic capacitors (0603) Murata GRM1885C1H101J
C14, C15	2	4pF ±5%, 50V C0G ceramic capacitors (0603) Murata GRM1885C1H4R0C
L1	1	22nH ±5% wire-wound inductor (0603) Murata LQW18AN22NJ00
L2	1	13nH ±5% wire-wound inductor (0603) Murata LQW18AN13NJ00
R1	1	0Ω resistor (0603)
Y1	1	16MHz crystal, Crystek 17466, Suntsu SCX284

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Functional Diagram



Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 SO	S16+3	21-0041

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