DATA SHEET



SAA8112HL
Digital camera signal processor and microcontroller

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PHILIPS

CONTENTS

1 FEATURES
2 APPLICATIONS
3 GENERAL DESCRIPTION
4 QUICK REFERENCE DATA
5 ORDERING INFORMATION
6 BLOCK DIAGRAM
7 PINNING
8 FUNCTIONAL DESCRIPTION
8.1 Synchronization and video windows
8.2 Optical black processing
8.3 Colour extractor
8.4 Colour matrix
8.4.1 RGB processing
8.5 YUV processing
8.5.1 Y processing
8.5.2 UV processing
8.6 Output formatter
8.7 Measurement Engine
8.8 Display features
8.9 Microcontroller
8.10 Mode control
8.11 SNERT (UART) interface - DSP registers
9 LIMITING VALUES
10 THERMAL CHARACTERISTICS
11 OPERATING CHARACTERISTICS
12 ELECTRICAL CHARACTERISTICS
13 APPLICATION INFORMATION
14 PACKAGE OUTLINE
15 SOLDERING
15.1 Introduction to soldering surface mount packages
15.2 Reflow soldering
15.3 Wave soldering
15.4 Manual soldering
15.5 Suitability of surface mount IC packages for wave and reflow soldering methods
16 DEFINITIONS
17 LIFE SUPPORT APPLICATIONS
18 PURCHASE OF PHILIPS I^2C COMPONENTS

Digital camera signal processor and microcontroller

SAA8112HL

1 FEATURES

- High precision digital processing with 8- to 10-bit input
- Embedded microcontroller (80C51 core based) for control loops Auto Optical Black (AOB), Auto White Balance (AWB) and Auto Exposure (AE)
- Supports a large number of sensors
- RGB Bayer or mosaic (yellow, magenta, green and cyan) colour processing
- Black and white processing without loss of resolution
- Compatible with interlaced or progressive modes
- Processes up to 800 active pixels per line
- Optical black processing
- Programmable colour matrix
- Programmable R, G and B offsets
- Programmable Knee and Gamma correction
- Programmable edge enhancement
- False colour detection and correction
- Y and UV adjustable coring filters
- Flexible Measurement Engine (ME) with up to 16 measurements per frame in 16 programmable windows
- Programmable measurement conditions on Y, U and V
- 8-bit YUV output with selectable formats:
  - YUV 4 : 2 : 2 CCIR656 with signal embedded synchronization codes (SAV/EAV)
  - Selectable YUV output format 4 : 0 : 0, 4 : 1 : 1, 4 : 2 : 2 and 4 : 4 : 4 (according to IEEE-1394 based digital camera specification)
  - Basic output window cutter and scaler.
- Programmable output clock for switched mode power supply
- 3-wire/13-bit interface for control of the TDA878X family (CDS + AGS + 10-bit ADC).

2 APPLICATIONS

- PC camera
- Videophone
- Security camera
- Camcorder.

3 GENERAL DESCRIPTION

The SAA8112HL is a powerful and versatile 10-bit digital processor for video cameras. It processes the digitized sensor data and converts it to a high quality, multi-format and YUV digital signal. In addition, the SAA8112HL performs programmable statistical measurements on the video stream allowing, for instance, a precise measurement of the exposure or the white balance levels.

An 80C51 microcontroller derivative with five I/O ports, I^2C-bus, 512 bytes of RAM and 32 kbytes of program memory is also embedded in the SAA8112HL.
The microcontroller is used in combination with the Digital Signal Processing (DSP) measurement capabilities to provide advanced AE, AWB and AOB. The microcontroller may also be used to control other devices in the camera, for example a USB or a 1394 interface.

In the following description of the SAA8112HL, four main functional blocks are given (see Fig.1):

- The DSP block
- The DSP ME block
- The microcontroller block
- The timing, interface and miscellaneous functions block.

4 QUICK REFERENCE DATA

Measured over full voltage and temperature range: V_{DDD} = 3.3 V ±10%; T_{amb} = 0 to 70 °C; unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
$I_{DDD(tot)}$	total supply current	V_{DDD} = 3.6 V T_{amb} = 70 °C	–	–	80	mA
V_I	input voltage	3.0 V < V_{DDD} < 3.6 V	low voltage TTL compatible			V
V_O	output voltage	3.0 V < V_{DDD} < 3.6 V	low voltage TTL compatible			V
$f_{clk(px)}$	pixel frequency		0	14.18	25	MHz
$f_{clk(\mu c)}$	microcontroller clock frequency		0	12	–	MHz
P_{tot}	total power dissipation	V_{DDD} = 3.6 V T_{amb} = 70 °C	–	–	288	mW
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	ambient temperature		0	25	70	°C
T_j	junction temperature	T_{amb} = 70 °C	–	–	125	°C

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA8112HL	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

6 BLOCK DIAGRAM

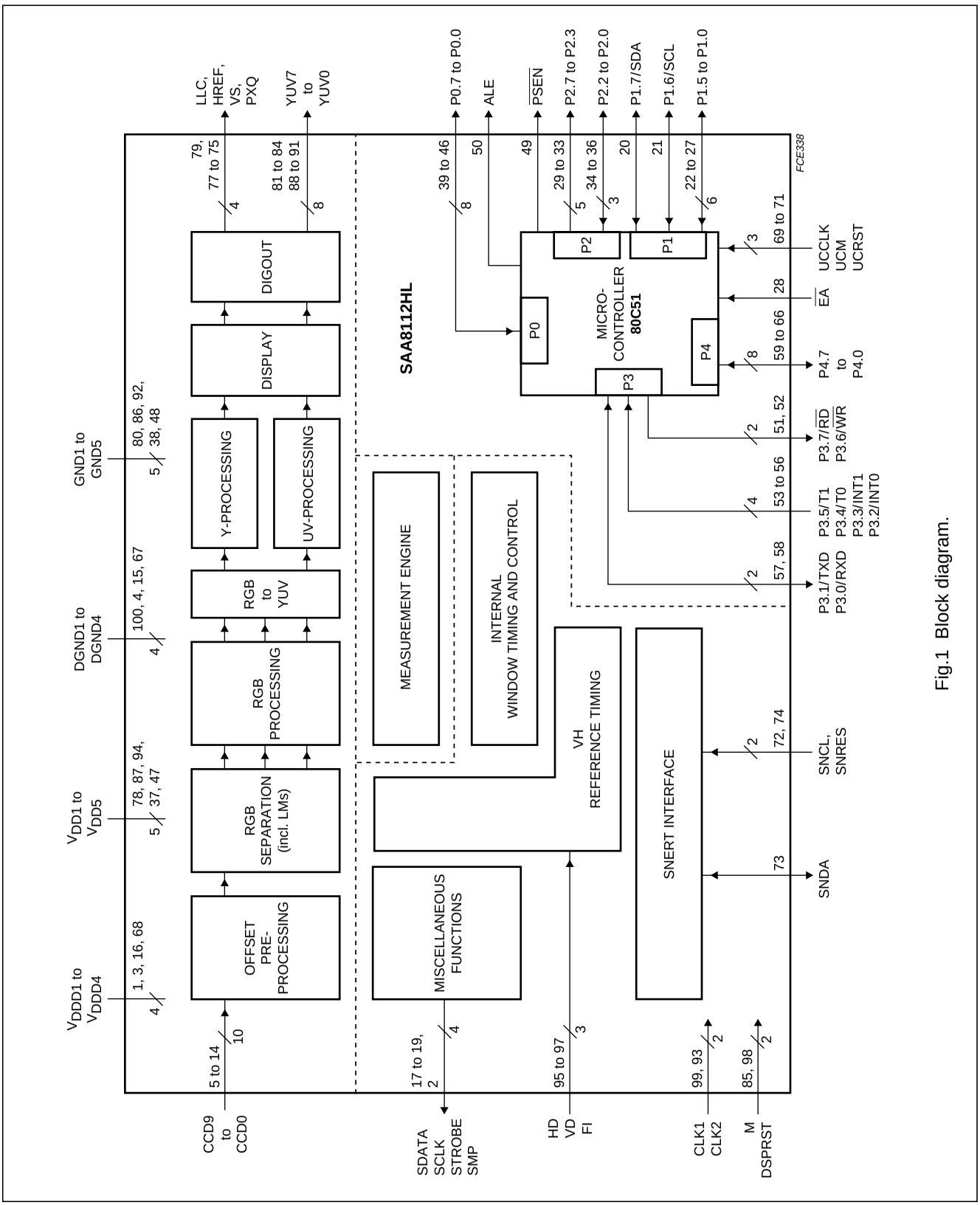


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
V_{DDD1}	1	P	digital supply voltage 1 for the DSP core (switchable supply domain)
SMP	2	O	switched mode pulse for DC-to-DC power supply
V_{DDD2}	3	P	digital supply voltage 2 for input buffers and predrivers
DGND2	4	P	digital ground 2 for input buffers and predrivers and for the digital core
CCD9	5	I	(preprocessed) AD-converted CCD; bit 9
CCD8	6	I	(preprocessed) AD-converted CCD; bit 8
CCD7	7	I	(preprocessed) AD-converted CCD; bit 7
CCD6	8	I	(preprocessed) AD-converted CCD; bit 6
CCD5	9	I	(preprocessed) AD-converted CCD; bit 5
CCD4	10	I	(preprocessed) AD-converted CCD; bit 4
CCD3	11	I	(preprocessed) AD-converted CCD; bit 3
CCD2	12	I	(preprocessed) AD-converted CCD; bit 2
CCD1	13	I	(preprocessed) AD-converted CCD; bit 1
CCD0	14	I	(preprocessed) AD-converted CCD; bit 0
DGND3	15	P	digital ground 3 for input buffers and predrivers and for the digital core
V_{DDD3}	16	P	digital supply voltage 3 for input buffers and predrivers and for the 80C51 core
SCLK	17	O	serial clock output to preprocessor
SDATA	18	O	serial data output to preprocessor
STROBE	19	O	strobe signal to preprocessor
P1.7/SDA	20	I/O	Port 1 bidirectional; bit 7/slave I^2C-bus data I/O
P1.6/SCL	21	I/O	Port 1 bidirectional; bit 6/slave I^2C-bus clock input
P1.5	22	I/O	Port 1 bidirectional; bit 5
P1.4	23	I/O	Port 1 bidirectional; bit 4
P1.3	24	I/O	Port 1 bidirectional; bit 3
P1.2	25	I/O	Port 1 bidirectional; bit 2
P1.1	26	I/O	Port 1 bidirectional; bit 1
P1.0	27	I/O	Port 1 bidirectional; bit 0
$\overline{EA}$	28	I	external access select - internal or external program memory (active LOW)
P2.7	29	O	Port 2 output; bit 7
P2.6	30	O	Port 2 output; bit 6
P2.5	31	O	Port 2 output; bit 5
P2.4	32	O	Port 2 output; bit 4
P2.3	33	O	Port 2 output; bit 3
P2.2	34	I/O	Port 2 bidirectional; bit 2
P2.1	35	I/O	Port 2 bidirectional; bit 1
P2.0	36	I/O	Port 2 bidirectional; bit 0
V_{DD4}	37	P	supply voltage 4 for output buffers
GND4	38	P	ground 4 for output buffers
P0.7	39	I/O	Port 0 bidirectional; bit 7
P0.6	40	I/O	Port 0 bidirectional; bit 6

SYMBOL	PIN	I/O	DESCRIPTION
P0.5	41	I/O	Port 0 bidirectional; bit 5
P0.4	42	I/O	Port 0 bidirectional; bit 4
P0.3	43	I/O	Port 0 bidirectional; bit 3
P0.2	44	I/O	Port 0 bidirectional; bit 2
P0.1	45	I/O	Port 0 bidirectional; bit 1
P0.0	46	I/O	Port 0 bidirectional; bit 0
V_{DD5}	47	P	supply voltage 5 for output buffers
GND5	48	P	ground 5 for output buffers
$\overline{PSEN}$	49	O	program store enable output for external memory (active LOW)
ALE	50	O	address latch enable output for external latch
P3.7/$\overline{RD}$	51	O	Port 3 output; bit 7/external data memory read output (active LOW)
P3.6/$\overline{WR}$	52	O	Port 3 output; bit 6/external data memory write output (active LOW)
P3.5/T1	53	I	Port 3 input; bit 5/Timer 1 external input
P3.4/T0	54	I	Port 3 input; bit 4/Timer 0 external input
P3.3/INT1	55	I	Port 3 input; bit 3/external interrupt 1
P3.2/INT0	56	I	Port 3 input; bit 2/external interrupt 0
P3.1/TXD	57	I/O	Port 3 input; bit 1/serial output port (UART)
P3.0/RXD	58	I/O	Port 3 input; bit 0/serial input port (UART)
P4.7	59	I/O	Port 4 bidirectional; bit 7
P4.6	60	I/O	Port 4 bidirectional; bit 6
P4.5	61	I/O	Port 4 bidirectional; bit 5
P4.4	62	I/O	Port 4 bidirectional; bit 4
P4.3	63	I/O	Port 4 bidirectional; bit 3
P4.2	64	I/O	Port 4 bidirectional; bit 2
P4.1	65	I/O	Port 4 bidirectional; bit 1
P4.0	66	I/O	Port 4 bidirectional; bit 0
DGND4	67	P	digital ground 4 for input buffers and predrivers and to the digital core
V_{DDD4}	68	P	digital voltage 4 for input buffers and predrivers and to the digital core
UCCLK	69	I	clock for internal 80C51
UCM	70	I	(test) mode control signal for internal 80C51
UCRST	71	I	Power-on reset for internal 80C51
SNCL	72	I	clock for DSP-SNERT interface (UART mode 0)
SNDA	73	I/O	data I/O for DSP-SNERT interface (UART mode 0)
SNRES	74	I	reset for DSP-SNERT interface (UART mode 0)
PXQ	75	O	pixel qualifier output for YUV-port
VS	76	O	vertical synchronization output for YUV-port
HREF	77	O	horizontal reference output for YUV-port
V_{DD1}	78	P	supply voltage 1 for output buffers
LLC	79	O	line-locked clock (delayed CLK2) for YUV-port
GND1	80	P	ground 1 for output buffers
YUV7	81	O	multiplexed YUV; bit 7

SYMBOL	PIN	I/O	DESCRIPTION
YUV6	82	O	multiplexed YUV; bit 6
YUV5	83	O	multiplexed YUV; bit 5
YUV4	84	O	multiplexed YUV; bit 4
M	85	I	(test) mode control signal for DSP core
GND2	86	P	ground 2 for output buffers
V_{DD2}	87	P	supply voltage 2 for output buffers
YUV3	88	O	multiplexed YUV; bit 3
YUV2	89	O	multiplexed YUV; bit 2
YUV1	90	O	multiplexed YUV; bit 1
YUV0	91	O	multiplexed YUV; bit 0
GND3	92	P	ground 3 for output buffers
CLK2	93	I	double pixel clock input
V_{DD3}	94	P	supply voltage 3 for output buffers
HD	95	I	horizontal definition input
VD	96	I	vertical definition input
FI	97	I	field identification input
DSPRST	98	I	Power-on reset for DSP
CLK1	99	I	pixel clock input
DGND1	100	P	digital ground 1 for input buffers and predrivers and for the digital core

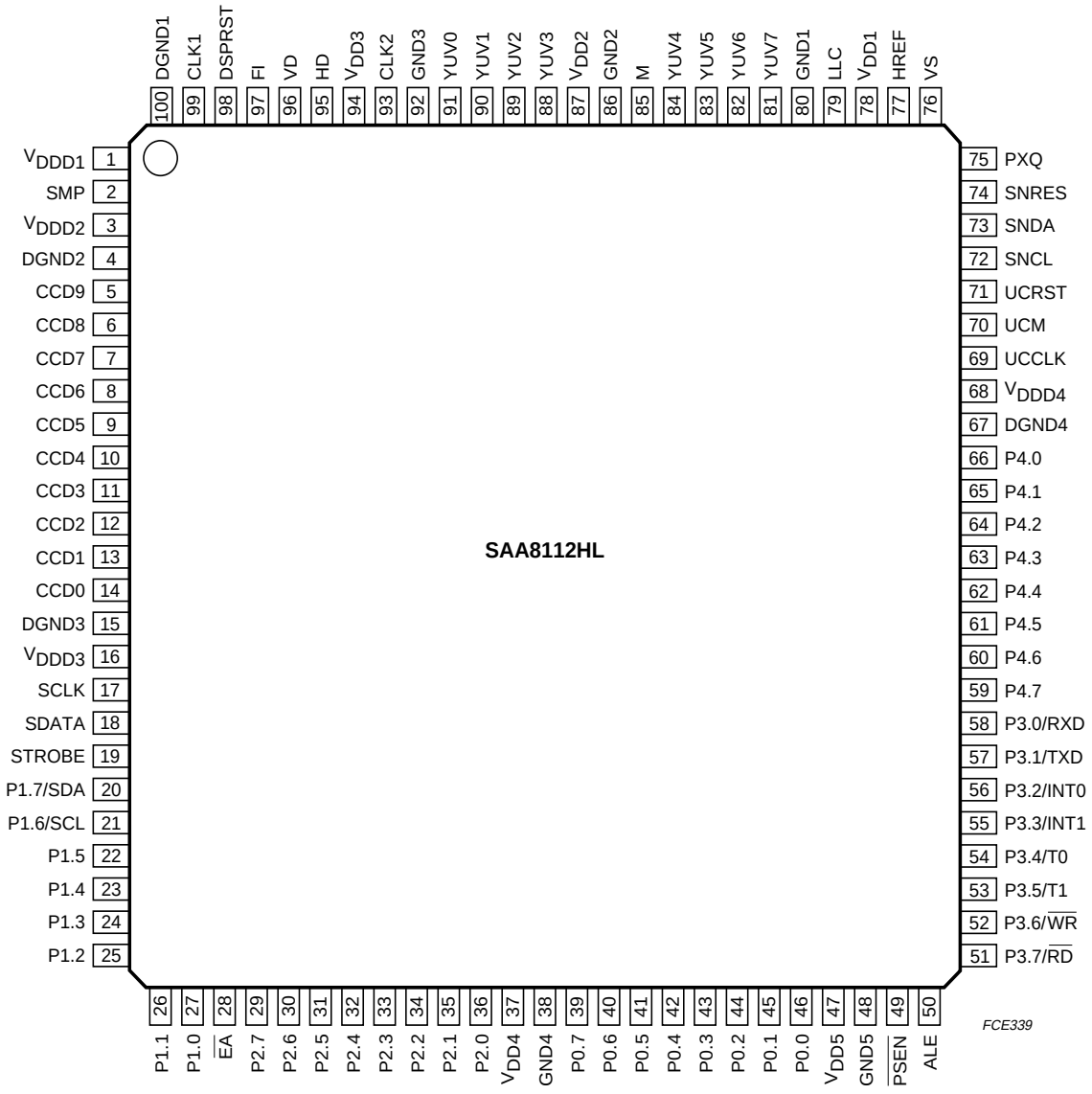


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

The SAA8112HL DSP block has a very high level of programmability. The DSP alone uses 95 (8-bit) registers (more registers are used for the ME). The SAA8112HL can accept 8- to 10-bit digital data from various sensors: CCD or CMOS, progressive or interlaced, with or without colour filters (see Table 1).

With B and W sensors, the full resolution is preserved. The DSP registers are accessed through a serial interface (UART).

8.1 Synchronization and video windows

To work properly, the SAA8112HL needs four or five input synchronization signals:

- CLK1 (pixel clock)
- CLK2 (2 times the pixel clock)
- HD (horizontal reference)
- VD (vertical reference)
- FI (Field ID, useless for progressive scanning).

The incoming CCD data is sampled on the rising edge of CLK1. The phase difference between CLK1 and CLK2 must be fixed.

The DSP working areas can be programmed and defined with reference to the rising edges of HD and VD.

Several registers allow the definition of the optical black window, the active video input window, the active video output window and the measurement windows. With interlaced applications, the windows are defined separately for the odd and the even fields.

The number of active pixels per line is limited to 800, although the total number of pixels can be higher. There is no size limitation in the vertical direction.

8.2 Optical black processing

The first processing block of the SAA8112HL is a digital clamp (denoted as OFFSET PRE_PROCESSING in Fig.1). It is used to align the optical black level to zero or to any arbitrary value.

When the digital clamp is set active, the average value of the black is measured in the programmable optical black window and then subtracted from the input signal.
A separate measurement is done for odd and even pixels and for odd and even frames.

When the digital clamp is set inactive, it is possible to subtract a fixed value from the incoming data stream.
A different value can be programmed for odd/even pixels, odd/even fields and odd/even lines.

The optical black window has a fixed size of 16 pixels (horizontally) by 128 (vertically), although the position of this window is fully programmable.

Table 1 Typical SAA8112HL compatible sensors

SENSOR TYPE	BRAND	PART NUMBER
VGA	SONY	ICX084 and ICX098
	PANASONIC	MN3777
	SHARP	LZ24BP
HR	SONY	ICX058, ICX059, ICX068, ICX069, ICX208 and ICX209
	SHARP	LZ2453 and LZ2463
MR	SONY	ICX054, ICX086 and ICX206
	SHARP	LZ2413 and LZ2423
	TOSHIBA	TCM5391AP
	PANASONIC	MN37210FP
CIF	SHARP	LZ244D and LZ2547
Other sensors	All sensors that fulfil the following criteria: • B and W; complementary mosaic or RGB Bayer colour filter • 8-, 9- or 10-bit input • Up to 800 active pixels per line • CMOS or CCD sensors • Interlaced; progressive and non-interlaced sensors.	

8.3 Colour extractor

The SAA8112HL colour extractor (denoted as RGB SEPARATION in Fig.1) can be programmed to work with both mosaic (yellow, magenta, green and cyan) and RGB Bayer colour sensors.

With mosaic sensors, a combination (either sum or subtraction) of consecutive pixels is used to extract a Y, (2R-G) and (2B-G) triplet for all pixels.

With RGB Bayer sensors, an RGB triplet is interpolated for every pixel on a 3×3 neighbourhood matrix.

With B and W sensors, the colour extractor can be disabled, thus maintaining the full sensor resolution.

Edges and video level information (white clip) are extracted at this stage (see Fig.3).

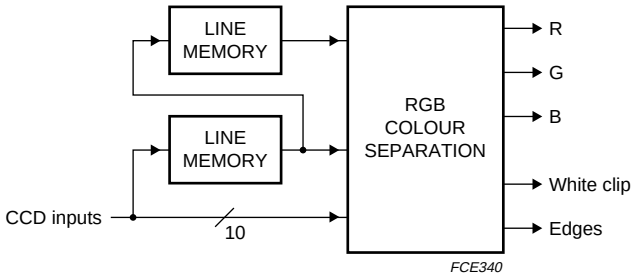


Fig.3 RGB separation diagram.

8.4 Colour matrix

A programmable 3 × 3 colour matrix (see Fig.4) is used to convert the extracted colour information, either Y, (2R-G), (2B-G) or R, G and B from the sensor colour space into a standard RGB colour space.

With B and W sensors, a unity matrix is used.

8.4.1 RGB PROCESSING

At the colour matrix output, the video signal is in RGB format. The following processing is applied on the RGB signals in this order:

- The gain of the red and blue streams can be changed to control the white balance
- A black offset (positive or negative) correction can be applied independently on each of the R, G and B signals
- A Knee function with adjustable gain and threshold can be applied to the signal to compress the highlights
- Finally, a Gamma function is applied; the Gamma curve is adjustable.

The same Knee and Gamma functions are applied on the three R, G and B signals.

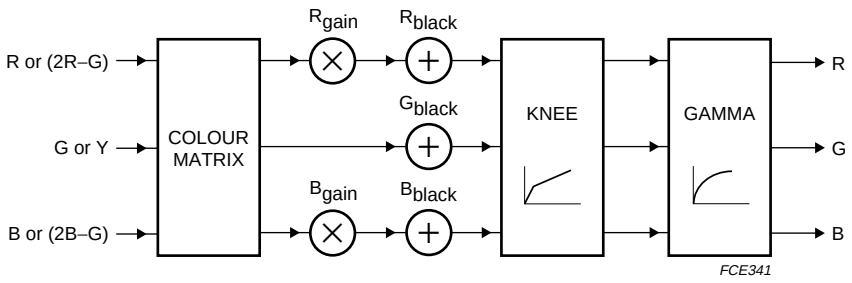


Fig.4 RGB processing diagram.

8.5 YUV processing

Following the RGB processing, the R, G and B signals are converted to YUV 4 : 2 : 2 by a fixed matrix (see Fig.5). Then, the luminance and chrominance signals are processed separately.

8.5.1 Y PROCESSING

The luminance processing consists of edge enhancement and noise reduction (see Fig.5).

The edge enhancement feature is very flexible. First, it is possible to adjust the bandwidth and the level of the edge detection. Secondly, the amount of edge enhancement can be independently adjusted for the horizontal or vertical edge or for the high or low frequency edges. The edge detection is also used for the false colour correction.

The noise reduction on the luminance signal is done by a coring filter. The amount of coring is adjustable.

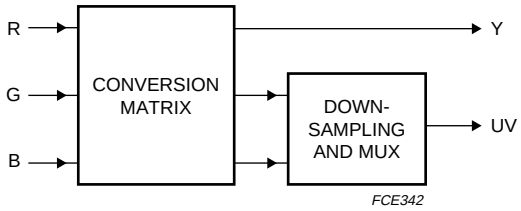


Fig.5 RGB to YUV conversion.

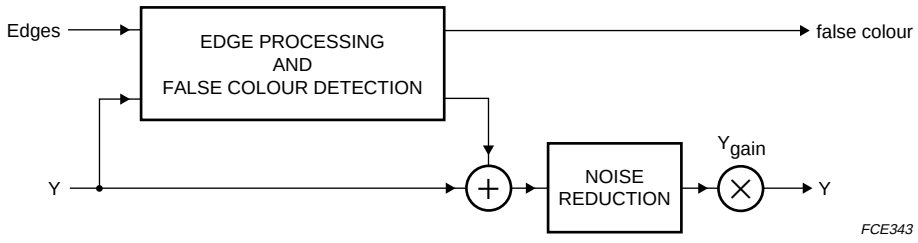


Fig.6 Y processing.

8.5.2 UV PROCESSING

The chrominance processing consists of noise reduction and colour error correction (see Fig.7). Symmetrical processing is done on the two chrominance signals. The noise reduction is done by an adjustable coring filter. The edge detection and the luminance level are used to reduce the colour errors caused by high exposure or sharp colour transitions. It is possible to adjust the number of pixels on which the correction is applied. With the sharp colour transition, the colour signal is filtered. With over exposure, the colour signal is cancelled.

The YUV processing block is terminated by three separate gain controls on the Y, U and V signals. These gains can be used to fine tune the Y, U and V colour balance and also to adjust the luminance and saturation without impacting the AE and AWB control loops.

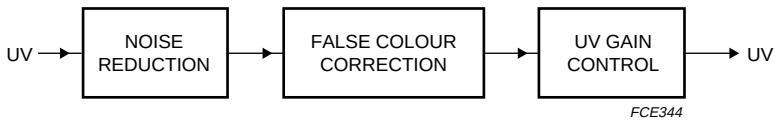


Fig.7 UV processing.

8.6 Output formatter

The last processing block of the SAA8112HL (denoted as DIGOUT in Fig.1) is a flexible output formatter, which performs two main tasks (see Table 2):

- Scaling
- Synchronization generation.

A scaler can be used to divide the horizontal or vertical resolution by two or four (high quality FIR filters are used to avoid artifacts). Also, a CIF (352 × 288) cut can be made from a VGA sensor. If not used, the scaler can be bypassed.

The output format is usually YUV 4 : 2 : 2. The YUV samples are multiplexed on a single 8-bit output port. The output data is in synchronization with the output clock (LLC). The output data rate is twice the pixel frequency. Synchronization codes SAV and EAV are inserted before and after the active line, as described in CCIR/ITU656.

In addition, three other synchronization signals are available:

- HREF: Horizontal reference. This pulse usually goes high with the first active data and goes low after the last active data. HREF does not usually include the SAV and EAV codes. To accommodate various sensor sizes, the start and stop positions of HREF are programmable.
- VS: vertical synchronization.
- PXQ: pixel qualifier; this pulse goes high with every valid pixel, including the SAV/EAV codes. It goes low when there are invalid pixels in a line, for example, when the scaler is used.

The SAA8112HL output formatter also features an IEEE1394 mode, which helps to support applications defined around the *"1394-based Digital Camera Specification"* of the IEEE1394 trade association.

In this case, the HREF, VS and PXQ signals are designed to help to packetize the video according to the following mode of the *"1394-based Digital Camera Specification"*:

- Format_0 (VGA), mode_0:
  160 × 120 YUV(4 : 4 : 4); 24 bits/pixel
- Format_0 (VGA), mode_1:
  320 × 240 YUV(4 : 2 : 2); 16 bits/pixel
- Format_0 (VGA), mode_2:
  640 × 480 YUV(4 : 1 : 1); 12 bits/pixel
- Format_0 (VGA), mode_3:
  640 × 480 YUV(4 : 2 : 2); 16 bits/pixel
- Format_0 (VGA), mode_5:
  640 × 480 Y (B and W); 8 bits/pixel.

For mode_0 and mode_2, the YUV 4 : 2 : 2 output is filtered to obtain 4 : 1 : 1 or 4 : 4 : 4.

With the IEEE1394 mode, the definition of the output synchronization pulses is changed as described below:

- HREF goes high during the first valid byte of a packet; it is low elsewhere
- VS can be programmed in length and position; this pulse can be used to set the SY field of the 1394 header to 1 for the first isochronous packet of a frame
- PXQ goes high during the valid Y, U or V data
- LLC remains the output clock and is synchronized with the data output.

Table 2 Typical cutter and scaler modes

SENSOR TYPE	OUTPUT FORMAT	CUTTER/SCALER MODES
VGA	SIF 320 × 240	scaled half horizontally and vertically
	QSIF 160 × 120	scaled quarter horizontally and vertically
High Resolution	CIF 352 × 288	scaled half horizontally and vertically
		cut
	QCIF 176 × 144	scaled quarter horizontally and vertically
		cut
		cut then scaled half horizontally and vertically
CIF	QCIF 176 × 144	scaled half horizontally and vertically

Note

1. With the HR sensor, the active area before scaling is 704 × 576 (PAL) or 704 × 486 (NTSC). Therefore, the formats generated by the scaler are: CIF 352 × 288 (PAL), 325 × 243 (NTSC) and QCIF 176 × 144 (PAL and NTSC).

8.7 Measurement Engine

The ME extracts statistical information from the video stream. These measurements are used to automatically control the white balance and the exposure. They can also be used for other purposes, such as colour detection.

The measurements are performed on pre-formatted Y, U and V streams (see Fig.5). It is possible to measure the accumulated value of the Y, U or V samples in any of 16 programmable windows. It is also possible to measure the accumulated value of the Y signal below a threshold or the number of Y samples above a threshold. Moreover, it is possible to only accumulate U and V values for which programmable conditions on Y, U and V are fulfilled.

The ME does up to 16 statistic measurements per frame (8 per field). Each measurement can be done on any of the pre-formatted signals and on any of the programmable windows.

A memory area of the SAA8112HL, called RAM workspace, is used to handle the ME operations.
In addition to the ME, a highlight counter is available, which counts the number of pixels above a programmable threshold. The highlight counter is usually used for exposure control.

8.8 Display features

The SAA8112HL also offers the possibility of visualizing selected zones of interests or selected pixels.
The visualization is done either by contrast reduction for the selected pixels or by constant level insertion.

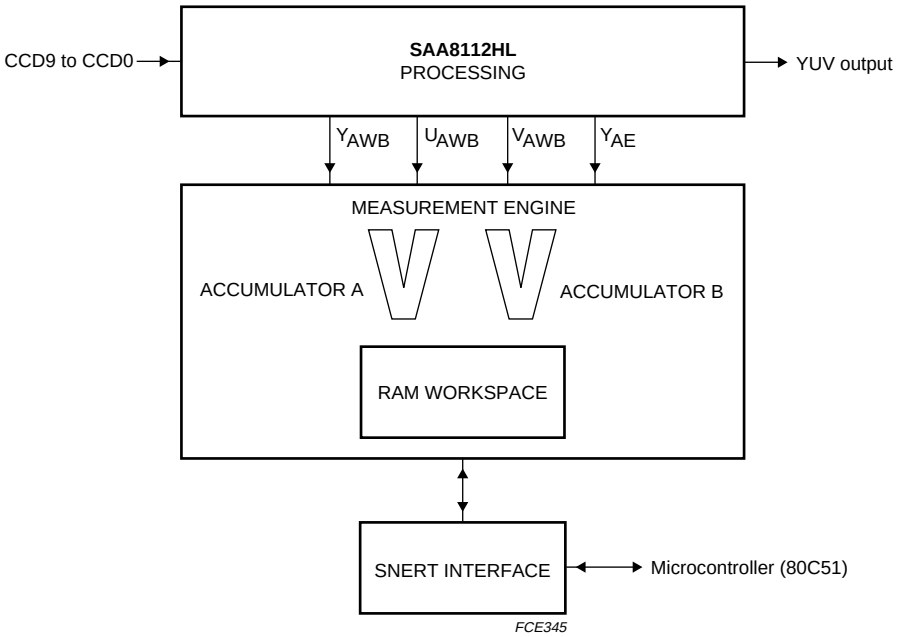


Fig.8 Measurement Engine.

8.9 Microcontroller

The embedded microcontroller is basically a 80C654 core (80C51 family) with five ports. Its functionality is standard, except that the ports are dedicated inputs, outputs or I/O ports (see Chapter 7). Ports P0 and P2 are available for connection to an emulator or to an external program PROM.

The microcontroller can control the AE and the AWB loops and can download the settings for the DSP registers from an optional EEPROM at power-up or reset, for instance.

The microcontroller includes the following features:

- 32 kbyte internal ROM
- 512 byte RAM
- Hardware I^2C-bus interface: P1.7 and P1.6
- Hardware UART interface: P3.0 and P3.1
- Power-down mode
- Two timers
- P4 is an open-drain port
- P0, P1, P2 and P3 are pull-up ports.

Table 3 80C51 Special Function Registers

SFR NAME	DESCRIPTION	SFR ADD	DATA BIT 7	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0
B	B register	F0H	B7	B6	B5	B4	B3	B2	B1	B0
ACC	accumulator	E0H	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0
SIADR	serial interface address	DBH	SA6	SA5	SA4	SA3	SA2	SA1	SA0	GC
SIDAT	serial interface data	DAH	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
SISTA	serial interface status	D9H	ST7	ST6	ST5	ST4	ST3	0	0	0
SICON	serial interface control	D8H	CR2	ENS1	STA	STO	SI	AA	CR1	CR0
PSW	program status word	D0H	CY	AC	F0	RS1	RS0	OV	–	P
P4	Port 4	C0H	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
IP	interrupt priority	B8H	–	IP6	IP5	IP4	PT1	PX1	PT0	PX0
P3	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	INT1	INT0	TXD	RXD
IE	interrupt enable	A8H	$\overline{EA}$	IE6	IE5	IE4	ET1	EX1	ET0	EX0
P2	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
SBUF	serial data buffer	99H	–	–	–	–	–	–	–	–
SCON	serial controller	98H	SM0	SM1	SM2	REN	TB8	RB8	T1	R1
P1	Port 1	90H	SDA	SCL	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
TH1	timer high 1	8DH	–	–	–	–	–	–	–	–
TH0	timer high 0	8CH	–	–	–	–	–	–	–	–
TL1	timer low 1	8BH	–	–	–	–	–	–	–	–
TL0	timer low 0	8AH	–	–	–	–	–	–	–	–
TMOD	timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0
TCON	timer control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
PCON	power control	87H	–	–	–	–	–	–	PD	IDL
DPH	data pointer high	83H	–	–	–	–	–	–	–	–
DPLI	data pointer low	82H	–	–	–	–	–	–	–	–
SP	stack pointer	81H	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
P0	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

8.10 Mode control

Two pins are dedicated to control the operational modes of the SAA8112HL: pin M for the DSP and pin UCM for the microcontroller (see Table 4). They are independent of each other.

Table 4 Mode control

M	UCM	MODE
0	0	DSP application mode
1	0	DSP test mode
0	0	microcontroller application mode
0	1	microcontroller test mode

8.11 SNERT (UART) interface - DSP registers

The DSP registers can be accessed via a SNERT interface. This SNERT interface is equivalent to the UART mode 0 interface of the 80C51 microcontroller. The DSP register list is shown in Table 5.

Table 5 Register list

ADDR	NAME	FUNCTION	FORMAT	RANGE
0	CONTROL0	see Table 6 for explanation	byte	n.a.
1	CONTROL1	see Table 7 for explanation	byte	n.a.
2	CONTROL2	see Table 8 for explanation	byte	n.a.
3	RESERVED1	–	–	–
4	OB_STARTL_F0	first line in optical black window in field 0	byte	[0 to 255]
5	OB_STARTL_F1	first line in optical black window in field 1	byte	256 + [0 to 255]
6	RESERVED2	–	–	–
7	OB_STARTP	first pixel in optical black window	byte	4 × [0 to 255]
8	OB_PE_F0	fixed optical black level for even pixel in field 0	byte	[0 to 127]
9	OB_PO_F0	fixed optical black level for odd pixel in field 0	byte	[0 to 127]
10	OB_PE_F1	fixed optical black level for even pixels in field 1	byte	[0 to 127]
11	OB_PO_F1	fixed optical black level for odd pixels in field 1	byte	[0 to 127]
12	OB_OFFSET_LE	optical black offset for even lines	byte	[0 to 255]
13	OB_OFFSET_LO	optical black offset for odd lines	byte	[0 to 255]
14	PRE_MAT_K1	factors for CCD (even pixels and lines; odd fields)	byte	[0 to 255]/256
15	PRE_MAT_K2	factors for CCD (even lines and fields; odd pixels)	byte	[0 to 255]/256
16	PRE_MAT_K3	factors for CCD (even pixels; odd lines and fields)	byte	[0 to 255]/256
17	PRE_MAT_K4	factors for CCD (odd pixels and lines; even fields)	byte	[0 to 255]/256
18	WHITE_CLIP_THR	threshold for white clip detector	byte	768 to 1023
19	COL_MAT_P11	colour matrix coefficient P11	byte	[–128 to +127]/16
20	COL_MAT_P12	colour matrix coefficient P12	byte	[–128 to +127]/16
21	COL_MAT_P13	colour matrix coefficient P13	byte	[–128 to +127]/16
22	COL_MAT_P21	colour matrix coefficient P21	byte	[–128 to +127]/16
23	COL_MAT_P22	colour matrix coefficient P22	byte	[–128 to +127]/16
24	COL_MAT_P23	colour matrix coefficient P23	byte	[–128 to +127]/16
25	COL_MAT_P31	colour matrix coefficient P31	byte	[–128 to +127]/16
26	COL_MAT_P32	colour matrix coefficient P32	byte	[–128 to +127]/16

ADDR	NAME	FUNCTION	FORMAT	RANGE
27	COL_MAT_P33	colour matrix coefficient P33	byte	[–128 to +127]/16
28	COL_MAT_RGAIN	red gain for white balance correction	byte	[0 to 255]/128
29	COL_MAT_BGAIN	blue gain for white balance correction	byte	[0 to 255]/64
30	PRE_MAT_K5	factors for CCD (odd pixels and fields; even lines)	byte	[0 to 255]/256
31	PRE_MAT_K6	factors for CCD (even pixels and fields; odd lines)	byte	[0 to 255]/256
32	PRE_MAT_K7	factors for CCD (odd pixels, lines and fields)	byte	[0 to 255]/256
33	PRE_MAT_K8	factors for CCD (even pixels, lines and fields)	byte	[0 to 255]/256
34	BLACK_LEVEL_R	fixed black offset in red channel	byte	[–128 to +127]
35	BLACK_LEVEL_G	fixed black offset in green channel	byte	[–128 to +127]
36	BLACK_LEVEL_B	fixed black offset in blue channel	byte	[–128 to +127]
37	RGB_KNEE_OFFSET	offset of the Knee compression	byte	[0 to 255]
38	GAMMA_DITH	control of gamma dithering (MSB)	2 bits	[0 to 3]
	GAMMA_BALANCE	control of gamma level (LSB)	6 bits	[0 to 63]/64
39	NPIX_LSB	total number of pixels on a line	byte	[0 to 255]
40	NPIX_MSB	most significant bits of total number of pixels/line	2 bits	[0 to 3]
41	FPIX_ACT	address of the first active pixel on a line	byte	[0 to 255]
42	LPIX_ACT_LSB	address of the last active pixel on a line	byte	[0 to 255]
43	FLINE_ACT_F0	address of the first active line in field 0	byte	[0 to 255]
44	LLINE_ACT_F0_LSB	address of the last active line in field 0	byte	[0 to 1023]
45	FLINE_ACT_F1_LSB	address of the first active line in field 1	byte	[0 to 1023]
46	LLINE_ACT_F1_LSB	address of the last active line in field 1	byte	[0 to 1023]
47	ACT_LINES_MSB	MSBs of active line numbers (see Table 9)	byte	n.a.
48	CTR_UPD_LINE	number of line for DB update of control registers	byte	[0 to 255]
49	VC_CNTRL	vertical contour control (see Table 10)	bit	n.a.
50	CLDLEV	contour level dependency level	byte	[0 to 255]
51	HCLGAIN	horizontal contour BPF low gain	nibble	[0 to 15]/16
	HCHGAIN	horizontal contour BPF high gain	nibble	[0 to 15]/16
52	CNCLEV	total contour noise coring level	6 bits	[0 to 63]
53	CONGAIN	total contour gain	byte	[0 to 63]/16
54	FCDLEV	false colour detection level	byte	[0 to 255]
55	YNCLEV	luminance noise coring level	byte	[0 to 127]/4
56	YGAIN	luminance gain	byte	[0 to 255]/128
57	GNONUNILEV	green non-uniformity level	byte	[0 to 255]
58	UVNCLEV	chrominance noise coring level	byte	[0 to 255]/4
59	UGAIN	U gain	byte	[0 to 255]/128
60	VGAIN	V gain	byte	[0 to 255]/128
61	CONTROLX	green non-uniformity control (see Table 11)	bit	n.a.
62	CIF_HFIL_CNTRL	CIF horizontal filter control (see Table 12)	bit	n.a.
63	HREFSTRT	HREF signal start position	byte	[0 to 255]/256
64	HREFSTPLSB	HREF signal stop position (LSB)	byte	[0 to 255]
65	HREFSTPMSB	HREF signal stop position (MSB) (see Table 13)	bit	n.a.

ADDR	NAME	FUNCTION	FORMAT	RANGE
66	A	AWB_A (ME)	byte	[–128 to +127]/128
67	B	AWB_B (ME)	byte	[–128 to +127]/128
68	C	AWB_C (ME)	byte	[–128 to +127]/128
69	D	AWB_D (ME)	byte	[–128 to +127]/128
70	E	AWB_E (ME)	6 bits	[0 to 63]
71	F	AWB_F (ME)	6 bits	[0 to 63]
72	HIGHLIGHTTHR	highlight threshold (ME)	byte	[0 to 255]
73	ME_RESSCALE	ME result of scaler (see Table 14)	4 bits	n.a.
74	MWHVGRID	vertical (4 MSBs) and horizontal (4 LSBs) window ME size	byte	[0 to 15]
75	DISPCNTRL	overlay control	bit	n.a.
76	YDISPLEV	overlay control	byte	[0 to 255]
77	DMWSEL	overlay control	bit	n.a.
78	VF_TGGLE	VF and FI toggle position	byte	[0 to 255] + 256
79	CIFHWIN	CIF horizontal input window control	byte	4 × [0 to 255]
80	OUTF_AVSC	output format selection register and AVSYNC (HREF) period selection (see Table 15)	bit	n.a.
81	SY_GEN	SY pulse generation control (see Table 16)	bit	n.a.
82	DOP_CNTRL0	digital output processing control (see Table 17)	bit	n.a.
83	DOP_CNTRL1	digital output processing control (see Table 18)	bit	n.a.
84	CIF_HPSTRTL	address (LSB) of first pixel in CIF cutting window	byte	[0 to 255]
85	CIF_VLSTRTL	address (LSB) of first line in CIF cutting window	byte	[0 to 255]
86	PRE_SI_LSB	control data for analog preprocessing	byte	[0 to 255]
87	PRE_SI_MSB	control data and address for analog preprocessing (see Table 19)	bit	n.a.
88	SMP_CNTRL	switched mode power supply control	byte	[0 to 255]
89	CIFVWIN	CIF vertical input window control	byte	4 × [0 to 255]
90	DIG_SETUP	set-up level in digital output	byte	[0 to 255]
91	RESERVED3	–	–	–
92	RESERVED4	–	–	–
93	RESERVED5	–	–	–
94	PRE_PROC_DEL	control compensation delay w.r.t. preprocessing	4 bits	[0 to 15]
126	RAMWRPTR	RAM write pointer to internal workspace	byte	[0 to 223]
127	RAMWRDATA	RAM write data to internal workspace	byte	[0 to 255]

Table 6 Register CONTROL0 (address: 0x00H)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								auto optical black control:	AUTO_OPT_BLACK
							1	on	
							0	off	
								type of sensor:	SENS_VGA
						1		RGB Bayer CCD (VGA)	
						0		complementary mosaic CCD (PAL/NTSC)	
								type of colour filter (if SENS_VGA = 0):	MOSAIC_FIL_TYPE
					1			filter type B	
					0			filter type A	
								colour separator (if SENS_VGA = 1):	RGC
					1			on	
					0			off (raw data mode)	
				1				synchronizes the colour separator on pixel level	PIX_PHASE
			1					synchronizes the colour separator on line level	LINE_PHASE
		1						synchronizes the colour separator on field level	FIELD_PHASE
0	0								Reserved

Table 7 Register CONTROL0 (address: 0x01H)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
						0	0		Reserved
								compression factor for RGB knee:	RGB_KNEE_K
				1	1			$\frac{1}{2}$	
				1	0			$\frac{3}{8}$	
				0	1			$\frac{1}{4}$	
				0	0			$\frac{1}{8}$	
								selection of filter characteristics of UV downsample filters:	MED_RES
			1					for medium resolution sensors	
			0					for high resolution sensors	
								video mode selection:	PAL_NTSC
		1						PAL	
		0						NTSC	
0	0								Reserved

Table 8 Register CONTROL2 (address: 0x02H)

X = don't care.

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
							1	false colour low pass filter (on = high)	FCC_FILTER
						1		non-interlaced mode selection	NI
				0	0				Reserved
								white clip mapping on UV grid	WH_CL_MAP
		1	X					[11111] spreading filter, kills 5 UV samples	
		0	1					[01110] spreading filter, kills 3 UV samples	
		0	0					[00100] spreading filter, kills only current UV sample	
								switch control for false colour concealment signal	FC_MAP
1	X							[11111] spreading filter, conceals 5 UV samples	
0	1							[01110] spreading filter, conceals 3 UV samples	
0	0							[00100] spreading filter, conceals only current UV sample	

Table 9 Register ACT_LINES_MSB (address: 0x2FH)

BIT								PARAMETER
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**
							1	bit 8 of LPIX_ACT_LSB (0x2AH)
						1		bit 9 of LPIX_ACT_LSB (0x2AH)
					1			bit 8 of LLINE_ACT_F0_LSB (0x2CH)
				1				bit 9 of LLINE_ACT_F0_LSB (0x2CH)
			1					bit 8 of FLINE_ACT_F1_LSB (0x2DH)
		1						bit 9 of FLINE_ACT_F1_LSB (0x2DH)
	1							bit 8 of LLINE_ACT_F1_LSB (0x2EH)
1								bit 9 of LLINE_ACT_F1_LSB (0x2EH)

Table 10 Register VC_CNTRL (address: 0x31H)

X = don't care.

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
				X	X	X	X	vertical contour gain (range 0 to 15)	VCGAIN
	X	X	X					vertical contour filter coefficient (range 0 to 7)	KCOMB
								horizontal VC filter	n.a.
1								on	
0								off	

Table 11 Register CONTROLX (address: 0x3DH)

BIT								PARAMETER
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**
								vertical contour filter gain
							1	normal
							0	double
0	0	0	0	0	0	0		reserved

Table 12 Register CIF_HFIL_CNTRL (address: 0x3EH)
X = don’t care.

BIT								PARAMETER
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**
								luminance CIF horizontal filter control
						1	X	quarter bandwidth
						0	1	half bandwidth
						0	0	bypass, full bandwidth
								chrominance horizontal filter control
				1	X			quarter bandwidth
				0	1			half bandwidth
				0	0			bypass, full bandwidth
0	0	0	0					reserved

Table 13 Register HREFSTPMSB (address: 0x41H)

BIT								PARAMETER
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**
							1	bit 8 of HREFSTPLSB (0x40H)
						1		bit 9 of HREFSTPLSB (0x40H)
0	0	0	0	0	0			reserved

Table 14 Register MECNTRL (address: 0x4BH)
X = don't care.

BIT								PARAMETER
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**
								ME result of scaler selection
					1	1	X	reserved
					1	0	1	divide by 32
					1	0	0	divide by 16
					0	1	1	divide by 8
					0	1	0	divide by 4
					0	0	1	divide by 2
					0	0	0	pass through
								ME synchronization
				1				in field mode
				0				in frame mode
0	0	0	0					reserved

Table 15 Register OUTF_AVSC (address: 0x50H)
X = don't care.

BIT								PARAMETER
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**
								AVSYNC (HREF) period (in CLK1 cycles during active video)
				1	1	1	1	2560 CLK1 cycles when AVVALID (PXQ) is high
				1	1	1	0	1920 CLK1 cycles
				1	1	0	1	1280 CLK1 cycles
				1	1	0	0	960 CLK1 cycles
				1	0	1	1	640 CLK1 cycles
				1	0	1	0	480 CLK1 cycles
				1	0	0	1	320 CLK1 cycles
				1	0	0	0	240 CLK1 cycles
				0	1	1	1	160 CLK1 cycles
				0	1	1	0	120 CLK1 cycles
				0	1	0	1	80 CLK1 cycles
				0	1	0	0	60 CLK1 cycles
				0	0	1	1	40 CLK1 cycles
				0	0	1	0	30 CLK1 cycles
				0	0	0	1	20 CLK1 cycles
				0	0	0	0	15 CLK1 cycles
								output format select code
	1	1	1					IEEE-1394 4 : 4 : 4 mode (IEEE-1384 camera mode_0)
	1	1	0					IEEE-1394 4 : 2 : 2 mode (IEEE-1384 camera mode_1 and mode_3)
	1	0	1					IEEE-1394 4 : 1 : 1 mode (IEEE-1384 camera mode_2)
	1	0	0					IEEE-1394 4 : 0 : 0 (B and W) mode (IEEE-1384 camera mode_5)
	0	X	X					standard 4 : 2 : 2 mode
X								MSB of SY (VS) duration

Table 16 Register SY_GEN (address: 0x51H)
X = don't care.

BIT								PARAMETER
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**
								SY (VS) vertical offset
					1	1	1	+4 lines
					1	1	0	+3 lines
					1	0	1	+2 lines
					1	0	0	+1 line
					0	1	1	0 line
					0	1	0	–1 line
					0	0	1	–2 lines
					0	0	0	–3 lines
								SY polarity
				1				negative
				0				positive
X	X	X	X					SY pulse duration code (4 LSBs) (range [0 to 32] × CLK2)

Table 17 Register DOP_CNTRL0 (address: 0x52H)
X = don't care.

BIT								PARAMETER
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**
								horizontal scaling processing control bits
						1	X	downsampling off
						0	1	downsample by 2
						0	0	downsample by 4
								vertical scaling processing control bits
				1	1			upsample by 2
				1	0			downsampling off
				0	1			downsample by 2
				0	0			downsample by 4
								temporal scaling processing control bits
		1	1					downsample by 8
		1	0					downsample by 4
		0	1					downsample by 2
		0	0					downsampling off
								scaling processing enable
	1							on
	0							off (bypass)
								CIF format
1								CIF
0								QCIF

Table 18 Register DOP_CNTRL1 (address: 0x53H)

BIT								PARAMETER
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**
							1	bit 8 of CIF_VLSTRTL (0x55H)
						1		bit 9 of CIF_VLSTRTL (0x55H)
					1			bit 8 of CIF_HPSTRTL (0x54H)
				1				bit 9 of CIF_HPSTRTL (0x54H)
			1					use PXQ output
			0					use CREF output
								sensor type
		1						CIF sensor
		0						non-CIF sensor
								digital output format
	1							D1
	0							B and W for IEEE-1394
								CLK1/CLK2 interface reset
1								reset
0								free running, normal operation

Table 19 Register PRE_SI_MSB (address: 0x57H)

BIT								PARAMETER
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**
							1	control data bits D8
						1		control data bits D9
					1			control address bits A0
				1				control address bits A1
			1					control address bits A2
0	0	0						reserved

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	notes 1 and 2	–0.5	+4.0	V
V_{DGND}	digital ground voltage	note 1	–0.5	+4.0	V
V_I	input signal voltage	note 1	–0.5	V_{DDD} + 0.5	V
V_O	output signal voltage	note 1	–0.5	V_{DDD} + 0.5	V
T_{stg}	storage temperature	note 1	–55	+150	°C
T_{amb}	ambient temperature	note 1	0	70	°C
T_j	junction temperature	note 1	–40	+125	°C

Notes

1. Stress beyond these levels may cause permanent damage to the device.
2. Only pin ‘16’ is connected to the microcontroller core.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	53	K/W

11 OPERATING CHARACTERISTICS

V_{DDD} = 3.3 V ±10%; T_{amb} = 0 to 70 °C; unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General supply						
V_{DDD}	digital power supply voltage		3.0	3.3	3.6	V
DGND	digital ground		0	0	0	V
$I_{DDD(tot)}$	digital power supply current (total)	V_{DDD} = 3.6 V T_{amb} = 70 °C	–	–	80	mA
Data and control inputs (CCD9 to CCD0, HD, VD, FI, CLK1, CLK2, M, DSPRST, $\overline{EA}$, UCCLK, UCM and UCRST)						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	–	V
I²C-bus, UART (SCLK, SDATA, STROBE, SNCL, SNDA and SNRES)						
V_{IL}	LOW-level input voltage		–	–	$0.3 \times V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DDD}$	–	–	V
Data and control outputs (SMP, P2.7 to P2.0, $\overline{PSEN}$, ALE, P0.7 to P0.0, YUV7 to YUV0, PXQ, VS, HREF and LLC)						
V_{OL}	LOW-level output voltage		0	–	$0.1 \times V_{DDD}$	V
V_{OH}	HIGH-level output voltage		$0.9 \times V_{DDD}$	–	V_{DDD}	V

12 ELECTRICAL CHARACTERISTICS

Table 20 Data input/output timing
V_{DDD} = 3.3 V ±10%; T_{amb} = 0 to 70 °C.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Data inputs related to CLK1 (CCD9 to CCD0, HD, VD and FI)					
$t_{su(i)(D)}$	data input set-up time	2	–	–	ns
$t_{h(i)(D)}$	data input hold time	1.5	–	–	ns
Data outputs related to CLK2 (YUV7 to YUV0, HREF)					
$t_{d(o)(D)}$	data output delay time	–	13.5	16	ns
Data outputs related to CLK2 (VS and PXQ)					
$t_{d(o)(D)}$	data output delay time	–	7.5	10	ns

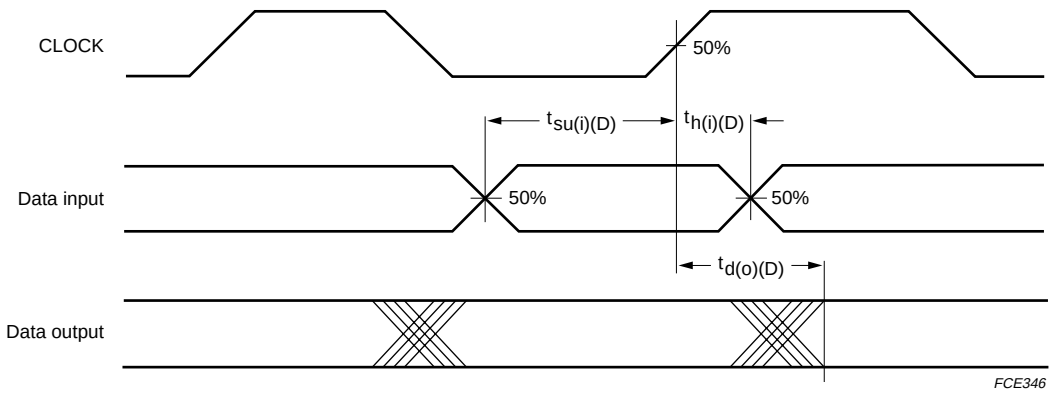


Fig.9 Data input/output timing diagrams.

13 APPLICATION INFORMATION

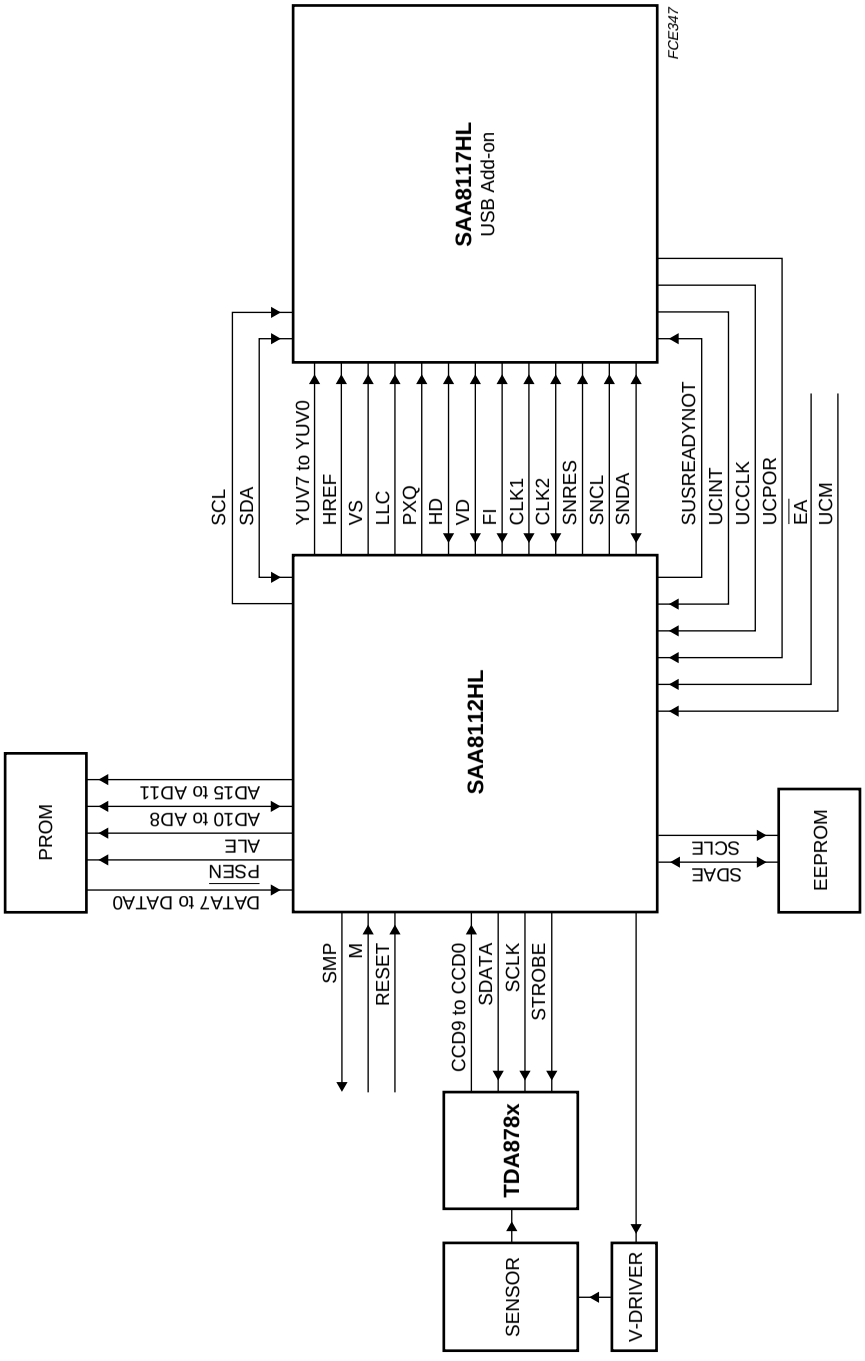


Fig.10 USB application.

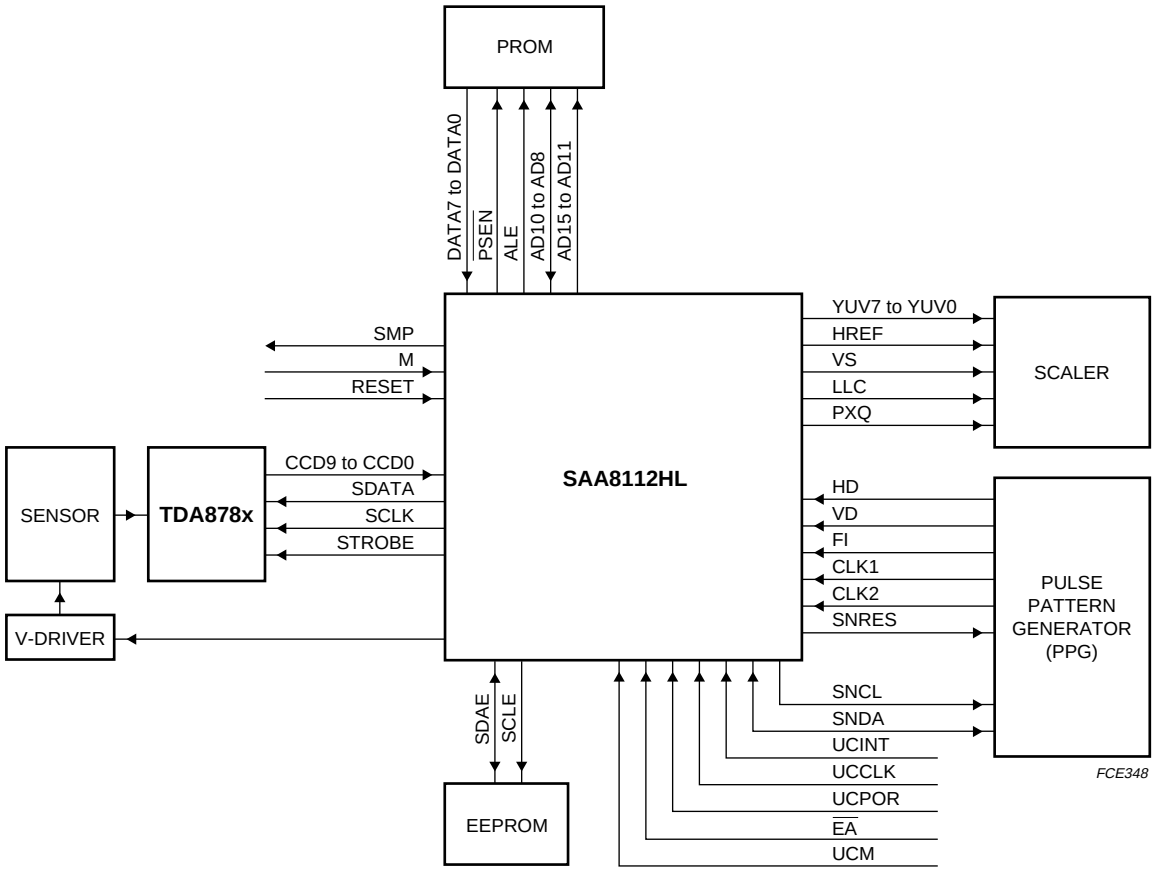
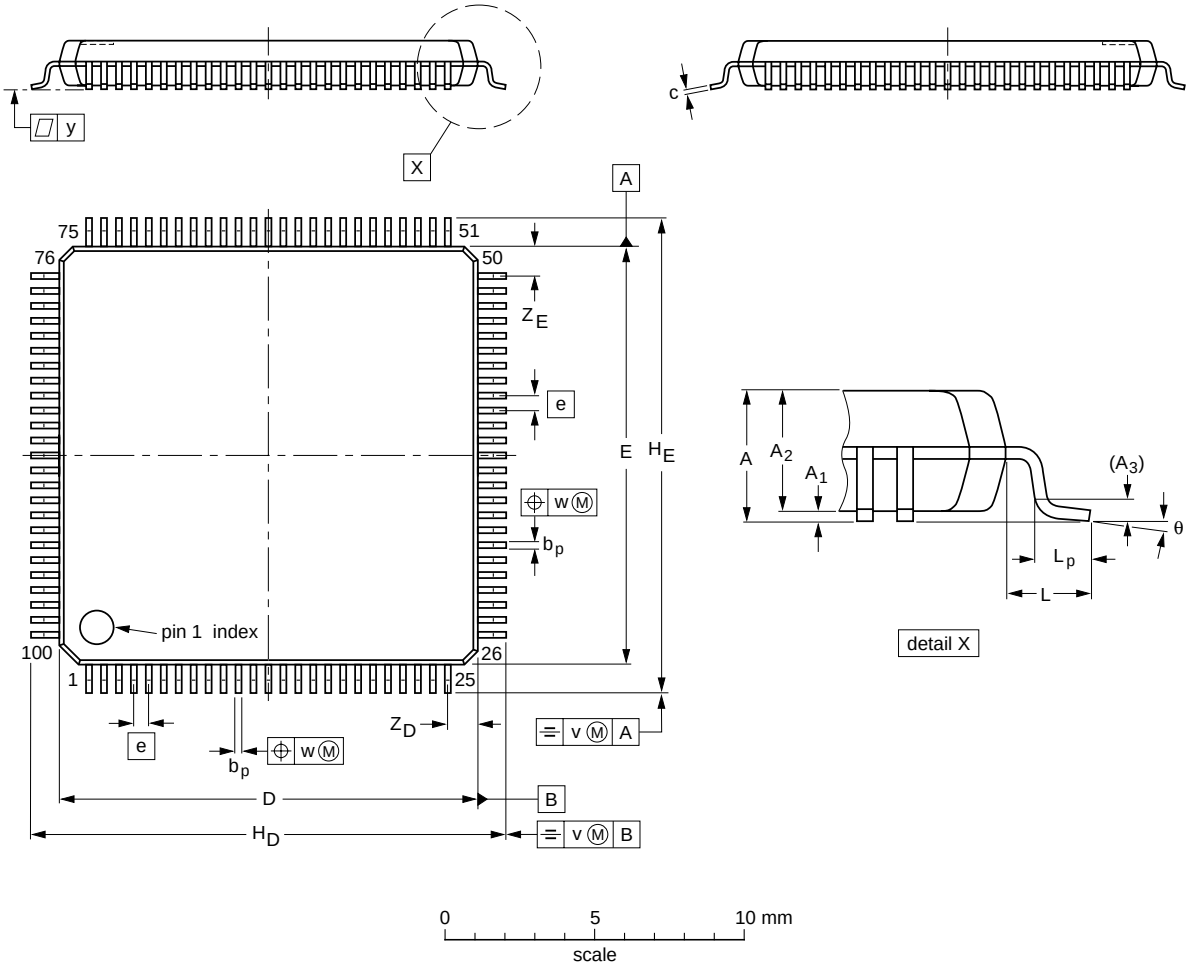


Fig.11 Digital module application (VGA PAL/NTSC/CIF PPG).

14 PACKAGE OUTLINE

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1		MS-026				~~97-08-04~~ 99-12-27

15 SOLDERING

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

16 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

17 LIFE SUPPORT APPLICATIONS

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