ZMDI
The Analog Mixed Signal Company

Brief Data Sheet

Rev. 1.00 / June 2013

ZSPM1005

True Digital PWM Controller (Single-Phase, Single-Rail)

Smart Power Management ICs



Power and Precision

ZSPM1005

True Digital PWM Controller (Single-Phase, Single-Rail)

The Analog Mixed Signal Company

Brief Description

The ZSPM1005 is a configurable true-digital single-phase PWM controller for high-current, non-isolated DC/DC supplies. It operates as a synchronous step-down converter in a single-rail and single-phase configuration.

The ZSPM1005 integrates a digital control loop, optimized for maximum flexibility and stability as well as load step and steady-state performance. In addition, a rich set of protection and monitoring functions is provided. To facilitate user configuration of the part, a set of configuration options can be pre-programmed in the ZSPM1005 that can be selected by setting the values of two external resistors.

ZMDI's Pink Power Designer™; a PC-based, user-friendly interface to the ZSPM1005, can be used to expedite the design of the digital compensator. It offers intuitive configuration methods for additional features, such as protection and sequencing. Once the part is programmed, the resistor options can be used to select the required configuration without a digital bus.

Features

- Programmable digital control loop
- Advanced, digital control techniques
  - Tru-sample Technology™
  - State-Law Control™ (SLC)
  - Sub-cycle Response™ (SCR)
- Improved transient response and noise immunity
- Protection features
  - Over-current protection
  - Over-voltage protection (VIN, VOUT)
  - Under-voltage protection (VIN, VOUT)
  - Overloaded startup
  - Restart and delay
- Support for SMOD and ZCD drivers
- Fuse-based one-time programmable (OTP) nonvolatile memory for improved reliability
- Operation from a single 5V or 3.3V supply
- 2-pin configuration for compensation, output voltage, and more

Benefits

- Fast configuration and design flexibility improves time-to-market
- Simplified design and integration
- FPGA designer-friendly solution
- Highest power density with smallest footprint
- Pin-to-pin compatible with the ZSPM1000 PWM controller enabling point-of-load power module platform designs with or without digital communication
- Higher energy efficiency across all output loading conditions

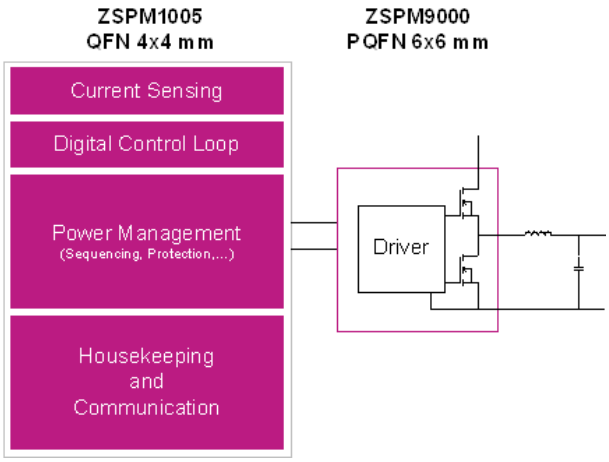
Available Support

- Evaluation Kit
- PC-based Pink Power Designer™

Physical Characteristics

- Operation temperature: -40°C to +125°C
- V_{OUT} max: 5V
- Lead free (RoHS compliant) 24-pin QFN package (4mm x 4mm)

ZSPM1005 Typical Application Diagram



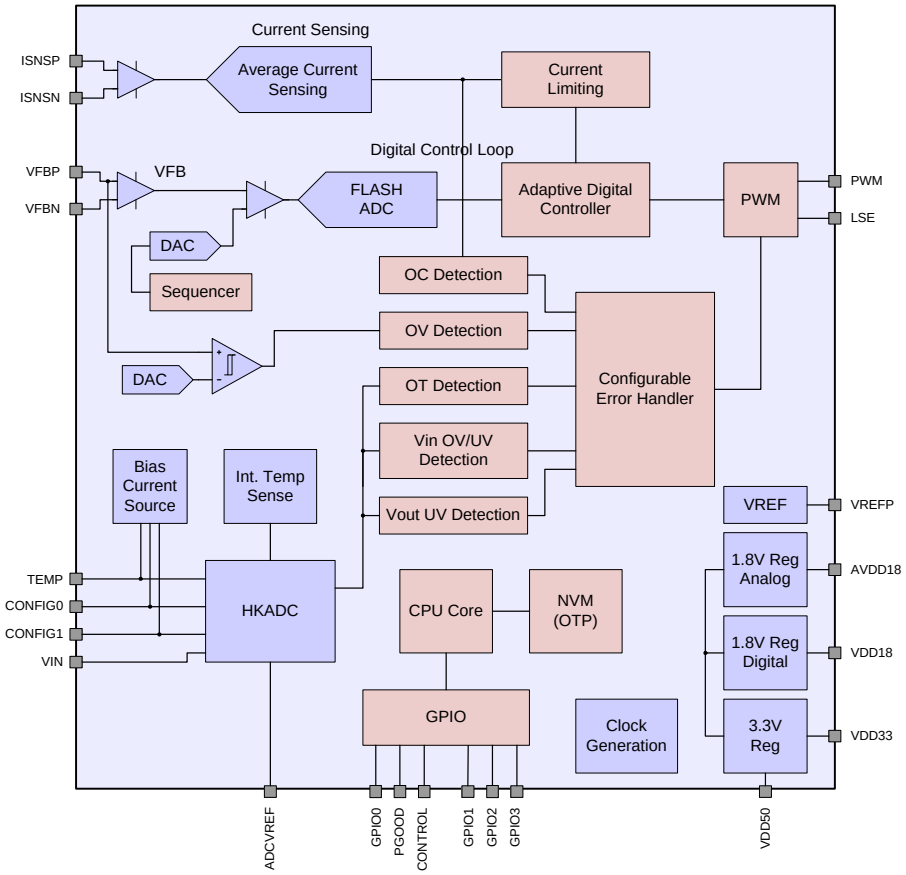
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ZSPM1005

True Digital PWM Controller (Single-Phase, Single-Rail)

ZSPM1005 Block Diagram



Optimal Applications

- *FPGA designs*
- *Point-of-load power modules for single-phase applications including telecommunication, base stations, servers and storage*

Ordering Information

Product Sales Code	Description	Package
ZSPM1005ZA1R 0	ZSPM1005 Lead-free QFN24 — Temperature range: -40°C to +125°C	Reel

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1 IC Characteristics

Note: The absolute maximum ratings are stress ratings only. The ZSPM1005 might not function or be operable above the recommended operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. ZMDI does not recommend designing to the “Absolute Maximum Ratings.”

1.1. Absolute Maximum Ratings

PARAMETER	PINS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltages						
5 V supply voltage	VDD50	dV/dt < 0.15V/µs	-0.3		5.5	V
Maximum slew rate					0.15	V/µs
3.3 V supply voltage	VDD33		-0.3		3.6	V
1.8 V supply voltage	VDD18 AVDD18		-0.3		2.0	V
Digital pins						
Digital I/O pins	GPIOx CONTROL PGOOD LSE PWM		-0.3		5.5	V
Analog pins						
Current sensing	ISNSP ISNSN		-0.3		5.5	V
Voltage feedback	VFBP VFBN		-0.3		2.0	V
All other analog pins	ADCVREF VREFP TEMP VIN CONFIGx		-0.3		2.0	V
Ambient conditions						
Storage temperature			-40		150	°C
Electrostatic discharge – Human Body Model [1)]					+/-2k	V
Electrostatic discharge – Charge Device Model [1)]					+/- 500	V

1) ESD testing is performed according to the respective JESD22 JEDEC standard.

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1.2. Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Ambient conditions						
Operation temperature	T_{AMB}		-40		125	°C
Thermal resistance junction to ambient	θ_{JA}			40		K/W

1.3. Electrical Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltages						
5 V supply voltage—VDD50 pin	V_{VDD50}		4.75	5.0	5.25	V
5 V supply current	I_{VDD50}	VDD50=5.0 V		23		mA
3.3 V supply voltage	V_{VDD33}	Supply for both the VDD33 and VDD50 pins if the internal 3.3V regulator is not used.	3.0	3.3	3.6	V
3.3 V supply current	I_{VDD33}	VDD50=VDD33=3.3 V		23		mA
Internally generated supply voltages						
3.3 V supply voltage—VDD33 pin	V_{VDD33}	VDD50=5.0 V	3.0	3.3	3.6	V
3.3 V output current	I_{VDD33}	VDD50=5.0 V			2.0	mA
1.8 V supply voltages—AVDD18 and VDD18 pins	V_{AVDD18} V_{VDD18}	VDD50=5.0 V	1.72	1.80	1.98	V
1.8 V output current					0	mA
Power-on reset threshold for VDD33 pin – on	$V_{TH_POR_ON}$			2.8		V
Power-on reset threshold for VDD33 pin – off	$V_{TH_POR_OFF}$			2.6		V
Digital IO pins (GPIOx, CONTROL, PGOOD)						
Input high voltage		VDD33=3.3 V	2.0			V
Input low voltage		VDD33=3.3 V			0.8	V
Output high voltage		VDD33=3.3 V	2.4		VDD33	V
Output low voltage					0.5	V
Input leakage current					±1	µA
Output current - high					2.0	mA
Output current - low					2.0	mA

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital IO pins with tri-state capability (LSE, PWM)						
Output high voltage		VDD33=3.3 V	2.4		VDD33	V
Output low voltage					0.5	V
Output current - high					2.0	mA
Output current - low					2.0	mA
Tri-state leakage current					±1.0	µA
Output voltage (without external feedback divider; see section 3.3.3)						
Set-point voltage			0		1.4	V
Set-point resolution				1.4		mV
Set-point accuracy		VOUT=1.4 V		1		%
Inductor current measurement						
Common mode voltage across ISNSP and ISNSN pins			0		5.0	V
Differential voltage range across ISNSP and ISNSN pins					±100	mV
Accuracy				5		%
Recommended DCR sense voltage for maximum output current			10			mV
Digital pulse width modulator						
Switching frequency	f_{SW}		177		1000	kHz
Resolution				163		ps
Frequency accuracy				2.0		%
Over-voltage protection						
Reference DAC						
Set-point voltage			0		1.58	V
Resolution				25		mV
Set point accuracy				2		%
Comparator						
Hysteresis				35		mV

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Housekeeping analog-to-digital converter (HKADC) input pins						
Input voltage—TEMP, VIN, CONFIG0, and CONFIG1 pins			0		1.44	V
Source impedance Vin sensing					3	kΩ
ADC resolution				0.7		mV
External temperature measurement (Note: Only PN-junction sense elements are supported)						
Bias currents for external temperature sensing—TEMP pin				60		µA
Resolution—TEMP pin				0.32		K
Accuracy of measurement—TEMP pin				±5.0		K
Internal temperature measurement						
Resolution				0.22		K
Accuracy of measurement				±5.0		K

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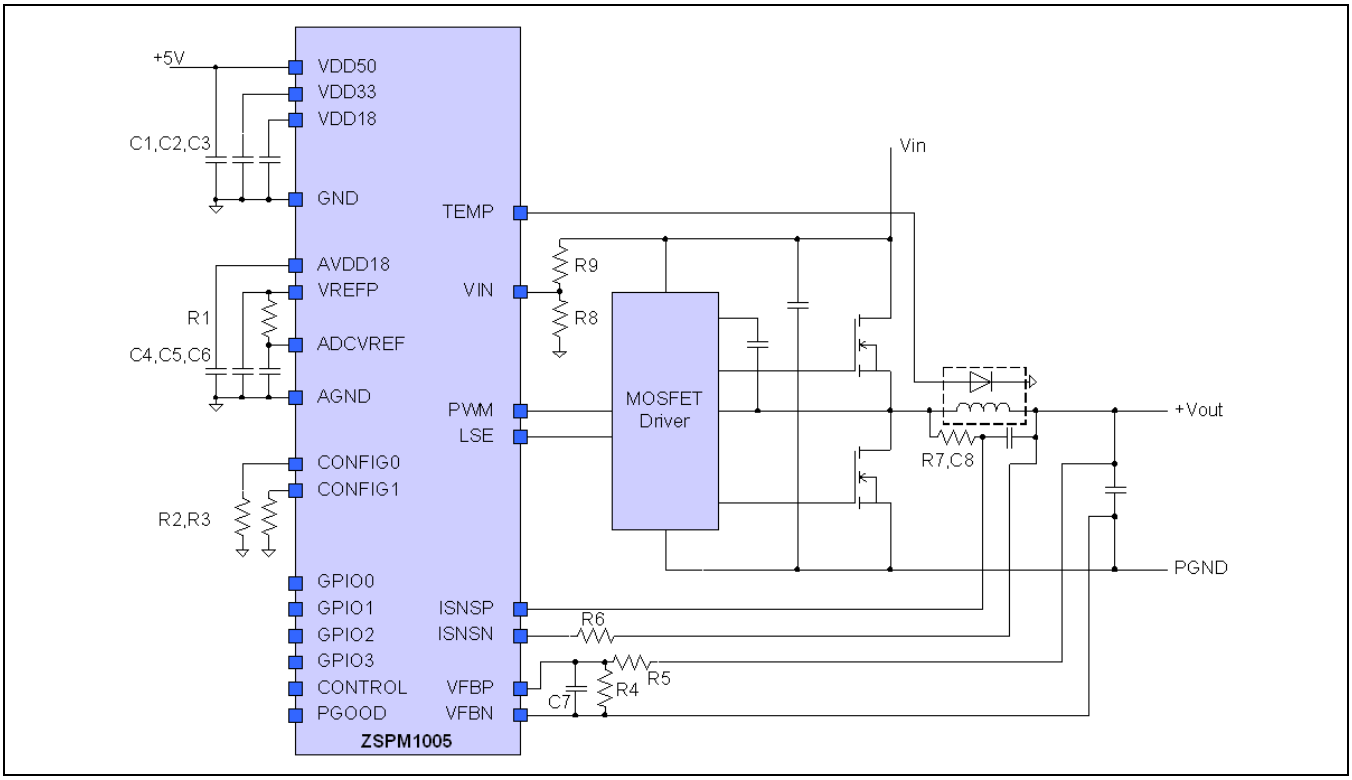
2 Product Summary

2.1. Overview

The ZSPM1005 is a configurable true-digital single-phase PWM controller for high-current, non-isolated DC/DC supplies, supporting switching frequencies up to 1MHz. It offers a configurable digital power control loop incorporating output voltage sensing, average inductor current sensing, and extensive fault monitoring and handling options. Several different functional units are integrated in the device. A dedicated digital control loop is used to provide fast loop response and optimal output voltage regulation. This includes output voltage sensing, average inductor current sensing, a digital control law, and a digital pulse-width modulator (DPWM). In parallel, a dedicated, configurable error handler allows fast and flexible detection of error signals and their appropriate handling. A housekeeping analog-to-digital converter (HKADC) ensures the reliable and efficient measurement of environmental signals, such as input voltage and temperature.

An application-specific, low-energy integrated microcontroller is used to control the overall system. It manages configuration of the various logic units according to the preprogrammed configuration look-up tables and the external configuration resistors connected to the CONFIG0 and CONFIG1 pins. These pin-strapping resistors expedite configuration of output voltage, compensation, rise time, and additional parameters without requiring digital communication. ZMDI's Pink Power Designer™ graphical user interface (GUI) allows the user to define the look-up tables and program additional parameters via the GPIO2 and GPIO3 pins.

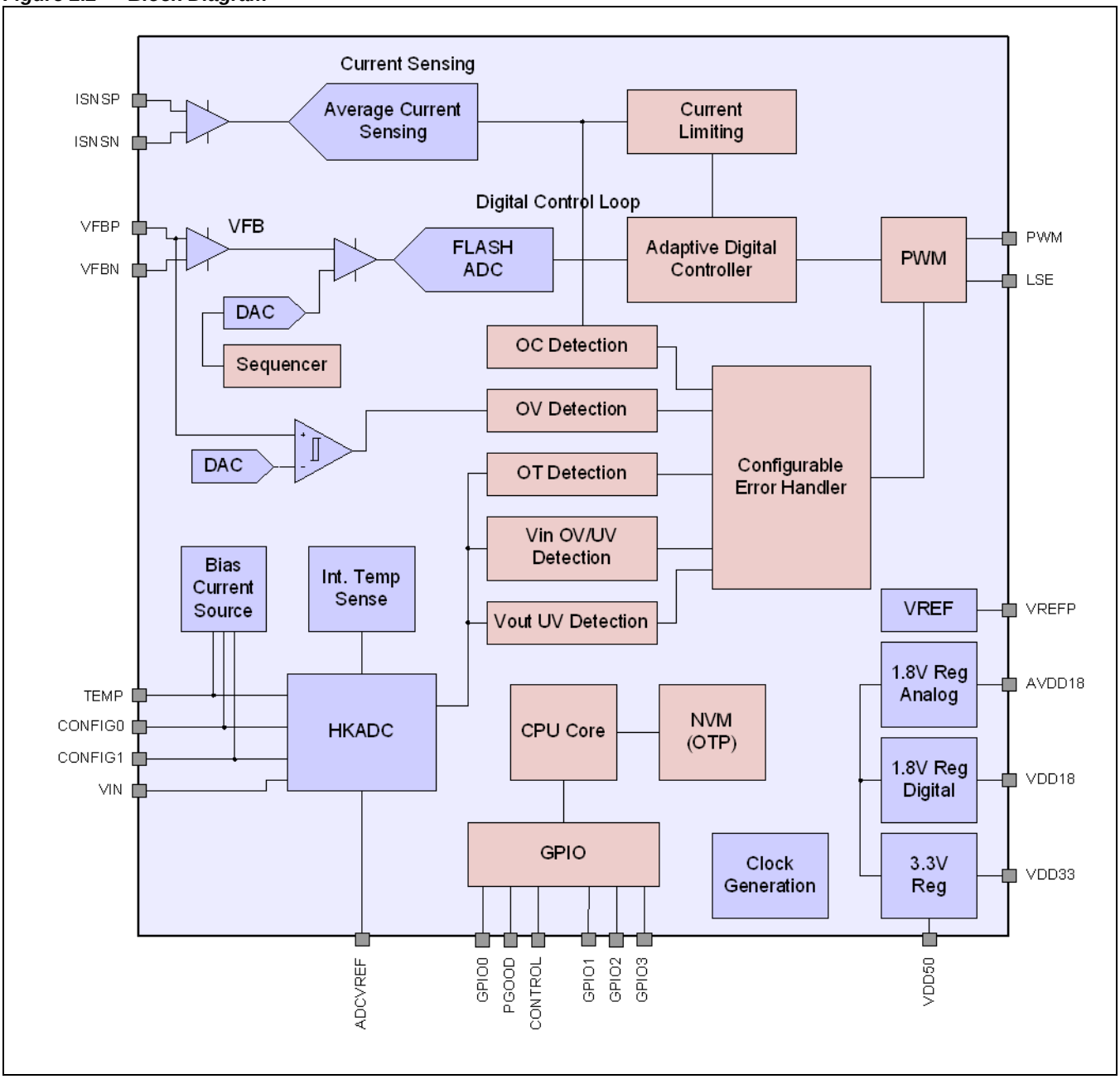
Figure 2.1 Typical Application Circuit with a 5 V Supply Voltage



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A high-reliability, high-temperature one-time programmable memory (OTP) is used to store configuration parameters. All required bias and reference voltages are internally derived from the external supply voltage.

Figure 2.2 Block Diagram



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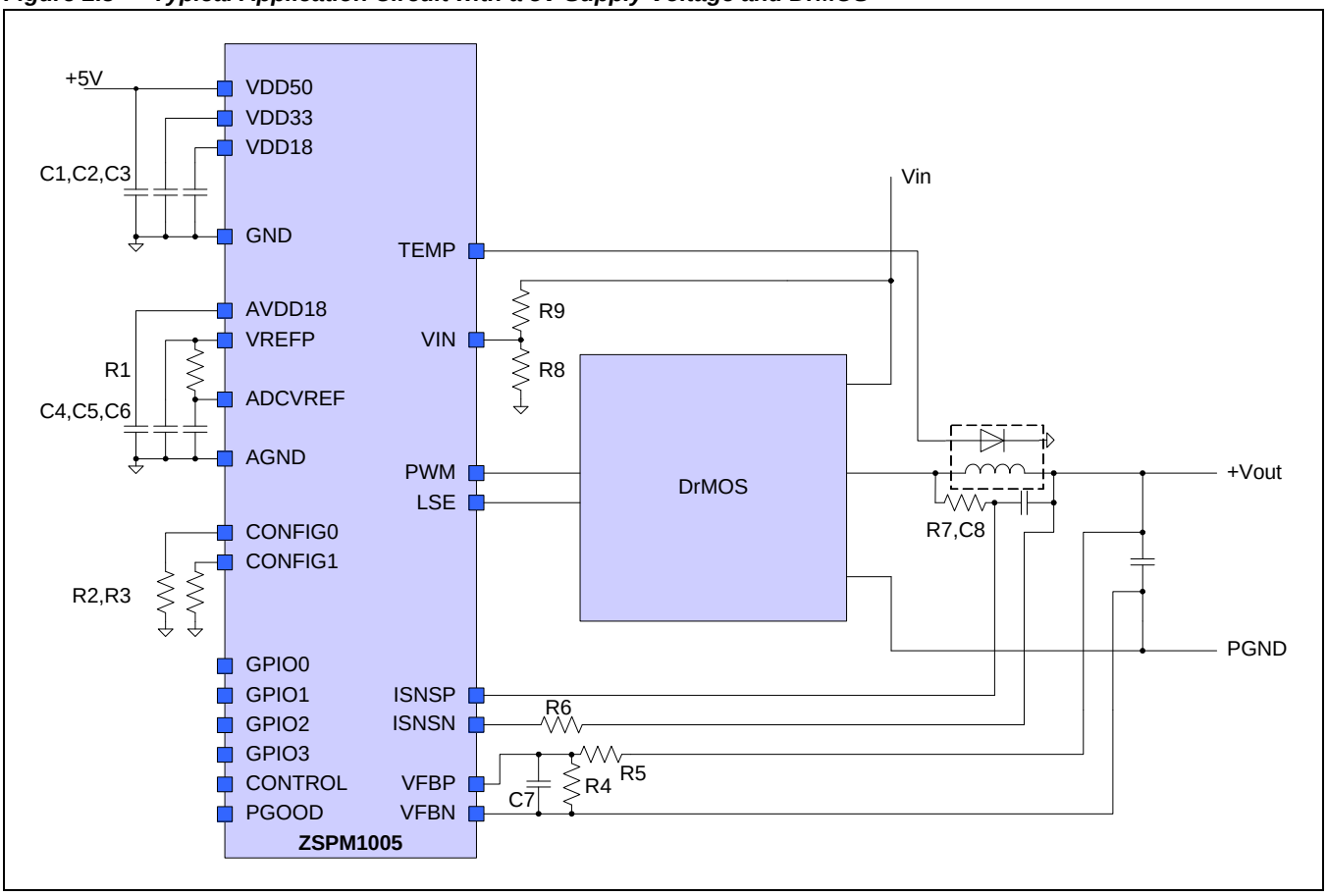
2.2. Pin Description

Pin	Name	Direction	Type	Description
1	AGND	Input	Supply	Analog Ground
2	VREFP	Output	Supply	Reference Terminal
3	VFBP	Input	Analog	Positive Input of Differential Feedback Voltage Sensing
4	VFBN	Input	Analog	Negative Input of Differential Feedback Voltage Sensing
5	ISNSP	Input	Analog	Positive Input of Differential Current Sensing
6	ISNSN	Input	Analog	Negative Input of Differential Current Sensing
7	TEMP	Input	Analog	Connection to External Temperature Sensing Element
8	VIN	Input	Analog	Power Supply Input Voltage Sensing
9	CONFIG0	Input	Analog	Configuration selection 0
10	CONFIG1	Input	Analog	Configuration selection 1
11	PWM	Output	Digital	High-side FET Control Signal
12	LSE	Output	Digital	Low-side FET Control Signal
13	PGOOD	Output	Digital	PGOOD Output (Internal Pull-Down)
14	CONTROL	Input	Digital	Control Input
15	GPIO0	Input/Output	Digital	General Purpose Input/Output Pin
16	GPIO1	Input/Output	Digital	General Purpose Input/Output Pin
17	GPIO2	Input/Output	Digital	General Purpose Input/Output Pin
18	GPIO3	Input/Output	Digital	General Purpose Input/Output Pin
19	GND	Input	Supply	Digital Ground
20	VDD18	Output	Supply	Internal 1.8 V Digital Supply Terminal
21	VDD33	Input/Output	Supply	3.3 V Supply Voltage Terminal
22	VDD50	Input	Supply	5.0 V Supply Voltage Terminal
23	AVDD18	Output	Supply	Internal 1.8 V Analog Supply Terminal
24	ADCVREF	Input	Analog	Analog-to-Digital Converter (ADC) Reference Terminal
PAD	PAD	Input	Analog	Exposed Pad, Digital Ground

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2.3. Typical Application Circuit

Figure 2.3 Typical Application Circuit with a 5V Supply Voltage and DrMOS

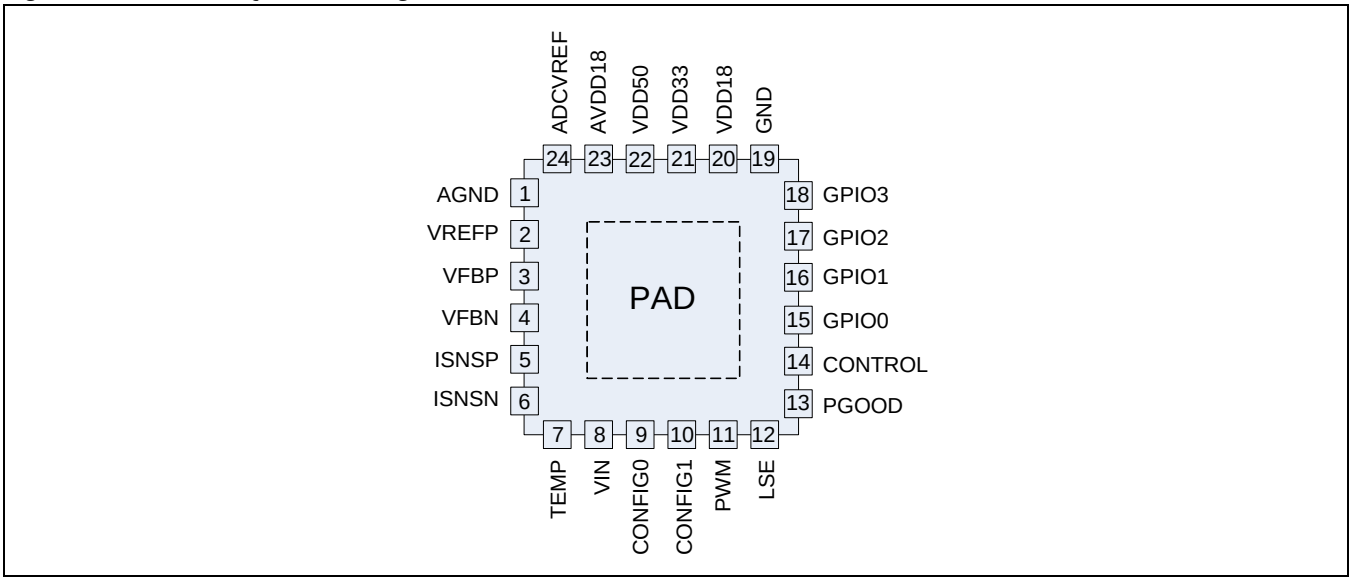


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2.4. Available Packages

The ZSPM1005 is available in a 24-pin QFN package. The pin-out is shown in Figure 2.4. The mechanical drawing of the package can be found in Figure 4.1.

Figure 2.4 Pin-out QFN24 Package



3 Functional Description

3.1. Power Supply Circuitry, Reference Decoupling, and Grounding

The ZSPM1005 incorporates several internal power regulators in order to derive all required supply and bias voltages from a single external supply voltage. This supply voltage can be either 5V or 3.3V depending on whether the internal 3.3V regulator should be used. If the internal 3.3V regulator is not used, 3.3V must be supplied to the 3.3V and 5V supply pins. Decoupling capacitors are required at the VDD33, VDD18, and AVDD18 pins (1.0µF minimum; 4.7µF recommended). If the 5.0V supply voltage is used, i.e., the internal 3.3V regulator is used, a small load current can be drawn from the VDD33 pin. This can be used to supply pull-up resistors, for example.

The reference voltages required for the analog-to-digital converters are generated within the ZSPM1005. External decoupling must be provided between the VREFP and ADCVREF pins. Therefore, a 4.7µF capacitor is required at the VREFP pin, and a 100nF capacitor is required at the ADCVREF pin. The two pins should be connected with approximately 50Ω resistance in order to provide sufficient decoupling between the pins.

Three different ground connections are available on the outside of the package. These should be connected together to a single ground tie. A differentiation between analog and digital ground is not required.

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3.2. Reset/Start-up Behavior

The ZSPM1005 employs an internal power-on-reset (POR) circuit to ensure proper start up and shut down with a changing supply voltage. Once the supply voltage increases above the POR threshold voltage (see section 1.3), the ZSPM1005 begins the internal start-up process. Upon its completion the device is ready for operation.

3.3. Digital Power Control

3.3.1. Overview

The digital power control loop consists of the integral parts required for the control functionality of the ZSPM1005. A high-speed analog front-end is used to digitize the output voltage. A digital control core uses the acquired information to provide duty-cycle information to the PWM that controls the drive signals to the power stage.

3.3.2. Switching Frequency

The ZSPM1005 supports the switching frequencies listed in Table 3.1.

Table 3.1 Supported Switching Frequencies

1000 kHz	400.0 kHz
800 kHz	333.3 kHz
666.6 kHz	285.7 kHz
571.4 kHz	266.6 kHz
500.0 kHz	222.0 kHz
444.4 kHz	177.0 kHz

3.3.3. Output Voltage Feedback

The voltage feedback signal is sampled with a high-speed analog front-end. The feedback voltage is differentially measured and subtracted from the voltage reference provided by a reference digital-to-analog converter (DAC) using an error amplifier. A flash ADC is then used to convert the voltage into its digital equivalent. This is followed by internal digital filtering to improve the system's noise rejection.

Although the reference DAC generates a voltage up to 1.44V, keeping the voltage on the feedback pin (VFBP) at approximately 1.20V is recommended to guarantee sufficient headroom. If a larger output voltage is required, an external feedback divider is required.

3.3.4. Digital Compensator

Important: *Section 3.3.4 is proprietary and requires a non-disclosure agreement (NDA) with ZMDI.*

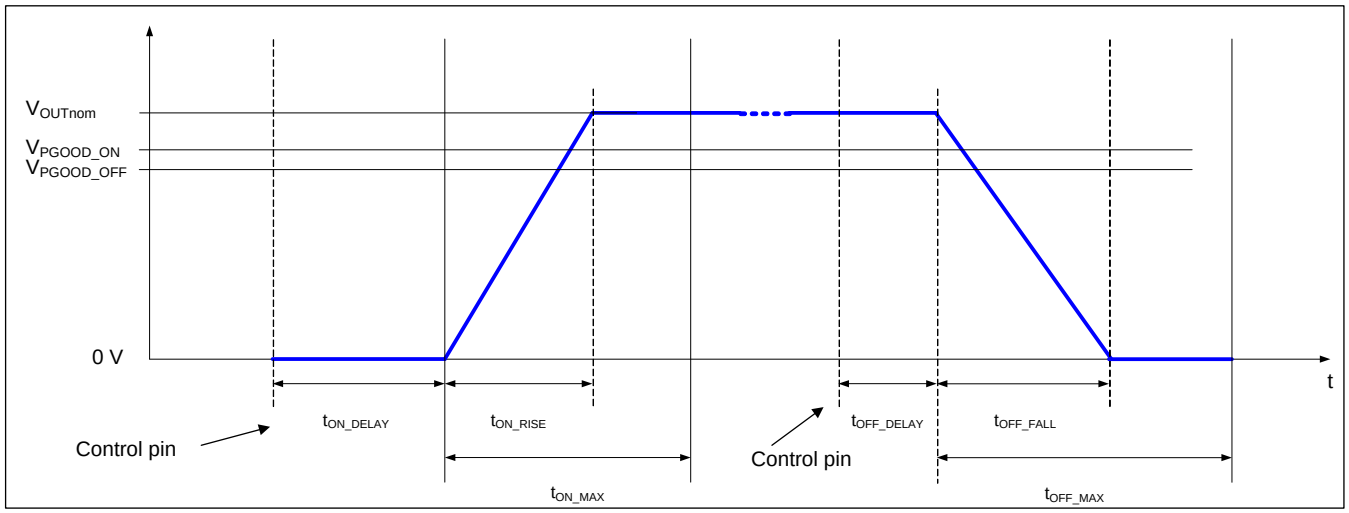
3.3.5. Power Sequencing and the CONTROL Pin

The ZSPM1005 supports power-sequencing features such as programmable ramp up/down and delays. The typical sequence of events is shown in Figure 3.1. The individual values for the delay, ramp time, and post ramp time can be configured. Note that the device is slew-rate controlled for ramping. Hence, when pin-strapping options for the output voltage are used, the ramp time can change based on the configured slew-rate and the actual selected output voltage. The slew rate can be selected in the application using the pin-strap options explained in section 3.7. The CONTROL pin can be configured for active low and active high operation.

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The ZSPM1005 features a power good (PGOOD) output, which can be used to indicate the state of the power rail. If the output voltage level is above the power good value, the pin is set to active, indicating a stable output voltage on the rail. Different levels for turn-on and turn-off are used to enable the use of a hysteresis if desired. Note that the configurable power good thresholds are stored in the device as factors relative to the output voltage. Hence, using the strapping options (section 3.7) to change the output voltage level also changes the PGOOD thresholds.

Figure 3.1 Power Sequencing



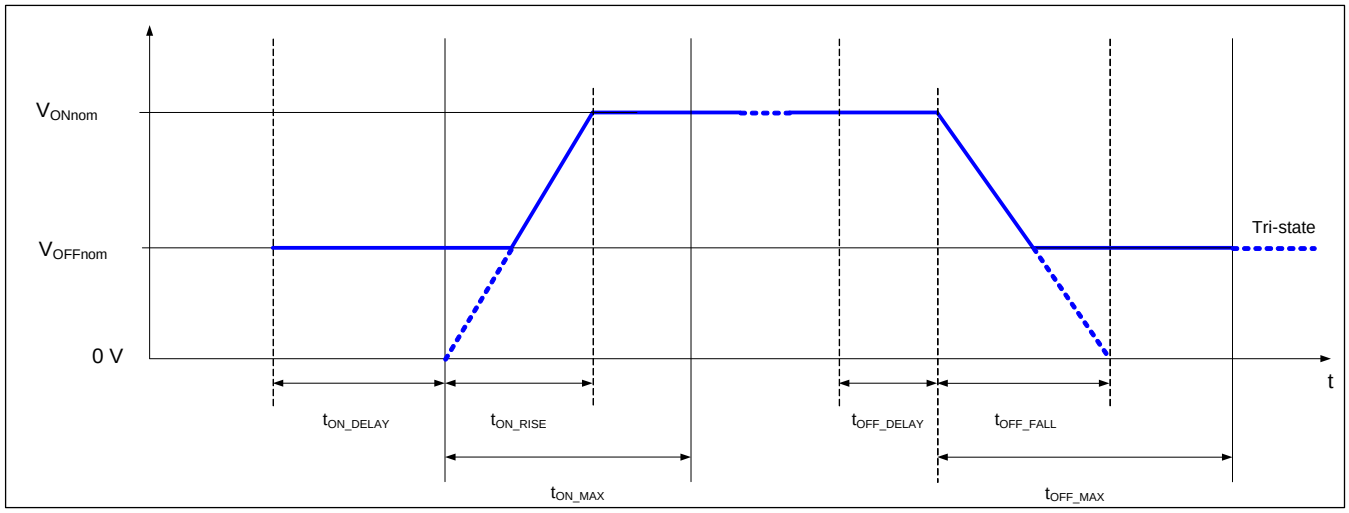
3.3.6. Pre-biased Start-up and Soft Stop

Dedicated pre-biased start-up logic ensures proper start-up of the power converter when the output capacitors are pre-charged to a non-zero output voltage. Closed-loop stability is ensured during this phase.

The ZSPM1005 also supports pre-biased off; i.e., the output voltage is not ramped down to zero and instead remains at a predefined level (V_{OFF_nom}). This value can be configured via the Pink Power Designer™ GUI. After de-assertion of the CONTROL pin, the ZSPM1005 ramps down the value to the predefined value. Once the value is reached, PWM and LSE will be turned off in order to put the output driver into tri-state mode.

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Figure 3.2 Power Sequencing with Non-zero Off Voltage



3.3.7. Current Sensing

Important: *Section 3.3.7 is proprietary and requires a non-disclosure agreement (NDA) with ZMDI.*

3.3.8. Temperature Measurement

The ZSPM1005 features two independent temperature measurement units: internal and external. The internal temperature sensing measures the temperatures inside the ZSPM1005. The external temperature sense element should be placed close to the inductor to measure its temperature. A PN-junction is used as the external temperature sense element. Small-signal transistors, such the 3904, are widely used for this application. The Pink Power Designer™ GUI must be used to enter the sensitivity and the offset for configuration of the external temperature measurement. A temperature calibration is highly recommended.

3.4. Fault Monitoring and Response Generation

The ZSPM1005 monitors various signals during operation. Depending on the selected configuration, it can respond to events generated by these signals. A wide range of options is configurable via the Pink Power Designer™ GUI. Typical monitoring within the ZSPM1005 is a three-step process. First, an event is generated by a configurable set of thresholds. This event is then digitally filtered before the ZSPM1005 reacts with a configurable response. An overview of the fault configuration is given in Table 3.2.

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Table 3.2 Fault Configuration Overview

Signal	Response Type	Delay Resolution	Maximum Delay
Output Over-Voltage Fault	Low impedance*	500µs	90ms
Output Under-Voltage Fault	Low-impedance*	500µs	90ms
Input Over-Voltage Fault	High-Z*	500µs	90ms
Input Under-Voltage Fault	High-Z*	500µs	90ms
Over-Current Fault	Low-impedance*	500µs	90ms
External Over-Temperature Fault	Soft-Off	5ms	900ms
Internal Over-Temperature Fault	Soft-Off	5ms	900ms

*The default options shown can be changed via the Pink Power Designer™ GUI.

The ZSPM1005 supports different response types individually configurable for each fault. The “low-impedance” response turns off the top MOSFET and enables the low-side MOSFET; i.e., PWM=0 and LSE=1. After t_{OFF_MAX} (see Figure 3.2), both MOSFETs will be turned off. A “high-Z” response will disable both MOSFETs instantaneously. A “Soft-Off” response ramps the output voltage down, similar to a power-down operation via the CONTROL pin, to the value selected for V_{OFF_nom}. After t_{OFF_MAX}, the controller will disable the power stage by turning both switches off.

For each fault response, a delay and a retry setting can be configured. If the delay value is set to non-zero, the ZSPM1005 will not respond to a fault immediately. Instead it will delay the response by the configured value and then reassess the signal. If the fault is still present, the appropriate response will be triggered. If the fault is no longer present, the previous detection will be disregarded. The retry setting configures the number of restarts of the power converter after a fault event. This number can be between 0 and 7, where a setting of 7 represents an infinite retry operation. In analog controllers, this feature is also known as “hiccup mode.”

3.4.1. Output Over/Under Voltage

To prevent damage to the load, the ZSPM1005 utilizes an output over-voltage protection circuit. The voltage at VFBP is continuously compared with a configurable threshold using a high-speed analog comparator. If the voltage exceeds the configured threshold, the fault response is generated and the PWM outputs are turned off. The voltage fault level is generated by a 6-bit DAC with a reference voltage of 1.60V resulting in 25mV resolution.

The ZSPM1005 also monitors the output voltage with a lower threshold. If the output voltage falls below the under-voltage fault level, a fault event is generated.

Note that the fault thresholds are stored in the ZSPM1005 as factors relative to the output voltage. Hence, using the strapping options (section 3.7) to change the output voltage level, also changes the fault thresholds.

3.4.2. Output Current Protection

The ZSPM1005 continuously monitors the average inductor current and utilizes this information to protect the power supply against excessive output current. A configurable maximum output current fault threshold can be used to shut down the ZSPM1005.

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3.4.3. Over-Temperature Protection

The ZSPM1005 monitors internal and external temperature. For each, a fault level can be configured and an appropriate response can be enabled.

3.5. Pin Configuration

The ZSPM1005 offers a flexible configuration scheme for its digital output pins. This enables using the LSE (low-side FET control signal) and GPIO0 pin (general purpose input/output) with different functions depending on the application requirements. The configuration options are listed in Table 3.3.

Table 3.3 Pin Configuration Overview

Pin	LSE	Thermal Shutdown	Driver Disable	Hardwire Option
LSE	Active high		High and low active	High and low active
GPIO0		High and low active	High and low active	

In LSE mode, the LSE pin is used as an SMOD signal to actively modulate the low-side FET of the power stage. Alternatively, it can be used as a control signal in order to enable/disable the driver. This signal is deasserted prior to the first switching on the PWM pin and asserted shortly after the last switching event. If the pin is not used in the application, a hardwire option can be used to set the pin to a defined level.

While the GPIO0 pin supports the driver disable feature, it can also be used as a thermal shutdown input. If the pin is asserted by an external source, e.g., the thermal shutdown flag of a DrMOS, the controller flags an external over-temperature fault and reacts accordingly.

Note that if the GPIO pin is configured as the driver disable, the LSE pin must be configured with the LSE feature.

3.6. Configuration and Engineering Mode

Important: *Section 3.6 is proprietary and requires a non-disclosure agreement (NDA) with ZMDI.*

3.7. Pin Strap Options

The ZSPM1005 supports multiple sets of configuration options that allow the user to employ two simple resistors to select various options from user-configured look-up tables that are stored in the nonvolatile memory (NVM).

The Pink Power Designer™ GUI is used to define the tables and store them in NVM. For the end user, the configuration is dramatically simplified by using the pin strap features to select the following parameters:

- Output Voltage
- Compensation
- Over-Current Protection Threshold
- Ramp-up Time

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The CONFIG0 and CONFIG1 pins are used to determine the index of the selected values using the resistor values listed in Table 3.4. Each pin is configured for either the E12 series of resistor values, which provides 15 options for index values, or for the E96 series, which provides 30 index values. A resistor variation of ~2% is taken into account for initial tolerance and temperature dependency. The values are read during the initialization phase and then used to look up the selected values from the user-configured look-up tables. The user can freely correlate the two configuration pins with the four parameters to choose the optimal configuration options for the desired application. A total of four compensation settings and 30 values for each of the other parameters are available.

Table 3.4 Pin Strap Resistor Values

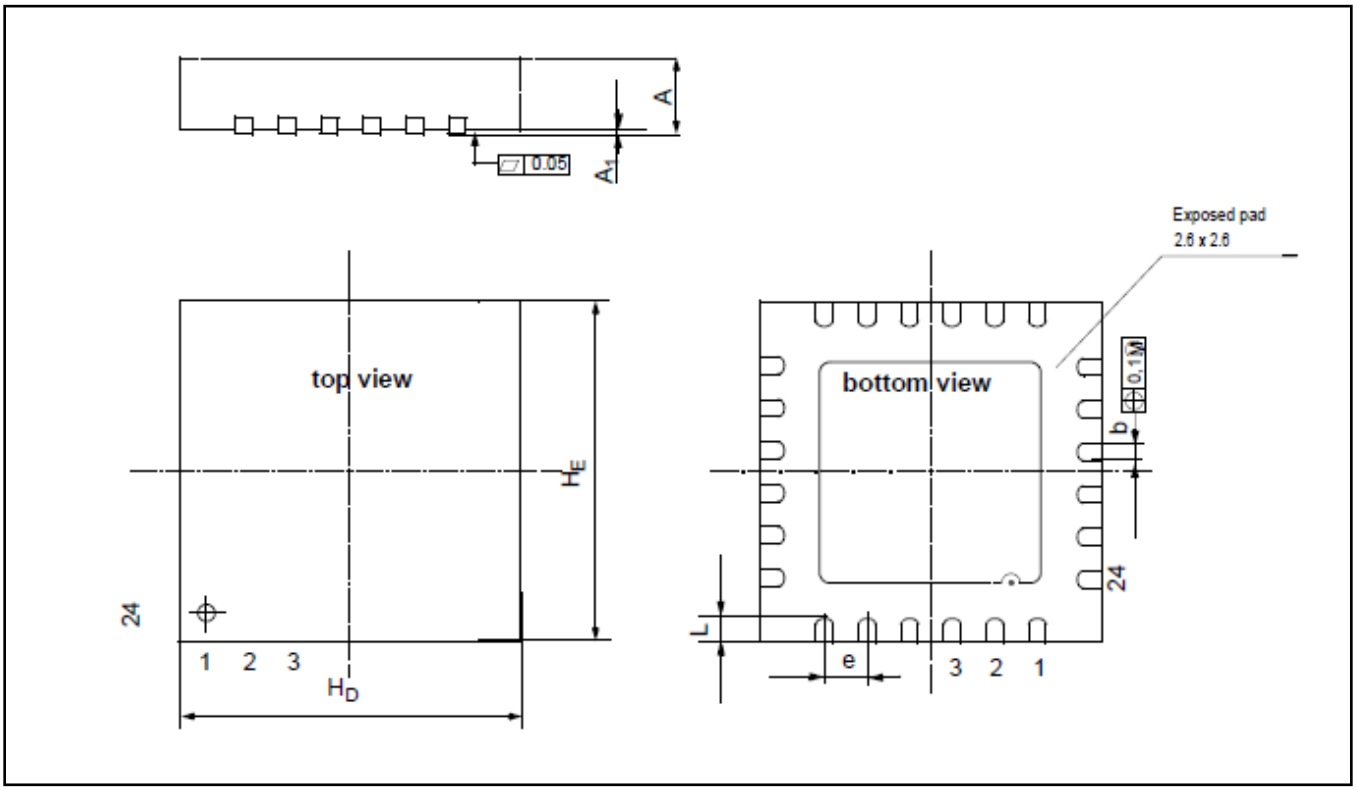
Index	Resistor Value Using the E12 Series	Resistor Value Using the E96 Series
0	0Ω	0Ω
1	680Ω	392Ω
2	1.2 kΩ	576Ω
3	1.8kΩ	787Ω
4	2.7kΩ	1.000kΩ
5	3.9kΩ	1.240kΩ
6	4.7kΩ	1.500kΩ
7	5.6kΩ	1.780kΩ
8	6.8kΩ	2.100kΩ
9	8.2kΩ	2.430kΩ
10	10kΩ	2.800kΩ
11	12kΩ	3.240kΩ
12*	15kΩ	3.740kΩ
13	18kΩ	4.220kΩ
14	22kΩ	4.750kΩ
15	N. A.	5.360kΩ
16	N. A.	6.040kΩ
17	N. A.	6.810kΩ
18	N. A.	7.680kΩ
19	N. A.	8.660kΩ
20	N. A.	9.530kΩ
21	N. A.	10.50kΩ
22	N. A.	11.80kΩ
23	N. A.	13.00kΩ
24	N. A.	14.30kΩ
25	N. A.	15.80kΩ
26	N. A.	17.40kΩ
27	N. A.	19.10kΩ
28	N. A.	21.00kΩ
29	N. A.	23.20kΩ

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4 Mechanical Specifications

Based on JEDEC MO-220. All dimensions are in millimeters.

Figure 4.1 24-pin QFN Package Drawing



Dimension	Min (mm)	Max (mm)
A	0.8	0.90
A_1	0.00	0.05
b	0.18	0.30
e	0.5 nominal	
H_D	3.90	4.1
H_E	3.90	4.1
L	0.35	0.45

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5 Glossary

Term	Description
ASIC	Application Specific Integrated Circuit
DPWM	Digital Pulse-Width Modulator
DCR	DC Resistance
DSP	Digital Signal Processing
FET	Field-Effect Transistor
FPGA	Field-Programmable Gate Array
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
HKADC	Housekeeping Analog-To-Digital Converter
NVM	Non-volatile Memory
OT	Over-Temperature
OTP	One-Time Programmable Memory
OV	Over-Voltage
PID	Proportional/Integral/Derivative
SCR	Sub-cycle Response™
SLC	State-Law Control™
SMOD	Skip Mode
SPM	Smart Power Management

6 Ordering Information

Product Sales Code	Description	Package
ZSPM1005ZA1R 0	ZSPM1005 Lead-free QFN24 — Temperature range: -40°C to +125°C	Reel

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7 Related Documents

Note: “RevX_xx” refers to the current revision of the document.

Document	File Name
ZSPM1005 Feature Sheet	*ZSPM1005_Data_Sheet_RevX_xx.pdf*
Pink Power Designer™ Graphic User Interface (GUI) for the ZSPM1005	*PinkPowerDesigner_UserMan_ZSPM1005_Rev_X_xy.pdf*
ZSPM10xx Application Note—Programming and Calibration	*ZSPM10xx_Calibration_Procedures_RevX_xx.pdf*

Visit ZMDI’s website www.zmdi.com or contact your nearest sales office for the latest version of these documents.

8 Document Revision History

Revision	Date	Description
1.00	June 21, 2013	First release.

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