LPC TO ISA BRIDGE SET

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1. GENERAL DESCRIPTION

W83626F/W83626D/W83626G is a transparent LPC-to-ISA bus conversion IC.

For the new generation Intel chipset Camino and Whitney, SiS Super South 960, featuring LPC bus, there is no support for ISA bus and slots. However, the demand of ISA devices still exists. For such case, W83626F/G is the best companion solution for the non-ISA chipset. Also the packages of W83626F/G had been chosen to be the most economic solution for save the M/B board layout size and cost.

For the new generation chipset featuring LPC interface and support no ISA bus, W83627HF/HG (Winbond LPC I/O) together with the set of W83626F/G is the complete solution.

2. FEATURES

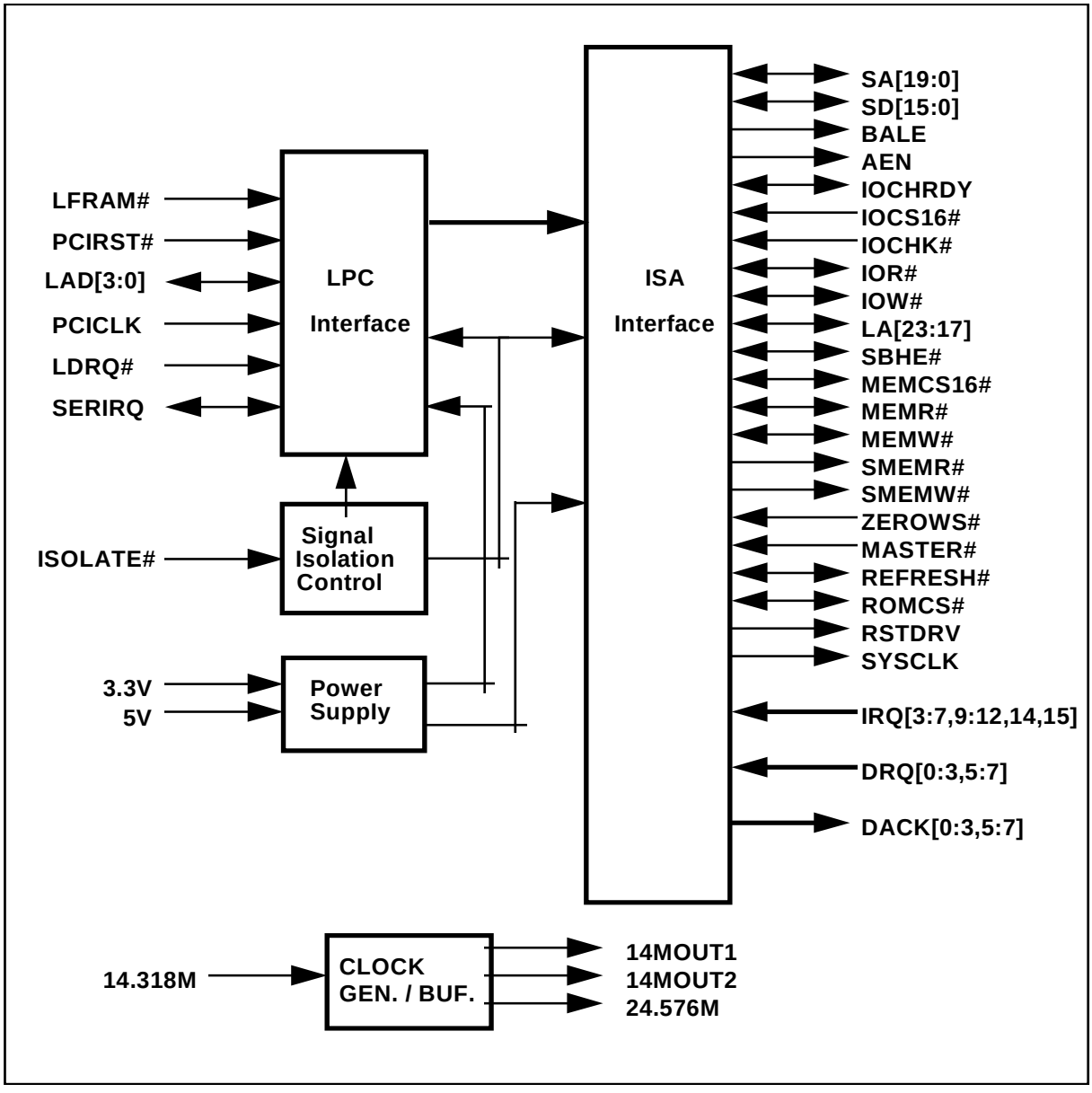
LPC to ISA Bridge

- Meet LPC Spec. 1.1
- Support LDRQ# (LPC DMA), SERIRQ (serial IRQ)
- Full ISA Bus Support except ISA Bus Masters, 16 bit I/O and Memory R/W
- 5V ISA and 3.3V LPC interfaces
- All Software Transparent
- IRQ Serializer for ISA Parallel IRQ transfer to Serial IRQ
- Supports 3 fully ISA Compatible Slots without Buffering
- LPC Bus at 33MHz
- Supports Programmable ISA Bus Divide the PCI Clock into 3 or 4
- All ISA Signals can be Isolated
- 14.318MHz in to generate two 14.318MHz buffer out and one 24.576MHz
- Specific Keyboard Functions supported
- Support 8 programmable general purpose I/O pins
- Supports Configuration registers for programming performance

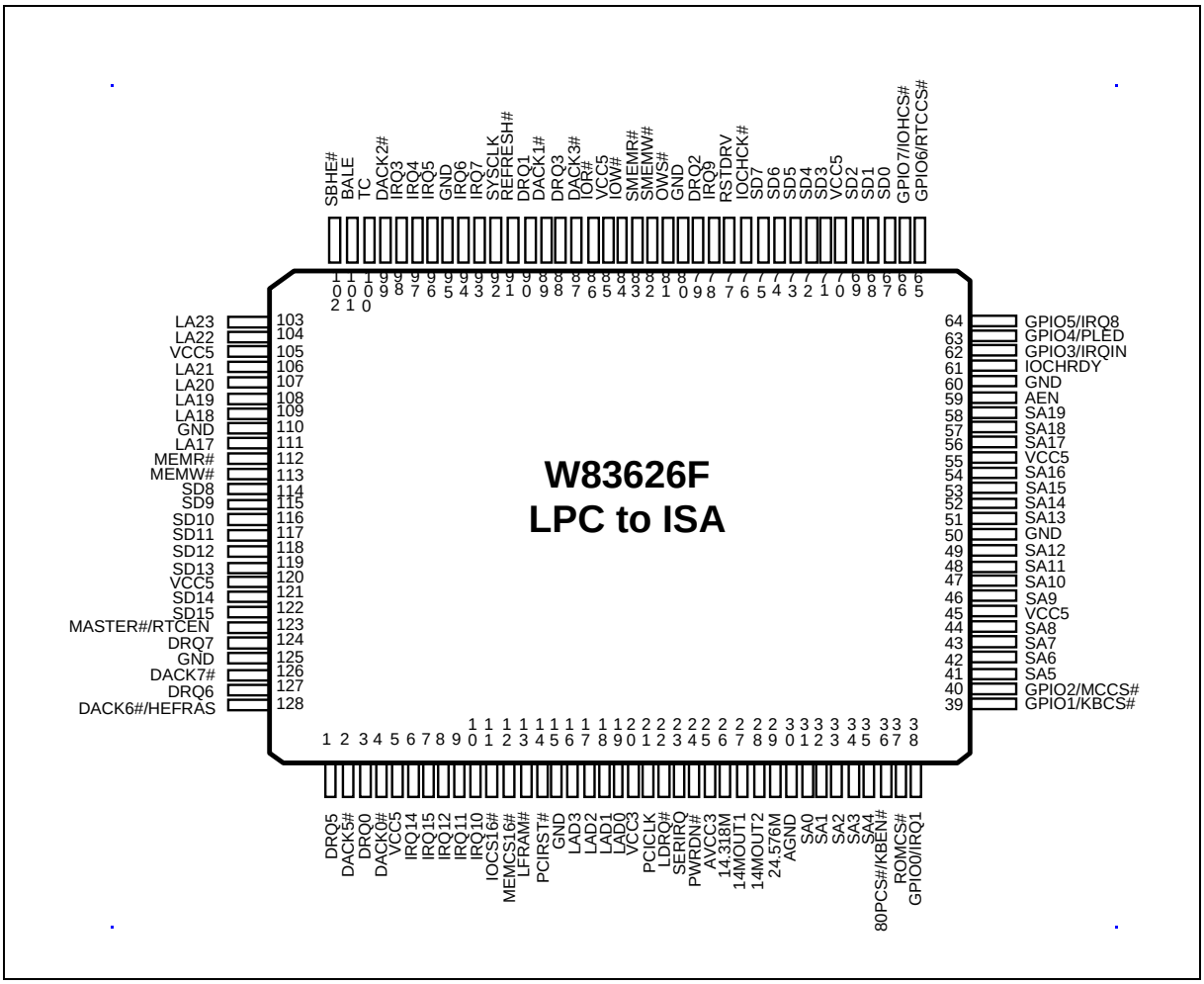
Package

- 128-pin PQFP for W83626F

3. BLOCK DIAGRAM OF W83626F/G



4. PIN CONFIGURATION OF W83626F/G



5. PIN DESCRIPTION

I/O12t - TTL level bi-directional pin with 12 m A source-sink capability
I/O24t - TTL level bi-directional pin with 24 m A source-sink capability
I/O12tp3 - 3.3V TTL level bi-directional pin with 12 m A source-sink capability
I/O24tp3 - 3.3V TTL level bi-directional pin with 24 m A source-sink capability
I/OD12t - TTL level bi-directional pin open drain output with 12 m A sink capability
I/O24t - TTL level bi-directional pin with 24 m A source-sink capability
OUT12 - TTL level output pin with 12 m A source-sink capability
OUT24 - TTL level output pin with 24 m A source-sink capability
O12p3 - 3.3V TTL level output pin with 12 m A source-sink capability
O24p3 - 3.3V TTL level output pin with 24 m A source-sink capability
OD12 - Open-drain output pin with 12 m A sink capability
OD24 - Open-drain output pin with 24 m A sink capability
INcs - CMOS level Schmitt-trigger input pin
INt - TTL level input pin
INtd - TTL level input pin with internal pull down resistor
INtu - TTL level input pin with internal pull up resistor
INts - TTL level Schmitt-trigger input pin
INtsp3 - 3.3V TTL level Schmitt-trigger input pin

5.1 W83626F/G PIN DESCRIPTION

5.1.1 LPC Interface

SYMBOL	PIN	I/O	FUNCTION
LAD[3:0]	16-19	I/O12tp3	These signal lines communicate address, control and data information over the LPC bus between a host and a peripheral.
LFRAME#	13	INtsp3	Indicates start of a new cycle or termination of a broken cycle.
PCICLK	21	INt	PCICLK provides timing for all transactions on the LPC bus. All LPC signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge.
PCIRST#	14	INtsp3	Reset signal. It can connect to PCIRST# signal on the host.
SERIRQ	23	I/OD12t	Serial IRQ Input/Output.
LDRQ#	22	O12tp3	Encoded DMA Request signal.
PWRDN#	24	INtu	Power Down. The signal is active low according to CR 44 Bit 7and wake-up enable by hardware setting. There are eight different power-down states (Power down Mode 3).

5.1.2 ISA Interface Signals

SYMBOL	PIN	I/O	FUNCTION
SA[19:17]	58-56	OUT_{24}	**System Address Bus.** These are the upper address lines that define the ISA's byte granular address space (up to 1 M byte). SA [19:17] are at an unknown state upon PCIRST#.
SA[16:0]	54-51 49-46 44-41 35-31	I/O24t	**System Address Bus.** These are the bi-directional lower address lines that define the ISA's byte granular address space (up to 1 M byte). SA [16:0] is at an unknown state upon PCIRST#.
SD[15:0]	122-121 119-114 75-71 69-67	I/O_{24t}	**System Data.** SD [15:0] provides the 16-bit data path for devices residing on the ISA Bus. W83626F/G tri-states SD [15:0] during PCIRST#.
AEN	59	OUT_{24}	**Address Enable.** AEN is asserted during DMA cycles. This signal is also driven high during W83626F/G initiated refresh cycles. AEN is driven low upon PCIRST#.
IOR#	86	I/O24t	**I/O Read.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD [15:0]).
IOW#	84	I/O24t	**I/O Write.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD [15:0]).
IOCHRDY	61	I/O24t	**I/O Channel Ready.** Resources on the ISA Bus negate IOCHRDY to indicate that additional time (wait states) is required to complete the cycle.
SYSCLK	92	OUT_{24}	**ISA System Clock.** SYSCLK is the reference clock for the ISA bus. The SYSCLK is generated by dividing PCICLK by 3 or 4.
RSTDRV	77	OUT_{24}	**Reset Drive.** W83628F asserts RSTDRV to reset devices that reside on the ISA Bus. The W83628F asserts this signal while the PCIRST# is asserted.
IOCS16#	11	IN_t	**16-bit I/O Chip Select.** This signal is driven by I/O devices on the ISA Bus to indicate that they support 16-bit I/O bus cycles.
MEMCS16#	12	IN_t	**Memory Chip Select 16.** MEMCS16# asserted indicates that the memory slave supports 16-bit accesses.
IOCHCK#	76	IN_t	**I/O Channel Check.** IOCHK# can be driven by any resource on the ISA bus during on detection of an error.

ISA Interface Signals, continued

SYMBOL	PIN	I/O	FUNCTION
OWS#	81	IN_t	**Zero Wait States.** An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be executed as an ISA zero wait state cycle. ZEROWS# has no effect during 16-bit I/O cycles.
LA[23:17]	103-104 106-109 111	I/O24t	**Unlatched Address.** The LA [23:17] address lines are bi-directional. These address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA [23:17] are outputs when the W83628F owns the ISA Bus.
SMEMW#	82	OUT_{24}	**Standard Memory Write.** SMEMW# asserted indicates the current ISA bus cycle is a memory write cycle to an address below 1 Mbyte.
SMEMR#	83	OUT_{24}	**Standard Memory Read.** SMEMR# asserted indicates the current ISA bus cycle is a memory read cycle to an address below 1 Mbyte.
REFRESH#	91	OUT_{24}	**Refresh.** REFRESH# asserted indicates that a refresh cycle is in progress, or that an ISA master is requesting W83626F/G to generate a refresh cycle. Upon PCIRST#, this signal is tri-stated.
BALE	101	OUT_{24}	**Bus Address Latch Enable.** BALE is an active high signal asserted by the W83626F/G to indicate that the address (SA [19:0], LA [23:17]) and SBHE# signal lines are valid. The LA [23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. BALE is driven low upon PCIRST#.
SBHE#	102	OUT_{24}	**System Byte High Enable.** SBHE# asserted indicates that a byte is being transferred on the upper byte (SD [15:8]) of the data bus. SBHE# is at an unknown state upon PCIRST#.
MEMR#	112	I/O24t	**Memory Read.** MEMR# asserted indicates the current ISA bus cycle is a memory read.
MEMW#	113	I/O24t	**Memory Write.** MEMW# asserted indicates the current ISA bus cycle is a memory write.
MASTER# RTCEN#	123	IN_t	**MASTER#.** This signal is used with a DREQ line by an ISA master to gain control of the ISA Bus. RTC Function Enable. The pin applies a pull-down resistor (4.7K ohm) to enable RTC functions (RTCCS#, and IRQ8)
IRQ3	98	IN_t	Parallel Interrupt Requested Input 3.
IRQ4	97	IN_t	Parallel Interrupt Requested Input 4.

ISA Interface Signals, continued

SYMBOL	PIN	I/O	FUNCTION
IRQ5	96	IN_t	Parallel Interrupt Requested Input 5.
IRQ6	94	IN_t	Parallel Interrupt Requested Input 6.
IRQ7	93	IN_t	Parallel Interrupt Requested Input 7.
IRQ9	78	IN_t	Parallel Interrupt Requested Input 9.
IRQ10	10	IN_t	Parallel Interrupt Requested Input 10.
IRQ11	9	IN_t	Parallel Interrupt Requested Input 11.
IRQ12	8	IN_t	Parallel Interrupt Requested Input 12.
IRQ14	6	IN_t	Parallel Interrupt Requested Input 14.
IRQ15	7	IN_t	Parallel Interrupt Requested Input 15.
DRQ0	3	IN_t	**DMA Request 0.** The DREQ signal indicates that either a slave DMA device is requesting DMA services, or an ISA bus master is requesting use of the ISA bus.
DRQ1	90	IN_t	DMA Request 1.
DRQ2	79	IN_t	DMA Request 2.
DRQ3	88	IN_t	DMA Request 3.
DRQ5	1	IN_t	DMA Request 5.
DRQ6	127	IN_t	DMA Request 6.
DRQ7	124	IN_t	DMA Request 7.
DACK0#	4	OUT_{24}	**DMA Acknowledge 0.** The DACK# signal indicates that either a DMA channel or an ISA bus master has been granted the ISA bus.
DACK1#	89	OUT_{24}	DMA Acknowledge 1.
DACK2#	99	OUT_{24}	DMA Acknowledge 2.
DACK3#	87	OUT_{24}	DMA Acknowledge 3.
DACK5#	2	OUT_{24}	DMA Acknowledge 5.
DACK6# HERFRA	128	I/O_{D24t}	DMA Acknowledge 6. During power-on reset, this is pulled-hi internally (Select 4Eh) and is defined as HEFRAS which provides the power-on value for CR3 bit4. A 4.7k ohm is recommended if intends to pull down. (Select 2Eh)
DACK7#	126	OUT_{24}	DMA Acknowledge 7.
TC	100	OUT_{24}	**Terminal Count.** The W83628F asserts TC to DMA slaves as a terminal count indicator.

5.1.3 K/B, GPIO AND 80h PCS# Function

SYMBOL	PIN	I/O	FUNCTION
80PCS# KBEN#	36	I/OD12t	**80h PORT Chip Select.(Default)** **Only decode IO address port 80h and must apply with IOW#.** K/B Functions Enable. During power-on reset this pin is weak pulled-up internally. The pin applied a pull-down resistor (4.7K ohm) to enable K/B functions. (IRQ1,KBCS#,and MCCS#)
ROMCS#	37	I/OD12t	ROMCS#, this pin enable positive decoder of BIOS address range [depend on CR03, bit 1 or external weak pulled-up during PCIRST is asserted].
GPIO0 IRQ1	38	I/OD12t	General purpose I/O pin 0. Parallel Interrupt Requested Input 1. This interrupt request is used for specific K/B functions.
GPIO1 KBCS#	39	I/O12t	General purpose I/O pin 1. Decode the address 60h and 64h to output chip selected signal. Enable by KBEN# power-on setting.
GPIO2 MCCS#	40	I/OD12t	General purpose I/O pin 2. Decode the address 62h and 66h to output chip selected signal Enable by KBEN# power-on setting
GPIO3 IRQIN	62	I/OD12t	General purpose I/O pin 3. Programmable parallel IRQ input transfers to serial IRQ Enable by KBEN# power-on setting
GPIO4 PLED	63	I/OD12t	General purpose I/O pin 4. Power LED output, this signal is low after system reset.
GPIO5 IRQ8	64	I/OD12t	General purpose I/O pin 5. Parallel Interrupt Requested Input 8. This interrupt request is used for specific RTC functions. Enable by RTCEN# power-on setting
GPIO6 RTCCS#	65	I/OD12t	General purpose I/O pin 6. Decode the address 70h and 71h to output chip selected signal Enable by RTCEN# power-on setting
GPIO7 IOHCS#	66	I/OD12t	General purpose I/O pin 7. Decode SA [15-11] is all 0 and setting by CR04 Bit 6.

5.1.4 Clock Buffer and Generator

SYMBOL	PIN	I/O	FUNCTION
14.318M	26	IN_t	Main 14.318 MHz Clock Input.
14MOUT 1	27	$OUT12t$	14.318 MHz Buffer Output 1.
14MOUT 2	28	$OUT12t$	14.318 MHz Buffer Output 2.
24.576M 25.000M	29	$OUT12t$	This pin is weak pull-up during 3 V_{DD} ramp-up period. The default setting is 24.576 MHz and selected 25.000 MHz by external pull-down with 4.7K ohm (recommended) during power ramp-up period. 24.576 MHz Clock Output for Audio Codec or selected 25.000 MHz Clock Output for LAN on board solution.

5.1.5 Power Signals

SYMBOL	PIN	I/O	FUNCTION
VCC5	5, 45, 55, 70, 85, 105, 120,	PWR	**Digital 5V Supply.**
VCC3	20	PWR	**Digital 3.3V Supply.**
GND	15, 50, 60, 80, 95, 110, 125	PWR	**Digital Ground.**
AVCC3	25	PWR	**Analog 3.3V Supply.**
AGND	30	PWR	**Analog Ground.**

5.1.6 Power-on strapping Signals

SYMBOL	PIN	I/O	FUNCTION
80PCS#/KBEN#	36	I/O_{D12t}	**Power-on strapping with pulled-down register will enable K/B and mouse functions. When it is set, pin 38, 39 and 40 will do IRQ1, KBCS# and MCCS# signals.**
ROMCS#	37	I/O_{D12t}	**If there is a boot-ROM (BIOS), the signal must power-on with a weak pulled-high register.**
MASTER/RTCEN#	123	IN_t	**Power-on strapping with pulled-down register will enable RTC functions. When it is set, pin 64 and 65 will do IRQ8 and RTCCS# signals.**
DACK6#/HEFRAS	128	I/O_{D24t}	**Set this function will change the port that is used to access configuration-registers. Default setting is 4Eh, but by power-on strapping with a pulled-down register change to 2Eh.**

6. CONFIGURATION REGISTER

6.1 1 Chip (Global) Control Register

Enable the following configuration registers by writing 26h to the location 4Eh twice.

Change the location to 2Eh by setting bit4 of CR03 or power-on strapping with a pulled-down register on pin 128.

CR03 (ROM Decoder Register, Default, 100011s0b)

Bit 7-5 Reserved.

Bit4 Configure Address and Value

= 0 Write 26h to the location 4E twice. (4Eh and 4Fh are index and data port)

= 1 Write 26h to the location 2E twice (By DACK6 power-on setting with weak pull-down resistor).(The pair are 2Eh and 2Fh)

Bit 3-2 BIOS Decode Range of High Memory.

= 00 1MB BIOS ROM positive decode.

= 01 2MB BIOS ROM positive decode.

= 10 4MB BIOS ROM positive decode.

= 11 8MB BIOS ROM positive decode. (Default setting)

Bit 1 BIOS ROM decoder Enable.

= 0 Disable BIOS ROM decoder. (Default setting)

=1 Enable BIOS ROM decoder.

Bit 0 BIOS Protected Mode.

=0 BIOS Write Disable. (Default setting)

=1 BIOS Write Enable.

This bit set to "1" for updated BIOS used allow Memory R/W to the range of BIOS decoded. This bit is always set to "0" after reset.

CR04 (GPIO Status Register, Default 0ss00sssb)

If the GPIO is selected GPIO function, it will be controlled by CR10, 13, 14, 15, and 16.The pins were set non-GPIO functions by power-on setting pin or software programmed.

Bit 7(GPIO7): = 1 Signal used as IOHCS# (Set by software only)
= 0 Signal used as GPIO function (Default)

Bit 6 (GPIO6): = 1 Signal used as RTCCS# (Set by pin123 RTCEN#)
= 0 Signal used as GPIO function (Default)

Bit 5 (GPIO5): = 1 Signal used as IRQ8 (Set by Pin 123 RTCEN#)
= 0 Signal used as GPIO function (Default)

Bit 4 (GPIO4): = 1 Signal used as PLED (Set by software only and programmed by CR CR17 bit [5, 4])
= 0 Signal used as GPIO function. (Default)

Bit 3 (GPIO3): = 1 Signal used as IRQIN (depended on CR17 bit [3, 0])
= 0 Signal used as GPIO function (Default)

Bit 2 (GPIO2): = 1 Signal used as MCCS# (decode address 62h and 66h)
By Pin 36 KBEN# power-on setting
= 0 Signal used as GPIO function (Default)

Bit 1 (GPIO1): = 1 Signal used as KBCS# (decode address 60h and 64h)
By Pin 36 KBEN# power-on setting
= 0 Signal used as GPIO (Default)

Bit 0 (GPIO0): = 1 Signal used as IRQ1 by Pin 36 KBEN# power-on setting
= 0 Signal used as GPIO (Default)

CR05 (System Clock Register, Default 0x4D)

Bit 7 SYSCLK Divider

= 0 SYSCLK is equal to PCICLK divided by 4.
= 1 SYSCLK is equal to PCICLK divided by 3.

Bit 6 8-bit I/O Recovery Enable

= 0 Disable bit [5:3] setting and uses 3.5 SYSCLKs for 8 bit I/O recovery time.
= 1 Enable bit [5:3] setting.

Bit 5:3 **8-bit I/O Recovery Times**

When bit 6= 1, these 3 bits field define the additional number of SYSCLKs added to standard 3.5 SYSCLK recovery time for 8 bit I/O

= 000 0 SYSCLK
= 001 1 SYSCLK
= 010 2 SYSCLKs
= 011 3 SYSCLKs
= 100 4 SYSCLKs
= 101 5 SYSCLKs
= 110 6 SYSCLKs
= 111 7 SYSCLKs

Bit 2 = 0 Ignore bits [1:0] setting and uses 3.5 SYSCLKs for 16-bit I/O recovery time.
= 1 The 16-bit I/O recovery time is decided by bits 1:0.

Bit 1:0 **16-bit I/O Recovery Times.**

When bit 2 = 1 , this 2-bit field defines the additional number of SYSCLKs added to standard 3.5 SYSCLK recovery time for 16 bit I/O

= 01 1 SYSCLK
= 10 2 SYSCLKs
= 11 3 SYSCLKs
= 00 4 SYSCLKs

CR10 (GPIO0-GPIO7 Function Enable Register, Default 0x00)

Bit 7 - 1: Reserved.

Bit 0: **GPIO Function Activity.**

= 1 All GPIO functions are activated. All registers (CR 11, 12, 13, 14, 15, 16) about GPIO function will be set default value .

= 0 All GPIO functions are inactive except the signals by power-on setting.

If any one of CR04 bit [7, 0] was set non-GPIO function, the bit just affect set GPIO function .

CR11, CR12 (Reserved Register for GPIO Control without Configure Mode Entry)

The register is programmable when the bit 0 of CR10 is set to "1 "and affected by the settings of CR14 (I/O Selection) and CR16 (Inversion).

User defines port address to control GPIO functions. To control GPIO state without entry configure mode. SA [0..7] can be defined on the bit [0..7] of CR11 and SA [8..15] on the bit [0..7] of CR12.

For example:

Define address 50h in CR11 and 01h in CR12 after reset.

bit 0= -GPIO0 (=0 low state,

=1 Hi state)

bit 1=-GPIO1 (=0 low state

=1 Hi state)

,bit 2=GPIO2,.....,bit 7=GPIO7 the same definition as bit 0.

Set CR14 to "00h "(output port) and CR16 to " 00h " (incoming/outgoing)

-o 150 aa ------(10101010) b indicated GP7,GP5,GP3 and GP1 are Hi state.

-o 150 55 ------(01010101) b indicated GP6,GP4,GP2,and GP0 are Hi state.

- i 150 ------show all states of GPIO[7..0]

CR13 (GPIO0-GPIO7 Address Decoder Rester, Default 0x00)

The register is programmable when the bit 0 of CR10 is set to " 1 ".

Bit 7: **Address Decoder 2**

=1 Enable address decoder .Generate a CS# signal to GPIO port which decided by bit[6..4] ,the specify address in CR34 and CR35 and mask range in CR 33.

=0 Disable address decoder.

Bit 6 -Bit 4: **Address Decoder 2 Output Selection.**

Define which GP port as address decoder depended on CR33, CR34 and CR35.

= 000 Selected GPIO 0 as CS# output

= 001 Selected GPIO 1 as CS# output

= 010 Selected GPIO 2 as CS# output

= 011 Selected GPIO 3 as CS# output

= 100 Selected GPIO 4 as CS# output

= 101 Selected GPIO 5 as CS# output

= 110 Selected GPIO 6 as CS# output

= 111 Selected GPIO 7 as CS# output

Bit 3: **Address Decoder 1**

=1 Enable address decoder. Generate a CS# signal to GPIO port which decided by bit[6..4] ,the specify address in CR31 and CR32 and mask range in CR 30.

=0 Disable address decoder.

Bit 2 -Bit 0: **Address Decoder 1 Output Selection.**

Define which GP port as address decoder depend on CR30,CR31 and CR32.

= 000 Selected GPIO 0 as CS# output
= 001 Selected GPIO 1 as CS# output
= 010 Selected GPIO 2 as CS# output
= 011 Selected GPIO 3 as CS# output
= 100 Selected GPIO 4 as CS# output
= 101 Selected GPIO 5 as CS# output
= 110 Selected GPIO 6 as CS# output
= 111 Selected GPIO 7 as CS# output

CR14 (GPI0-GPIO7 I/O Selection Register, Default 0xFF)

The register is programmable when the bit 0 of CR10 is set to "1 ".

Bit [7..0] are corresponding with GPIO [7..0] .

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CR15 (GPIO0-GPIO7 Data Register, Default 0x00)

The register is programmable when the bit 0 of CR10 is set to "1 ".

Bit [7..0] are corresponding with GPIO [7..0] .

If a port is programmed to be an output port, then its respective bit can be read / written.

If a port is programmed to be an input port, then its respective bit can only be read.

CR16 (GPIO0-GPIO7 Inversion Register, Default 0x00)

The register is programmable when the bit 0 of CR10 is set to "1".

Bit [7..0] are corresponding with GPIO [7..0] .

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CR17 (Power LED & IRQIN Control Register, Default 0x00)

Bit 7 -6: Reserved

Bit 5 -4: =00 Power LED pin is tri-stated.
=01 Power LED pin is driven low.
=10 Power LED pin is a 1Hz toggle pulse with 50 duty cycle.
=11 Power LED pin is a 1/4 Hz toggle pulse with 50 duty cycle.

Bit 3 - 0: These bits select IRQ resource for IRQIN. Four bits transfer the decimal value to octal system. For example: Bit [3..0] = 1001b = 0x9h means IRQ 9 be selected.

Bit [3..0] = 1100b = 0xCh means IRQ12 be selected

CR20 (Chip ID Register 1, Default 0x62)

Bit 7 - 0:DEVIDB7 - DEBIDB0 --> Device ID Bit 7 - Bit 0 = 0x 62(read only).

CR21 (Chip ID Register 2, Default 0x6x)

Bit 7 - 0: DEVREVB7 - DEBREVB0 --> Device Rev Bit 7 - Bit 0 = 0x61(read only).

Bit [3..0] indicate the version of the chip.

CR30 (Mask Range of Address Decoder 1 Register, Default 0x00)

This register is used to mask address bits (A7~A0) for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding address bit (A7~A0) is ignore by the specify address decoder.

For example: If the decoding range is 0x3F8 ~ 0x3FF, you can set 0x3F8 to CR 31, 32 and 07h to CR30.

CR31, 32 (Address Decoder 1 Specification Register, Default 0x00)

This register contains the address for specify decoder.

CR 31 Bit [7..0] are used to define low byte of specify address.

CR 32 Bit [7..0] are used to define high byte of specify address.

For example: Decoding address was set to be 0x3F5h and write F5h to CR 31 and 03h to CR 32 .

CR33 ((Mask Range of Address Decoder 2 Register, Default 0x00)

This register is used to mask address bits (A7~A0) for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding address bit (A7~A0) is ignore by the specify address decoder.

For example: If the decoding range is 0x3F8 ~ 0x3FF,you can set 0x3F8 to CR 34, 35 and 07h to CR33 .

CR34, 35 Address Decoder 2 Specification Register, Default 0x00)

This register contains the address for specify decoder.

CR 34 Bit [7..0] are used to define low byte of specify address.

CR 35 Bit [7..0] are used to define high byte of specify address.

For example: Decoding address was set to be 0x3F5h and write F5h to CR34 and 03h to CR35.

This register contains the address for specify decoder.

CR40 (Clock controllable Register, Default 0x00)

This register is used to enable clock power-down state of the chip. It will shut down 14.318MHz.

Bit 7 -1: Reserved.

Bit 0 : =1 Power down mode. When entry power down mode, clock output will be turn off.
=0 Normal used.

CR41 (Clock tested Register, Reserved for Winbond internal test)

CR42 (Tristate controllable Register (Power-down Mode1) , Default 0x1B)

Bit 7: REFRESH Cycles Tristated.

Bit 6: SYSCLK Output Tristated.

Bit 5: Address Signals Tristated Enable.

Bit 4 - 0: Defined tristated address signals range.(See Table 1)

For example:

Define address Bit [4..0] = 0x10h

SA [19..16] and LA [23..17] signals will be tristated.

Table 1

SET VALUE(HEX)	TRI_STATE RANGE	WORKABLE
00	SA[19..0] and LA[23..17]	None one
01	SA[19..1] and LA[23..17]	SA[0]
02	SA[19..2] and LA[23..17]	SA[1..0]
. .	. .	. .
14	LA[23..17]	SA[19..0]
Set value(Hex)	Tri_state range	Workable

Table 1, continued.

SET VALUE(HEX)	TRI_STATE RANGE	WORKABLE
. .	. .	. .
1A	LA[23]	SA[19..0] and LA[22..17]
1B	None one	SA[19..0] and LA[23..17]

CR43 (Tristate controllable Register (Power-down Mode2), Default 0x07)

The Fast mode is used to improve the performance of transferable interface, because some applications will do fast transaction. To set the suitable bits to decide on specify range or all ISA cycles will meet the requested I/O cycles.

Bit 7: Reserved.

Bit 6: = 1 Enable Fast mode by ADDRESS DECODER 2 and SYSCLK is depended on the state of Bit 3 .
= 0 ADDRESS DECORDER 2 doesn't affect Fast Mode and do original operation.

Bit 5: = 1 Enable Fast mode by ADDRESS DECODER 1 and SYSCLK is depended on the state of Bit 3.
= 0 ADDRESS DECORDER 1 doesn't affect Fast Mode and do original operation.

Bit 4: = 1 Enable Fast Mode of whole chip, whole ISA cycle of this bridge will be done Fast Mode operation and SYSCLK is depended on the state of Bit 3.
= 0 Normal operation, just Bit 6 and Bit 5 can affect Fast Mode operation.

Bit 3: = 1 SYSCLK is equal to PCICLK divided by 1 when decoding range is in Fast Mode.
= 0 SYSCLK is equal to PCICLK divided by 2 when decoding range is in Fast Mode.

Bit 2: = 1 Disabled Memory cycles.
= 0 Normal used.

Bit 1: = 1 Forced 16 bit cycles.
= 0 Normal used.

Bit 0: = 1 8-bit data bus decode only. Only SD [7..0] signals are active.
= 0 Normal used.

CR44 (Tristate controllable Register (Power-down Mode3) , Default 0x07)

Bit 7: =1 Enable Power-down functions.(ISOLATE# was power-on setting.)
=0 Normal used.

Bit 6: Reserved.

Bit 5: =1 SA10 is set as mask (ignored) bit in ADDRESS DECODER 2.
The function is used to improved
the performance of ECP mode of LPT.
If the decoding range is 0x378-0x37F and 0x778-0x77F
,you can set this bit to 1 for Fast Mode operation.
= 0 Normal operation.

Bit 4: =1 SA10 is set as mask (ignored) bit in ADDRESS DECODER 1.
The function is used to improved
the performance of ECP mode of LPT.
If the decoding range is 0x378-0x37F and 0x778-0x77F
,you can set this bit to 1 for Fast Mode operation.
= 0 Normal operation.

Bit 3: SERIRQ POWER DOWN SELECT.
=1 When the chip is in power down mode, the SERIRQ block is inactive.
=0 When the chip is in power down mode, the SERIRQ block is active.

Bit 2 -0: Set SYSCLK divided ratio.(2,4,8,16,32,64)
= 000 Disable Power-down Mode3.
= 001 SYSCLK divided by 2.
= 010 SYSCLK divided by 4.
= 010 SYSCLK divided by 4
= 011 SYSCLK divided by 8
= 100 SYSCLK divided by 16
= 101 SYSCLK divided by 32
= 110 SYSCLK divided by 64
= 111 LPC I/F,all clocks and signals will be tristated.

CR45 (Wake-Up Event Register, Default 0x01)

Bit 7: =0 Normal used.
=1 Wake up from power-down mode by IRQ 7 occurred.

Bit 6: =0 Normal used.
=1 Wake up from power-down mode by IRQ 6 occurred.

Bit 5: =0 Normal used.
=1 Wake up from power-down mode by IRQ 5 occurred.

Bit 4: =0 Normal used.
=1 Wake up from power-down mode by IRQ 4 occurred.

Bit 3: =0 Normal used.
=1 Wake up from power-down mode by IRQ 3 occurred.

Bit 2: Reserved.

Bit 1: =0 Normal used.
=1 Wake up from power-down mode by IRQ 1 occurred.

Bit 0: =0 Normal used.
=1 Wake up from power-down mode by rising edge of ISOLATE# signal occurred.

CR46 (Wake-Up Event Register, Default 0x00)

Bit 7 -5: Reserved

Bit 4: =0 Normal used.
=1 Wake up from power-down mode by IRQ 12 occurred.

Bit 3: =0 Normal used.
=1 Wake up from power-down mode by IRQ 11 occurred.

Bit 2: =0 Normal used.
=1 Wake up from power-down mode by IRQ 10 occurred.

Bit 1: =0 Normal used.
=1 Wake up from power-down mode by IRQ 9 occurred.

Bit 0: =0 Normal used.
=1 Wake up from power-down mode by IRQ 8 occurred.

CR48 (DMA CYCLES FAST MODE SELECT, Default 0x00) (Write only)

The Fast mode is used to improve the performance of transferable interface, because some applications will do fast transaction. To set the suitable bits to decide on specify range or all ISA cycles will meet the requested DMA cycles.

Bit 7: = 0 Normal used.
= 1 The DMA cycles of channel 7 is in fast mode.

Bit 6: = 0 Normal used.
= 1 The DMA cycles of channel 6 is in fast mode.

Bit 5: = 0 Normal used.
= 1 The DMA cycles of channel 5 is in fast mode.

Bit 4: Reserved.

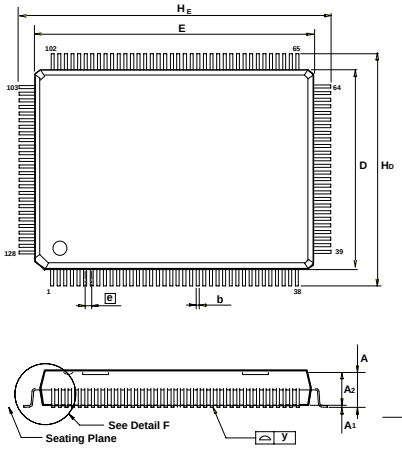
Bit 3: = 0 Normal used.
= 1 The DMA cycles of channel 3 is in fast mode.

Bit 2: = 0 Normal used.
= 1 The DMA cycles of channel 2 is in fast mode.

Bit 1: = 0 Normal used.
= 1 The DMA cycles of channel 1 is in fast mode.

Bit 0: = 0 Normal used.
= 1 The DMA cycles of channel 0 is in fast mode.

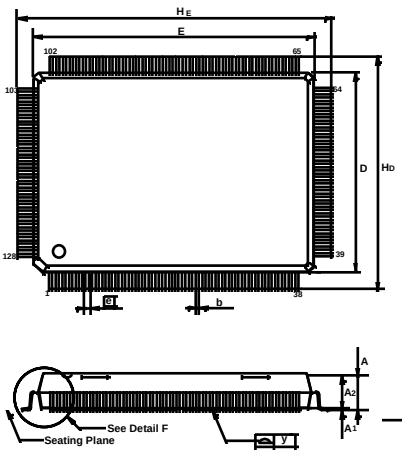
7. PACKAGE DIMENSIONS 1 FOR W83626F (128-PIN PQFP)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	——	0.50	——	—	0.020	—
H_D	17.00	17.20	17.40	0.669	0.677	0.685
H_E	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	——	1.60	——	—	0.063	—
y	——	——	0.08	—	—	0.003
θ	0	——	7	0	—	7

Note:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

8. PACKAGE DIMENSIONS 2 FOR W83626D (128-PIN LQFP)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.05	-----	0.15	0.002	----	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.16	0.23	0.005	0.006	0.009
c	0.10	-----	0.20	0.004	-----	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	-----	0.40 BSC	-----	-----	0.016	-----
H_D	-----	16.00	-----	-----	0.630	-----
H_E	-----	22.00	-----	-----	0.866	-----
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	——	1.00	——	—	0.039	—
y	——	——	0.08	—	—	0.003
θ	0	——	7	0	—	7

Note:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

9. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May 25, 2005	23	ADD Important Notice

Important Notice

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