AT93C46E

3-wire Serial EEPROM
1K (64 x 16)

DATASHEET

Features

- Low-voltage and Standard-voltage Operation
  - V_{CC} = 1.8V to 5.5V
- User-selectable Internal Organization
  - 1K: 64 x 16
- 3-wire Serial Interface
- 2MHz Clock Rate (5.0V)
- Self-timed Write Cycle (5ms Max)
- High Reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead, and TSSOP Packages
- Lead-free/Halogen-free Device

Description

The Atmel® AT93C46E provides 1,024 bits of Serial Electrically-Erasable Programmable Read-Only Memory (EEPROM) organized as 64 words of 16 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT93C46E is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead, and TSSOP packages.

The AT93C46E is enabled through the Chip Select pin (CS) and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output DO pin. The write cycle is completely self-timed, and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the Erase/Write Enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the Ready/Busy status of the part.

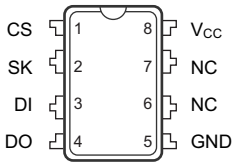
The AT93C46E is available from 1.8V to 5.5V.

1. Pin Descriptions and Pinouts

Table 1-1. Pin Configurations

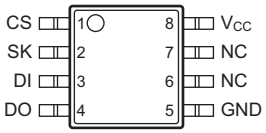
Pin	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
NC	No Connect

8-lead PDIP



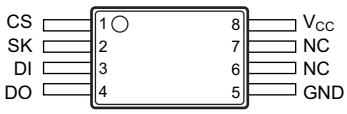
Top View

8-lead SOIC



Top View

8-lead TSSOP



Top View

Note: Drawings are not to scale.

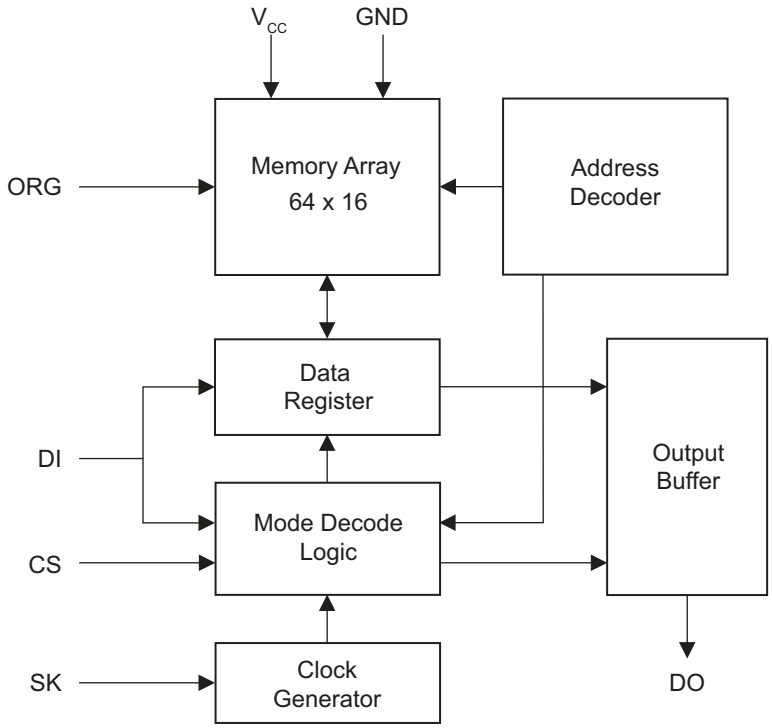
1.1 Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Block Diagram

Figure 2-1. Block Diagram



3. Memory Organization

3.1 Pin Capacitance

Table 3-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = +5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

3.2 DC Characteristics

Table 3-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	Read at 1.0MHz		0.5	2.0	mA
			Write at 1.0MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V	CS = 0V		0.4	1.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V		10.0	15.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1}[1]	Input Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V		-0.6		0.8	V
V_{IH1}[1]	Input High Voltage			2.0		V_{CC} + 1	
V_{IL2}[1]	Input Low Voltage	1.8V ≤ V_{CC} ≤ 2.7V		-0.6		V_{CC} x 0.3	V
V_{IH2}[1]	Input High Voltage			V_{CC} x 0.7		V_{CC} + 1	
V_{OL1}	Output Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1mA			0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -0.4mA	2.4			V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15mA			0.2	V
V_{OH2}	Output High Voltage		I_{OH} = -100µA	V_{CC} – 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

3.3 AC Characteristics

Table 3-3. AC Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = +2.7V to + 5.5V, CL = 1 TTL Gate and 100pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency		4.5V ≤ V_{CC} ≤ 5.5V	0		2	MHz
			2.7V ≤ V_{CC} ≤ 5.5V	0		1	
			1.8V ≤ V_{CC} ≤ 5.5V	0		0.25	
t_{SKH}	SK High Time		4.5V ≤ V_{CC} ≤ 5.5V	250			ns
			2.7V ≤ V_{CC} ≤ 5.5V	250			
			1.8V ≤ V_{CC} ≤ 5.5V	1,000			
t_{SKL}	SK Low Time		4.5V ≤ V_{CC} ≤ 5.5V	250			ns
			2.7V ≤ V_{CC} ≤ 5.5V	250			
			1.8V ≤ V_{CC} ≤ 5.5V	1,000			
t_{CS}	Minimum CS Low Time		4.5V ≤ V_{CC} ≤ 5.5V	250			ns
			2.7V ≤ V_{CC} ≤ 5.5V	250			
			1.8V ≤ V_{CC} ≤ 5.5V	1,000			
t_{CSS}	CS Setup Time	Relative to SK	4.5V ≤ V_{CC} ≤ 5.5V	50			ns
			2.7V ≤ V_{CC} ≤ 5.5V	50			
			1.8V ≤ V_{CC} ≤ 5.5V	200			
t_{DIS}	DI Setup Time	Relative to SK	4.5V ≤ V_{CC} ≤ 5.5V	100			ns
			2.7V ≤ V_{CC} ≤ 5.5V	100			
			1.8V ≤ V_{CC} ≤ 5.5V	400			
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	4.5V ≤ V_{CC} ≤ 5.5V	100			ns
			2.7V ≤ V_{CC} ≤ 5.5V	100			
			1.8V ≤ V_{CC} ≤ 5.5V	400			
t_{PD1}	Output Delay to “1”	AC Test	4.5V ≤ V_{CC} ≤ 5.5V			250	ns
			2.7V ≤ V_{CC} ≤ 5.5V			250	
			1.8V ≤ V_{CC} ≤ 5.5V			1,000	
t_{PD0}	Output Delay to “0”	AC Test	4.5V ≤ V_{CC} ≤ 5.5V			250	ns
			2.7V ≤ V_{CC} ≤ 5.5V			250	
			1.8V ≤ V_{CC} ≤ 5.5V			1,000	
t_{SV}	CS to Status Valid	AC Test	4.5V ≤ V_{CC} ≤ 5.5V			250	ns
			2.7V ≤ V_{CC} ≤ 5.5V			250	
			1.8V ≤ V_{CC} ≤ 5.5V			1,000	
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	4.5V ≤ V_{CC} ≤ 5.5V			100	ns
			2.7V ≤ V_{CC} ≤ 5.5V			150	
			1.8V ≤ V_{CC} ≤ 5.5V			400	
t_{WP}	Write Cycle Time			0.10	3	5	ms
Endurance(1)	5.0V, 25°C			1M			Write Cycle

Note: 1. This parameter is ensured by characterization.

4. Functional Description

The AT93C46E is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a Start condition (Logic 1) followed by the appropriate opcode and the desired memory address location.

Table 4-1. Instruction Set

Instruction	SB	Opcode	Address	Comments
			x16	
READ	1	10	$A_5 - A_0$	Reads data stored in memory, at specified address.
EWEN	1	00	11XXXX	Write enable must precede all programming modes.
ERASE	1	11	$A_5 - A_0$	Erase memory location $A_n - A_0$.
WRITE	1	01	$A_5 - A_0$	Writes memory location $A_n - A_0$.
ERAL	1	00	10XXXX	Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXX	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXX	Disables all programming instructions.

READ: The READ instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the Serial Output (DO) pin. Output data changes are synchronized with the rising edges of Serial Clock (SK).

Note: It should be noted that a dummy bit (Logic 0) precedes the 16-bit data output string.

ERASE/WRITE ENABLE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out.

Note: Once in the EWEN state, programming remains enabled until an EWDS instruction is executed or V_{CC} power is removed from the device.

ERASE: The ERASE instruction programs all bits in the specified memory location to the Logic 1 state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the device if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A Logic 1 at pin DO indicates that the selected memory location has been erased and the part is ready for another instruction.

WRITE: The WRITE instruction contains the 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A Logic 0 at DO indicates that programming is still in progress. A Logic 1 indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/Busy status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP}.

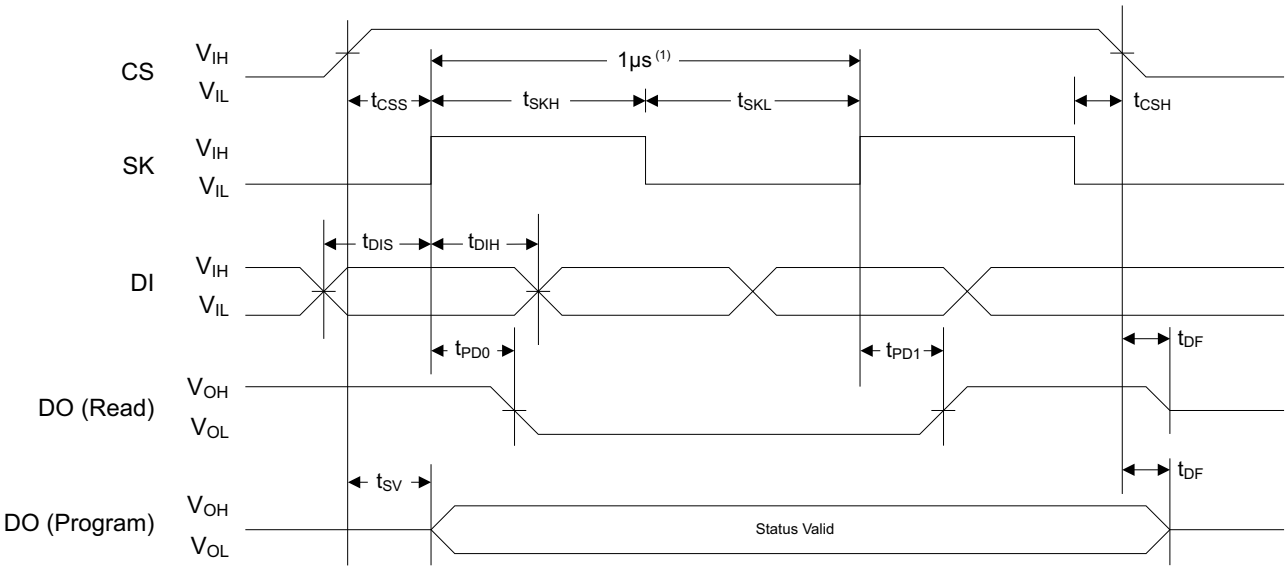
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the Logic 1 state and is primarily used for testing purposes. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

Erase/Write Disable (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

5. Timing Diagrams

Figure 5-1. Synchronous Data Timing



Note: 1. This is the minimum SK period.

Table 5-1. Organization Key for Timing Diagrams

I/O	x16
A_N	A_5
D_N	D_{15}

Figure 5-2. Read Timing

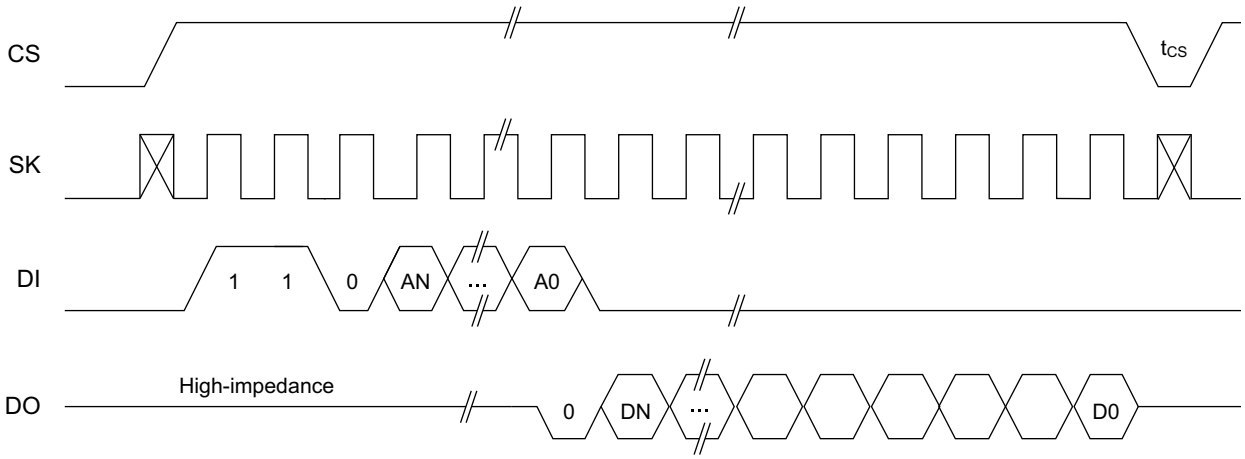
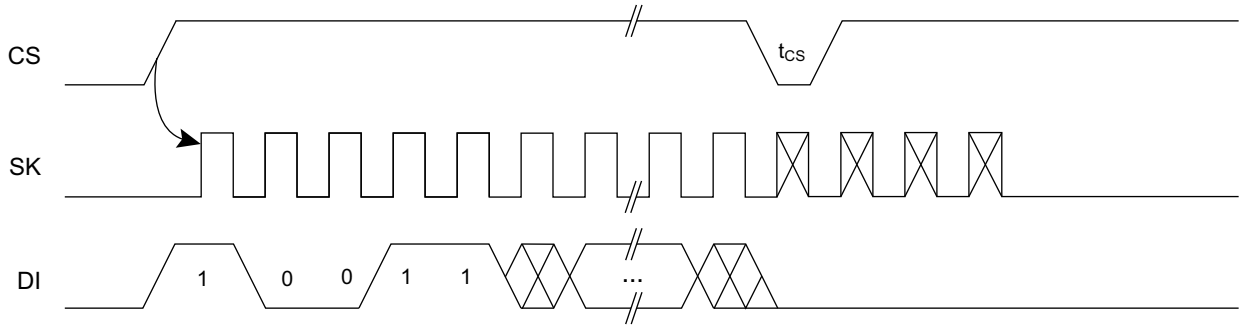


Figure 5-3. EWEN Timing[1]



Note: 1. Requires a minimum of nine clock cycles.

Figure 5-4. ERASE Timing

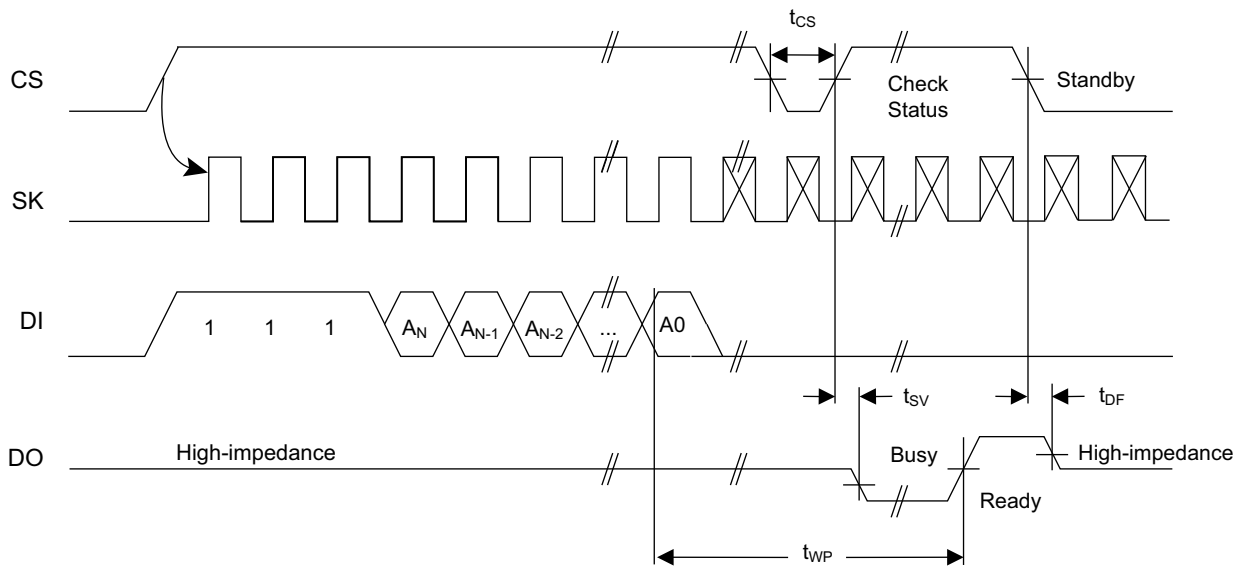


Figure 5-5. Write Timing

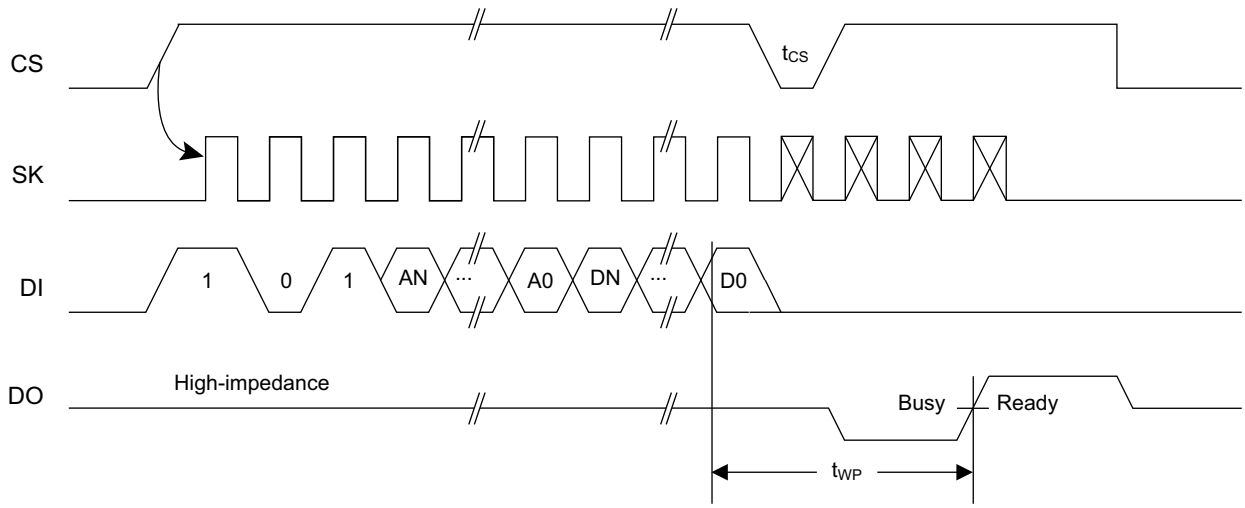
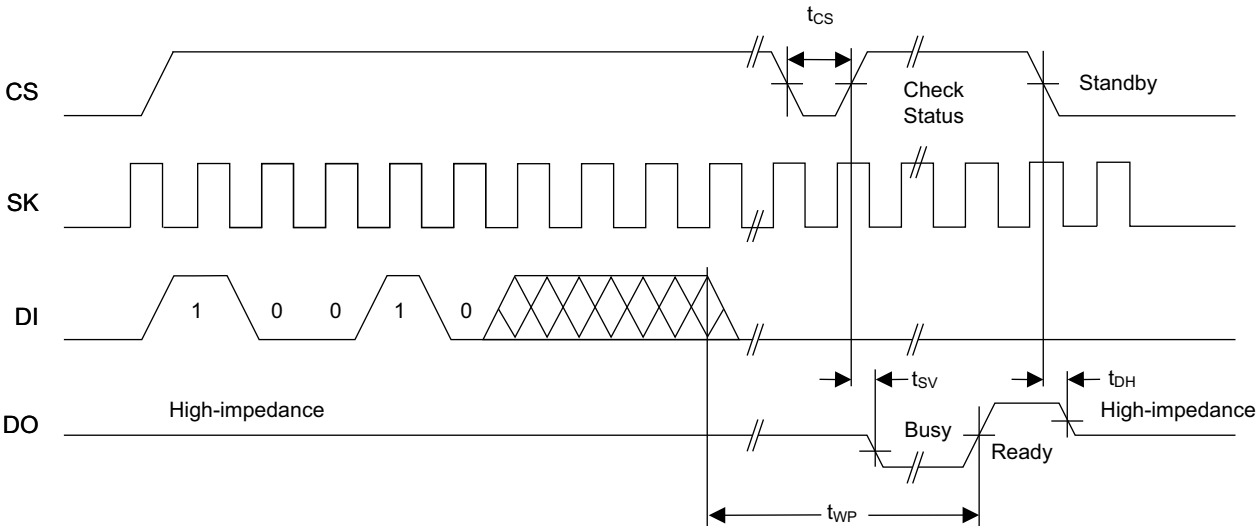
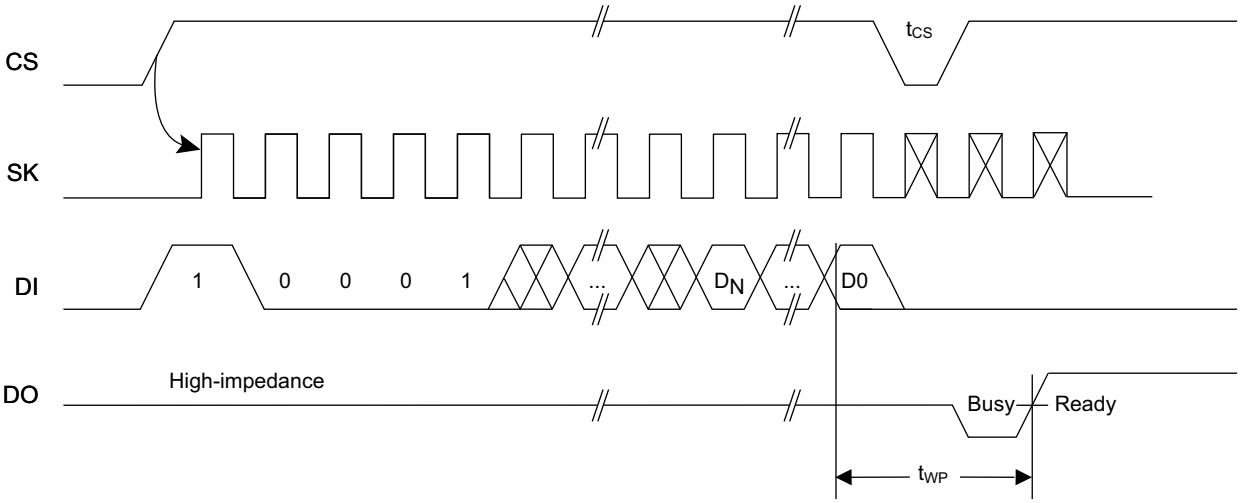


Figure 5-6. ERAL Timing(1)



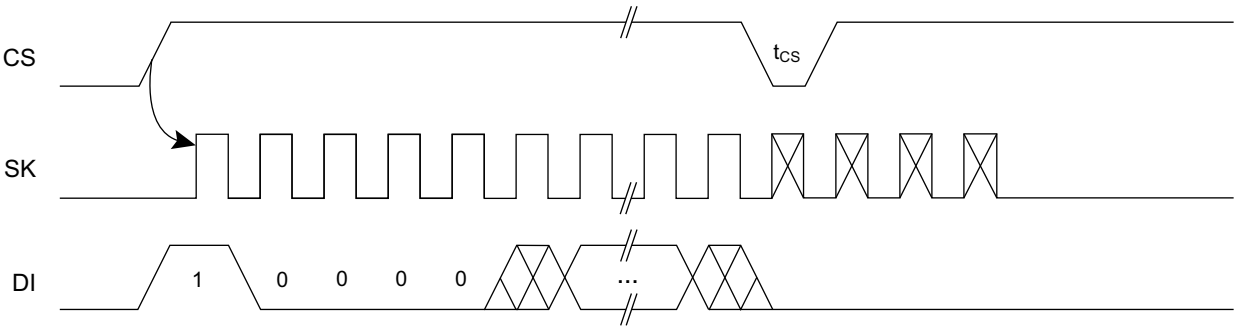
Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

Figure 5-7. WRAL Timing(1) (2)



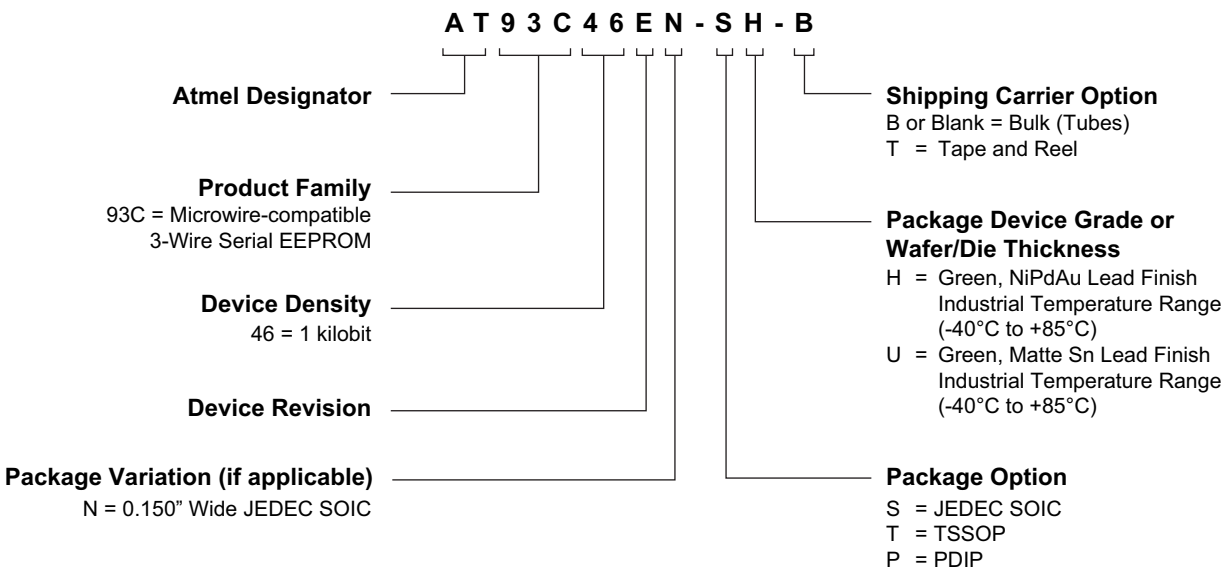
Notes: 1. Valid only at V_{CC} = 4.5V to 5.5V.
2. Requires a minimum of nine clock cycles.

Figure 5-8. EWDS Timing(1)



Note: 1. Requires a minimum of nine clock cycles.

6. Ordering Code Detail



7. Ordering Information

Atmel Ordering Code	Lead Finish	Package	Voltage	Operation Range
AT93C46EN-SH-B[1]	NiPdAu (Lead-free/Halogen-free)	8S1	1.8V to 5.5V	Industrial Temperature (-40°C to 85°C)
AT93C46EN-SH-T[2]				
AT93C46E-TH-B[1]		8X		
AT93C46E-TH-T[2]				
AT93C46E-PU	Matte Tin (Lead-free/Halogen-free)	8P3		

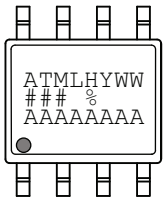
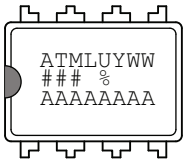
Notes: 1. -B = Bulk
- SOIC and TSSOP = 100 units per tube.
- PDIP = 50 units per tube.

2. -T = Tape and Reel, Standard Quantity Option:
- SOIC = 4,000 units per reel.
- TSSOP = 5,000 units per reel.

Package Type	
8S1	8-lead, 0.150” wide, Plastic Gull Wing, Small Outline (JEDEC SOIC)
8X	8-lead, 0.170” wide, Thin Shrink Small Outline (TSSOP)
8P3	8-lead, 0.300” wide body, Plastic Dual In-line Package (PDIP)

8. Part Markings

AT93C46E: Package Marking Information

8-lead SOIC	8-lead TSSOP	8-lead PDIP
	 Note: Lot Number and location of assembly and on the bottom side of the package.	

Note 1: ● designates pin 1
Note 2: Package drawings are not to scale

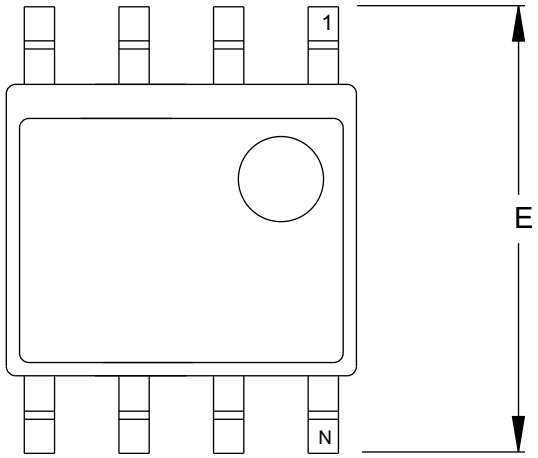
Catalog Number Truncation			
AT93C46E		Truncation Code ###: 46E	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	% = Minimum Voltage
4: 2014 8: 2018 5: 2015 9: 2019 6: 2016 0: 2020 7: 2017 1: 2021	A: January B: February ... L: December	02: Week 2 04: Week 4 ... 52: Week 52	1: 1.8V min
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		U: Industrial/Matte Tin/SnAgCu H: Industrial/NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

3/13/14

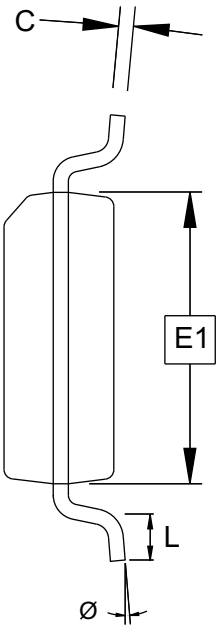
Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	**TITLE** **93C46ESM**, AT93C46E Package Marking Information	**DRAWING NO.** 93C46ESM	**REV.** A

9. Packaging Information

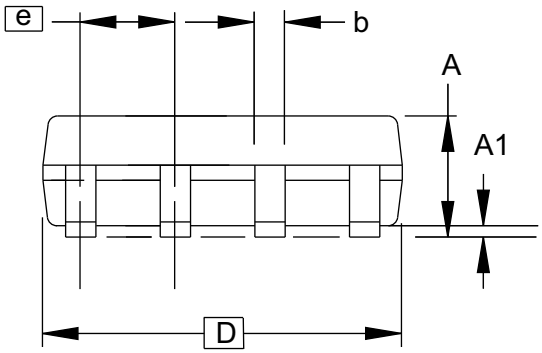
9.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

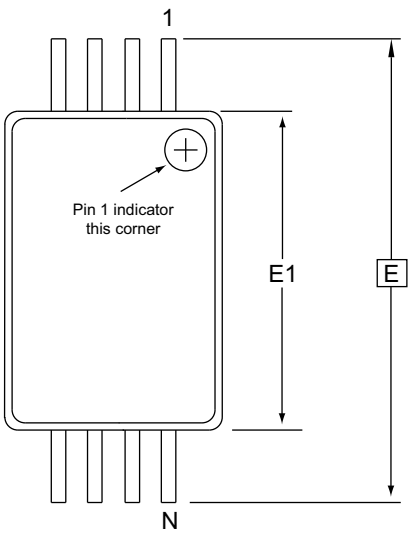
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

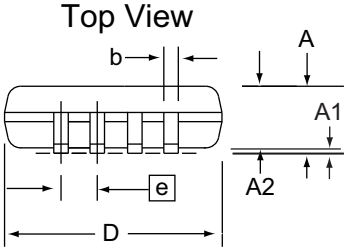
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	GPC SWB	DRAWING NO. 8S1	REV. G

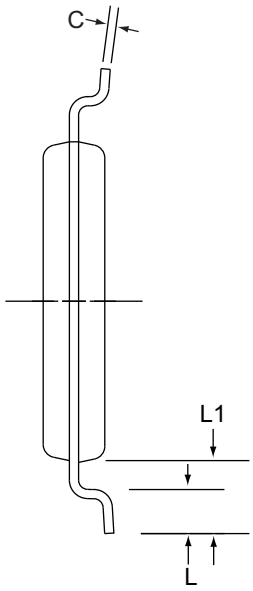
9.2 8X — 8-lead TSSOP



Top View



Side View



End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

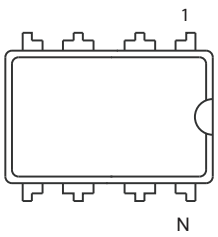
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

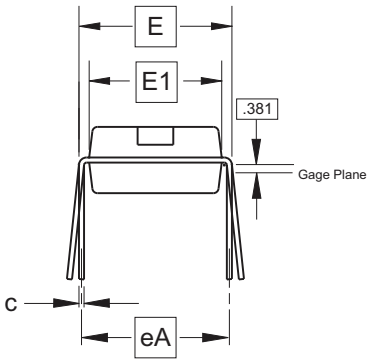
2/27/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	**GPC** TNR	**DRAWING NO.** 8X	**REV.** E

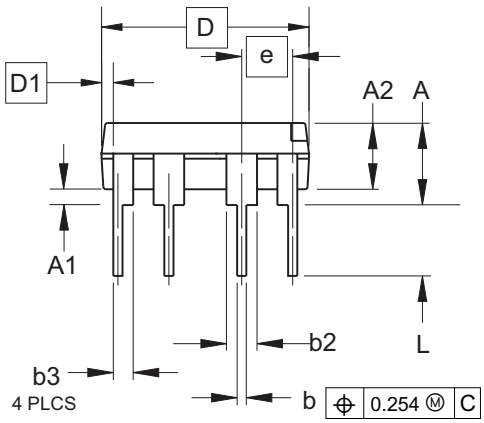
9.3 8P3 — 8-lead PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	5.334	2
A1	0.381	-	-	
A2	2.921	3.302	4.953	
b	0.356	0.457	0.559	5
b2	1.143	1.524	1.778	6
b3	0.762	0.991	1.143	6
c	0.203	0.254	0.356	
D	9.017	9.271	10.160	3
D1	0.127	0.000	0.000	3
E	7.620	7.874	8.255	4
E1	6.096	6.350	7.112	3
e	2.540 BSC			
eA	7.620 BSC			4
L	2.921	3.302	3.810	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

07/31/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8P3, 8-lead, 0.300” Wide Body, Plastic Dual In-line Package (PDIP)	GPC PTC	DRAWING NO. 8P3	REV. E

10. Revision History

Doc. Rev.	Date	Comments
5207E	10/2014	Added the part markings and ordering code detail. Updated the package outline drawings and the 8A2 to 8X. Updated template, Atmel logos, and disclaimer page.
5207D	01/2008	Removed ‘preliminary’ status
5207C	11/2007	Modified ‘max’ value on AC Characteristics table
5207B	08/2007	Modified Part Marking Scheme Tables
5207A	01/2007	Initial document release

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