P10N65F

Silicon 650V N-Channel MOS

VOLTAGE	650 Volts	CURRENT	10 Ampers

FEATURES

- Low RDS(ON)
- Ultra Low Gate Charge
- RoHS Compliant
- 100% UIS and RG Tested

TYPICAL APPLICATIONS

- Power factor correction（PFC）
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply（UPS）

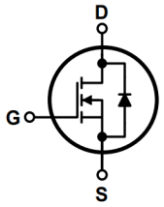
PRODUCT SUMMARY

VDS	650	V
ID	10	A
RDS(ON) ,Typ@10V	0.8	Ω
Qg	30	nC

Marking

TO-220F-3L

1 2 3



Gate:1
Drain:2
Source:3

Absolute Maximum Ratings (Ratings at 25℃ ambient temperature unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	(Note 1)	I_D	10	A
Drain Current-Pulsed	(Note 1)	I_{DM}	40	A
Total Dissipation		P_D	50	W
Junction Temperature		T_J	150	℃
Storage temperature range		T_{STD}	-55 to +150	℃
Single Pulse Avalanche Energy	(Note 2)	E_{AS}	750	mJ

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Thermal Characteristcs (Ratings at 25℃ ambient temperature unless otherwise specified)

Parameter		Symbol	Max	Unit
Thermal Resistance Junction-Case		$R_{\theta JC}$	3.0	℃/W
Thermal Resistance Junction to Ambient	(Note 3)	$R_{\theta JA}$	62.5	℃/W

Notes: 1. Ensure that the channel temperature does not exceed 150℃.

2. VDD=50V, Tch= 25℃(initial), IAS=12A, Rg=25Ω.

3. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The value in any given application depends on the user's specific board design.

This transistor is sensitive to electrostatic discharge and should be handled with care.

P10N65F

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Electrical Characteristcs (Ratings at 25℃ ambient temperature unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Static Parameters						
Drain-Source Breakdown Voltage	BV_{DSS}	VGS=0V,ID=250uA	650	-	-	V
Drain-Source Leakage Current	I_{DSS}	VDS=650V,VGS=0V	-	-	1	uA
Gate-Body Leakage Current	I_{GSS}	VGS=±30V,VDS=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(TH)}$	VGS=VDS,ID=250uA	2	3	4	V
Drain-Source On Resistance	$R_{DS(ON)}$	VGS=10V,ID=6A	-	0.80	1.00	Ω
Dynamic Characteristics						
Input Capacitance	C_{iss}	VDS=25V,VGS=0V, f=1.0MHz	-	1210	-	pF
Output Capacitance	C_{oss}		-	145	-	pF
Reverse Transfer Capacitance	C_{rss}		-	16	-	pF
Gate Resistance	R_g	VDS=0V,VGS=0V, f=1.0MHz	-	2.5	-	Ω
Switching Paramters						
Turn-On Delay Time	$t_{d(on)}$	VDS=325V,ID=12A, VGS=10V,RG=25Ω	-	20	-	ns
Turn-On Rise Time	t_r		-	30	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	90	-	ns
Turn-Off Rise Time	t_f		-	40	-	ns
Total Gate Charge	Q_g	VDS=520V,ID=12A, VGS=10V	-	30	-	nc
Gate-Source Charge	Q_{gs}		-	5.0	-	nc
Gate-Drain Charge	Q_{gd}		-	14	-	nc
Source-Drain Characteristics						
Max. Diode Forward Cuurent	I_S		-	-	10	A
Max. Pulsed Forward Cuurent	I_{SM}		-	-	40	A
Diode Forward Voltage	V_{SD}	VGS=0V,IS=12A	-	0.92	1.5	V
Reverse Recovery Time	t_{rr}	VR=400V,IF=12A, di/dt=100A/us	-	450	-	ns
Reverse Recovery Charge	Q_{rr}		-	4	-	μC

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RATING AND CHARACTERIS TICCURVES

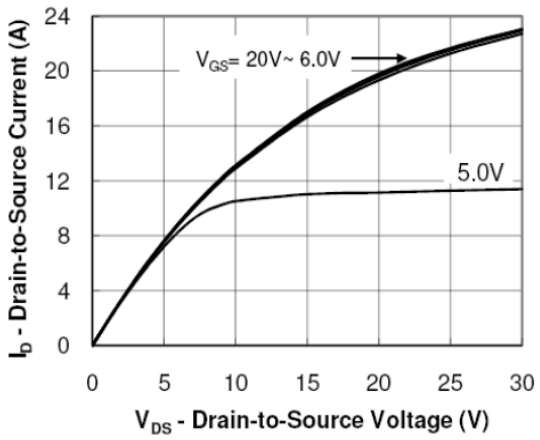

Fig.1-Output Characteritsics

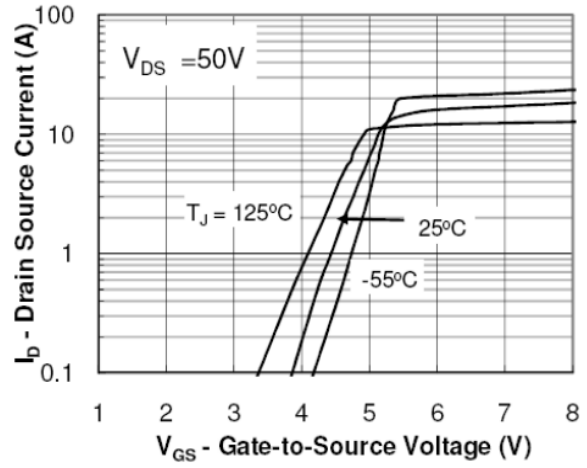

Fig.2- Transfer Characteritsics

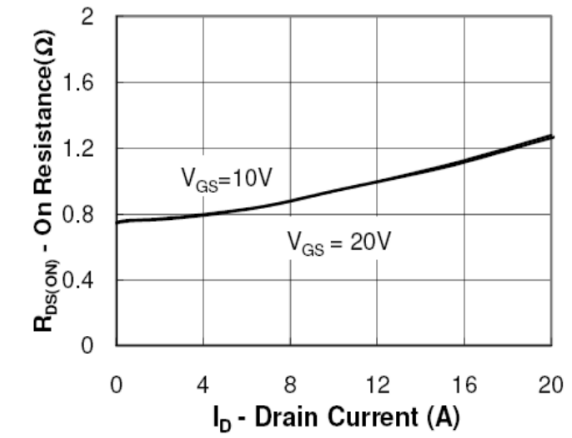

Fig.3- On Resistance Vs Drain Current

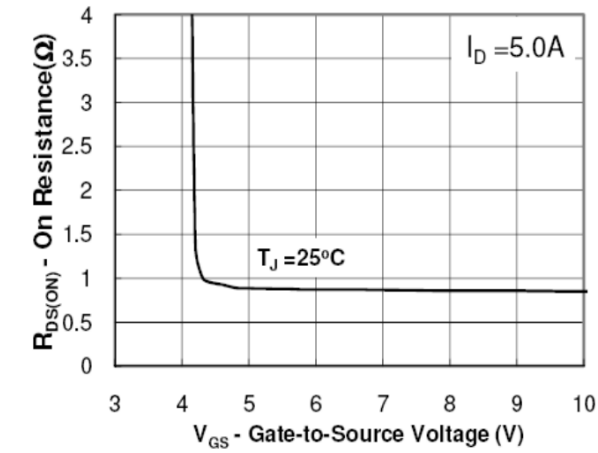

Fig.4- On Resistance Vs Gate Source Voltage

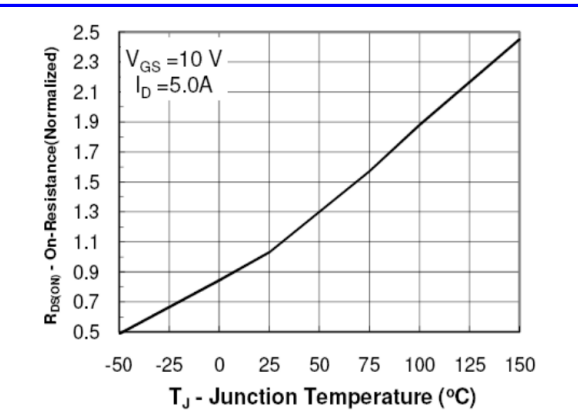

Fig.5-Rdson-JunctionTemperature

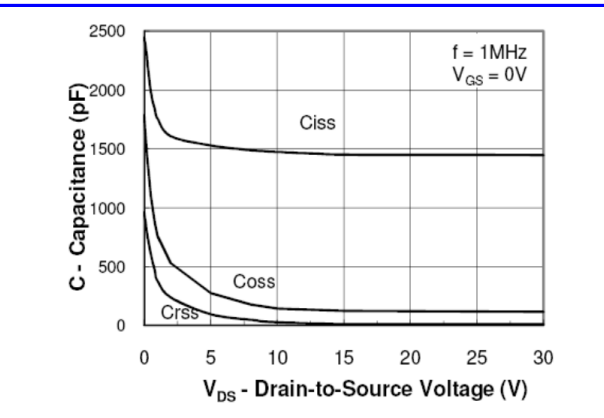

Fig.6-Capacitance

P10N65F

Silicon 650V N-Channel MOS

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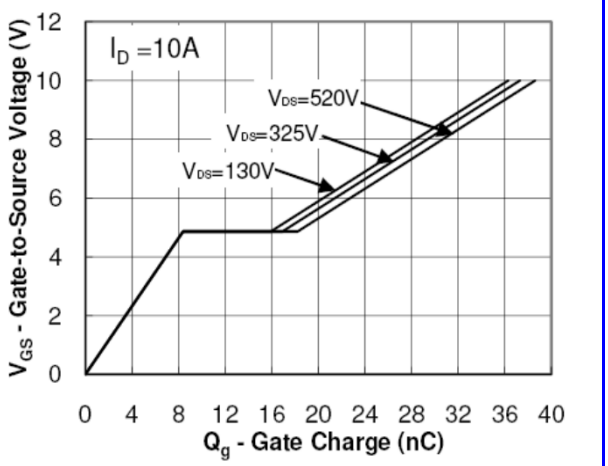


Fig.7-Gate Charge Waveform

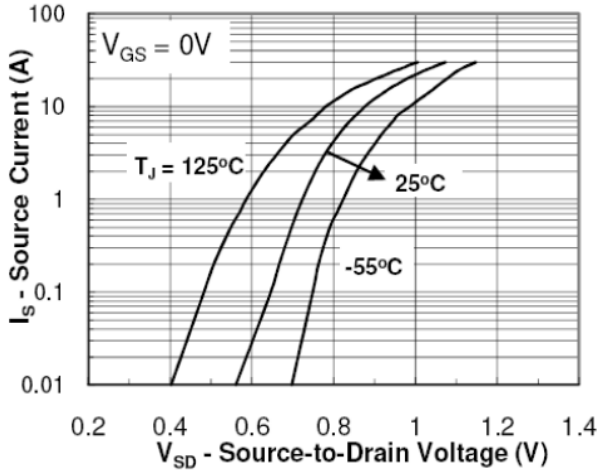


Fig.8- Source-Drain Diode Forward Voltage

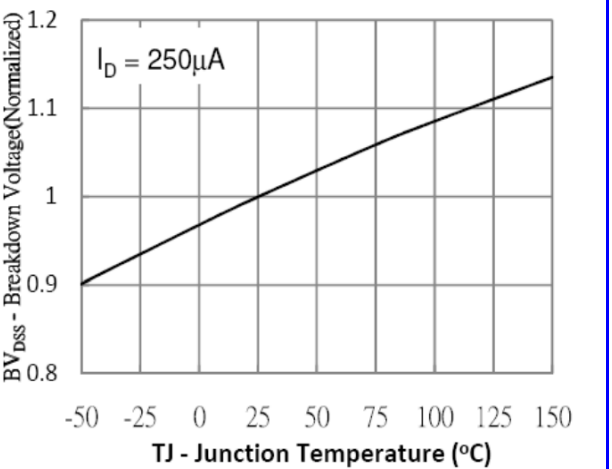


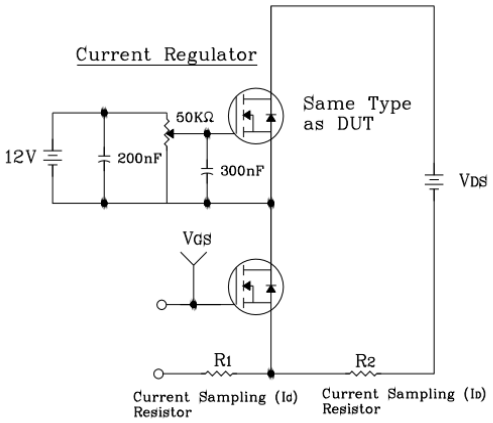
Fig.9- Breakdown Voltage Vs Junction Temperature

Note： The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

P10N65F

Silicon 650V N-Channel MOS

Test Circuit & Waveform



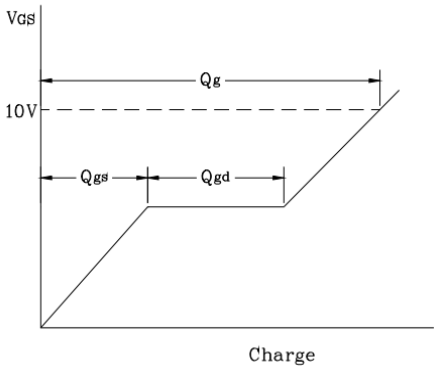
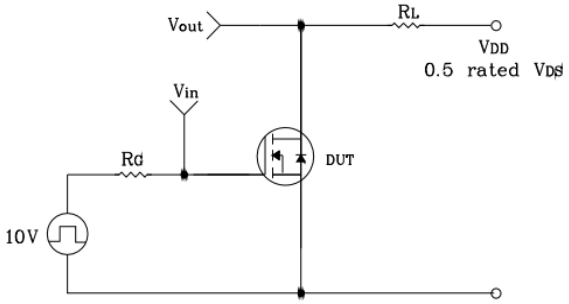


Fig.10-Gate Charge Test Circuit & Waveform



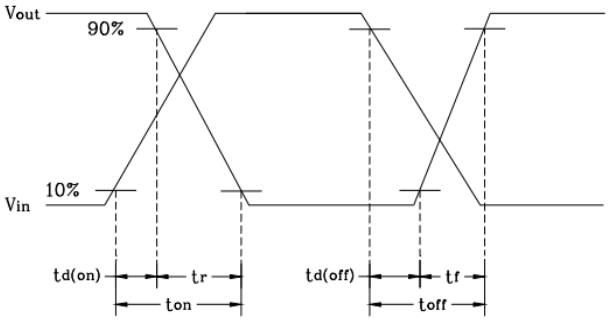
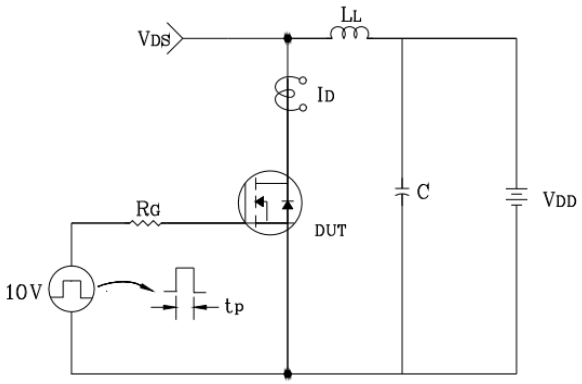


Fig.11- Resistive Switching Test Circuit & Waveform



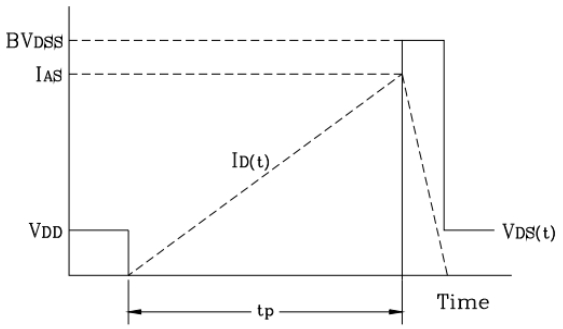


Fig.12- EAS Test Circuit & Waveform

P10N65F

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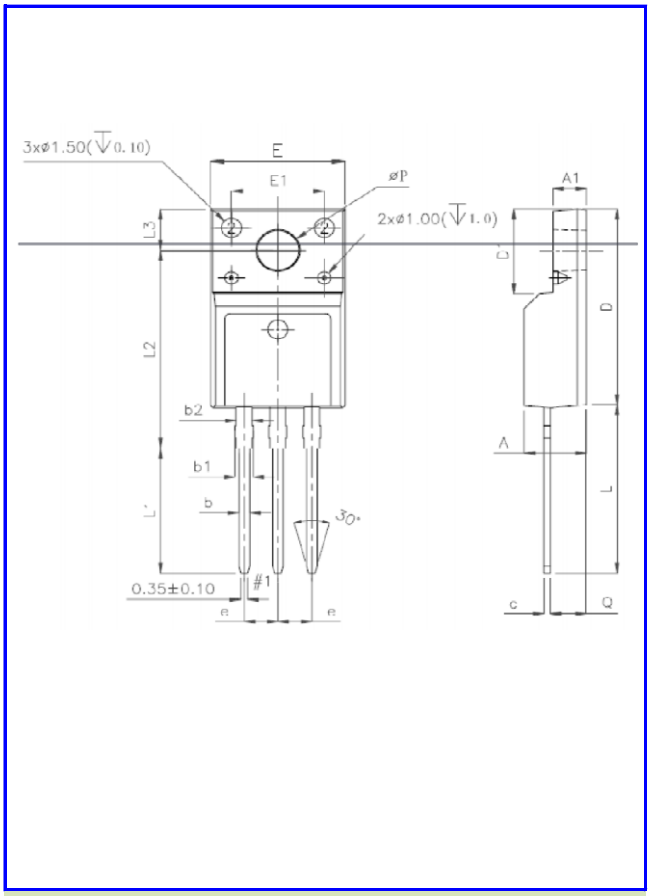
OUTLINE DRAWINGS



TO-220F-3L

Items	Values(mm)		
	Min.	Nom	Max.
A	4.50		4.90
A1	2.30		2.90
b	0.65		0.90
b1	1.10		1.70
b2	1.20		1.40
c	0.35		0.65
D	14.50		16.50
D1	6.10		6.90
E	9.60		10.30
E1	6.50	7.00	7.50
e	2.44	2.54	2.64
L	12.50		14.30
L1	9.45		10.05
L2	15.00		16.00
L3	3.20		4.40
ΦP	3.00		3.30
Q	2.50		2.90

Packing Information

Product code	Pack	Box Size L×W×H(mm)	Quantity(pcs/box)	Carton SizeL×W×H(mm)	Quantity(box/carton)
P10N65F	P/T	550*150*40	1000	580*230*175	5