TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS026C – Revised September 2003

# CD4016B Types

## CMOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (20-Volt Rating)

■ CD4016B Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch on or off.

The CD4016 "B" Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

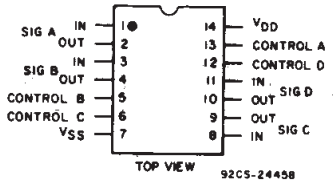
*Features:*

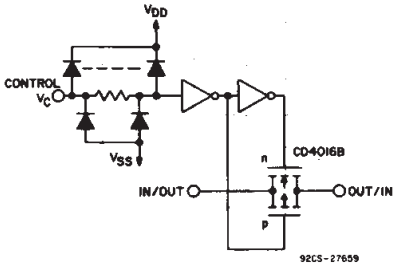
- **20-V digital or ± 10-V peak-to-peak switching**
- **280-Ω typical on-state resistance for 15-V operation**
- **Switch on-state resistance matched to within 10 Ω typ. over 15-V signal-input range**
- **High on/off output-voltage ratio: 65 dB typ. @ $f_{is}$ = 10 kHz, $R_L$ = 10 kΩ**
- **High degree of linearity: <0.5% distortion typ. @ $f_{is}$ = 1 kHz, $V_{is}$ = 5 $V_{p-p}$, $V_{DD}-V_{SS} \geq 10$ V, $R_L$ = 10 kΩ**
- **Extremely low off-state switch leakage resulting in very low offset current and high effective off-state resistance: 100 pA typ. @ $V_{DD}-V_{SS}$=18 V, $T_A$=25°C**
- **Extremely high control input impedance (control circuit isolated from signal circuit: $10^{12}$ Ω typ.**
- **Low crosstalk between switches: –50 dB typ. @ $f_{is}$ = 0.9 MHz, $R_L$ = 1 kΩ**
- **Matched control-input to signal-output capacitance: Reduces output signal transients**
- **Frequency response, switch on = 40 MHz (typ.)**
- **100% tested for quiescent current at 20 V**
- **Maximum control input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V at 25°C**
- **5-V, 10-V, and 15-V parametric ratings**

*Applications:*

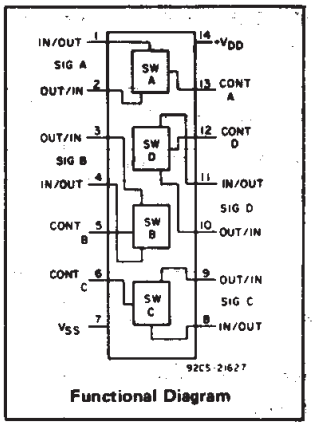
- **Analog signal switching/multiplexing**
  - **Signal gating**
  - **Squelch control**
  - **Chopper**
  - **Modulator**
  - **Demodulator**
  - **Commutating switch**
- **Digital signal switching/multiplexing**
- **CMOS logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**

**Terminal Assignment**




*Schematic diagram - 1 of 4 identical sections.*




**Functional Diagram**

**RECOMMENDED OPERATING CONDITIONS**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | Min. | Max. | |
| Supply Voltage Range (For $T_A$ = Full Package Temperature Range) | 3 | 18 | V |

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltages referenced to $V_{SS}$ Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55°C to +100°C ..... 500mW
For $T_A$ = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

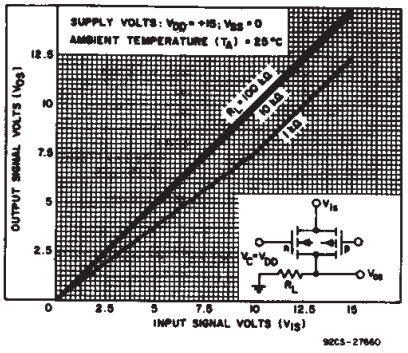



*Fig. 1– Typ. on-state characteristics for 1 of 4 switches with $V_{DD}$ = +15 V, $V_{SS}$ = 0 V.*

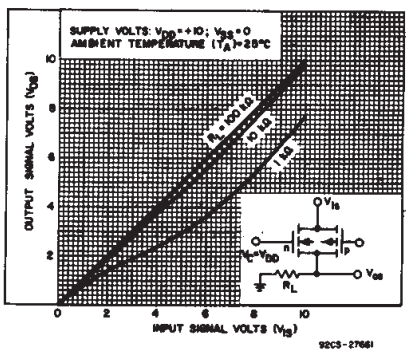



*Fig. 2– Typ. on-state characteristics for 1 of 4 switches with $V_{DD}$ = +10 V, $V_{SS}$ = 0 V.*

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## ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | TEST CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | +25 Typ. | +25 Max. | |
| Quiescent Device Current, $I_{DD}$ | | 0,5 | 5 | 0.25 | 0.25 | 7.5 | 7.5 | 0.01 | 0.25 | μA |
| | | 0,10 | 10 | 0.5 | 0.5 | 15 | 15 | 0.01 | 0.5 | |
| | | 0,15 | 15 | 1 | 1 | 30 | 30 | 0.01 | 1 | |
| | | 0,20 | 20 | 5 | 5 | 150 | 150 | 0.02 | 5 | |
| **Signal Inputs ($V_{is}$) and Output ($V_{os}$)** | | | | | | | | | | |
| On-State Resistance, $r_{on}$ Max. | $V_C = V_{DD}$, $R_L = 10k\Omega$ Returned to $\frac{V_{DD}-V_{SS}}{2}$ | $V_{is}=V_{DD}$ or $V_{SS}$ | 10 | 600 | 610 | 840 | 960 | – | 660 | Ω |
| | | $V_{is}$=4.75 to 5.75 V | 10 | 1870 | 1900 | 2380 | 2600 | – | 2000 | |
| | | $V_{is}=V_{DD}$ or $V_{SS}$ | 15 | 360 | 370 | 520 | 600 | – | 400 | |
| | | $V_{is}$=7.25 to 7.75 V | 15 | 775 | 790 | 1080 | 1230 | – | 850 | |
| ΔOn-State Resistance Between Any 2 Switches, $\Delta r_{on}$ | $R_L$=10 kΩ, $V_C = V_{DD}$ | | 5 | – | – | – | – | 15 | – | Ω |
| | | | 10 | – | – | – | – | 10 | – | |
| | | | 15 | – | – | – | – | 5 | – | |
| Total Harmonic Distortion, THD | $V_C=V_{DD}$ = 5 V, $V_{SS}$ = −5 V, $V_{is(p-p)}$ = 5 V (Sine wave centered on 0 V) $R_L$=10 kΩ, $f_{is}$=1 kHz sine wave | | | – | – | – | – | 0.4 | – | % |
| −3dB Cutoff Frequency (Switch on) | $V_C=V_{DD}$=5 V, $V_{SS}$ = −5 V, $V_{is(p-p)}$ =5 V (Sine wave centered on 0 V) $R_L$ = 1 kΩ, | | | – | – | – | – | 40 | – | MHz |
| −50dB Feed-through Frequency (Switch off) | $V_C=V_{SS}$= −5 V, $V_{is(p-p)}$=5 V (Sine wave centered on 0 V) $R_L$ = 1 kΩ | | | – | – | – | – | 1.25 | – | MHz |
| Input/Output Leakage Current (Switch off) $I_{is}$ Max. | $V_C$ = 0 V $V_{is}$ = 18 V, $V_{os}$ = 0 V; $V_{is}$ = 0 V, $V_{os}$ = 18 V | | 18 | ±0.1 | ±0.1 | ±1 | ±1 | $10^{-4}$ | ±0.1 | μA |
| −50 dB Crosstalk Frequency | $V_C$(A) = $V_{DD}$ = +5 V, $V_C$(B) = $V_{SS}$ = −5 V, $V_{is}$(A) = 5 $V_{p-p}$, 50 Ω source $R_L$ = 1 kΩ | | | – | – | – | – | 0.9 | – | MHz |
| Propagation Delay (Signal Input to Signal Output) $t_{pd}$ | $R_L$ = 200 kΩ $V_C = V_{DD}$, $V_{SS}$ = GND, $C_L$ = 50 pF $V_{is}$ = Square Wave 0 to $V_{DD}$ $t_r$, $t_f$ = 20 ns | | 5 | – | – | – | – | 40 | 100 | ns |
| | | | 10 | – | – | – | – | 20 | 40 | |
| | | | 15 | – | – | – | – | 15 | 30 | |
| Capacitance: Input, $C_{is}$ | $V_{DD}$ = +5 V $V_C = V_{SS}$ = −5 V | | | – | – | – | – | 4 | – | pF |
| Output, $C_{os}$ | | | | – | – | – | – | 4 | – | |
| Feedthrough, $C_{ios}$ | | | | – | – | – | – | 0.2 | – | |

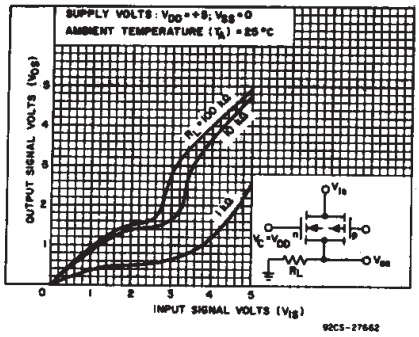



*Fig. 3—Typ. on-state characteristics for 1 of 4 switches with $V_{DD}$ = +5 V, $V_{SS}$ = 0 V.*

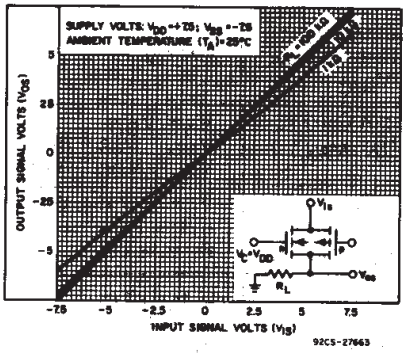



*Fig. 4—Typ. on-state characteristics for 1 of 4 switches with $V_{DD}$ = +7.5 V, $V_{SS}$ = −7.5 V.*

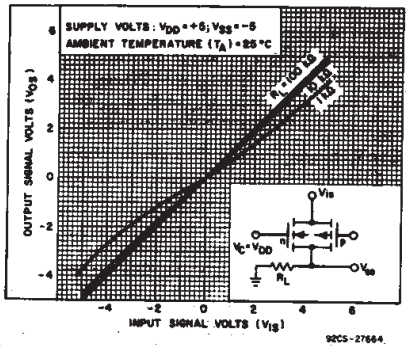



*Fig. 5— Typ. on-state characteristics for 1 of 4 switches with $V_{DD}$ = +5 V, $V_{SS}$ = −5 V.*

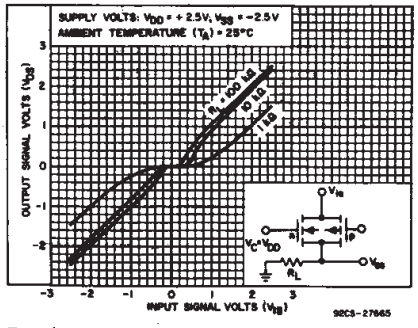



*Fig. 6— Typ. on-state characteristics for 1 of 4 switches with $V_{DD}$ = +2.5 V, $V_{SS}$ = −2.5 V.*

## ELECTRICAL CHARACTERISTICS (cont'd)

| CHARACTERISTIC | TEST CONDITIONS | $V_{DD}$ (V) | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | +25 | | |
| | | | −55 | −40 | +85 | +125 | Typ. | Max. | |
| **Control ($V_C$)** | | | | | | | | | |
| Control Input Low Voltage, $V_{ILC}$ (Max.) | $\|I_{is}\| < 10\,\mu A$<br>$V_{is} = V_{SS}$, $V_{OS} = V_{DD}$ and<br>$V_{is} = V_{DD}$, $V_{OS} = V_{SS}$ | 5,10, 15 | 0.9 | 0.9 | 0.4 | 0.4 | – | 0.7 | V |
| Control Input High Voltage, $V_{IHC}$ | See Fig. 10 | 5 | 3.5 (Min.) | | | | | | V |
| | | 10 | 7 (Min.) | | | | | | |
| | | 15 | 11 (Min.) | | | | | | |
| Input Current, $I_{IN}$ (Max.) | $V_{is} \leq V_{DD}$<br>$V_{DD} - V_{SS} = 18$ V<br>$V_{CC} \leq V_{DD} - V_{SS}$ | 18 | ±0.1 | ±0.1 | ±1 | ±1 | $\pm 10^{-5}$ | ±0.1 | μA |
| Crosstalk (Control Input to Signal Output) | $V_C = 10$ V (Sq. Wave)<br>$t_r$, $t_f = 20$ ns<br>$R_L = 10$ kΩ | 10 | – | – | – | – | 50 | – | mV |
| Turn-On Propagation Delay | $t_r$, $t_f = 20$ ns<br>$C_L = 50$ pF<br>$R_L = 1$ kΩ | 5 | – | – | – | – | 35 | 70 | ns |
| | | 10 | – | – | – | – | 20 | 40 | |
| | | 15 | – | – | – | – | 15 | 30 | |
| Maximum Control Input Repetition Rate | $V_{is} = V_{DD}$, $V_{SS}$ = GND,<br>$R_L = 1$ kΩ to gnd,<br>$C_L = 50$ pF,<br>$V_C = 10$ V (Square wave centered on 5 V)<br>$t_r$, $t_f = 20$ ns,<br>$V_{os} = ½\ V_{os}$ @ 1 kHz | 10 | – | – | – | – | 10 | – | MHz |
| Input Capacitance, $C_{IN}$ | | | – | – | – | – | 5 | 7.5 | μF |

| $V_{DD}$ (V) | $V_{is}$ (V) | Switch Input $I_{is}$ (mA) −55°C | −40°C | 25°C* | 25°C▲ | +85°C | +125°C | Switch Output $V_{OS}$ (V) Min. | Max. |
|---|---|---|---|---|---|---|---|---|---|
| 5 | 0 | 0.25 | 0.2 | 0.2 | 0.16 | 0.12 | 0.14 | – | 0.4 |
| 5 | 5 | −0.25 | −0.2 | −0.2 | −0.16 | −0.12 | −0.14 | 4.6 | – |
| 10 | 0 | 0.62 | 0.5 | 0.5 | 0.4 | 0.3 | 0.35 | – | 0.5 |
| 10 | 10 | −0.62 | −0.5 | −0.5 | −0.4 | −0.3 | −0.35 | 9.5 | – |
| 15 | 0 | 1.8 | 1.4 | 1.5 | 1.2 | 1 | 1.1 | – | 1.5 |
| 15 | 15 | −1.8 | −1.4 | −1.5 | −1.2 | −1 | −1.1 | 13.5 | – |

* Plastic package ▲ Ceramic package

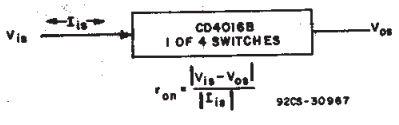



*Fig. 10— Determination of $r_{on}$ as a test condition for control input high voltage ($V_{IHC}$) specification.*

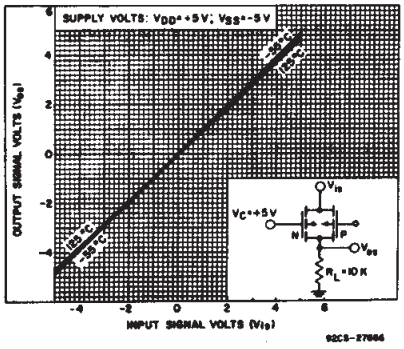



*Fig. 7— Typ. on-state characteristics as a function of temp. for 1 of 4 switches with $V_{DD}$ = +5 V, $V_{SS}$ = −5 V.*

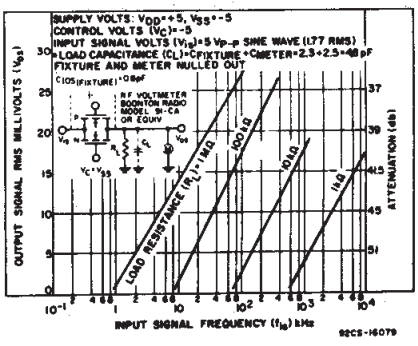



*Fig. 8 — Typ. feedthru vs. frequency — switch off.*

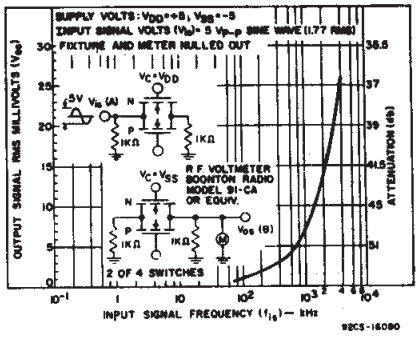



*Fig. 9— Typical crosstalk between switch circuits in the same package.*

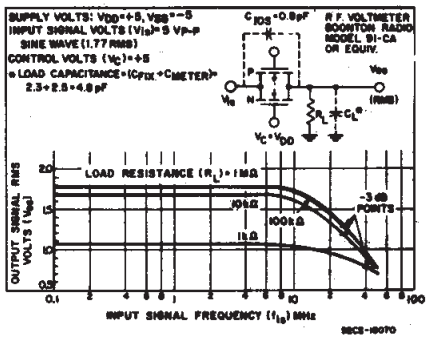



*Fig. 11 — Typical frequency response — switch on.*

## TYPICAL ON-STATE RESISTANCE CHARACTERISTICS, $T_A$ = 25°C

| CHARACTERISTIC* | SUPPLY CONDITIONS | | LOAD CONDITIONS | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | $R_L$ = 1kΩ | | $R_L$ = 10kΩ | | $R_L$ = 100kΩ | |
| | $V_{DD}$ (V) | $V_{SS}$ (V) | VALUE (Ω) | $V_{is}$ (V) | VALUE (Ω) | $V_{is}$ (V) | VALUE (Ω) | $V_{is}$ (V) |
| $r_{on}$ | +15 | 0 | 200 | +15 | 200 | +15 | 180 | +15 |
| | | | 200 | 0 | 200 | 0 | 200 | 0 |
| $r_{on}$ (max.) | +15 | 0 | 300 | +11 | 300 | +9.3 | 320 | +9.2 |
| $r_{on}$ | +10 | 0 | 290 | +10 | 250 | +10 | 240 | +10 |
| | | | 290 | 0 | 250 | 0 | 300 | 0 |
| $r_{on}$ (max.) | +10 | 0 | 500 | +7.4 | 560 | +5.6 | 610 | +5.5 |
| $r_{on}$ | + 5 | 0 | 860 | + 5 | 470 | + 5 | 450 | + 5 |
| | | | 600 | 0 | 580 | 0 | 800 | 0 |
| $r_{on}$ (max.) | + 5 | 0 | 1.7k | +4.2 | 7k | +2.9 | 33k | +2.7 |
| $r_{on}$ | +7.5 | −7.5 | 200 | +7.5 | 200 | +7.5 | 180 | +7.5 |
| | | | 200 | −7.5 | 200 | −7.5 | 180 | −7.5 |
| $r_{on}$ (max.) | +7.5 | −7.5 | 290 | ±0.25 | 280 | ±25 | 400 | ±0.25 |
| $r_{on}$ | + 5 | − 5 | 260 | + 5 | 250 | + 5 | 240 | + 5 |
| | | | 310 | − 5 | 250 | − 5 | 240 | − 5 |
| $r_{on}$ (max.) | + 5 | − 5 | 600 | ±0.25 | 580 | ±0.25 | 760 | ±0.25 |
| $r_{on}$ | +2.5 | −2.5 | 590 | +2.5 | 450 | +2.5 | 490 | +2.5 |
| | | | 720 | -2.5 | 520 | -2.5 | 520 | −2.5 |
| $r_{on}$ (max.) | +2.5 | −2.5 | 232k | ±0.25 | 300k | ±0.25 | 870k | ±0.25 |

* Variation from aperfect switch, $r_{on}$ = 0 Ω.

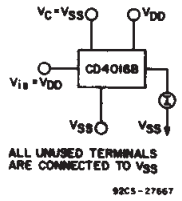



*Fig. 12 – Off-state switch input or output leakage current test circuit.*

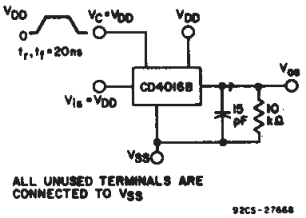
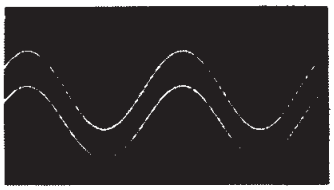


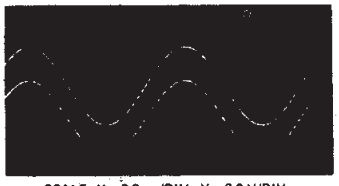

*Fig.13 – Test circuit for square-wave response.*



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
$V_{DD}$ = $V_C$ = +7.5V, $V_{SS}$ = -7.5V, $R_L$ = 10KΩ
$C_L$ = 15 pF
$f_{IS}$ = 1 KHz $V_{IS}$ = 5V p-p
DISTORTION = 0.2 %

92CS-27612

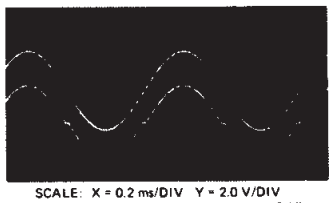
*Fig.14 – Typical sine wave response of $V_{DD}$ = +7.5 V, $V_{SS}$ = −7.5 V.*



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
$V_{DD}$ = $V_C$ = +5 V, $V_{SS}$ = -5 V, $R_L$ = 10KΩ
$C_L$ = 15 pF
$f_{IS}$ = 1 KHz $V_{IS}$ = 5 V p-p
DISTORTION = 0.4 %

92CS-27613

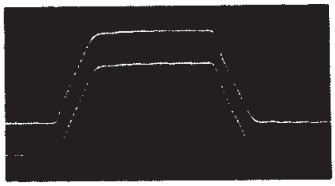
*Fig.15 – Typical sine wave response of $V_{DD}$ = +5 V, $V_{SS}$ = −5 V.*



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
$V_{DD}$ = $V_C$ = +2.5V, $V_{SS}$ = -2.5V, $R_L$ = 10KΩ
$C_L$ = 15 pF
$f_{IS}$ = 1 KHz $V_{IS}$ = 5V p-p
DISTORTION = 3 %

92CS-27614

*Fig.16 – Typical sine wave response of $V_{DD}$ = +2.5 V, $V_{SS}$ = −2.5 V.*



SCALE: X = 100 ns/DIV
Y = 5.0 V/DIV

92CS-27615

*Fig.17 – Typical square wave response at $V_{DD}$ = $V_C$ = +15 V, $V_{SS}$ = Gnd.*



SCALE: X = 100 ns/DIV
Y = 5.0 V/DIV

92CS-27616

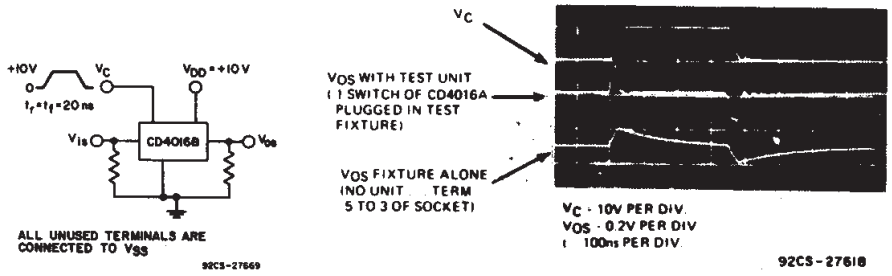
*Fig.18 – Typical square wave response at $V_{DD}$ = $V_C$ = +10 V, $V_{SS}$ = Gnd.*



SCALE: X = 100 ns/DIV
Y = 2 V/DIV

92CS-27617

*Fig.19 – Typical square wave response at $V_{DD}$ = $V_C$ = +5 V, $V_{SS}$ = Gnd.*




(a) (b)

*Fig.20 – Crosstalk-control input to signal output.*

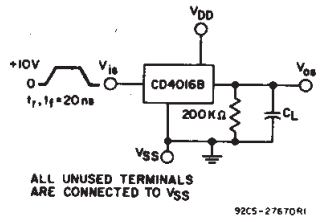



*Fig.21 – Propagation delay time signal input ($V_{IS}$) to signal output ($V_{OS}$).*

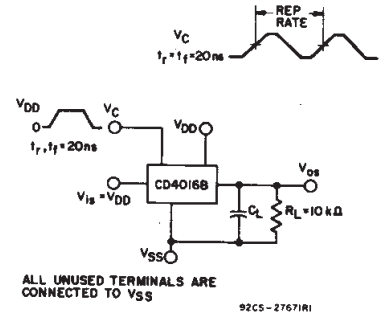



*Fig. 22 – Max. control-input repetition rate.*

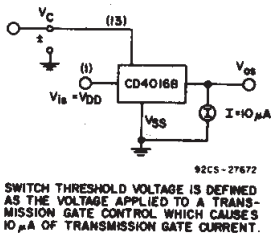



*Fig.23 – Switch threshold voltage.*

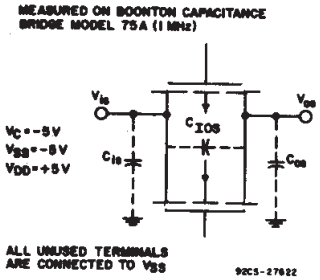



*Fig.24 – Capacitance $C_{IOS}$ and $C_{OS}$.*

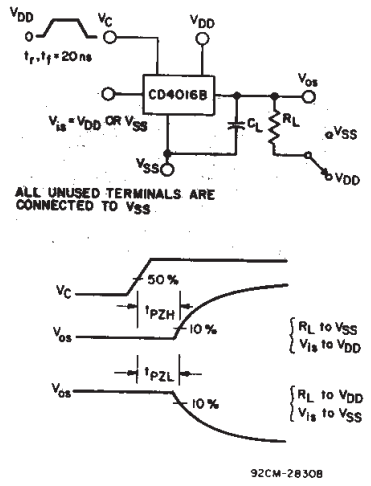
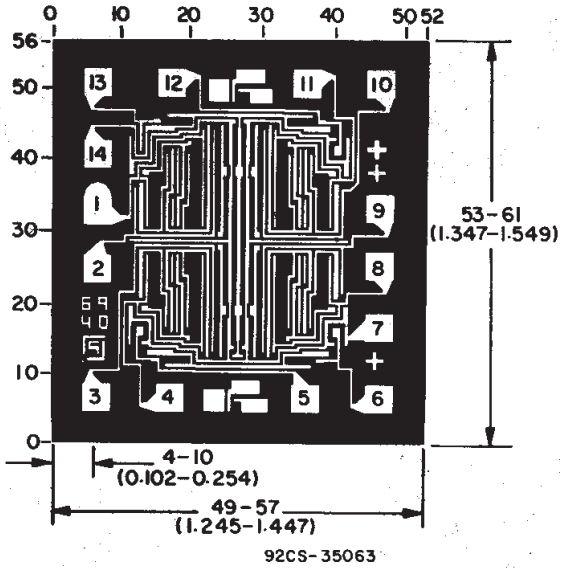



*Fig.25 – Turn-On propagation delay-control input.*

**Dimensions and pad layout for CD4016BH**




*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).*

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9064001CA | ACTIVE | CDIP | J | 14 | 1 | TBD | Call TI | Call TI | |
| CD4016BE | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| CD4016BEE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| CD4016BF | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | |
| CD4016BF3A | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | |
| CD4016BM | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BM96 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BM96E4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BM96G4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BME4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BMG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BMT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BMTE4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BMTG4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BNSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BNSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BNSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BPWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| CD4016BPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BPWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD4016BPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF CD4016B, CD4016B-MIL :**

- Catalog: CD4016B

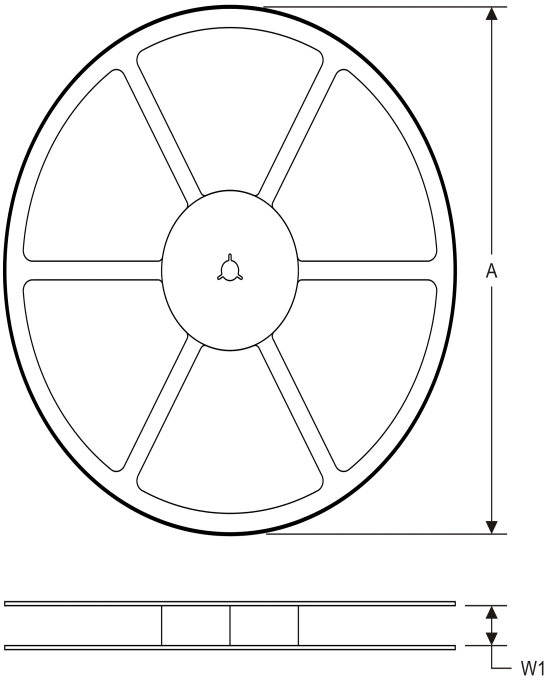
- Military: CD4016B-MIL

NOTE: Qualified Version Definitions:

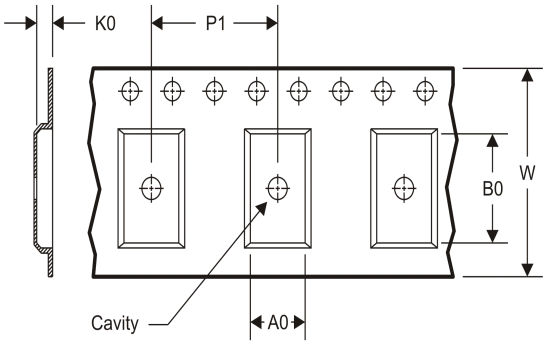
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



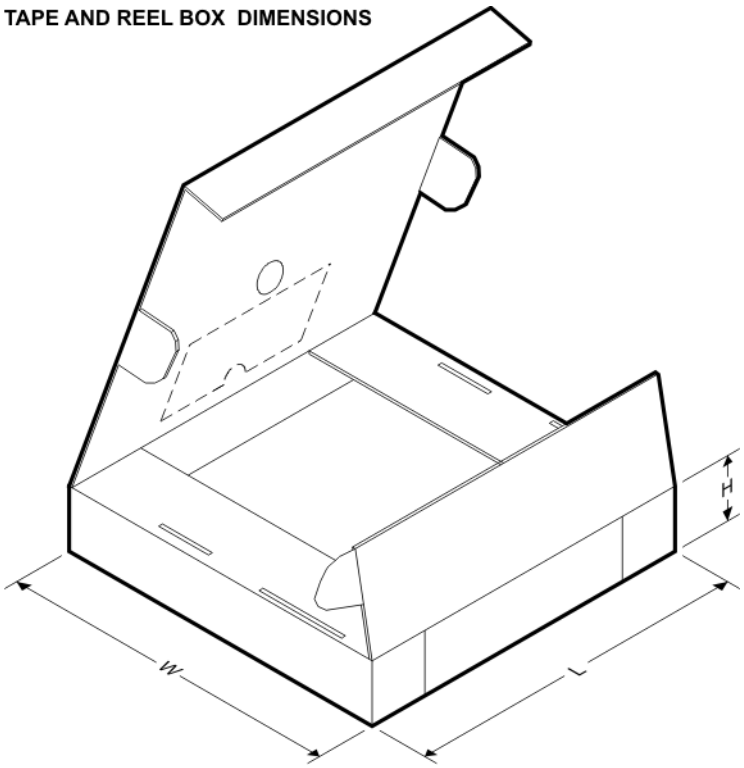

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD4016BM96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4016BMT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4016BNSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4016BPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



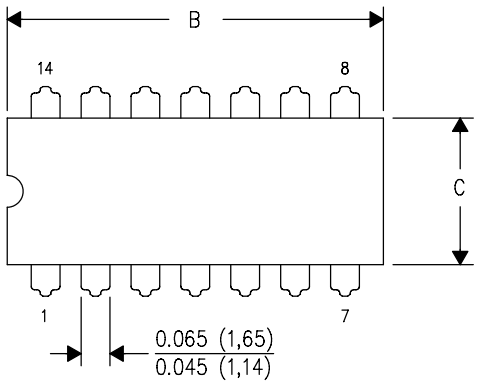

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD4016BM96 | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| CD4016BMT | SOIC | D | 14 | 250 | 367.0 | 367.0 | 38.0 |
| CD4016BNSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| CD4016BPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

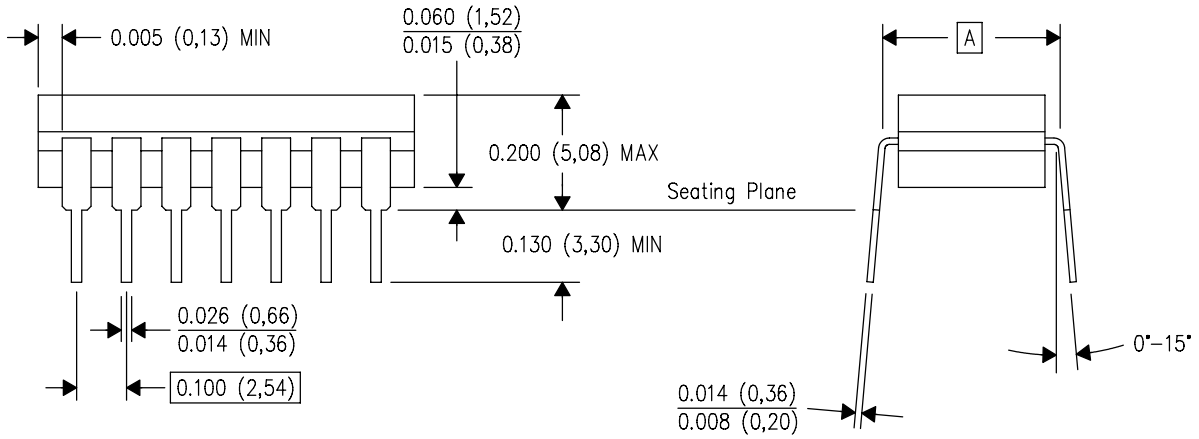
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



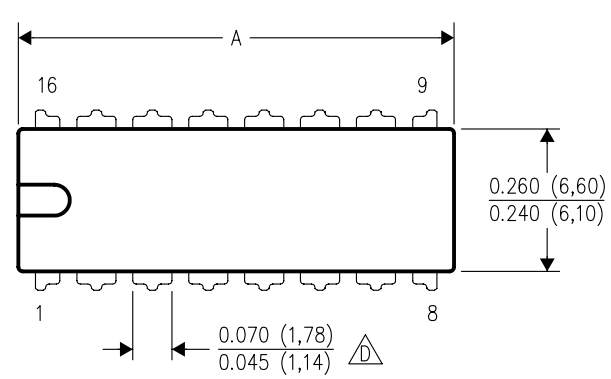

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

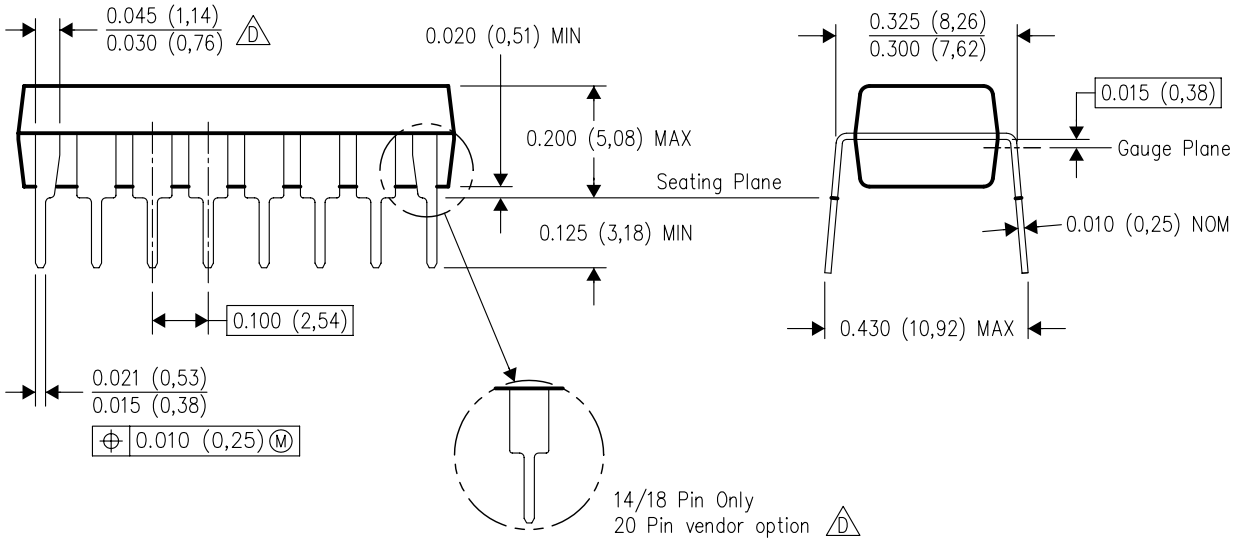
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



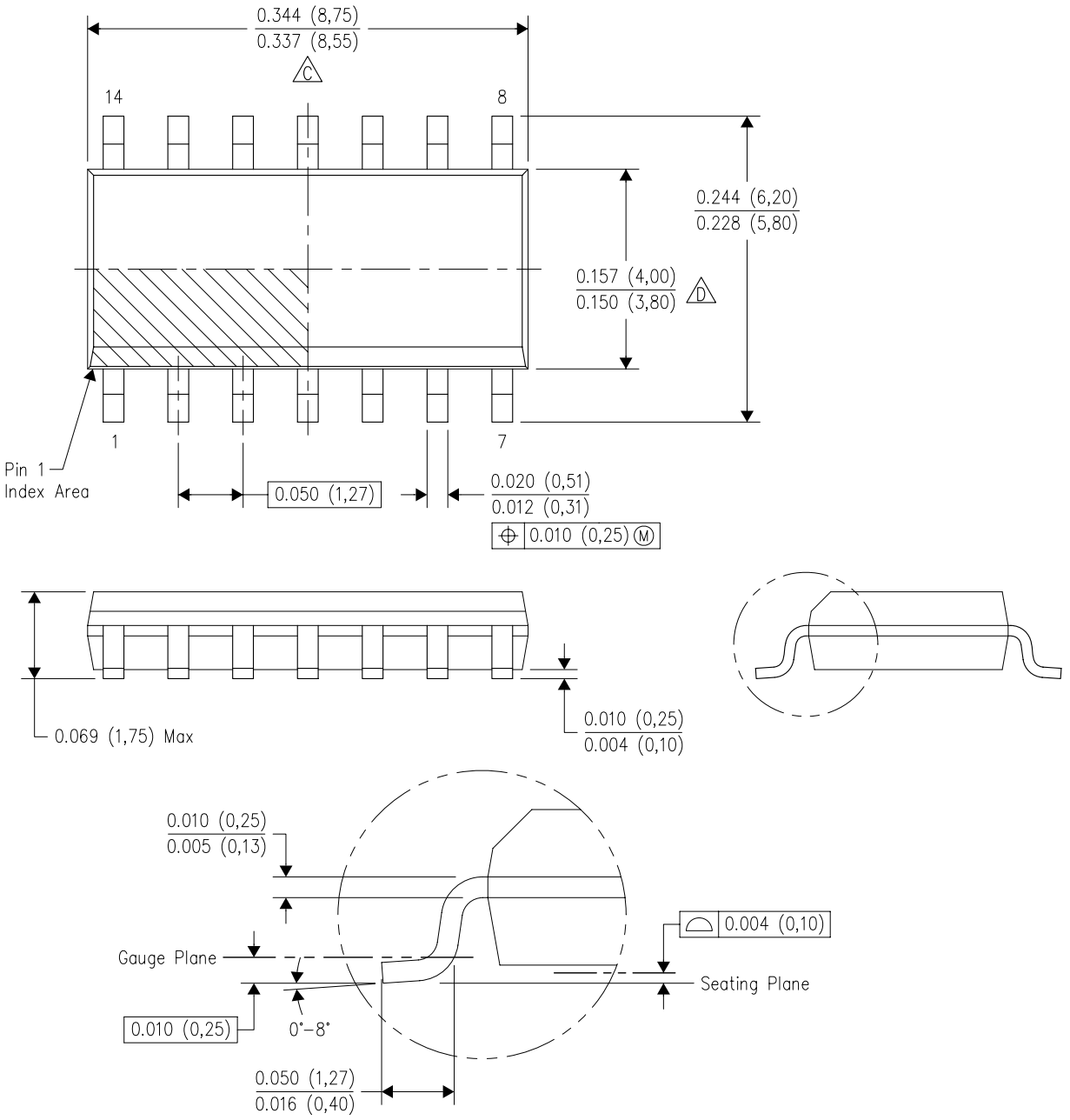

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

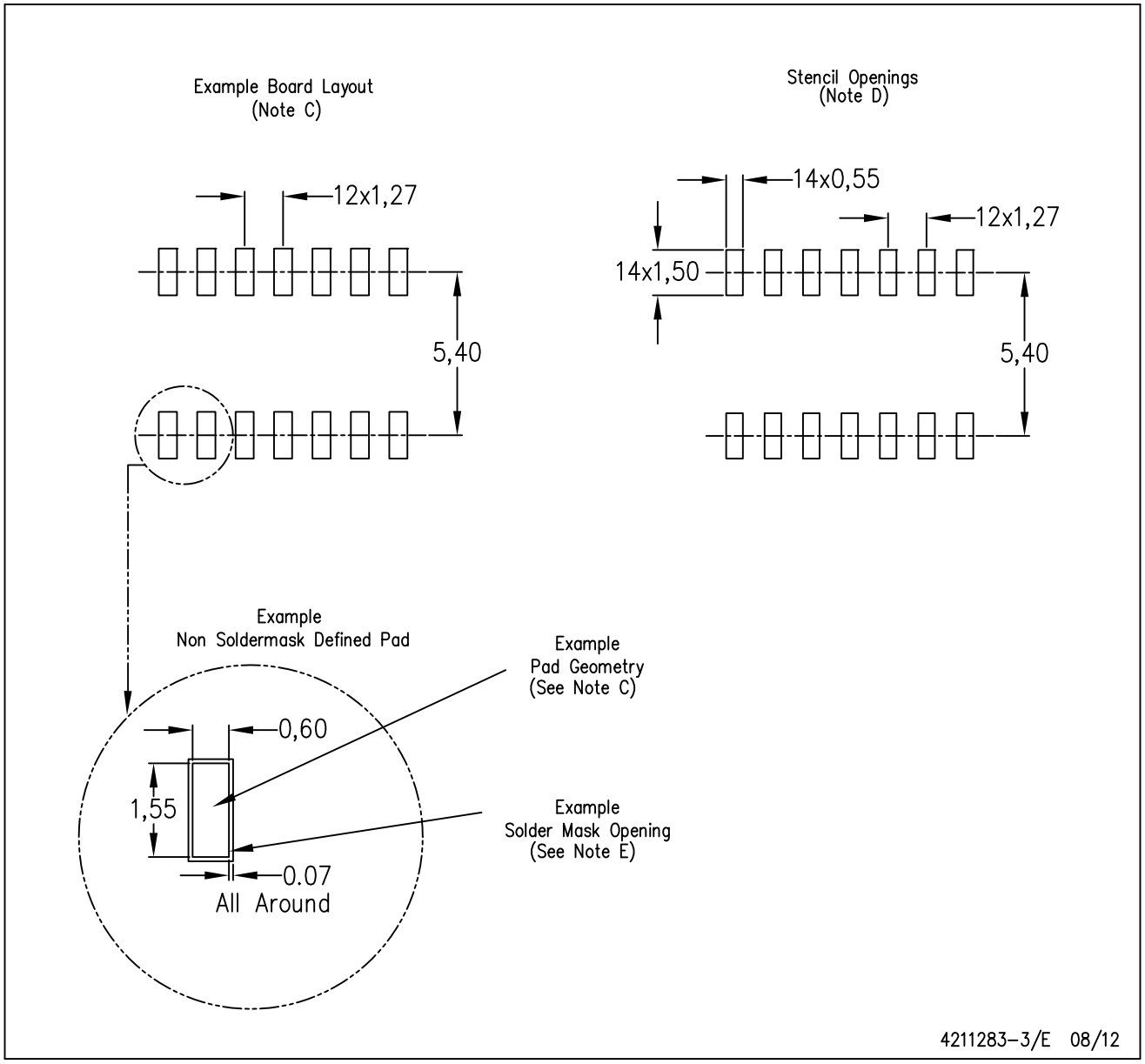
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

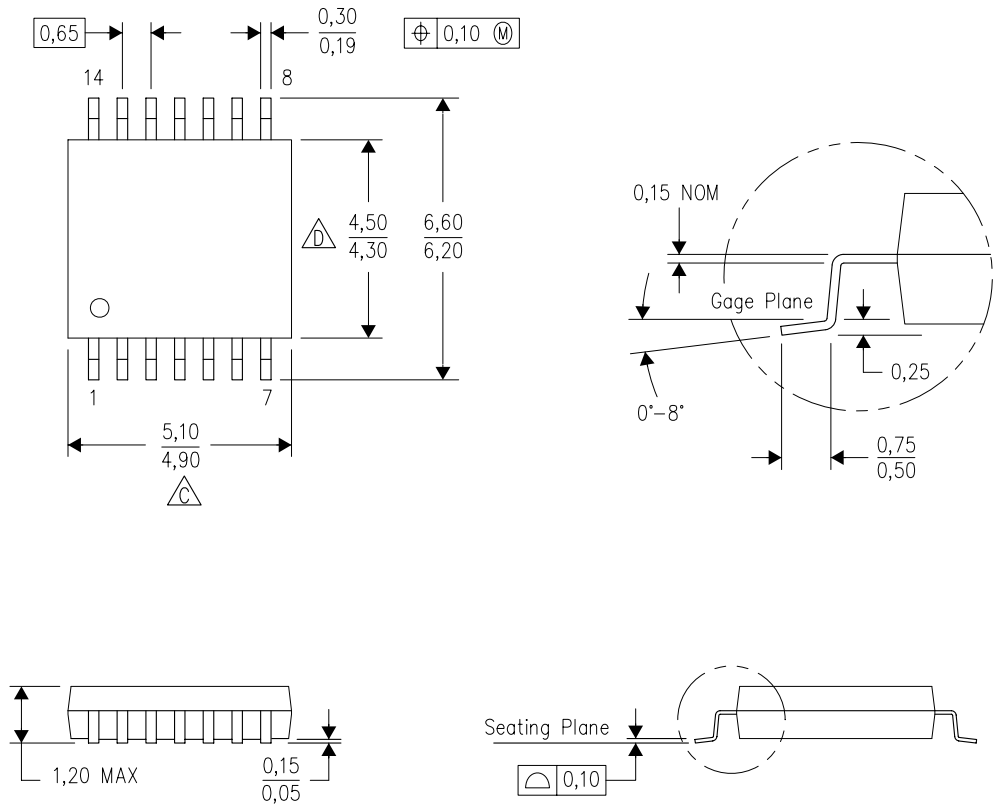
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

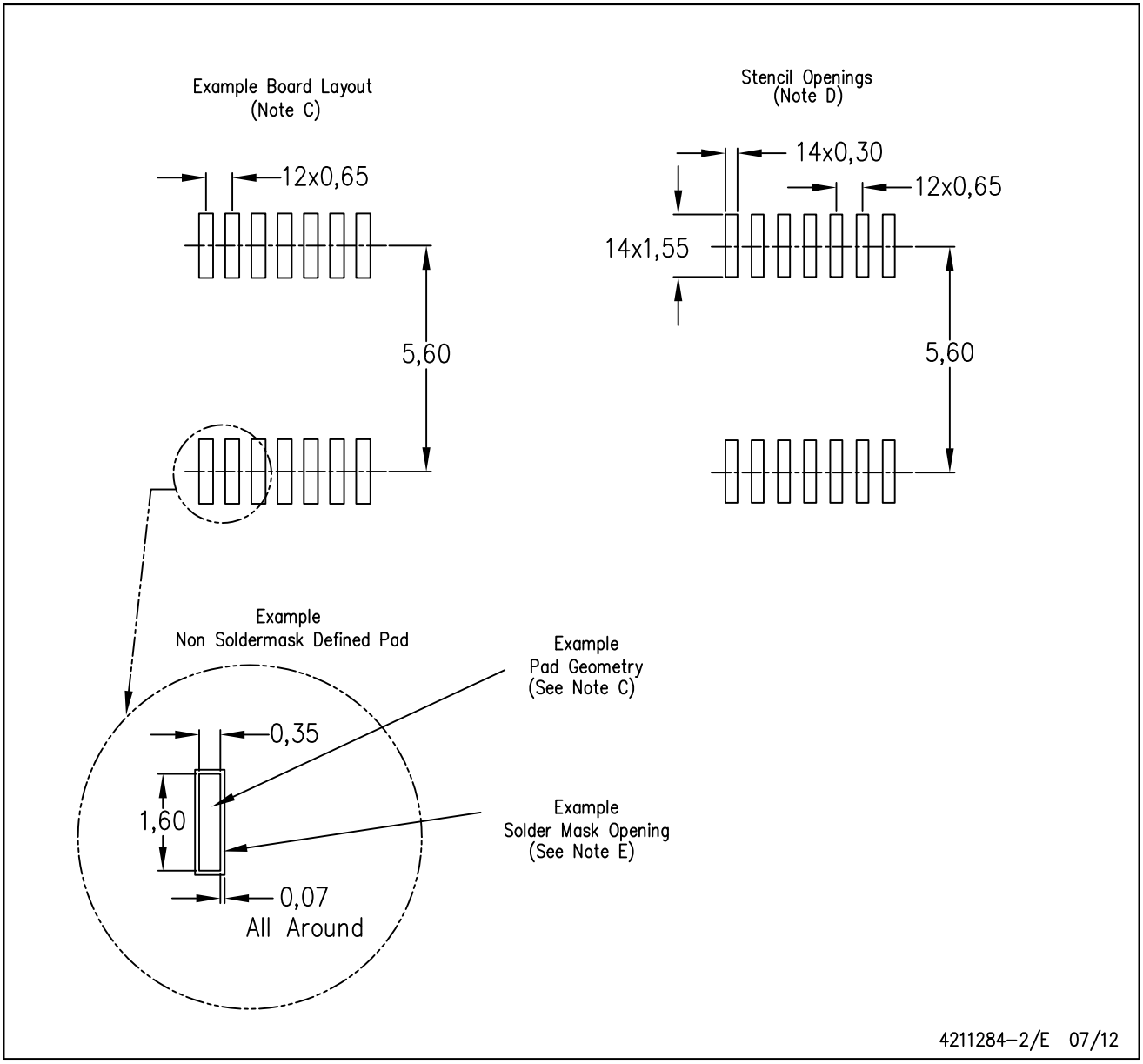
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

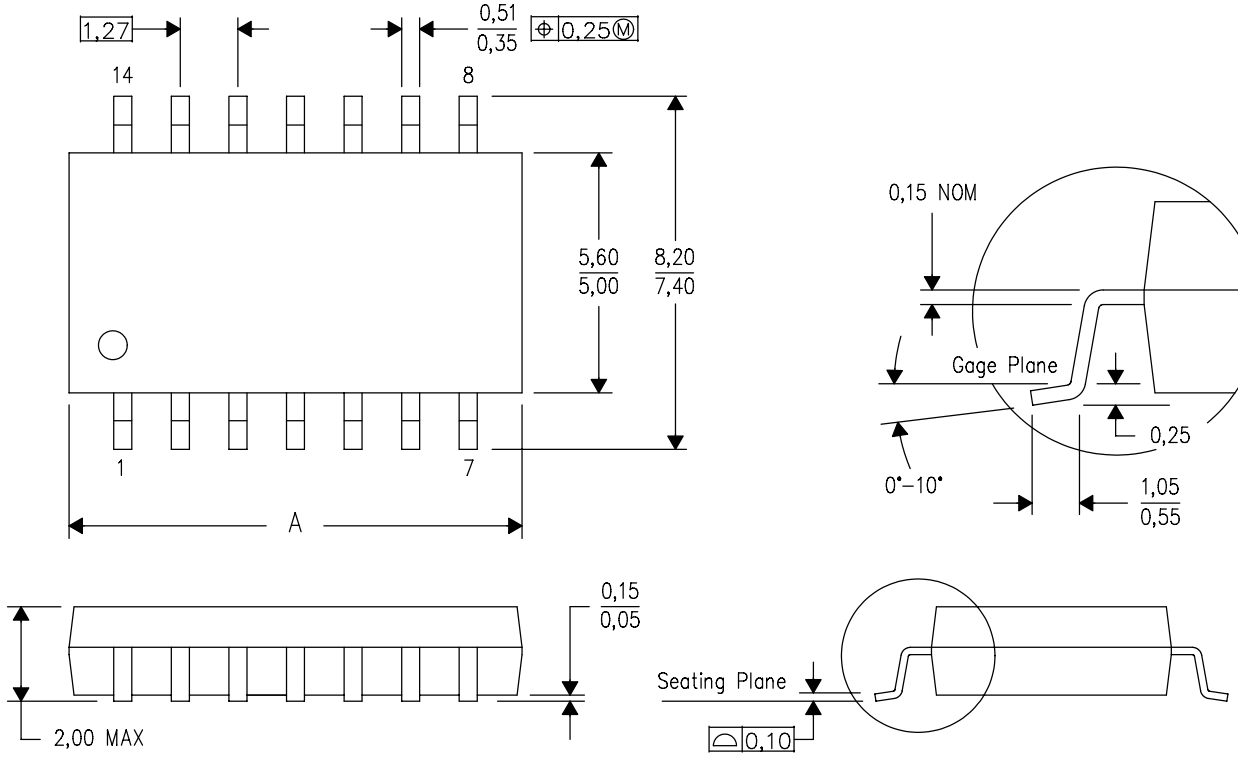



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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# Mouser Electronics

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CD4016BNSR CD4016BM CD4016BE CD4016BM96G4 CD4016BMG4 CD4016BMTG4 CD4016BPWG4 CD4016BPWRG4 CD4016BNSRG4 CD4016BEE4 CD4016BM96 CD4016BM96E4 CD4016BME4 CD4016BMT CD4016BMTE4 CD4016BNSRE4 CD4016BPW CD4016BPWE4 CD4016BPWR CD4016BPWRE4