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UM10430

LPC18xx ARM Cortex-M3 microcontroller

Rev. 00.13 — 20 July 2011 User manual

Document information

Info	Content
Keywords	LPC18xx, LPC1850, LPC1830, LPC1820, LPC1810, LPC1857, LPC1853, LPC1837, LPC1833, LPC1827, LPC1825, LPC1823, LPC1822, LPC1817, LPC1815, LPC1813, LPC1812, LPC1810, ARM Cortex-M3, SPIFI, SCT, USB, Ethernet
Abstract	LPC18xx User manual describing Rev '-' and Rev 'A' version of parts LPC1850/30/20/10 (flashless parts). A preliminary description of parts LPC1857/53/37/33/27/25/23/22/17/15/13/12 (flash-based parts) is included.

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Revision history

Rev	Date	Description
0.13	<tbd>	Preliminary LPC18xx User manual.
Modifications:		• Location of C_CAN1 reset updated in the RGU (see Table 91, Table 93, Table 97). • Pin P2_7 replaced by pin P2_9 as boot pin in Table 107 and Table 8. • Pin P2_7 designated as ISP entry pin in Table 107. • Boot ROM size increased to 64 kB. • Editorial updates. • ISP commands for flashless parts included in Chapter 40.
0.12	<tbd>	Preliminary LPC18xx User manual.
Modifications:		• All content relating to LPC1850/30/20/10 rev '-' moved to Chapter 42. • Repeater and plain input mode swapped in SFSP registers (see Section 42.7.4.1). • Chapter 7 added. • Use of divide-by-two clock for EMC added (Section 19.1). • Bit description of RIT MASK register updated (Table 608). • Overdrive mode removed in bits 1:0 of the PUMUCON register (see Table 32 and Table 918).
0.11	<tbd>	Preliminary LPC18xx User manual.
Modifications:		• Chapter 5, Chapter 6, Chapter 7, Chapter 14, Chapter 35 added.
0.10	<tbd>	Preliminary LPC18xx User manual.
Modifications:		• Chapter 14, Chapter 9, Chapter 13, Chapter 15 added.
0.09	<tbd>	Preliminary LPC18xx User manual.
Modifications:		• Register bit description and functional description removed in Chapter 17. API calls to be added. • Description of MSGVAL bit updated in Table 757. • MAC_RWAKE_FRFLT register cannot used with bit-banding. See Table 413. • Description of RMII and MII pins corrected in Table 401. • Description of Ethernet function in pins P1_16 and PC_8 updated. • AES description removed Chapter 4 "LPC18xx Security features". • CGU PLL0 output updated in Table 107. • In Table 175, Pin PC_0: Change function 0 to n.c. and move ENET_RX_CLK to function 3. • In Table 175, remove all SDIO functions. • In Table 175, change CAN1_RD, CAN1_TD to CAN_RD, CAN_TD. • Polarity of the ENABLE bit updated in Table 112 (1= power-down). • WIC replaced by Event router throughout the manual.

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Revision history *...continued*

Rev	Date	Description
0.08	<tbd>	Preliminary LPC18xx User manual.
Modifications:		• Updated the reference clock for the frequency monitor register (Section 12.6.1). • Description of RTC calibration updated (Section 31.7.1). • USB0 clock source description added to Table 294. • USB1 clock source description added to Table 358. • Boot source bit 3 (pin P2_7) and USB0/1 boot modes added to Table 7 and Table 8. • Add SRAM control register ETBCFG in CREG block (Table 36). • RTC initialization steps updated (Section 31.2). • Access of LCD controller to SRAM updated (Section 23.7.1.1 and Section 23.7.1.2). • ADC measurement range corrected (Section 38.3). • GPDMA, CxCONTROL register: bits TRANSFERSIZE are given in number of transfers (Table 214). • Chapter 4 “LPC18xx Security features” added. • Pin configuration updated (Table 175). • Flash parts added (see Chapter 1 “Introductory information” and Chapter 2 “LPC18xx Memory mapping”. • Chapter 40 “LPC18xx flash programming interface” added.
0.07	<tbd>	Preliminary LPC18xx User manual.

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1.1 Introduction

The LPC18xx are ARM Cortex-M3 based microcontrollers for embedded applications. The ARM Cortex-M3 is a next generation core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration.

The LPC18xx operate at CPU frequencies of up to 150 MHz. The ARM Cortex-M3 CPU incorporates a 3-stage pipeline and uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals. The ARM Cortex-M3 CPU also includes an internal prefetch unit that supports speculative branching.

The LPC18xx include up to 200 kB of on-chip SRAM data memory (flashless parts) or up to 136 kB of on-chip SRAM and up to 1 MB of flash (parts with on-chip flash), a quad SPI Flash Interface (SPIFI), a State Configurable Timer (SCT) subsystem, two High-speed USB controllers, Ethernet, LCD, an external memory controller, and multiple digital and analog peripherals.

Remark: This user manual describes the Rev '-' and Rev 'A' versions of parts LPC1850/30/20/10 (flashless parts) and provides a preliminary description of the flash-based LPC18xx parts.

The following peripherals are available on LPC1350/30/20/10 Rev 'A' only:

- I2S1
- C_CAN1
- GPIO pin interrupts
- GPIO group interrupt 0/1
- Global Input Multiplexer Array (GIMA)

1.2 Features

- Processor core
  - ARM Cortex-M3 processor, running at frequencies of up to 150 MHz.
  - ARM Cortex-M3 built-in Memory Protection Unit (MPU) supporting eight regions.
  - ARM Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input.
  - JTAG and Serial Wire Debug, serial trace, eight breakpoints, and four watch points.
  - ETM and ETB support.
  - System tick timer.
- On-chip memory (flashless parts LPC1850/30/20/10)
  - Up to 200 kB SRAM total for code and data use.

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- Two 32 kB SRAM blocks with separate bus access. Both SRAM blocks can be powered down individually.
- 64 kB ROM containing boot code and on-chip software drivers.
- 32-bit One-Time Programmable (OTP) memory for general-purpose customer use.

• On-chip memory (parts with on-chip flash)
  - Up to 1 MB total dual bank flash memory with flash accelerator.
  - In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
  - Up to 136 kB SRAM for code and data use.
  - Two 32 kB SRAM blocks with separate bus access. Both SRAM blocks can be powered down individually.
  - 32 kB ROM containing boot code and on-chip software drivers.
  - 32-bit One-Time Programmable (OTP) memory for general-purpose customer use.

• Clock generation unit
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy.
  - Ultra-low power RTC crystal oscillator.
  - Three PLLs allow CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. The second PLL is dedicated to the High-speed USB, the third PLL can be used as audio PLL.
  - Clock output.

• Serial interfaces:
  - Quad SPI Flash Interface (SPIFI) with four lanes and data rates of up to 40 MB per second total.
  - 10/100T Ethernet MAC with RMII and MII interfaces and DMA support for high throughput at low CPU load. Support for IEEE 1588 time stamping/advanced time stamping (IEEE 1588-2008 v2).
  - One High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip PHY.
  - One High-speed USB 2.0 Host/Device interface with DMA support, on-chip full-speed PHY and ULPI interface to external high-speed PHY.
  - USB interface electrical test software included in ROM USB stack.
  - Four 550 UARTs with DMA support: one UART with full modem interface; one UART with IrDA interface; three USARTs support synchronous mode and a smart card interface conforming to ISO7816 specification.
  - Two C_CAN 2.0B controllers with one channel each.
  - Two SSP controllers with FIFO and multi-protocol support. Both SSPs with DMA support.
  - One Fast-mode Plus I^2C-bus interface with monitor mode and with open-drain I/O pins conforming to the full I^2C-bus specification. Supports data rates of up to 1 Mbit/s.
  - One standard I^2C-bus interface with monitor mode and standard I/O pins.

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- Two I^2S interfaces with DMA support, each with one input and one output.

- Digital peripherals:
  - External Memory Controller (EMC) supporting external SRAM, ROM, NOR flash, and SDRAM devices.
  - LCD controller with DMA support and a programmable display resolution of up to 1024H × 768V. Supports monochrome and color STN panels and TFT color panels; supports 1/2/4/8 bpp CLUT and 16/24-bit direct pixel mapping.
  - SD/MMC card interface.
  - Eight-channel General-Purpose DMA (GPDMA) controller can access all memories on the AHB and all DMA-capable AHB slaves.
  - Up to 80 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors and open-drain modes.
  - GPIO registers are located on the AHB for fast access. GPIO ports have DMA support.
  - State Configurable Timer (SCT) subsystem on AHB.
  - Four general-purpose timer/counters with capture and match capabilities.
  - One motor control PWM for three-phase motor control.
  - One Quadrature Encoder Interface (QEI).
  - Repetitive Interrupt timer (RI timer).
  - Windowed watchdog timer.
  - Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
  - Alarm timer; can be battery powered.

- Digital peripherals available on flash-based parts LPC18xx only:
  - <tbd>

- Analog peripherals:
  - One 10-bit DAC with DMA support and a data conversion rate of 400 kSamples/s.
  - Two 10-bit ADCs with DMA support and a data conversion rate of 400 kSamples/s.

- Security:
  - Hardware-based AES security engine programmable through an on-chip API.
  - Two 128-bit secure OTP memories for AES key storage and customer use.
  - Unique ID for each device.

- Power:
  - Single 3.3 V (2.2 V to 3.6 V) power supply with on-chip internal voltage regulator for the core supply and the RTC power domain.
  - RTC power domain can be powered separately by a 3 V battery supply.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Sleep mode via wake-up interrupts from various peripherals.

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– Wake-up from Deep-sleep, Power-down, and Deep power-down modes via external interrupts and interrupts generated by battery powered blocks in the RTC power domain.
– Brownout detect with four separate thresholds for interrupt and forced reset.
– Power-On Reset (POR).

- Available as 100-pin, 144-pin, and 208-pin LQFP packages and as 100-pin, 180-pin, and 256-pin LBGA packages.

1.3 Ordering information (flashless parts LPC1850/30/20/10)

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1850FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	sot740-2
LPC1850FET180	TFBGA180	Thin fine-pitch ball grid array package; 180 balls	sot570-3
LPC1850FBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm	sot459-1
LPC1830FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	sot740-2
LPC1830FET180	TFBGA180	Thin fine-pitch ball grid array package; 180 balls	sot570-3
LPC1830FET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm	sot926-1
LPC1830FBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm	sot486-1
LPC1820FET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm	sot926-1
LPC1820FBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm	sot486-1
LPC1820FBD100	LQFP100	Plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm	sot407-1
LPC1810FET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm	sot926-1

Table 2. Ordering options

Type number	Total SRAM	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)	GPIO	Package
LPC1850FET256	200 kB	yes	yes	yes	yes	164	LBGA256
LPC1850FET180	200 kB	yes	yes	yes	yes	118	TFBGA180
LPC1850FBD208	200 kB	yes	yes	yes	yes	164	LQFP208
LPC1830FET256	200 kB	no	yes	yes	yes	164	LBGA256
LPC1830FET180	200 kB	no	yes	yes	yes	118	TFBGA180
LPC1830FET100	200 kB	no	yes	yes	yes	49	TFBGA100
LPC1830FBD144	200 kB	no	yes	yes	yes	83	LQFP144
LPC1820FET100	168 kB	no	no	yes	no	49	TFBGA100
LPC1820FBD144	168 kB	no	no	yes	no	83	LQFP144
LPC1820FBD100	168 kB	no	no	yes	no	49	LQFP100
LPC1810FET100	136 kB	no	no	no	no	49	TFBGA100

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1.4 Ordering information (parts with on-chip flash)

Table 3. Ordering information (parts with on-chip flash)

Type number	Package		
	Name	Description	Version
LPC1857FET256	LBGA256	plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	sot740-2
LPC1857	LQFP208	<tbd>	<tbd>
LPC1857	BGA180	<tbd>	<tbd>
LPC1837FET256	LBGA256	plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	sot740-2
LPC1837	LQFP208	<tbd>	<tbd>
LPC1837	BGA180	<tbd>	<tbd>
LPC1827	LQFP144	<tbd>	<tbd>
LPC1827FET100	BGA100	<tbd>	<tbd>
LPC1825	LQFP144	<tbd>	<tbd>
LPC1825FET100	BGA100	<tbd>	<tbd>
LPC1823	LQFP144	<tbd>	<tbd>
LPC1823FET100	BGA100	<tbd>	<tbd>
LPC1822	LQFP144	<tbd>	<tbd>
LPC1822FET100	BGA100	<tbd>	<tbd>
LPC1817	LQFP144	<tbd>	<tbd>
LPC1817FET100	BGA100	<tbd>	<tbd>
LPC1815	LQFP144	<tbd>	<tbd>
LPC1815FET100	BGA100	<tbd>	<tbd>
LPC1813	LQFP144	<tbd>	<tbd>
LPC1813FET100	BGA100	<tbd>	<tbd>
LPC1811	LQFP144	<tbd>	<tbd>
LPC1811FET100	BGA100	<tbd>	<tbd>

Table 4. Ordering options (parts with on-chip flash)

Type	SRAM total	Flash total	Flash bank A	Flash bank B	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)	Packages
LPC1857	136 kB	1 MB	512 kB	512 kB	yes	yes	yes	yes	LBGA256; BGA180; LQFP208
LPC1853	136 kB	512 kB	256 kB	256 kB	yes	yes	yes	yes	LBGA256; BGA180; LQFP208
LPC1837	136 kB	1 MB	512 kB	512 kB	no	yes	yes	yes	LBGA256; BGA180; LQFP208
LPC1833	136 kB	512 kB	256 kB	256 kB	no	yes	yes	yes	LBGA256; BGA180; LQFP208
LPC1827	136 kB	1 MB	512 kB	512 kB	no	no	yes	no	LQFP144; BGA100
LPC1825	136 kB	768 kB	384 kB	384 kB	no	no	yes	no	LQFP144; BGA100
LPC1823	104 kB	512 kB	256 kB	256 kB	no	no	yes	no	LQFP144; BGA100
LPC1822	104 kB	512 kB	512 kB	0	no	no	yes	no	LQFP144; BGA100

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Table 4. Ordering options (parts with on-chip flash)

Type	SRAM total	Flash total	Flash bank A	Flash bank B	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)	Packages
LPC1817	136 kB	1 MB	512 kB	512 kB	no	no	no	no	LQFP144; BGA100
LPC1815	136 kB	768 kB	384 kB	384 kB	no	no	no	no	LQFP144; BGA100
LPC1813	104 kB	512 kB	256 kB	256 kB	no	no	no	no	LQFP144; BGA100
LPC1812	104 kB	512 kB	512 kB	0	no	no	no	no	LQFP144; BGA100

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1.5 Block diagram (flashless parts LPC1850/30/20/10)

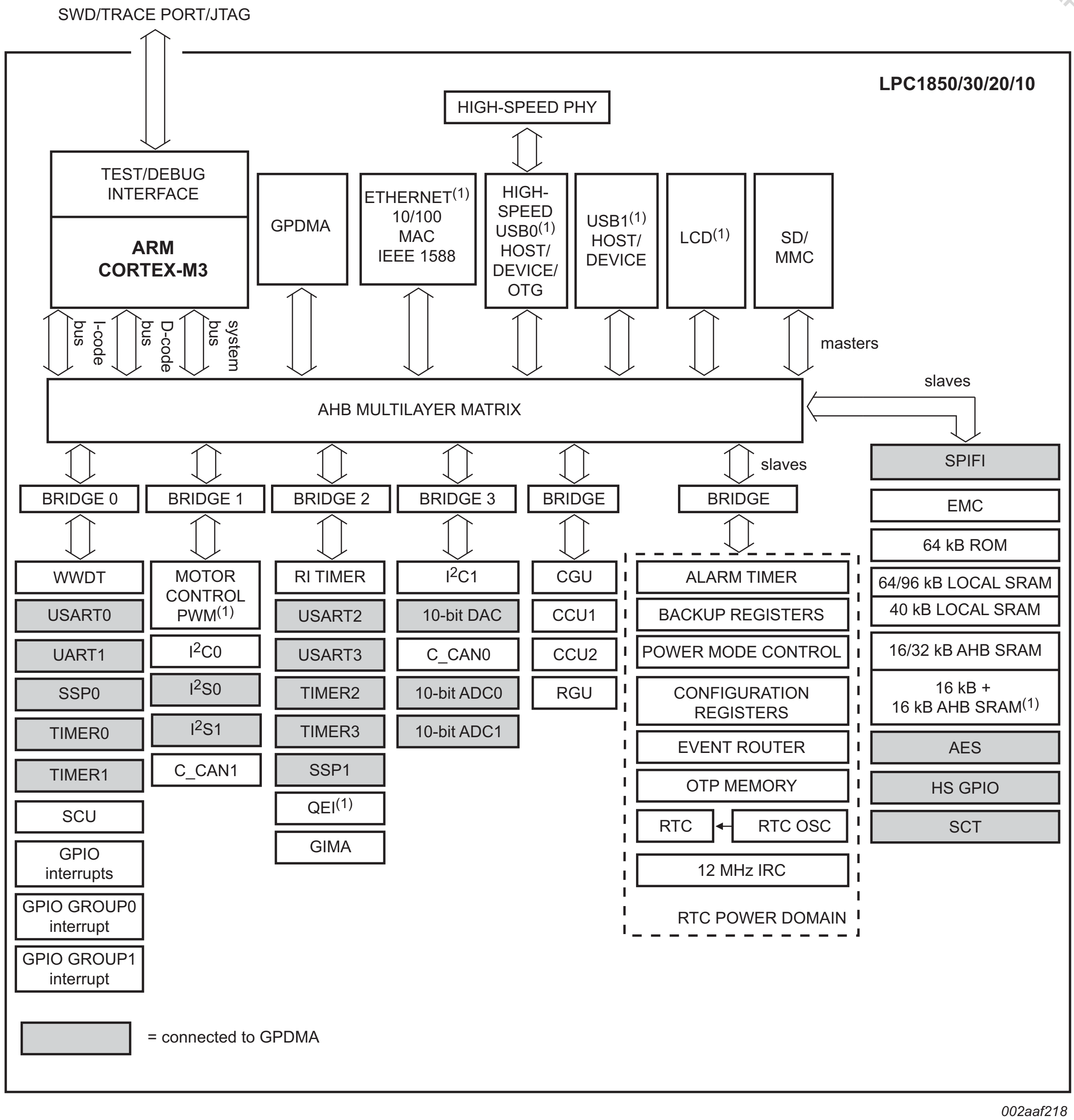


Fig 1. LPC18xx Block diagram (flashless parts)

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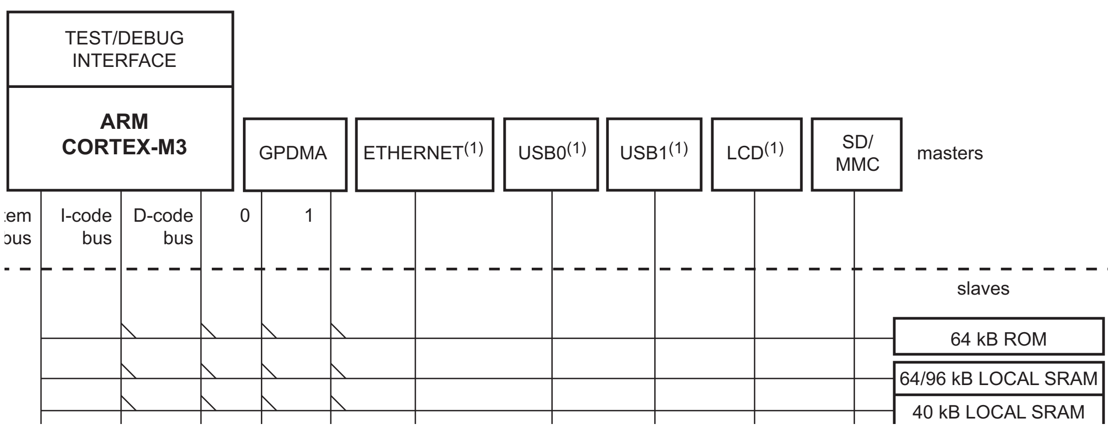
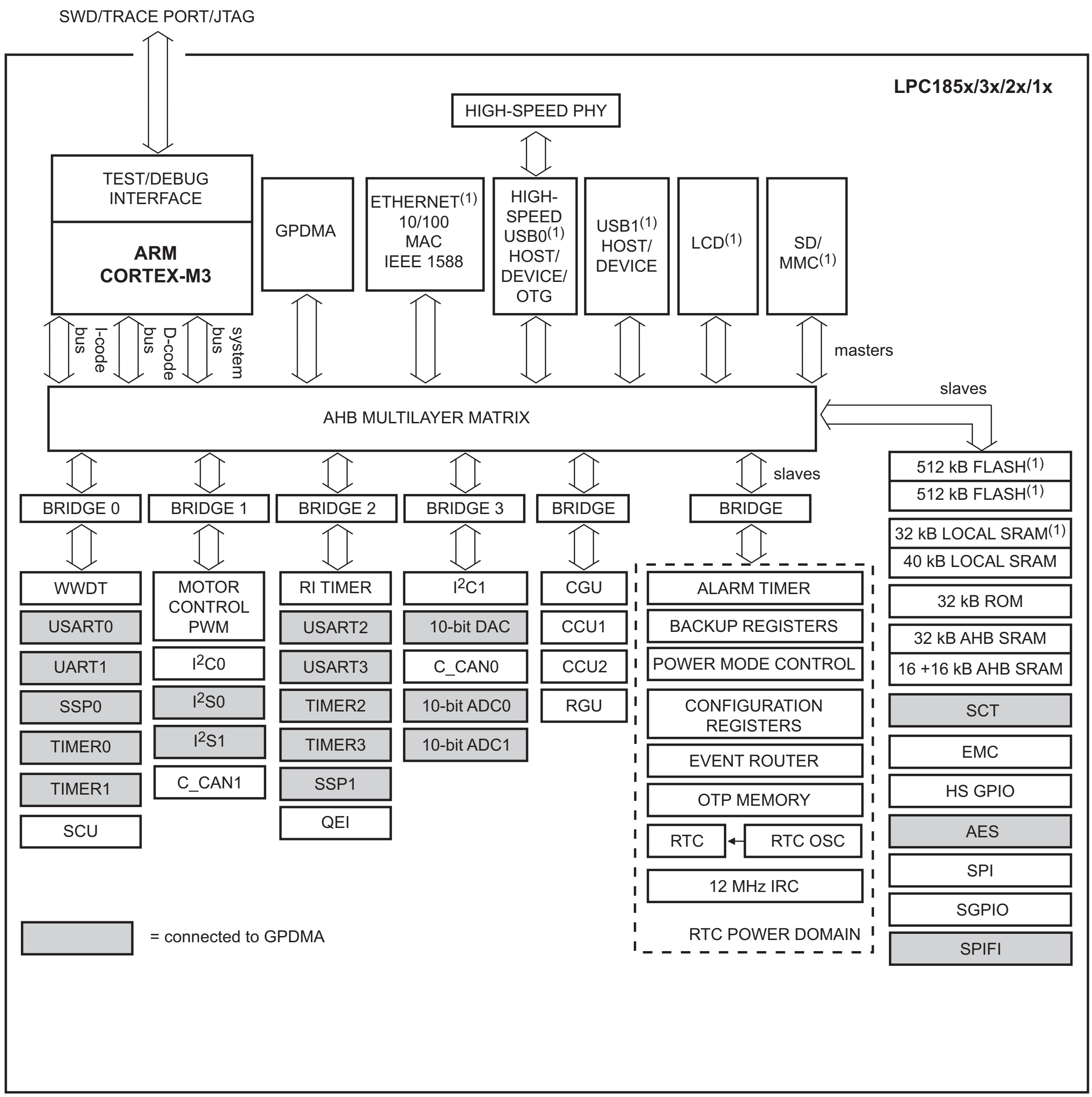


Fig 2. LPC18xx AHB multilayer matrix connections (flashless parts)

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1.6 Block diagram (parts with on-chip flash)

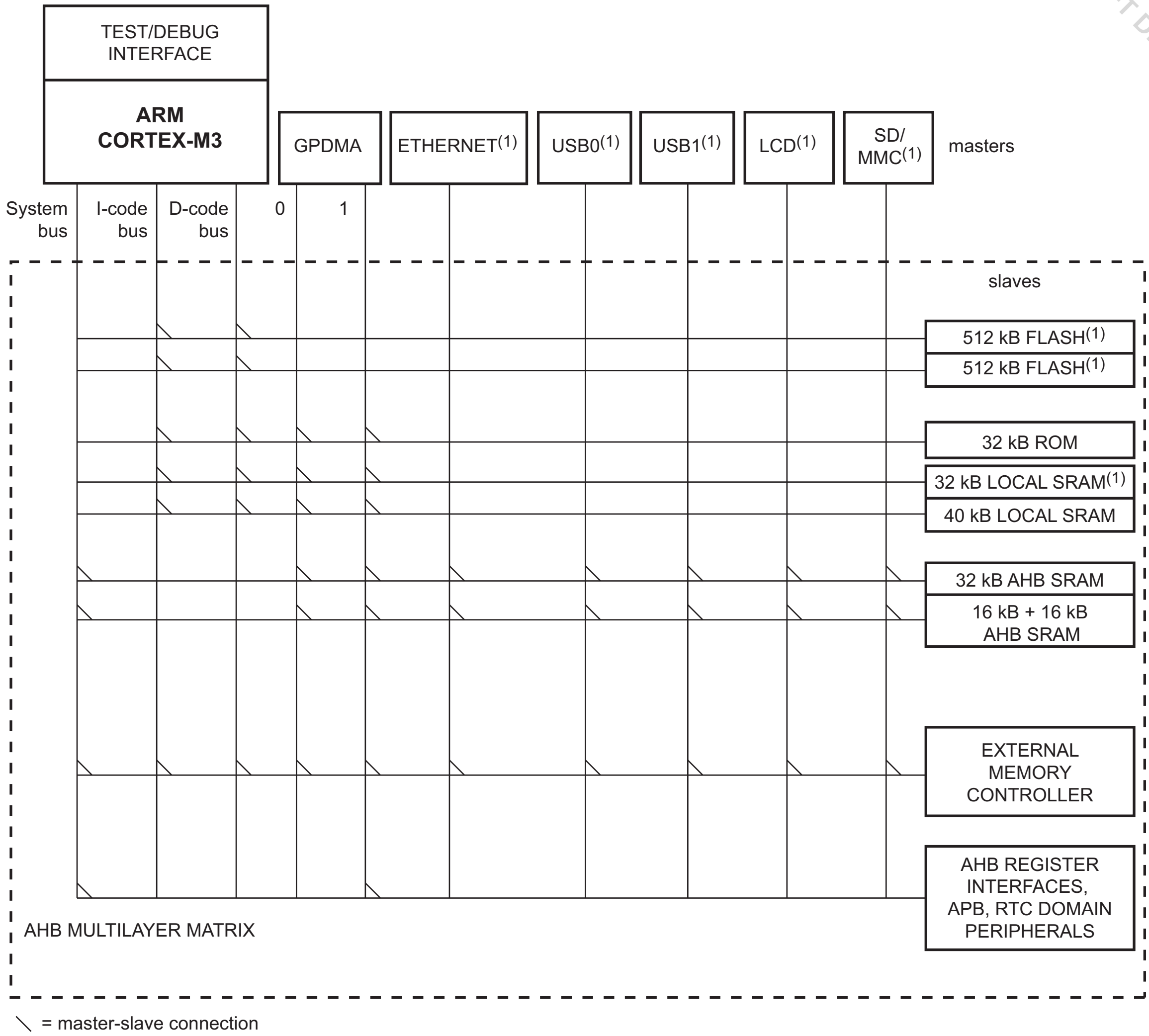


(1) Not available on all parts (see Table 4).

Fig 3. LPC185x/3x/2x/1x block diagram (parts with on-chip flash)

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(1) Not available on all parts (see Table 4).

Fig 4. AHB multilayer matrix master and slave connections

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2.1 How to read this chapter

The available peripherals and their memories vary for different parts.

- Ethernet: available on LPC185x/3x.
- USB0: available on LPC185x/3x/2x.
- USB1: available on LPC185x/3x.
- SRAM: see Table 5.
- Flash: see Table 6.

The registers and memory regions corresponding to unavailable peripheral and memory blocks are reserved.

The following memory blocks are available on LPC1350/30/20/10 Rev ‘A’ only:

- I2S1 at address 0x400A 3000.
- C_CAN1 at address 0x400A 4000.
- GPIO pin interrupts 0x4008 7000.
- GPIO group interrupt 0/1 at addresses 0x4008 8000 and 0x4008 9000.
- High-speed GPIO at address 0x400F 4000 (on parts LPC1850/30/20/10 Rev ‘-’ parts, the GPIO block resides at address 0x400F 0000).
- Global Input Multiplexer Array (GIMA) at address 0x400C 7000.

2.2 Basic configuration

In the CREG block (see Table 36), select the interface to access the 16 kB block of RAM located at address 0x2000 C000. This RAM memory block can be accessed either by the ETB (this is the default) or be used as normal SRAM on the AHB bus.

2.3 Memory configuration

2.3.1 On-chip static RAM

The LPC18xx support up to 136 kB SRAM (parts with on-chip flash) or up to 200 kB SRAM (flashless parts LPC1850/30/20/10) with separate bus master access for higher throughput and individual power control for low power operation.

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Table 5. LPC185x/3x/2x/1x SRAM configuration

Part	Local SRAM 0x1000 0000	Local SRAM 0x1001 0000	Local SRAM 0x1008 0000	Local SRAM 0x1008 8000	AHB SRAM 0x2000 0000	AHB SRAM 0x2000 8000	AHB SRAM 0x2000 C000	
LPC1850	64 kB	32 kB	32 kB	8 kB	32 kB	16 kB	16 kB	Figure 5
LPC1830	64 kB	32 kB	32 kB	8 kB	32 kB	16 kB	16 kB	Figure 5
LPC1820	64 kB	32 kB	32 kB	8 kB	16 kB	-	16 kB	Figure 5
LPC1810	64 kB	-	32 kB	8 kB	16 kB	-	16 kB	Figure 5
LPC1857	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	Figure 7
LPC1853	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	Figure 7
LPC1837	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	Figure 7
LPC1833	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	Figure 7
LPC1827	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	Figure 7
LPC1825	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	Figure 7
LPC1823	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	Figure 7
LPC1822	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	Figure 7
LPC1817	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	Figure 7
LPC1815	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	Figure 7
LPC1813	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	Figure 7
LPC1812	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	Figure 7

2.3.2 On-chip flash

The available flash configuration for the LPC185x/3x/2x/1x is shown in Table 6. A flash accelerator maximizes performance for use with the two fast AHB buses.

Table 6. LPC185x/3x/2x/1x Flash configuration

Part	Flash bank A 256 kB 0x1A00 0000	Flash bank A 128 kB 0x1A04 000	Flash bank A 128 kB 0x1A0 6000	Flash bank B 256 kB 0x1B00 0000	Flash bank B 128 kB 0x1B04 000	Flash bank B 128 kB 0x1B0 6000
LPC1857	yes	yes	yes	yes	yes	yes
LPC1853	yes	no	no	yes	no	no
LPC1837	yes	yes	yes	yes	yes	yes
LPC1833	yes	no	no	yes	no	no
LPC1827	yes	yes	yes	yes	yes	yes
LPC1825	yes	yes	no	yes	yes	no
LPC1823	yes	no	no	yes	no	no
LPC1822	yes	yes	yes	no	no	no
LPC1817	yes	yes	yes	yes	yes	yes

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Table 6. LPC185x/3x/2x/1x Flash configuration

Part	Flash bank A 256 kB 0x1A00 0000	Flash bank A 128 kB 0x1A04 000	Flash bank A 128 kB 0x1A0 6000	Flash bank B 256 kB 0x1B00 0000	Flash bank B 128 kB 0x1B04 000	Flash bank B 128 kB 0x1B0 6000
LPC1815	yes	yes	no	yes	yes	no
LPC1813	yes	no	no	yes	no	no
LPC1812	yes	yes	yes	no	no	no

2.3.3 Bit banding

Remark: Bit banding can not be used with the MAC_RWAKE_FRFLT register (see Section 22.6.10).

2.4 General description

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2.5 Memory map (flashless parts LPC1850/30/20/10)

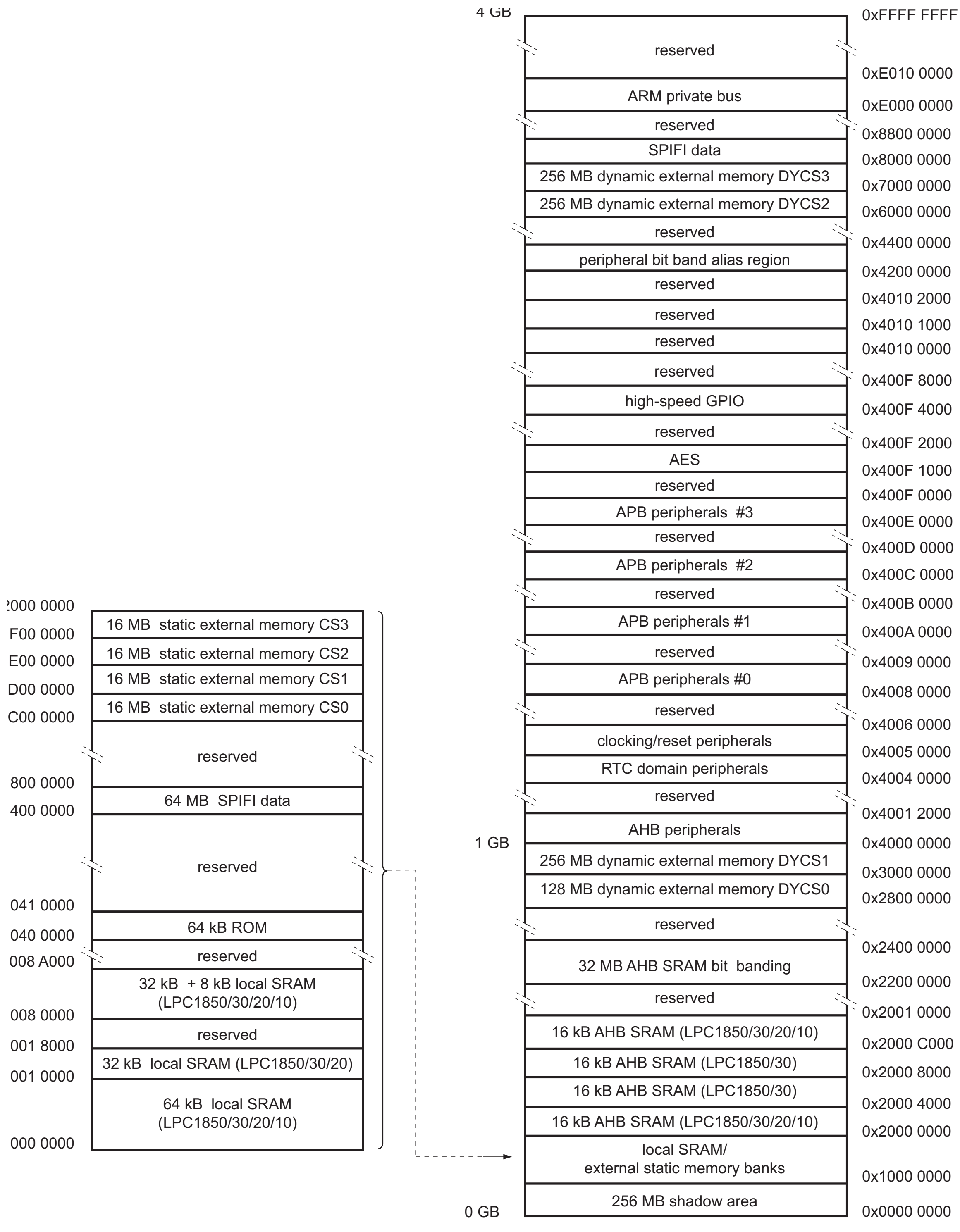


Fig 5. System memory map - flashless parts LPC1850/30/20/10 (see Figure 6 for detailed addresses of all peripherals)

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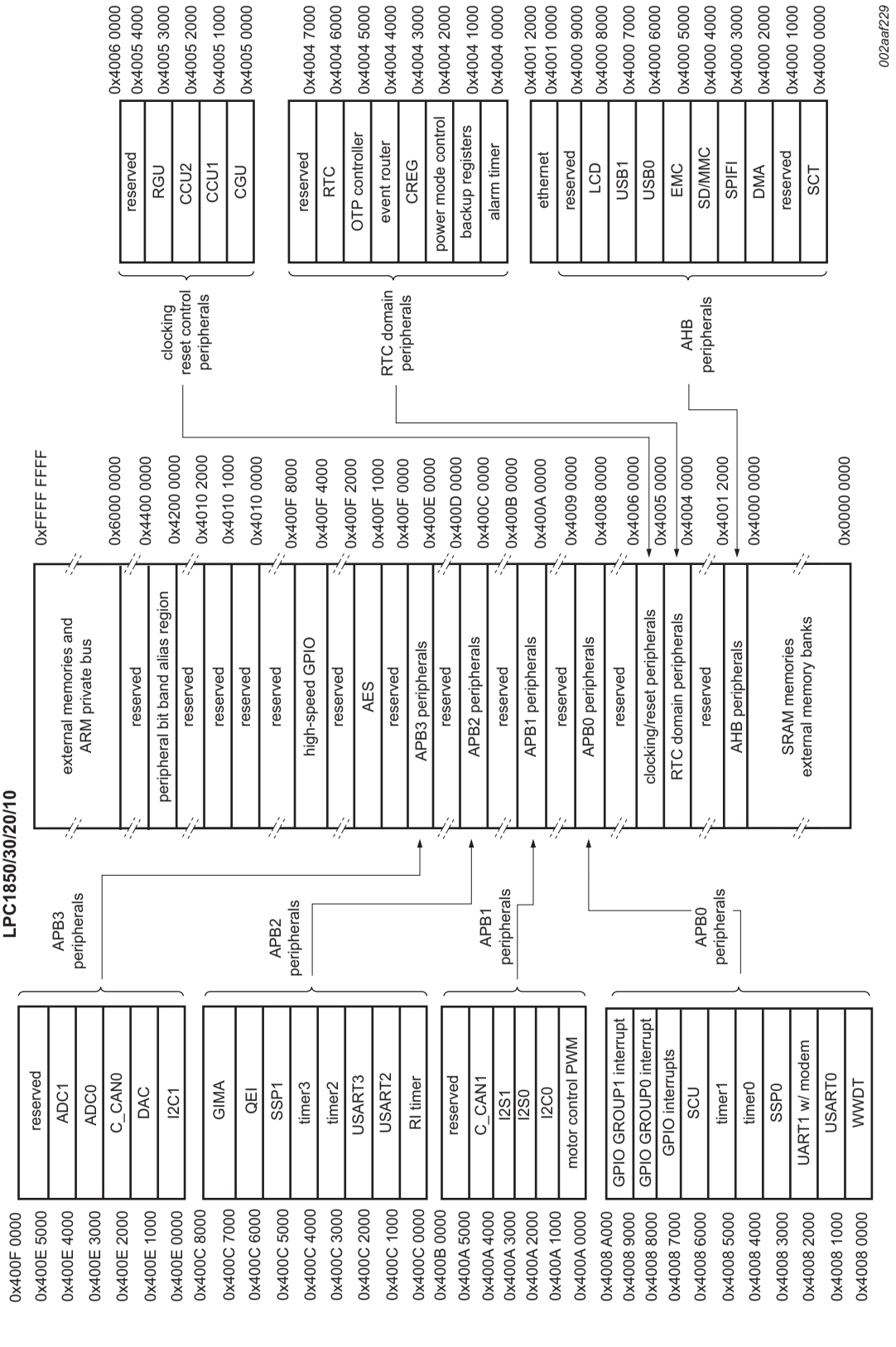


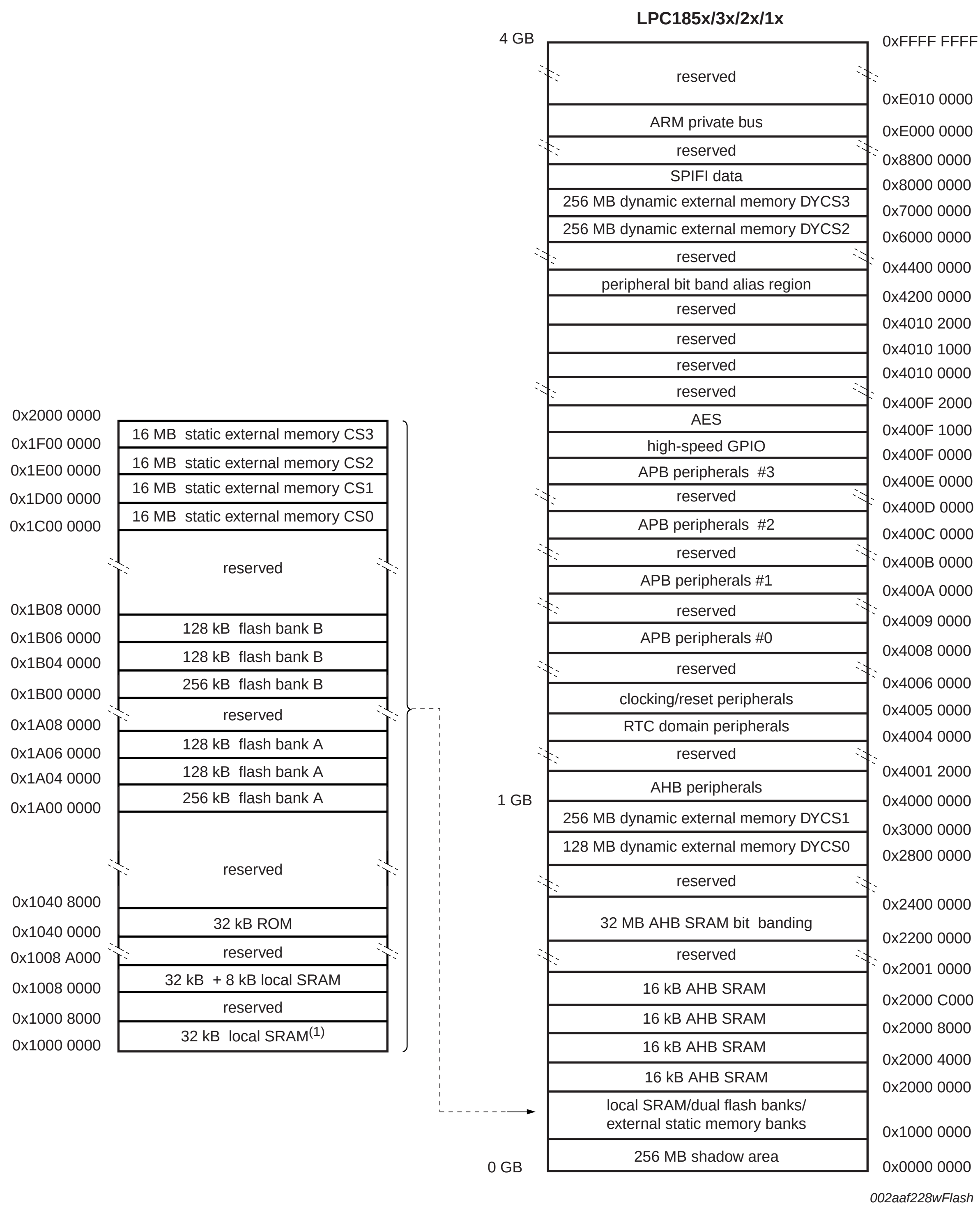
Fig 6. Memory map with peripherals - flashless parts LPC1850/30/20/10 (see Figure 5 for detailed addresses of memory blocks)

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2.6 Memory map (parts with on-chip flash)

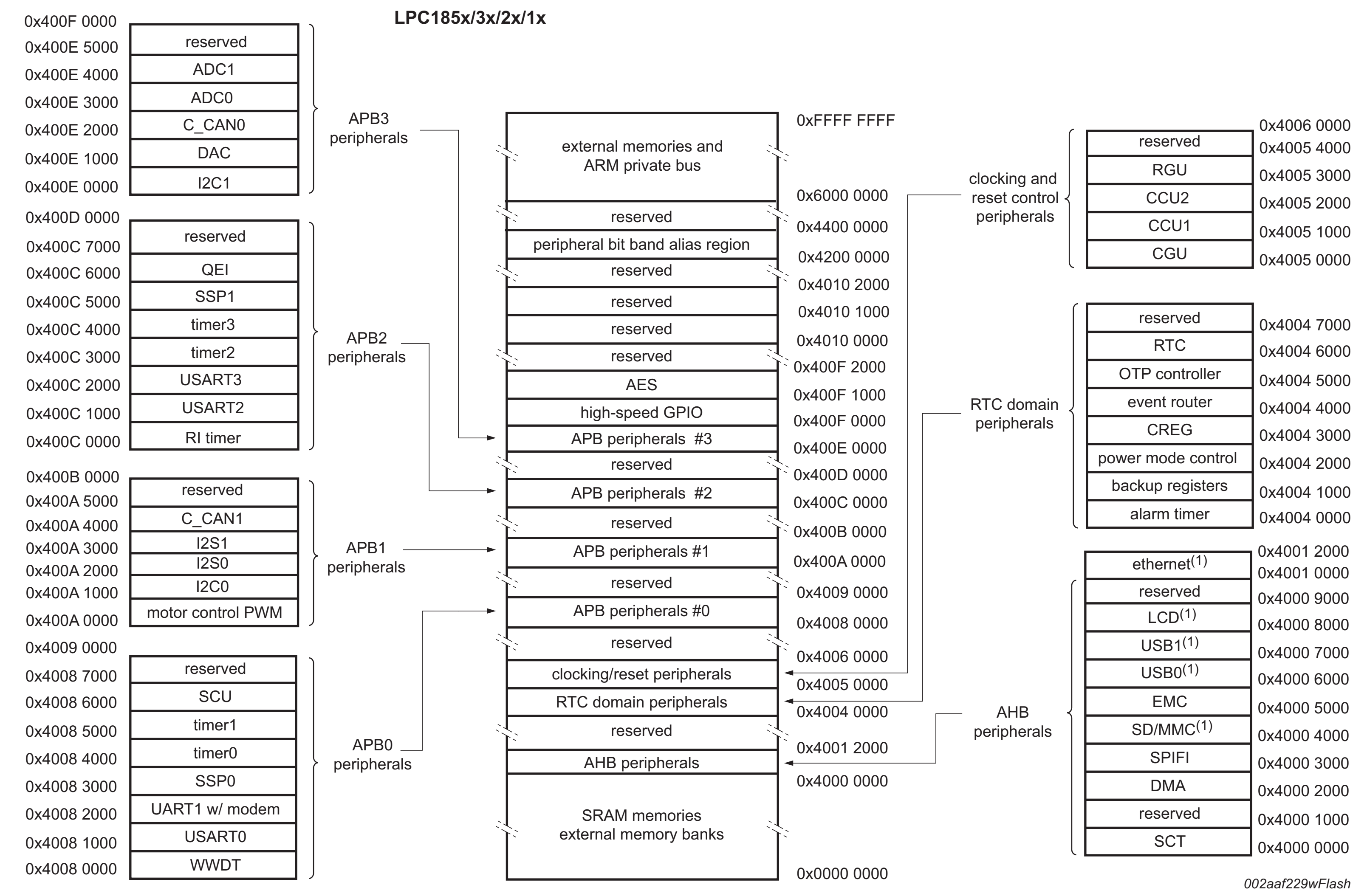


(1) Not available on all parts (see Table 4).

Fig 7. System memory map - parts with on-chip flash (overview)

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(1) Not available on all parts (see Table 4).

Fig 8. Memory mapping - parts with on-chip flash (peripherals)

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3.1 How to read this chapter

This chapter applies to flashless parts LPC1850/30/20/10 only.

3.2 Features

The boot ROM memory includes the following features:

- ROM memory size is 64 kB.
- Supports booting from UART interfaces and external static memory such as NOR flash, SPI flash, quad SPI flash.
- Includes APIs for power control and OTP programming.
- Includes SPIFI and USB drivers.
- ISP mode for loading data to on-chip SRAM and execute code from on-chip SRAM.

AES capable parts also support:

- CMAC authentication on the boot image.
- Secure booting from an encrypted image.
- Supports development mode for booting from a plain text image. Development mode is terminated by programming the AES key.
- API for AES programming.

3.3 Functional description

The internal ROM memory is used to store the boot code. After a reset, the ARM processor will start its code execution from this memory.

The ARM core is configured to start executing code, upon reset, with the program counter being set to the value 0x0000 0000. The LPC18xx contains a shadow pointer that allows areas of memory to be mapped to address 0x0000 0000. The default value of the shadow pointer is 0x1040 0000, ensuring that the code contained in the boot ROM is executed at reset.

Several boot modes are available depending on the values of the OTP bits BOOT_SRC. If the OTP memory is not programmed or the BOOT_SRC bits are all zero, the boot mode is determined by the states of the boot pins p2_8, P2_8, P1_2, and P1_1.

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Table 7. Boot mode when OTP BOOT_SRC bits are programmed

Boot mode	BOOT_SRC bit 3	BOOT_SRC bit 2	BOOT_SRC bit 1	BOOT_SRC bit 0	Description
Boot pins	0	0	0	0	Boot source is defined by the reset state of P1_1, P1_2, and P2_8 pins. See Table 8.
UART	0	0	0	1	Boot from device connected to USART0 using pins P2_0 and P2_1.
SPIFI	0	0	1	0	Boot from Quad SPI flash connected to the SPIFI interface using pins P3_3 to P3_8.
EMC 8-bit	0	0	1	1	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	0	1	0	0	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	0	1	0	1	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	0	1	1	0	Boot from USB0.
USB1	0	1	1	1	Boot from USB1.
SPI (SSP)	1	0	0	0	Boot from SPI flash connected to the SSP0 interface on P3_3, P3_6, P3_7 and P3_8[1].
USART3	1	0	0	1	Boot from device connected to USART3 using pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.

Table 8. Boot mode when OPT BOOT_SRC bits are zero

Boot mode	P2_9	P2_8	P1_2	P1_1	Description
USART0	LOW	LOW	LOW	LOW	Boot from device connected to USART0 using pins P2_0 and P2_1.
SPIFI	LOW	LOW	LOW	HIGH	Boot from Quad SPI flash connected to the SPIFI interface on P3_3 to P3_8[1].
EMC 8-bit	LOW	LOW	HIGH	LOW	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	LOW	LOW	HIGH	HIGH	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	LOW	HIGH	LOW	LOW	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	LOW	HIGH	LOW	HIGH	Boot from USB0.
USB1	LOW	HIGH	HIGH	LOW	Boot from USB1.
SPI (SSP)	LOW	HIGH	HIGH	HIGH	Boot from SPI flash connected to the SSP0 interface on P3_3, P3_6, P3_7 and P3_8[1].
USART3	HIGH	LOW	LOW	LOW	Boot from device connected to USART3 using pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.

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3.3.1 AES capable devices

AES capable products will normally always boot from a secure (encrypted) image and use CMAC authentication. However a special development mode allows booting from a plain text image. This development mode is active when the AES key has not been programmed. In this case the AES key consists of all zeros. Once the key is programmed (to a non-zero value), the development mode is terminated.

3.3.2 Boot process

The top level boot process is illustrated in Figure 9. The boot starts after Reset is released. The IRC is selected as CPU clock and the Cortex-M3 starts by executing boot ROM. By default the JTAG access to the chip is disabled at reset. When the part is non-AES capable or it is AES capable but the AES key has not been programmed then JTAG access is enabled.

As shown in Figure 9, the boot ROM determines the boot mode based on the OTP BOOT_SRC value or reset state of the pins P1_1, P1_2, P2_8, and P2_9. The boot ROM copies the image to internal SRAM at location 0x1000 0000 and jumps to that location (sets ARM's shadow pointer to 0x1000 0000) after image verification. Hence the images for LPC18xx should be compiled with entry point at 0x0000 0000. On AES capable LPC18xx with a programmed AES key the image and header are authenticated using the CMAC algorithm. If authentication fails the device is reset.

On AES capable LPC18xx in development mode and non-AES capable LPC18xx, the image and header are not authenticated. If the image is not preceded by a header then the image is not copied to SRAM but assumed to be executable as-is. In that case the shadow pointer is set to the first address location of the external boot memory. The header-less images for LPC18xx should be compiled with entry point at 0x0000 0000, the same as for an image with header.

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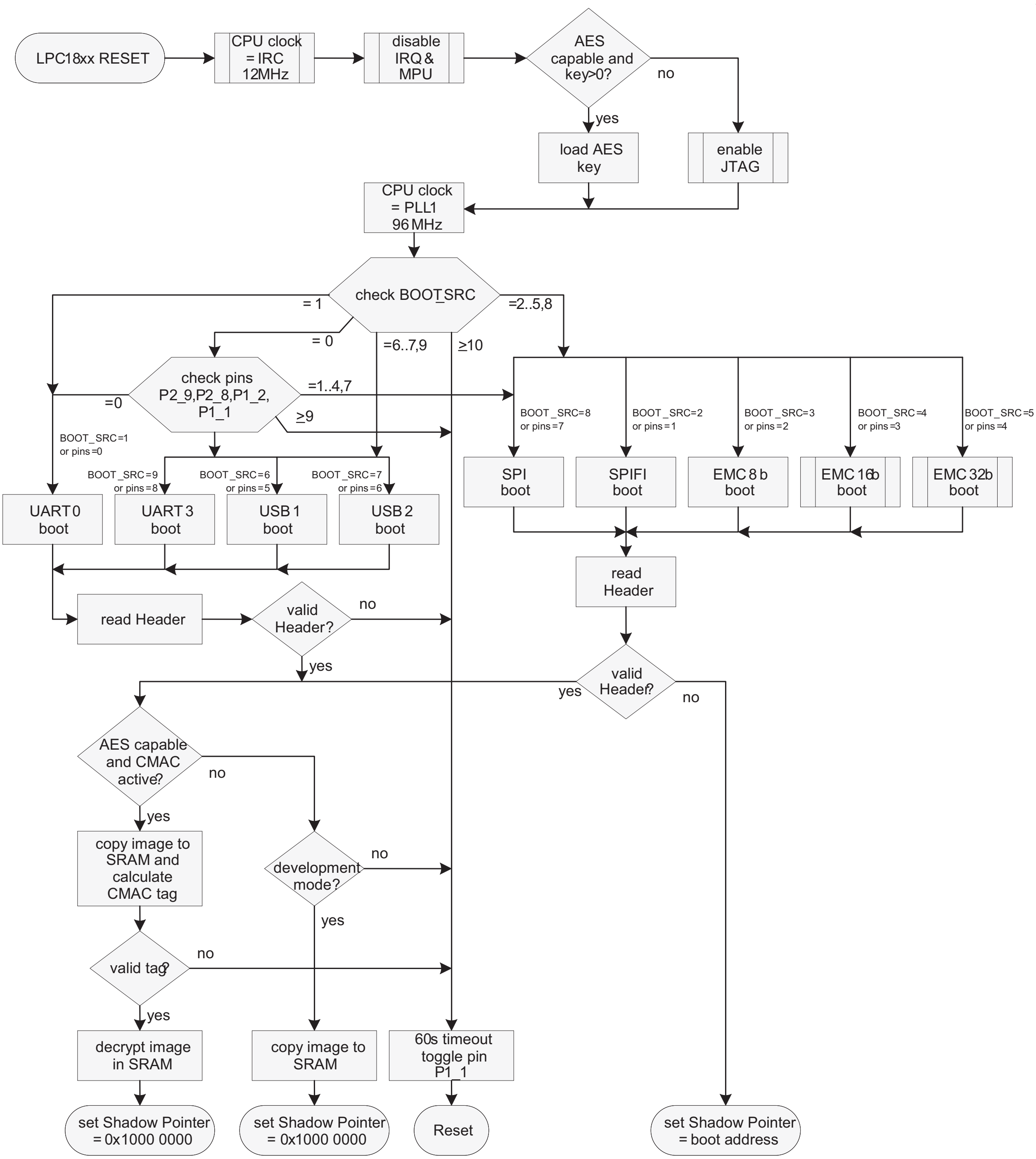


Fig 9. Boot process

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3.3.3 Boot image format

AES capable products with a programmed AES key will always boot from a secure image and use CMAC authentication. A secure image should always include a header.

Non-AES capable products may boot from an image with header or execute directly from the boot source (when the boot source is memory mapped; SPIFI or EMC). When no valid header is found then the CPU will try to execute code from the first location of the memory mapped boot source. The user should take care that this location contains executable code, otherwise a hard fault exception will occur. This exception jumps to a while(1) loop.

The image must be preceded by a header that has the layout described in Table 9. Non-encrypted images may omit the header.

Table 9. Image header

Address	Name	Description	size [bits]
5:0	AES_ACTIVE[1]	AES encryption active 0x25 (100101): AES encryption active 0x1A (011010): AES encryption not active else: invalid image	6
7:6	HASH_ACTIVE[1]	Indicates whether a hash is used: 00: CMAC hash is used, value is HASH_VALUE 01: reserved 10: reserved 11: no hash is used	2
13:8	reserved	11...11 (binary)	6
15:14	AES_CONTROL	These 2 bits can be set to a value such that when AES encryption is active, that the AES_ACTIVE field, after AES encryption, is not equal to the value 0x1A (AES encryption not active)	2
31:16	HASH_SIZE[3]	Size of the part of the image over which the hash value is calculated in number of 512 Byte frames. Also size of image copied to internal SRAM at boot time. Hash size = 16[2] + HASH_SIZE x 512 Byte.	16
95:32	HASH_VALUE	CMAC hash value calculated over the first bytes of the image (starting right from the header) as indicated by HASH_SIZE. The value is truncated to the 64 MSB.	64
127:96	reserved	11...11 (binary)	32

[1] Can only be active if device is AES capable, else is considered an invalid image.

[2] 16 extra bytes are required for the header bytes.

[3] The image size should be set to no more than the size of the SRAM located at 0x1000 0000.

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3.3.4 Boot image creation

3.3.4.1 CMAC

The CMAC algorithm is used to calculate a tag which is used for image authentication. The tag is stored in the header field HASH_VALUE.

The authentication process is as follows:

1. Use the CMAC algorithm to generate the 128-bit tag. Truncate the tag to 64 MSB and insert this truncated tag in the header.
2. At boot time the tag is recalculated. Authentication passes when the calculated tag is equal to the received tag in the image header.

To generate an l-bit CMAC tag T of message M using a 128-bit block cipher AES and secret key K, the CMAC tag generation process is as follows:

1. Generate sub key K_1:
   – Calculate a temporary value $K_0 = AES_K(0)$.
   – If $msb(K_0) = 0$ then $K_1 = (K_0 << 1)$ else $K_1 = (K_0 << 1) \oplus 0x87$
2. Divide message into 128-bit blocks $M = M_1 || ... || M_{n-1} || M_n^*$, where $M_1 ...M_{n-1}$ are complete blocks.
3. The last block, M_n^*, should be padded to be a complete block and then $M_n = K_1 \oplus M_n^*$.
4. Let $c_0 = 00...0$.
5. For i = 1, ..., n, calculate $c_i = AES_K(c_{i-1} \oplus M_i)$.
6. Output $T = msb_l(c_n)$.

The first message block is the header. Since the CMAC tag is stored in the header field HASH_VALUE, and this tag is not yet known until after CMAC calculation, a temporary header with a dummy tag value of 0x3456789A is used during CMAC calculation. This dummy value should be replaced by the calculated tag value in the final header field HASH_VALUE.

For LPC18xx the chosen CMAC parameters are: encryption key K = User Key (same as used for decryption) and tag length l = 64. Data is processed in little endian mode. This means that the first byte read from the image is integrated into the AES codeword as least significant byte. The 16th byte read from the image is the most significant byte of the first AES codeword.

CMAC is calculated over the header and encrypted image.

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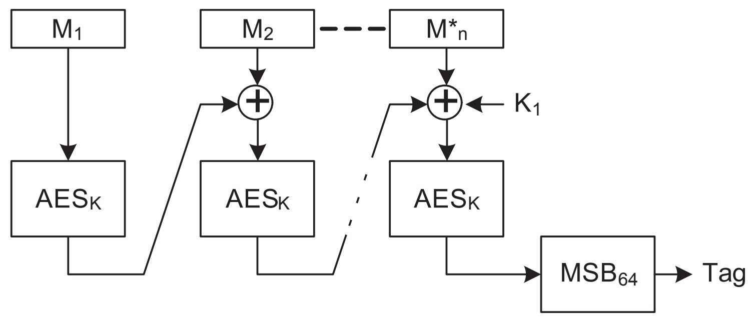


Fig 10. CMAC generation

3.3.4.2 UART boot mode

Figure 11 details the boot-flow steps of the UART boot mode. The execution of this mode happens only if the boot mode is set accordingly (see boot modes Table 7 and Table 8).

As illustrated in Figure 11, configure the UART with the following settings:

- Baudrate = 115200 (UART divisor registers are programmed assuming a 12 MHz clock frequency).
- Data bits = 8.
- Parity = None.
- Stop bits = 1.

Auto baud is active; boot waits until 0x3F is received and responds with “OK”. This should be followed by the header and image. The boot ROM doesn't implement any flow control or any handshake mechanisms during file transfer.

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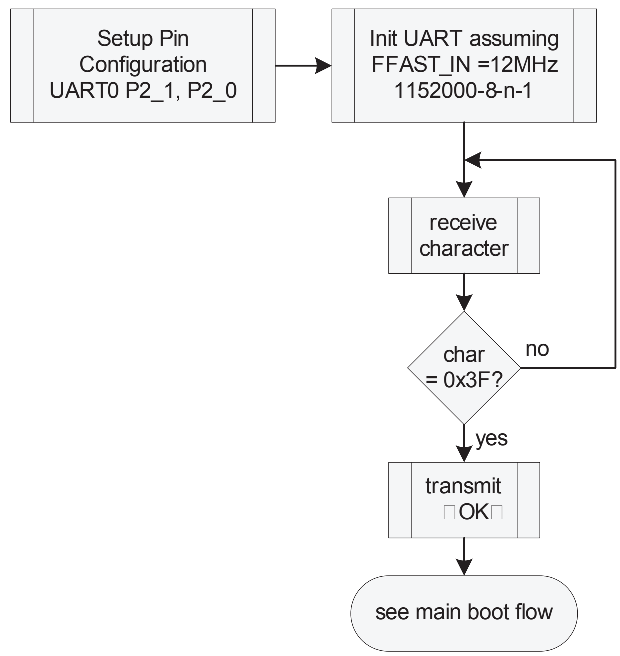


Fig 11. UART boot process

3.3.4.3 SPIFI boot mode

Figure 12 details the boot-flow steps of the Quad SPI flash boot mode. The execution of this mode happens only if the boot mode is set accordingly (see boot modes Table 7 and Table 8). The SPIFI clock is 36 MHz.

Boot ROM to support a SPI flash boot, the device should support “High frequency continuous array read” (command 0x0B). Since the boot ROM doesn't rely on a response for commands 0xAB, 0xB9 and 0x9F, as long as the SPI device ignores or responds correctly to these commands, the LPC18xx will be able to boot from them.

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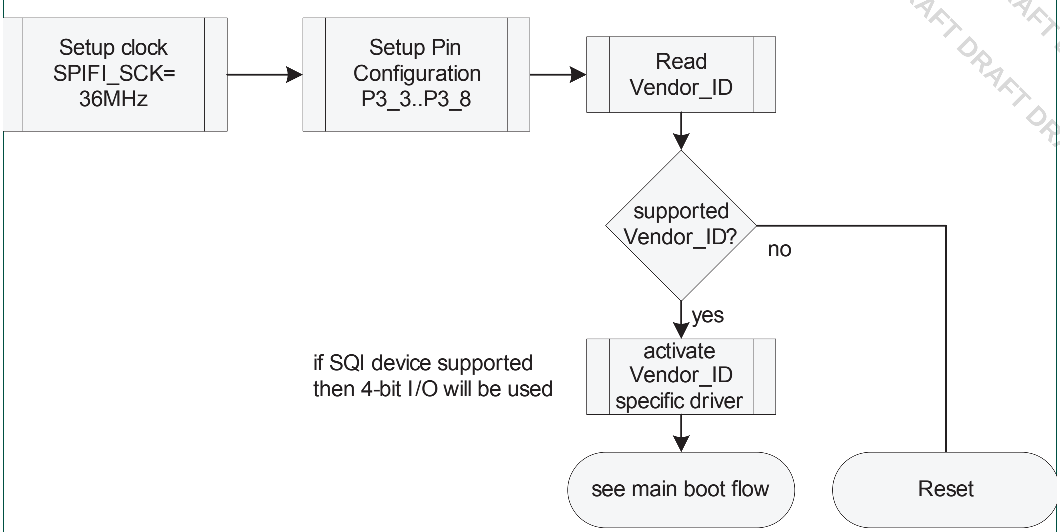


Fig 12. SPIFI boot process

3.3.4.4 EMC boot modes

The EMC boot process follows the main flow shown in Figure 13. Tthe CPU clock is set to 72 MHz, and a non-AES capable LPC18xx will boot directly from EMC when the image does not contain a header. The EMC uses 8 wait states.

Note that the number of address bits selected in pin configuration is initially EXTBUS_A[13:0]. After reading the header the address bits are extended to be in line with the image size as defined by HASH_SIZE, e.g. if HASH_SIZE is 100 kB then pins EXTBUS_A[16:14] are configured since 2^{17} > 100 kB. When booting without header then the image should configure extra address pins beyond the initially configured EXTBUS_A[13:0].

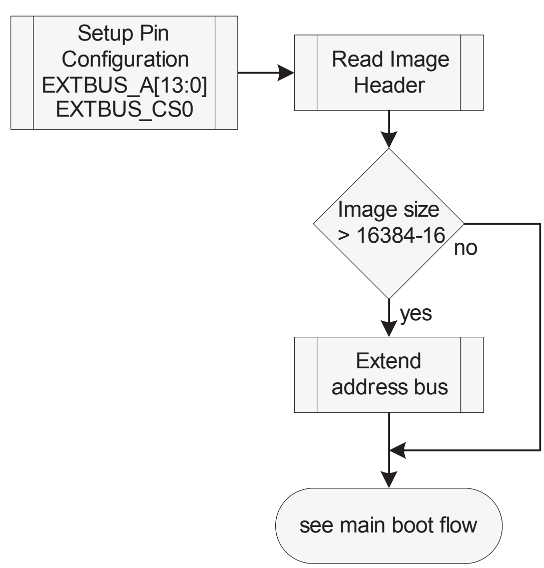


Fig 13. EMC boot process

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3.3.4.5 SPI boot mode

The boot uses SSP0 in SPI mode. The SPI clock is 18 MHz.

Figure 14 details the boot-flow steps of the SPI flash boot mode. The execution of this mode happens only if the boot mode is set accordingly (see boot modes Table 7 and Table 8).

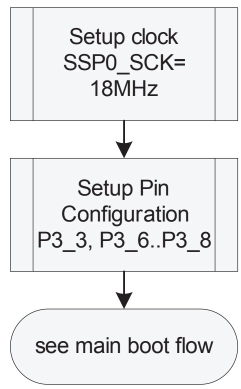


Fig 14. SPI boot process

3.3.5 Boot process timimg

The following paramters describe the timing of the boot process:

Table 10. Boot process timing parameters

Parameter	Description	Value
t_a	Check boot selection pins	< 1 µs
t_b	Initialize device	250 µs
t_c	Copy image to embedded SRAM If part is executing from external flash with no copy	< 0.3 µs
	If the image is encrypted or must be copied	< 1 µs to 10000 µs depending on the size of the image and the speed of the boot memory

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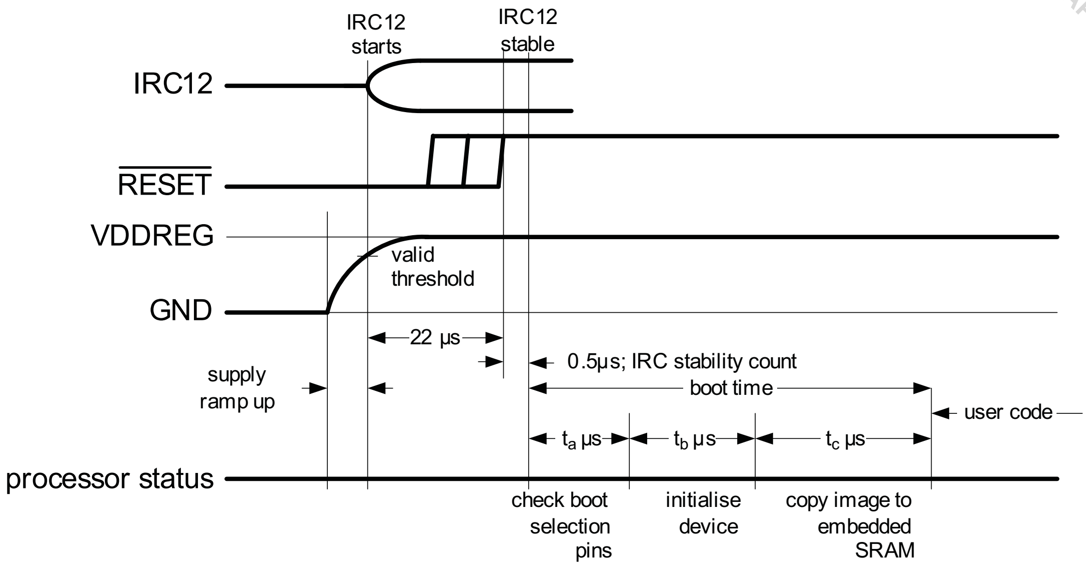


Fig 15. Boot process timing

3.3.6 ISP

In-System programming (ISP) is programming or re-programming the on-chip SRAM memory, using the boot loader software and the USART0 serial port. This can be done when the part resides in the end-user board. ISP allows to load data into on-chip SRAM and execute code from on-chip SRAM. For details, see Chapter 40.

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4.1 How to read this chapter

All LPC18xx parts support AES decoding.

4.2 Features

- Decoding of external image data.
- Secure storage of decoding keys.
- Support for CMAC hash calculation to authenticate data.
- AES engine performance of 1 byte/clock cycle.
- AES engine supports:
  - ECB decode mode with 128-bit key.
  - CBC decode mode with 128-bit key.
  - CMAC hash calculation.

4.3 General description

The LPC18xx uses an external image to store instruction code and data. If customers want to protect the external image content, then the LPC18xx offers hardware to accelerate processing for data decoding, data integrity and proof of origin.

The hardware consists of:

- One-time programmable (OTP) non-volatile memories to store the AES key. Two instances (OTP1/2) are offered to store two keys. A 3rd OTP (OTP3) is used by the LPC18xx for storing other data.
- An AES engine to perform the AES decoding. This engine supports an external GPDMA module to read and write data. The engine uses a 128-bit key and processes blocks of 128-bit. The key can use a dedicated hardware interface that is not visible to software or a software interface.

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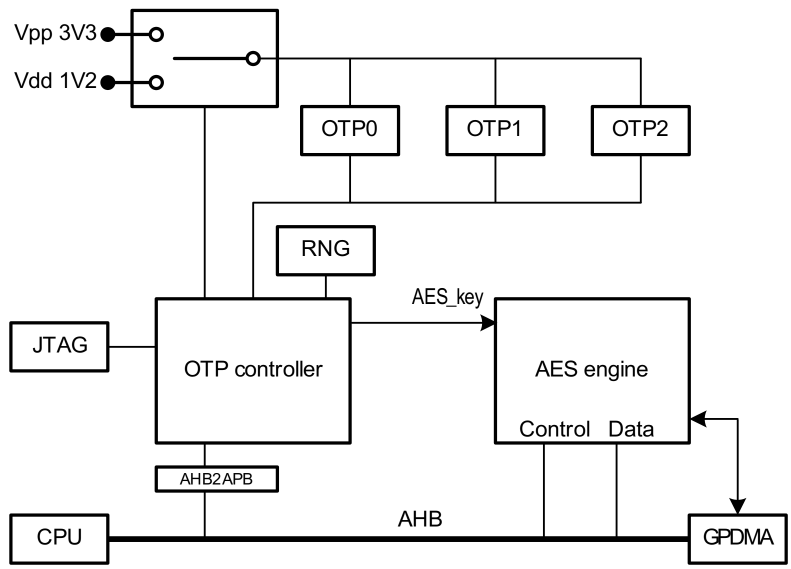


Fig 16. AES engine

4.4 AES API calls

4.4.1 Security API

The security API controls the AES block.

Table 11. Security API calls

Function	Offset relative to the API entry point	Description
AES_API_Set_Mode	0x00	Defines AES engine operation mode Parameter: unsigned cmd with values: 0 - Reserved. Do not use. 1 - AES_API_CMD_DECODE_ECB 2 - Reserved. Do not use. 3 - AES_API_CMD_DECODE_CBC Return - unsigned: see general error codes.
AES_API_Load_Key_1	0x04	Loads 128 bit AES user key 1 Parameter - void Return - void
AES_API_Load_Key_2	0x08	Loads 128 bit AES user key 2 Parameter - void Return - void
AES_API_Load_Key_RNG	0x0C	Loads randomly generated key in AES engine. Parameter - void Return - void

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Table 11. Security API calls

Function	Offset relative to the API entry point	Description
AES_API_Load_Key_SW	0x10	Loads 128 bit AES software defined user key Parameter - unsigned char *key(16 bytes) Return - void
AES_API_Load_IV_SW	0x14	Loads 128 bit AES init vector Parameter - unsigned char *iv(16 bytes) Return - void
AES_API_Load_IV_IC	0x18	Loads 128 bit AES IC specific init vector, which is used to decode a boot image. Parameter - void Return - void
AES_API_Operate	0x1C	Performs an operation pre-selected by the selected mode and therefore a key. A previously loaded iv is used. Data_out=AES_OP(data_in*size, key, [iv]) Parameter 1 - unsigned char *data_out Parameter 2 - unsigned char *data_in Parameter 3 - unsigned size (128 bits word - 16 bytes) Return - unsigned: see general error codes.
AES_API_Program_Key_1	0x20	Programs 128 bit AES key in OTP. Parameter: unsigned char *key (16 bytes) Return - unsigned: see general error codes.
AES_API_Program_Key_2	0x24	Programs 128 bit AES key in OTP. Parameter: unsigned char *key (16 bytes) Return - unsigned: see general error codes.

4.4.2 OTP memory

The virgin OTP state is all zeros. This implies that a zero value can be overwritten by a one value, but a one value cannot be changed.

Programming the OTP requires a higher voltage than reading. The read voltage is generated internally. The programming voltage is supplied via pin VPP. If this pin is not connected, then the OTP can not be programmed.

The OTP controller automatically selects the correct voltage.

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Chapter 5: LPC18xx NVIC

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5.1 How to read this chapter

Remark: This chapter describes the NVIC connections of parts LPC1850/30/20/10 Rev ‘A’.

The available NVIC interrupt sources vary for different parts.

- Ethernet interrupt: available on LPC1850/30.
- USB0 interrupt: available on LPC1850/30/20.
- USB1 interrupt: available on LPC1850/30.

5.2 Basic configuration

The NVIC is part of the ARM Cortex-M3 core.

5.3 Features

- Nested Vectored Interrupt Controller that is an integral part of the ARM Cortex-M3
- Tightly coupled interrupt controller provides low interrupt latency
- Controls system exceptions and peripheral interrupts
- On the LPC18xx, the NVIC supports 32 vectored interrupts
- 32 programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table
- Non-Maskable Interrupt
- Software interrupt generation

5.4 General description

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

Refer to the Cortex-M3 User Guide for details of NVIC operation.

5.5 Pin description

Table 12. NVIC pin description

Function	Direction	Description
NMI	I	External Non-Maskable Interrupt (NMI) input

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5.6 Interrupt sources

Table 13 lists the interrupt sources for each peripheral function. Each peripheral device may have one or more interrupt lines to the Vectored Interrupt Controller. Each line may represent more than one interrupt source, as noted.

Exception numbers relate to where entries are stored in the exception vector table. Interrupt numbers are used in some other contexts, such as software interrupts.

In addition, the NVIC handles the Non-Maskable Interrupt (NMI). In order for NMI to operate from an external signal, the NMI function must be connected to the related device pin (P4_0 or PE_4). When connected, a logic one on the pin will cause the NMI to be processed. For details, refer to the Cortex-M3 User Guide.

Table 13. Connection of interrupt sources to the NVIC

Interrupt ID	Exception Number	Vector Offset	Function	Flag(s)
0	16	0x40	DAC	
1	17	0x44	-	Reserved
2	18	0x48	DMA	
3	19	0x4C	-	Reserved
4	20	0x50	-	Reserved
5	21	0x54	Ethernet	Ethernet interrupt sbd_intr_o
6	22	0x58	SD/MMC	
7	23	0x5C	LCD	
8	24	0x60	USB0	OTG interrupt
9	25	0x64	USB1	OTG interrupt
10	26	0x68	SCT	SCT combined interrupt
11	27	0x6C	RI timer	
12	28	0x70	Timer0	
13	29	0x74	Timer1	
14	30	0x78	Timer2	
15	31	0x7C	Timer3	
16	32	0x80	Motor control PWM	
17	33	0x84	ADC0	
18	34	0x88	I2C0	
19	35	0x8C	I2C1	
20	36	0x90	-	Reserved
21	37	0x94	ADC1	
22	38	0x98	SSP0	
23	39	0x9C	SSP1	
24	40	0xA0	USART0	
25	41	0xA4	UART1	UART and modem interrupt
26	42	0xA8	USART2	
27	43	0xAC	USART3	USART and IrDA interrupt
28	44	0xB0	I2S0	

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Table 13. Connection of interrupt sources to the NVIC

Interrupt ID	Exception Number	Vector Offset	Function	Flag(s)
29	45	0xB4	I2S1	
30	46	0xB8	SPIFI	
31	47	0xBC	-	Reserved
32	48	0xC0	GPIO pin interrupt 0	
33	49	0xC4	GPIO pin interrupt 1	
34	50	0xC8	GPIO pin interrupt 2	
35	51	0xCC	GPIO pin interrupt 3	
36	52	0xD0	GPIO pin interrupt 4	
37	53	0xC4	GPIO pin interrupt 5	
38	54	0xC8	GPIO pin interrupt 6	
39	55	0xCC	GPIO pin interrupt 7	
40	56	0xD0	GPIO group interrupt 0	
41	57	0xD4	GPIO group interrupt 1	
42	58	0xD8	Event router	Combined interrupt from the event router sources
43	59	0xDC	C_CAN1 interrupt	
44	60	0xE0	Reserved	
45	61	0xE4	Reserved	
46	62	0xE8	ATIMER	
47	63	0xEC	Reserved	
48	64	0xF0	Reserved	
49	65	0xF4	WWDT	
50	66	0xF8	Reserved	
51	67	0xFC	C_CAN0	
52	68	0x100	QEI	

5.7 Register description

The following table summarizes the registers in the NVIC as implemented in the LPC18xx. The Cortex-M3 User Guide provides a functional description of the NVIC.

Table 14. Register overview: NVIC (base address 0xE000 E000)

Name	Access	Address offset	Description	Reset value
ISER0	RW	0x100	Interrupt Set-Enable Register 0. This register allows enabling interrupts and reading back the interrupt enables for specific peripheral functions.	0
ISER1	RW	0x104	Interrupt Set-Enable Register 1. This register allows enabling interrupts and reading back the interrupt enables for specific peripheral functions.	0
ICER0	RW	0x180	Interrupt Clear-Enable Register 0. This register allows disabling interrupts and reading back the interrupt enables for specific peripheral functions.	0

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Table 14. Register overview: NVIC (base address 0xE000 E000) *…continued*

Name	Access	Address offset	Description	Reset value
ICER1	RW	0x184	Interrupt Clear-Enable Register 1. This register allows disabling interrupts and reading back the interrupt enables for specific peripheral functions.	0
ISPR0	RW	0x200	Interrupt Set-Pending Register 0. This register allows changing the interrupt state to pending and reading back the interrupt pending state for specific peripheral functions.	0
ISPR1	RW	0x204	Interrupt Set-Pending Register 1. This register allows changing the interrupt state to pending and reading back the interrupt pending state for specific peripheral functions.	0
ICPR0	RW	0x280	Interrupt Clear-Pending Register 0. This register allows changing the interrupt state to not pending and reading back the interrupt pending state for specific peripheral functions.	0
ICPR1	RW	0x284	Interrupt Clear-Pending Register 0. This register allows changing the interrupt state to not pending and reading back the interrupt pending state for specific peripheral functions.	0
IABR0	RO	0x300	Interrupt Active Bit Register 0. This register allows reading the current interrupt active state for specific peripheral functions.	0
IABR1	RO	0x304	Interrupt Active Bit Register 1. This register allows reading the current interrupt active state for specific peripheral functions.	0
IPR0	RW	0x400	Interrupt Priority Registers 0. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR1	RW	0x404	Interrupt Priority Registers 1 This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR2	RW	0x408	Interrupt Priority Registers 2. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR3	RW	0x40C	Interrupt Priority Registers 3. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR4	RW	0x410	Interrupt Priority Registers 4. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR5	RW	0x414	Interrupt Priority Registers 5. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR6	RW	0x418	Interrupt Priority Registers 6. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR7	RW	0x41C	Interrupt Priority Registers 7. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
STIR	WO	0xF00	Software Trigger Interrupt Register. This register allows software to generate an interrupt.	0

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6.1 How to read this chapter

Remark: This chapter applies to parts LPC1850/30/30/10 Rev ‘A’ only.

Remark: The event router controls the wake-up process and various event inputs to the NVIC.

The available event router sources vary for different parts.

- Ethernet: available on LPC1850/30.
- USB0: available on LPC1850/30/20.
- USB1: available on LPC1850/30.

6.2 Basic configuration

- See Table 15 for clocking.
- An event created in the event router can be output on the RTC_ALARM pin (see Table 31).
- The event router is connected to interrupt #42 in the NVIC (see Table 13).

Table 15. Event router clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to event router	BASE_M3_CLK	CLK_M3_BUS	150 MHz

6.3 General description

The event router is used to process wake-up events such as certain interrupts and external or internal inputs for wake-up from any of the low power modes (Sleep, Deep-sleep, Power-down, and Deep power-down modes). The event router has multiple event inputs from various peripherals. When the proper edge detection is set in the EDGE configuration register, the event router can wake up the part or can raise an interrupt in the NVIC.

Each event input to the event router can be configured to trigger an output signal on rising or falling edges or on HIGH or LOW levels. The event router combines all events to an output signal which is used as follows:

- Create an interrupt if the event router interrupt is enabled in the NVIC.
- Send a wake-up signal to the power management unit to wake up from Deep-sleep, Power-down, and Deep power-down modes.
- Send a wake-up signal to CCU1 and CCU2 for waking up from Sleep mode (see Section 14.5.3).

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6.4 Event router inputs

Table 16. Event router inputs

Event #	Source	Notes
0	WAKEUP0	WAKEUP0 pin
1	WAKEUP1	WAKEUP1 pin
2	WAKEUP2	WAKEUP2 pin
3	WAKEUP3	WAKEUP3 pin
4	Alarm timer	Alarm timer interrupt
5	RTC	RTC interrupt
6	BOD trip level 1	BOD interrupt; wake-up from low power mode
7	WWDT	WWDT interrupt
8	Ethernet	Wake-up packet indicator
9	USB0	Wake-up request signal
10	USB1	ahb_needclk signal
11	SD/MMC	SD/MMC interrupt
12	C_CAN0/1	ORed C_CAN0 and C_CAN1 interrupt
13	GIMA output 25	Output 2 of the combined timer (ORed output of SCT output 2 and the match channel 2 of timer 0). See Table 134.
14	GIMA output 26	Output 6 of the combined timer (ORed output of SCT output 6 and the match channel 2 of timer 1). See Table 134.
15	QEI	QEI interrupt
16	GIMA output 27	Output 14 of the combined timer (ORed output of SCT output 14 and the match channel 2 of timer 3). See Table 134.
17	-	Reserved
18	-	Reserved
19	Reset	<tbd>
20	BOD trip level 2	<tbd>
25-21	-	Reserved

6.5 Pin description

Table 17. Event router pin description

Pin	Direction	Description
WAKEUP0/1/2/3	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.

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6.6 Register description

Table 18. Register overview: Event router (base address 0x4004 4000)

Name	Access	Address offset	Description	Reset Value
HILO	R/W	0x000	Level configuration register	0x000
EDGE	R/W	0x004	Edge configuration	0x000
-	-	0x008 - 0xFD4	Reserved	-
CLR_EN	W	0xFD8	Event clear enable register	0x0
SET_EN	W	0xFDC	Event set enable register	0x0
STATUS	R	0xFE0	Status register	0x0
ENABLE	R	0xFE4	Enable register	0x0
CLR_STAT	W	0xFE8	Clear register	0x0
SET_STAT	W	0xFEC	Set register	0x0

6.6.1 Level configuration register

This register works in combination with the edge configuration register EDGE (see Table 21) to configure the level and edge detection for each input to the event router.

Table 19. Level configuration register (HILO - address 0x4004 4000) bit description

Bit	Symbol	Value	Description	Reset value
0	WAKEUP0_L		Level detect mode for WAKEUP0 event.	0
		0	Detect LOW level if bit 0 in the EDGE register is 0. Detect falling edge if bit 0 in the EDGE register is 1.	
		1	Detect HIGH level if bit 0 in the EDGE register is 0. Detect rising edge if bit 0 in the EDGE register is 1.	
1	WAKEUP1_L		Level detect mode for WAKEUP1 event. The corresponding bit in the EDGE register must be 0.	0
		0	Detect LOW level if bit 1 in the EDGE register is 0.	
		1	Detect HIGH level if bit 1 in the EDGE register is 0. Detect rising edge if bit 1 in the EDGE register is 1.	
2	WAKEUP2_L		Level detect mode for WAKEUP2 event.	0
		0	Detect LOW level if bit 2 in the EDGE register is 0. Detect falling edge if bit 2 in the EDGE register is 1.	
		1	Detect HIGH level if bit 2 in the EDGE register is 0. Detect rising edge if bit 2 in the EDGE register is 1.	
3	WAKEUP3_L		Level detect mode for WAKEUP3 event.	0
		0	Detect LOW level if bit 3 in the EDGE register is 0. Detect falling edge if bit 3 in the EDGE register is 1.	
		1	Detect HIGH level if bit 3 in the EDGE register is 0. Detect rising edge if bit 3 in the EDGE register is 1.	

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Table 19. Level configuration register (HILO - address 0x4004 4000) bit description

Bit	Symbol	Value	Description	Reset value
4	ATIMER_L		Level detect mode for alarm timer event.	0
		0	Detect LOW level if bit 4 in the EDGE register is 0. Detect falling edge if bit 4 in the EDGE register is 1.	
		1	Detect HIGH level if bit 4 in the EDGE register is 0. Detect rising edge if bit 4 in the EDGE register is 1.	
5	RTC_L		Level detect mode for RTC event.	0
		0	Detect LOW level if bit 5 in the EDGE register is 0. Detect falling edge if bit 5 in the EDGE register is 1.	
		1	Detect HIGH level if bit 5 in the EDGE register is 0. Detect rising edge if bit 5 in the EDGE register is 1.	
6	BOD_L		Level detect mode for BOD event.	0
		0	Detect LOW level if bit 6 in the EDGE register is 0. Detect falling edge if bit 6 in the EDGE register is 1.	
		1	Detect HIGH level if bit 6 in the EDGE register is 0. Detect rising edge if bit 6 in the EDGE register is 1.	
7	WWDT_L		Level detect mode for WWDTD event.	0
		0	Detect LOW level if bit 7 in the EDGE register is 0. Detect falling edge if bit 7 in the EDGE register is 1.	
		1	Detect HIGH level if bit 7 in the EDGE register is 0. Detect rising edge if bit 7 in the EDGE register is 1.	
8	ETH_L			0
		0	Detect LOW level if bit 8 in the EDGE register is 0. Detect falling edge if bit 8 in the EDGE register is 1.	
		1	Detect HIGH level if bit 8 in the EDGE register is 0. Detect rising edge if bit 8 in the EDGE register is 1.	
9	USB0_L			0
		0	Detect LOW level if bit 9 in the EDGE register is 0. Detect falling edge if bit 9 in the EDGE register is 1.	
		1	Detect HIGH level if bit 9 in the EDGE register is 0. Detect rising edge if bit 9 in the EDGE register is 1.	
10	USB1_L			0
		0	Detect LOW level if bit 10 in the EDGE register is 0. Detect falling edge if bit 10 in the EDGE register is 1.	
		1	Detect HIGH level if bit 10 in the EDGE register is 0. Detect rising edge if bit 10 in the EDGE register is 1.	
11	-	-	Reserved.	
12	CAN_L		Level detect mode for C_CAN event.	0
		0	Detect LOW level if bit 12 in the EDGE register is 0. Detect falling edge if bit 12 in the EDGE register is 1.	
		1	Detect HIGH level if bit 12 in the EDGE register is 0. Detect rising edge if bit 12 in the EDGE register is 1.	

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Table 19. Level configuration register (HILO - address 0x4004 4000) bit description

Bit	Symbol	Value	Description	Reset value
13	TIM2_L		Level detect mode for combined timer output 2 event.	0
		0	Detect LOW level if bit 13 in the EDGE register is 0. Detect falling edge if bit 13 in the EDGE register is 1.	
		1	Detect HIGH level if bit 13 in the EDGE register is 0. Detect rising edge if bit 13 in the EDGE register is 1.	
14	TIM6_L		Level detect mode for combined timer output 6 event.	0
		0	Detect LOW level if bit 14 in the EDGE register is 0. Detect falling edge if bit 14 in the EDGE register is 1.	
		1	Detect HIGH level if bit 14 in the EDGE register is 0. Detect rising edge if bit 14 in the EDGE register is 1.	
15	QEI_L		Level detect mode for QEI event.	0
		0	Detect LOW level if bit 15 in the EDGE register is 0. Detect falling edge if bit 15 in the EDGE register is 1.	
		1	Detect HIGH level if bit 15 in the EDGE register is 0. Detect rising edge if bit 15 in the EDGE register is 1.	
16	TIM14_L		Level detect mode for combined timer output 14 event.	0
		0	Detect LOW level if bit 16 in the EDGE register is 0. Detect falling edge if bit 16 in the EDGE register is 1.	
		1	Detect HIGH level if bit 16 in the EDGE register is 0. Detect rising edge if bit 16 in the EDGE register is 1.	
18:17	-	-	Reserved.	
19	RESET_L		.	0
		0	Detect LOW level if bit 17 in the EDGE register is 0. Detect falling edge if bit 17 in the EDGE register is 1.	
		1	Detect HIGH level if bit 17 in the EDGE register is 0. Detect rising edge if bit 17 in the EDGE register is 1.	
31:20	-	-	Reserved.	

6.6.2 Edge configuration register

This register works in combination with the level configuration register HILO (see Table 19) to configure the level or edge detection for each input to the event router.

The EDGE configuration register determines whether the event router responds to a level change (EDGEn=1), or a constant level (EDGEn=0). The HILOn bit determines a response to a rising edge (HILOn=1) or a falling edge (HILOn=0).

Table 20. EDGE and HILO combined register settings

HILOn	EDGEn	Description
0	0	Detect LOW level
0	1	Detect falling edge
1	0	Detect HIGH level
1	1	Detect rising edge

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When a HIGH level detect is active, the event router status bits cannot be cleared until the signal is LOW. When a rising edge detect is active, the event router status bit can be cleared right after the event has occurred.

Table 21. Edge configuration register (EDGE - address 0x4004 4004) bit description

Bit	Symbol	Value	Description	Reset value
0	WAKEUP0_E		Edge detect mode for WAKEUP0 event.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 0 in the HILO register is 0. Detect rising edge if bit 0 in the HILO register is 1.	
1	WAKEUP1_E		Edge/level detect mode for WAKEUP1 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 1 in the HILO register is 0. Detect rising edge if bit 1 in the HILO register is 1.	
2	WAKEUP2_E		Edge/level detect mode for WAKEUP2 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 2 in the HILO register is 0. Detect rising edge if bit 2 in the HILO register is 1.	
3	WAKEUP3_E		Edge/level detect mode for WAKEUP3 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 30 in the HILO register is 0. Detect rising edge if bit 3 in the HILO register is 1.	
4	ATIMER_E		Edge/level detect mode for alarm timer event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 4 in the HILO register is 0. Detect rising edge if bit 4 in the HILO register is 1.	
5	RTC_E		Edge/level detect mode for RTC event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 5 in the HILO register is 0. Detect rising edge if bit 5 in the HILO register is 1.	
6	BOD_E		Edge/level detect mode for BOD event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 6 in the HILO register is 0. Detect rising edge if bit 6 in the HILO register is 1.	

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Table 21. Edge configuration register (EDGE - address 0x4004 4004) bit description

Bit	Symbol	Value	Description	Reset value
7	WWDT_E		Edge/level detect mode for WWDTD event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 7 in the HILO register is 0. Detect rising edge if bit 7 in the HILO register is 1.	
8	ETH_E		The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 8 in the HILO register is 0. Detect rising edge if bit 8 in the HILO register is 1.	
9	USB0_E		The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 9 in the HILO register is 0. Detect rising edge if bit 9 in the HILO register is 1.	
10	USB1_E		The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 10 in the HILO register is 0. Detect rising edge if bit 10 in the HILO register is 1.	
11	-	-	Reserved.	
12	CAN_E		Edge/level detect mode for C_CAN event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 12 in the HILO register is 0. Detect rising edge if bit 12 in the HILO register is 1.	
13	TIM2_E		Edge/level detect mode for combined timer output 2 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 13 in the HILO register is 0. Detect rising edge if bit 13 in the HILO register is 1.	
14	TIM6_E		Edge/level detect mode for combined timer output 6 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 14 in the HILO register is 0. Detect rising edge if bit 14 in the HILO register is 1.	

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Table 21. Edge configuration register (EDGE - address 0x4004 4004) bit description

Bit	Symbol	Value	Description	Reset value
15	QEI_E		Edge/level detect mode for QEI interrupt signal. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 15 in the HILO register is 0. Detect rising edge if bit 15 in the HILO register is 1.	
16	TIM14_E		Edge/level detect mode for combined timer output 14 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 16 in the HILO register is 0. Detect rising edge if bit 16 in the HILO register is 1.	
18:17	-	-	Reserved.	
19	RESET_E		. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 19 in the HILO register is 0. Detect rising edge if bit 19 in the HILO register is 1.	
31:20	-	-	Reserved.	

6.6.3 Interrupt clear enable register

Table 22. Interrupt clear enable register (CLR_EN - address 0x4004 4FD8) bit description

Bit	Symbol	Description	Reset value
0	WAKEUP0_CLREN	Writing a 1 to this bit clears the event enable bit 0 in the ENABLE register.	-
1	WAKEUP1_CLREN	Writing a 1 to this bit clears the event enable bit 1 in the ENABLE register.	-
2	WAKEUP2_CLREN	Writing a 1 to this bit clears the event enable bit 2 in the ENABLE register.	-
3	WAKEUP3_CLREN	Writing a 1 to this bit clears the event enable bit 3 in the ENABLE register.	-
4	ATIMER_CLREN	Writing a 1 to this bit clears the event enable bit 4 in the ENABLE register.	-
5	RTC_CLREN	Writing a 1 to this bit clears the event enable bit 5 in the ENABLE register.	-
6	BOD_CLREN	Writing a 1 to this bit clears the event enable bit 6 in the ENABLE register.	-
7	WWDT_CLREN	Writing a 1 to this bit clears the event enable bit 7 in the ENABLE register.	-
8	ETH_CLREN	Writing a 1 to this bit clears the event enable bit 8 in the ENABLE register.	-
9	USB0_CLREN	Writing a 1 to this bit clears the event enable bit 9 in the ENABLE register.	-

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Table 22. Interrupt clear enable register (CLR_EN - address 0x4004 4FD8) bit description

Bit	Symbol	Description	Reset value
10	USB1_CLREN	Writing a 1 to this bit clears the event enable bit 10 in the ENABLE register.	-
11	-	Reserved.	-
12	CAN_CLREN	Writing a 1 to this bit clears the event enable bit 12 in the ENABLE register.	-
13	TIM2_CLREN	Writing a 1 to this bit clears the event enable bit 13 in the ENABLE register.	-
14	TIM6_CLREN	Writing a 1 to this bit clears the event enable bit 14 in the ENABLE register.	-
15	QEI_CLREN	Writing a 1 to this bit clears the event enable bit 15 in the ENABLE register.	-
16	TIM14_CLREN	Writing a 1 to this bit clears the event enable bit 16 in the ENABLE register.	-
18:17	-	Reserved.	-
19	RESET_CLREN	Writing a 1 to this bit clears the event enable bit 19 in the ENABLE register.	-
31:20	-	Reserved.	-

6.6.4 Event set enable register

Table 23. Event set enable register (SET_EN - address 0x4004 4FDC) bit description

Bit	Symbol	Description	Reset value
0	WAKEUP0_SETEN	Writing a 1 to this bit sets the event enable bit 0 in the ENABLE register.	-
1	WAKEUP1_SETEN	Writing a 1 to this bit sets the event enable bit 1 in the ENABLE register.	-
2	WAKEUP2_SETEN	Writing a 1 to this bit sets the event enable bit 2 in the ENABLE register.	-
3	WAKEUP3_SETEN	Writing a 1 to this bit sets the event enable bit 3 in the ENABLE register.	-
4	ATIMER_SETEN	Writing a 1 to this bit sets the event enable bit 4 in the ENABLE register.	-
5	RTC_SETEN	Writing a 1 to this bit sets the event enable bit 5 in the ENABLE register.	-
6	BOD_SETEN	Writing a 1 to this bit sets the event enable bit 6 in the ENABLE register.	-
7	WWDT_SETEN	Writing a 1 to this bit sets the event enable bit 7 in the ENABLE register.	-
8	ETH_SETEN	Writing a 1 to this bit sets the event enable bit 8 in the ENABLE register.	-
9	USB0_SETEN	Writing a 1 to this bit sets the event enable bit 9 in the ENABLE register.	-
10	USB1_SETEN	Writing a 1 to this bit sets the event enable bit 10 in the ENABLE register.	-
11	-	Reserved.	-

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Table 23. Event set enable register (SET_EN - address 0x4004 4FDC) bit description

Bit	Symbol	Description	Reset value
12	CAN_SETEN	Writing a 1 to this bit sets the event enable bit 12 in the ENABLE register.	-
13	TIM2_SETEN	Writing a 1 to this bit sets the event enable bit 13 in the ENABLE register.	-
14	TIM6_SETEN	Writing a 1 to this bit sets the event enable bit 14 in the ENABLE register.	-
15	QEI_SETEN	Writing a 1 to this bit sets the event enable bit 15 in the ENABLE register.	-
16	TIM14_SETEN	Writing a 1 to this bit sets the event enable bit 16 in the ENABLE register.	-
18:17	-	Reserved.	-
19	RESET_SETEN	Writing a 1 to this bit sets the event enable bit 19 in the ENABLE register.	-
31:20	-	Reserved.	-

6.6.5 Event status register

Table 24. Interrupt status register (STATUS - address 0x4004 4FE0) bit description

Bit	Symbol	Description	Reset value
0	WAKEUP0_ST	A 1 in this bit shows that the WAKEUP0 event has been raised.	-
1	WAKEUP1_ST	A 1 in this bit shows that the WAKEUP1 event has been raised.	-
2	WAKEUP2_ST	A 1 in this bit shows that the WAKEUP2 event has been raised.	-
3	WAKEUP3_ST	A 1 in this bit shows that the WAKEUP3 event has been raised.	-
4	ATIMER_ST	A 1 in this bit shows that the ATIMER event has been raised.	-
5	RTC_ST	A 1 in this bit shows that the RTC event has been raised.	-
6	BOD_ST	A 1 in this bit shows that the BOD event has been raised.	-
7	WWDT_ST	A 1 in this bit shows that the WWDT event has been raised.	-
8	ETH_ST	A 1 in this bit shows that the ETHERNET event has been raised.	-
9	USB0_ST	A 1 in this bit shows that the USB0 event has been raised.	-
10	USB1_ST	A 1 in this bit shows that the USB1 event has been raised.	-
11	-	Reserved.	-
12	CAN_ST	A 1 in this bit shows that the C_CAN event has been raised.	-
13	TIM2_ST	A 1 in this bit shows that the combined timer 2 output event has been raised.	-
14	TIM6_ST	A 1 in this bit shows that the combined timer 6 output event has been raised.	-
15	QEI_ST	A 1 in this bit shows that the QEI event has been raised.	-
16	TIM14_ST	A 1 in this bit shows that the combined timer 14 output event has been raised.	-
18:17	-	Reserved.	-
19	RESET_ST	A 1 in this bit shows that the <tbd> event has been raised.	-
31:20	-	Reserved.	-

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6.6.6 Event enable register

Table 25. Event enable register (ENABLE - address 0x4004 4FE4) bit description

Bit	Symbol	Description	Reset value
0	WAKEUP0_EN	A 1 in this bit shows that the WAKEUP0 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
1	WAKEUP1_EN	A 1 in this bit shows that the WAKEUP1 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
2	WAKEUP2_EN	A 1 in this bit shows that the WAKEUP2 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
3	WAKEUP3_EN	A 1 in this bit shows that the WAKEUP3 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
4	ATIMER_EN	A 1 in this bit shows that the ATIMER event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
5	RTC_EN	A 1 in this bit shows that the RTC event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
6	BOD_EN	A 1 in this bit shows that the BOD event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
7	WWDT_EN	A 1 in this bit shows that the WWDT event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
8	ETH_EN	A 1 in this bit shows that the ETHERNET event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
9	USB0_EN	A 1 in this bit shows that the USB0 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
10	USB1_EN	A 1 in this bit shows that the USB1 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
11	-	Reserved.	-
12	CAN_EN	A 1 in this bit shows that the CAN event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
13	TIM2_EN	A 1 in this bit shows that the TIM2 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
14	TIM6_EN	A 1 in this bit shows that the TIM6 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
15	QEI_EN	A 1 in this bit shows that the QEI event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0

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Table 25. Event enable register (ENABLE - address 0x4004 4FE4) bit description

Bit	Symbol	Description	Reset value
16	TIM14_EN	A 1 in this bit shows that the TIM14 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
18:17	-		-
19	RESET_EN	A 1 in this bit shows that the RESET event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
31:20	-	Reserved.	-

6.6.7 Clear status register

Table 26. Interrupt clear status register (CLR_STAT - address 0x4004 4FE8) bit description

Bit	Symbol	Description	Reset value
0	WAKEUP0_CLRST	Writing a 1 to this bit clears the STATUS event bit 0 in the STATUS register.	
1	WAKEUP1_CLRST	Writing a 1 to this bit clears the STATUS event bit 1 in the STATUS register.	
2	WAKEUP2_CLRST	Writing a 1 to this bit clears the STATUS event bit 2 in the STATUS register.	
3	WAKEUP3_CLRST	Writing a 1 to this bit clears the STATUS event bit 3 in the STATUS register.	
4	ATIMER_CLRST	Writing a 1 to this bit clears the STATUS event bit 4 in the STATUS register.	
5	RTC_CLRST	Writing a 1 to this bit clears the STATUS event bit 5 in the STATUS register.	
6	BOD_CLRST	Writing a 1 to this bit clears the STATUS event bit 6 in the STATUS register.	
7	WWDT_CLRST	Writing a 1 to this bit clears the STATUS event bit 7 in the STATUS register.	
8	ETH_CLRST	Writing a 1 to this bit clears the STATUS event bit 8 in the STATUS register.	
9	USB0_CLRST	Writing a 1 to this bit clears the STATUS event bit 9 in the STATUS register.	
10	USB1_CLRST	Writing a 1 to this bit clears the STATUS event bit 10 in the STATUS register.	
11	-	Reserved.	
12	CAN_CLRST	Writing a 1 to this bit clears the STATUS event bit 12 in the STATUS register.	
13	TIM2_CLRST	Writing a 1 to this bit clears the STATUS event bit 13 in the STATUS register.	
14	TIM6_CLRST	Writing a 1 to this bit clears the STATUS event bit 14 in the STATUS register.	
15	QEI_CLRST	Writing a 1 to this bit clears the STATUS event bit 15 in the STATUS register.	

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Table 26. Interrupt clear status register (CLR_STAT - address 0x4004 4FE8) bit description

Bit	Symbol	Description	Reset value
16	TIM14_CLRST	Writing a 1 to this bit clears the STATUS event bit 16 in the STATUS register.	
18:17	-		
19	RESET_CLRST	Writing a 1 to this bit clears the STATUS event bit 19 in the STATUS register.	
31:20	-	Reserved.	-

6.6.8 Set status register

Table 27. Interrupt set status register (SET_STAT - address 0x4004 4FEC) bit description

Bit	Symbol	Description	Reset value
0	WAKEUP0_SETST	Writing a 1 to this bit sets the STATUS event bit 0 in the STATUS register.	
1	WAKEUP1_SETST	Writing a 1 to this bit sets the STATUS event bit 1 in the STATUS register.	
2	WAKEUP2_SETST	Writing a 1 to this bit sets the STATUS event bit 2 in the STATUS register.	
3	WAKEUP3_SETST	Writing a 1 to this bit sets the STATUS event bit 3 in the STATUS register.	
4	ATIMER_SETST	Writing a 1 to this bit sets the STATUS event bit 4 in the STATUS register.	
5	RTC_SETST	Writing a 1 to this bit sets the STATUS event bit 5 in the STATUS register.	
6	BOD_SETST	Writing a 1 to this bit sets the STATUS event bit 6 in the STATUS register.	
7	WWDT_SETST	Writing a 1 to this bit sets the STATUS event bit 7 in the STATUS register.	
8	ETH_SETST	Writing a 1 to this bit sets the STATUS event bit 8 in the STATUS register.	
9	USB0_SETST	Writing a 1 to this bit sets the STATUS event bit 9 in the STATUS register.	
10	USB1_SETST	Writing a 1 to this bit sets the STATUS event bit 10 in the STATUS register.	
11	-	Reserved.	
12	CAN_SETST	Writing a 1 to this bit sets the STATUS event bit 12 in the STATUS register.	
13	TIM2_SETST	Writing a 1 to this bit sets the STATUS event bit 13 in the STATUS register.	
14	TIM6_SETST	Writing a 1 to this bit sets the STATUS event bit 14 in the STATUS register.	
15	QEI_SETST	Writing a 1 to this bit sets the STATUS event bit 15 in the STATUS register.	
16	TIM14_SETST	Writing a 1 to this bit sets the STATUS event bit 16 in the STATUS register.	

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Table 27. Interrupt set status register (SET_STAT - address 0x4004 4FEC) bit description

Bit	Symbol	Description	Reset value
18:17	-	Reserved.	
19	RESET_SETST	Writing a 1 to this bit sets the STATUS event bit 19 in the STATUS register.	
31:20	-	Reserved.	-

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7.1 How to read this chapter

Remark: This chapter applies to LPC1850/30/20/10 Rev 'A' only.

The available peripherals vary for different parts.

- Ethernet: available on LPC1850/30.
- USB0: available on LPC1850/30/20.
- USB1: available on LPC1850/30.

If a peripheral is not available, the corresponding bits in the CREG registers are reserved.

7.2 Basic configuration

The CREG block is configured as follows:

- See Table 28 for clocking and power control.
- The CREG block can not be reset by software.

Table 28. CREG clocking and power control

	Base clock	Branch clock	Maximum frequency
CREG	BASE_M3_CLK	CLK_M3_CREG	150 MHz

7.3 Features

The following settings are controlled in the configuration register block:

- BOD trip settings
- Oscillator output
- DMA-to-peripheral muxing
- Ethernet mode
- Memory mapping
- Timer/UART inputs
-

In addition, the Creg block contains the part id and the part configuration information.

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7.4 Register description

Table 29. Register overview: Configuration registers (base address 0x4004 3000)

Name	Access	Address offset	Description	Reset value
IRCTRM	RO	0x000	IRC trim register	0x000F F2BC
CREG0	R/W	0x004	Chip configuration register 32 kHz oscillator output and BOD control register.	
PMUCON		0x008	Power mode control register.	0x0000 0000
-	-	0x008 - 0x0FC	Reserved	-
M3MEMMAP	R/W	0x100	ARM Cortex-M3 memory mapping	
-	-	0x104	Reserved	-
CREG1	RO	0x108	Chip configuration register 1	
CREG2	RO	0x10C	Chip configuration register 2	
CREG3	RO	0x110	Chip configuration register 3	
CREG4	RO	0x114	Chip configuration register 4	
CREG5	R/W	0x118	Chip configuration register 5. Controls JTAG access.	
DMAMUX	R/W	0x11C	DMA muxing control	
-	-	0x120 - 0x124	Reserved	-
ETBCFG	R/W	0x128	ETB RAM configuration	0x0000 0000
CREG6	R/W	0x12C		
-	-	0x130 - 0x1FC	Reserved	-
CHIPID	RO	0x200	Part ID	
-	-	0x204 - 0x2FC	Reserved	-
-	-	0x300		
		0x304		
		0x308		
-	-	0x30C - 0xEFC	Reserved	-
LOCKREG		0xF00	Lock register; blocks write access to CREG registers	

7.4.1 IRC trim register

Table 30. IRC trim register (IRCTRM, address 0x4004 3000) bit description

Bit	Symbol	Description	Reset value	Access
11:0	TRM	IRC trim value	0x2BC	R
19:12	-	Reserved	0xFF	R
31:20	-	Reserved	-	-

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7.4.2 CREG0 control register

Table 31. CREG0 register (CREG0, address 0x4004 3004) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	EN1KHZ		Enable 1 kHz output.	0	R/W
		0	1 kHz output disabled.		
		1	1 kHz output enabled.		
1	EN32KHZ		Enable 32 kHz output	0	R/W
		0	32 kHz output disabled.		
		1	32 kHz output enabled.		
2	RESET32KHZ		32 kHz oscillator reset	1	R/W
		0	<tbd>		
		1	<tbd>		
3	32KHZPD		32 kHz power control.	1	R/W
		0	32 kHz oscillator powered.		
		1	32 kHz oscillator powered-down.		
4	-		Reserved	-	-
5	USB0PHY		USB0 PHY power control.	<tbd>	R/W
		0	USB0 PHY powered.		
		1	USB0 PHY powered down.		
7:6	ALARMCTRL		RTC_ALARM pin output control	<tbd>	R/W
		0x0	RTC alarm.		
		0x1	Event router event.		
		0x2	Event router or <tbd>.		
		0x3	Inactive.		
9:8	BODLVL1		BOD trip level to generate an interrupt.	11	R/W
		0x0	2.75 V		
		0x1	2.85 V		
		0x2	2.95 V		
		0x3	3.05 V		
11:10	BODLVL2		BOD trip level to generate a reset.	11	R/W
		0x0	1.70 V		
		0x1	1.80 V		
		0x2	1.90 V		
		0x3	2.00 V		
31:12	-		Reserved	-	-

7.4.3 Power mode control register

For details on power mode selection, see Section 8.2.

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Table 32. Power mode control register (PMUCON, address 0x4004 3008) bit description

Bit	Symbol	Value	Description	Reset value	Access
1:0	PMUCON		Controls power mode.	0	R/W
		0x0	Normal		
		0x1	Low-power		
		0x2	Reserved		
		0x3	Normal		
31:2	-		Reserved	-	-

7.4.4 ARM Cortex-M3 memory mapping register

Table 33. Memory mapping register (M3MEMMAP, address 0x4004 3100) bit description

Bit	Symbol	Description	Reset value	Access
11:0		Reserved	0x000	-
31:12	M3MAP	Shadow address when accessing memory at address 0x0000 0000	0x1040 0000	R/W

7.4.5 CREG5 control register

Table 34. CREG5 control register (CREG5, address 0x4004 3118) bit description

Bit	Symbol	Description	Reset value	Access
4:0	-	Reserved.	-	-
5	-	Reserved.	0	-
6	M3TAPSEL	<tbd>	0	R/W
7	-	Reserved.	0	-
8	-	Reserved.	0	-
31:9	-	Reserved.	-	-

7.4.6 DMA muxing register

This register controls which set of peripherals is connected to the DMA controller (see Table 195).

Table 35. DMA muxing register (DMAMUX, address 0x4004 311C) bit description

Bit	Symbol	Value	Description	Reset value	Access
1:0	DMAMUXCH0		Select DMA to peripheral connection for DMA peripheral 0.	0	R/W
		0x0	SPIFI		
		0x1	SCT match 2		
		0x2	Reserved		
		0x3	T3 match 1		

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Table 35. DMA muxing register (DMAMUX, address 0x4004 311C) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
3:2	DMAMUXCH1		Select DMA to peripheral connection for DMA peripheral 1	0	R/W
		0x0	Timer 0 match 0		
		0x1	USART0 transmit		
		0x2	Reserved		
		0x3	AES input		
5:4	DMAMUXCH2		Select DMA to peripheral connection for DMA peripheral 2.	0	R/W
		0x0	Timer 0 match 1		
		0x1	USART0 receive		
		0x2	Reserved		
		0x3	AES output		
7:6	DMAMUXCH3		Select DMA to peripheral connection for DMA peripheral 3.	0	R/W
		0x0	Timer 1 match 0		
		0x1	UART1 transmit		
		0x2	I2S1 channel 0		
		0x3	SSP1 transmit		
9:8	DMAMUXCH4		Select DMA to peripheral connection for DMA peripheral 4.	0	R/W
		0x0	Timer 1 match 1		
		0x1	UART1 receive		
		0x2	I2S1 channel 1		
		0x3	SSP1 receive		
11:10	DMAMUXCH5		Select DMA to peripheral connection for DMA peripheral 5.	0	R/W
		0x0	Timer 2 match 0		
		0x1	USART2 transmit		
		0x2	SSP1 transmit		
		0x3	Reserved		
13:12	DMAMUXCH6		Selects DMA to peripheral connection for DMA peripheral 6.	0	R/W
		0x0	Timer 2 match 1		
		0x1	USART2 receive		
		0x2	SSP1 receive		
		0x3	Reserved		
15:14	DMAMUXCH7		Selects DMA to peripheral connection for DMA peripheral 7.	0	R/W
		0x0	Timer 3 match l 0		
		0x1	USART3 transmit		
		0x2	SCT match output 0		
		0x3	Reserved		

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Table 35. DMA muxing register (DMAMUX, address 0x4004 311C) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
17:16	DMAMUXCH8		Select DMA to peripheral connection for DMA peripheral 8.	0	R/W
		0x0	Timer 3 match 1		
		0x1	USART3 receive		
		0x2	SCT match output 1		
		0x3	Reserved		
19:18	DMAMUXCH9		Select DMA to peripheral connection for DMA peripheral 9.	0	R/W
		0x0	SSP0 receive		
		0x1	I2S0 channel 0		
		0x2	SCT match output 1		
		0x3	Reserved		
21:20	DMAMUXCH10		Select DMA to peripheral connection for DMA peripheral 10.	0	R/W
		0x0	SSP0 transmit		
		0x1	I2S0 channel 1		
		0x2	SCT match output 0		
		0x3	Reserved		
23:22	DMAMUXCH11		Selects DMA to peripheral connection for DMA peripheral 11.	0	R/W
		0x0	SSP1 receive		
		0x1	Reserved		
		0x2	USART0 transmit		
		0x3	Reserved		
25:24	DMAMUXCH12		Select DMA to peripheral connection for DMA peripheral 12.	0	R/W
		0x0	SSP1 transmit		
		0x1	Reserved		
		0x2	USART0 receive		
		0x3	Reserved		
27:26	DMAMUXCH13		Select DMA to peripheral connection for DMA peripheral 13.	0	R/W
		0x0	ADC0		
		0x1	AES input		
		0x2	SSP1 receive		
		0x3	USART3 receive		
29:28	DMAMUXCH14		Select DMA to peripheral connection for DMA peripheral 14.	0	R/W
		0x0	ADC1		
		0x1	AES output		
		0x2	SSP1 transmit		
		0x3	USART3 transmit		

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Table 35. DMA muxing register (DMAMUX, address 0x4004 311C) bit description ...continued

Bit	Symbol	Value	Description	Reset value	Access
31:30	DMAMUXCH15		Select DMA to peripheral connection for DMA peripheral 15.	0	R/W
		0x0	DAC		
		0x1	SCT match output 3		
		0x2	Reserved		
		0x3	Timer 3 match 0		

7.4.7 ETB SRAM configuration register

This register selects the interface that is used to the 16 kB block of RAM located at address 0x2000 C000. This RAM memory block can be accessed either by the ETB or be used as normal SRAM on the AHB bus.

Note that by default, this memory area will be accessed by the ETB.

Table 36. ETB SRAM configuration register (ETBCFG, address 0x4004 3128) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	ETB		Select SRAM interface	0	R/W
		0	ETB accesses SRAM at address 0x2000 C000.		
		1	AHB accesses SRAM at address 0x2000 C000.		
31:1	-		Reserved.	-	-

7.4.8 CREG6 control register

This register controls various aspects of the LPC18xx:

- Bits 2:0 control the Ethernet PHY interface. The ethernet block reads this register during set-up, and therefore the ethernet must be reset after changing the PHY interface.
- Bits 12:15 control the I2S connections.
- Bit 16 controls the external memory controller clocking.

Table 37. CREG6 control register (CREG6, address 0x4004 312C) bit description

Bit	Symbol	Value	Description	Reset value	Access
2:0	ETHMODE		Selects the Ethernet mode. Reset the ethernet after changing the PHY interface. All other settings are reserved.		R/W
		0x0	MII		
		0x4	RMII		
3	-		Reserved.		R/W
4	TIMCTRL		<tbd>	0	R/W
		0	<tbd>		
		1	<tbd>		

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Table 37. CREG6 control register (CREG6, address 0x4004 312C) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
11: 5	-		Reserved.	-	-
12	I2S0_TX_SCK_IN_SEL		I2S0_TX_SCK input select	0	R/W
		0	I2 S clock selected as defined by the I2S transmit mode register Table 744.		
		1	Audio PLL for I2S transmit clock MCLK input and MCLK output. The I2S must be configured in slave mode.		
13	I2S0_RX_SCK_IN_SEL		I2S0_RX_SCK input select	0	R/W
		0	I2 S clock selected as defined by the I2S receive mode register Table 745.		
		1	Audio PLL for I2S receive clock MCLK input and MCLK output. The I2S must be configured in slave mode.		
14	I2S1_TX_SCK_IN_SEL		I2S1_TX_SCK input select	0	R/W
		0	I2 S clock selected as defined by the I2S transmit mode register Table 744.		
		1	Audio PLL for I2S transmit clock MCLK input and MCLK output. The I2S must be configured in slave mode.		
15	I2S1_RX_SCK_IN_SEL		I2S1_RX_SCK input select	0	R/W
		0	I2 S clock selected as defined by the I2S receive mode register Table 745.		
		1	Audio PLL for I2S receive clock MCLK input and MCLK output. The I2S must be configured in slave mode.		
16	EMC_CLK_SEL		EMC_CLK divided clock select (see Section 19.1).	0	R/W
		0	EMC_CLK_DIV not divided.		
		1	EMC_CLK_DIV divided by 2.		
31: 17	-		Reserved.	-	-

7.4.9 Part ID register

Table 38. Part ID register (CHIPID, address 0x4004 3200) bit description

Bit	Symbol	Description	Reset value	Access
31:0	ID	<tbd>		

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8.1 How to read this chapter

The power management controller is identical on all LPC18xx parts.

8.2 General description

The PMC implements the control sequences to enable transitioning between different power modes and controls the power state of each peripheral. In addition, wake-up from a low-power mode based on hardware events is supported.

Low-power modes can be reached from Active mode only, and transitions between low-power modes are not allowed.

The PMC supports the following low-power modes: Deep-sleep, Power-down, and Deep power-down. The wake-up from a low-power mode will always result in the Active mode.

The LPC18xx supports five power modes in order from highest to lowest power consumption:

1. Active mode
2. Sleep mode (controlled by the ARM Cortex-M3 core)
3. Deep-sleep mode (controlled by the ARM Cortex-M3 core)
4. Power-down mode (controlled by the ARM Cortex-M3 core)
5. Deep power-down mode

8.2.1 Active mode

By default, the LPC18xx is in Active mode, which means that every peripheral can perform a functional operation at nominal operating conditions. The other low-power modes are standby modes in which the peripheral clocks are disabled and operating conditions are adapted to achieve further power savings. The peripheral clocks are enabled again at wake-up.

In Active (or Sleep mode), three operating modes are supported.

- Low-power mode: The CPU and core logic operate slower and the core supply voltage is reduced.
- Normal mode: The CPU operates at the nominal supply voltage.

The operating modes are programmable through a power API and through the PMUCON register in the CREG block (see Table 32).

8.2.2 Sleep mode

In Sleep mode the CPU clock is shut down to save power; the peripherals can still remain active and fully functional. The Sleep mode is entered by a WFI or WFE instruction if the SLEEPDEEP bit in the ARM Cortex-M3 system control register is set to 0.

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As in active mode, low-power and normal modes can be selected.

8.2.3 Deep-sleep mode

In Deep-sleep mode the CPU clock and peripheral clocks are shut down to save power; logic states and SRAM memory are maintained. All analog blocks and the BOD control circuit are powered down. The Deep-sleep mode is entered by a WFI or WFE instruction if the SLEEPDEEP bit in the ARM Cortex-M3 system control register is set to 1 and the PD0_SLEEP0_MODE register (see Table 41) is programmed with the Deep-sleep mode value.

When the LPC18xx wakes up from Deep-sleep mode, the 12 MHz IRC is used as the clock source for all base clocks.

Remark: Before entering Deep-sleep mode, program the CGU as follows:

- Switch the clock source of all base clocks to the IRC.
- Put the PLLs in power-down mode.

Reprogramming the CGU avoids any undefined or unlocked PLL clocks at wake-up and minimizes power consumption during Deep-sleep mode.

8.2.4 Power-down mode

In Power-down mode the CPU clock and peripheral clocks are shut down but logic states are maintained. All SRAM memory except for the upper 8 kB of the local SRAM located at 0x1008 0000, all analog blocks, and the BOD control circuit are powered down.The Power-down mode is entered by a WFI or WFE instruction if the SLEEPDEEP bit in the ARM Cortex-M3 system control register is set to 1 and the PD0_SLEEP0_MODE register (see Table 41) is programmed with the Power-down mode value.

When the LPC18xx wakes up from Power-down mode, the 12 MHz IRC is used as the clock source for all base clocks.

Remark: Before entering Power-down mode, program the CGU as follows:

- Switch the clock source of all base clocks to the IRC.
- Put the PLLs in power-down mode.

Reprogramming the CGU avoids any undefined or unlocked PLL clocks at wake-up and minimizes power consumption during Power-down mode.

8.2.5 Deep power-down

In Deep power-down mode the entire core logic is powered down. Only the logic in the RTC power domain remains active. The Deep power-down mode is entered by a WFI or WFE instruction if the SLEEPDEEP bit in the ARM Cortex-M3 system control register is set to 1 and the PD0_SLEEP0_MODE register (see Table 41) is programmed with the Deep power-down value.

When the LPC18xx wakes up from Deep power-down mode, the boot loader configures the PLL1 as the clock source running at 72 MHz.

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8.3 Register description

Table 39. Register overview: Power Mode Controller (PMC) (base address 0x4004 2000)

Name	Access	Address offset	Description	Reset value
PD0_SLEEP0_HW_ENA	R/W	0x000	Hardware sleep event enable register	0x0000 0001
-	-	0x004 - 0x018	Reserved	-
PD0_SLEEP0_MODE	R/W	0x01C	Sleep power mode register	

8.3.1 Hardware sleep event enable register PD0_SLEEP0_HW_ENA

Table 40. Hardware sleep event enable register (PD0_SLEEP0_HW_ENA - address 0x4004 2000) bit description

Bit	Symbol	Description	Reset value	Access
0	ENA_EVENT0	Writing a 1 enables any sleep modes for Cortex-M3.	1	R/W
31:1	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-	-

8.3.2 Sleep power mode register PD0_SLEEP0_MODE

The PD0_SLEEP0_MODE register controls which of the three reduced power modes, Deep-sleep, Power-down, or Deep power-down is entered when an ARM WFE/WFI instruction is issued and the SLEEPDEEP bit is set to 1.

Remark: Only the three values listed in Table 41 are allowed settings for the PD0_SLEEP0_MODE register.

Table 41. Sleep power mode register (PD0_SLEEP0_MODE - address 0x4004 201C) bit description

Bit	Symbol	Description	Reset value	Access
31:0	PWR_STATE	Selects between Deep-sleep, Power-down, and Deep power-down modes. Only one of the following three values can be programmed in this register: 0x003F 00AA = Deep-sleep mode 0x003F FCBA = Power-down mode 0x003F FF7F = Deep power-down mode		R/W

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8.4 Functional description

8.4.1 Run-time programming

The PD0_SLEEP0_MODE register can be programmed at run-time to change the default power state of the LPC18xx after the next transition to a reduced-power state. The default state is Deep power-down corresponding to a reset value of the PD0_SLEEP0_MODE register of 0x003F FF7F.

Table 42. Typical settings for PMC power modes

Power mode	PD0_SLEEP0_MODE register bit settings	Description
Deep-sleep	0x0030 00AA	CPU, peripherals, analog, USB PHY, and retention supplies in retention mode; all SRAM supplies in active mode; IO pads powered [1], BOD in power-down mode.
Power-down	0x0030 FC3A	CPU, peripherals, analog supplies in retention mode; USB PHY in power-down mode; retention in retention mode; SRAM1 in active mode; all other SRAMs in power-down mode; IO pads powered[1], BOD in power-down mode.
Deep power-down	0x0030 FF7F	CPU, peripherals, analog, USB PHY in power-down mode; all SRAMs, IO pads powered[1], BOD in power-down mode.

[1] When the IO pads are off, the external IO supply should be removed. Pin RTC_ALARM can be used to indicate when the event router and the core become active and when the IO should be powered on.

8.4.2 Power API

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9.1 How to read this chapter

Remark: This chapter describes the clock generation of parts LPC1850/30/20/10 Rev 'A' and parts LPC18xx (with on-chip flash). Note that register clocks and clock control registers are specific to parts LPC1850/30/20/10 rev "A" and parts LPC18xx (with on-chip flash). For a description of the CGU of parts LPC1850/30/20/10 Rev '-', see Section 42.4.

Ethernet, USB0, USB1, and LCD related clocks are not available on all packages. See Section 1.3. The corresponding clock control registers are reserved.

9.2 Basic configuration

The CGU is configured as follows:

- See Table 43 for clocking and power control.
- Do not reset the CGU during normal operation.

Table 43. CGU clocking and power control

	Base clock	Branch clock	Maximum frequency
CGU	BASE_M3_CLK	CLK_M3_BUS	150 MHz

9.3 Features

- PLL control
- Oscillator control
- Clock generation and clock source multiplexing
- Five integer dividers

9.4 General description

The CGU generates multiple independent clocks for the core and the peripheral blocks of the LPC18x. Each independent clock is called a base clock and itself is one of the inputs to the two Clock Control Units (CCUs) which control the branch clocks to the individual peripherals (see Chapter 10).

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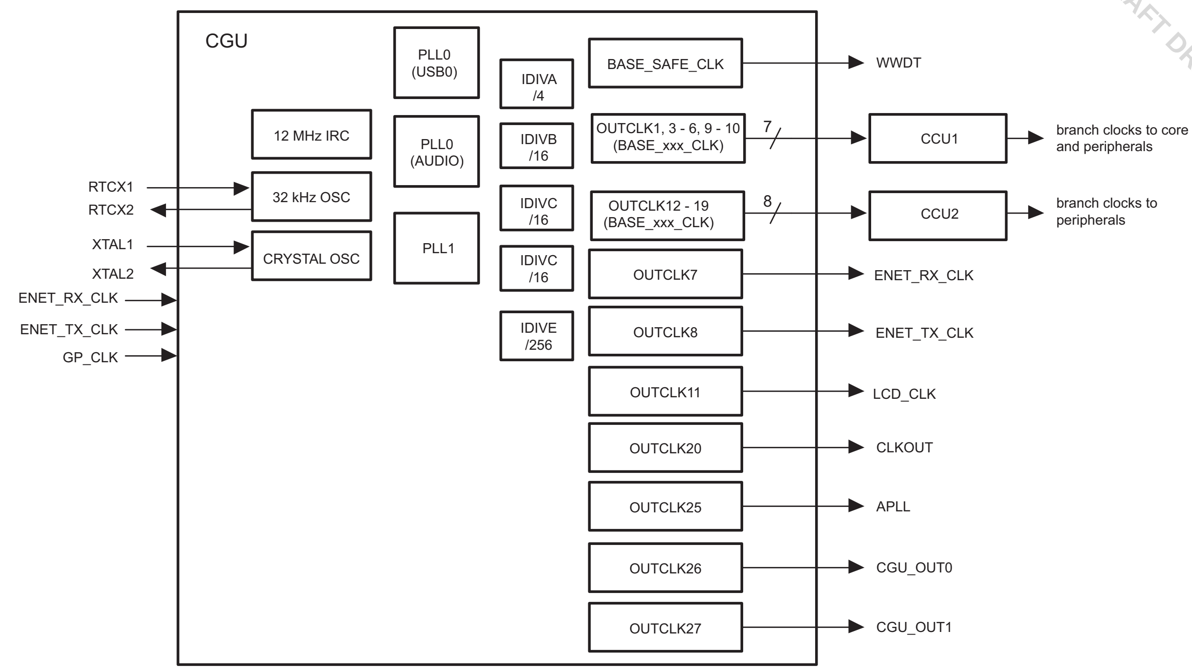


Fig 17. CGU and CCU0/1 block diagram

The CGU selects the inputs to the clock generators from multiple clock sources, controls the clock generation, and routes the outputs of the clock generators through the clock source bus to the output stages. Each output stage provides an independent clock source and corresponds to one of the base clocks for the LPC18xx. See Table 44 for a description of each base clock and Table 46 for the possible clock sources for each base clock.

The CGU contains four types of clock generators:

1. External clock inputs and internal clocks: The external clock inputs are the Ethernet PHY clocks and the general purpose input clock GP_CLKIN. The clocks from the internal oscillators are the IRC and the 32 kHz oscillator output clocks. These clock generators have no selectable inputs from the clock source bus and provide one clock output each to the clock source bus.
2. Crystal oscillator: The crystal oscillator is controlled by the CGU. The input to the crystal oscillator are the XTAL pins. The crystal oscillator creates one output to the clock source bus.
3. PLLs: PLL0 (USB0), PLL0 (audio), and PLL1 are controlled by the CGU. Each PLL can select one input from the clock source bus and provides one output to the clock source bus. The input to the PLLs can be selected from all external and internal clocks and oscillators, from the other PLLs, and from the outputs of any of the integer dividers (see Table 45). One PLL0 cannot select the other PLL0 as input.
4. Integer dividers: Each of the five integer dividers can select one input from the clock source bus and creates one divided output clock to the clock source bus. The input to all integer dividers can be selected from all external and internal clocks and oscillators, and from all three PLLs. In addition, the output of the first integer divider can be selected as an input to all other integer dividers (see Table 45).

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– Integer divider A: maximum division factor = 4 (see Table 62).
– Integer dividers B, C, D: maximum division factor = 16 (see Table 63).
– Integer divider E: maximum division factor = 256 (see Table 64).

The output stages select a clock source from the clock source bus for each base clock (see Table 46). Except for the base clocks to the WWDT (BASE_SAFE_CLK) and USB0 (BASE_USB0_CLK), the clock source for each output stage can be any of the external and internal clocks and oscillators directly or one of the PLL outputs or any of the outputs of the integer dividers.

Table 44. CGU0 base clocks

Number	Name	Frequency [1]	Description
0	BASE_SAFE_CLK	12 MHz	Base safe clock (always on) for WDT
1	BASE_USB0_CLK	480 MHz	Base clock for USB0
2	-	-	Reserved
3	BASE_USB1_CLK	150 MHz	Base clock for USB1
4	BASE_M3_CLK	150 MHz	System base clock for ARM Cortex-M3 core and APB peripheral blocks #0 and #2
5	BASE_SPIFI_CLK	150 MHz	Base clock for SPIFI
6	-	150 MHz	Reserved
7	BASE_PHY_RX_CLK	75 MHz	Base clock for Ethernet PHY Rx
8	BASE_PHY_TX_CLK	75 MHz	Base clock for Ethernet PHY Tx
9	BASE_APB1_CLK	150 MHz	Base clock for APB peripheral block # 1
10	BASE_APB3_CLK	150 MHz	Base clock for APB peripheral block # 3
11	BASE_LCD_CLK	150 MHz	Base clock for LCD
12	BASE_ENET_CSR_CLK	<tbd>	Base clock for <tbd>
13	BASE_SDIO_CLK	150 MHz	Base clock for SD/MMC
14	BASE_SSP0_CLK	150 MHz	Base clock for SSP0
15	BASE_SSP1_CLK	150 MHz	Base clock for SSP1
16	BASE_UART0_CLK	150 MHz	Base clock for UART0
17	BASE_UART1_CLK	150 MHz	Base clock for UART1
18	BASE_UART2_CLK	150 MHz	Base clock for UART2
19	BASE_UART3_CLK	150 MHz	Base clock for UART3
20	BASE_OUT_CLK	150 MHz	Base clock for CLKOUT pin
21-24	-	-	Reserved
25	BASE_APLL_CLK	150 MHz	Base clock for audio PLL
26	BASE_CGU_OUT0_CLK	150 MHz	Base clock for CGU_OUT0 clock output
27	BASE_CGU_OUT1_CLK	150 MHz	Base clock for CGU_OUT1 clock output

[1] Maximum frequency that guarantees stable operation of the LPC18xx.

Table 45 shows all available input clock sources for each clock generator.

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Table 45. Available clock sources for clock generators with selectable inputs

Clock sources	Clock generators PLL0 (USB)	PLL0 (audio)	PLL1	IDIVA /4	IDIVB /16	IDIVC /16	IDIVD /16	IDIVE /256
32 kHz oscillator	yes	yes	yes	yes	yes	yes	yes	yes
IRC 12 MHz	yes	yes	yes	yes	yes	yes	yes	yes
ENET_RX_CLK	yes	yes	yes	yes	yes	yes	yes	yes
ENET_TX_CLK	yes	yes	yes	yes	yes	yes	yes	yes
GP_CLKIN	yes	yes	yes	yes	yes	yes	yes	yes
Crystal oscillator	yes	yes	yes	yes	yes	yes	yes	yes
PLL0 (USB)	no	no	yes	yes	no	no	no	no
PLL0 (audio)	no	no	yes	yes	yes	yes	yes	yes
PLL1	yes	yes	no	yes	yes	yes	yes	yes
IDIVA	yes	yes	yes	no	yes	yes	yes	yes
IDIVB	yes	yes	yes	no	no	no	no	no
IDIVC	yes	yes	yes	no	no	no	no	no
IDIVD	yes	yes	yes	no	no	no	no	no
IDIVE	yes	yes	yes	no	no	no	no	no

Table 46. Clock sources for output stages

Clock sources	Output stages (d = default clock source, y = yes (clock source available), n = no (clock source not available)) BASE_SAFE_CLK	BASE_USB0_CLK	BASE_USB1_CLK	BASE_M3_CLK	BASE_SPIFI_CLK	Reserved	BASE_PHY_RX_CLK	BASE_PHY_TX_CLK	BASE_APB1_CLK	BASE_APB3_CLK	BASE_LCD_CLK	BASE_ENETCSR_CLK	BASE_SDIO_CLK	BASE_SSP0_CLK	BASE_SSP1_CLK	BASE_UART0_CLK	BASE_UART1_CLK	BASE_UART2_CLK	BASE_UART3_CLK	BASE_OUT_CLK	BASE_APLL_CLK	BASE_CGU_OUT0_CLK	BASE_CGU_OUT1_CLK
32 kHz oscillator	n	n	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
IRC 12 MHz	d	n	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d
ENET_ RX_CLK	n	n	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
ENET_ TX_CLK	n	n	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
GP_ CLKIN	n	n	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
Crystal oscillator	n	n	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
PLL0 (USB)	n	d	y	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	y	n	y	y
PLL0 (audio)	n	n	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y

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Table 46. Clock sources for output stages

Clock sources	Output stages (d = default clock source, y = yes (clock source available), n = no (clock source not available))																						
	BASE_SAFE_CLK	BASE_USB0_CLK	BASE_USB1_CLK	BASE_M3_CLK	BASE_SPIFI_CLK	Reserved	BASE_PHY_RX_CLK	BASE_PHY_TX_CLK	BASE_APB1_CLK	BASE_APB3_CLK	BASE_LCD_CLK	BASE_ENETCSR_CLK	BASE_SDIO_CLK	BASE_SSP0_CLK	BASE_SSP1_CLK	BASE_UART0_CLK	BASE_UART1_CLK	BASE_UART2_CLK	BASE_UART3_CLK	BASE_OUT_CLK	BASE_APLL_CLK	BASE_CGU_OUT0_CLK	BASE_CGU_OUT1_CLK
PLL1	n	n	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
IDIVA	n	n	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
IDIVB	n	n	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
IDIVC	n	n	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
IDIVD	n	n	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
IDIVE	n	n	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y

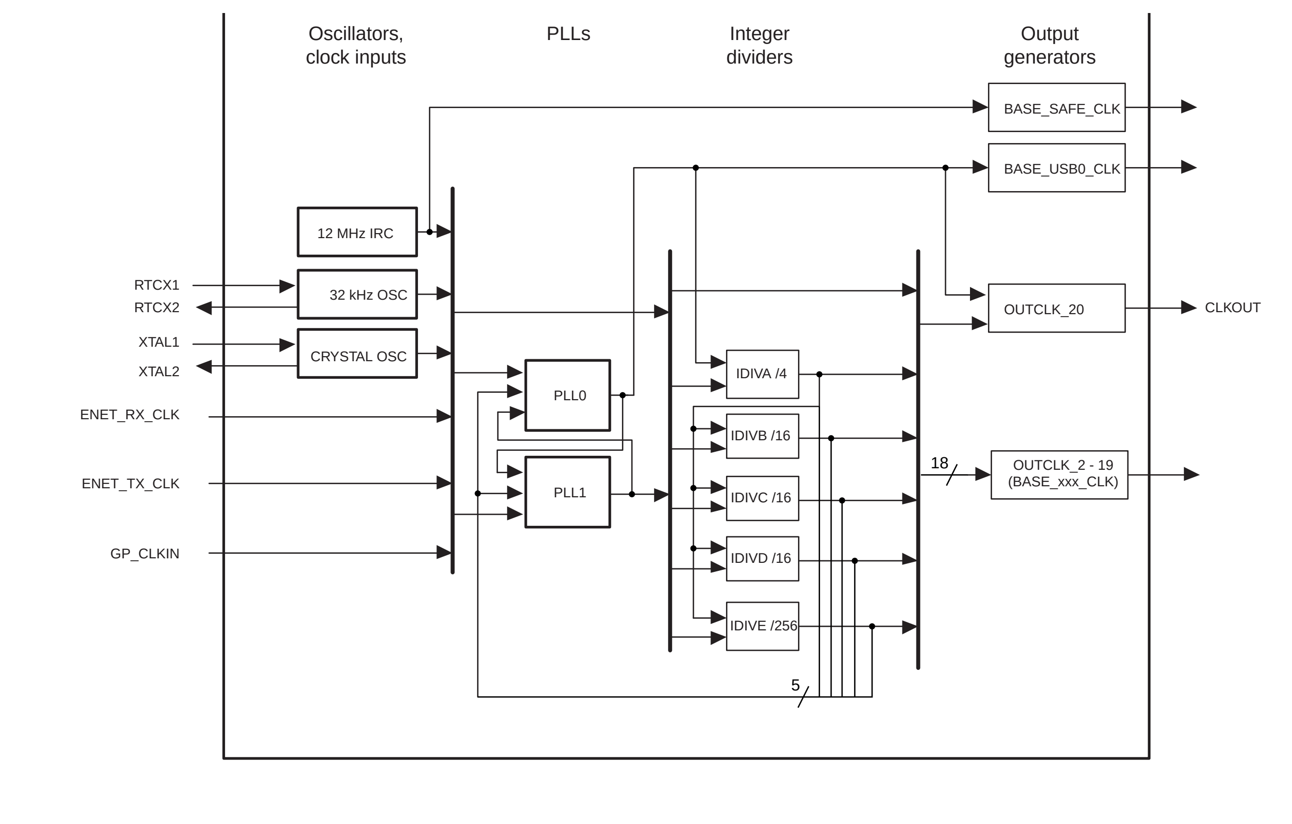


Fig 18. CGU block diagram

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9.5 Pin description

Table 47. CGU pin description

Pin name/ function name	Direction	Description
XTAL1	I	Crystal oscillator input
XTAL2	O	Crystal oscillator output
RTCX1	I	RTC 32 kHz oscillator input
RTCX2	O	RTC 32 kHz oscillator output
GP_CLKIN	I	General purpose input clock
ENET_TX_CLK	I	Ethernet PHY transmit clock
ENET_RX_CLK	I	Ethernet PHY receive clock
CLKOUT	O	Clock output pin
CGU_OUT0	O	CGU spare output 0
CGU_OUT1	O	CGU spare output 1

9.6 Register description

The register addresses of the CGU are shown in Table 48.

Remark: The CGU is configured by the boot loader at reset and when waking up from Deep power-down to produce a 72 MHz clock using PLL1. Note that this configuration is not reflected in the reset values given in Table 48.

Table 48. Register overview: CGU (base address 0x4005 0000)

Name	Access	Address offset	Description	Reset value
-	R	0x000	Reserved	0x0110 0106
-	R	0x004	Reserved	0x0010 0500
-	R	0x008	Reserved	0x1C00 0000
-	R	0x00C	Reserved	0x0000 0000
-	-	0x010	Reserved	-
FREQ_MON	R/W	0x014	Frequency monitor register	0x0000 0000
XTAL_OSC_CTRL	R/W	0x018	Crystal oscillator control register	0x0000 0005
PLL0USB_STAT	R	0x01C	PLL0 (USB) status register	0x0100 0000
PLL0USB_CTRL	R/W	0x020	PLL0 (USB) control register	0x0100 0003
PLL0USB_MDIV	R/W	0x024	PLL0 (USB) M-divider register	0x05F8 5B6A
PLL0USB_NP_DIV	R/W	0x028	PLL0 (USB) N/P-divider register	0x000B 1002
PLL0AUDIO_STAT	R	0x02C	PLL0 (audio) status register	0x0100 0000
PLL0AUDIO_CTRL	R/W	0x030	PLL0 (audio) control register	0x0100 4003
PLL0AUDIO_MDIV	R/W	0x034	PLL0 (audio) M-divider register	0x05F8 5B6A
PLL0AUDIO_NP_DIV	R/W	0x038	PLL0 (audio) N/P-divider register	0x000B 1002
PLLAUDIO_FRAC	R/W	0x03C	PLL0 (audio)	0x0020 0000
PLL1_STAT	R	0x040	PLL1 status register	0x0100 0000
PLL1_CTRL	R/W	0x044	PLL1 control register	0x0100 0003

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Table 48. Register overview: CGU (base address 0x4005 0000)

Name	Access	Address offset	Description	Reset value
IDIVA_CTRL	R/W	0x048	Integer divider A control register	0x0100 0000
IDIVB_CTRL	R/W	0x04C	Integer divider B control register	0x0100 0000
IDIVC_CTRL	R/W	0x050	Integer divider C control register	0x0100 0000
IDIVD_CTRL	R/W	0x054	Integer divider D control register	0x0100 0000
IDIVE_CTRL	R/W	0x058	Integer divider E control register	0x0100 0000
OUTCLK_0_CTRL	R/W	0x05C	Output stage 0 control register for base clock BASE_SAFE_CLK	0x0100 0000
OUTCLK_1_CTRL	R/W	0x060	Output stage 1 control register for base clock BASE_USB0_CLK	0x0700 0000
-	-	0x064	Reserved	-
OUTCLK_3_CTRL	R/W	0x068	Output stage 3 control register for base clock BASE_USB1_CLK	0x0100 0000
OUTCLK_4_CTRL	R/W	0x06C	Output stage 4 control register for base clock BASE_M3_CLK	0x0100 0000
OUTCLK_5_CTRL	R/W	0x070	Output stage 5 control register for base clock BASE_SPIFI_CLK	0x0100 0000
-	R/W	0x074	Reserved	0x0100 0000
OUTCLK_7_CTRL	R/W	0x078	Output stage 7 control register for base clock BASE_PHY_RX_CLK	0x0100 0000
OUTCLK_8_CTRL	R/W	0x07C	Output stage 8 control register for base clock BASE_PHY_TX_CLK	0x0100 0000
OUTCLK_9_CTRL	R/W	0x080	Output stage 9 control register for base clock BASE_APB1_CLK	0x0100 0000
OUTCLK_10_CTRL	R/W	0x084	Output stage 10 control register for base clock BASE_APB3_CLK	0x0100 0000
OUTCLK_11_CTRL	R/W	0x088	Output stage 11 control register for base clock BASE_LCD_CLK	0x0100 0000
OUTCLK_12_CTRL	R/W	0x08C	Output stage 11 control register for base clock BASE_ENET_CSR_CLK	0x0100 0000
OUTCLK_13_CTRL	R/W	0x090	Output stage 13 control register for base clock BASE_SDIO_CLK	0x0100 0000
OUTCLK_14_CTRL	R/W	0x094	Output stage 14 control register for base clock BASE_SSP0_CLK	0x0100 0000
OUTCLK_15_CTRL	R/W	0x098	Output stage 15 control register for base clock BASE_SSP1_CLK	0x0100 0000
OUTCLK_16_CTRL	R/W	0x09C	Output stage 16 control register for base clock BASE_UART0_CLK	0x0100 0000
OUTCLK_17_CTRL	R/W	0x0A0	Output stage 17 control register for base clock BASE_UART1_CLK	0x0100 0000
OUTCLK_18_CTRL	R/W	0x0A4	Output stage 18 control register for base clock BASE_UART2_CLK	0x0100 0000
OUTCLK_19_CTRL	R/W	0x0A8	Output stage 19 control register for base clock BASE_UART3_CLK	0x0100 0000

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Table 48. Register overview: CGU (base address 0x4005 0000)

Name	Access	Address offset	Description	Reset value
OUTCLK_20_CTRL	R/W	0x0AC	Output stage 20 control register for base clock BASE_OUT_CLK	0x0100 0000
OUTCLK_21_CTRL to OUTCLK_24_CTRL	R/W	0x0B0 to 0x0BC	Reserved output stages	-
OUTCLK_25_CTRL	R/W	0x0C0	Output stage 25 control register for base clock BASE_APLL_CLK	
OUTCLK_26_CTRL	R/W	0x0C4	Output stage 26 control register for base clock BASE_CGU_OUT0_CLK	
OUTCLK_27_CTRL	R/W	0x0C8	Output stage 27 control register for base clock BASE_CGU_OUT1_CLK	

9.6.1 Frequency monitor register

The CGU can report the relative frequency of any operating clock. The clock to be measured must be selected by software, while the fixed-frequency IRC clock fref is used as the reference frequency. A 14-bit counter then counts the number of cycles of the measured clock that occur during a user-defined number of reference-clock cycles. When the MEAS bit is set, the measured-clock counter is reset to 0 and counts up, while the 9-bit reference-clock counter is loaded with the value in RCNT and then counts down towards 0. When either counter reaches its terminal value both counters are disabled and the MEAS bit is reset to 0. The current values of the counters can then be read out and the selected frequency obtained by the following equation:

$$fselected = \frac{Qselected}{(Qref[initial] - Qref[final])} \times fref$$

If RCNT is programmed to a value equal to the core clock frequency in kHz and reaches 0 before the FCNT counter saturates, the value stored in FCNT would then show the measured clock's frequency in kHz without the need for any further calculation.

Note that the accuracy of this measurement can be affected by several factors:

1. Quantization error is noticeable if the ratio between the two clocks is large (e.g. 100 kHz vs. 1 kHz), because one counter saturates while the other still has only a small count value.
2. Due to synchronization, the counters are not started and stopped at exactly the same time.
3. The measured frequency can only be to the same level of precision as the reference frequency.

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Table 49. FREQ_MON register (FREQ_MON, address 0x4005 0014) bit description

Bit	Symbol	Value	Description	Reset value	Access
8:0	RCNT		9-bit reference clock-counter value	0	R/W
22:9	FCNT		14-bit selected clock-counter value	0	R
23	MEAS		Measure frequency	0	R/W
		0	RCNT and FCNT disabled		
		1	Frequency counters started		
28:24	CLK_SEL		Clock-source selection for the clock to be measured. All other values are reserved.	0	R/W
		0x00	32 kHz oscillator (default)		
		0x01	IRC		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	Crystal oscillator		
		0x07	PLL0 (USB)		
		0x08	PLL0 (audio)		
		0x09	PLL1		
		0x0A	Reserved		
		0x0B	Reserved		
		0x0C	IDIVA		
		0x0D	IDIVB		
		0x0E	IDIVC		
		0x0F	IDIVD		
		0x10	IDIVE		
31:29	-		Reserved	-	-

9.6.2 Crystal oscillator control register

The register XTAL_OSC_CONTROL contains the control bits for the crystal oscillator.

Table 50. XTAL_OSC_CTRL register (XTAL_OSC_CTRL, address 0x4005 0018) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	ENABLE		Oscillator-pad enable. Do not change the BYPASS and ENABLE bits in one write-action: this will result in unstable device operation!	1	R/W
		0	Enable		
		1	Power-down (default)		

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Table 50. XTAL_OSC_CTRL register (XTAL_OSC_CTRL, address 0x4005 0018) bit description

Bit	Symbol	Value	Description	Reset value	Access
1	BYPASS		Configure crystal operation or external-clock input pin XTAL1. Do not change the BYPASS and ENABLE bits in one write-action: this will result in unstable device operation!	0	R/W
		0	Operation with crystal connected (default).		
		1	Bypass mode. Use this mode when an external clock source is used instead of a crystal.		
2	HF		Select frequency range	1	R/W
		0	Oscillator low-frequency mode (crystal or external clock source 1 to 20 MHz). Between 15 MHz to 20 MHz, the state of the HF bit is don’t care.		
		1	Oscillator high-frequency mode; crystal or external clock source 15 to 25 MHz. Between 15 MHz to 20 MHz, the state of the HF bit is don’t care (default)		
31:3	-		Reserved	-	-

9.6.3 PLL0 (for USB) registers

The PLL0 provides a dedicated clock to the High-speed USB0 interface and to USB1.

See Section 9.7.4.5 for instructions on how to set up the PLL0.

9.6.3.1 PLL0 (for USB) status register

Table 51. PLL0USB status register (PLL0USB_STAT, address 0x4005 001C) bit description

Bit	Symbol	Description	Reset value	Access
0	LOCK	PLL0 lock indicator	0	R
1	FR	PLL0 free running indicator	0	R
31:2	-	Reserved		-

9.6.3.2 PLL0 (for USB) control register

Table 52. PLL0USB control register (PLL0USB_CTRL, address 0x4005 0020) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		PLL0 power down	1	R/W
		0	PLL0 enabled		
		1	PLL0 powered down		
1	BYPASS		Input clock bypass control	1	R/W
		0	CCO clock sent to post-dividers. Use this in normal operation.		
		1	PLL0 input clock sent to post-dividers (default).		
2	DIRECTI		PLL0 direct input	0	R/W

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Table 52. PLL0USB control register (PLL0USB_CTRL, address 0x4005 0020) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
3	DIRECTO		PLL0 direct output	0	R/W
4	CLKEN		PLL0 clock enable	0	R/W
5	-		Reserved	-	-
6	FRM		Free running mode	0	R/W
7	-		Reserved	0	R/W
8	-		Reserved. Reads as zero. Do not write one to this register.	0	R/W
9	-		Reserved. Reads as zero. Do not write one to this register.	0	R/W
10	-		Reserved. Reads as zero. Do not write one to this register.	0	R/W
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-
28:24	CLK_SEL		Clock source selection. All other values are reserved.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x06	Crystal oscillator		
		0x09	PLL1		
		0x0C	IDIVA		
		0x0D	IDIVB		
		0x0E	IDIVC		
		0x0F	IDIVD		
		0x10	IDIVE		
31:29	-		Reserved	-	-

9.6.3.3 PLL0 (for USB) M-divider register

Table 53. PLL0USB M-divider register (PLL0USB_MDIV, address 0x4005 0024) bit description

Bit	Symbol	Description	Reset value	Access
16:0	MDEC	Decoded M-divider coefficient value. Select values for the M-divider between 1 and 131071.	0x5B6A	R/W

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Table 53. PLL0USB M-divider register (PLL0USB_MDIV, address 0x4005 0024) bit description
…continued

Bit	Symbol	Description	Reset value	Access
21:17	SELP	Bandwidth select P value	11100	R/W
27:22	SELI	Bandwidth select I value	010111	R/W
31:28	SELR	Bandwidth select R value	0000	R/W

9.6.3.4 PLL0 (for USB) NP-divider register

Table 54. PLL0USB NP-divider register (PLL0USB_NP_DIV, address 0x4005 0028) bit description

Bit	Symbol	Description	Reset value	Access
6:0	PDEC	Decoded P-divider coefficient value	000 0010	R/W
11:7	-	Reserved	-	-
21:12	NDEC	Decoded N-divider coefficient value	1011 0001	R/W
31:22	-	Reserved	-	-

9.6.4 PLL0 (for audio) registers

See Section 9.7.4.5 for instructions on how to set up the PLL0.

9.6.4.1 PLL0 (for audio) status register

Table 55. PLL0AUDIO status register (PLL0AUDIO_STAT, address 0x4005 002C) bit description

Bit	Symbol	Description	Reset value	Access
0	LOCK	PLL0 lock indicator	0	R
1	FR	PLL0 free running indicator	0	R
31:2	-	Reserved		-

9.6.4.2 PLL0 (for audio) control register

Table 56. PLL0AUDIO control register (PLL0AUDIO_CTRL, address 0x4005 0030) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		PLL0 power down	1	R/W
		0	PLL0 enabled		
		1	PLL0 powered down		
1	BYPASS		Input clock bypass control	1	R/W
		0	CCO clock sent to post-dividers. Use this in normal operation.		
		1	PLL0 input clock sent to post-dividers (default).		

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Table 56. PLL0AUDIO control register (PLL0AUDIO_CTRL, address 0x4005 0030) bit description
…continued

Bit	Symbol	Value	Description	Reset value	Access
2	DIRECTI		PLL0 direct input	0	R/W
3	DIRECTO		PLL0 direct output	0	R/W
4	CLKEN		PLL0 clock enable	0	R/W
5	-		Reserved	-	-
6	FRM		Free running mode	0	R/W
7	-		Reserved	0	R/W
8	-		Reserved. Reads as zero. Do not write one to this register.	0	R/W
9	-		Reserved. Reads as zero. Do not write one to this register.	0	R/W
10	-		Reserved. Reads as zero. Do not write one to this register.	0	R/W
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
12	PLLFRAQ_ REQ		Fractional PLL word write request	0	R/W
13	SEL_EXT		SD modulator bypass	0	R/W
14	MOD_PD		SD modulator power-down	1	R/W
		0	SD modulator enabled		
		1	SD modulator powered down		
23:15	-		Reserved	-	-
28:24	CLK_SEL		Clock source selection. All other values are reserved.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x06	Crystal oscillator		
		0x09	PLL1		
		0x0C	IDIVA		
		0x0D	IDIVB		
		0x0E	IDIVC		
		0x0F	IDIVD		
		0x10	IDIVE		
31:29	-		Reserved	-	-

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9.6.4.3 PLL0 (for audio) M-divider register

Table 57. PLL0AUDIO M-divider register (PLL0AUDIO_MDIV, address 0x4005 0034) bit description

Bit	Symbol	Description	Reset value	Access
16:0	MDEC	Decoded M-divider coefficient value. Select values for the M-divider between 1 and 131071.	0x5B6A	R/W
21:17	SELP	Bandwidth select P value	11100	R/W
27:22	SELI	Bandwidth select I value	010111	R/W
31:28	SELR	Bandwidth select R value	0000	R/W

9.6.4.4 PLL0 (for audio) NP-divider register

Table 58. PLL0 AUDIO NP-divider register (PLL0AUDIO_NP_DIV, address 0x4005 0038) bit description

Bit	Symbol	Description	Reset value	Access
6:0	PDEC	Decoded P-divider coefficient value	000 0010	R/W
11:7	-	Reserved	-	-
21:12	NDEC	Decoded N-divider coefficient value	1011 0001	R/W
31:22	-	Reserved	-	-

9.6.4.5 PLL0 (for audio) fractional divider register

Table 59. PLL0AUDIO fractional divider register (PLL0AUDIO_FRAC, address 0x4005 003C) bit description

Bit	Symbol	Description	Reset value	Access
21:0	PLLFRACT_CTRL	PLL fractional divider control word	000 0000	R/W
31:22	-	Reserved	-	-

9.6.5 PLL1 registers

The PLL1 is used for the core and all peripheral blocks.

9.6.5.1 PLL1 status register

Table 60. PLL1 status register (PLL1_STAT, address 0x4005 0040) bit description

Bit	Symbol	Description	Reset value	Access
0	LOCK	PLL1 lock indicator	0	R
31:1	-	Reserved	-	-

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9.6.5.2 PLL1 control register

Table 61. PLL1_CTRL register (PLL1_CTRL, address 0x4005 0044) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		PLL1 power down	1	R/W
		0	PLL1 enabled		
		1	PLL1 powered down		
1	BYPASS		Input clock bypass control	1	R/W
		0	CCO clock sent to post-dividers. Use for normal operation.		
		1	PLL1 input clock sent to post-dividers (default).		
2	-		Reserved. Do not write one to this bit.	0	R/W
5:3	-		Reserved. Do not write one to these bits.	-	-
6	FBSEL		PLL feedback select (see Figure 20 “PLL1 block diagram”).	0	R/W
		0	CCO output is used as feedback divider input clock.		
		1	PLL output clock (clkout) is used as feedback divider input clock. Use for normal operation.		
7	DIRECT		PLL direct CCO output	0	R/W
		0	Disabled		
		1	Enabled		
9:8	PSEL[		Post-divider division ratio. The value applied is 2xP.	01	R/W
		0x0	1		
		0x1	2 (default)		
		0x2	4		
		0x3	8		
10	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
13:12	NSEL		Pre-divider division ratio	10	R/W
		0x0	1		
		0x1	2		
		0x2	3 (default)		
		0x3	4		
15:14	-		Reserved	-	-

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Table 61. PLL1_CTRL register (PLL1_CTRL, address 0x4005 0044) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
23:16	MSEL		Feedback-divider division ratio (M) 00000000 = 1 00000001 = 2 ... 11111111 = 256	11000	R/W
27:24	CLK_SEL		Clock-source selection.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	crystal oscillator		
		0x07	PLL0		
		0x08	Reserved		
		0x09	Reserved		
		0x0A	Reserved		
		0x0B	IDIVA		
		0x0C	IDIVB		
		0x0D	IDIVC		
		0x0E	IDIVD		
		0x0F	IDIVE		
31:28	-		Reserved	-	-

9.6.6 Integer divider register A

Table 62. IDIVA control register (IDIVA_CTRL, address 0x4005 0048) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Integer divider A power down	0	R/W
		0	IDIVA enabled (default)		
		1	power-down		
1	-		Reserved	-	-
3:2	IDIV		Integer divider A divider values (1/(IDIV + 1))	00	R/W
		0x0	1 (default)		
		0x1	2		
		0x2	3		
		0x3	4		
10:4	-		Reserved	-	-

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Table 62. IDIVA control register (IDIVA_CTRL, address 0x4005 0048) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-
28:24	CLK_SEL		Clock source selection. All other values are reserved.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x06	Crystal oscillator		
		0x07	PLL0 (for USB)		
		0x08	PLL0 (for audio)		
		0x09	PLL1		
31:29	-		Reserved	-	-

9.6.7 Integer divider register B, C, D

Table 63. IDIVB/C/D control registers (IDIVB_CTRL, address 0x4005 004C; IDIVC_CTRL, address 0x4005 0050; IDIVC_CTRL, address 0x4005 0054) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Integer divider power down	0	R/W
		0	IDIV enabled (default)		
		1	power-down		
1	-		Reserved	-	-
5:2	IDIV		Integer divider B, C, D divider values (1/(IDIV + 1)) 0000 = 1 (default) 0001 = 2 ... 1111 = 16	0000	R/W
10:6	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-

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Table 63. IDIVB/C/D control registers (IDIVB_CTRL, address 0x4005 004C; IDIVC_CTRL, address 0x4005 0050; IDIVC_CTRL, address 0x4005 0054) bit description

Bit	Symbol	Value	Description	Reset value	Access
28:24	CLK_SEL		Clock-source selection. All other values are reserved.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x06	Crystal oscillator		
		0x08	PLL0 (for audio)		
		0x09	PLL1		
		0x0C	IDIVA		
31:29	-		Reserved	-	-

9.6.8 Integer divider register E

Table 64. IDIVE control register (IDIVE_CTRL, address 0x4005 0058) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Integer divider power down	0	R/W
		0	IDIV enabled (default)		
		1	power-down		
1	-		Reserved	-	-
9:2	IDIV		Integer divider E divider values (1/(IDIV + 1)) 00000000 = 1 (default) 00000001 = 2 ... 111111111 = 256	00000000	R/W
10	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-

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Table 64. IDIVE control register (IDIVE_CTRL, address 0x4005 0058) bit description

Bit	Symbol	Value	Description	Reset value	Access
27:24	CLK_SEL		Clock-source selection. All other values are reserved.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x06	Crystal oscillator		
		0x08	PLL0 (for audio)		
		0x09	PLL1		
		0x0C	IDIVA		
31:28	-		Reserved	-	-

9.6.9 Output stage 0 control register

This register controls the BASE_SAFE_CLK to the watchdog oscillator. The only possible clock source for this base clock is the IRC.

Table 65. Output stage 0 control register (OUTCLK_0_CTRL, address 0x4005 005C) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Output stage power down	0	R/W
		0	Output stage enabled (default)		
		1	power-down		
10:1	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-
28:24	CLK_SEL		Clock source selection. All other values are reserved.	0x01	R/W
		0x01	IRC (default)		
31:29	-		Reserved	-	-

9.6.10 Output stage 1 control register

This register controls the BASE_USB0_CLK to the High-speed USB0. The only possible clock source for this base clock is the PLL0 (USB) output.

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Table 66. Output stage 1 control register (OUTCLK_1_CTRL, address 0x4005 0060) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Output stage power down	0	R/W
		0	Output stage enabled (default)		
		1	power-down		
10:1	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-
28:24	CLK_SEL		Clock-source selection.	0x07	R/W
		0x07	PLL0 (for USB, default)		
31:29	-		Reserved	-	-

9.6.11 Output stage 3 control register

These registers control base clocks 3 (USB1).

Table 67. Output stage 3 control register (OUTCLK_3_CTRL, address 0x4005 0068) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Output stage power down	0	R/W
		0	Output stage enabled (default)		
		1	power-down		
10:1	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-

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Table 67. Output stage 3 control register (OUTCLK_3_CTRL, address 0x4005 0068) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
28:24	CLK_SEL		Clock source selection. All other values are reserved.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x06	Crystal oscillator		
		0x07	PLL0 (for USB)		
		0x08	PLL0 (for audio)		
		0x09	PLL1		
		0x0C	IDIVA		
		0x0D	IDIVB		
		0x0E	IDIVC		
		0x0F	IDIVD		
		0x10	IDIVE		
31:29	-		Reserved	-	-

9.6.12 Output stage 4 to 19 control registers

These registers control base clocks 4 to 19.

Table 68. Output stage 4 to 19 control registers (OUTCLK_4_CTRL to OUTCLK_19_CTRL, address 0x4005 006C to 0x4005 00A8) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Output stage power down	0	R/W
		0	Output stage enabled (default)		
		1	power-down		
10:1	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-

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Table 68. Output stage 4 to 19 control registers (OUTCLK_4_CTRL to OUTCLK_19_CTRL, address 0x4005 006C to 0x4005 00A8) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
28:24	CLK_SEL		Clock source selection. All other values are reserved.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x06	Crystal oscillator		
		0x08	PLL0 (for audio)		
		0x09	PLL1		
		0x0C	IDIVA		
		0x0D	IDIVB		
		0x0E	IDIVC		
		0x0F	IDIVD		
		0x10	IDIVE		
31:29	-		Reserved	-	-

9.6.13 Output stage 20 register

This register controls the clock output to the CLKOUT pin. All clock generator outputs can be monitored through this pin.

Table 69. Output stage 20 control register (OUTCLK_20_CTRL, addresses 0x4005 00AC) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Output stage power down	0	R/W
		0	Output stage enabled (default)		
		1	power-down		
10:1	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-

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Table 69. Output stage 20 control register (OUTCLK_20_CTRL, addresses 0x4005 00AC) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
27:24	CLK_SEL		Clock-source selection.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	Crystal oscillator		
		0x07	PLL0 (for USB)		
		0x08	PLL0 (for audio)		
		0x09	PLL1		
		0x0C	IDIVA		
		0x0D	IDIVB		
		0x0E	IDIVC		
		0x0F	IDIVD		
		0x10	IDIVE		
31:28	-		Reserved	-	-

9.6.14 Output stage 25 register

This register controls the clock output to the <tbd>.

Table 70. Output stage 25 control register (OUTCLK_25_CTRL, addresses 0x4005 00C0) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Output stage power down	0	R/W
		0	Output stage enabled (default)		
		1	power-down		
10:1	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-

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Table 70. Output stage 25 control register (OUTCLK_25_CTRL, addresses 0x4005 00C0) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
27:24	CLK_SEL		Clock-source selection.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	Crystal oscillator		
		0x07	Reserved		
		0x08	PLL0 (for audio)		
		0x09	PLL1		
		0x0C	IDIVA		
		0x0D	IDIVB		
		0x0E	IDIVC		
		0x0F	IDIVD		
		0x10	IDIVE		
31:28	-		Reserved	-	-

9.6.15 Output stage 26 to 27 register

This register controls the clock output to the spare CGU outputs pins CGU_OUT0 and CGU_OUT1. All clock generator outputs can be monitored through this pin.

Table 71. Output stage 26 to 27 control register (OUTCLK_26_CTRL to OUTCLK_27_CTRL, addresses 0x4005 00C4 to 0x4005 00C8) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Output stage power down	0	R/W
		0	Output stage enabled (default)		
		1	power-down		
10:1	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-

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Table 71. Output stage 26 to 27 control register (OUTCLK_26_CTRL to OUTCLK_27_CTRL, addresses 0x4005 00C4 to 0x4005 00C8) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
27:24	CLK_SEL		Clock-source selection.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	Crystal oscillator		
		0x07	PLL0 (for USB)		
		0x08	PLL0 (for audio)		
		0x09	PLL1		
		0x0C	IDIVA		
		0x0D	IDIVB		
		0x0E	IDIVC		
		0x0F	IDIVD		
		0x10	IDIVE		
31:28	-		Reserved	-	-

9.7 Functional description

9.7.1 32 kHz oscillator

The 32 kHz oscillator output is controlled by the CREG block (see Table 31). The RTC and the Alarm timer are connected directly to the 32 kHz oscillator.

9.7.2 IRC

The IRC is a trimmed 12 MHz internal oscillator. Although it's part of the CGU, the CGU has no control over this clock source. The IRC is put into power down depending on the power saving mode.

9.7.3 Crystal oscillator

The crystal oscillator is controlled by the XTAL_OSC_CTRL register in the CGU (see Table 50).

9.7.4 PLL0 (for USB and audio)

9.7.4.1 Features

- Input frequency: 14 kHz to 150 MHz. The input from an external crystal is limited to 25 MHz.
- CCO frequency: 275 MHz to 550 MHz.

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- Output clock range: 4.3 MHz to 550 MHz.
- Programmable dividers:
  - Pre-divider N (N, 1 to 2^8)
  - Feedback-divider 2 x M (M, 1 to 2^{15})
  - Post-divider P x 2 (P, 1 to 2^5).
- Programmable bandwidth (integrating action, proportional action, high frequency pole).
- On-the-fly adjustment of the clock possible (dividers with handshake control).
- Positive edge clocking.
- Frequency limiter to avoid hang-up of the PLL.
- Lock detector.
- Power-down mode.
- Free running mode

Remark: Both PLL0 blocks are functionally identical. The PLL0 for audio applications (PLL0 for audio) supports an additional fractional divider stage (see Section 9.7.5).

9.7.4.2 PLL0 description

The block diagram of the PLL is shown in Figure 19. The clock input has to be fed to pin clkin. Pin clkout is the PLL clock output. The analog part of the PLL consists of a Phase Frequency Detector (PFD), filter and a Current Controlled Oscillator (CCO). The PFD has two inputs, a reference input from the (divided) external clock and one input from the divided CCO output clock. The PFD compares the phase/frequency of these input signals and generates a control signal if they don't match. This control signal is fed to a filter which drives the CCO.

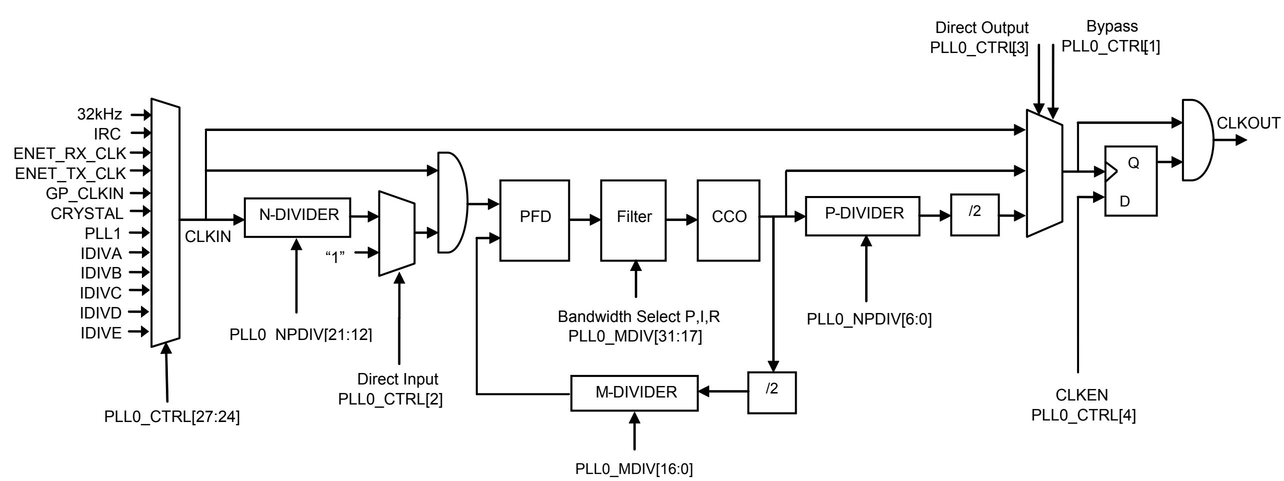


Fig 19. PLL0 block diagram

The PLL contains three programmable dividers: pre-divider (N), feedback-divider (M) and post-divider (P). The PLL contains a lock detector which measures the phase difference between the rising edges of the input and feedback clocks. Only when this difference is

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smaller than the so called “lock criterion” for more than seven consecutive input clock periods, the lock output switches from low to high. A single too large phase difference immediately resets the counter and causes the lock signal to drop (if it was high). Requiring seven phase measurements in a row to be below a certain figure ensures that the lock detector will not indicate lock until both the phase and frequency of the input and feedback clocks are very well aligned. This effectively prevents false lock indications, and thus ensures a glitch free lock signal.

To avoid frequency hang-up the PLL contains a frequency limiter. This feature is built in to prevent the CCO from running too fast, this can occur if e.g. a wrong feedback-divider (M) ratio is applied to the PLL.

9.7.4.3 Use of PLL0 operating modes

Table 72. PLL operating modes

	PLL0_Mode bit settings:					
Mode	**PD**	**CLKEN**	**BYPASS**	**DIRECTI**	**DIRECTO**	**FRM**
1: Normal	0	1	0	1/0	1/0	0
3: Power Down	1	x	x	x	x	x

9.7.4.3.1 Normal Mode

Mode 1 is the normal operating mode.

The pre- and post-divider can be selected to give:

- mode 1a: Normal operating mode without post-divider and without pre-divider
- mode 1b: Normal operating mode with post-divider and without pre-divider
- mode 1c: Normal operating mode without post-divider and with pre-divider
- mode 1d: Normal operating mode with post-divider and with pre-divider

To get at the output of the PLL (clkout) the best phase-noise and jitter performance, the highest possible reference clock (clkref) at the PFD has to be used. Therefore mode 1a and 1b are recommended, when it is possible to make the right output frequency without pre-divider.

By using the post-divider the clock at the output of the PLL (clkout) the divider ratio is always even because the divide-by-2 divider after the post-divider.

Table 73. DIRECTL and DIRECTO bit settings in HP0/1_Mode register

Mode	DIRECTI	DIRECTO
1a	1	1
1b	1	0
1c	0	1
1d	0	0

9.7.4.3.2 Mode 1a: Normal operating mode without post-divider and without pre-divider

In normal operating mode 1a the post-divider and pre-divider are bypassed. The operating frequencies are:

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$Fout = Fcco = 2 \times M \times Fin \ \Lambda \ (275\ MHz \leq Fcco \leq 550\ MHz,\ 4\ kHz \leq Fin \leq 150\ MHz)$

The feedback divider ratio is programmable:

- Feedback-divider M (M, 1 to 2^{15})

9.7.4.3.3 Mode 1b: Normal operating mode with post-divider and without pre-divider

In normal operating mode 1b the pre-divider is bypassed. The operating frequencies are:

$Fout = Fcco / (2 \times P) = (M / P) \times Fin \ \Lambda \ (275\ MHz \leq Fcco \leq 550\ MHz,\ 4\ kHz \leq Fin \leq 150\ MHz)$

The divider ratios are programmable:

- Feedback-divider M (M, 1 to 2^{15})
- Post-divider P (P, 1 to 32)

9.7.4.3.4 Mode 1c: Normal operating mode without post-divider and with pre-divider

In normal operating mode 1c the post-divider with divide-by-2 divider is bypassed. The operating frequencies are:

$Fout = Fcco = 2 \times M \times Fin / N \ \Lambda \ (275\ MHz \leq Fcco \leq 550\ MHz,\ 4\ kHz \leq Fin/N \leq 150\ MHz)$

The divider ratios are programmable:

- Pre-divider N (N, 1 to 256)
- Feedback-divider M (M, 1 to 2^{15})

9.7.4.3.5 Mode 1d: Normal operating mode with post-divider and with pre-divider

In normal operating mode 1d none of the dividers are bypassed. The operating frequencies are:

$Fout = Fcco / (2 \times P) = M \times Fin / (N \times P) \ \Lambda \ (275\ MHz \leq Fcco \leq 550\ MHz,\ 4\ kHz \leq Fin/N \leq 150\ MHz)$

The divider ratios are programmable:

- Pre-divider N (N, 1 to 256)
- Feedback-divider M (M, 1 to 2^{15})
- Post-divider P (P, 1 to 32)

9.7.4.3.6 Mode 3: Power down mode (pd)

In this mode (pd = '1'), the oscillator will be stopped, the lock output will be made low, and the internal current reference will be turned off. During pd it is also possible to load new divider ratios at the input buses (msel, psel, nsel). Power-down mode is ended by making pd low, causing the PLL to start up. The lock signal will be made high once the PLL has regained lock on the input clock.

9.7.4.4 Settings for USB0

Table 74 shows the divider settings used for configuring a certain output frequency F_{out} for USB0.

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Table 74. System PLL divider ratio settings for 12 MHz

Fout (MHz)	FCCo (MHz)	Ndec	Mdec	Pdec	SELR	SELI	SELP
<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>

9.7.4.5 Usage notes

In order to set up the PLL0, follow these steps:

1. Power down the PLL0 by setting bit 1 in the PLL0_CTRL register to 1. This step is only needed if the PLL0 is currently enabled.
2. Configure the PLL0 m, n, and p divider values in the PLL0_M and PLL0_NP registers.
3. Power up the PLL0 by setting bit 1 in the PLL0_CTRL register to 0.
4. Wait for the PLL0 to lock by monitoring the LOCK bit in the PLL0_STAT register.
5. Enable the PLL0 clock output in the PLL0_CTRL register.

9.7.5 Fractional divider for the PLL0 (for audio)

The PLL0 for audio applications (PLL0 (for audio)) includes an additional fractional divider.<tbd>

9.7.6 PLL1

9.7.6.1 Features

- 1 MHz to 50 MHz input frequency. The input from an external crystal is limited to 25 MHz.
- 9.75 MHz to 320 MHz selectable output frequency with 50% duty cycle.
- 156 MHz to 320 MHz Current Controlled Oscillator (CCO) frequency.
- Power-down mode.
- Lock detector.

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9.7.6.2 PLL1 description

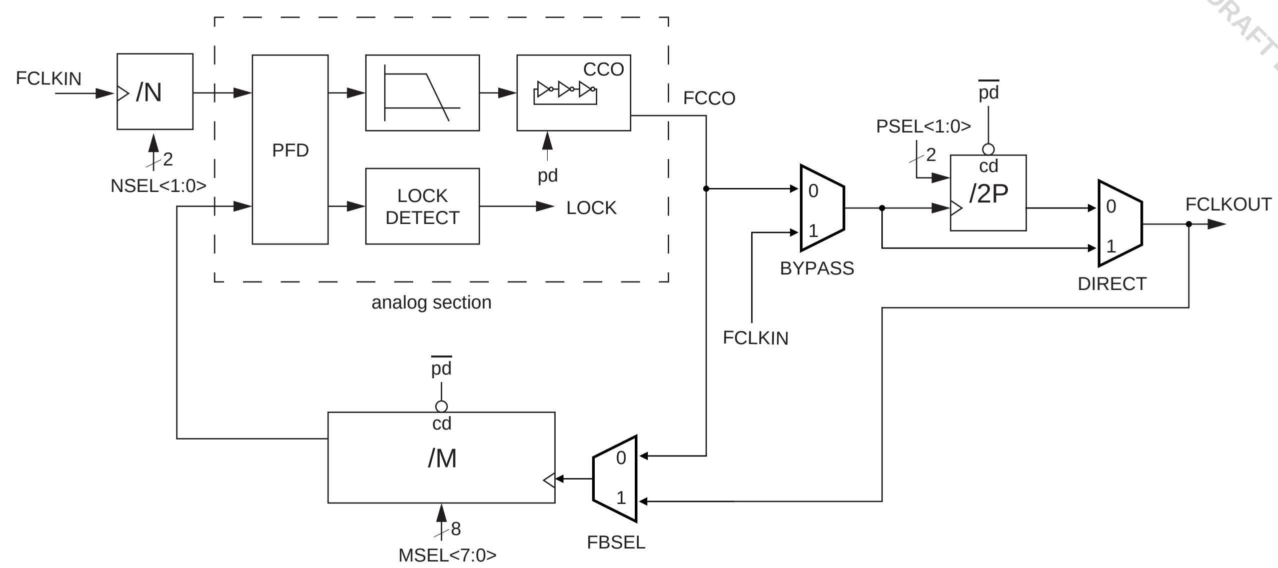


Fig 20. PLL1 block diagram

The block diagram of this PLL is shown in Figure 20. The input frequency range is 10 MHz to 25 MHz. The input clock is fed directly to the Phase-Frequency Detector (PFD). This block compares the phase and frequency of its inputs, and generates a control signal when phase and/ or frequency do not match. The loop filter filters these control signals and drives the current controlled oscillator (CCO), which generates the main clock. The CCO frequency range is 156 MHz to 320 MHz.These clocks are either divided by 2xP by the programmable post divider to create the output clocks, or are sent directly to the outputs. The main output clock is then divided by M by the programmable feedback divider to generate the feedback clock. The output signal of the phase-frequency detector is also monitored by the lock detector, to signal when the PLL has locked on to the input clock.

9.7.6.3 Lock detector

The lock detector measures the phase difference between the rising edges of the input and feedback clocks. Only when this difference is smaller than the so called “lock criterion” for more than eight consecutive input clock periods, the lock output switches from low to high. A single too large phase difference immediately resets the counter and causes the lock signal to drop (if it was high). Requiring eight phase measurements in a row to be below a certain figure ensures that the lock detector will not indicate lock until both the phase and frequency of the input and feedback clocks are very well aligned. This effectively prevents false lock indications, and thus ensures a glitch free lock signal.

9.7.6.4 Power-down control

To reduce the power consumption when the PLL clock is not needed, a Power-down mode has been incorporated. In this mode, the internal current reference will be turned off, the oscillator and the phase-frequency detector will be stopped and the dividers will enter a reset state. While in Power-down mode, the lock output will be low to indicate that

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the PLL is not in lock. When the Power-down mode is terminated, the PLL will resume its normal operation and will make the lock signal high once it has regained lock on the input clock.

9.7.6.5 Selectable feedback divider clock

To allow a trade-off to be made between functionality and power consumption, the feedback divider can be connected to either the CCO clock by setting FBSEL to 0 or to the output clock by setting FBSEL to 1. If the post-divider is used to divide down the CCO clock the current consumption of the feedback divider can be reduced by making it run on the lower output clock instead of the CCO clock, but doing so will limit the relation between output and phase detector clock frequencies to integer values.

9.7.6.6 Direct output mode

In normal operating mode (with DIRECT set to 0) the CCO clock is divided by 2, 4, 8 or 16 depending on the value of PSEL[1:0], automatically giving an output clock with a 50% duty cycle. If a higher output frequency is needed, the CCO clock can be sent directly to the output by setting DIRECT to 1. Since the CCO was designed to directly generate a clock with a 50% duty cycle, the output clock duty cycle will also be 50% in direct mode.

9.7.6.7 Divider ratio programming

Pre-divider

The pre-divider's division ratio is controlled by the NSEL[1:0] input. The division ratio between PLL's input clock and the phase detector clock is the decimal value on NSEL[1:0] plus one.

Post-divider

The division ratio of the post divider is controlled by the PSEL bits. The division ratio is two times the value of P selected by PSEL bits. This guarantees an output clock with a 50% duty cycle.

Feedback divider

The feedback divider's division ratio is controlled by the MSEL bits. The division ratio between the PLL's output clock and the input clock is the decimal value on MSEL bits plus one.

Changing the divider values

Changing the divider ratio while the PLL is running is not recommended. As there is no way to synchronize the change of the NSEL, MSEL, and PSEL values with the dividers, the risk exists that the counter will read in an undefined value, which could lead to unwanted spikes or drops in the frequency of the output clock. The recommended way of changing between divider settings is to power down the PLL, adjust the divider settings and then let the PLL start up again.

9.7.6.8 Frequency selection

The PLL frequency equations use the following parameters (also see Figure 20):

Integer mode

In this mode the post divider is enabled and the feedback divider is set to run on the PLL output clock, giving the following frequency relations:

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(1)

$$FCLKOUT = M \times \frac{FCLKIN}{N}$$

(2)

$$FCCO = 2 \times P \times FCLKOUT = 2 \times P \times M \times \frac{FCLKIN}{N}$$

Non-integer mode

In this mode the post-divider is enabled and the feedback divider is set to run directly on the CCO clock, which gives the following frequency dividers:

(3)

$$FCLKOUT = \frac{FCCO}{2 \times P} = \frac{M}{2 \times P} \times \frac{FCLKIN}{N}$$

(4)

$$FCCO = M \times \frac{FCLKIN}{N}$$

Direct mode

In this mode, the post-divider is disabled and the CCO clock is sent directly to the output, leading to the following frequency equation:

(5)

$$FCLKOUT = FCCO = M \times \frac{FCLKIN}{N}$$

Power-down mode

In this mode, the internal current reference will be turned off, the oscillator and the phase-frequency detector will be stopped and the dividers will enter a reset state. While in Power-down mode, the lock output will be low, to indicate that the PLL is not in lock. When the Power-down mode is terminated, the PLL will resume its normal operation and will make the lock signal high once it has regained lock on the input clock.

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9.8 Example CGU configurations

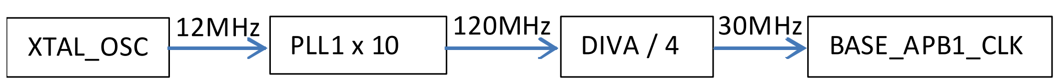
9.8.1 Programming the CGU for Deep-sleep and Power-down modes

Before the LPC18xx enters Deep-sleep or Power-down mode, the IRC must be programmed as the clock source in the control registers for all output stages (OUTCLK_0 to OUTCLK_27). In addition, the PLLs must be in Power-down mode.

When the LPC18xx wakes up from Deep-sleep or Power-down mode, the IRC is used as the clock sources for all output stages. Also see <tbd> and <tbd>.

9.8.2 Programming the CGU for using I2S at peripheral clock rate of 30 MHz

In this example the peripheral clock of the I2S interface is set to 30 MHz. The peripheral I2S clock is a branch of the BASE_APB1_CLK. Using a crystal of 12 MHz as clock source, a PLL1 multiplier of 10, and an integer divider of 4 provide the desired clock rate.



For this example, program the CGU as follows:

1. Enable the crystal oscillator in the XTAL_OSC_CTRL register (Table 50).
2. Wait for the crystal to stabilize.
3. Select the crystal oscillator as input to the PLL1 and set up the divider in the PLL1_CTRL register (see Table 61):
   – Set bits CLK_SEL in the PLL1_CTRL register to 0x6.
   – Set MSEL = 9.
   – Set NSEL = 0.
   – Set PSEL = 1.
   – Set FBSEL = 1.
   – Set BYPASS = 0, DIRECT = 0.
4. Wait for the PLL1 to lock.
5. Select the PLL1 as clock source of the integer divider A (IDIVA) in the IDIVA register and set AUTOBLOCK = 1 (see Table 61).
6. Select IDIVA as clock source of the base clock BASE_APB1_CLK and set AUTOBLOCK = 1 (see Table 62).
7. Ensure that the I2S branch clock CLK_APB1_I2S is enabled in the CCU (see Table 78).

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10.1 How to read this chapter

Remark: This chapter applies to parts LPC1850_30_20_10 rev “A”.

Remark: The VADC is not available on parts LPC1850_30_10_10 rev “A”.

Ethernet, USB0, USB1, and LCD related clocks are not available on all packages. See Table 4.

10.2 Basic configuration

The CCU1/2 are configured as follows:

- See Table 75 for clocking and power control.
- Do not reset the CCUs during normal operation.
- The output clock for the EMC clock divider (Table 84) must be configured together with bit 16 in the CREG6 register (Table 37).

Table 75. CCU clocking and power control

	Base clock	Branch clock	Maximum frequency
CCU1	BASE_M3_CLK	CLK_M3_BUS	150 MHz
CCU2	BASE_M3_CLK	CLK_M3_BUS	150 MHz

10.3 Features

The CCUs switch the clocks to individual peripherals on or off.

- Auto mode activates the AHB disable protocol before switching off the branch clock.
- Wake-up mode allows to select clocks to run automatically after a wake-up event.

10.4 General description

Each CGU base clock has several clock branches which can be turned on or off independently by the Clock Control Units CCU1 or CCU2. The branch clocks are distributed between CCU1 and CCU2.

Table 76. CCU1 branch clocks

Base clock	Branch clock	Description
BASE_APB3_CLK	CLK_APB3_BUS	APB3 bus clock.
	CLK_APB3_I2C1	Clock to the I2C1 register interface and I2C1 peripheral clock.
	CLK_APB3_DAC	Clock to the DAC register interface.

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Table 76. CCU1 branch clocks

Base clock	Branch clock	Description
	CLK_APB3_ADC0	Clock to the ADC0 register interface and ADC0 peripheral clock.
	CLK_APB3_ADC1	Clock to the ADC1 register interface and ADC1 peripheral clock.
	CLK_APB3_CAN0	Clock to the C_CAN0 register interface and C_CAN0 peripheral clock.
BASE_APB1_CLK	CLK_APB1_BUS	APB1 bus clock.
	CLK_APB1_MOTOCON	Clock to the PWM Motor control block and PWM Motocon peripheral clock.
	CLK_APB1_I2C0	Clock to the I2C0 register interface and I2C0 peripheral clock.
	CLK_APB1_I2S	Clock to the I2S0 and I2S1 register interfaces and I2S0 and I2S1 peripheral clock.
	CLK_APB1_CAN1	Clock to the C_CAN1 register interface and C_CAN1 peripheral clock.
BASE_SPIFI_CLK	CLK_SPIFI	clock for the SPIFI SCKI clock input.
BASE_M3_CLK	CLK_M3_BUS	M3 bus clock.
	CLK_M3_SPIFI	Clock to the SPIFI register interface.
	CLK_M3_GPIO	Clock to the GPIO register interface
	CLK_M3_LCD	Clock to the LCD register interface.
	CLK_M3_ETHERNET	Clock to the Ethernet register interface.
	CLK_M3_USB0	Clock to the USB0 register interface.
	CLK_M3_EMC	Clock to the External memory controller.
	CLK_M3_SDIO	Clock to the SD/MMC register interface.
	CLK_M3_DMA	Clock to the DMA register interface.
	CLK_M3_M3CORE	Clock to the Cortex-M3 core
	CLK_M3_AES	Clock to the AES register interface.
	CLK_M3_SCT	Clock to the SCT register interface.
	CLK_M3_USB1	Clock to the USB1 register interface.
	CLK_M3_EMC_DIV	Clock to the EMC with clock divider.
	CLK_M3_VADC	Clock to the VADC.
	CLK_M3_WWDT	Clock to the WWDT register interface.
	CLK_M3_UART0	Clock to the USART0 register interface.
	CLK_M3_UART1	Clock to the UART1 register interface.
	CLK_M3_SSP0	Clock to the SSP0 register interface.
	CLK_M3_TIMER0	Clock to the timer0 register interface and timer0 peripheral clock.
	CLK_M3_TIMER1	Clock to the timer1 register interface and timer1 peripheral clock.
	CLK_M3_SCU	Clock to the System control unit register interface.
	CLK_M3_CREG	Clock to the CREG register interface.
	CLK_M3_RITIMER	Clock to the RI timer register interface and RI timer peripheral clock.

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Table 76. CCU1 branch clocks

Base clock	Branch clock	Description
	CLK_M3_UART2	Clock to the UART2 register interface.
	CLK_M3_UART3	Clock to the UART3 register interface.
	CLK_M3_TIMER2	Clock to the timer2 register interface and timer2 peripheral clock.
	CLK_M3_TIMER3	Clock to the timer3 register interface and timer3 peripheral clock.
BASE_M3_CLK	CLK_M3_SSP1	
	CLK_M3_QEI	Clock to the QEI register interface and QEI peripheral clock.
BASE_USB0_CLK	CLK_USB0	USB0 peripheral clock.
BASE_USB1_CLK	CLK_USB1	USB1 peripheral clock.
-	-	Reserved.
BASE_ENET_CSR_CLK	CLK_VADC	VADC clock.

Table 77. CCU2 branch clocks

Base clock	Branch clock	Description
BASE_APLL_CLK	CLK_APLL	Audio PLL clock
BASE_UART3_CLK	CLK_APB2_UART3	USART3 peripheral clock.
BASE_UART2_CLK	CLK_APB2_UART2	USART2 peripheral clock.
BASE_UART1_CLK	CLK_APB0_UART1	UART1 peripheral clock.
BASE_UART0_CLK	CLK_APB0_UART0	USART0 peripheral clock.
BASE_SSP1_CLK	CLK_APB2_SSP1	SSP1 peripheral clock.
BASE_SSP0_CLK	CLK_APB0_SSP0	SSP0 peripheral clock.
BASE_SDIO_CLK	CLK_SDIO	SD/MMC peripheral clock.

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10.5 Register description

Table 78. Register overview: CCU1 (base address 0x4005 1000)

Name	Access	Address offset	Description	Reset value
PM	R/W	0x000	CCU1 power mode register	0x0000 0000
BASE_STAT	R	0x004	CCU1 base clocks status register	0x0000 0FFF
-	-	0x008 to 0x0FC	Reserved	-
CLK_APB3_BUS_CFG	R/W	0x100	CLK_APB3_BUS clock configuration register	0x0000 0001
CLK_APB3_BUS_STAT	R	0x104	CLK_APB3_BUS clock status register	0x0000 0001
CLK_APB3_I2C1_CFG	R/W	0x108	CLK_APB3_I2C1 configuration register	0x0000 0001
CLK_APB3_I2C1_STAT	R	0x10C	CLK_APB3_I2C1v status register	0x0000 0001
CLK_APB3_DAC_CFG	R/W	0x110	CLK_APB3_DAC configuration register	0x0000 0001
CLK_APB3_DAC_STAT	R	0x114	CLK_APB3_DAC status register	0x0000 0001
CLK_APB3_ADC0_CFG	R/W	0x118	CLK_APB3_ADC0 configuration register	0x0000 0001
CLK_APB3_ADC0_STAT	R	0x11C	CLK_APB3_ADC0 status register	0x0000 0001
CLK_APB3_ADC1_CFG	R/W	0x120	CLK_APB3_ADC1 configuration register	0x0000 0001
CLK_APB3_ADC1_STAT	R	0x124	CLK_APB3_ADC1 status register	0x0000 0001
CLK_APB3_CAN0_CFG	R/W	0x128	CLK_APB3_CAN0 configuration register	0x0000 0001
CLK_APB3_CAN0_STAT	R	0x12C	CLK_APB3_CAN0 status register	0x0000 0001
-	-	0x130 to 0x1FC	Reserved	-
CLK_APB1_BUS_CFG	R/W	0x200	CLK_APB1_BUS configuration register	0x0000 0001
CLK_APB1_BUS_STAT	R	0x204	CLK_APB1_BUS status register	0x0000 0001
CLK_APB1_MOTOCONPWM_CFG	R/W	0x208	CLK_APB1_MOTOCON configuration register	0x0000 0001
CLK_APB1_MOTOCONPWM_STAT	R	0x20C	CLK_APB1_MOTOCON status register	0x0000 0001
CLK_APB1_I2C0_CFG	R/W	0x210	CLK_APB1_I2C0 configuration register	0x0000 0001
CLK_APB1_I2C0_STAT	R	0x214	CLK_APB1_I2C0 status register	0x0000 0001
CLK_APB1_I2S_CFG	R/W	0x218	CLK_APB1_I2S configuration register	0x0000 0001
CLK_APB1_I2S_STAT	R	0x21C	CLK_APB1_I2S status register	0x0000 0001
CLK_APB1_CAN1_CFG	R/W	0x220	CLK_APB3_CAN1 configuration register	0x0000 0001
CLK_APB1_CAN1_STAT	R	0x224	CLK_APB3_CAN1 status register	0x0000 0001
-	-	0x220 to 0x2FC	Reserved	-
CLK_SPIFI_CFG	R/W	0x300	CLK_SPIFI configuration register	0x0000 0001
CLK_SPIFI_STAT	R	0x304	CLK_SPIFI status register	0x0000 0001
-	-	0x308 to 0x3FC	Reserved	-
CLK_M3_BUS_CFG	R/W	0x400	CLK_M3_BUS configuration register	0x0000 0001
CLK_M3_BUS_STAT	R	0x404	CLK_M3_BUS status register	0x0000 0001
CLK_M3_SPIFI_CFG	R/W	0x408	CLK_M3_SPIFI configuration register	0x0000 0001
CLK_M3_SPIFI_STAT	R	0x40C	CLK_M3_SPIFI status register	0x0000 0001

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Table 78. Register overview: CCU1 (base address 0x4005 1000)

Name	Access	Address offset	Description	Reset value
CLK_M3_GPIO_CFG	R/W	0x410	CLK_M3_GPIO configuration register	0x0000 0001
CLK_M3_GPIO_STAT	R	0x414	CLK_M3_GPIO status register	0x0000 0001
CLK_M3_LCD_CFG	R/W	0x418	CLK_M3_LCD configuration register	0x0000 0001
CLK_M3_LCD_STAT	R	0x41C	CLK_M3_LCD status register	0x0000 0001
CLK_M3_ETHERNET_CFG	R/W	0x420	CLK_M3_ETHERNET configuration register	0x0000 0001
CLK_M3_ETHERNET_STAT	R	0x424	CLK_M3_ETHERNET status register	0x0000 0001
CLK_M3_USB0_CFG	R/W	0x428	CLK_M3_USB0 configuration register	0x0000 0001
CLK_M3_USB0_STAT	R	0x42C	CLK_M3_USB0 status register	0x0000 0001
CLK_M3_EMC_CFG	R/W	0x430	CLK_M3_EMC configuration register	0x0000 0001
CLK_M3_EMC_STAT	R	0x434	CLK_M3_EMC status register	0x0000 0001
CLK_M3_SDIO_CFG	R/W	0x438	CLK_M3_SDIO configuration register	0x0000 0001
CLK_M3_SDIO_STAT	R	0x43C	CLK_M3_SDIO status register	0x0000 0001
CLK_M3_DMA_CFG	R/W	0x440	CLK_M3_DMA configuration register	0x0000 0001
CLK_M3_DMA_STAT	R	0x444	CLK_M3_DMA status register	0x0000 0001
CLK_M3_M3CORE_CFG	R/W	0x448	CLK_M3_M3CORE configuration register	0x0000 0001
CLK_M3_M3CORE_STAT	R	0x44C	CLK_M3_M3CORE status register	0x0000 0001
-	-	0x450 to 0x45C	Reserved	-
CLK_M3_AES_CFG	R/W	0x460	CLK_M3_AES configuration register	0x0000 0001
CLK_M3_AES_STAT	R	0x464	CLK_M3_AES status register	0x0000 0001
CLK_M3_SCT_CFG	R/W	0x468	CLK_M3_SCT configuration register	0x0000 0001
CLK_M3_SCT_STAT	R	0x46C	CLK_M3_SCT status register	0x0000 0001
CLK_M3_USB1_CFG	R/W	0x470	CLK_M3_USB1 configuration register	0x0000 0001
CLK_M3_USB1_STAT	R	0x474	CLK_M3_USB1 status register	0x0000 0001
CLK_M3_EMCDIV_CFG	R/W	0x478	CLK_M3_EMCDIV configuration register	0x0000 0001
CLK_M3_EMCDIV_STAT	R	0x47C	CLK_M3_EMCDIV status register	0x0000 0001
-	-	0x480 to 0x4FC	Reserved	-
CLK_M3_WWDT_CFG	R/W	0x500	CLK_M3_WWDT configuration register	0x0000 0001
CLK_M3_WWDT_STAT	R	0x504	CLK_M3_WWDT status register	0x0000 0001
CLK_M3_USART0_CFG	R/W	0x508	CLK_M3_UART0 configuration register	0x0000 0001
CLK_M3_USART0_STAT	R	0x50C	CLK_M3_UART0 status register	0x0000 0001
CLK_M3_UART1_CFG	R/W	0x510	CLK_M3_UART1 configuration register	0x0000 0001
CLK_M3_UART1_STAT	R	0x514	CLK_M3_UART1 status register	0x0000 0001
CLK_M3_SSP0_CFG	R/W	0x518	CLK_M3_SSP0 configuration register	0x0000 0001
CLK_M3_SSP0_STAT	R	0x51C	CLK_M3_SSP0 status register	0x0000 0001
CLK_M3_TIMER0_CFG	R/W	0x520	CLK_M3_TIMER0 configuration register	0x0000 0001
CLK_M3_TIMER0_STAT	R	0x524	CLK_M3_TIMER0 status register	0x0000 0001
CLK_M3_TIMER1_CFG	R/W	0x528	CLK_M3_TIMER1 configuration register	0x0000 0001
CLK_M3_TIMER1_STAT	R	0x52C	CLK_M3_TIMER1 status register	0x0000 0001
CLK_M3_SCU_CFG	R/W	0x530	CLK_M3_SCU configuration register	0x0000 0001

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Table 78. Register overview: CCU1 (base address 0x4005 1000)

Name	Access	Address offset	Description	Reset value
CLK_M3_SCU_STAT	R	0x534	CLK_M3_SCU status register	0x0000 0001
CLK_M3_CREG_CFG	R/W	0x538	CLK_M3_CREG configuration register	0x0000 0001
CLK_M3_CREG_STAT	R	0x53C	CLK_M3_CREG status register	0x0000 0001
-	-	0x540 to 0x5FC	Reserved	-
CLK_M3_RITIMER_CFG	R/W	0x600	CLK_M3_RITIMER configuration register	0x0000 0001
CLK_M3_RITIMER_STAT	R	0x604	CLK_M3_RITIMER status register	0x0000 0001
CLK_M3_USART2_CFG	R/W	0x608	CLK_M3_UART2 configuration register	0x0000 0001
CLK_M3_USART2_STAT	R	0x60C	CLK_M3_UART2 status register	0x0000 0001
CLK_M3_USART3_CFG	R/W	0x610	CLK_M3_UART3 configuration register	0x0000 0001
CLK_M3_USART3_STAT	R	0x614	CLK_M3_UART3 status register	0x0000 0001
CLK_M3_TIMER2_CFG	R/W	0x618	CLK_M3_TIMER2 configuration register	0x0000 0001
CLK_M3_TIMER2_STAT	R	0x61C	CLK_M3_TIMER2 status register	0x0000 0001
CLK_M3_TIMER3_CFG	R/W	0x620	CLK_M3_TIMER3 configuration register	0x0000 0001
CLK_M3_TIMER3_STAT	R	0x624	CLK_M3_TIMER3 status register	0x0000 0001
CLK_M3_SSP1_CFG	R/W	0x628	CLK_M3_SSP1 configuration register	0x0000 0001
CLK_M3_SSP1_STAT	R	0x62C	CLK_M3_SSP1 status register	0x0000 0001
CLK_M3_QEI_CFG	R/W	0x630	CLK_M3_QEI configuration register	0x0000 0001
CLK_M3_QEI_STAT	R	0x634	CLK_M3_QEI status register	0x0000 0001
-	R/W	0x638 to 0x6FC	Reserved	-
-	R/W	0x700 to 0x7FC	Reserved	-
CLK_USB0_CFG	R/W	0x800	CLK_USB0 configuration register	0x0000 0001
CLK_USB0_STAT	R	0x804	CLK_USB0 status register	0x0000 0001
-	-	0x808 to 0x8FC	Reserved	-
CLK_USB1_CFG	R/W	0x900	CLK_USB1 configuration register	0x0000 0001
CLK_USB1_STAT	R	0x904	CLK_USB1 status register	0x0000 0001
-	-	0x908 to 0x9FC	Reserved	-
CLK_VADC_CFG	R/W	0xA00	CLK_VADC configuration register	0x0000 0001
CLK_VADC_STAT	R	0xA04	CLK_VADC status register	0x0000 0001

Table 79. Register overview: CCU2 (base address 0x4005 2000)

Name	Access	Address offset	Description	Reset value
PM	R/W	0x000	CCU2 power mode register	0x0000 0000
BASE_STAT	R	0x004	CCU2 base clocks status register	0x0000 0FFF
-	-	0x008 to 0x0FC	Reserved	-
CLK_APLL_CFG	R/W	0x100	CLK_APLL configuration register	0x0000 0001

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Table 79. Register overview: CCU2 (base address 0x4005 2000)

Name	Access	Address offset	Description	Reset value
CLK_APLL_STAT	R	0x104	CLK_APLL status register	0x0000 0001
-	-	0x108 to 0x1FC	Reserved	-
CLK_APB2_USART3_CFG	R/W	0x200	CLK_APB2_UART3 configuration register	0x0000 0001
CLK_APB2_USART3_STAT	R	0x204	CLK_APB2_UART3 status register	0x0000 0001
-	-	0x208 to 0x2FC	Reserved	-
CLK_APB2_USART2_CFG	R/W	0x300	CLK_APB2_UART2 configuration register	0x0000 0001
CLK_APB2_USART2_STAT	R	0x304	CLK_APB2_UART2 status register	0x0000 0001
-	-	0x308 to 0x3FC	Reserved	-
CLK_APB0_UART1_CFG	R/W	0x400	CLK_APB0_UART1 configuration register	0x0000 0001
CLK_APB0_UART1_STAT	R	0x404	CLK_APB0_UART1 status register	0x0000 0001
-	-	0x408 to 0x4FC	Reserved	-
CLK_APB0_USART0_CFG	R/W	0x500	CLK_APB0_UART0 configuration register	0x0000 0001
CLK_APB0_USART0_STAT	R	0x504	CLK_APB0_UART0 status register	0x0000 0001
-	-	0x508 to 0x5FC	Reserved	-
CLK_APB2_SSP1_CFG	R/W	0x600	CLK_APB2_SSP1 configuration register	0x0000 0001
CLK_APB2_SSP1_STAT	R	0x604	CLK_APB2_SSP1 status register	0x0000 0001
-	-	0x608 to 0x6FC	Reserved	-
CLK_APB0_SSP0_CFG	R/W	0x700	CLK_APB0_SSP0 configuration register	0x0000 0001
CLK_APB0_SSP0_STAT	R	0x704	CLK_APB0_SSP0 status register	0x0000 0001
-	-	0x708 to 0x7FC	Reserved	-
CLK_SDIO_CFG	R/W	0x800	CLK_SDIO configuration register	0x0000 0001
CLK_SDIO_STAT	R	0x804	CLK_SDIO status register	0x0000 0001

10.5.1 Power mode register

This register contains a single bit, PD, that when set will disable all output clocks with Wake-up enabled (i.e. W = 1 in the CCU branch clock configuration registers, Section 10.5.3). Clocks disabled by writing to this register will be reactivated when a wake-up interrupt is detected or when a 0 is written into the PD bit.

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Table 80. CCU1/2 power mode register (CCU1_PM, address 0x4005 1000 and CCU2_PM, address 0x4005 2000) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Initiate power-down mode	0	R/W
		0	Normal operation.		
		1	Clocks with wake-up mode enabled (W = 1) are disabled.		
31:1	-		Reserved.	-	-

10.5.2 Base clock status register

Each bit in this register indicates if the specified base clock can be safely switched off. A logic zero indicates that all branch clocks generated from this base clock are disabled. Hence, the base clock can also be switched off. A logic one value indicates that there is still at least one branch clock running.

Remark: The base clock must be reactivated before writing to the configuration register of the branch clock.

Table 81. CCU1 base clock status register (CCU1_BASE_STAT, address 0x4005 1004) bit description

Bit	Symbol	Description	Reset value	Access
0	BASE_APB3_CLK_IND	Base clock indicator for BASE_APB3_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
1	BASE_APB1_CLK_IND	Base clock indicator for BASE_APB1_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
2	BASE_SPIFI_CLK_IND	Base clock indicator for BASE_SPIFI_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
3	BASE_M3_CLK_IND	Base clock indicator for BASE_M3_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
6:4	-	Reserved	-	-
7	BASE_USB0_CLK_IND	Base clock indicator for BASE_USB0_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
8	BASE_USB1_CLK_IND	Base clock indicator for BASE_USB1_CLK 0 = All branch clocks switched off. 1 = at least one branch clock running.	1	R
31:9	-	Reserved	-	-

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Table 82. CCU2 base clock status register (CCU2_BASE_STAT, address 0x4005 2004) bit description

Bit	Symbol	Description	Reset value	Access
0	-	Reserved.	-	-
1	BASE_UART3_CLK	Base clock indicator for BASE_UART3_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
2	BASE_UART2_CLK	Base clock indicator for BASE_UART2_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
3	BASE_UART1_CLK	Base clock indicator for BASE_UART1_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
4	BASE_UART0_CLK	Base clock indicator for BASE_UART0_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
5	BASE_SSP1_CLK	Base clock indicator for BASE_SSP1_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
6	BASE_SSP0_CLK	Base clock indicator for BASE_SSP0_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
7	-	Reserved.	-	-
31:8	-	Reserved.	-	-

10.5.3 CCU1/2 branch clock configuration registers

Each generated output clock from the CCU has a configuration register. They all follow the format as described in Table 83 and Table 85.

On the LPC18xx, all branch clocks are in Run mode after reset. Auto and wake-up features are disabled.

The clock can be configured to run in the following modes described by the bits RUN, AUTO, and WAKEUP in the CLK_XXX_CFG registers:

RUN — The WAKEUP, PD, and AUTO control bits determine the activation of the branch clock. If register bit AUTO is set the AHB disable protocol must complete before the clock is switched off. The PD bit is set in Table 80.

AUTO — Enable auto (AHB disable mechanism). The PMU initiates the AHB disable protocol before switching the clock off. This protocol ensures that all AHB transactions have been completed before turning the clock off.

WAKEUP — The branch clock is wake-up enabled when the PD bit in the Power Mode register (seeTable 80) is set and clocks which are wake-up enabled are switched off. These clocks will be switched on if a wake-up event is detected or if the PD bit is cleared. If register bit AUTO is set, the AHB disable protocol must complete before the clock is switched off.

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Remark: In order to safely disable any of the branch clocks, use two separate writes to the CLK_XXX_CFG register: first set the AUTO bit, and then on the next write, disable the clock by setting the RUN bit to zero.

Table 83. CCU1 branch clock configuration register (CLK_XXX_CFG, addresses 0x4005 1100, 0x4005 1104,..., 0x4005 1A00) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	RUN		Run enable	1	R/W
		0	Clock is disabled.		
		1	Clock is enabled.		
1	AUTO		Auto (AHB disable mechanism) enable	0	R/W
		0	Auto is disabled.		
		1	Auto is enabled.		
2	WAKEUP		Wake-up mechanism enable	0	R/W
		0	Wake-up is disabled.		
		1	Wake-up is enabled.		
31:3	-		Reserved	-	-

Remark: The output clock for the EMC clock divider (Table 84) must be configured together with bit 16 in the CREG6 register (Table 37).

Table 84. CCU1 branch clock configuration register (CLK_EMCDIV_CFG, addresses 0x4005 1478) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	RUN		Run enable	1	R/W
		0	Clock is disabled.		
		1	Clock is enabled.		
1	AUTO		Auto (AHB disable mechanism) enable	0	R/W
		0	Auto is disabled.		
		1	Auto is enabled.		
2	WAKEUP		Wake-up mechanism enable	0	R/W
		0	Wake-up is disabled.		
		1	Wake-up is enabled.		
3	-		Reserved	-	-
4	-		Reserved	-	-
7:5	DIV		Clock divider value	0	R/W
		0x0	No division (divide by 1).		
		0x1	Divide by 2.		
		0x2	Reserved		
		0x3	Reserved		
		0x4	Reserved		
31:8	-		Reserved	-	-

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Table 85. CCU2 branch clock configuration register (CLK_XXX_CFG, addresses 0x4005 2100, 0x4005 2200,..., 0x4005 2800) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	RUN		Run enable	1	R/W
		0	Clock is disabled.		
		1	Clock is enabled.		
1	AUTO		Auto (AHB disable mechanism) enable	0	R/W
		0	Auto is disabled.		
		1	Auto is enabled.		
2	WAKEUP		Wake-up mechanism enable	0	R/W
		0	Wake-up is disabled.		
		1	Wake-up is enabled.		
31:3	-		Reserved	-	-

10.5.4 CCU1/2 branch clock status registers

Like the Configuration Register, each generated output clock from the CCU has a status register. When the configuration register of an output clock is written into, the value of the actual hardware signals may not be updated immediately because of the Auto or Wake-up mechanism. The Status Register shows the current value of these signals. All output clock Status Registers follow the format as described in Table 86 and Table 87.

Table 86. CCU1 branch clock status register (CLK_XXX_STAT, addresses 0x4005 1104, 0x4005 110C,..., 0x4005 1A04) bit description

Bit	Symbol	Description	Reset value	Access
0	RUN	Run enable status 0 = clock is disabled. 1 = clock is enabled.	1	R
1	AUTO	Auto (AHB disable mechanism) enable status 0 = Auto is disabled. 1 = Auto is enabled.	0	R
2	WAKEUP	Wake-up mechanism enable status 0 = Wake-up is disabled. 1 = Wake-up is enabled.	0	R
31:3	-	Reserved	-	-

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Table 87. CCU2 branch clock status register (CLK_XXX_STAT, addresses 0x4005 2104, 0x4005 2204,..., 0x4005 2804) bit description

Bit	Symbol	Description	Reset value	Access
0	RUN	Run enable status 0 = clock is disabled 1 = clock is enabled	1	R
1	AUTO	Auto (AHB disable mechanism) enable status 0 = Auto is disabled 1 = Auto is enabled	0	R
2	WAKEUP	Wake-up mechanism enable status 0 = Wake-up is disabled 1 = Wake-up is enabled	0	R
31:3	-	Reserved	-	-

10.6 Functional description

<tbd>

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11.1 How to read this chapter

The C_CAN1 reset (#54) is available on parts LPC1850_30_20_10 Rev ‘A’ only.

11.2 Basic configuration

Table 88. RGU clocking and power control

	Base clock	Branch clock	Maximum frequency
RGU	BASE_M3_CLK	CLK_M3_BUS	150 MHz
RGU delay clocks	BASE_SAFE_CLK	-	12 MHz

The RGU is reset by a BUS_RST (reset #8).

Remark: Support for the ARM Cortex-M3 SYSRESETREQ is not implemented on the LPC18xx.

11.3 General description

The RGU allows generation of independent reset signals for various blocks and peripherals on the LPC18xx. Each reset signal is asserted by a reset generator with one output (the reset signal) and one or more inputs, which link the reset generators together and create a reset hierarchy.

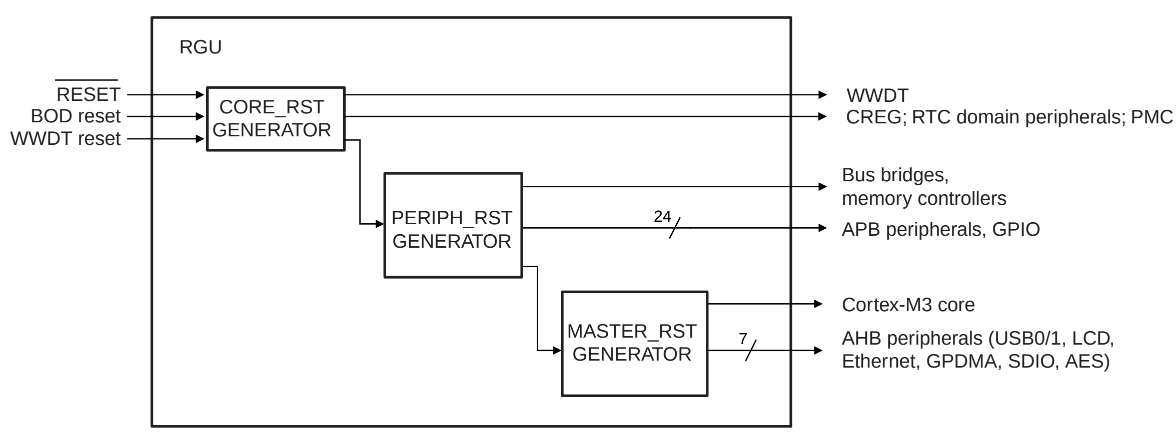


Fig 21. RGU Block diagram

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Table 89. Reset output configuration

Reset output generator	Reset output #	Reset source	Parts of the device reset when activated
CORE_RST	0	external reset, BOD reset, WWDT time-out reset	Entire chip including peripherals in the battery-powered domain: CGU, power management controller, general purpose registers, alarm timer, parts of the CREG block, and RTC.
PERIPH_RST	1	CORE_RST	All peripherals with reset source PERIPH_RST and MASTER_RST
MASTER_RST	2	PERIPH_RST	All peripherals with reset source MASTER_RST
Reserved	3	-	-
WWDT_RST	4	CORE_RST	WWDT. No software reset.
CREG_RST	5	CORE_RST	Configuration register block, Event router, backup registers, RTC, alarm timer. No software reset.
Reserved	6 - 7	-	-
BUS_RST	8	PERIPH_RST	Buses; RGU, CCU, and CGU registers; memory controllers; bus bridges. Do not use during normal operation.
SCU_RST	9	PERIPH_RST	System control unit
Reserved	10 - 12	-	-
M3_RST	13	MASTER_RST	Cortex-M3 system reset
Reserved	14	-	-
Reserved	15	-	-
LCD_RST	16	MASTER_RST	LCD controller reset
USB0_RST	17	MASTER_RST	USB0 reset
USB1_RST	18	MASTER_RST	USB1 reset
DMA_RST	19	MASTER_RST	DMA reset
SDIO_RST	20	MASTER_RST	SDIO reset
EMC_RST	21	MASTER_RST	External memory controller reset
ETHERNET_RST	22	MASTER_RST	Ethernet reset
AES_RST	23	MASTER_RST	AES reset
Reserved	24 - 27	-	-
GPIO_RST	28	PERIPH_RST	GPIO reset
Reserved	29 - 31	-	-
TIMER0_RST	32	PERIPH_RST	Timer0 reset
TIMER1_RST	33	PERIPH_RST	Timer1 reset
TIMER2_RST	34	PERIPH_RST	Timer2 reset
TIMER3_RST	35	PERIPH_RST	Timer3 reset
RITIMER_RST	36	PERIPH_RST	Repetitive Interrupt timer reset
SCT_RST	37	PERIPH_RST	State Configurable Timer reset
MOTOCONPWM_RST	38	PERIPH_RST	Motor control PWM reset
QEI_RST	39	PERIPH_RST	QEI reset

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Table 89. Reset output configuration *…continued*

Reset output generator	Reset output #	Reset source	Parts of the device reset when activated
ADC0_RST	40	PERIPH_RST	ADC0 reset (ADC register interface and analog block)
ADC1_RST	41	PERIPH_RST	ADC1 reset (ADC register interface and analog block)
DAC_RST	42	PERIPH_RST	DAC reset (DAC register interface and analog block)
Reserved	43	-	-
UART0_RST	44	PERIPH_RST	USART0 reset
UART1_RST	45	PERIPH_RST	UART1 reset
UART2_RST	46	PERIPH_RST	USART2 reset
UART3_RST	47	PERIPH_RST	USART3 reset
I2C0_RST	48	PERIPH_RST	I2C0 reset
I2C1_RST	49	PERIPH_RST	I2C1 reset
SSP0_RST	50	PERIPH_RST	SSP0 reset
SSP1_RST	51	PERIPH_RST	SSP1 reset
I2S_RST	52	PERIPH_RST	I2S0 and I2S1 reset
SPIFI_RST	53	PERIPH_RST	SPIFI reset
CAN1_RST	54	PERIPH_RST	C_CAN1 reset
CAN0_RST	55	PERIPH_RST	C_CAN0 reset
Reserved	56	-	-
Reserved	57	-	-
Reserved	59 - 63	-	-

The RGU also monitors the reset cause for each reset output. The reset cause can be retrieved with two levels of granularity.

The first level is monitored by the RESET_STATUS0 to 3 registers and indicates one of the following reset causes (see Table 94 to Table 97):

- No reset has taken place.
- Reset generated by software (using the registers RESET_CTRL0 and RESET_CTRL1).
- Reset generated by any of the reset sources.

The second level of granularity is monitored by one individual register for each reset output (RESET_EXT_STATUSn) in which the detailed reset cause is indicated, that is whether or not any of the possible inputs to each reset generator are activated. The following lists all inputs, but note that only a subset of inputs are connected to each reset generator:

- External reset (from external reset pin)
- CORE_RST output
- PERIPH_RST output
- MASTER_RST output

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- BOD reset signal
- WWDT time-out signal

11.3.1 Reset hierarchy

The hierarchy is as follows (see Table 90):

1. External reset, BOD reset signal, WWDT time-out, and reset signal from the PMU
2. CORE_RST (inputs are the external reset pin, BOD reset, and the WWDT time-out reset); resets the whole chip including the WWDT and the configuration register block CREG.
3. PERIPH_RST (input is the CORE_RST); resets all APB peripherals and the ARM core, but not the WWDT and the CREG block.
4. MASTER_RST (input is the PERIPH_RST); resets the ARM Cortex-M3 core and the AHB peripherals (DMA, USB0/1, LCD, SDIO, EMC, AES).

Table 90. Reset priority

Priority	Reset input	WWDT	CREG/ RTC/ Event router	ABP peripherals	Cortex-M3 Core	AHB peripherals	RGU	EMC	GPIO	SRAM controllers
1	External reset pin, BOD, WWDT	yes	yes	yes	yes	yes	yes	yes	yes	yes
2	CORE_RST	yes	yes	yes	yes	yes	yes	yes	yes	yes
3	PERIPH_RST	no	no	yes	yes	yes	yes	yes	yes	yes
4	MASTER_RST	no	no	no	yes	yes	yes	yes	yes	yes

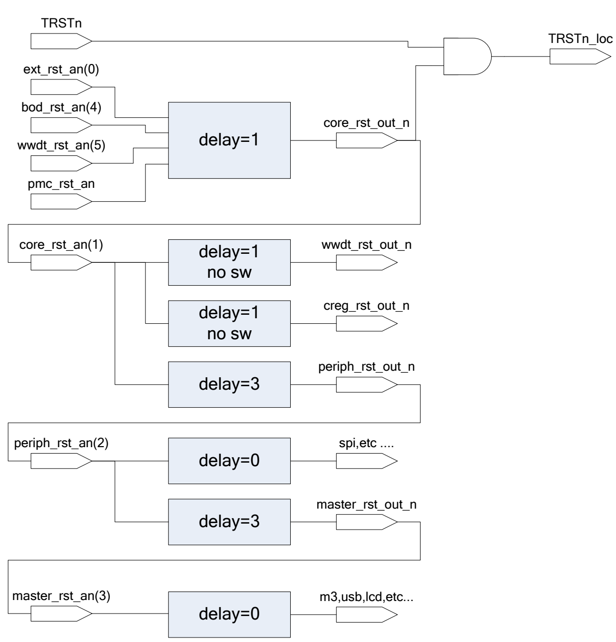


Fig 22. RGU Reset structure

11.4 Register overview

Table 91. Register overview: RGU (base address: 0x4005 3000)

Name	Access	Address offset	Description	Reset value	Reference
RESET_CTRL0	W	0x100	Reset control register 0	-	see Table 92
RESET_CTRL1	W	0x104	Reset control register 1	-	see Table 93
RESET_STATUS0	R/W	0x110	Reset status register 0	0x5555 0050	see Table 94
RESET_STATUS1	R/W	0x114	Reset status register 1	0x5555 5555	see Table 95
RESET_STATUS2	R/W	0x118	Reset status register 2	0x5555 5555	see Table 96
RESET_STATUS3	R/W	0x11C	Reset status register 3	0x5555 5555	see Table 97
RESET_ACTIVE_STATUS0	R	0x150	Reset active status register 0	0x0	see Table 98
RESET_ACTIVE_STATUS1	R	0x154	Reset active status register 1	0x0	see Table 99
RESET_EXT_STAT0	R/W	0x400	Reset external status register 0 for CORE_RST	0x0	see Table 100
RESET_EXT_STAT1	R/W	0x404	Reset external status register 1 for PERIPH_RST	0x0	see Table 101
RESET_EXT_STAT2	R/W	0x408	Reset external status register 2 for MASTER_RST	0x0	see Table 102
RESET_EXT_STAT3	-	0x40C	Reserved	-	
RESET_EXT_STAT4	R/W	0x410	Reset external status register 4 for WWDT_RST	0x0	see Table 103
RESET_EXT_STAT5	R/W	0x414	Reset external status register 5 for CREG_RST	0x0	see Table 104
RESET_EXT_STAT6	-	0x418	Reserved	-	-
RESET_EXT_STAT7	-	0x41C	Reserved	-	-
RESET_EXT_STAT8	R/W	0x420	Reset external status register 8 for BUS_RST	0x0	see Table 105
RESET_EXT_STAT9	R/W	0x424	Reset external status register 9 for SCU_RST	0x0	see Table 105
RESET_EXT_STAT10	-	0x428	Reserved	-	-
RESET_EXT_STAT11	-	0x42C	Reserved	-	-
RESET_EXT_STAT12	-	0x430	Reserved	-	-
RESET_EXT_STAT13	R/W	0x434	Reset external status register 13 for M3_RST	0x0	see Table 106
RESET_EXT_STAT14	-	0x438	Reserved	-	-
RESET_EXT_STAT15	-	0x43C	Reserved	-	-
RESET_EXT_STAT16	R/W	0x440	Reset external status register 16 for LCD_RST	0x0	see Table 106
RESET_EXT_STAT17	R/W	0x444	Reset external status register 17 for USB0_RST	0x0	see Table 106
RESET_EXT_STAT18	R/W	0x448	Reset external status register 18 for USB1_RST	0x0	see Table 106
RESET_EXT_STAT19	R/W	0x44C	Reset external status register 19 for DMA_RST	0x0	see Table 106

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Table 91. Register overview: RGU (base address: 0x4005 3000) *…continued*

Name	Access	Address offset	Description	Reset value	Reference
RESET_EXT_STAT20	R/W	0x450	Reset external status register 20 for SDIO_RST	0x0	see Table 106
RESET_EXT_STAT21	R/W	0x454	Reset external status register 21 for EMC_RST	0x0	see Table 106
RESET_EXT_STAT22	R/W	0x458	Reset external status register 22 for ETHERNET_RST	0x0	see Table 106
RESET_EXT_STAT23	R/W	0x45C	Reset external status register 23 for AES_RST	0x0	see Table 106
RESET_EXT_STAT24	-	0x460	Reserved	-	-
RESET_EXT_STAT25	-	0x464	Reserved	-	-
RESET_EXT_STAT26	-	0x468	Reserved	-	-
RESET_EXT_STAT27	-	0x46C	Reserved	-	-
RESET_EXT_STAT28	R/W	0x470	Reset external status register 28 for GPIO_RST	0x0	see Table 105
RESET_EXT_STAT29	-	0x474	Reserved	-	-
RESET_EXT_STAT30	-	0x478	Reserved	-	-
RESET_EXT_STAT31	-	0x47C	Reserved	-	-
RESET_EXT_STAT32	R/W	0x480	Reset external status register 32 for TIMER0_RST	0x0	see Table 105
RESET_EXT_STAT33	R/W	0x484	Reset external status register 33 for TIMER1_RST	0x0	see Table 105
RESET_EXT_STAT34	R/W	0x488	Reset external status register 34 for TIMER2_RST	0x0	see Table 105
RESET_EXT_STAT35	R/W	0x48C	Reset external status register 35 for TIMER3_RST	0x0	see Table 105
RESET_EXT_STAT36	R/W	0x490	Reset external status register 36 for RITIMER_RST	0x0	see Table 105
RESET_EXT_STAT37	R/W	0x494	Reset external status register 37 for SCT_RST	0x0	see Table 105
RESET_EXT_STAT38	R/W	0x498	Reset external status register 38 for MOTOCONPWM_RST	0x0	see Table 105
RESET_EXT_STAT39	R/W	0x49C	Reset external status register 39 for QEI_RST	0x0	see Table 105
RESET_EXT_STAT40	R/W	0x4A0	Reset external status register 40 for ADC0_RST	0x0	see Table 105
RESET_EXT_STAT41	R/W	0x4A4	Reset external status register 41 for ADC1_RST	0x0	see Table 105
RESET_EXT_STAT42	R/W	0x4A8	Reset external status register 42 for DAC_RST	0x0	see Table 105
RESET_EXT_STAT43	-	0x4AC	Reserved	0x0	-
RESET_EXT_STAT44	R/W	0x4B0	Reset external status register 44 for UART0_RST	0x0	see Table 105
RESET_EXT_STAT45	R/W	0x4B4	Reset external status register 45 for UART1_RST	0x0	see Table 105

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Table 91. Register overview: RGU (base address: 0x4005 3000) *…continued*

Name	Access	Address offset	Description	Reset value	Reference
RESET_EXT_STAT46	R/W	0x4B8	Reset external status register 46 for UART2_RST	0x0	see Table 105
RESET_EXT_STAT47	R/W	0x4BC	Reset external status register 47 for UART3_RST	0x0	see Table 105
RESET_EXT_STAT48	R/W	0x4C0	Reset external status register 48 for I2C0_RST	0x0	see Table 105
RESET_EXT_STAT49	R/W	0x4C4	Reset external status register 49 for I2C1_RST	0x0	see Table 105
RESET_EXT_STAT50	R/W	0x4C8	Reset external status register 50 for SSP0_RST	0x0	see Table 105
RESET_EXT_STAT51	R/W	0x4CC	Reset external status register 51 for SSP1_RST	0x0	see Table 105
RESET_EXT_STAT52	R/W	0x4D0	Reset external status register 52 for I2S_RST	0x0	see Table 105
RESET_EXT_STAT53	R/W	0x4D4	Reset external status register 53 for SPIFI_RST	0x0	see Table 105
RESET_EXT_STAT54	R/W	0x4D8	Reset external status register 54 for CAN1_RST	0x0	see Table 105
RESET_EXT_STAT55	R/W	0x4DC	Reset external status register 55 for CAN0_RST	0x0	see Table 105
RESET_EXT_STAT56	-	0x4E0	Reserved	-	-
RESET_EXT_STAT57	-	0x4E4	Reserved	-	-
RESET_EXT_STAT58	-	0x4E8	Reserved	-	-
RESET_EXT_STAT59	-	0x4EC	Reserved	-	-
RESET_EXT_STAT60	-	0x4F0	Reserved	-	-
RESET_EXT_STAT61	-	0x4F4	Reserved	-	-
RESET_EXT_STAT62	-	0x4F8	Reserved	-	-
RESET_EXT_STAT63	-	0x4FC	Reserved	-	-

11.4.1 RGU reset control register

The RGU reset control register allows software to activate and clear individual reset outputs. Each bit corresponds to an individual reset output, and writing a one activates that output. The reset output is automatically de-activated after a fixed delay period. If the reset output has a manual release, it stays activated once pulled low until a 0 is written to the appropriate bit in this register. This applies whether the reset activation came from the Reset Control Register or any other source

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Table 92. Reset control register 0 (RESET_CTRL0, address 0x4005 3100) bit description

Bit	Symbol	Description	Reset value	Access
0	CORE_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
1	PERIPH_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after three clock cycles.	0	W
2	MASTER_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after three clock cycles.	0	W
3	-	Reserved	0	-
4	WWDT_RST	Writing a one to this bit has no effect.	0	-
5	CREG_RST	Writing a one to this bit has no effect.	0	-
6	-	Reserved	0	-
7	-	Reserved	0	-
8	BUS_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle. Do not use during normal operation	0	W
9	SCU_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
10	PINMUX_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
11	-	Reserved	0	-
11	-	Reserved	0	-
13	M3_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
14	-	Reserved	0	-
15	-	Reserved	0	-
16	LCD_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
17	USB0_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
18	USB1_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
19	DMA_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
20	SDIO_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
21	EMC_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
22	ETHERNET_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
23	AES_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
24	-	Reserved	-	-
25	-	Reserved	-	-
26	-	Reserved	-	-
27	-	Reserved	-	-

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Table 92. Reset control register 0 (RESET_CTRL0, address 0x4005 3100) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
28	GPIO_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
29	-	Reserved	-	-
30	-	Reserved	-	-
31	-	Reserved	-	-

Table 93. Reset control register 1 (RESET_CTRL1, address 0x4005 3104) bit description

Bit	Symbol	Description	Reset value	Access
0	TIMER0_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
1	TIMER1_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
2	TIMER2_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
3	TIMER3_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
4	OSTIMER_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
5	SCT_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
6	MOTOCONPWM_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
7	QEI_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
8	ADC0_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
9	ADC1_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
10	DAC_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
11	-	Reserved	-	-
12	UART0_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
13	UART1_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
14	UART2_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
15	UART3_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
16	I2C0_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
17	I2C1_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W

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Table 93. Reset control register 1 (RESET_CTRL1, address 0x4005 3104) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
18	SSP0_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
19	SSP1_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
20	I2S_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
21	SPIFI_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
22	CAN1_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
23	CAN0_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
24	-	Reserved	-	-
25	-	Reserved	-	-
26	-	Reserved	-	-
27	-	Reserved	-	-
28	-	Reserved	-	-
29	-	Reserved	-	-
30	-	Reserved	-	-
31	-	Reserved	-	-

11.4.2 RGU reset status register

The reset status register shows which source (if any) caused the last reset activation per individual reset output of the RGU. When one (or more) inputs of the RGU caused the Reset Output to go active (indicated by value 01), the corresponding RESET_EXT_STATUS register can be read, see Section 11.4.4.

The RESET_STATUS registers are cleared by writing 0 to each of the status bits.

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Table 94. Reset status register 0 (RESET_STATUS0, address 0x4005 3110) bit description

Bit	Symbol	Description	Reset value	Access
1:0	CORE_RST	Status of the CORE_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	00	R/W
3:2	PERIPH_RST	Status of the PERIPH_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	00	R/W
5:4	MASTER_RST	Status of the MASTER_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
7:6	-	Reserved	01	
9:8	WWDT_RST	Status of the WWDT_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reserved	01	R/W
11:10	CREG_RST	Status of the CREG_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reserved	01	R/W
13:12	-	Reserved	01	-
15:14	-	Reserved	01	-
17:16	BUS_RST	Status of the BUS_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
19:18	SCU_RST	Status of the SCU_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
21:20	-	Reserved	01	-
23:22	-	Reserved	01	-
25:24	-	Reserved	01	-

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Table 94. Reset status register 0 (RESET_STATUS0, address 0x4005 3110) bit description

Bit	Symbol	Description	Reset value	Access
27:26	M3_RST	Status of the M3_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
29:28	-	Reserved	01	-
31:30	-	Reserved	01	-

Table 95. Reset status register 1 (RESET_STATUS1, address 0x4005 3114) bit description

Bit	Symbol	Description	Reset value	Access
1:0	LCD_RST	Status of the LCD_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
3:2	USB0_RST	Status of the USB0_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
5:4	USB1_RST	Status of the USB1_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
7:6	DMA_RST	Status of the DMA_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
9:8	SDIO_RST	Status of the SDIO_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
11:10	EMC_RST	Status of the EMC_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W

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Table 95. Reset status register 1 (RESET_STATUS1, address 0x4005 3114) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
13:12	ETHERNET_RST	Status of the ETHERNET_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
15:14	AES_RST	Status of the AES_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
17:16	-	Reserved	01	-
19:18	-	Reserved	01	-
21:20	-	Reserved	01	-
23:22	-	Reserved	01	-
25:24	GPIO_RST	Status of the GPIO_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
27:26	-	Reserved	01	-
29:28	-	Reserved	01	-
31:30	-	Reserved	01	-

Table 96. Reset status register 2 (RESET_STATUS2, address 0x4005 3118) bit description

Bit	Symbol	Description	Reset value	Access
1:0	TIMER0_RST	Status of the TIMER0_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
3:2	TIMER1_RST	Status of the TIMER1_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
5:4	TIMER2_RST	Status of the TIMER2_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W

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Table 96. Reset status register 2 (RESET_STATUS2, address 0x4005 3118) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
7:6	TIMER3_RST	Status of the TIMER3_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
9:8	RITIMER_RST	Status of the OSTIMER_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
11:10	SCT_RST	Status of the SCT_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
13:12	MOTOCONPWM_RST	Status of the MOTOCONPWM_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
15:14	QEI_RST	Status of the QEI_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
17:16	ADC0_RST	Status of the ADC0_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
19:18	ADC1_RST	Status of the ADC1_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
21:20	DAC_RST	Status of the DAC_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
23:22	-	Reserved	01	R/W

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Table 96. Reset status register 2 (RESET_STATUS2, address 0x4005 3118) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
25:24	UART0_RST	Status of the UART0_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
27:26	UART1_RST	Status of the UART1_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
29:28	UART2_RST	Status of the UART2_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
31:30	UART3_RST	Status of the UART3_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W

Table 97. Reset status register 3 (RESET_STATUS3, address 0x4005 311C) bit description

Bit	Symbol	Description	Reset value	Access
1:0	I2C0_RST	Status of the I2C0_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
3:2	I2C1_RST	Status of the I2C1_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
5:4	SSP0_RST	Status of the SSP0_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W

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Table 97. Reset status register 3 (RESET_STATUS3, address 0x4005 311C) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
7:6	SSP1_RST	Status of the SSP1_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
9:8	I2S_RST	Status of the I2S_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
11:10	SPIFI_RST	Status of the SPIFI_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
13:12	CAN1_RST	Status of the CAN1_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
15:14	CAN0_RST	Status of the CAN0_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
17:16	-	Reserved	01	-
19:18	-	Reserved	01	-
21:20	-	Reserved	01	-
23:22	-	Reserved	01	-
25:24	-	Reserved	01	-
27:26	-	Reserved	01	-
29:28	-	Reserved	01	-
31:30	-	Reserved	01	-

11.4.3 RGU reset active status register

The reset active status register shows the current value of the reset outputs of the RGU. Note that the resets are active LOW.

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Table 98. Reset active status register 0 (RESET_ACTIVE_STATUS0, address 0x4005 3150) bit description

Bit	Symbol	Description	Reset value	Access
0	CORE_RST	Current status of the CORE_RST 0 = Reset asserted 1 = No reset	0	R
1	PERIPH_RST	Current status of the PERIPH_RST 0 = Reset asserted 1 = No reset	0	R
2	MASTER_RST	Current status of the MASTER_RST 0 = Reset asserted 1 = No reset	0	R
3	-	Reserved	0	
4	WWDT_RST	Current status of the WWDT_RS 0 = Reset asserted 1 = No reset	0	R
5	CREG_RST	Current status of the CREG_RST 0 = Reset asserted 1 = No reset	0	R
6	-	Reserved	0	
7	-	Reserved	0	
8	BUS_RST	Current status of the BUS_RST 0 = Reset asserted 1 = No reset	0	R
9	SCU_RST	Current status of the SCU_RST 0 = Reset asserted 1 = No reset	0	R
10	PINMUX_RST	Current status of the PINMUX_RST 0 = Reset asserted 1 = No reset	0	R
11	-	Reserved	0	-
12	-	Reserved	0	-
13	M3_RST	Current status of the M3_RST 0 = Reset asserted 1 = No reset	0	R
14	-	Reserved	0	
15	-	Reserved	0	
16	LCD_RST	Current status of the LCD_RST 0 = Reset asserted 1 = No reset	0	R
17	USB0_RST	Current status of the USB0_RST 0 = Reset asserted 1 = No reset	0	R

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Table 98. Reset active status register 0 (RESET_ACTIVE_STATUS0, address 0x4005 3150) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
18	USB1_RST	Current status of the USB1_RST 0 = Reset asserted 1 = No reset	0	R
19	DMA_RST	Current status of the DMA_RST 0 = Reset asserted 1 = No reset	0	R
20	SDIO_RST	Current status of the SDIO_RST 0 = Reset asserted 1 = No reset	0	R
21	EMC_RST	Current status of the EMC_RST 0 = Reset asserted 1 = No reset	0	R
22	ETHERNET_RST	Current status of the ETHERNET_RST 0 = Reset asserted 1 = No reset	0	R
23	AES_RST	Current status of the AES_RST 0 = Reset asserted 1 = No reset	0	R
24	-	Reserved	-	-
25	-	Reserved	-	-
26	-	Reserved	-	-
27	-	Reserved	-	-
28	GPIO_RST	Current status of the GPIO_RST 0 = Reset asserted 1 = No reset	0	R
29	-	Reserved	-	-
30	-	Reserved	-	-
31	-	Reserved	-	-

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Table 99. Reset active status register 1 (RESET_ACTIVE_STATUS1, address 0x4005 3154) bit description

Bit	Symbol	Description	Reset value	Access
0	TIMER0_RST	Current status of the TIMER0_RST 0 = Reset asserted 1 = No reset	0	R
1	TIMER1_RST	Current status of the TIMER1_RST 0 = Reset asserted 1 = No reset	0	R
2	TIMER2_RST	Current status of the TIMER2_RST 0 = Reset asserted 1 = No reset	0	R
3	TIMER3_RST	Current status of the TIMER3_RST 0 = Reset asserted 1 = No reset	0	R
4	RITIMER_RST	Current status of the OSTIMER_RST 0 = Reset asserted 1 = No reset	0	R
5	SCT_RST	Current status of the SCT_RST 0 = Reset asserted 1 = No reset	0	R
6	MOTOCONPWM_RST	Current status of the MOTOCONPWM_RST 0 = Reset asserted 1 = No reset	0	R
7	QEI_RST	Current status of the QEI_RST 0 = Reset asserted 1 = No reset	0	R
8	ADC0_RST	Current status of the ADC0_RST 0 = Reset asserted 1 = No reset	0	R
9	ADC1_RST	Current status of the ADC1_RST 0 = Reset asserted 1 = No reset	0	R
10	DAC_RST	Current status of the DAC_RST 0 = Reset asserted 1 = No reset	0	R
11	-		-	-
12	UART0_RST	Current status of the UART0_RST 0 = Reset asserted 1 = No reset	0	R
13	UART1_RST	Current status of the UART1_RST 0 = Reset asserted 1 = No reset	0	R

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Table 99. Reset active status register 1 (RESET_ACTIVE_STATUS1, address 0x4005 3154) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
14	UART2_RST	Current status of the UART2_RST 0 = Reset asserted 1 = No reset	0	R
15	UART3_RST	Current status of the UART3_RST 0 = Reset asserted 1 = No reset	0	R
16	I2C0_RST	Current status of the I2C0_RST 0 = Reset asserted 1 = No reset	0	R
17	I2C1_RST	Current status of the I2C1_RST 0 = Reset asserted 1 = No reset	0	R
18	SSP0_RST	Current status of the SSP0_RST 0 = Reset asserted 1 = No reset	0	R
19	SSP1_RST	Current status of the SSP1_RST 0 = Reset asserted 1 = No reset	0	R
20	I2S_RST	Current status of the I2S_RST 0 = Reset asserted 1 = No reset	0	R
21	SPIFI_RST	Current status of the SPIFI_RST 0 = Reset asserted 1 = No reset	0	R
22	CAN1_RST	Current status of the CAN1_RST 0 = Reset asserted 1 = No reset	0	R
23	CAN0_RST	Current status of the CAN0_RST 0 = Reset asserted 1 = No reset	0	R
24	-	Reserved.	-	-
24	-	Reserved.	-	-
26	-	Reserved.	-	-
27	-	Reserved.	-	-
28	-	Reserved.	-	-
29	-	Reserved.	-	-
30	-	Reserved.	-	-
31	-	Reserved.	-	-

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11.4.4 Reset external status registers

The external status registers indicate which input to the reset generator caused the reset output to go active. Any bit set to 1 in the Reset external status register should be cleared to 0 after a read operation to allow the detection of the next reset.

All reset generators except the WWDT time-out reset, the BOD reset, the reset signal from the PMU, and the software reset, which have no inputs, have an associated external status register. The CORE_RST reset generator has three possible inputs (the WWDT time-out reset, the BOD reset, and the PMU), and which input caused the reset is indicated in the external status register. All other reset generators have only one input which, depending on the hierarchy, can be either the CORE_RST, the PERIPHERAL_RST, or the MASTER_RST.

Note that the external status register does not show whether or not the reset was activated by a software reset. The software reset is indicated in the reset status registers 0 to 3 (see Table 94 to Table 97).

11.4.4.1 Reset external status register 0 for CORE_RST

This register shows whether or not any of the inputs to the CORE_RST reset generator has activated the CORE_RST. The CORE_RST can be activated by the external reset pin, a WWDT time-out, a BOD reset or by writing to bit 0 of the RESET_CTRL0 register.

Table 100. Reset external status register 0 (RESET_EXT_STAT0, address 0x4005 3400) bit description

Bit	Symbol	Description	Reset value	Access
0	EXT_RESET	Reset activated by external reset from reset pin. Write 0 to clear. 0 = Reset not activated by reset pin 1 = Reset activated	0	R/W
1	-	Reserved. Do not modify; read as logic 0.	0	-
2	-	Reserved. Do not modify; read as logic 0.	0	-
3	-	Reserved. Do not modify; read as logic 0.	0	-
4	BOD_RESET	Reset activated by BOD reset. Write 0 to clear. 0 = Reset not activated by BOD 1 = Reset activated	0	R/W
5	WWDT_RESET	Reset activated by WWDT time-out. Write 0 to clear. 0 = Reset not activated by WWDT 1 = Reset activated	0	R/W
31:6	-	Reserved. Do not modify; read as logic 0.	0	-

11.4.4.2 Reset external status register 1 for PERIPH_RST

This register shows whether or not the CORE_RST output has activated the PERIPH_RST. A reset generated from the CORE_RST is the only possible reset source for the PERIPH_RST aside from a software reset by writing to the RESET_CTRL register.

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Table 101. Reset external status register 1 (RESET_EXT_STAT1, address 0x4005 3404) bit description

Bit	Symbol	Description	Reset value	Access
0	-	Reserved. Do not modify; read as logic 0.	0	-
1	CORE_RESET	Reset activated by CORE_RST output. Write 0 to clear. 0 = Reset not activated 1 = Reset activated	0	R/W
31:2	-	Reserved. Do not modify; read as logic 0.	0	-

11.4.4.3 Reset external status register 2 for MASTER_RST

Table 102. Reset external status register 2 (RESET_EXT_STAT2, address 0x4005 3408) bit description

Bit	Symbol	Description	Reset value	Access
1:0	-	Reserved. Do not modify; read as logic 0.	0	-
2	PERIPHERAL_RESET	Reset activated by PERIPHERAL_RST output. Write 0 to clear. 0 = Reset not activated 1 = Reset activated	0	R/W
31:3	-	Reserved. Do not modify; read as logic 0.	0	-

11.4.4.4 Reset external status register 4 for WWDT_RST

Table 103. Reset external status register 4 (RESET_EXT_STAT4, address 0x4005 3410) bit description

Bit	Symbol	Description	Reset value	Access
0	-	Reserved. Do not modify; read as logic 0.	0	-
1	CORE_RESET	Reset activated by CORE_RST output. Write 0 to clear. 0 = Reset not activated 1 = Reset activated	0	R/W
31:2	-	Reserved. Do not modify; read as logic 0.	0	-

11.4.4.5 Reset external status register 5 for CREG_RST

Table 104. Reset external status register 5 (RESET_EXT_STAT5, address 0x4005 3414) bit description

Bit	Symbol	Description	Reset value	Access
0	-	Reserved. Do not modify; read as logic 0.	0	-
1	CORE_RESET	Reset activated by CORE_RST output. Write 0 to clear. 0 = Reset not activated 1 = Reset activated	0	R/W
31:2	-	Reserved. Do not modify; read as logic 0.	0	-

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11.4.4.6 Reset external status registers for PERIPHERAL_RESET

Refer to Table 91 for reset generators which have the PERIPH_RST output as reset source.

Table 105. Reset external status registers x (RESET_EXT_STATx, address 0x4005 34xx) bit description

Bit	Symbol	Description	Reset value	Access
1:0	-	Reserved. Do not modify; read as logic 0.	0	-
2	PERIPHERAL_RESET	Reset activated by PERIPHERAL_RST output. Write 0 to clear. 0 = Reset not activated 1 = Reset activated	0	R/W
31:3	-	Reserved. Do not modify; read as logic 0.	0	-

11.4.4.7 Reset external status registers for MASTER_RESET

Refer to Table 91 for reset generators which have the MASTER_RST output as reset source. These are the ARM Cortex-M3 core, the LCD controller, the USB0, the GPDMA, the SDIO controller, the external memory controller, the Ethernet controller, and the AES.

The reset value is dependent on the peripheral, see Table 91.

Table 106. Reset external status registers y (RESET_EXT_STATy, address 0x4005 34yy) bit description

Bit	Symbol	Description	Reset value	Access
2:0	-	Reserved. Do not modify; read as logic 0.	0	-
3	MASTER_RESET	Reset activated by MASTER_RST output. Write 0 to clear. 0 = Reset not activated 1 = Reset activated	0	R/W
31:4	-	Reserved. Do not modify; read as logic 0.	0	-

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12.1 How to read this chapter

This chapter applies to parts LPC1850_30_20_10 Rev 'A' only.

12.2 Pin description

On the LPC18xx, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin may support up to four different digital functions, including General Purpose I/O (GPIO), selectable through the SCU registers. Note that the pin name is not indicative of the GPIO port assigned to it.

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Table 107. Pin description

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
Multiplexed digital pins									
P0_0	L3	x	x	x	32	[3]	I; PU	I/O	**GPIO0[0]** — General purpose digital input/output pin.
								I/O	**SSP1_MISO** — Master In Slave Out for SSP1.
								I	**ENET_RXD1** — Ethernet receive data 1 (RMII/MII interface).
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**I2S0_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
								I/O	**I2S1_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
P0_1	M2	x	x	x	34	[3]	I; PU	I/O	**GPIO0[1]** — General purpose digital input/output pin.
								I/O	**SSP1_MOSI** — Master Out Slave in for SSP1.
								I	**ENET_COL** — Ethernet Collision detect (MII interface).
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
									ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
								I/O	**I2S1_TX_SDA** — I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
P1_0	P2	x	x	x	38	[3]	I; PU	I/O	**GPIO0[4]** — General purpose digital input/output pin.
								I	**CTIN_3** — SCT input 3. Capture input 1 of timer 1.
								I/O	**EMC_A5** — External memory address line 5.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SSP0_SSEL** — Slave Select for SSP0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description ...*continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P1_1	R2	x	x	x	42	[3]	I; PU	I/O	**GPIO0[8]** — General purpose digital input/output pin. Boot pin (see Table 8).
								O	**CTOUT_7** — SCT output 7. Match output 3 of timer 1.
								I/O	**EMC_A6** — External memory address line 6.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SSP0_MISO** — Master In Slave Out for SSP0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P1_2	R3	x	x	x	43	[3]	I; PU	I/O	**GPIO0[9]** — General purpose digital input/output pin. Boot pin (see Table 8).
								O	**CTOUT_6** — SCT output 6. Match output 2 of timer 1.
								I/O	**EMC_A7** — External memory address line 7.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SSP0_MOSI** — Master Out Slave in for SSP0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P1_3	P5	x	x	x	44	[3]	I; PU	I/O	**GPIO0[10]** — General purpose digital input/output pin.
								O	**CTOUT_8** — SCT output 8. Match output 0 of timer 2.
								-	**R** — Function reserved.
								O	**EMC_OE** — LOW active Output Enable signal.
								O	**USB0_IND1** — USB0 port indicator LED control output 1.
								I/O	**SSP1_MISO** — Master In Slave Out for SSP1.
								-	**R** — Function reserved.
								O	**SD_RST** — SD/MMC reset signal for MMC4.4 card.
P1_4	T3	x	x	x	47	[3]	I; PU	I/O	**GPIO0[11]** — General purpose digital input/output pin.
								O	**CTOUT_9** — SCT output 9. Match output 1 of timer 2.
								-	**R** — Function reserved.
								O	**EMC_BLS0** — LOW active Byte Lane select signal 0.
								O	**USB0_IND0** — USB0 port indicator LED control output 0.
								I/O	**SSP1_MOSI** — Master Out Slave in for SSP1.
								-	**R** — Function reserved.
								O	**SD_VOLT1** — SD/MMC bus voltage select output 1.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P1_5	R5	x	x	x	48	[3]	I; PU	I/O	**GPIO1[8]** — General purpose digital input/output pin.
								O	**CTOUT_10** — SCT output 10. Match output 2 of timer 2.
								-	**R** — Function reserved.
								O	**EMC_CS0** — LOW active Chip Select 0 signal.
								O	**USB0_PWR_FAULT** — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
								I/O	**SSP1_SSEL** — Slave Select for SSP1.
								-	**R** — Function reserved.
								O	**SD_POW** — <tbd>.
P1_6	T4	x	x	x	49	[3]	I; PU	I/O	**GPIO1[9]** — General purpose digital input/output pin.
								I	**CTIN_5** — SCT input 5. Capture input 2 of timer 2.
								-	**R** — Function reserved.
								O	**EMC_WE** — LOW active Write Enable signal.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SD_CMD** — SD/MMC command signal.
P1_7	T5	x	x	x	50	[3]	I; PU	I/O	**GPIO1[0]** — General purpose digital input/output pin.
								I	**U1_DSR** — Data Set Ready input for UART1.
								O	**CTOUT_13** — SCT output 13. Match output 1 of timer 3.
								I/O	**EMC_D0** — External memory data line 0.
								O	**USB0_PWR_EN** — VBUS drive signal (towards external charge pump or power management unit); indicates that Vbus must be driven (active high).
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P1_8	R7	x	x	x	51	[3]	I; PU	I/O	**GPIO1[1]** — General purpose digital input/output pin.
								O	**U1_DTR** — Data Terminal Ready output for UART1.
								O	**CTOUT_12** — SCT output 12. Match output 0 of timer 3.
								I/O	**EMC_D1** — External memory data line 1.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**SD_VOLT0** — SD/MMC bus voltage select output 0.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P1_9	T7	x	x	x	52	[3]	I; PU	I/O	**GPIO1[2]** — General purpose digital input/output pin.
								O	**U1_RTS** — Request to Send output for UART1.
								O	**CTOUT_11** — SCT output 11. Match output 3 of timer 2.
								I/O	**EMC_D2** — External memory data line 2.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SD_DAT0** — SD/MMC data bus line 0.
P1_10	R8	x	x	x	53	[3]	I; PU	I/O	**GPIO1[3]** — General purpose digital input/output pin.
								I	**U1_RI** — Ring Indicator input for UART1.
								O	**CTOUT_14** — SCT output 14. Match output 2 of timer 3.
								I/O	**EMC_D3** — External memory data line 3.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SD_DAT1** — SD/MMC data bus line 1.
P1_11	T9	x	x	x	55	[3]	I; PU	I/O	**GPIO1[4]** — General purpose digital input/output pin.
								I	**U1_CTS** — Clear to Send input for UART1.
								O	**CTOUT_15** — SCT output 15. Match output 3 of timer 3.
								I/O	**EMC_D4** — External memory data line 4.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SD_DAT2** — SD/MMC data bus line 2.
P1_12	R9	x	x	x	56	[3]	I; PU	I/O	**GPIO1[5]** — General purpose digital input/output pin.
								I	**U1_DCD** — Data Carrier Detect input for UART1.
								-	**R** — Function reserved.
								I/O	**EMC_D5** — External memory data line 5.
								I	**T0_CAP1** — Capture input 1 of timer 0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SD_DAT3** — SD/MMC data bus line 3.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P1_13	R10	x	x	x	60	[3]	I; PU	I/O	**GPIO1[6]** — General purpose digital input/output pin.
								O	**U1_TXD** — Transmitter output for UART1.
								-	**R** — Function reserved.
								I/O	**EMC_D6** — External memory data line 6.
								I	**T0_CAP0** — Capture input 0 of timer 0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**SD_CD** — SD/MMC card detect input.
P1_14	R11	x	x	x	61	[3]	I; PU	I/O	**GPIO1[7]** — General purpose digital input/output pin.
								I	**U1_RXD** — Receiver input for UART1.
								-	**R** — Function reserved.
								I/O	**EMC_D7** — External memory data line 7.
								O	**T0_MAT2** — Match output 2 of timer 0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P1_15	T12	x	x	x	62	[3]	I; PU	I/O	**GPIO0[2]** — General purpose digital input/output pin.
								O	**U2_TXD** — Transmitter output for USART2.
								-	**R** — Function reserved.
								I	**ENET_RXD0** — Ethernet receive data 0 (RMII/MII interface).
								O	**T0_MAT1** — Match output 1of timer 0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P1_16	M7	x	x	x	64	[3]	I; PU	I/O	**GPIO0[3]** — General purpose digital input/output pin.
								I	**U2_RXD** — Receiver input for USART2.
								-	**R** — Function reserved.
								I	**ENET_CRS** — Ethernet Carrier Sense (MII interface).
								O	**T0_MAT0** — Match output 0 of timer 0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**ENET_RX_DV** — Ethernet Receive Data Valid (RMII/MII interface).

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P1_17	M8	x	x	x	66	[4]	I; PU	I/O	**GPIO0[12]** — General purpose digital input/output pin.
								I/O	**U2_UCLK** — Serial clock input/output for USART2 in synchronous mode.
								-	**R** — Function reserved.
								I/O	**ENET_MDIO** — Ethernet MIIM data input and output.
								I	**T0_CAP3** — Capture input 3 of timer 0.
								O	**CAN1_TD** — CAN1 transmitter output.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P1_18	N12	x	x	x	67	[3]	I; PU	I/O	**GPIO0[13]** — General purpose digital input/output pin.
								I/O	**U2_DIR** — RS-485/EIA-485 output enable/direction control for USART2.
								-	**R** — Function reserved.
								O	**ENET_TXD0** — Ethernet transmit data 0 (RMII/MII interface).
								O	**T0_MAT3** — Match output 3 of timer 0.
								I	**CAN1_RD** — CAN1 receiver input.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P1_19	M11	x	x	x	68	[3]	I; PU	I	**ENET_TX_CLK (ENET_REF_CLK)** — Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
								I/O	**SSP1_SCK** — Serial clock for SSP1.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**CLKOUT** — Clock output pin.
								-	**R** — Function reserved.
								O	**I2S0_RX_MCLK** — I2S receive master clock.
								I/O	**I2S1_TX_SCK** — Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
P1_20	M10	x	x	x	70	[3]	I; PU	I/O	**GPIO0[15]** — General purpose digital input/output pin.
								I/O	**SSP1_SSEL** — Slave Select for SSP1.
								-	**R** — Function reserved.
								O	**ENET_TXD1** — Ethernet transmit data 1 (RMII/MII interface).
								I	**T0_CAP2** — Capture input 2 of timer 0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P2_0	T16	x	x	x	75	[3]	I; PU	-	**R** — Function reserved.
								O	**U0_TXD** — Transmitter output for USART0.
								I/O	**EMC_A13** — External memory address line 13.
								O	**USB0_PWR_EN** — VBUS drive signal (towards external charge pump or power management unit); indicates that Vbus must be driven (active high).
								I/O	**GPIO5[0]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								I	**T3_CAP0** — Capture input 0 of timer 3.
								O	**ENET_MDC** — Ethernet MIIM clock.
P2_1	N15	x	x	x	81	[3]	I; PU	-	**R** — Function reserved.
								I	**U0_RXD** — Receiver input for USART0.
								I/O	**EMC_A12** — External memory address line 12.
								O	**USB0_PWR_FAULT** — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
								I/O	**GPIO5[1]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								I	**T3_CAP1** — Capture input 1 of timer 3.
								-	**R** — Function reserved.
P2_2	M15	x	x	x	84	[3]	I; PU	-	**R** — Function reserved.
								I/O	**U0_UCLK** — Serial clock input/output for USART0 in synchronous mode.
								I/O	**EMC_A11** — External memory address line 11.
								O	**USB0_IND1** — USB0 port indicator LED control output 1.
								I/O	**GPIO5[2]** — General purpose digital input/output pin.
								O	**CTOUT_6** — SCT output 6. Match output 2 of timer 1.
								I	**T3_CAP2** — Capture input 2 of timer 3.
								-	**R** — Function reserved.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P2_3	J12	x	x	x	87	[4]	I; PU	-	**R** — Function reserved.
								I/O	**I2C1_SDA** — I^2C1 data input/output (this pin does not use a specialized I^2C pad).
								O	**U3_TXD** — Transmitter output for USART3.
								I	**CTIN_1** — SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
								I/O	**GPIO5[3]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								O	**T3_MAT0** — Match output 0 of timer 3.
								O	**USB0_PWR_EN** — VBUS drive signal (towards external charge pump or power management unit); indicates that Vbus must be driven (active HIGH).
P2_4	K11	x	x	x	88	[4]	I; PU	-	**R** — Function reserved.
								I/O	**I2C1_SCL** — I^2C1 clock input/output (this pin does not use a specialized I^2C pad).
								I	**U3_RXD** — Receiver input for USART3.
								I	**CTIN_0** — SCT input 0. Capture input 0 of timer 0, 1, 2, 3.
								I/O	**GPIO5[4]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								O	**T3_MAT1** — Match output 1 of timer 3.
								O	**USB0_PWR_FAULT** — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
P2_5	K14	x	x	x	91	[4]	I; PU	-	**R** — Function reserved.
								I	**CTIN_2** — SCT input 2. Capture input 2 of timer 0.
								I	**USB1_VBUS** — Monitors the presence of USB1 bus power. **Note:** This signal must be HIGH for USB reset to occur.
								I	**ADCTRIG1** — ADC trigger input 1.
								I/O	**GPIO5[5]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								O	**T3_MAT2** — Match output 2 of timer 3.
								O	**USB0_IND0** — USB0 port indicator LED control output 0.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P2_6	K16	x	x	x	95	[3]	I; PU	-	**R** — Function reserved.
								I/O	**U0_DIR** — RS-485/EIA-485 output enable/direction control for USART0.
								I/O	**EMC_A10** — External memory address line 10.
								O	**USB0_IND0** — USB0 port indicator LED control output 0.
								I/O	**GPIO5[6]** — General purpose digital input/output pin.
								I	**CTIN_7** — SCT input 7.
								I	**T3_CAP3** — Capture input 3 of timer 3.
								-	**R** — Function reserved.
P2_7	H14	x	x	x	96	[3]	I; PU	I/O	**GPIO0[7]** — General purpose digital input/output pin. ISP entry pin. If this pin is pulled LOW at reset, the part enters ISP mode using USART0.
								O	**CTOUT_1** — SCT output 1. Match output 1 of timer 0.
								I/O	**U3_UCLK** — Serial clock input/output for USART3 in synchronous mode.
								I/O	**EMC_A9** — External memory address line 9.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**T3_MAT3** — Match output 3 of timer 3.
								-	**R** — Function reserved.
P2_8	J16	x	x	x	98	[3]	I; PU	-	n.c. - Boot pin (see Table 8).
								O	**CTOUT_0** — SCT output 0. Match output 0 of timer 0.
								I/O	**U3_DIR** — RS-485/EIA-485 output enable/direction control for USART3.
								I/O	**EMC_A8** — External memory address line 8.
								I/O	**GPIO5[7]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P2_9	H16	x	x	x	102	[3]	I; PU	I/O	**GPIO1[10]** — General purpose digital input/output pin. Boot pin (see Table 8).
								O	**CTOUT_3** — SCT output 3. Match output 3 of timer 0.
								I/O	**U3_BAUD** — <tbd> for USART3.
								I/O	**EMC_A0** — External memory address line 0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P2_10	G16	x	x	x	104	[3]	I; PU	I/O	**GPIO0[14]** — General purpose digital input/output pin.
								O	**CTOUT_2** — SCT output 2. Match output 2 of timer 0.
								O	**U2_TXD** — Transmitter output for USART2.
								I/O	**EMC_A1** — External memory address line 1.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P2_11	F16	x	x	x	105	[3]	I; PU	I/O	**GPIO1[11]** — General purpose digital input/output pin.
								O	**CTOUT_5** — SCT output 5. Match output 1 of timer 1.
								I	**U2_RXD** — Receiver input for USART2.
								I/O	**EMC_A2** — External memory address line 2.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P2_12	E15	x	x	x	106	[3]	I; PU	I/O	**GPIO1[12]** — General purpose digital input/output pin.
								O	**CTOUT_4** — SCT output 4. Match output 0 of timer 1.
								-	**R** — Function reserved.
								I/O	**EMC_A3** — External memory address line 3.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**U2_UCLK** — Serial clock input/output for USART2 in synchronous mode.
P2_13	C16	x	x	x	108	[3]	I; PU	I/O	**GPIO1[13]** — General purpose digital input/output pin.
								I	**CTIN_4** — SCT input 4. Capture input 2 of timer 1.
								-	**R** — Function reserved.
								I/O	**EMC_A4** — External memory address line 4.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**U2_DIR** — RS-485/EIA-485 output enable/direction control for USART2.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P3_0	F13	x	x	x	112	[3]	I; PU	I/O	**I2S0_RX_SCK** — I2S transmit clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
								O	**I2S0_RX_MCLK** — I2S receive master clock.
								I/O	**I2S0_TX_SCK** — Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I²S-bus specification.
								O	**I2S0_TX_MCLK** — I2S transmit master clock.
								I/O	**SSP0_SCK** — Serial clock for SSP0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P3_1	G11	x	x	x	114	[3]	I; PU	I/O	**I2S0_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
								I/O	**I2S0_RX_WS** — Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
								I	**CAN0_RD** — CAN receiver input.
								O	**USB1_IND1** — USB1 Port indicator LED control output 1.
								I/O	**GPIO5[8]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								O	**LCD_VD15** — LCD data.
								-	**R** — Function reserved.
P3_2	F11	x	x	x	116	[3]	I; PU	I/O	**I2S0_TX_SDA** — I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
								I/O	**I2S0_RX_SDA** — I2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
								O	**CAN0_TD** — CAN transmitter output.
								O	**USB1_IND0** — USB1 Port indicator LED control output 0.
								I/O	**GPIO5[9]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								O	**LCD_VD14** — LCD data.
								-	**R** — Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P3_3	B14	x	x	x	118	[5]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SSP0_SCK** — Serial clock for SSP0.
								O	**SPIFI_SCK** — Serial clock for SPIFI.
								O	**CGU_OUT1** — CGU spare clock output 1.
								-	**R** — Function reserved.
								O	**I2S0_TX_MCLK** — I2S transmit master clock.
								I/O	**I2S1_TX_SCK** — Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
P3_4	A15	x	x	x	119	[3]	I; PU	I/O	**GPIO1[14]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SPIFI_SIO3** — I/O lane 3 for SPIFI.
								O	**U1_TXD** — Transmitter output for UART 1.
								I/O	**I2S0_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
								I/O	**I2S1_RX_SDA** — I2S1 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
								O	**LCD_VD13** — LCD data.
P3_5	C12	x	x	x	121	[3]	I; PU	I/O	**GPIO1[15]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SPIFI_SIO2** — I/O lane 2 for SPIFI.
								I	**U1_RXD** — Receiver input for UART 1.
								I/O	**I2S0_TX_SDA** — I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
								I/O	**I2S1_RX_WS** — Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
								O	**LCD_VD12** — LCD data.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P3_6	B13	x	x	x	122	[3]	I; PU	I/O	**GPIO0[6]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								I/O	**SSP0_SSEL** — Slave Select for SSP0.
								I/O	**SPIFI_MISO** — Input 1 in SPIFI quad mode; SPIFI output IO1.
								-	**R** — Function reserved.
								I/O	**SSP0_MISO** — Master In Slave Out for SSP0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P3_7	C11	x	x	x	123	[3]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SSP0_MISO** — Master In Slave Out for SSP0.
								I/O	**SPIFI_MOSI** — Input I0 in SPIFI quad mode; SPIFI output IO0.
								I/O	**GPIO5[10]** — General purpose digital input/output pin.
								I/O	**SSP0_MOSI** — Master Out Slave in for SSP0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P3_8	C10	x	x	x	124	[3]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SSP0_MOSI** — Master Out Slave in for SSP0.
								I/O	**SPIFI_CS** — SPIFI serial flash chip select.
								I/O	**GPIO5[11]** — General purpose digital input/output pin.
								I/O	**SSP0_SSEL** — Slave Select for SSP0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P4_0	D5	x	-	x	1	[3]	I; PU	I/O	**GPIO2[0]** — General purpose digital input/output pin.
								O	**MCOA0** — Motor control PWM channel 0, output A.
								I	**NMI** — External interrupt input to NMI.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**LCD_VD13** — LCD data.
								I/O	**U3_UCLK** — Serial clock input/output for USART3 in synchronous mode.
								-	**R** — Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P4_1	A1	x	-	x	3	[6]	I; PU	I/O	**GPIO2[1]** — General purpose digital input/output pin.
								O	**CTOUT_1** — SCT output 1. Match output 1 of timer 0.
								O	**LCD_VD0** — LCD data.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**LCD_VD19** — LCD data.
								O	**U3_TXD** — Transmitter output for USART3.
								I	**ENET_COL** — Ethernet Collision detect (MII interface).
								I	**ADC0_1** — ADC0, input channel 1.
P4_2	D3	x	-	x	8	[3]	I; PU	I/O	**GPIO2[2]** — General purpose digital input/output pin.
								O	**CTOUT_0** — SCT output 0. Match output 0 of timer 0.
								O	**LCD_VD3** — LCD data.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**LCD_VD12** — LCD data.
								I	**U3_RXD** — Receiver input for USART3.
								-	**R** — Function reserved.
P4_3	C2	x	-	x	7	[6]	I; PU	I/O	**GPIO2[3]** — General purpose digital input/output pin.
								O	**CTOUT_3** — SCT output 0. Match output 3 of timer 0.
								O	**LCD_VD2** — LCD data.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**LCD_VD21** — LCD data.
								I/O	**U3_BAUD** — <tbd> for USART3.
								-	**R** — Function reserved.
								I	**ADC0_0** — ADC0, input channel 0.
P4_4	B1	x	-	x	9	[6]	I; PU	I/O	**GPIO2[4]** — General purpose digital input/output pin.
								O	**CTOUT_2** — SCT output 2. Match output 2 of timer 0.
								O	**LCD_VD1** — LCD data.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**LCD_VD20** — LCD data.
								I/O	**U3_DIR** — RS-485/EIA-485 output enable/direction control for USART3.
								-	**R** — Function reserved.
								O	**DAC** — DAC output.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P4_5	D2	x	-	x	10	[3]	I; PU	I/O	**GPIO2[5]** — General purpose digital input/output pin.
								O	**CTOUT_5** — SCT output 5. Match output 1 of timer 1.
								O	**LCD_FP** — Frame pulse (STN). Vertical synchronization pulse (TFT).
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P4_6	C1	x	-	x	11	[3]	I; PU	I/O	**GPIO2[6]** — General purpose digital input/output pin.
								O	**CTOUT_4** — SCT output 4. Match output 0 of timer 1.
								O	**LCD_ENAB/LCDM** — STN AC bias drive or TFT data enable input.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P4_7	H4	x	-	x	14	[3]	<tbd>	O	**LCD_DCLK** — LCD panel clock.
								I	**GP_CLKIN** — General purpose clock input to the CGU.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**I2S1_TX_SCK** — Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
								I/O	**I2S0_TX_SCK** — Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
P4_8	E2	x	-	x	15	[3]	I; PU	-	**R** — Function reserved.
								I	**CTIN_5** — SCT input 5. Capture input 2 of timer 2.
								O	**LCD_VD9** — LCD data.
								-	**R** — Function reserved.
								I/O	**GPIO5[12]** — General purpose digital input/output pin.
								O	**LCD_VD22** — LCD data.
								O	**CAN1_TD** — CAN1 transmitter output.
								-	**R** — Function reserved.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P4_9	L2	x	-	x	33	[3]	I; PU	-	**R** — Function reserved.
								I	**CTIN_6** — SCT input 6. Capture input 1 of timer 3.
								O	**LCD_VD11** — LCD data.
								-	**R** — Function reserved.
								I/O	**GPIO5[13]** — General purpose digital input/output pin.
								O	**LCD_VD15** — LCD data.
								I	**CAN1_RD** — CAN1 receiver input.
								-	**R** — Function reserved.
P4_10	M3	x	-	x	35	[3]	I; PU	-	**R** — Function reserved.
								I	**CTIN_2** — SCT input 2. Capture input 2 of timer 0.
								O	**LCD_VD10** — LCD data.
								-	**R** — Function reserved.
								I/O	**GPIO5[14]** — General purpose digital input/output pin.
								O	**LCD_VD14** — LCD data.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P5_0	N3	x	-	x	37	[3]	I; PU	I/O	**GPIO2[9]** — General purpose digital input/output pin.
								O	**MCOB2** — Motor control PWM channel 2, output B.
								I/O	**EMC_D12** — External memory data line 12.
								-	**R** — Function reserved.
								I	**U1_DSR** — Data Set Ready input for UART 1.
								I	**T1_CAP0** — Capture input 0 of timer 1.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P5_1	P3	x	-	x	39	[3]	I; PU	I/O	**GPIO2[10]** — General purpose digital input/output pin.
								I	**MCI2** — Motor control PWM channel 2, input.
								I/O	**EMC_D13** — External memory data line 13.
								-	**R** — Function reserved.
								O	**U1_DTR** — Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
								I	**T1_CAP1** — Capture input 1 of timer 1.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P5_2	R4	x	-	x	46	[3]	I; PU	I/O	**GPIO2[11]** — General purpose digital input/output pin.
								I	**MCI1** — Motor control PWM channel 1, input.
								I/O	**EMC_D14** — External memory data line 14.
								-	**R** — Function reserved.
								O	**U1_RTS** — Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
								I	**T1_CAP2** — Capture input 2 of timer 1.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P5_3	T8	x	-	x	54	[3]	I; PU	I/O	**GPIO2[12]** — General purpose digital input/output pin.
								I	**MCI0** — Motor control PWM channel 0, input.
								I/O	**EMC_D15** — External memory data line 15.
								-	**R** — Function reserved.
								I	**U1_RI** — Ring Indicator input for UART 1.
								I	**T1_CAP3** — Capture input 3 of timer 1.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P5_4	P9	x	-	x	57	[3]	I; PU	I/O	**GPIO2[13]** — General purpose digital input/output pin.
								O	**MCOB0** — Motor control PWM channel 0, output B.
								I/O	**EMC_D8** — External memory data line 8.
								-	**R** — Function reserved.
								I	**U1_CTS** — Clear to Send input for UART 1.
								O	**T1_MAT0** — Match output 0 of timer 1.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P5_5	P10	x	-	x	58	[3]	I; PU	I/O	**GPIO2[14]** — General purpose digital input/output pin.
								O	**MCOA1** — Motor control PWM channel 1, output A.
								I/O	**EMC_D9** — External memory data line 9.
								-	**R** — Function reserved.
								I	**U1_DCD** — Data Carrier Detect input for UART 1.
								O	**T1_MAT1** — Match output 1 of timer 1.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P5_6	T13	x	-	x	63	[3]	I; PU	I/O	**GPIO2[15]** — General purpose digital input/output pin.
								O	**MCOB1** — Motor control PWM channel 1, output B.
								I/O	**EMC_D10** — External memory data line 10.
								-	**R** — Function reserved.
								O	**U1_TXD** — Transmitter output for UART 1.
								O	**T1_MAT2** — Match output 2 of timer 1.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P5_7	R12	x	-	x	65	[3]	I; PU	I/O	**GPIO2[7]** — General purpose digital input/output pin.
								O	**MCOA2** — Motor control PWM channel 2, output A.
								I/O	**EMC_D11** — External memory data line 11.
								-	**R** — Function reserved.
								I	**U1_RXD** — Receiver input for UART 1.
								O	**T1_MAT3** — Match output 3 of timer 1.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P6_0	M12	x	x	x	73	[3]	I; PU	-	**R** — Function reserved.
								O	**I2S0_RX_MCLK** — I2S receive master clock.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**I2S0_RX_SCK** — Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P6_1	R15	x	x	x	74	[3]	I; PU	I/O	**GPIO3[0]** — General purpose digital input/output pin.
								O	**EMC_DYCS1** — SDRAM chip select 1.
								I/O	**U0_UCLK** — Serial clock input/output for USART0 in synchronous mode.
								I/O	**I2S0_RX_WS** — Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
								-	**R** — Function reserved.
								I	**T2_CAP0** — Capture input 2 of timer 2.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P6_2	L13	x	x	x	78	[3]	I; PU	I/O	**GPIO3[1]** — General purpose digital input/output pin.
								O	**EMC_CKEOUT1** — SDRAM clock enable 1.
								I/O	**U0_DIR** — RS-485/EIA-485 output enable/direction control for USART0.
								I/O	**I2S0_RX_SDA** — I2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^{2}S-bus specification*.
								-	**R** — Function reserved.
								I	**T2_CAP1** — Capture input 1 of timer 2.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P6_3	P15	x	-	x	79	[3]	I; PU	I/O	**GPIO3[2]** — General purpose digital input/output pin.
								O	**USB0_PWR_EN** — VBUS drive signal (towards external charge pump or power management unit); indicates that the VBUS signal must be driven (active HIGH).
								-	**R** — Function reserved.
								O	**EMC_CS1** — LOW active Chip Select 1 signal.
								-	**R** — Function reserved.
								I	**T2_CAP2** — Capture input 2 of timer 2.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P6_4	R16	x	x	x	80	[3]	I; PU	I/O	**GPIO3[3]** — General purpose digital input/output pin.
								I	**CTIN_6** — SCT input 6. Capture input 1 of timer 3.
								O	**U0_TXD** — Transmitter output for USART0.
								O	**EMC_CAS** — LOW active SDRAM Column Address Strobe.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P6_5	P16	x	x	x	82	[3]	I; PU	I/O	**GPIO3[4]** — General purpose digital input/output pin.
								O	**CTOUT_6** — SCT output 6. Match output 2 of timer 1.
								I	**U0_RXD** — Receiver input for USART0.
								O	**EMC_RAS** — LOW active SDRAM Row Address Strobe.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P6_6	L14	x	-	x	83	[3]	I; PU	I/O	**GPIO0[5]** — General purpose digital input/output pin.
								O	**EMC_BLS1** — LOW active Byte Lane select signal 1.
								-	**R** — Function reserved.
								O	**USB0_PWR_FAULT** — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
								-	**R** — Function reserved.
								I	**T2_CAP3** — Capture input 3 of timer 2.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P6_7	J13	x	-	x	85	[3]	I; PU	-	**R** — Function reserved.
								I/O	**EMC_A15** — External memory address line 15.
								-	**R** — Function reserved.
								O	**USB0_IND1** — USB0 port indicator LED control output 1.
								I/O	**GPIO5[15]** — General purpose digital input/output pin.
								O	**T2_MAT0** — Match output 0 of timer 2.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P6_8	H13	x	-	x	86	[3]	I; PU	-	**R** — Function reserved.
								I/O	**EMC_A14** — External memory address line 14.
								-	**R** — Function reserved.
								O	**USB0_IND0** — USB0 port indicator LED control output 0.
								I/O	**GPIO5[16]** — General purpose digital input/output pin.
								O	**T2_MAT1** — Match output 1 of timer 2.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P6_9	J15	x	x	x	97	[3]	I; PU	I/O	**GPIO3[5]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**EMC_DYCS0** — SDRAM chip select 0.
								-	**R** — Function reserved.
								O	**T2_MAT2** — Match output 2 of timer 2.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P6_10	H15	x	-	x	100	[3]	I; PU	I/O	**GPIO3[6]** — General purpose digital input/output pin.
								O	**MCABORT** — Motor control PWM, LOW-active fast abort.
								-	**R** — Function reserved.
								O	**EMC_DQMOUT1** — Data mask 1 used with SDRAM and static devices.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P6_11	H12	x	x	x	101	[3]	I; PU	I/O	**GPIO3[7]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**EMC_CKEOUT0** — SDRAM clock enable 0.
								-	**R** — Function reserved.
								O	**T2_MAT3** — Match output 2 of timer 3.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P6_12	G15	x	-	x	103	[3]	I; PU	I/O	**GPIO2[8]** — General purpose digital input/output pin.
								O	**CTOUT_7** — SCT output 7. Match output 3 of timer 1.
								-	**R** — Function reserved.
								O	**EMC_DQMOUT0** — Data mask 0 used with SDRAM and static devices.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P7_0	B16	x	-	x	110	[3]	I; PU	I/O	**GPIO3[8]** — General purpose digital input/output pin.
								O	**CTOUT_14** — SCT output 14. Match output 2 of timer 3.
								-	**R** — Function reserved.
								O	**LCD_LE** — Line end signal.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P7_1	C14	x	-	x	113	[3]	I; PU	I/O	**GPIO3[9]** — General purpose digital input/output pin.
								O	**CTOUT_15** — SCT output 15. Match output 3 of timer 3.
								I/O	**I2S0_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
								O	**LCD_VD19** — LCD data.
								O	**LCD_VD7** — LCD data.
								-	**R** — Function reserved.
								O	**U2_TXD** — Transmitter output for USART2.
								-	**R** — Function reserved.
P7_2	A16	x	-	x	113	[3]	I; PU	I/O	**GPIO3[10]** — General purpose digital input/output pin.
								I	**CTIN_4** — SCT input 4. Capture input 2 of timer 1.
								I/O	**I2S0_TX_SDA** — I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
								O	**LCD_VD18** — LCD data.
								O	**LCD_VD6** — LCD data.
								-	**R** — Function reserved.
								I	**U2_RXD** — Receiver input for USART2.
								-	**R** — Function reserved.
P7_3	C13	x	-	x	117	[3]	I; PU	I/O	**GPIO3[11]** — General purpose digital input/output pin.
								I	**CTIN_3** — SCT input 3. Capture input 1 of timer 1.
								-	**R** — Function reserved.
								O	**LCD_VD17** — LCD data.
								O	**LCD_VD5** — LCD data.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P7_4	C8	x	-	x	132	[6]	I; PU	I/O	**GPIO3[12]** — General purpose digital input/output pin.
								O	**CTOUT_13** — SCT output 13. Match output 1 of timer 3.
								-	**R** — Function reserved.
								O	**LCD_VD16** — LCD data.
								O	**LCD_VD4** — LCD data.
								O	**TRACEDATA[0]** — Trace data, bit 0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**ADC0_4** — ADC0, input channel 4.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P7_5	A7	x	-	x	133	[6]	I; PU	I/O	**GPIO3[13]** — General purpose digital input/output pin.
								O	**CTOUT_12** — SCT output 12. Match output 0 of timer 3.
								-	**R** — Function reserved.
								O	**LCD_VD8** — LCD data.
								O	**LCD_VD23** — LCD data.
								O	**TRACEDATA[1]** — Trace data, bit 1.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**ADC0_3** — ADC0, input channel 3.
P7_6	C7	x	-	x	134	[3]	I; PU	I/O	**GPIO3[14]** — General purpose digital input/output pin.
								O	**CTOUT_11** — SCT output 1. Match output 3 of timer 2.
								-	**R** — Function reserved.
								O	**LCD_LP** — Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
								-	**R** — Function reserved.
								O	**TRACEDATA[2]** — Trace data, bit 2.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
P7_7	B6	x	-	x	140	[6]	I; PU	I/O	**GPIO3[15]** — General purpose digital input/output pin.
								O	**CTOUT_8** — SCT output 8. Match output 0 of timer 2.
								-	**R** — Function reserved.
								O	**LCD_PWR** — LCD panel power enable.
								-	**R** — Function reserved.
								O	**TRACEDATA[3]** — Trace data, bit 3.
								O	**ENET_MDC** — Ethernet MIIM clock.
								-	**R** — Function reserved.
								I	**ADC1_6** — ADC1, input channel 6.
P8_0	E5	x	-	x	-	[4]	I; PU	I/O	**GPIO4[0]** — General purpose digital input/output pin.
								O	**USB0_PWR_FAULT** — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
								-	**R** — Function reserved.
								I	**MCI2** — Motor control PWM channel 2, input.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**T0_MAT0** — Match output 0 of timer 0.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P8_1	H5	x	-	x	-	[4]	I; PU	I/O	**GPIO4[1]** — General purpose digital input/output pin.
								O	**USB0_IND1** — USB0 port indicator LED control output 1.
								-	**R** — Function reserved.
								I	**MCI1** — Motor control PWM channel 1, input.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**T0_MAT1** — Match output 1 of timer 0.
P8_2	K4	x	-	x	-	[4]	I; PU	I/O	**GPIO4[2]** — General purpose digital input/output pin.
								O	**USB0_IND0** — USB0 port indicator LED control output 0.
								-	**R** — Function reserved.
								I	**MCI0** — Motor control PWM channel 0, input.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**T0_MAT2** — Match output 2 of timer 0.
P8_3	J3	x	-	x	-	[3]	I; PU	I/O	**GPIO4[3]** — General purpose digital input/output pin.
								I/O	**USB1_ULPI_D2** — ULPI link bidirectional data line 2.
								-	**R** — Function reserved.
								O	**LCD_VD12** — LCD data.
								O	**LCD_VD19** — LCD data.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**T0_MAT3** — Match output 3 of timer 0.
P8_4	J2	x	-	x	-	[3]	I; PU	I/O	**GPIO4[4]** — General purpose digital input/output pin.
								I/O	**USB1_ULPI_D1** — ULPI link bidirectional data line 1.
								-	**R** — Function reserved.
								O	**LCD_VD7** — LCD data.
								O	**LCD_VD16** — LCD data.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**T0_CAP0** — Capture input 0 of timer 0.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P8_5	J1	x	-	x	-	[3]	I; PU	I/O	**GPIO4[5]** — General purpose digital input/output pin.
								I/O	**USB1_ULPI_D0** — ULPI link bidirectional data line 0.
								-	**R** — Function reserved.
								O	**LCD_VD6** — LCD data.
								O	**LCD_VD8** — LCD data.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**T0_CAP1** — Capture input 1 of timer 0.
P8_6	K3	x	-	x	-	[3]	I; PU	I/O	**GPIO4[6]** — General purpose digital input/output pin.
								I	**USB1_ULPI_NXT** — ULPI link NXT signal. Data flow control signal from the PHY.
								-	**R** — Function reserved.
								O	**LCD_VD5** — LCD data.
								O	**LCD_LP** — Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**T0_CAP2** — Capture input 2 of timer 0.
P8_7	K1	x	-	x	-	[3]	I; PU	I/O	**GPIO4[7]** — General purpose digital input/output pin.
								O	**USB1_ULPI_STP** — ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
								-	**R** — Function reserved.
								O	**LCD_VD4** — LCD data.
								O	**LCD_PWR** — LCD panel power enable.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**T0_CAP3** — Capture input 3 of timer 0.
P8_8	L1	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								I	**USB1_ULPI_CLK** — ULPI link CLK signal. 60 MHz clock generated by the PHY.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**CGU_OUT0** — CGU spare clock output 0.
								O	**I2S1_TX_MCLK** — I2S1 transmit master clock.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P9_0	T1	x	-	x	-	[3]	I; PU	I/O	**GPIO4[12]** — General purpose digital input/output pin.
								O	**MCABORT** — Motor control PWM, LOW-active fast abort.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**ENET_CRS** — Ethernet Carrier Sense (MII interface).
								-	**R** — Function reserved.
								I/O	**SSP0_SSEL** — Slave Select for SSP0.
P9_1	N6	x	-	x	-	[3]	I; PU	I/O	**GPIO4[13]** — General purpose digital input/output pin.
								O	**MCOA2** — Motor control PWM channel 2, output A.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**I2S0_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
								I	**ENET_RX_ER** — Ethernet receive error (MII interface).
								-	**R** — Function reserved.
								I/O	**SSP0_MISO** — Master In Slave Out for SSP0.
P9_2	N8	x	-	x	-	[3]	I; PU	I/O	**GPIO4[14]** — General purpose digital input/output pin.
								O	**MCOB2** — Motor control PWM channel 2, output B.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**I2S0_TX_SDA** — I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
								I	**ENET_RXD3** — Ethernet receive data 3 (MII interface).
								-	**R** — Function reserved.
								I/O	**SSP0_MOSI** — Master Out Slave in for SSP0.
P9_3	M6	x	-	x	-	[3]	I; PU	I/O	**GPIO4[15]** — General purpose digital input/output pin.
								O	**MCOA0** — Motor control PWM channel 0, output A.
								O	**USB1_IND1** — USB1 Port indicator LED control output 1.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**ENET_RXD2** — Ethernet receive data 2 (MII interface).
								-	**R** — Function reserved.
								O	**U3_TXD** — Transmitter output for USART3.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
P9_4	N10	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								O	**MCOB0** — Motor control PWM channel 0, output B.
								O	**USB1_IND0** — USB1 Port indicator LED control output 0.
								-	**R** — Function reserved.
								I/O	**GPIO5[17]** — General purpose digital input/output pin.
								O	**ENET_TXD2** — Ethernet transmit data 2 (MII interface).
								-	**R** — Function reserved.
								I	**U3_RXD** — Receiver input for USART3.
P9_5	M9	x	-	x	69	[3]	I; PU	-	**R** — Function reserved.
								O	**MCOA1** — Motor control PWM channel 1, output A.
								O	**USB1_VBUS_EN** — USB1 VBUS power enable.
								-	**R** — Function reserved.
								I/O	**GPIO5[18]** — General purpose digital input/output pin.
								O	**ENET_TXD3** — Ethernet transmit data 3 (MII interface).
								-	**R** — Function reserved.
								O	**U0_TXD** — Transmitter output for USART0.
P9_6	L11	x	-	x	72	[3]	I; PU	I/O	**GPIO4[11]** — General purpose digital input/output pin.
								O	**MCOB1** — Motor control PWM channel 1, output B.
								O	**USB1_PWR_FAULT** — USB1 Port power fault signal indicating over-current condition; this signal monitors over-current on the USB1 bus (external circuitry required to detect over-current condition).
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**ENET_COL** — Ethernet Collision detect (MII interface).
								-	**R** — Function reserved.
								I	**U0_RXD** — Receiver input for USART0.
PA_0	L12	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**I2S1_RX_MCLK** — I2S1 receive master clock.
								O	**CGU_OUT1** — CGU spare clock output 1.
								-	**R** — Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PA_1	J14	x	-	x	-	[4]	I; PU	I/O	**GPIO4[8]** — General purpose digital input/output pin.
								I	**QEI_IDX** — Quadrature Encoder Interface INDEX input.
								-	**R** — Function reserved.
								O	**U2_TXD** — Transmitter output for USART2.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PA_2	K15	x	-	x	-	[4]	I; PU	I/O	**GPIO4[9]** — General purpose digital input/output pin.
								I	**QEI_PHB** — Quadrature Encoder Interface PHB input.
								-	**R** — Function reserved.
								I	**U2_RXD** — Receiver input for USART2.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PA_3	H11	x	-	x	-	[4]	I; PU	I/O	**GPIO4[10]** — General purpose digital input/output pin.
								I	**QEI_PHA** — Quadrature Encoder Interface PHA input.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PA_4	G13	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CTOUT_9** — SCT output 9. Match output 1 of timer 2.
								-	**R** — Function reserved.
								I/O	**EMC_A23** — External memory address line 23.
								I/O	**GPIO5[19]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PB_0	B15	x	-	x	-	[3]	I; PU	-	**R —** Function reserved.
								O	**CTOUT_10 —** SCT output 10. Match output 2 of timer 2.
								O	**LCD_VD23 —** LCD data.
								-	**R —** Function reserved.
								I/O	**GPIO5[20] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
PB_1	A14	x	-	x	-	[3]	I; PU	-	**R —** Function reserved.
								I	**USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULP data line direction.
								O	**LCD_VD22 —** LCD data.
								-	**R —** Function reserved.
								I/O	**GPIO5[21] —** General purpose digital input/output pin.
								O	**CTOUT_6 —** SCT output 6. Match output 2 of timer 1.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
PB_2	B12	x	-	x	-	[3]	I; PU	-	**R —** Function reserved.
								I/O	**USB1_ULPI_D7 —** ULPI link bidirectional data line 7.
								O	**LCD_VD21 —** LCD data.
								-	**R —** Function reserved.
								I/O	**GPIO5[22] —** General purpose digital input/output pin.
								O	**CTOUT_7 —** SCT output 7. Match output 3 of timer 1.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
PB_3	A13	x	-	x	-	[3]	I; PU	-	**R —** Function reserved.
								I/O	**USB1_ULPI_D6 —** ULPI link bidirectional data line 6.
								O	**LCD_VD20 —** LCD data.
								-	**R —** Function reserved.
								I/O	**GPIO5[23] —** General purpose digital input/output pin.
								O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
								-	**R —** Function reserved.
								-	**R —** Function reserved.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PB_4	B11	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								I/O	**USB1_ULPI_D5** — ULPI link bidirectional data line 5.
								O	**LCD_VD15** — LCD data.
								-	**R** — Function reserved.
								I/O	**GPIO5[24]** — General purpose digital input/output pin.
								I	**CTIN_5** — SCT input 5. Capture input 2 of timer 2.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PB_5	A12	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								I/O	**USB1_ULPI_D4** — ULPI link bidirectional data line 4.
								O	**LCD_VD14** — LCD data.
								-	**R** — Function reserved.
								I/O	**GPIO5[25]** — General purpose digital input/output pin.
								I	**CTIN_7** — SCT input 7.
								O	**LCD_PWR** — LCD panel power enable.
								-	**R** — Function reserved.
PB_6	A6	x	-	x	-	[6]	I; PU	-	**R** — Function reserved.
								I/O	**USB1_ULPI_D3** — ULPI link bidirectional data line 3.
								O	**LCD_VD13** — LCD data.
								-	**R** — Function reserved.
								I/O	**GPIO5[26]** — General purpose digital input/output pin.
								I	**CTIN_6** — SCT input 6. Capture input 1 of timer 3.
								O	**LCD_VD19** — LCD data.
								-	**R** — Function reserved.
								I	**ADC0_6** — ADC0, input channel 6.
PC_0	D4	x	-	x	-	[6]	I; PU	-	**R** — Function reserved.
								I	**USB1_ULPI_CLK** — ULPI link CLK signal. 60 MHz clock generated by the PHY.
								-	**R** — Function reserved.
								I/O	**ENET_RX_CLK** — Ethernet Receive Clock (MII interface).
								O	**LCD_DCLK** — LCD panel clock.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SD_CLK** — SD/MMC card clock.
								I	**ADC1_1** — ADC1, input channel 1.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PC_1	E4	-	-	x	-	[3]	I; PU	I/O	**USB1_ULPI_D7 —** ULPI link bidirectional data line 7.
								-	**R —** Function reserved.
								I	**U1_RI —** Ring Indicator input for UART 1.
								O	**ENET_MDC —** Ethernet MIIM clock.
								I/O	**GPIO6[0] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								I	**T3_CAP0 —** Capture input 0 of timer 3.
								O	**SD_VOLT0 —** SD/MMC bus voltage select output 0.
PC_2	F6	-	-	x	-	[3]	I; PU	I/O	**USB1_ULPI_D6 —** ULPI link bidirectional data line 6.
								-	**R —** Function reserved.
								I	**U1_CTS —** Clear to Send input for UART 1.
								O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
								I/O	**GPIO6[1] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								O	**SD_RST —** SD/MMC reset signal for MMC4.4 card.
PC_3	F5	-	-	x	-	[6]	I; PU	I/O	**USB1_ULPI_D5 —** ULPI link bidirectional data line 5.
								-	**R —** Function reserved.
								O	**U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
								O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
								I/O	**GPIO6[2] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								O	**SD_VOLT1 —** SD/MMC bus voltage select output 1.
								I	**ADC1_0 —** ADC1, input channel 0.
PC_4	F4	-	-	x	-	[3]	I; PU	-	**R —** Function reserved.
								I/O	**USB1_ULPI_D4 —** ULPI link bidirectional data line 4.
								-	**R —** Function reserved.
									ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
								I/O	**GPIO6[3] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								I	**T3_CAP1 —** Capture input 1 of timer 3.
								I/O	**SD_DAT0 —** SD/MMC data bus line 0.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PC_5	G4	-	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								I/O	**USB1_ULPI_D3** — ULPI link bidirectional data line 3.
								-	**R** — Function reserved.
								O	**ENET_TX_ER** — Ethernet Transmit Error (MII interface).
								I/O	**GPIO6[4]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								I	**T3_CAP2** — Capture input 2 of timer 3.
								I/O	**SD_DAT1** — SD/MMC data bus line 1.
PC_6	H6	-	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								I/O	**USB1_ULPI_D2** — ULPI link bidirectional data line 2.
								-	**R** — Function reserved.
								I	**ENET_RXD2** — Ethernet receive data 2 (MII interface).
								I/O	**GPIO6[5]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								I	**T3_CAP3** — Capture input 3 of timer 3.
								I/O	**SD_DAT2** — SD/MMC data bus line 2.
PC_7	G5	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								I/O	**USB1_ULPI_D1** — ULPI link bidirectional data line 1.
								-	**R** — Function reserved.
								I	**ENET_RXD3** — Ethernet receive data 3 (MII interface).
								I/O	**GPIO6[6]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								O	**T3_MAT0** — Match output 0 of timer 3.
								I/O	**SD_DAT3** — SD/MMC data bus line 3.
PC_8	N4	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								I/O	**USB1_ULPI_D0** — ULPI link bidirectional data line 0.
								-	**R** — Function reserved.
								I	**ENET_RX_DV** — Ethernet Receive Data Valid (RMII/MII interface).
								I/O	**GPIO6[7]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								O	**T3_MAT1** — Match output 1 of timer 3.
								I	**SD_CD** — SD/MMC card detect input.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PC_9	K2	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								I	**USB1_ULPI_NXT** — ULPI link NXT signal. Data flow control signal from the PHY.
								-	**R** — Function reserved.
								I	**ENET_RX_ER** — Ethernet receive error (MII interface).
								I/O	**GPIO6[8]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								O	**T3_MAT2** — Match output 2 of timer 3.
								O	**SD_POW** — <tbd>.
PC_10	M5	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								O	**USB1_ULPI_STP** — ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
								I	**U1_DSR** — Data Set Ready input for UART 1.
								-	**R** — Function reserved.
								I/O	**GPIO6[9]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								O	**T3_MAT3** — Match output 3 of timer 3.
								I/O	**SD_CMD** — SD/MMC command signal.
PC_11	L5	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								I	**USB1_ULPI_DIR** — ULPI link DIR signal. Controls the ULP data line direction.
								I	**U1_DCD** — Data Carrier Detect input for UART 1.
								-	**R** — Function reserved.
								I/O	**GPIO6[10]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SD_DAT4** — SD/MMC data bus line 4.
PC_12	L6	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**U1_DTR** — Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
								-	**R** — Function reserved.
								I/O	**GPIO6[11]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								I/O	**I2S0_TX_SDA** — I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^{2}S-bus specification*.
								I/O	**SD_DAT5** — SD/MMC data bus line 5.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PC_13	M1	-	-	-	-	[3]	I; PU	-	**R —** Function reserved.
								-	**R —** Function reserved.
								O	**U1_TXD —** Transmitter output for UART 1.
								-	**R —** Function reserved.
								I/O	**GPIO6[12] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
								I/O	**SD_DAT6 —** SD/MMC data bus line 6.
PC_14	N1	-	-	-	-	[3]	I; PU	-	**R —** Function reserved.
								-	**R —** Function reserved.
								I	**U1_RXD —** Receiver input for UART 1.
								-	**R —** Function reserved.
								I/O	**GPIO6[13] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
								I/O	**SD_DAT7 —** SD/MMC data bus line 7.
PD_0	N2	-	-	-	-	[3]	I; PU	-	**R —** Function reserved.
								O	**CTOUT_15 —** SCT output 15. Match output 3 of timer 3.
								O	**EMC_DQMOUT2 —** Data mask 2 used with SDRAM and static devices.
								-	**R —** Function reserved.
								I/O	**GPIO6[14] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
PD_1	P1	-	-	-	-	[3]	I; PU	-	**R —** Function reserved.
								-	**R —** Function reserved.
								O	**EMC_CKEOUT2 —** SDRAM clock enable 2.
								-	**R —** Function reserved.
								I/O	**GPIO6[15] —** General purpose digital input/output pin.
								O	**SD_POW —** <tbd>.
								-	**R —** Function reserved.
								-	**R —** Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PD_2	R1	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CTOUT_7** — SCT output 7. Match output 3 of timer 1.
								I/O	**EMC_D16** — External memory data line 16.
								-	**R** — Function reserved.
								I/O	**GPIO6[16]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PD_3	P4	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CTOUT_6** — SCT output 7. Match output 2 of timer 1.
								I/O	**EMC_D17** — External memory data line 17.
								-	**R** — Function reserved.
								I/O	**GPIO6[17]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PD_4	T2	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CTOUT_8** — SCT output 8. Match output 0 of timer 2.
								I/O	**EMC_D18** — External memory data line 18.
								-	**R** — Function reserved.
								I/O	**GPIO6[18]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PD_5	P6	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CTOUT_9** — SCT output 9. Match output 1 of timer 2.
								I/O	**EMC_D19** — External memory data line 19.
								-	**R** — Function reserved.
								I/O	**GPIO6[19]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PD_6	R6	-	-	x	-	[3]	I; PU	-	**R —** Function reserved.
								O	**CTOUT_10 —** SCT output 10. Match output 2 of timer 2.
								I/O	**EMC_D20 —** External memory data line 20.
								-	**R —** Function reserved.
								I/O	**GPIO6[20] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
PD_7	T6	-	-	x	-	[3]	I; PU	-	**R —** Function reserved.
								I	**CTIN_5 —** SCT input 5. Capture input 2 of timer 2.
								I/O	**EMC_D21 —** External memory data line 21.
								-	**R —** Function reserved.
								I/O	**GPIO6[21] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
PD_8	P8	-	-	x	-	[3]	I; PU	-	**R —** Function reserved.
								I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
								I/O	**EMC_D22 —** External memory data line 22.
								-	**R —** Function reserved.
								I/O	**GPIO6[22] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
PD_9	T11	-	-	x	-	[3]	I; PU	-	**R —** Function reserved.
								O	**CTOUT_13 —** SCT output 13. Match output 1 of timer 3.
								I/O	**EMC_D23 —** External memory data line 23.
								-	**R —** Function reserved.
								I/O	**GPIO6[23] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PD_10	P11	-	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								I	**CTIN_1** — SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
								O	**EMC_BLS3** — LOW active Byte Lane select signal 3.
								-	**R** — Function reserved.
								I/O	**GPIO6[24]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PD_11	N9	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**EMC_CS3** — LOW active Chip Select 3 signal.
								-	**R** — Function reserved.
								I/O	**GPIO6[25]** — General purpose digital input/output pin.
								I/O	**USB1_ULPI_D0** — ULPI link bidirectional data line 0.
								O	**CTOUT_14** — SCT output 14. Match output 2 of timer 3.
								-	**R** — Function reserved.
PD_12	N11	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**EMC_CS2** — LOW active Chip Select 2 signal.
								-	**R** — Function reserved.
								I/O	**GPIO6[26]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								O	**CTOUT_10** — SCT output 10. Match output 2 of timer 2.
								-	**R** — Function reserved.
PD_13	T14	x	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								I	**CTIN_0** — SCT input 0. Capture input 0 of timer 0, 1, 2, 3.
								O	**EMC_BLS2** — LOW active Byte Lane select signal 2.
								-	**R** — Function reserved.
								I/O	**GPIO6[27]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								O	**CTOUT_13** — SCT output 13. Match output 1 of timer 3.
								-	**R** — Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PD_14	R13	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**EMC_DYCS2** — SDRAM chip select 2.
								-	**R** — Function reserved.
								I/O	**GPIO6[28]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								O	**CTOUT_11** — SCT output 11. Match output 3 of timer 2.
								-	**R** — Function reserved.
PD_15	T15	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**EMC_A17** — External memory address line 17.
								-	**R** — Function reserved.
								I/O	**GPIO6[29]** — General purpose digital input/output pin.
								I	**SD_WP** — SD/MMC card write protect input.
								O	**CTOUT_8** — SCT output 8. Match output 0 of timer 2.
								-	**R** — Function reserved.
PD_16	R14	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**EMC_A16** — External memory address line 16.
								-	**R** — Function reserved.
								I/O	**GPIO6[30]** — General purpose digital input/output pin.
								O	**SD_VOLT2** — SD/MMC bus voltage select output 2.
								O	**CTOUT_12** — SCT output 12. Match output 0 of timer 3.
								-	**R** — Function reserved.
PE_0	P14	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**EMC_A18** — External memory address line 18.
								I/O	**GPIO7[0]** — General purpose digital input/output pin.
								O	**CAN1_TD** — CAN1 transmitter output.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PE_1	N14	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**EMC_A19** — External memory address line 19.
								I/O	**GPIO7[1]** — General purpose digital input/output pin.
								I	**CAN1_RD** — CAN1 receiver input.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PE_2	M14	x	-	x	-	[3]	I; PU	I	**ADCTRIG0** — ADC trigger input 0.
								I	**CAN0_RD** — CAN receiver input.
								-	**R** — Function reserved.
								I/O	**EMC_A20** — External memory address line 20.
								I/O	**GPIO7[2]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PE_3	K12	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CAN0_TD** — CAN transmitter output.
								I	**ADCTRIG1** — ADC trigger input 1.
								I/O	**EMC_A21** — External memory address line 21.
								I/O	**GPIO7[3]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PE_4	K13	x	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								I	**NMI** — External interrupt input to NMI.
								-	**R** — Function reserved.
								I/O	**EMC_A22** — External memory address line 22.
								I/O	**GPIO7[4]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PE_5	N16	-	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CTOUT_3** — SCT output 3. Match output 3 of timer 0.
								O	**U1_RTS** — Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
								I/O	**EMC_D24** — External memory data line 24.
								I/O	**GPIO7[5]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PE_6	M16	-	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CTOUT_2** — SCT output 2. Match output 2 of timer 0.
								I	**U1_RI** — Ring Indicator input for UART 1.
								I/O	**EMC_D25** — External memory data line 25.
								I/O	**GPIO7[6]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PE_7	F15	-	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CTOUT_5** — SCT output 5. Match output 1 of timer 1.
								I	**U1_CTS** — Clear to Send input for UART1.
								I/O	**EMC_D26** — External memory data line 26.
								I/O	**GPIO7[7]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PE_8	F14	-	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CTOUT_4** — SCT output 4. Match output 0 of timer 0.
								I	**U1_DSR** — Data Set Ready input for UART 1.
								I/O	**EMC_D27** — External memory data line 27.
								I/O	**GPIO7[8]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PE_9	E16	-	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								I	**CTIN_4** — SCT input 4. Capture input 2 of timer 1.
								I	**U1_DCD** — Data Carrier Detect input for UART 1.
								I/O	**EMC_D28** — External memory data line 28.
								I/O	**GPIO7[9]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PE_10	E14	-	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								I	**CTIN_3** — SCT input 3. Capture input 1 of timer 1.
								O	**U1_DTR** — Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
								I/O	**EMC_D29** — External memory data line 29.
								I/O	**GPIO7[10]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PE_11	D16	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CTOUT_12** — SCT output 12. Match output 0 of timer 3.
								O	**U1_TXD** — Transmitter output for UART 1.
								I/O	**EMC_D30** — External memory data line 30.
								I/O	**GPIO7[11]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PE_12	D15	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CTOUT_11** — SCT output 11. Match output 3 of timer 2.
								I	**U1_RXD** — Receiver input for UART 1.
								I/O	**EMC_D31** — External memory data line 31.
								I/O	**GPIO7[12]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PE_13	G14	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CTOUT_14** — SCT output 14. Match output 2 of timer 3.
								I/O	**I2C1_SDA** — I^2C1 data input/output (this pin does not use a specialized I^2C pad).
								O	**EMC_DQMOUT3** — Data mask 3 used with SDRAM and static devices.
								I/O	**GPIO7[13]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PE_14	C15	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**EMC_DYCS3** — SDRAM chip select 3.
								I/O	**GPIO7[14]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PE_15	E13	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								O	**CTOUT_0** — SCT output 0. Match output 0 of timer 0.
								I/O	**I2C1_SCL** — I^2C1 clock input/output (this pin does not use a specialized I^2C pad).
								O	**EMC_CKEOUT3** — SDRAM clock enable 3.
								I/O	**GPIO7[15]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PF_0	D12	-	-	-	-	[3]	I;IA	I/O	**SSP0_SCK** — Serial clock for SSP0.
								I	**GP_CLKIN** — General purpose clock input to the CGU.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**I2S1_TX_MCLK** — I2S1 transmit master clock.

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PF_1	E11	-	-	-	-	[3]	I; PU	-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SSP0_SSEL** — Slave Select for SSP0.
								-	**R** — Function reserved.
								I/O	**GPIO7[16]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PF_2	D11	-	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								O	**U3_TXD** — Transmitter output for USART3.
								I/O	**SSP0_MISO** — Master In Slave Out for SSP0.
								-	**R** — Function reserved.
								I/O	**GPIO7[17]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PF_3	E10	-	-	x	-	[3]	I; PU	-	**R** — Function reserved.
								I	**U3_RXD** — Receiver input for USART3.
								I/O	**SSP0_MOSI** — Master Out Slave in for SSP0.
								-	**R** — Function reserved.
								I/O	**GPIO7[18]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
PF_4	D10	x	x	x	120	[3]	I;IA	I/O	**SSP1_SCK** — Serial clock for SSP1.
								I	**GP_CLKIN** — General purpose clock input to the CGU.
								O	**TRACECLK** — Trace clock.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**I2S0_TX_MCLK** — I2S transmit master clock.
								I/O	**I2S0_RX_SCK** — I2S transmit clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^{2}S-bus specification*.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PF_5	E9	-	-	x	-	[6]	I; PU	-	**R** — Function reserved.
								I/O	**U3_UCLK** — Serial clock input/output for USART3 in synchronous mode.
								I/O	**SSP1_SSEL** — Slave Select for SSP1.
								O	**TRACEDATA[0]** — Trace data, bit 0.
								I/O	**GPIO7[19]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**ADC1_4** — ADC1, input channel 4.
PF_6	E7	-	-	x	-	[6]	I; PU	-	**R** — Function reserved.
								I/O	**U3_DIR** — RS-485/EIA-485 output enable/direction control for USART3.
								I/O	**SSP1_MISO** — Master In Slave Out for SSP1.
								O	**TRACEDATA[1]** — Trace data, bit 1.
								I/O	**GPIO7[20]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**I2S1_TX_SDA** — I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
								I	**ADC1_3** — ADC1, input channel 3.
PF_7	B7	-	-	x	-	[6]	I; PU	-	**R** — Function reserved.
								I/O	**U3_BAUD** — <tbd> for USART3.
								I/O	**SSP1_MOSI** — Master Out Slave in for SSP1.
								O	**TRACEDATA[2]** — Trace data, bit 2.
								I/O	**GPIO7[21]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**I2S1_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
								I/O	**ADC1_7** — ADC1, input channel 7 or band gap output.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
PF_8	E6	-	-	x	-	[6]	I; PU	-	**R** — Function reserved.
								I/O	**U0_UCLK** — Serial clock input/output for USART0 in synchronous mode.
								I	**CTIN_2** — SCT input 2. Capture input 2 of timer 0.
								O	**TRACEDATA[3]** — Trace data, bit 3.
								I/O	**GPIO7[22]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**ADC0_2** — ADC0, input channel 2.
PF_9	D6	-	-	x	-	[6]	I; PU	-	**R** — Function reserved.
								I/O	**U0_DIR** — RS-485/EIA-485 output enable/direction control for USART0.
								O	**CTOUT_1** — SCT output 1. Match output 1 of timer 0.
								-	**R** — Function reserved.
								I/O	**GPIO7[23]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I	**ADC1_2** — ADC1, input channel 2.
PF_10	A3	-	-	x	-	[6]	I; PU	-	**R** — Function reserved.
								O	**U0_TXD** — Transmitter output for USART0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**GPIO7[24]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								I	**SD_WP** — SD/MMC card write protect input.
								-	**R** — Function reserved.
								I	**ADC0_5** — ADC0, input channel 5.
PF_11	A2	-	-	x	-	[6]	I; PU	-	**R** — Function reserved.
								I	**U0_RXD** — Receiver input for USART0.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**GPIO7[25]** — General purpose digital input/output pin.
								-	**R** — Function reserved.
								O	**SD_VOLT2** — SD/MMC bus voltage select output 2.
								-	**R** — Function reserved.
								I	**ADC1_5** — ADC1, input channel 5.
Clock pins									

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
CLK0	N5	x	x	x	45	[5]	O; PU	O	**EMC_CLK0** — SDRAM clock 0.
								O	**CLKOUT** — Clock output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SD_CLK** — SD/MMC card clock.
								O	**EMC_CLK01** — SDRAM clock 0 and clock 1 combined.
								I/O	**SSP1_SCK** — Serial clock for SSP1.
								I	**ENET_TX_CLK (ENET_REF_CLK)** — Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
CLK1	T10	x	-	-	-	[5]	O; PU	O	**EMC_CLK1** — SDRAM clock 1.
								O	**CLKOUT** — Clock output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**CGU_OUT0** — CGU spare clock output 0.
								-	**R** — Function reserved.
								O	**I2S1_TX_MCLK** — I2S1 transmit master clock.
CLK2	D14	x	x	x	99	[5]	O; PU	O	**EMC_CLK3** — SDRAM clock 3.
								O	**CLKOUT** — Clock output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								I/O	**SD_CLK** — SD/MMC card clock.
								O	**EMC_CLK23** — SDRAM clock 2 and clock 3 combined.
								O	**I2S0_TX_MCLK** — I2S transmit master clock.
								I/O	**I2S1_RX_SCK** — Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
CLK3	P12	x	-	-	-	[5]	O; PU	O	**EMC_CLK2** — SDRAM clock 2.
								O	**CLKOUT** — Clock output pin.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								-	**R** — Function reserved.
								O	**CGU_OUT1** — CGU spare clock output 1.
								-	**R** — Function reserved.
								I/O	**I2S1_RX_SCK** — Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
Debug pins									

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Table 107. Pin description *...continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
DBGEN	L4	x	x	x	28	[3]	I; PD	I	JTAG interface control signal. Also used for boundary scan.
TCK/SWDCLK	J5	x	x	x	27	[3]	I; F	I	Test Clock for JTAG interface (default) or Serial Wire (SW) clock.
$\overline{\text{TRST}}$	M4	x	x	x	29	[3]	I; PU	I	Test Reset for JTAG interface.
TMS/SWDIO	K6	x	x	x	30	[3]	I; PU	I	Test Mode Select for JTAG interface (default) or SW debug data input/output.
TDO/SWO	K5	x	x	x	31	[3]	O; PU	O	Test Data Out for JTAG interface (default) or SW trace output.
TDI	J4	x	x	x	26	[3]	I; PU	I	Test Data In for JTAG interface.
USB0 pins									
USB0_DP	F2	x	x	x	18	[7]	-	I/O	USB0 bidirectional D+ line.
USB0_DM	G2	x	x	x	20	[7]	-	I/O	USB0 bidirectional D– line.
USB0_VBUS	F1	x	x	x	21	[7]	-	I/O	VBUS pin (power on USB cable).
USB0_ID	H2	x	x	x	22	[8]	-	I	Indicates to the transceiver whether connected to an A-device (LOW) or a B-device (HIGH).
USB0_RREF	H1	x	x	x	24	[8]	-		12.0 kΩ (accuracy 1%) on-board resistor to ground for current reference.
USB1 pins									
USB1_DP	F12	x	x	x	89	[9]	-	I/O	USB1 bidirectional D+ line.
USB1_DM	G12	x	x	x	90	[9]	-	I/O	USB1 bidirectional D– line.
I²C-bus pins									
I2C0_SCL	L15	x	x	x	92	[10]	I; F	I/O	I²C clock input/output. Open-drain output (for I²C-bus compliance).
I2C0_SDA	L16	x	x	x	93	[10]	I; F	I/O	I²C data input/output. Open-drain output (for I²C-bus compliance).
Reset and wake-up pins									
$\overline{\text{RESET}}$	D9	x	x	x	128	[11]	I; IA	I	External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
WAKEUP0	A9	x	x	x	130	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.
WAKEUP1	A10	x	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.
WAKEUP2	C9	x	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.
WAKEUP3	D8	x	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.
ADC pins									
ADC0_0/ ADC1_0/DAC	E3	x	x	x	6	[8]	I; IA	I	ADC input channel 0. Shared between 10-bit ADC0/1 and DAC.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
ADC0_1/ ADC1_1	C3	x	x	x	2	[8]	I; IA	I	ADC input channel 1. Shared between 10-bit ADC0/1.
ADC0_2/ ADC1_2	A4	x	x	x	143	[8]	I; IA	I	ADC input channel 2. Shared between 10-bit ADC0/1.
ADC0_3/ ADC1_3	B5	x	x	x	139	[8]	I; IA	I	ADC input channel 3. Shared between 10-bit ADC0/1.
ADC0_4/ ADC1_4	C6	x	-	x	138	[8]	I; IA	I	ADC input channel 4. Shared between 10-bit ADC0/1.
ADC0_5/ ADC1_5	B3	x	-	x	144	[8]	I; IA	I	ADC input channel 5. Shared between 10-bit ADC0/1.
ADC0_6/ ADC1_6	A5	x	-	x	142	[8]	I; IA	I	ADC input channel 6. Shared between 10-bit ADC0/1.
ADC0_7/ ADC1_7	C5	x	-	x	136	[8]	I; IA	I	ADC input channel 7. Shared between 10-bit ADC0/1.
RTC									
RTC_ALARM	A11	x	x	x	129	[11]	-	O	RTC controlled output.
RTCX1	A8	x	x	x	125	[8]	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	B8	x	x	x	126	[8]	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
Crystal oscillator pins									
XTAL1	D1	x	x	x	12	[8]	-	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	E1	x	x	x	13	[8]	-	O	Output from the oscillator amplifier.
Power and ground pins									
USB0_VDDA 3V3_DRIVER	F3	x	x	x	16		-	-	Separate analog 3.3 V power supply for driver.
USB0 _VDDA3V3	G3	x	x	x	17		-	-	USB 3.3 V separate power supply voltage.
USB0_VSSA _TERM	H3	x	x	x	19		-	-	Dedicated analog ground for clean reference for termination resistors.
USB0_VSSA _REF	G1	x	x	x	23		-	-	Dedicated clean analog ground for generation of reference currents and voltages.
VDDA	B4	x	x	x	137		-	-	Analog power supply and ADC reference voltage.
VBAT	B10	x	x	x	127		-	-	RTC power supply: 3.3 V on this pin supplies power to the RTC.
VDDREG	F10, F9, L8, L7	x	x	x	94, 131, 59, 25			-	Main regulator power supply.
VPP	E8	x	x	x	x		-	-	OTP programming voltage.

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Table 107. Pin description *…continued*

Symbol	LBGA256	BGA180[1]	BGA100[1]	LQFP208[1]	LQFP144		Reset state [2]	Type	Description
VDDIO	D7, E12, F7, F8, G10, H10, J6, J7, K7, L9, L10, N7, N13	x	x	x	5, 36, 41, 71, 77, 107, 111, 141		-	-	I/O power supply.
VSS	G9, H7, J10, J11, K8	x	x	x	-	[12]	-	-	Ground.
VSSIO	C4, D13, G6, G7, G8, H8, H9, J8, J9, K9, K10, M13, P7, P13	x	x	x	4, 40, 76, 109	[12]	-	-	Ground.
VSSA	B2	x	x	x	135		-	-	Analog ground.
Not connected									
-	B9						-	-	n.c.

[1] x = available; - = not pinned out.

[2] I = input, O = output, IA = inactive; PU = pull-up enabled (weak pull-up resistor pulls up pin to $V_{DD(IO)}$); F = floating

[3] 5 V tolerant pad with 15 ns glitch filter; provides digital I/O functions with TTL levels and hysteresis; normal drive strength.

[4] 5 V tolerant pad with 15 ns glitch filter providing digital I/O functions with TTL levels, and hysteresis; high drive strength.

[5] 5 V tolerant pad with 15 ns glitch filter providing high-speed digital I/O functions with TTL levels and hysteresis.

[6] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input or output. When configured as a ADC input or DAC output, the pin is not 5 V tolerant and the digital section of the pad must be disabled by setting the pin to an input function and disabling the pull-up resistor through the pin's SFSP register.

[7] 5 V tolerant transparent analog pad.

[8] Transparent analog pad. Not 5 V tolerant.

[9] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

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[10] Open-drain 5 V tolerant digital I/O pad, compatible with I2C-bus 400 kHz specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I2C-bus is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[11] 5 V tolerant pad with 20 ns glitch filter; provides digital I/O functions with open-drain output with weak pull-up resistor and hysteresis.

[12] For the LQFP144 package, VSSIO and VSS are connected to a common ground plane.

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13.1 How to read this chapter

Remark: This chapter describes parts LPC1850/30/20/10 Rev ‘A’ and parts LPC18xx (with on-chip flash). For a description of the SCU for parts LPC1850/30/20/10 Rev ‘-’, see Section 42.7.

The following peripherals are not available on all parts, and the corresponding bit values that select those functions in the SFSP registers are reserved:

- Ethernet: available on LPC1850/30.
- USB0: available on LPC1850/30/20.
- USB1: available on LPC1850/30.

13.2 Basic configuration

The SCU is configured as follows:

- See Table 108 for clocking and power control.
- The SCU is reset by the SCU_RST (reset # 9).

Table 108. SCU clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to SCU register interface	BASE_M3_CLK	CLK_M3_SCU	150 MHz

13.3 General description

The system control unit determines the function and electrical mode of the digital pins. By default function 0 is selected for all pins with pull-up enabled.

Remark: Analog I/Os for the ADCs and the DAC as well as several USB functions reside on separate pins and are not controlled through the SCU.

13.3.1 Digital pin function

The FUNC bits in the SFSX_Y registers control the function of each pin. If the function is GPIO, the GPIOnDIR registers determine whether the pin is configured as an input or output (see Table 280). For any peripheral function, the pin direction is controlled automatically depending on the pin’s functionality. The GPIOnDIR registers have no effect for peripheral functions.

13.3.2 Digital pin mode

The MODE bits in the SFSX_Y registers allow the selection of on-chip pull-up or pull-down resistors for each pin or select the repeater mode.

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The possible on-chip resistor configurations are pull-up enabled, pull-down enabled, or no pull-up/pull-down. The default value is pull-up enabled.

The repeater mode enables the pull-up resistor if the pin is at a logic HIGH and enables the pull-down resistor if the pin is at a logic LOW. This causes the pin to retain its last known state if it is configured as an input and is not driven externally. Repeater mode may typically be used to prevent a pin from floating (and potentially using significant power if it floats to an indeterminate state) if it is temporarily not driven.

13.3.3 I^{2}C0-bus pins

The EHS bits of the SFSI2C0 register (Table 120) configure different I^{2}C-modes:

- Standard mode/Fast-mode I^{2}C (this includes an open-drain output according to the I^{2}C-bus specification).
- Fast-mode Plus and High-speed mode (this includes an open-drain output according to the I^{2}C-bus specification).

13.3.4 USB1 DP1/DM1 pins

The input signal to the USB1 is controlled by the SFSUSB register (Table 119). The USB_ESEA bit in this register must be set to one to enable the USB1 block.

13.3.5 EMC signal delay control

The SCU contains a programmable delay control for all EMC input and output data, address, and control signals. For detail on use of the EMC delay modes, see Table 271.

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13.3.6 Pin multiplexing

Table 109. Pin multiplexing

Symbol	LBGA256	BGA180	BGA100	LQFP208	LQFP144	Function level 0	1	2	3	4	5	6	7	8	Reference
P0_0	L3	x	x	x	32	GPIO0[0]	SSP1_ MISO	ENET_ RXD1	R	R	R	I2S0_ TX_WS	I2S1_ TX_WS	-	Table 111
P0_1	M2	x	x	x	34	GPIO0[1]	SSP1_ MOSI	ENET_ COL	R	R	R	ENET_ TX_EN	I2S1_ TX_SDA	-	Table 111
P1_0	P2	x	x	x	38	GPIO0[4]	CTIN_3	EMC_A5	R	R	SSP0_ SSEL	R	R	-	Table 111
P1_1	R2	x	x	x	42	GPIO0[8]	CTOUT_7	EMC_A6	R	R	SSP0_ MISO	R	R	-	Table 111
P1_2	R3	x	x	x	43	GPIO0[9]	CTOUT_6	EMC_A7	R	R	SSP0_ MOSI	R	R	-	Table 111
P1_3	P5	x	x	x	44	GPIO0[10]	CTOUT_8	R	EMC_OE	USB0_ IND1	SSP1_ MISO	R	SD_RST	-	Table 111
P1_4	T3	x	x	x	47	GPIO0[11]	CTOUT_9	R	EMC_BLS0	USB0_ IND0	SSP1_ MOSI	R	SD_ VOLT1	-	Table 111
P1_5	R5	x	x	x	48	GPIO1[8]	CTOUT_10	R	EMC_CS0	USB0_ PWR_ FAULT	SSP1_ SSEL	R	SD_POW	-	Table 111
P1_6	T4	x	x	x	49	GPIO1[9]	CTIN_5	R	EMC_WE	R	R	R	SD_CMD		Table 111
P1_7	T5	x	x	x	50	GPIO1[0]	U1_DSR	CTOUT_13	EMC_D0	USB0_ PWR_EN	R	R	R		Table 111
P1_8	R7	x	x	x	51	GPIO1[1]	U1_DTR	CTOUT_12	EMC_D1	R	R	R	SD_ VOLT0	-	Table 111
P1_9	T7	x	x	x	52	GPIO1[2]	U1_RTS	CTOUT_11	EMC_D2	R	R	R	SD_D0	-	Table 111
P1_10	R8	x	x	x	53	GPIO1[3]	U1_RI	CTOUT_14	EMC_D3	R	R	R	SD_D1	-	Table 111
P1_11	T9	x	x	x	55	GPIO1[4]	U1_CTS	CTOUT_15	EMC_D4	R	R	R	SD_D2	-	Table 111
P1_12	R9	x	x	x	56	GPIO1[5]	U1_DCD	R	EMC_D5	T0_CAP1	R	R	SD_D3	-	Table 111
P1_13	R10	x	x	x	60	GPIO1[6]	U1_TXD	R	EMC_D6	T0_CAP0	R	R	SD_CD	-	Table 111
P1_14	R11	x	x	x	61	GPIO1[7]	U1_RXD	R	EMC_ D7	T0_MAT2	R	R	R	-	Table 111

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Table 109. Pin multiplexing

Symbol	LBGA256	BGA180	BGA100	LQFP208	LQFP144	Function level									Reference
						0	1	2	3	4	5	6	7	8	
P1_15	T12	x	x	x	62	GPIO0[2]	U2_TXD	R	ENET_ RXD0	T0_MAT1	R	R	R	-	Table 111
P1_16	M7	x	x	x	64	GPIO0[3]	U2_RXD	R	ENET_ CRS	T0_MAT0	R	R	ENET_ RX_DV	-	Table 111
P1_17	M8	x	x	x	66	GPIO0[12]	U2_UCLK	R	ENET_ MDIO	T0_CAP3	CAN1_TD	R	R	-	Table 112
P1_18	N12	x	x	x	67	GPIO0[13]	U2_DIR	R	ENET_ TXD0	T0_MAT3	CAN1_RD	R	R	-	Table 111
P1_19	M11	x	x	x	68	ENET_ TX_CLK (ENET_R EF_CLK)	SSP1_SCK	R	R	CLKOUT	R	I2S0_RX_ MCLK	I2S1_TX_ SCK	-	Table 111
P1_20	M10	x	x	x	70	GPIO0[15]	SSP1_ SSEL	R	ENET_ TXD1	T0_CAP2	R	R	R	-	Table 111
P2_0	T16	x	x	x	75	R	U0_TXD	EMC_A13	USB0_ PWR_EN	GPIO5[0]	R	T3_CAP0	ENET_ MDC	-	Table 111
P2_1	N15	x	x	x	81	R	U0_RXD	EMC_A12	USB0_ PWR_ FAULT	GPIO5[1]	R	T3_CAP1	R	-	Table 111
P2_2	M15	x	x	x	84	R	U0_UCLK	EMC_A11	USB0_ IND1	GPIO5[2]	CTOUT_6	T3_CAP2	R	-	Table 111
P2_3	J12	x	x	x	87	R	I2C1_SDA	U3_TXD	CTIN_1	GPIO5[3]	R	T3_MAT0	USB0_ PWR_EN	-	Table 112
P2_4	K11	x	x	x	88	R	I2C1_SCL	U3_RXD	CTIN_0	GPIO5[4]	R	T3_MAT1	USB0_ PWR_ FAULT	-	Table 112
P2_5	K14	x	x	x	91	R	CTIN_2	USB1_ VBUS	ADCTRIG1	GPIO5[5]	R	T3_MAT2	USB0_ IND0	-	Table 112
P2_6	K16	x	x	x	95	R	U0_DIR	EMC_A10	USB0_ IND0	GPIO5[6]	CTIN_7	T3_CAP3	R	-	Table 111
P2_7	H14	x	x	x	96	GPIO0[7]	CTOUT_1	U3_UCLK	EMC_A9	R	R	T3_MAT3	R	-	Table 111
P2_8	J16	x	x	x	98	Boot pin	CTOUT_0	U3_DIR	EMC_A8	GPIO5[7]	R	R	R	-	Table 111

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Table 109. Pin multiplexing

Symbol	LBGA256	BGA180	BGA100	LQFP208	LQFP144	Function level 0	1	2	3	4	5	6	7	8	Reference
P2_9	H16	x	x	x	102	GPIO1[10]	CTOUT_3	U3_BAUD	EMC_A0	R	R	R	R	-	Table 111
P2_10	G16	x	x	x	104	GPIO0[14]	CTOUT_2	U2_TXD	EMC_A1	R	R	R	R	-	Table 111
P2_11	F16	x	x	x	105	GPIO1[11]	CTOUT_5	U2_RXD	EMC_A2	R	R	R	R	-	Table 111
P2_12	E15	x	x	x	106	GPIO1[12]	CTOUT_4	R	EMC_A3	R	R	R	U2_UCLK	-	Table 111
P2_13	C16	x	x	x	108	GPIO1[13]	CTIN_4	R	EMC_A4	R	R	R	U2_DIR	-	Table 111
P3_0	F13	x	x	x	112	I2S0_RX_ SCK	I2S0_RX_ MCLK	I2S0_TX_ SCK	I2S0_TX_ MCLK	SSP0_ SCK	R	R	R	-	Table 111
P3_1	G11	x	x	x	114	I2S0_TX_ WS	I2S0_RX_ WS	CAN0_RD	USB1_ IND1	GPIO5[8]	R	LCD_VD15	R	-	Table 111
P3_2	F11	x	x	x	116	I2S0_TX_ SDA	I2S0_RX_ SDA	CAN0_TD	USB1_ IND0	GPIO5[9]	R	LCD_VD14	R	-	Table 111
P3_3	B14	x	x	x	118	R	R	SSP0_SCK	SPIFI_SCK	CGU_ OUT1	R	I2S0_TX_ MCLK	I2S1_TX_ SCK	-	Table 111
P3_4	A15	x	x	x	119	GPIO1[14]	R	R	SPIFI_ SIO3	U1_TXD	I2S0_TX_ WS	I2S1_RX_ SDA	LCD__VD 13	-	Table 111
P3_5	C12	x	x	x	121	GPIO1[15]	R	R	SPIFI_ SIO2	U1_RXD	I2S0_TX_ SDA	I2S1_RX_ WS	LCD_VD1 2	-	Table 111
P3_6	B13	x	x	x	122	GPIO0[6]	R	SSP0_ SSEL	SPIFI_ MISO	R	SSP0_ MISO	R	R	-	Table 111
P3_7	C11	x	x	x	123	R	R	SSP0_ MISO	SPIFI_ MOSI	GPIO5[10]	SSP0_ MOSI	R	R	-	Table 111
P3_8	C10	x	x	x	124	R	R	SSP0_ MOSI	SPIFI_CS	GPIO5[11]	SSP0_ SSEL	R	R	-	Table 111
P4_0	D5	x	-	x	1	GPIO2[0]	MCOA0	NMI	R	R	LCD_ VD13	U3_UCLK	R	-	Table 111
P4_1	A1	x	-	x	3	GPIO2[1]	CTOUT_1	LCD_VD0	R	R	LCD_ VD19	U3_TXD	ENET_ COL	ADC0_1	Table 111Table 114
P4_2	D3	x	-	x	8	GPIO2[2]	CTOUT_0	LCD_VD3	R	R	LCD_ VD12	U3_RXD	R	-	Table 111
P4_3	C2	x	-	x	7	GPIO2[3]	CTOUT_3	LCD_VD2	R	R	LCD_ VD21	U3_BAUD	R	ADC0_0	Table 111Table 114

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Table 109. Pin multiplexing

Symbol	LBGA256	BGA180	BGA100	LQFP208	LQFP144	Function level 0	1	2	3	4	5	6	7	8	Reference
P4_4	B1	x	-	x	9	GPIO2[4]	CTOUT_2	LCD_VD1	R	R	LCD_VD20	U3_DIR	R	DAC	Table 111Table 118
P4_5	D2	x	-	x	10	GPIO2[5]	CTOUT_5	LCD_FP	R	R	R	R	R	-	Table 111
P4_6	C1	x	-	x	11	GPIO2[6]	CTOUT_4	LCD_ENAB /LCD_M	R	R	R	R	R	-	Table 111
P4_7	H4	x	-	x	14	LCD_DCLK	GP_CLKIN	R	R	R	R	I2S1_TX_SCK	I2S0_TX_SCK	-	Table 111
P4_8	E2	x	-	x	15	R	CTIN_5	LCD_VD9	R	GPIO5[12]	LCD_VD22	CAN1_TD	R	-	Table 111
P4_9	L2	x	-	x	33	R	CTIN_6	LCD_VD11	R	GPIO5[13]	LCD_VD15	CAN1_RD	R	-	Table 111
P4_10	M3	x	-	x	35	R	CTIN_2	LCD_VD10	R	GPIO5[14]	LCD_VD14	R	R	-	Table 111
P5_0	N3	x	-	x	37	GPIO2[9]	MCOB2	EMCEMC_D12	R	U1_DSR	T1_CAP0	R	R	-	Table 111
P5_1	P3	x	-	x	39	GPIO2[10]	MCI2	EMC_D13	R	U1_DTR	T1_CAP1	R	R	-	Table 111
P5_2	R4	x	-	x	46	GPIO2[11]	MCI1	EMC_D14	R	U1_RTS	T1_CAP2	R	R	-	Table 111
P5_3	T8	x	-	x	54	GPIO2[12]	MCI0	EMC_D15	R	U1_RI	T1_CAP3	R	R	-	Table 111
P5_4	P9	x	-	x	57	GPIO2[13]	MCOB0	EMC_D8	R	U1_CTS	T1_MAT0	R	R	-	Table 111
P5_5	P10	x	-	x	58	GPIO2[14]	MCOA1	EMC_D9	R	U1_DCD	T1_MAT1	R	R	-	Table 111
P5_6	T13	x	-	x	63	GPIO2[15]	MCOB1	EMC_D10	R	U1_TXD	T1_MAT2	R	R	-	Table 111
P5_7	R12	x	-	x	65	GPIO2[7]	MCOA2	EMC_D11	R	U1_RXD	T1_MAT3	R	R	-	Table 111
P6_0	M12	x	x	x	73	R	I2S0_RX_MCLK	R	R	I2S0_RX_SCK	R	R	R	-	Table 111
P6_1	R15	x	x	x	74	GPIO3[0]	EMC_DYCS1	U0_UCLK	I2S0_RX_WS	R	T2_CAP0	R	R	-	Table 111
P6_2	L13	x	x	x	78	GPIO3[1]	EMC_CKEOUT1	U0_DIR	I2S0_RX_SDA	R	T2_CAP1	R	R	-	Table 111
P6_3	P15	x	-	x	79	GPIO3[2]	USB0_PWR_EN	R	EMC_CS1	R	T2_CAP2	R	R	-	Table 111
P6_4	R16	x	x	x	80	GPIO3[3]	CTIN_6	U0_TXD	EMC_CAS	R	R	R	R	-	Table 111

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Table 109. Pin multiplexing

Symbol	LBGA256	BGA180	BGA100	LQFP208	LQFP144	Function level 0	1	2	3	4	5	6	7	8	Reference
P6_5	P16	x	x	x	82	GPIO3[4]	CTOUT_6	U0_RXD	EMC_RAS	R	R	R	R	-	Table 111
P6_6	L14	x	-	x	83	GPIO0[5]	EMC_ BLS1	R	USB0_ PWR_ FAULT	R	T2_CAP3	R	R	-	Table 111
P6_7	J13	x	-	x	85	R	EMC_A15	R	USB0_ IND1	GPIO5[15]	T2_MAT0	R	R	-	Table 111
P6_8	H13	x	-	x	86	R	EMC_A14	R	USB0_ IND0	GPIO5[16]	T2_MAT1	R	R	-	Table 111
P6_9	J15	x	x	x	97	GPIO3[5]	R	R	EMC_ DYCS0	R	T2_MAT2	R	R	-	Table 111
P6_10	H15	x	-	x	100	GPIO3[6]	MCABORT	R	EMC_ DQMOUT1	R	R	R	R	-	Table 111
P6_11	H12	x	x	x	101	GPIO3[7]	R	R	EMC_ CKEOUT0	R	T2_MAT3	R	R	-	Table 111
P6_12	G15	x	-	x	103	GPIO2[8]	CTOUT_7	R	EMC_ DQMOUT0	R	R	R	R	-	Table 111
P7_0	B16	x	-	x	110	GPIO3[8]	CTOUT_14	R	LCD_LE	R	R	R	R	-	Table 111
P7_1	C14	x	-	x	113	GPIO3[9]	CTOUT_15	I2S0_TX_ WS	LCD_VD19	LCD_VD7	R	U2_TXD	R	-	Table 111
P7_2	A16	x	-	x	113	GPIO3[10]	CTIN_4	I2S0_TX_ SDA	LCD_VD18	LCD_VD6	R	U2_RXD	R	-	Table 111
P7_3	C13	x	-	x	117	GPIO3[11]	CTIN_3	R	LCD_VD17	LCD_VD5	R	R	R	-	Table 111
P7_4	C8	x	-	x	132	GPIO3[12]	CTOUT_13	R	LCD_VD16	LCD_VD4	TRACE DATA[0]	R	R	ADC0_4	Table 111Table 114
P7_5	A7	x	-	x	133	GPIO3[13]	CTOUT_12	R	LCD_VD8	LCD_ VD23	TRACE DATA[1]	R	R	ADC0_3	Table 111Table 114
P7_6	C7	x	-	x	134	GPIO3[14]	CTOUT_11	R	LCD_LP	R	TRACE DATA[2]	R	R	-	Table 111
P7_7	B6	x	-	x	140	GPIO3[15]	CTOUT_8	R	LCD_PWR	R	TRACE DATA[3]	ENET_ MDC	R	ADC1_6	Table 111Table 116

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Table 109. Pin multiplexing

Symbol	LBGA256	BGA180	BGA100	LQFP208	LQFP144	Function level 0	1	2	3	4	5	6	7	8	Reference
P8_0	E5	x	-	x	-	GPIO4[0]	USB0_ PWR_ FAULT	R	MCI2	R	R	R	T0_MAT0	-	Table 112
P8_1	H5	x	-	x	-	GPIO4[1]	USB0_ IND1	R	MCI1	R	R	R	T0_MAT1	-	Table 112
P8_2	K4	x	-	x	-	GPIO4[2]	USB0_ IND0	R	MCI0	R	R	R	T0_MAT2	-	Table 112
P8_3	J3	x	-	x	-	GPIO4[3]	USB1_ ULPI_D2	R	LCD_VD12	LCD_ VD19	R	R	T0_MAT3	-	Table 111
P8_4	J2	x	-	x	-	GPIO4[4]	USB1_ ULPI_D1	R	LCD_VD7	LCD_ VD16	R	R	T0_CAP0	-	Table 111
P8_5	J1	x	-	x	-	GPIO4[5]	USB1_ ULPI_D0	R	LCD_VD6	LCD_VD8	R	R	T0_CAP1	-	Table 111
P8_6	K3	x	-	x	-	GPIO4[6]	USB1_ ULPI_NXT	R	LCD_VD5	LCD_LP	R	R	T0_CAP2	-	Table 111
P8_7	K1	x	-	x	-	GPIO4[7]	USB1_ ULPI_STP	R	LCD_VD4	LCD_ PWR	R	R	T0_CAP3	-	Table 111
P8_8	L1	x	-	x	-	R	USB1_ ULPI_CLK	R	R	R	R	CGU_ OUT0	I2S1_TX_ MCLK	-	Table 111
P9_0	T1	x	-	x	-	GPIO4[12]	MCABORT	R	R	R	ENET_ CRS	R	SSP0_ SSEL	-	Table 111
P9_1	N6	x	-	x	-	GPIO4[13]	MCOA2	R	R	I2S0_TX_ WS	ENET_ RX_ER	R	SSP0_ MISO	-	Table 111
P9_2	N8	x	-	x	-	GPIO4[14]	MCOB2	R	R	I2S0_TX_ SDA	ENET_ RXD3	R	SSP0_ MOSI	-	Table 111
P9_3	M6	x	-	x	-	GPIO4[15]	MCOA0	USB1_ IND1	R	R	ENET_ RXD2	R	U3_TXD	-	Table 111
P9_4	N10	x	-	x	-	R	MCOB0	USB1_ IND0	R	GPIO5[17]	ENET_ TXD2	R	U3_RXD	-	Table 111
P9_5	M9	x	-	x	69	R	MCOA1	USB1_ VBUS_EN	R	GPIO5[18]	ENET_ TXD3	R	U0_TXD	-	Table 111

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Table 109. Pin multiplexing

Symbol	LBGA256	BGA180	BGA100	LQFP208	LQFP144	Function level 0	1	2	3	4	5	6	7	8	Reference
P9_6	L11	x	-	x	72	GPIO4[11]	MCOB1	USB1_ PWR_FAU LT	R	R	ENET_ COL	R	U0_RXD	-	Table 111
PA_0	L12	x	-	x	-	R	R	R	R	R	I2S1_RX_ MCLK	CGU_ OUT1	R	-	Table 111
PA_1	J14	x	-	x	-	GPIO4[8]	QEI_IDX	R	U2_TXD	R	R	R	R	-	Table 112
PA_2	K15	x	-	x	-	GPIO4[9]	QEI_PHB	R	U2_RXD	R	R	R	R	-	Table 112
PA_3	H11	x	-	x	-	GPIO4[10]	QEI_PHA	R	R	R	R	R	R	-	Table 112
PA_4	G13	x	-	x	-	R	CTOUT_9	R	EMC_A23	GPIO5[19]	R	R	R	-	Table 111
PB_0	B15	x	-	x	-	R	CTOUT_10	LCD_VD23	R	GPIO5[20]	R	R	R	-	Table 111
PB_1	A14	x	-	x	-	R	USB1_ ULPI_DIR	LCD_VD22	R	GPIO5[21]	CTOUT_6	R	R	-	Table 111
PB_2	B12	x	-	x	-	R	USB1_ ULPI_D7	LCD_VD21	R	GPIO5[22]	CTOUT_7	R	R	-	Table 111
PB_3	A13	x	-	x	-	R	USB1_ ULPI_D6	LCD_VD20	R	GPIO5[23]	CTOUT_8	R	R	-	Table 111
PB_4	B11	x	-	x	-	R	USB1_ ULPI_D5	LCD_VD15	R	GPIO5[24]	CTIN_5	R	R	-	Table 111
PB_5	A12	x	-	x	-	R	USB1_ ULPI_D4	LCD_VD14	R	GPIO5[25]	CTIN_7	LCD_PWR	R	-	Table 111
PB_6	A6	x	-	x	-	R	USB1_ ULPI_D3	LCD_VD13	R	GPIO5[26]	CTIN_6	LCD_VD19	R	ADC0_6	Table 111Table 114
PC_0	D4	x	-	x	-	R	USB1_ ULPI_CLK	R	ENET_RX_ CLK	LCD_ DCLK	R	R	SD_CLK	ADC1_1	Table 111Table 116
PC_1	E4	-	-	x	-	USB1_ ULPI_D7	R	U1_RI	ENET_ MDC	GPIO6[0]	R	T3_CAP0	SD_ VOLT0	-	Table 111
PC_2	F6	-	-	x	-	USB1_ ULPI_D6	R	U1_CTS	ENET_ TXD2	GPIO6[1]	R	R	SD_RST	-	Table 111
PC_3	F5	-	-	x	-	USB1_ ULPI_D5	R	U1_RTS	ENET_ TXD3	GPIO6[2]	R	R	SD_ VOLT1	ADC1_0	Table 111Table 116

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Table 109. Pin multiplexing

Symbol	LBGA256	BGA180	BGA100	LQFP208	LQFP144	Function level 0	1	2	3	4	5	6	7	8	Reference
PC_4	F4	-	-	x	-	R	USB1_ ULPI_D4	R	ENET_ TX_EN	GPIO6[3]	R	T3_CAP1	SD_D0	-	Table 111
PC_5	G4	-	-	x	-	R	USB1_ ULPI_D3	R	ENET_ TX_ER	GPIO6[4]	R	T3_CAP2	SD_D1	-	Table 111
PC_6	H6	-	-	x	-	R	USB1_ ULPI_D2	R	ENET_ RXD2	GPIO6[5]	R	T3_CAP3	SD_D2	-	Table 111
PC_7	G5	-	-	-	-	R	USB1_ ULPI_D1	R	ENET_ RXD3	GPIO6[6]	R	T3_MAT0	SD_D3	-	Table 111
PC_8	N4	-	-	-	-	R	USB1_ ULPI_D0	R	ENET_ RX_DV	GPIO6[7]	R	T3_MAT1	SD_CD	-	Table 111
PC_9	K2	-	-	-	-	R	USB1_ ULPI_NXT	R	ENET_ RX_ER	GPIO6[8]	R	T3_MAT2	SD_POW	-	Table 111
PC_10	M5	-	-	-	-	R	USB1_ ULPI_STP	U1_DSR	R	GPIO6[9]	R	T3_MAT3	SD_CMD	-	Table 111
PC_11	L5	-	-	-	-	R	USB1_ ULPI_DIR	U1_DCD	R	GPIO6[10]	R	R	SD_D4	-	Table 111
PC_12	L6	-	-	-	-	R	R	U1_DTR	R	GPIO6[11]	R	I2S0_TX_S DA	SD_D5	-	Table 111
PC_13	M1	-	-	-	-	R	R	U1_TXD	R	GPIO6[12]	R	I2S0_TX_ WS	SD_D6	-	Table 111
PC_14	N1	-	-	-	-	R	R	U1_RXD	R	GPIO6[13]	R	ENET_ TX_ER	SD_D7	-	Table 111
PD_0	N2	-	-	-	-	R	CTOUT_15	EMC_ DQMOUT2	R	GPIO6[14]	R	R	R	-	Table 111
PD_1	P1	-	-	-	-	R	R	EMC_ CKEOUT2	R	GPIO6[15]	SD_POW	R	R	-	Table 111
PD_2	R1	-	-	-	-	R	CTOUT_7	EMC_D16	R	GPIO6[16]	R	R	R	-	Table 111
PD_3	P4	-	-	-	-	R	CTOUT_6	EMC_D17	R	GPIO6[17]	R	R	R	-	Table 111
PD_4	T2	-	-	-	-	R	CTOUT_8	EMC_D18	R	GPIO6[18]	R	R	R	-	Table 111
PD_5	P6	-	-	-	-	R	CTOUT_9	EMC_D19	R	GPIO6[19]	R	R	R	-	Table 111
PD_6	R6	-	-	x	-	R	CTOUT_10	EMC_D20	R	GPIO6[20]	R	R	R	-	Table 111

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Table 109. Pin multiplexing

Symbol	LBGA256	BGA180	BGA100	LQFP208	LQFP144	Function level 0	1	2	3	4	5	6	7	8	Reference
PD_7	T6	-	-	x	-	R	CTIN_5	EMC_D21	R	GPIO6[21]	R	R	R	-	Table 111
PD_8	P8	-	-	x	-	R	CTIN_6	EMC_D22	R	GPIO6[22]	R	R	R	-	Table 111
PD_9	T11	-	-	x	-	R	CTOUT_13	EMC_D23	R	GPIO6[23]	R	R	R	-	Table 111
PD_10	P11	-	-	x	-	R	CTIN_1	EMC_BLS3	R	GPIO6[24]	R	R	R	-	Table 111
PD_11	N9	x	-	x	-	R	R	EMC_CS3	R	GPIO6[25]	USB1_ ULPI_D0	CTOUT_14	R	-	Table 111
PD_12	N11	x	-	x	-	R	R	EMC_CS2	R	GPIO6[26]	R	CTOUT_10	R	-	Table 111
PD_13	T14	x	-	-	-	R	CTIN_0	EMC_BLS2	R	GPIO6[27]	R	CTOUT_13	R	-	Table 111
PD_14	R13	x	-	x	-	R	R	EMC_ DYCS2	R	GPIO6[28]	R	CTOUT_11	R	-	Table 111
PD_15	T15	x	-	x	-	R	R	EMC_A17	R	GPIO6[29]	SD_WP	CTOUT_8	R	-	Table 111
PD_16	R14	x	-	x	-	R	R	EMC_A16	R	GPIO6[30]	SD_ VOLT2	CTOUT_12	R	-	Table 111
PE_0	P14	x	-	x	-	R	R	R	EMC_A18	GPIO7[0]	CAN1_TD	R	R	-	Table 111
PE_1	N14	x	-	x	-	R	R	R	EMC_A19	GPIO7[1]	CAN1_RD	R	R	-	Table 111
PE_2	M14	x	-	x	-	ADC TRIG0	CAN0_RD	R	EMC_A20	GPIO7[2]	R	R	R	-	Table 111
PE_3	K12	x	-	x	-	R	CAN0_TD	ADCTRIG1	EMC_A21	GPIO7[3]	R	R	R	-	Table 111
PE_4	K13	x	-	x	-	R	NMI	R	EMC_A22	GPIO7[4]	R	R	R	-	Table 111
PE_5	N16	-	-	x	-	R	CTOUT_3	U1_RTS	EMC_D24	GPIO7[5]	R	R	R	-	Table 111
PE_6	M16	-	-	x	-	R	CTOUT_2	U1_RI	EMC_D25	GPIO7[6]	R	R	R	-	Table 111
PE_7	F15	-	-	x	-	R	CTOUT_5	U1_CTS	EMC_D26	GPIO7[7]	R	R	R	-	Table 111
PE_8	F14	-	-	x	-	R	CTOUT_4	U1_DSR	EMC_D27	GPIO7[8]	R	R	R	-	Table 111
PE_9	E16	-	-	x	-	R	CTIN_4	U1_DCD	EMC_D28	GPIO7[9]	R	R	R	-	Table 111
PE_10	E14	-	-	x	-	R	CTIN_3	U1_DTR	EMC_D29	GPIO7[10]	R	R	R	-	Table 111
PE_11	D16	-	-	-	-	R	CTOUT_12	U1_TXD	EMC_D30	GPIO7[11]	R	R	R	-	Table 111
PE_12	D15	-	-	-	-	R	CTOUT_11	U1_RXD	EMC_D31	GPIO7[12]	R	R	R	-	Table 111
PE_13	G14	-	-	-	-	R	CTOUT_14	I2C1_SDA	EMC_ DQMOUT3	GPIO7[13]	R	R	R	-	Table 111

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Table 109. Pin multiplexing

Symbol	LBGA256	BGA180	BGA100	LQFP208	LQFP144	Function level 0	1	2	3	4	5	6	7	8	Reference
PE_14	C15	-	-	-	-	R	R	R	EMC_ DYCS3	GPIO7[14]	R	R	R	-	Table 111
PE_15	E13	-	-	-	-	R	CTOUT_0	I2C1_SCL	EMC_ CKEOUT3	GPIO7[15]	R	R	R	-	Table 111
PF_0	D12	-	-	-	-	SSP0_ SCK	GP_CLKIN	R	R	R	R	R	I2S1_TX_ MCLK	-	Table 111
PF_1	E11	-	-	-	-	R	R	SSP0_ SSEL	R	GPIO7[16]	R	R	R	-	Table 111
PF_2	D11	-	-	x	-	R	U3_TXD	SSP0_ MISO	R	GPIO7[17]	R	R	R	-	Table 111
PF_3	E10	-	-	x	-	R	U3_RXD	SSP0_ MOSI	R	GPIO7[18]	R	R	R	-	Table 111
PF_4	D10	x	x	x	120	SSP1_ SCK	GP_CLKIN	TRACE CLK	R	R	R	I2S0_TX_ MCLK	I2S0_RX_ SCK	-	Table 111
PF_5	E9	-	-	x	-	R	U3_UCLK	SSP1_ SSEL	TRACE DATA[0]	GPIO7[19]	R	R	R	ADC1_4	Table 111Table 116
PF_6	E7	-	-	x	-	R	U3_DIR	SSP1_ MISO	TRACE DATA[1]	GPIO7[20]	R	R	I2S1_TX_ SDA	ADC1_3	Table 111Table 116
PF_7	B7	-	-	x	-	R	U3_BAUD	SSP1_ MOSI	TRACE DATA[2]	GPIO7[21]	R	R	I2S1_TX_ WS	ADC1_7	Table 111Table 116
PF_8	E6	-	-	x	-	R	U0_UCLK	CTIN_2	TRACE DATA[3]	GPIO7[22]	R	R	R	ADC0_2	Table 111Table 114
PF_9	D6	-	-	x	-	R	U0_DIR	CTOUT_1	R	GPIO7[23]	R	R	R	ADC1_2	Table 111Table 116
PF_10	A3	-	-	x	-	R	U0_TXD	R	R	GPIO7[24]	R	SD_WP	R	ADC0_5	Table 111Table 114
PF_11	A2	-	-	x	-	R	U0_RXD	R	R	GPIO7[25]	R	SD_ VOLT2	R	ADC1_5	Table 111Table 116
Clock pins														-	Table 111

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Table 109. Pin multiplexing

Symbol	LBGA256	BGA180	BGA100	LQFP208	LQFP144	Function level 0	1	2	3	4	5	6	7	8	Reference
CLK0	N5	x	x	x	45	EMC_CLK0	CLKOUT	R	R	SD_CLK	EMC_CLK01	SSP1_SCK	ENET_TX_CLK (ENET_REF_CLK)	-	Table 111
CLK1	T10	x	-	-	-	EMC_CLK1	CLKOUT	R	R	R	CGU_OUT0	R	I2S1_TX_MCLK	-	Table 111
CLK2	D14	x	x	x	99	EMC_CLK3	CLKOUT	R	R	SD_CLK	EMC_CLK23	I2S0_TX_MCLK	I2S1_RX_SCK	-	Table 111
CLK3	P12	x	-	-	-	EMC_CLK2	CLKOUT	R	R	R	CGU_OUT1	R	I2S1_RX_SCK	-	Table 111

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13.4 Register description

Table 110. Register overview: System Control Unit (SCU) (base address 0x4008 6000)

Name	Access	Address offset	Description	Reset value
Pins P0_n				
SFSP0_0	R/W	0x000	Pin configuration register for pin P0_0	0x00
SFSP0_1	R/W	0x004	Pin configuration register for pin P0_1	0x00
-	-	0x008 - 0x07C	Reserved	-
Pins P1_n				
SFSP1_0	R/W	0x080	Pin configuration register for pin P1_0	0x00
SFSP1_1	R/W	0x084	Pin configuration register for pin P1_1	0x00
SFSP1_2	R/W	0x088	Pin configuration register for pin P1_2	0x00
SFSP1_3	R/W	0x08C	Pin configuration register for pin P1_3	0x00
SFSP1_4	R/W	0x090	Pin configuration register for pin P1_4	0x00
SFSP1_5	R/W	0x094	Pin configuration register for pin P1_5	0x00
SFSP1_6	R/W	0x098	Pin configuration register for pin P1_6	0x00
SFSP1_7	R/W	0x09C	Pin configuration register for pin P1_7	0x00
SFSP1_8	R/W	0x0A0	Pin configuration register for pin P1_8	0x00
SFSP1_9	R/W	0x0A4	Pin configuration register for pin P1_9	0x00
SFSP1_10	R/W	0x0A8	Pin configuration register for pin P1_10	0x00
SFSP1_11	R/W	0x0AC	Pin configuration register for pin P1_11	0x00
SFSP1_12	R/W	0x0B0	Pin configuration register for pin P1_12	0x00
SFSP1_13	R/W	0x0B4	Pin configuration register for pin P1_13	0x00
SFSP1_14	R/W	0x0B8	Pin configuration register for pin P1_14	0x00
SFSP1_15	R/W	0x0BC	Pin configuration register for pin P1_15	0x00
SFSP1_16	R/W	0x0C0	Pin configuration register for pin P1_16	0x00
SFSP1_17	R/W	0x0C4	Pin configuration register for pin P1_17	0x00
SFSP1_18	R/W	0x0C8	Pin configuration register for pin P1_18	0x00
SFSP1_19	R/W	0x0CC	Pin configuration register for pin P1_19	0x00
SFSP1_20	R/W	0x0D0	Pin configuration register for pin P1_20	0x00

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Table 110. Register overview: System Control Unit (SCU) (base address 0x4008 6000) *…continued*

Name	Access	Address offset	Description	Reset value
-	-	0x0D4 - 0x0FC	Reserved	-
Pins P2_n				
SFSP2_0	R/W	0x100	Pin configuration register for pin P2_0	0x00
SFSP2_1	R/W	0x104	Pin configuration register for pin P2_1	0x00
SFSP2_2	R/W	0x108	Pin configuration register for pin P2_2	0x00
SFSP2_3	R/W	0x10C	Pin configuration register for pin P2_3	0x00
SFSP2_4	R/W	0x110	Pin configuration register for pin P2_4	0x00
SFSP2_5	R/W	0x114	Pin configuration register for pin P2_5	0x00
SFSP2_6	R/W	0x118	Pin configuration register for pin P2_6	0x00
SFSP2_7	R/W	0x11C	Pin configuration register for pin P2_7	0x00
SFSP2_8	R/W	0x120	Pin configuration register for pin P2_8	0x00
SFSP2_9	R/W	0x124	Pin configuration register for pin P2_9	0x00
SFSP2_10	R/W	0x128	Pin configuration register for pin P2_10	0x00
SFSP2_11	R/W	0x12C	Pin configuration register for pin P2_11	0x00
SFSP2_12	R/W	0x130	Pin configuration register for pin P2_12	0x00
SFSP2_13	R/W	0x134	Pin configuration register for pin P2_13	0x00
-	-	0x138 - 0x17C	Reserved	-
Pins P3_n				
SFSP3_0	R/W	0x180	Pin configuration register for pin P3_0	0x00
SFSP3_1	R/W	0x184	Pin configuration register for pin P3_1	0x00
SFSP3_2	R/W	0x188	Pin configuration register for pin P3_2	0x00
SFSP3_3	R/W	0x18C	Pin configuration register for pin P3_3	0x00
SFSP3_4	R/W	0x190	Pin configuration register for pin P3_4	0x00
SFSP3_5	R/W	0x194	Pin configuration register for pin P3_5	0x00
SFSP3_6	R/W	0x198	Pin configuration register for pin P3_6	0x00
SFSP3_7	R/W	0x19C	Pin configuration register for pin P3_7	0x00
SFSP3_8	R/W	0x1A0	Pin configuration register for pin P3_8	0x00
-	-	0x1A4 - 0x1FC	Reserved	-
Pins P4_n				
SFSP4_0	R/W	0x200	Pin configuration register for pin P4_0	0x00
SFSP4_1	R/W	0x204	Pin configuration register for pin P4_1	0x00
SFSP4_2	R/W	0x208	Pin configuration register for pin P4_2	0x00
SFSP4_3	R/W	0x20C	Pin configuration register for pin P4_3	0x00
SFSP4_4	R/W	0x210	Pin configuration register for pin P4_4	0x00
SFSP4_5	R/W	0x214	Pin configuration register for pin P4_5	0x00
SFSP4_6	R/W	0x218	Pin configuration register for pin P4_6	0x00
SFSP4_7	R/W	0x21C	Pin configuration register for pin P4_7	0x00

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Table 110. Register overview: System Control Unit (SCU) (base address 0x4008 6000) *…continued*

Name	Access	Address offset	Description	Reset value
SFSP4_8	R/W	0x220	Pin configuration register for pin P4_8	0x00
SFSP4_9	R/W	0x224	Pin configuration register for pin P4_9	0x00
SFSP4_10	R/W	0x228	Pin configuration register for pin P4_10	0x00
-	-	0x22C - 0x27C	Reserved	-
Pins P5_n				
SFSP5_0	R/W	0x280	Pin configuration register for pin P5_0	0x00
SFSP5_1	R/W	0x284	Pin configuration register for pin P5_1	0x00
SFSP5_2	R/W	0x288	Pin configuration register for pin P5_2	0x00
SFSP5_3	R/W	0x28C	Pin configuration register for pin P5_3	0x00
SFSP5_4	R/W	0x290	Pin configuration register for pin P5_4	0x00
SFSP5_5	R/W	0x294	Pin configuration register for pin P5_5	0x00
SFSP5_6	R/W	0x298	Pin configuration register for pin P5_6	0x00
SFSP5_7	R/W	0x29C	Pin configuration register for pin P5_7	0x00
-	-	0x2A0 - 0x2FC	Reserved	-
Pins P6_n				
SFSP6_0	R/W	0x300	Pin configuration register for pin P6_0	0x00
SFSP6_1	R/W	0x304	Pin configuration register for pin P6_1	0x00
SFSP6_2	R/W	0x308	Pin configuration register for pin P6_2	0x00
SFSP6_3	R/W	0x30C	Pin configuration register for pin P6_3	0x00
SFSP6_4	R/W	0x310	Pin configuration register for pin P6_4	0x00
SFSP6_5	R/W	0x314	Pin configuration register for pin P6_5	0x00
SFSP6_6	R/W	0x318	Pin configuration register for pin P6_6	0x00
SFSP6_7	R/W	0x31C	Pin configuration register for pin P6_7	0x00
SFSP6_8	R/W	0x320	Pin configuration register for pin P6_8	0x00
SFSP6_9	R/W	0x324	Pin configuration register for pin P6_9	0x00
SFSP6_10	R/W	0x328	Pin configuration register for pin P6_10	0x00
SFSP6_11	R/W	0x32C	Pin configuration register for pin P6_11	0x00
SFSP6_12	R/W	0x330	Pin configuration register for pin P6_12	0x00
-	-	0x334 - 0x37C	Reserved	-
Pins P7_n				
SFSP7_0	R/W	0x380	Pin configuration register for pin P7_0	0x00
SFSP7_1	R/W	0x384	Pin configuration register for pin P7_1	0x00
SFSP7_2	R/W	0x388	Pin configuration register for pin P7_2	0x00
SFSP7_3	R/W	0x38C	Pin configuration register for pin P7_3	0x00
SFSP7_4	R/W	0x390	Pin configuration register for pin P7_4	0x00
SFSP7_5	R/W	0x394	Pin configuration register for pin P7_5	0x00
SFSP7_6	R/W	0x398	Pin configuration register for pin P7_6	0x00

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Table 110. Register overview: System Control Unit (SCU) (base address 0x4008 6000) *…continued*

Name	Access	Address offset	Description	Reset value
SFSP7_7	R/W	0x39C	Pin configuration register for pin P7_7	0x00
-	-	0x3A0 - 0x3FC	Reserved	-
Pins P8_n				
SFSP8_0	R/W	0x400	Pin configuration register for pin P8_0	0x00
SFSP8_1	R/W	0x404	Pin configuration register for pin P8_1	0x00
SFSP8_2	R/W	0x408	Pin configuration register for pin P8_2	0x00
SFSP8_3	R/W	0x40C	Pin configuration register for pin P8_3	0x00
SFSP8_4	R/W	0x410	Pin configuration register for pin P8_4	0x00
SFSP8_5	R/W	0x414	Pin configuration register for pin P8_5	0x00
SFSP8_6	R/W	0x418	Pin configuration register for pin P8_6	0x00
SFSP8_7	R/W	0x41C	Pin configuration register for pin P8_7	0x00
SFSP8_8	R/W	0x420	Pin configuration register for pin P8_8	0x00
-	-	0x424 - 0x47C	Reserved	-
Pins P9_n				
SFSP9_0	R/W	0x480	Pin configuration register for pin P9_0	0x00
SFSP9_1	R/W	0x484	Pin configuration register for pin P9_1	0x00
SFSP9_2	R/W	0x488	Pin configuration register for pin P9_2	0x00
SFSP9_3	R/W	0x49C	Pin configuration register for pin P9_3	0x00
SFSP9_4	R/W	0x490	Pin configuration register for pin P9_4	0x00
SFSP9_5	R/W	0x494	Pin configuration register for pin P9_5	0x00
SFSP9_6	R/W	0x498	Pin configuration register for pin P9_6	0x00
-	-	0x49C - 0x4FC	Reserved	-
Pins PA_n				
-	R/W	0x500	Reserved	-
SFSPA_1	R/W	0x504	Pin configuration register for pin PA_1	0x00
SFSPA_2	R/W	0x508	Pin configuration register for pin PA_2	0x00
SFSPA_3	R/W	0x50C	Pin configuration register for pin PA_3	0x00
SFSPA_4	R/W	0x510	Pin configuration register for pin PA_4	0x00
-	-	0x514 - 0x57C	Reserved	-
Pins PB_n				
SFSPB_0	R/W	0x580	Pin configuration register for pin PB_0	0x00
SFSPB_1	R/W	0x584	Pin configuration register for pin PB_1	0x00
SFSPB_2	R/W	0x588	Pin configuration register for pin PB_2	0x00
SFSPB_3	R/W	0x58C	Pin configuration register for pin PB_3	0x00
SFSPB_4	R/W	0x590	Pin configuration register for pin PB_4	0x00
SFSPB_5	R/W	0x594	Pin configuration register for pin PB_5	0x00

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Table 110. Register overview: System Control Unit (SCU) (base address 0x4008 6000) *…continued*

Name	Access	Address offset	Description	Reset value
SFSPB_6	R/W	0x598	Pin configuration register for pin PB_6	0x00
-	-	0x59C - 0x5FC	Reserved	-
Pins PC_n				
SFSPC_0	R/W	0x600	Pin configuration register for pin PC_0	0x00
SFSPC_1	R/W	0x604	Pin configuration register for pin PC_1	0x00
SFSPC_2	R/W	0x608	Pin configuration register for pin PC_2	0x00
SFSPC_3	R/W	0x60C	Pin configuration register for pin PC_3	0x00
SFSPC_4	R/W	0x610	Pin configuration register for pin PC_4	0x00
SFSPC_5	R/W	0x614	Pin configuration register for pin PC_5	0x00
SFSPC_6	R/W	0x618	Pin configuration register for pin PC_6	0x00
SFSPC_7	R/W	0x61C	Pin configuration register for pin PC_7	0x00
SFSPC_8	R/W	0x620	Pin configuration register for pin PC_8	0x00
SFSPC_9	R/W	0x624	Pin configuration register for pin PC_9	0x00
SFSPC_10	R/W	0x628	Pin configuration register for pin PC_10	0x00
SFSPC_11	R/W	0x62C	Pin configuration register for pin PC_11	0x00
SFSPC_12	R/W	0x630	Pin configuration register for pin PC_12	0x00
SFSPC_13	R/W	0x634	Pin configuration register for pin PC_13	0x00
SFSPC_14	R/W	0x638	Pin configuration register for pin PC_14	0x00
-	-	0x63C - 0x67C	Reserved	-
Pins PD_n				
SFSPD_0	R/W	0x680	Pin configuration register for pin PD_0	0x00
SFSPD_1	R/W	0x684	Pin configuration register for pin PD_1	0x00
SFSPD_2	R/W	0x688	Pin configuration register for pin PD_2	0x00
SFSPD_3	R/W	0x68C	Pin configuration register for pin PD_3	0x00
SFSPD_4	R/W	0x690	Pin configuration register for pin PD_4	0x00
SFSPD_5	R/W	0x694	Pin configuration register for pin PD_5	0x00
SFSPD_6	R/W	0x698	Pin configuration register for pin PD_6	0x00
SFSPD_7	R/W	0x69C	Pin configuration register for pin PD_7	0x00
SFSPD_8	R/W	0x6A0	Pin configuration register for pin PD_8	0x00
SFSPD_9	R/W	0x6A4	Pin configuration register for pin PD_9	0x00
SFSPD_10	R/W	0x6A8	Pin configuration register for pin PD_10	0x00
SFSPD_11	R/W	0x6AC	Pin configuration register for pin PD_11	0x00
SFSPD_12	R/W	0x6B0	Pin configuration register for pin PD_12	0x00
SFSPD_13	R/W	0x6B4	Pin configuration register for pin PD_13	0x00
SFSPD_14	R/W	0x6B8	Pin configuration register for pin PD_14	0x00
SFSPD_15	R/W	0x6BC	Pin configuration register for pin PD_15	0x00
SFSPD_16	R/W	0x6C0	Pin configuration register for pin PD_16	0x00

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Table 110. Register overview: System Control Unit (SCU) (base address 0x4008 6000) *…continued*

Name	Access	Address offset	Description	Reset value
-	-	0x6C4 - 0x6FC	Reserved	-
Pins PE_n				
SFSPE_0	R/W	0x700	Pin configuration register for pin PE_0	0x00
SFSPE_1	R/W	0x704	Pin configuration register for pin PE_1	0x00
SFSPE_2	R/W	0x708	Pin configuration register for pin PE_2	0x00
SFSPE_3	R/W	0x70C	Pin configuration register for pin PE_3	0x00
SFSPE_4	R/W	0x710	Pin configuration register for pin PE_4	0x00
SFSPE_5	R/W	0x714	Pin configuration register for pin PE_5	0x00
SFSPE_6	R/W	0x718	Pin configuration register for pin PE_6	0x00
SFSPE_7	R/W	0x71C	Pin configuration register for pin PE_7	0x00
SFSPE_8	R/W	0x720	Pin configuration register for pin PE_8	0x00
SFSPE_9	R/W	0x724	Pin configuration register for pin PE_9	0x00
SFSPE_10	R/W	0x728	Pin configuration register for pin PE_10	0x00
SFSPE_11	R/W	0x72C	Pin configuration register for pin PE_11	0x00
SFSPE_12	R/W	0x730	Pin configuration register for pin PE_12	0x00
SFSPE_13	R/W	0x734	Pin configuration register for pin PE_13	0x00
SFSPE_14	R/W	0x738	Pin configuration register for pin PE_14	0x00
SFSPE_15	R/W	0x73C	Pin configuration register for pin PE_15	0x00
-	-	0x740 - 0x77C	Reserved	-
Pins PF_n				
SFSPF_0	R/W	0x780	Pin configuration register for pin PF_0	0x00
SFSPF_1	R/W	0x784	Pin configuration register for pin PF_1	0x00
SFSPF_2	R/W	0x788	Pin configuration register for pin PF_2	0x00
SFSPF_3	R/W	0x78C	Pin configuration register for pin PF_3	0x00
SFSPF_4	R/W	0x790	Pin configuration register for pin PF_4	0x00
SFSPF_5	R/W	0x794	Pin configuration register for pin PF_5	0x00
SFSPF_6	R/W	0x798	Pin configuration register for pin PF_6	0x00
SFSPF_7	R/W	0x79C	Pin configuration register for pin PF_7	0x00
SFSPF_8	R/W	0x7A0	Pin configuration register for pin PF_8	0x00
SFSPF_9	R/W	0x7A4	Pin configuration register for pin PF_9	0x00
SFSPF_10	R/W	0x7A8	Pin configuration register for pin PF_10	0x00
SFSPF_11	R/W	0x7AC	Pin configuration register for pin PF_11	0x00
-	-	0x7B0 - 0xBFC	Reserved	-
CLKn pins				
SFSCLK0	R/W	0xC00	Pin configuration register for pin CLK0	0x00
SFSCLK1	R/W	0xC04	Pin configuration register for pin CLK1	0x00
SFSCLK2	R/W	0xC08	Pin configuration register for pin CLK2	0x00

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Table 110. Register overview: System Control Unit (SCU) (base address 0x4008 6000) *…continued*

Name	Access	Address offset	Description	Reset value
SFSCLK3	R/W	0xC0C	Pin configuration register for pin CLK3	0x00
-	-	0xC10 - 0xC84	Reserved	-
ADC pin select registers				
ENAIO0	R/W	0xC88	ADC0 function select register	<tbd>
ENAIO1	R/W	0xC8C	ADC1 function select register	<tbd>
ENAIO2	R/W	0xC90	Analog function select register	<tbd>
USB DP1/DPM pins and I^{2}C-bus open-drain pins				
SFSUSB	R/W	0xC80	Pin configuration register for	0x00
SFSI2C0	R/W	0xC84	Pin configuration register for I^{2}C0-bus pins	0x00
EMC delay registers				
EMCCLKDELAY	R/W	0xD00	EMC clock delay register	
EMCCTRLDELAY	R/W	0xD04	EMC control delay register	
EMCCSDELAY	R/W	0xD08	EMC chip select delay register	
EMCDOUTDELAY	R/W	0xD0C	EMC data out delay register	
EMCFBCLKDELAY	R/W	0xD10	EMC FBCLK delay register	
EMCADDRDELAY0	R/W	0xD14	EMC address line delay register 0	
EMCADDRDELAY1	R/W	0xD18	EMC address line delay register 1	
EMCADDRDELAY2	R/W	0xD1C	EMC address line delay register 2	
-	-	0xD20	Reserved	
EMCDINDELAY	R/W	0xD24	EMC data delay register	
Pin interrupt select registers				
PINTSEL0	R/W	0xE00	Pin interrupt select register for pin interrupts 0 to 3.	
PINTSEL1	R/W	0xE04	Pin interrupt select register for pin interrupts 4 to 7.	

13.4.1 Pin configuration registers for normal drive pins

Each digital pin and each clock pin on the LPC18xx have an associated pin configuration register which determines the pin's function and electrical characteristics. The assigned functions for each pin are listed in Table 109.

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Table 111. Pin configuration for normal drive pins P0_n to PF_n and CLK0 to CLK3 registers (SFS, address 0x4008 6000 (SPSP0_0) to 0x4008 6C0C (SFSCLK3)) bit description

Bit	Symbol	Value	Description	Reset value	Access
2:0	MODE		Select pin function	0	R/W
		0x0	Function 0 (default)		
		0x1	Function 1		
		0x2	Function 2		
		0x3	Function 3		
		0x4	Function 4		
		0x5	Function 5		
		0x6	Function 6		
		0x7	Function 7		
3	EPD		Enable pull-down resistor at pad	0	R/W
		0	Disable pull-down.		
		1	Enable pull-down.		
4	EPUN		Disable pull-up resistor at pad. By default, the pull-up resistor is enabled at reset.	0	R/W
		0	Enable pull-up		
		1	Disable pull-up		
5	EHS		Slew rate	0	R/W
		0	Slow		
		1	Fast		
6	EZI		Input buffer enable. The input buffer is disabled by default at reset and must be enabled for receiving.	0	R/W
		0	Disable input buffer		
		1	Enable input buffer		
31:7	-		Reserved	-	-

13.4.2 Pin configuration registers for high drive pins

Each digital pin and each clock pin on the LPC18xx have an associated pin configuration register which determines the pin’s function and electrical characteristics. The assigned functions for each pin are listed in Table 109.

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Table 112. Pin configuration for high drive pins P0_n to PF_n and CLK0 to CLK3 registers (SFS, address 0x4008 6000 (SFSP0_0) to 0x4008 6C0C (SFSCLK3) bit description

Bit	Symbol	Value	Description	Reset value	Access
2:0	MODE		Select pin function	0	R/W
		0x0	Function 0 (default)		
		0x1	Function 1		
		0x2	Function 2		
		0x3	Function 3		
		0x4	Function 4		
		0x5	Function 5		
		0x6	Function 6		
		0x7	Function 7		
3	EPD		Enable pull-down resistor at pad	0	R/W
		0	Disable pull-down.		
		1	Enable pull-down.		
4	EPUN		Disable pull-up resistor at pad. By default, the pull-up resistor is enabled at reset.	0	R/W
		0	Enable pull-up		
		1	Disable pull-up		
5	EHS		Slew rate	0	R/W
		0	Slow		
		1	Fast		
6	EZI		Input buffer enable. The input buffer is disabled by default at reset but must be enabled to transfer data from the I/O buffer to the pad.	0	R/W
		0	Disable input buffer		
		1	Enable input buffer		
7	-		Reserved	-	-
9:8	EHD		Select drive strength	0	R/W
		0x0	Standard drive: 4 mA drive strength		
		0x1	Medium drive: 8 mA drive strength		
		0x2	High drive: 14 mA drive strength		
		0x3	Ultra-high drive: 20 mA drive strength		
31:10	-		Reserved	-	-

13.4.3 ADC0 function select register

For pins which have digital and analog functions, this register selects the input channel of the ADC0 over any of the possible digital functions. This option is not available for channel ADC0_7.

In addition, each analog function is pinned out on a dedicated analog pin which is not affected by this register.

The following pins are controlled by the ENAIO0 register:

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Table 113. Pins controlled by the ENAIO0 register

Pin	ADC function	ENAIO0 register bit
P4_3	ADC0_0	0
P4_1	ADC0_1	1
PF_8	ADC0_2	2
P7_5	ADC0_3	3
P7_4	ADC0_4	4
PF_10	ADC0_5	5
PB_6	ADC0_6	6

By default, all pins are connected to their digital function 0 and the corresponding ENAIO0 register bit is set to one. In this case, only the digital pad is available.

Before selecting the analog pad by setting the ENAIO0 register bit to zero, the digital pad must be set as follows using the corresponding SFSP register:

1. Tri-state the output driver by selecting an input at the pinmux e.g. GPIO function in input mode.
2. Disable the receiver by setting the EZI bit to zero (see Table 111 or Table 112). This is the default setting.
3. Disable the pull-up resistor by setting the EPUN bit to one, and disable the pull-down resistor by setting the EPD bit to zero.

Table 114. ADC0 function select register (ENAIO0, address 0x4008 6C88) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	ADC0_0		Select ADC0_0	0	R/W
		0	Analog function ADC0_0 selected on pin P4_3.		
		1	Digital function selected on pin P4_3.		
1	ADC0_1		Select ADC0_1	0	R/W
		0	Analog function ADC0_1 selected on pin P4_1.		
		1	Digital function selected on pin P4_1.		
2	ADC0_2		Select ADC0_2	0	R/W
		0	Analog function ADC0_2 selected on pin PF_8.		
		1	Digital function selected on pin PF_8.		
3	ADC0_3		Select ADC0_3	0	R/W
		0	Analog function ADC0_3 selected on pin P7_5.		
		1	Digital function selected on pin P7_5.		
4	ADC0_4		Select ADC0_4	0	R/W
		0	Analog function ADC0_4 selected on pin P7_4.		
		1	Digital function selected on pin P7_4.		
5	ADC0_5		Select ADC0_5	0	R/W
		0	Analog function ADC0_5 selected on pin PF_10.		
		1	Digital function selected on pin PF_10.		

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Table 114. ADC0 function select register (ENAIO0, address 0x4008 6C88) bit description

Bit	Symbol	Value	Description	Reset value	Access
6	ADC0_6		Select ADC0_6	0	R/W
		0	Analog function ADC0_6 selected on pin PB_6.		
		1	Digital function selected on pin PB_6.		
31:7			Reserved	-	-

13.4.4 ADC1 function select register

For pins which have digital and analog functions, this register selects the ADC1 function over any of the possible digital functions.

In addition, each analog function is pinned out on a dedicated analog pin which is not affected by this register.

The following pins are controlled by the ENAIO1 register:

Table 115. Pins controlled by the ENAIO1 register

Pin	ADC function	ENAIO1 register bit
PC_3	ADC1_0	0
PC_0	ADC1_1	1
PF_9	ADC1_2	2
PF_6	ADC1_3	3
PF_5	ADC1_4	4
PF_11	ADC1_5	5
P7_7	ADC1_6	6
PF_7	ADC1_7	7

By default, all pins are connected to their digital function 0 and the corresponding ENAIO1 register bit is set to one. In this case, only the digital pad is available.

Before selecting the analog pad by setting the ENAIO1 register bit to zero, the digital pad must be set as follows using the corresponding SFSP register:

1. Tri-state the output driver by selecting an input at the pinmux e.g. GPIO function in input mode.
2. Disable the receiver by setting the EZI bit to zero (see Table 111 or Table 112). This is the default setting.
3. Disable the pull-up resistor by setting the EPUN bit to one, and disable the pull-down resistor by setting the EPD bit to zero.

Table 116. ADC1 function select register (ENAIO1, address 0x4008 6C8C) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	ADC1_0		Select ADC1_0	0	R/W
		0	Analog function ADC1_0 selected on pin PC_3.		
		1	Digital function selected on pin PC_3.		

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Table 116. ADC1 function select register (ENAIO1, address 0x4008 6C8C) bit description

Bit	Symbol	Value	Description	Reset value	Access
1	ADC1_1		Select ADC1_1	0	R/W
		0	Analog function ADC1_1 selected on pin PC_0.		
		1	Digital function selected on pin PC_0.		
2	ADC1_2		Select ADC1_2	0	R/W
		0	Analog function ADC1_2 selected on pin PF_9.		
		1	Digital function selected on pin PF_9.		
3	ADC1_3		Select ADC1_3	0	R/W
		0	Analog function ADC1_3 selected on pin PF_6.		
		1	Digital function selected on pin PF_6.		
4	ADC1_4		Select ADC1_4	0	R/W
		0	Analog function ADC1_4 selected on pin PF_5.		
		1	Digital function selected on pin PF_5.		
5	ADC1_5		Select ADC1_5	0	R/W
		0	Analog function ADC1_5 selected on pin PF_11.		
		1	Digital function selected on pin PF_11.		
6	ADC1_6		Select ADC1_6	0	R/W
		0	Analog function ADC1_6 selected on pin P7_7.		
		1	Digital function selected on pin P7_7.		
7	ADC1_7		Select ADC1_7	0	R/W
		0	Analog function ADC1_7 selected on pin PF_7.		
		1	Digital function selected on pin PF_7.		
31:8			Reserved	-	-

13.4.5 Analog function select register

For pins which have digital and analog functions, this register selects the analog DAC and band gap function over any of the possible digital functions.

In addition, the DAC function is pinned out on a dedicated analog pin which is not affected by this register.

The following pins are controlled by the ENAIO1 register:

Table 117. Pins controlled by the ENAIO2 register

Pin	ADC function	ENAIO2 register bit
P4_4	DAC	0
PF_7	BG (band gap output)	4

By default, all pins are connected to their digital function 0 and the corresponding ENAIO2 register bit is set to one. In this case, only the digital pad is available.

Before selecting the analog pad by setting the ENAIO2 register bit to zero, the digital pad must be set as follows using the corresponding SFSP register:

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1. Tri-state the output driver by selecting an input at the pinmux e.g. GPIO function in input mode.
2. Disable the receiver by setting the EZI bit to zero (see Table 111 or Table 112). This is the default setting.
3. Disable the pull-up resistor by setting the EPUN bit to one, and disable the pull-down resistor by setting the EPD bit to zero.

Table 118. Analog function select register (ENAIO2, address 0x4008 6C90) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	DAC		Select DAC	0	R/W
		0	Analog function DAC selected on pin P4_4.		
		1	Digital function selected on pin P4_4.		
3:1			Reserved	-	-
4	BG		Select band gap output	0	R/W
		0	Band gap output selected for pin PF_7.		
		1	Digital function selected on pin PF_7.		
31:5			Reserved	-	-

13.4.6 Pin configuration register for USB1 pins DP1/DM1

Remark: The USB_ESEA bit must be set to one to use USB1.

Table 119. Pin configuration for pins DP1/DM1 register (SFSUSB, address 0x4008 6C80) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	USB_AIM		Differential data input AIP/AIM 0 = Going LOW with full speed edge rate 1 = Going HIGH with full speed edge rate	0	R/W
		0	Going LOW with full speed edge rate		
		1	Going HIGH with full speed edge rate		
1	USB_ESEA		Control signal for differential input or single input	0	R/W
		0	Reserved. Do not use.		
		1	Single input AIP. Enables USB1.		
31:2	-		Reserved	-	-

13.4.7 Pin configuration register for open-drain I²C-bus pins

Table 120. Pin configuration for open-drain I²C-bus pins register (SFSI2C0, address 0x4008 6C84) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	SDA_EHS		Configures I²C0-bus speed for SDA0 pin	0	R/W
		0	Standard/Fast mode (400 kbit/s)		
		1	High-speed mode (3.4 Mbit/s)		

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Table 120. Pin configuration for open-drain I2C-bus pins register (SFSI2C0, address 0x4008 6C84) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
1	SCL_EHS		Configures I2C0-bus speed for SCL0 pin	0	R/W
		0	Standard/Fast mode (400 kbit/s)		
		1	High-speed mode (3.4 Mbit/s)		
2	SCL_ECS		Direction (only applies if SCL_EHS = 1)	0	R/W
		0	Receive		
		1	Transmit		
31:3	-		Reserved	-	-

13.4.8 EMC clock delay register

This register provides a programmable delay for the EMC clock outputs. The delay for each clock output is approximately 0.5 ns × CLKn_DELAY or 0.5 ns × CKEn_DELAY. (CLKn_DELAY/CKEn_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

Table 121. EMC clock delay register (EMCCLKDELAY, address 0x4008 6D00) bit description

Bit	Symbol	Description	Reset value	Access
2:0	CLK0_DELAY	Delay of the EMC_CLK0 clock output.	0	R/W
3	-	Reserved.	-	-
6:4	CLK1_DELAY	Delay of the EMC_CLK0 clock output.	0	R/W
7	-	Reserved.	-	-
10:8	CLK2_DELAY	Delay of the EMC_CLK2 clock output.	0	R/W
11	-	Reserved.	-	-
14:12	CLK3_DELAY	Delay of the EMC_CLK3 clock output.	0	R/W
15	-	Reserved.	-	-
18:16	CKE0_DELAY	Delay of the EMC_CKEOUT0 clock enable output.	0	R/W
19	-	Reserved.	-	-
22:20	CKE1_DELAY	Delay of the EMC_CKEOUT1 clock enable output.	0	R/W
23	-	Reserved.	-	-
26:24	CKE2_DELAY	Delay of the EMC_CKEOUT2 clock enable output.	0	R/W
27	-	Reserved.	-	-
30:28	CKE3_DELAY	Delay of the EMC_CKEOUT3 clock enable output.	0	R/W
31	-	Reserved.	-	-

13.4.9 EMC control delay register

This register provides a programmable delay for the EMC control outputs. The delay for each control output is approximately 0.5 ns × XXX_DELAY. (XXX_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

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Table 122. EMC control delay register (EMCCTRLDELAY, address 0x4008 6D04) bit description

Bit	Symbol	Description	Reset value	Access
2:0	RAS_DELAY	Delay of the EMC_RAS output.	0	R/W
3	-	Reserved.	-	-
6:4	CAS_DELAY	Delay of the EMC_CAS output.	0	R/W
7	-	Reserved.	-	-
10:8	OE_DELAY	Delay of the EMC_OE output.	0	R/W
11	-	Reserved.	-	-
14:12	WE_DELAY	Delay of the EMC_WE output.	0	R/W
15	-	Reserved.	-	-
18:16	BLS0_DELAY	Delay of the EMC_BLS0 output.	0	R/W
19	-	Reserved.	-	-
22:20	BLS1_DELAY	Delay of the EMC_BLS1 output.	0	R/W
23	-	Reserved.	-	-
26:24	BLS2_DELAY	Delay of the EMC_BLS2 clock enable output.	0	R/W
27	-	Reserved.	-	-
30:28	BLS3_DELAY	Delay of the EMC_BLS3 clock enable output.	0	R/W
31	-	Reserved.	-	-

13.4.10 EMC chip select delay register

This register provides a programmable delay for the EMC chip select outputs. The delay for each control output is approximately 0.5 ns × XXX_DELAY. (XXX_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

Table 123. EMC chip select delay register (EMCCSDELAY, address 0x4008 6D08) bit description

Bit	Symbol	Description	Reset value	Access
2:0	DYCS0_DELAY	Delay of the EMC_DYCS0 output.	0	R/W
3	-	Reserved.	-	-
6:4	DYCS1_DELAY	Delay of the EMC_DYCS1 output.	0	R/W
7	-	Reserved.	-	-
10:8	DYCS2_DELAY	Delay of the EMC_DYCS2 output.	0	R/W
11	-	Reserved.	-	-
14:12	DYCS3_DELAY	Delay of the EMC_DYCS3 output.	0	R/W
15	-	Reserved.	-	-
18:16	CS0_DELAY	Delay of the EMC_CS0 output.	0	R/W
19	-	Reserved.	-	-
22:20	CS1_DELAY	Delay of the EMC_CS1 output.	0	R/W
23	-	Reserved.	-	-
26:24	CS2_DELAY	Delay of the EMC_CS2 clock enable output.	0	R/W

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Table 123. EMC chip select delay register (EMCCSDELAY, address 0x4008 6D08) bit description ...continued

Bit	Symbol	Description	Reset value	Access
27	-	Reserved.	-	-
30:28	CS3_DELAY	Delay of the EMC_CS3 clock enable output.	0	R/W
31	-	Reserved.	-	-

13.4.11 EMC data out delay register

This register provides a programmable delay for the EMC DQM and EMC data outputs (8 data lanes per delay control). The delay for each control output is approximately 0.5 ns × XXX_DELAY. (XXX_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

Table 124. EMC data out delay register (EMCDOUTDELAY, address 0x4008 6D0C) bit description

Bit	Symbol	Description	Reset value	Access
2:0	DQM0_DELAY	Delay of the EMC_DQM0 output.	0	R/W
3	-	Reserved.	-	-
6:4	DQM1_DELAY	Delay of the EMC_DQM1 output.	0	R/W
7	-	Reserved.	-	-
10:8	DQM2_DELAY	Delay of the EMC_DQM2 output.	0	R/W
11	-	Reserved.	-	-
14:12	DQM3_DELAY	Delay of the EMC_DQM3 output.	0	R/W
15	-	Reserved.	-	-
18:16	D0_DELAY	Delay of the EMC_D0 to EMC_D7 outputs.	0	R/W
19	-	Reserved.	-	-
22:20	D1_DELAY	Delay of the EMC_D8 to EMC_D15 outputs.	0	R/W
23	-	Reserved.	-	-
26:24	D2_DELAY	Delay of the EMC_D16 to EMC_D23 outputs.	0	R/W
27	-	Reserved.	-	-
30:28	D3_DELAY	Delay of the EMC_D24 to EMC_D31 outputs.	0	R/W
31	-	Reserved.	-	-

13.4.12 EMC feedback clock delay register

This register provides a programmable delay for the EMC feedback clocks (8 data lanes per feedback clock). The delay for each control output is approximately 0.5 ns × XXX_DELAY. (XXX_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

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Table 125. EMC DQM delay register (EMCFBCLKDELAY, address 0x4008 6D10) bit description

Bit	Symbol	Description	Reset value	Access
2:0	FBCLK0_DELAY	Delay of the EMC feedback clock 0 (for byte lane 0).	0	R/W
3	-	Reserved.	-	-
6:4	FBCLK1_DELAY	Delay of the EMC feedback clock 1 (for byte lane 1).	0	R/W
7	-	Reserved.	-	-
10:8	FBCLK2_DELAY	Delay of the EMC feedback clock 2 (for byte lane 2).	0	R/W
11	-	Reserved.	-	-
14:12	FBCLK3_DELAY	Delay of the EMC feedback clock 3 (for byte lane 3).	0	R/W
15	-	Reserved.	-	-
18:16	CCLK_DELAY	Delay of the EMC CCLKDELAY clock.	0	R/W
31:19	-	Reserved.	-	-

13.4.13 EMC address delay register 0

This register provides a programmable delay for the EMC address outputs. The delay for each control output is approximately 0.5 ns × ADDRn_DELAY. (ADDRn_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

Table 126. EMC address delay register 0 (EMCADDRDELAY0, address 0x4008 6D14) bit description

Bit	Symbol	Description	Reset value	Access
2:0	ADDR0_DELAY	Delay of the EMC_A0 output.	0	R/W
3	-	Reserved.	-	-
6:4	ADDR1_DELAY	Delay of the EMC_A1 output.	0	R/W
7	-	Reserved.	-	-
10:8	ADDR2_DELAY	Delay of the EMC_A2 output.	0	R/W
11	-	Reserved.	-	-
14:12	ADDR3_DELAY	Delay of the EMC_A3 output.	0	R/W
15	-	Reserved.	-	-
18:16	ADDR4_DELAY	Delay of the EMC_A4 output.	0	R/W
19	-	Reserved.	-	-
22:20	ADDR5_DELAY	Delay of the EMC_A5 output.	0	R/W
23	-	Reserved.	-	-
26:24	ADDR6_DELAY	Delay of the EMC_A6 output.	0	R/W
27	-	Reserved.	-	-
30:28	ADDR7_DELAY	Delay of the EMC_A7 output.	0	R/W
31	-	Reserved.	-	-

13.4.14 EMC address delay register 1

This register provides a programmable delay for the EMC address outputs. The delay for each control output is approximately 0.5 ns × ADDRn_DELAY. (ADDRn_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

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Table 127. EMC address delay register 1 (EMCADDRDELAY1, address 0x4008 6D18) bit description

Bit	Symbol	Description	Reset value	Access
2:0	ADDR8_DELAY	Delay of the EMC_A8 output.	0	R/W
3	-	Reserved.	-	-
6:4	ADDR9_DELAY	Delay of the EMC_A9 output.	0	R/W
7	-	Reserved.	-	-
10:8	ADDR10_DELAY	Delay of the EMC_A10 output.	0	R/W
11	-	Reserved.	-	-
14:12	ADDR11_DELAY	Delay of the EMC_A11 output.	0	R/W
15	-	Reserved.	-	-
18:16	ADDR12_DELAY	Delay of the EMC_A12 output.	0	R/W
19	-	Reserved.	-	-
22:20	ADDR13_DELAY	Delay of the EMC_A13 output.	0	R/W
23	-	Reserved.	-	-
26:24	ADDR14_DELAY	Delay of the EMC_A14 output.	0	R/W
27	-	Reserved.	-	-
30:28	ADDR15_DELAY	Delay of the EMC_A15 output.	0	R/W
31	-	Reserved.	-	-

13.4.15 EMC address delay register 2

This register provides a programmable delay for the EMC address outputs. The delay for each control output is approximately 0.5 ns × ADDRn_DELAY. (ADDRn_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

Table 128. EMC address delay register 2 (EMCADDRDELAY2, address 0x4008 6D1C) bit description

Bit	Symbol	Description	Reset value	Access
2:0	ADDR16_DELAY	Delay of the EMC_A16 output.	0	R/W
3	-	Reserved.	-	-
6:4	ADDR17_DELAY	Delay of the EMC_A17 output.	0	R/W
7	-	Reserved.	-	-
10:8	ADDR18_DELAY	Delay of the EMC_A18 output.	0	R/W
11	-	Reserved.	-	-
14:12	ADDR19_DELAY	Delay of the EMC_A19 output.	0	R/W
15	-	Reserved.	-	-
18:16	ADDR20_DELAY	Delay of the EMC_A20 output.	0	R/W
19	-	Reserved.	-	-
22:20	ADDR21_DELAY	Delay of the EMC_A21 output.	0	R/W
23	-	Reserved.	-	-
26:24	ADDR22_DELAY	Delay of the EMC_A22 output.	0	R/W

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Table 128. EMC address delay register 2 (EMCADDRDELAY2, address 0x4008 6D1C) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
27	-	Reserved.	-	-
30:28	ADDR23_DELAY	Delay of the EMC_A23 output.	0	R/W
31	-	Reserved.	-	-

13.4.16 EMC data in delay register

This register provides a programmable delay for the EMC data inputs (8 data lanes per delay control). The delay for each control output is approximately 0.5 ns × ADDRn_DELAY. (ADDRn_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

Table 129. EMC data in delay register 3 (EMCDINDELAY, address 0x4008 6D24) bit description

Bit	Symbol	Description	Reset value	Access
2:0	DIN0_DELAY	Delay of the EMC_D0 to EMC_D7 inputs.	0	R/W
3	-	Reserved.	-	-
6:4	DIN1_DELAY	Delay of the EMC_D8 to EMC_D15 inputs.	0	R/W
7	-	Reserved.	-	-
10:8	DIN2_DELAY	Delay of the EMC_D23 to EMC_D16 inputs.	0	R/W
11	-	Reserved.	-	-
14:12	DIN3_DELAY	Delay of the EMC_D31 to EMC_D24 inputs.	0	R/W
15	-	Reserved.	-	-
18:16	DEN0_DELAY		0	R/W
19	-	Reserved.	-	-
22:20	DEN1_DELAY	Delay of the data enable lines 8 to 15.	0	R/W
23	-	Reserved.	-	-
26:24	DEN2_DELAY	Delay of the data enable lines 16 to 23.	0	R/W
31:27	-	Reserved.	-	-

13.4.17 Pin interrupt select register 0

This register selects one GPIO pin from all GPIO pins on all ports as the source for pin interrupts 0 to 3.

As an example, for pin interrupt 1, INTPIN1 = 0xA selects GPIO pin GPIO0[10] if PORTSEL1 = 0 or pin GPIO1[10] if PORTSEL = 1. Each pin interrupt must be enabled in the NVIC using interrupt slot # <tbd>.

To enable each pin interrupt and configure its edge or level sensitivity, use the GPIO pin interrupt registers (see <tbd>).

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Table 130. Pin interrupt select register 0 (PINTSEL0, address 0x4008 6E00) bit description

Bit	Symbol	Value	Description	Reset value
4:0	INTPIN0		Pint interrupt 0: Select the pin number within the GPIO port selected by the PORTSEL0 bit in this register.	0
7:5	PORTSEL0		Pin interrupt 0: Select the port for the pin number to be selected in the INTPIN0 bits of this register.	0
		0x0	GPIO Port 0	
		0x1	GPIO Port 1	
		0x2	GPIO Port 2	
		0x3	GPIO Port 3	
		0x4	GPIO Port 4	
		0x5	GPIO Port 5	
		0x6	GPIO Port 6	
		0x7	GPIO Port 7	
12:8	INTPIN1		Pint interrupt 1: Select the pin number within the GPIO port selected by the PORTSEL1 bit in this register.	0
15:13	PORTSEL1		Pin interrupt 1: Select the port for the pin number to be selected in the INTPIN1 bits of this register.	0
		0x0	GPIO Port 0	
		0x1	GPIO Port 1	
		0x2	GPIO Port 2	
		0x3	GPIO Port 3	
		0x4	GPIO Port 4	
		0x5	GPIO Port 5	
		0x6	GPIO Port 6	
		0x7	GPIO Port 7	
20:16	INTPIN2		Pint interrupt 2: Select the pin number within the GPIO port selected by the PORTSEL2 bit in this register.	0
23:21	PORTSEL2		Pin interrupt 2: Select the port for the pin number to be selected in the INTPIN2 bits of this register.	0
		0x0	GPIO Port 0	
		0x1	GPIO Port 1	
		0x2	GPIO Port 2	
		0x3	GPIO Port 3	
		0x4	GPIO Port 4	
		0x5	GPIO Port 5	
		0x6	GPIO Port 6	
		0x7	GPIO Port 7	
28:24	INTPIN3		Pint interrupt 3: Select the pin number within the GPIO port selected by the PORTSEL3 bit in this register.	0

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Table 130. Pin interrupt select register 0 (PINTSEL0, address 0x4008 6E00) bit description

Bit	Symbol	Value	Description	Reset value
31:29	PORTSEL3		Pin interrupt 3: Select the port for the pin number to be selected in the INTPIN3 bits of this register.	0
		0x0	GPIO Port 0	
		0x1	GPIO Port 1	
		0x2	GPIO Port 2	
		0x3	GPIO Port 3	
		0x4	GPIO Port 4	
		0x5	GPIO Port 5	
		0x6	GPIO Port 6	
		0x7	GPIO Port 7	

13.4.18 Pin interrupt select register 1

This register selects one GPIO pin from all GPIO pins on all ports as the source for pin interrupts 4 to 7.

As an example, for pin interrupt 4, INTPIN4 = 0xA selects GPIO pin GPIO0[10] if PORTSEL1 = 0 or pin GPIO1[10] if PORTSEL = 1. Each pin interrupt must be enabled in the NVIC using interrupt slots 32 to 39.

To enable each pin interrupt and configure its edge or level sensitivity, use the GPIO pin interrupt registers (see Section 15.4.1).

Table 131. Pin interrupt select register 1 (PINTSEL1, address 0x4008 6E04) bit description

Bit	Symbol	Value	Description	Reset value
4:0	INTPIN4		Pint interrupt 4: Select the pin number within the GPIO port selected by the PORTSEL4 bit in this register.	0
7:5	PORTSEL4		Pin interrupt 4: Select the port for the pin number to be selected in the INTPIN4 bits of this register.	0
		0x0	GPIO Port 0	
		0x1	GPIO Port 1	
		0x2	GPIO Port 2	
		0x3	GPIO Port 3	
		0x4	GPIO Port 4	
		0x5	GPIO Port 5	
		0x6	GPIO Port 6	
		0x7	GPIO Port 7	
12:8	INTPIN5		Pint interrupt 5: Select the pin number within the GPIO port selected by the PORTSEL5 bit in this register.	0

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Table 131. Pin interrupt select register 1 (PINTSEL1, address 0x4008 6E04) bit description

Bit	Symbol	Value	Description	Reset value
15:13	PORTSEL5		Pin interrupt 5: Select the port for the pin number to be selected in the INTPIN5 bits of this register.	0
		0x0	GPIO Port 0	
		0x1	GPIO Port 1	
		0x2	GPIO Port 2	
		0x3	GPIO Port 3	
		0x4	GPIO Port 4	
		0x5	GPIO Port 5	
		0x6	GPIO Port 6	
		0x7	GPIO Port 7	
20:16	INTPIN6		Pint interrupt 6: Select the pin number within the GPIO port selected by the PORTSEL6 bit in this register.	0
23:21	PORTSEL6		Pin interrupt 6: Select the port for the pin number to be selected in the INTPIN6 bits of this register.	0
		0x0	GPIO Port 0	
		0x1	GPIO Port 1	
		0x2	GPIO Port 2	
		0x3	GPIO Port 3	
		0x4	GPIO Port 4	
		0x5	GPIO Port 5	
		0x6	GPIO Port 6	
		0x7	GPIO Port 7	
28:24	INTPIN7		Pint interrupt 7: Select the pin number within the GPIO port selected by the PORTSEL7 bit in this register.	0
31:29	PORTSEL7		Pin interrupt 7: Select the port for the pin number to be selected in the INTPIN7 bits of this register.	0
		0x0	GPIO Port 0	
		0x1	GPIO Port 1	
		0x2	GPIO Port 2	
		0x3	GPIO Port 3	
		0x4	GPIO Port 4	
		0x5	GPIO Port 5	
		0x6	GPIO Port 6	
		0x7	GPIO Port 7	

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14.1 How to read this chapter

Remark: This chapter describes parts LPC1850/30/20/10 Rev 'A'.

Remark: The VADC block is not available on the LPC1850/30/20/10 Rev 'A'.

14.2 Basic configuration

The GIMA is configured as follows:

- See Table 132 for clocking and power control.
- The GIMA is reset by the GIMA_RST (reset # <tbd>).
- The GIMA outputs are connected to the timer, SCT, ADC, and event router peripherals (see Figure 24 and Figure 25).

Table 132. GIMA clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to GIMA register interface	BASE_M3_CLK	CLK_M3_BUS	150 MHz

14.3 General description

The Global Input Multiplexer Array (GIMA) provides an internal crosslink multiplexer array to connect and synchronize inputs from the pads or internal inputs to event driven peripherals such as the timers, the ADC, or the event router.

The GIMA has 30 outputs, each of which is connected to a peripheral function like a timer capture input or the ADC conversion start input. One register for each output configures the input and controls the synchronizer.

Table 133. GIMA inputs

Input	Source	Possible connections to peripheral blocks			
0	GPIO6[28]	VADC			
1	GPIO5[3]	VADC			
4:2	reserved	-			
5	MCOB2	VADC			
6	pin CTIN_0	T0 CAP0	T1 CAP0	T3 CAP0	SCT CAP0
7	pin CTIN_1	T0 CAP1	T2 CAP1	SCT CAP1	
8	pin CTIN_2	T0 CAP2	SCT CAP2		
9	pin CTIN_3	T1 CAP1	SCT CAP3		
10	pin CTIN_4	T1 CAP2	SCT CAP4		
11	pin CTIN_5	T2 CAP2	SCT CAP5		
12	pin CTIN_6	T3 CAP1	SCT CAP6		
13	pin CTIN_7	T3 CAP2	SCT CAP7		

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Table 133. GIMA inputs

Input	Source	Possible connections to peripheral blocks		
14	T0 MAT0 or CTOUT 0	VADC		
15	T0 MAT2 or CTOUT_2	Event router channel 13		
16	T0 MAT3 or CTOUT 3	T1 CAP3		
17	T1 MAT2 or CTOUT 6	Event router channel 14		
18	T1 MAT3 or CTOUT 7	T2 CAP3		
19	T2 MAT0 or CTOUT 8	VADC	ADC start conversion (START = 0x3)	
20	T2 MAT3 or CTOUT 11	T3 CAP3		
21	T3 MAT2 or CTOUT 14	Event router channel 16		
22	T3 MAT3 or CTOUT 15	T0 CAP3	ADC start conversion (START = 0x2)	
23	U0 TXD	T1 CAP1	SCT CAP3	
24	U0 RXD	T1 CAP2	SCT CAP4	
25	U2 TXD	T0 CAP1	T2 CAP1	SCT CAP1
26	U2 RXD	T2 CAP2	SCT CAP5	
27	U3 TXD	T3 CAP1	SCT CAP6	
28	U3 RXD	T3 CAP2	SCT CAP7	
29	<tbd>I2S0_RX_MWS	T3 CAP0	SCT CAP6	
30	<tbd>I2S0_TX_MWS	T3 CAP1	SCT CAP6	
31	SOF0	T3 CAP2	SCT CAP7	
32	SOF1	T3 CAP3	SCT CAP7	
36:33	Reserved			
37	<tbd>I2S1_RX_MWS	T2 CAP1	SCT CAP3	SCT CAP4
38	<tbd>I2S1_TX_MWS	T2 CAP2	SCT CAP3	SCT CAP4
39	pin T0_CAP0	T0 CAP0		
40	pin T0_CAP1	T0 CAP1		
41	pin T0_CAP2	T0 CAP2		
42	pin T0_CAP3	T0 CAP3		
43	pin T1_CAP0	T1 CAP0		
44	pin T1_CAP1	T1 CAP1		
45	pin T1_CAP2	T1 CAP2		
46	pin T1_CAP3	T1 CAP3		
47	pin T2_CAP0	T2 CAP0		
48	pin T2_CAP1	T2 CAP1		
49	pin T2_CAP2	T2 CAP2		
50	pin T2_CAP3	T2 CAP3		
51	pin T3_CAP0	T3 CAP0		
52	pin T3_CAP1	T3 CAP1		

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Table 133. GIMA inputs

Input	Source	Possible connections to peripheral blocks	
53	pin T3_CAP2	T3 CAP2	
54	pin T3_CAP3	T3 CAP3	
55	T0 MAT0	VADC	ADC start0 conversion (ADC CR register bit START = 0x2)
56	T0 MAT2	Event router channel 13	
57	T0 MAT3	T1 CAP3	
58	T1 MAT2	Event router channel 14	
59	T1 MAT3	T2 CAP3	
60	T2 MAT0	VADC	ADC start1 conversion (ADC CR register bit START = 0x3)
61	T2 MAT3	T3 CAP3	
62	T3 MAT2	Event router channel 16	
63	T3 MAT3	T0 CAP3	

Each GIMA output control consists of five stages:

1. Input selection
2. Input inversion: inverts the path between source and destination.
3. Asynchronous capture
4. Synchronization to peripheral clock
5. Pulse generation

If the source generates shorter pulses than the output clock, the source pulses can be missed. In this case, the asynchronous capture stage can be used to capture the rising edge, the synchronizer stage synchronizes the edge to the peripheral clock and pulse generator stage can optionally generate a singe cycle pulse. (By default the generated pulse is two clock cycles.)

Remark: Use the capture and the synchronizer stage together to avoid the creation of very short, spurious pulses.

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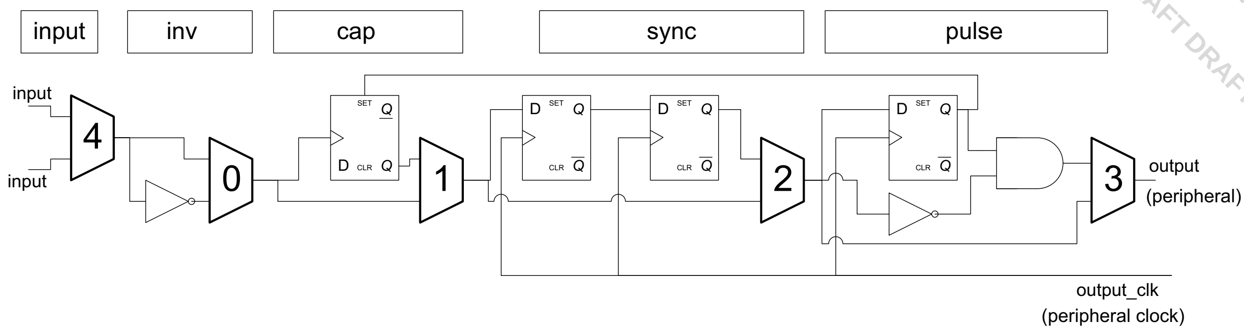


Fig 23. GIMA input stages

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14.3.1 GIMA cross connections

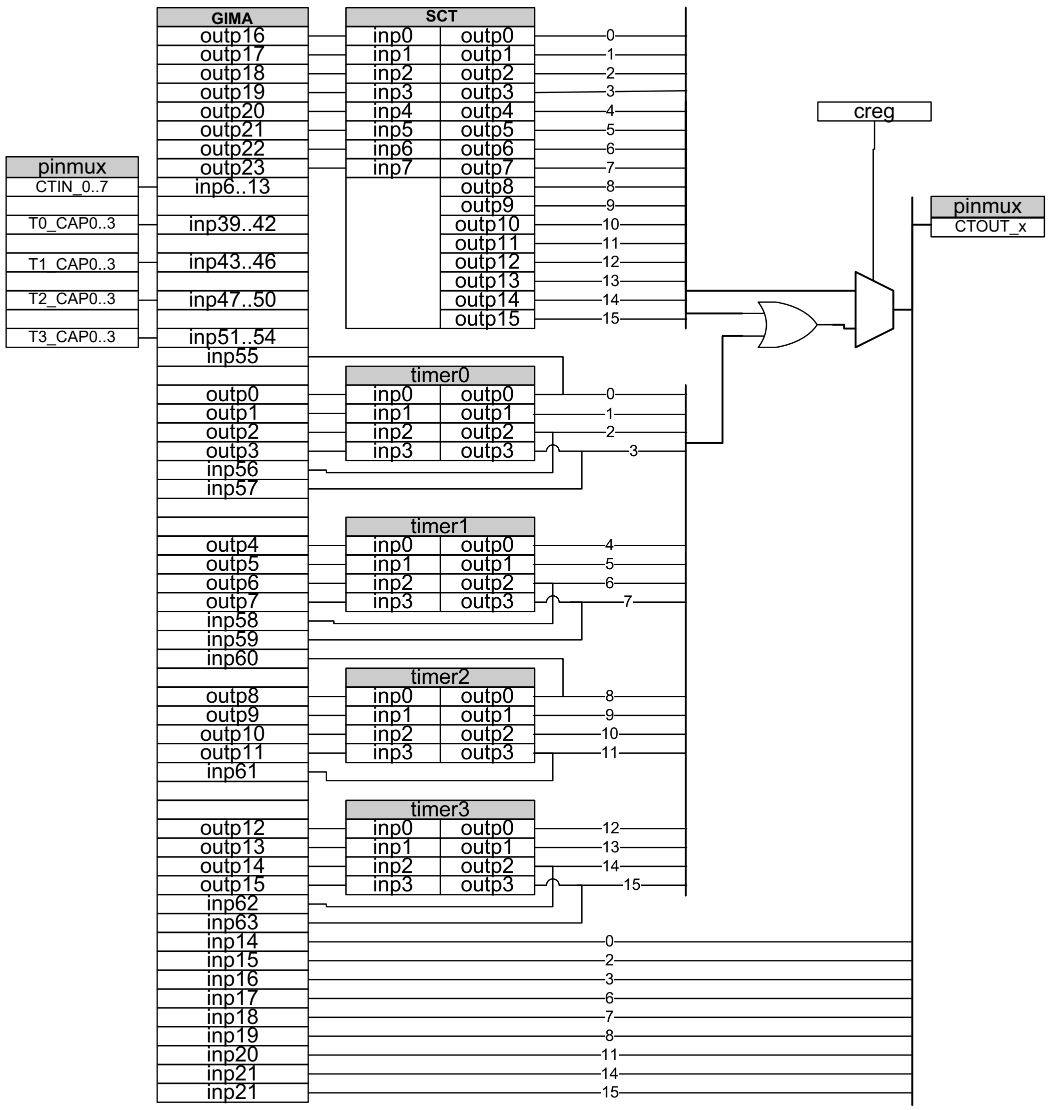


Fig 24. Cross connections between GIMA, SCT, and timer0/1/2/3

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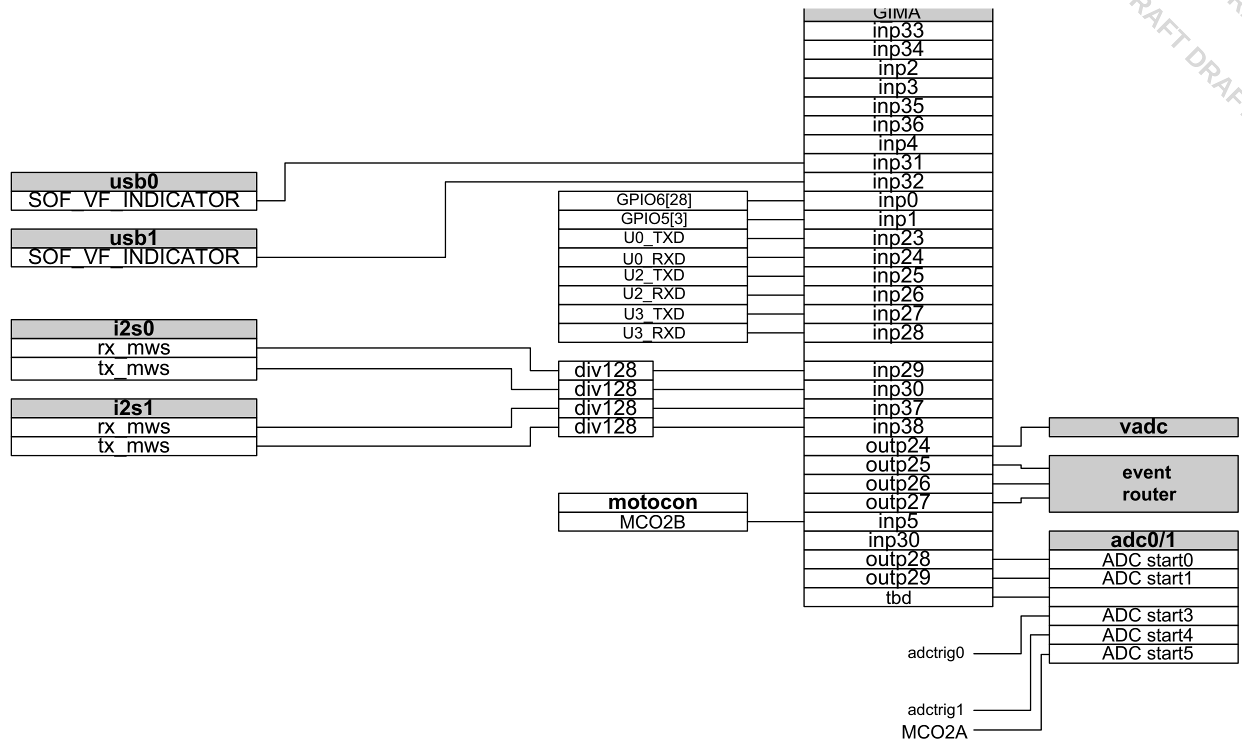


Fig 25. Cross connections between GIMA, ADC, and event router

14.4 Register description

Table 134. Register overview: GIMA (base address: 0x400C 7000)

Name	Access	Address offset	Description	Reset value
CAP0_0_IN	R/W	0x000	Timer 0 CAP0_0 capture input multiplexer (GIMA output 0)	0
CAP0_1_IN	R/W	0x004	Timer 0 CAP0_1 capture input multiplexer (GIMA output 1)	0
CAP0_2_IN	R/W	0x008	Timer 0 CAP0_2 capture input multiplexer (GIMA output 2)	0
CAP0_3_IN	R/W	0x00C	Timer 0 CAP0_3 capture input multiplexer (GIMA output 3)	0
CAP1_0_IN	R/W	0x010	Timer 1 CAP1_0 capture input multiplexer (GIMA output 4)	0
CAP1_1_IN	R/W	0x014	Timer 1 CAP1_1 capture input multiplexer (GIMA output 5)	0
CAP1_2_IN	R/W	0x018	Timer 1 CAP1_2 capture input multiplexer (GIMA output 6)	0
CAP1_3_IN	R/W	0x01C	Timer 1 CAP1_3 capture input multiplexer (GIMA output 7)	0
CAP2_0_IN	R/W	0x020	Timer 2 CAP2_0 capture input multiplexer (GIMA output 8)	0

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Table 134. Register overview: GIMA (base address: 0x400C 7000)

Name	Access	Address offset	Description	Reset value
CAP2_1_IN	R/W	0x024	Timer 2 CAP2_1 capture input multiplexer (GIMA output 9)	0
CAP2_2_IN	R/W	0x028	Timer 2 CAP2_2 capture input multiplexer (GIMA output 10)	0
CAP2_3_IN	R/W	0x02C	Timer 2 CAP2_3 capture input multiplexer (GIMA output 11)	0
CAP3_0_IN	R/W	0x030	Timer 3 CAP3_0 capture input multiplexer (GIMA output 12)	0
CAP3_1_IN	R/W	0x034	Timer 3 CAP3_1 capture input multiplexer (GIMA output 13)	0
CAP3_2_IN	R/W	0x038	Timer 3 CAP3_2 capture input multiplexer (GIMA output 14)	0
CAP3_3_IN	R/W	0x03C	Timer 3 CAP3_3 capture input multiplexer (GIMA output 15)	0
CTIN_0_IN	R/W	0x040	SCT CTIN_0 capture input multiplexer (GIMA output 16)	0
CTIN_1_IN	R/W	0x044	SCT CTIN_1 capture input multiplexer (GIMA output 17)	0
CTIN_2_IN	R/W	0x048	SCT CTIN_2 capture input multiplexer (GIMA output 18)	0
CTIN_3_IN	R/W	0x04C	SCT CTIN_3 capture input multiplexer (GIMA output 19)	0
CTIN_4_IN	R/W	0x050	SCT CTIN_4 capture input multiplexer (GIMA output 20)	0
CTIN_5_IN	R/W	0x054	SCT CTIN_5 capture input multiplexer (GIMA output 21)	0
CTIN_6_IN	R/W	0x058	SCT CTIN_6 capture input multiplexer (GIMA output 22)	0
CTIN_7_IN	R/W	0x05C	SCT CTIN_7 capture input multiplexer (GIMA output 23)	0
VADC_TRIGGER_IN	R/W	0x060	VADC trigger input multiplexer (GIMA output 24)	0
EVENTROUTER_13_IN	R/W	0x064	Event router input 13 multiplexer (GIMA output 25)	0
EVENTROUTER_14_IN	R/W	0x068	Event router input 14 multiplexer (GIMA output 26)	0
EVENTROUTER_16_IN	R/W	0x06C	Event router input 16 multiplexer (GIMA output 27)	0
ADCSTART0_IN	R/W	0x070	ADC start0 input multiplexer (GIMA output 28)	0
ADCSTART1_IN	R/W	0x074	ADC start1 input multiplexer (GIMA output 29)	0

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14.4.1 Timer 0 CAP0_0 capture input multiplexer (CAP0_0_IN)

Table 135. Timer 0 CAP0_0 capture input multiplexer (CAP0_0_IN, address 0x400C 7000) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTIN_0	
		0x1	Reserved	
		0x2	T0_CAP0	
31:8	-		Reserved	

14.4.2 Timer 0 CAP0_1 capture input multiplexer (CAP0_1_IN)

Table 136. Timer 0 CAP0_1 capture input multiplexer (CAP0_1_IN, address 0x400C 7004) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTIN_1	

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Table 136. Timer 0 CAP0_1 capture input multiplexer (CAP0_1_IN, address 0x400C 7004) bit description

Bit	Symbol	Value	Description	Reset value
		0x1	U2_TXD	
		0x2	T0_CAP1	
31:8	-		Reserved	

14.4.3 Timer 0 CAP0_2 capture input multiplexer (CAP0_2_IN)

Table 137. Timer 0 CAP0_2 capture input multiplexer (CAP0_2_IN, address 0x400C 7008) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTIN_2	
		0x1	Reserved	
		0x2	T0_CAP2	
31:8	-		Reserved	

14.4.4 Timer 0 CAP0_3 capture input multiplexer (CAP0_3_IN)

Table 138. Timer 0 CAP0_3 capture input multiplexer (CAP0_3_IN, address 0x400C 700C) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	

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Table 138. Timer 0 CAP0_3 capture input multiplexer (CAP0_3_IN, address 0x400C 700C) bit description

Bit	Symbol	Value	Description	Reset value
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTOUT_15 or T3_MAT3	
		0x1	T0_CAP3	
		0x2	T3_MAT3	
31:8	-		Reserved	

14.4.5 Timer 1 CAP1_0 capture input multiplexer (CAP1_0_IN)

Table 139. Timer 1 CAP1_0 capture input multiplexer (CAP1_0_IN, address 0x400C 7010) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTIN_0	
		0x1	Reserved	
		0x2	T1_CAP0	
31:8	-		Reserved	

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14.4.6 Timer 1 CAP1_1 capture input multiplexer (CAP1_1_IN)

Table 140. Timer 1 CAP1_1 capture input multiplexer (CAP1_1_IN, address 0x400C 7014) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTIN_3	
		0x1	U0_TXD	
		0x2	T1_CAP1	
31:8	-		Reserved	

14.4.7 Timer 1 CAP1_2 capture input multiplexer (CAP1_2_IN)

Table 141. Timer 1 CAP1_2 capture input multiplexer (CAP1_2_IN, address 0x400C 7018) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTIN_4	

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Table 141. Timer 1 CAP1_2 capture input multiplexer (CAP1_2_IN, address 0x400C 7018) bit description

Bit	Symbol	Value	Description	Reset value
		0x1	U0_RXD	
		0x2	T1_CAP2	
31:8	-		Reserved	

14.4.8 Timer 1 CAP1_3 capture input multiplexer (CAP1_3_IN)

Table 142. Timer 1 CAP1_3 capture input multiplexer (CAP1_3_IN, address 0x400C 701C) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTOUT_3 or T0_MAT3	
		0x1	T1_CAP3	
		0x2	T0_MAT3	
31:8	-		Reserved	

14.4.9 Timer 2 CAP2_0 capture input multiplexer (CAP2_0_IN)

Table 143. Timer 2 CAP2_0 capture input multiplexer (CAP2_0_IN, address 0x400C 7020) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	

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Table 143. Timer 2 CAP2_0 capture input multiplexer (CAP2_0_IN, address 0x400C 7020) bit description

Bit	Symbol	Value	Description	Reset value
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x4 to 0xF are reserved.	
		0x0	CTIN_0	
		0x1	Reserved	
		0x2	T2_CAP0	
31:8	-		Reserved	

14.4.10 Timer 2 CAP2_1 capture input multiplexer (CAP2_1_IN)

Table 144. Timer 2 CAP2_1 capture input multiplexer (CAP2_1_IN, address 0x400C 7024) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x4 to 0xF are reserved.	
		0x0	CTIN_1	
		0x1	U2_TXD	
		0x2	<tbd> - I2S1_RX_MWS	
		0x3	T2_CAP1	
31:8	-		Reserved	

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14.4.11 Timer 2 CAP2_2 capture input multiplexer (CAP2_2_IN)

Table 145. Timer 2 CAP2_2 capture input multiplexer (CAP2_2_IN, address 0x400C 7028) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x4 to 0xF are reserved.	
		0x0	CTIN_5	
		0x1	U2_RXD	
		0x2	<tbd> - I2S1_TX_MWS	
		0x3	T2_CAP2	
31:8	-		Reserved	

14.4.12 Timer 2 CAP2_3 capture input multiplexer (CAP2_3_IN)

Table 146. Timer 2 CAP2_3 capture input multiplexer (CAP2_3_IN, address 0x400C 702C) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	

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Table 146. Timer 2 CAP2_3 capture input multiplexer (CAP2_3_IN, address 0x400C 702C) bit description

Bit	Symbol	Value	Description	Reset value
		0x0	CTOUT_7 or T1_MAT3	
		0x1	T2_CAP3	
		0x2	T1_MAT3	
31:8	-		Reserved	

14.4.13 Timer 3 CAP3_0 capture input multiplexer (CAP3_0_IN)

Table 147. Timer 3 CAP3_0 capture input multiplexer (CAP3_0_IN, address 0x400C 7030) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTIN_0	
		0x1	<tbd> I2S0_RX_MWS	
		0x2	T3_CAP0	
31:8	-		Reserved	

14.4.14 Timer 3 CAP3_1 capture input multiplexer (CAP3_1_IN)

Table 148. Timer 3 CAP3_1 capture input multiplexer (CAP3_1_IN, address 0x400C 7034) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	

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Table 148. Timer 3 CAP3_1 capture input multiplexer (CAP3_1_IN, address 0x400C 7034) bit description

Bit	Symbol	Value	Description	Reset value
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x4 to 0xF are reserved.	
		0x0	CTIN_6	
		0x1	U3_TXD	
		0x2	TBD - I2S0_TX_MWS	
		0x3	T3_CAP1	
31:8	-		Reserved	

14.4.15 Timer 3 CAP3_2 capture input multiplexer (CAP3_2_IN)

Table 149. Timer 3 CAP3_2 capture input multiplexer (CAP3_2_IN, address 0x400C 7038) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x4 to 0xF are reserved.	
		0x0	CTIN_7	
		0x1	U3_RXD	
		0x2	SOF0 (Start-Of-Frame USB0)	
		0x3	T3_CAP2	
31:8	-		Reserved	

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14.4.16 Timer 3 CAP3_3 capture input multiplexer (CAP3_3_IN)

Table 150. Timer 3 CAP3_3 capture input multiplexer (CAP3_3_IN, address 0x400C 703C) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x4 to 0xF are reserved.	
		0x0	CTOUT11 or T2_MAT3	
		0x1	SOF1	
		0x2	T3_CAP3	
		0x3	T2_MAT3	
31:8	-		Reserved	

14.4.17 SCT CTIN_0 capture input multiplexer (CTIN_0_IN)

Table 151. SCT CTIN_0 capture input multiplexer (CTIN_0_IN, address 0x400C 7040) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTIN_0	

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Table 151. SCT CTIN_0 capture input multiplexer (CTIN_0_IN, address 0x400C 7040) bit description

Bit	Symbol	Value	Description	Reset value
		0x1	Reserved	
		0x2	Reserved	
31:8	-		Reserved	

14.4.18 SCT CTIN_1 capture input multiplexer (CTIN_1_IN)

Table 152. SCT CTIN_1 capture input multiplexer (CTIN_1_IN, address 0x400C 7044) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTIN_1	
		0x1	U2_TXD	
		0x2	Reserved	
31:8	-		Reserved	

14.4.19 SCT CTIN_2 capture input multiplexer (CTIN_2_IN)

Table 153. SCT CTIN_2 capture input multiplexer (CTIN_2_IN, address 0x400C 7048) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	

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Table 153. SCT CTIN_2 capture input multiplexer (CTIN_2_IN, address 0x400C 7048) bit description

Bit	Symbol	Value	Description	Reset value
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTIN_2	
		0x1	Reserved	
		0x2	Reserved	
31:8	-		Reserved	

14.4.20 SCT CTIN_3 capture input multiplexer (CTIN_3_IN)

Table 154. SCT CTIN_3 capture input multiplexer (CTIN_3_IN, address 0x400C 704C) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x4 to 0xF are reserved.	
		0x0	CTIN_3	
		0x1	U0_TXD	
		0x2	Reserved	
		0x3	Reserved	
31:8	-		Reserved	

14.4.21 SCT CTIN_4 capture input multiplexer (CTIN_4_IN)

Table 155. SCT CTIN_4 capture input multiplexer (CTIN_4_IN, address 0x400C 7050) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	

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Table 155. SCT CTIN_4 capture input multiplexer (CTIN_4_IN, address 0x400C 7050) bit description

Bit	Symbol	Value	Description	Reset value
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x4 to 0xF are reserved.	
		0x0	CTIN_4	
		0x1	U0_RXD	
		0x2	TBD - I2S1_RX_MWS1	
		0x3	TBD - I2S1_TX_MWS1	
31:8	-		Reserved	

14.4.22 SCT CTIN_5 capture input multiplexer (CTIN_5_IN)

Table 156. SCT CTIN_5 capture input multiplexer (CTIN_5_IN, address 0x400C 7054) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTIN_5	
		0x1	U2_RXD	
		0x2	Reserved	
31:8	-		Reserved	

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14.4.23 SCT CTIN_6 capture input multiplexer (CTIN_6_IN)

Table 157. SCT CTIN_6 capture input multiplexer (CTIN_6_IN, address 0x400C 7058) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x4 to 0xF are reserved.	
		0x0	CTIN_6	
		0x1	U3_TXD	
		0x2	TBD - I2S0_RX_MWS	
		0x3	TBD - I2S0_TX_MWS	
31:8	-		Reserved	

14.4.24 SCT CTIN_7 capture input multiplexer (CTIN_7_IN)

Table 158. SCT CTIN_7 capture input multiplexer (CTIN_7_IN, address 0x400C 705C) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x4 to 0xF are reserved.	
		0x0	CTIN_7	
		0x1	U3_RXD	

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Table 158. SCT CTIN_7 capture input multiplexer (CTIN_7_IN, address 0x400C 705C) bit description

Bit	Symbol	Value	Description	Reset value
		0x2	SOF0 (Start-Of-Frame USB0)	
		0x3	SOF1 (Start-Of-Frame USB1)	
31:8	-		Reserved	

14.4.25 VADC trigger input multiplexer (VADC_TRIGGER_IN)

Table 159. ADC trigger input multiplexer (VADC_TRIGGER_IN, address 0x400C 7060) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0xA to 0xF are reserved.	
		0x0	GPIO6[28]	
		0x1	GPIO5[3]	
		0x2	Reserved	
		0x3	Reserved	
		0x4	Reserved	
		0x5	MCOB2	
		0x6	CTOUT_0 or T0_MAT0	
		0x7	CTOUT_8 or T2_MAT0	
		0x8	T0_MAT0	
		0x9	T2_MAT0	
31:8	-		Reserved	

14.4.26 Event router input 13 multiplexer (EVENTROUTER_13_IN)

Table 160. Event router input 13 multiplexer (EVENTROUTER_13_IN, address 0x400C 7064) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	

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Table 160. Event router input 13 multiplexer (EVENTROUTER_13_IN, address 0x400C 7064) bit description

Bit	Symbol	Value	Description	Reset value
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTOUT_2 or T0_MAT2	
		0x1	Reserved	
		0x2	T0_MAT2	
31:8	-		Reserved	

14.4.27 Event router input 14 multiplexer (EVENTROUTER_14_IN)

Table 161. Event router input 14 multiplexer (EVENTROUTER_14_IN, address 0x400C 7068) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x3 to 0xF are reserved.	
		0x0	CTOUT_6 or T1_MAT2	
		0x1	Reserved	
		0x2	T1_MAT2	
31:8	-		Reserved	

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14.4.28 Event router input 16 multiplexer (EVENTROUTER_16_IN)

Table 162. Event router input 16multiplexer (EVENTROUTER_16_IN, address 0x400C 706C) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x2 to 0xF are reserved.	
		0x0	CTOUT_14 or T3_MAT2	
		0x1	T3_MAT2	
31:8	-		Reserved	

14.4.29 ADC start0 input multiplexer (ADCSTART0_IN)

Table 163. ADC start0 input multiplexer (ADCSTART0_IN, address 0x400C 7070) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x2 to 0xF are reserved.	
		0x0	CTOUT_15 or T3_MAT3	
		0x1	T0_MAT0	
31:8	-		Reserved	

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14.4.30 ADC start1 input multiplexer (ADCSTART1_IN)

Table 164. ADC start1 input multiplexer (ADCSTART1_IN, address 0x400C 7074) bit description

Bit	Symbol	Value	Description	Reset value
0	INV		Invert input	
		0	Not inverted.	
		1	Input inverted.	
1	EDGE		Enable rising edge detection	
		0	No edge detection.	
		1	Rising edge detection enabled.	
2	SYNCH		Enable synchronization	
		0	Disable synchronization.	
		1	Enable synchronization.	
3	PULSE		Enable single pulse generation.	
		0	Disable single pulse generation.	
		1	Enable single pulse generation.	
7:4	SELECT		Select input. Values 0x2 to 0xF are reserved.	
		0x0	CTOUT_8 or T2_MAT0	
		0x1	T2_MAT0	
31:8	-		Reserved	

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15.1 How to read this chapter

Remark: This chapter describes the GPIO of the LPC18xx Rev ‘A’ parts. For the GPIO block of the LPC18xx Rev ‘-’ parts, see Section 42.8.

All GPIO register bit descriptions refer to up to 31 pins on each GPIO port. Depending on the package type, not all pins are available, and the corresponding bits in the GPIO registers are reserved (see Table 165).

Table 165. GPIO pins available

	LBGA256	TFBGA180	TFBGA100	LQFP208	LQFP144	LQFP100
GPIO Port 0	GPIO0[15:0]	GPIO0[15:0]	GPIO0[4:0]; GPIO0[15:6]	GPIO0[15:0]	GPIO0[15:0]	GPIO0[4:0]; GPIO0[15:6]
GPIO Port 1	GPIO1[15:0]	GPIO1[15:0]	GPIO1[15:0]	GPIO1[15:0]	GPIO1[15:0]	GPIO1[15:0]
GPIO Port 2	GPIO2[15:0]	GPIO2[15:0]	-	GPIO2[15:0]	GPIO2[15:0]	-
GPIO Port 3	GPIO3[15:0]	GPIO3[15:0]	GPIO3[1:0]; GPIO3[5:3]; GPIO3[7]	GPIO3[15:0]	GPIO3[15:0]	GPIO3[1:0]; GPIO3[5:3]; GPIO3[7]
GPIO Port 4	GPIO4[15:0]	GPIO4[15:0]	-	GPIO4[15:0]	GPIO4[11]	-
GPIO Port 5	GPIO5[26:0]	GPIO5[26:0]	GPIO5[11:0]	GPIO5[26:0]	GPIO5[16:0]; GPIO5[18]	GPIO5[11:0]
GPIO Port 6	GPIO6[30:0]	GPIO6[30:25]	-	GPIO6[30:0]	-	-
GPIO Port 7	GPIO7[25:0]	GPIO7[4:0]	-	GPIO7[25:0]	-	-

15.2 Basic configuration

The GPIO blocks share a common clock and reset connection and are configured as follows:

- See Table 166 for clocking and power control.
- The GPIO is reset by a GPIO_RST (reset #28).
- All GPIO pins are set to input by default.
- For the pin interrupts, select up to 8 external interrupt pins from all GPIO port pins in the SCU (see Table 130 and Table 131). The pin interrupts must be enabled in the NVIC (see Table 13).
- The GPIO group interrupts must be enabled in the NVIC (see Table 13).

Table 166. GPIO clocking and power control

	Base clock	Branch clock	Maximum frequency
GPIO, GPIO pin interrupt, GPIO group0 interrupt, GPIO group1 interrupt	BASE_M3_CLK	CLK_M3_GPIO	150 MHz

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15.3 Features

15.3.1 GPIO pin interrupt features

- Up to 8 pins can be selected from all GPIO pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
- Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
- Level-sensitive interrupt pins can be HIGH- or LOW-active.

15.3.2 GPIO group interrupt features

- The inputs from any number of GPIO pins can be enabled to contribute to a combined group interrupt.
- The polarity of each input enabled for the group interrupt can be configured HIGH or LOW.
- Enabled interrupts can be logically combined through an OR or AND operation.
- Two group interrupts are supported to reflect two distinct interrupt patterns.
- The GPIO group interrupts can wake up the part from sleep, deep-sleep or power-down modes.

15.3.3 GPIO port features

- GPIO pins can be configured as input or output by software.
- All GPIO pins default to inputs with interrupt disabled at reset.
- Pin registers allow pins to be sensed and set individually.

15.4 Introduction

The GPIO pins can be used in several ways to set pins as inputs or outputs and use the inputs as combinations of level and edge sensitive interrupts.

15.4.1 GPIO pin interrupts

From all available GPIO pins, up to eight pins can be selected in the system control block to serve as external interrupt pins (see <tbd>). The external interrupt pins are connected to eight individual interrupts in the NVIC and are created based on rising or falling edges or on the input level on the pin.

15.4.2 GPIO group interrupt

For each port/pin connected to one of the two the GPIO Grouped Interrupt blocks (GROUP0 and GROUP1), the GPIO grouped interrupt registers determine which pins are enabled to generate interrupts and what the active polarities of each of those inputs are.

The GPIO grouped interrupt registers also select whether the interrupt output will be level or edge triggered and whether it will be based on the OR or the AND of all of the enabled inputs.

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When the designated pattern is detected on the selected input pins, the GPIO grouped interrupt block will generate an interrupt. If the part is in a power-savings mode it will first asynchronously wake the part up prior to asserting the interrupt request. The interrupt request line can be cleared by writing a one to the interrupt status bit in the control register.

15.4.3 GPIO port

The GPIO port registers can be used to configure each GPIO pin as input or output and read the state of each pin if the pin is configured as input or set the state of each pin if the pin is configured as output.

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15.5 Register description

The GPIO consists of the following blocks:

- The GPIO pin interrupts block at address 0x4008 7000. Registers in this block enable the up to 8 pin interrupts selected in (see <tbd>) and configure the level and edge sensitivity for each selected pin interrupt. The GPIO interrupt registers are listed in <tbd> and <tbd>
- The GPIO GROUP0 interrupt block at address 0x4008 8000. Registers in this block allow to configure any pin on port 0 and 1 to contribute to a combined interrupt. The GPIO GROUP0 registers are listed in Table 168 and Section 15.5.2.
- The GPIO GROUP1 interrupt block at address 0x4008 9000. Registers in this block allow to configure any pin on port 0 and 1 to contribute to a combined interrupt. The GPIO GROUP1 registers are listed in Table 169 and Section 15.5.2.
- The GPIO port block at address 0x400F 4000. Registers in this block allow to read and write to port pins and configure port pins as inputs or outputs.The GPIO port registers are listed in Table 170 and Section 15.5.3.

Note: In all GPIO registers, bits that are not shown are **reserved**.

Table 167. Register overview: GPIO pin interrupts (base address: 0x4008 7000)

Name	Access	Address offset	Description	Reset value
ISEL	R/W	0x000	Pin Interrupt Mode register	0
IENR	R/W	0x004	Pin Interrupt Enable (Rising) register	0
SIENR	WO	0x008	Set Pin Interrupt Enable (Rising) register	NA
CIENR	WO	0x00C	Clear Pin Interrupt Enable (Rising) register	NA
IENF	R/W	0x010	Pin Interrupt Enable Falling Edge / Active Level register	0
SIENF	WO	0x014	Set Pin Interrupt Enable Falling Edge / Active Level register	NA
CIENF	WO	0x018	Clear Pin Interrupt Enable Falling Edge / Active Level address	NA
RISE	R/W	0x01C	Pin Interrupt Rising Edge register	0
FALL	R/W	0x020	Pin Interrupt Falling Edge register	0
IST	R/W	0x024	Pin Interrupt Status register	0

Table 168. Register overview: GPIO GROUP0 interrupt (base address 0x4008 8000)

Name	Access	Address offset	Description	Reset value
CTRL	R/W	0x000	GPIO grouped interrupt control register	0
PORT_POL0	R/W	0x020	GPIO grouped interrupt port 0 polarity register	0xFFFF FFFF
PORT_POL1	R/W	0x024	GPIO grouped interrupt port 1 polarity register	0xFFFF FFFF
PORT_POL2	R/W	0x028	GPIO grouped interrupt port 2 polarity register	0xFFFF FFFF

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Table 168. Register overview: GPIO GROUP0 interrupt (base address 0x4008 8000)

Name	Access	Address offset	Description	Reset value
PORT_POL3	R/W	0x02C	GPIO grouped interrupt port 3 polarity register	0xFFFF FFFF
PORT_POL4	R/W	0x030	GPIO grouped interrupt port 4 polarity register	0xFFFF FFFF
PORT_POL5	R/W	0x034	GPIO grouped interrupt port 5 polarity register	0xFFFF FFFF
PORT_POL6	R/W	0x038	GPIO grouped interrupt port 6 polarity register	0xFFFF FFFF
PORT_POL7	R/W	0x03C	GPIO grouped interrupt port 7 polarity register	0xFFFF FFFF
PORT_ENA0	R/W	0x040	GPIO grouped interrupt port 0 enable register	0
PORT_ENA1	R/W	0x044	GPIO grouped interrupt port 1 enable register	0
PORT_ENA2	R/W	0x048	GPIO grouped interrupt port 2 enable register	0
PORT_ENA3	R/W	0x04C	GPIO grouped interrupt port 3 enable register	0
PORT_ENA4	R/W	0x050	GPIO grouped interrupt port 4 enable register	0
PORT_ENA5	R/W	0x054	GPIO grouped interrupt port 5 enable register	0
PORT_ENA6	R/W	0x058	GPIO grouped interrupt port 5 enable register	0
PORT_ENA7	R/W	0x05C	GPIO grouped interrupt port 5 enable register	0

Table 169. Register overview: GPIO GROUP1 interrupt (base address 0x4008 9000)

Name	Access	Address offset	Description	Reset value
CTRL	R/W	0x000	GPIO grouped interrupt control register	0
PORT_POL0	R/W	0x020	GPIO grouped interrupt port 0 polarity register	0xFFFF FFFF
PORT_POL1	R/W	0x024	GPIO grouped interrupt port 1 polarity register	0xFFFF FFFF
PORT_POL2	R/W	0x028	GPIO grouped interrupt port 2 polarity register	0xFFFF FFFF
PORT_POL3	R/W	0x02C	GPIO grouped interrupt port 3 polarity register	0xFFFF FFFF
PORT_POL4	R/W	0x030	GPIO grouped interrupt port 4 polarity register	0xFFFF FFFF
PORT_POL5	R/W	0x034	GPIO grouped interrupt port 5 polarity register	0xFFFF FFFF
PORT_POL6	R/W	0x038	GPIO grouped interrupt port 6 polarity register	0xFFFF FFFF
PORT_POL7	R/W	0x03C	GPIO grouped interrupt port 7 polarity register	0xFFFF FFFF
PORT_ENA0	R/W	0x040	GPIO grouped interrupt port 0 enable register	0
PORT_ENA1	R/W	0x044	GPIO grouped interrupt port 1 enable register	0
PORT_ENA2	R/W	0x048	GPIO grouped interrupt port 2 enable register	0
PORT_ENA3	R/W	0x04C	GPIO grouped interrupt port 3 enable register	0
PORT_ENA4	R/W	0x050	GPIO grouped interrupt port 4 enable register	0

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Table 169. Register overview: GPIO GROUP1 interrupt (base address 0x4008 9000)

Name	Access	Address offset	Description	Reset value
PORT_ENA5	R/W	0x054	GPIO grouped interrupt port 5 enable register	0
PORT_ENA6	R/W	0x058	GPIO grouped interrupt port 5 enable register	0
PORT_ENA7	R/W	0x05C	GPIO grouped interrupt port 5 enable register	0

GPIO port addresses can be read and written as bytes, halfwords, or words.

Table 170. Register overview: GPIO port (base address 0x400F 4000)

Name	Access	Address offset	Description	Reset value	Width
B0 to B31	R/W	0x0000 to x001F	Byte pin registers port 0; pins PIO0_0 to PIO0_31	ext[1]	byte (8 bit)
B32 to Bx	R/W	0x0020 to 0x003F	Byte pin registers port 1	ext[1]	byte (8 bit)
B64 to Bx	R/W	0x0040 to 0x005F	Byte pin registers port 2	ext[1]	byte (8 bit)
B96 to Bx	R/W	0x0060 to 0x007F	Byte pin registers port 3	ext[1]	byte (8 bit)
B128 to Bx	R/W	0x0080 to 0x009F	Byte pin registers port 4	ext[1]	byte (8 bit)
B160 to Bx	R/W	0x00A0 to 0x00BF	Byte pin registers port 5	ext[1]	byte (8 bit)
B192 to Bx	R/W	0x00C0 to0x00DF	Byte pin registers port 6	ext[1]	byte (8 bit)
B224 to Bx	R/W	0x00E0 to 0x00FC	Byte pin registers port 7	ext[1]	byte (8 bit)
W0 to Wx	R/W	0x1000 to 0x107C	Word pin registers port 0	ext[1]	word (32 bit)
W32 to Wx	R/W	0x1080 to 0x10FC	Word pin registers port 1	ext[1]	word (32 bit)
W64 to Wx	R/W	0x1100 to 0x11FC	Word pin registers port 2	ext[1]	word (32 bit)
W96 to Wx	R/W	0x1180 to 0x11FC	Word pin registers port 3	ext[1]	word (32 bit)
W128 to Wx	R/W	0x1200 to 0x12FC	Word pin registers port 4	ext[1]	word (32 bit)
W160 to Wx	R/W	0x1280 to 0x12FC	Word pin registers port 5	ext[1]	word (32 bit)
W192 to Wx	R/W	0x1300 to 0x137C	Word pin registers port 6	ext[1]	word (32 bit)
W224 to Wx	R/W	0x1380 to 0x13FC	Word pin registers port 7	ext[1]	word (32 bit)
DIR0	R/W	0x2000	Direction registers port 0	0	word (32 bit)
DIR1	R/W	0x2004	Direction registers port 1	0	word (32 bit)
DIR2	R/W	0x2008	Direction registers port 2	0	word (32 bit)
DIR3	R/W	0x200C	Direction registers port 3	0	word (32 bit)
DIR4	R/W	0x2010	Direction registers port 4	0	word (32 bit)
DIR5	R/W	0x2014	Direction registers port 5	0	word (32 bit)
DIR6	R/W	0x2018	Direction registers port 6	0	word (32 bit)
DIR7	R/W	0x201C	Direction registers port 7	0	word (32 bit)
MASK0	R/W	0x2080	Mask register port 0	0	word (32 bit)
MASK1	R/W	0x2084	Mask register port 1	0	word (32 bit)
MASK2	R/W	0x2088	Mask register port 2	0	word (32 bit)
MASK3	R/W	0x208C	Mask register port 3	0	word (32 bit)
MASK4	R/W	0x2090	Mask register port 4	0	word (32 bit)
MASK5	R/W	0x2094	Mask register port 5	0	word (32 bit)
MASK6	R/W	0x2098	Mask register port 6	0	word (32 bit)
MASK7	R/W	0x209C	Mask register port 7	0	word (32 bit)

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Table 170. Register overview: GPIO port (base address 0x400F 4000)

Name	Access	Address offset	Description	Reset value	Width
PIN0	R/W	0x2100	Port pin register port 0	ext[1]	word (32 bit)
PIN1	R/W	0x2104	Port pin register port 1	ext[1]	word (32 bit)
PIN2	R/W	0x2108	Port pin register port 2	ext[1]	word (32 bit)
PIN3	R/W	0x210C	Port pin register port 3	ext[1]	word (32 bit)
PIN4	R/W	0x2110	Port pin register port 4	ext[1]	word (32 bit)
PIN5	R/W	0x2114	Port pin register port 5	ext[1]	word (32 bit)
PIN6	R/W	0x2118	Port pin register port 6	ext[1]	word (32 bit)
PIN7	R/W	0x211C	Port pin register port 7	ext[1]	word (32 bit)
MPIN0	R/W	0x2180	Masked port register port 0	ext[1]	word (32 bit)
MPIN1	R/W	0x2184	Masked port register port 1	ext[1]	word (32 bit)
MPIN2	R/W	0x2188	Masked port register port 2	ext[1]	word (32 bit)
MPIN3	R/W	0x218C	Masked port register port 3	ext[1]	word (32 bit)
MPIN4	R/W	0x2190	Masked port register port 4	ext[1]	word (32 bit)
MPIN5	R/W	0x2194	Masked port register port 5	ext[1]	word (32 bit)
MPIN6	R/W	0x2198	Masked port register port 6	ext[1]	word (32 bit)
MPIN7	R/W	0x219C	Masked port register port 7	ext[1]	word (32 bit)
SET0	R/W	0x2200	Write: Set register for port 0 Read: output bits for port 0	0	word (32 bit)
SET1	R/W	0x2204	Write: Set register for port 1 Read: output bits for port 1	0	word (32 bit)
SET2	R/W	0x2208	Write: Set register for port 2 Read: output bits for port 2	0	word (32 bit)
SET3	R/W	0x220C	Write: Set register for port 3 Read: output bits for port 3	0	word (32 bit)
SET4	R/W	0x2210	Write: Set register for port 4 Read: output bits for port 4	0	word (32 bit)
SET5	R/W	0x2214	Write: Set register for port 5 Read: output bits for port 5	0	word (32 bit)
SET6	R/W	0x2218	Write: Set register for port 6 Read: output bits for port 6	0	word (32 bit)
SET7	R/W	0x221C	Write: Set register for port 7 Read: output bits for port 7	0	word (32 bit)
CLR0	WO	0x2280	Clear port 0	NA	word (32 bit)
CLR1	WO	0x2284	Clear port 1	NA	word (32 bit)
CLR2	WO	0x2288	Clear port 2	NA	word (32 bit)
CLR3	WO	0x228C	Clear port 3	NA	word (32 bit)
CLR4	WO	0x2290	Clear port 4	NA	word (32 bit)
CLR5	WO	0x2294	Clear port 5	NA	word (32 bit)
CLR6	WO	0x2298	Clear port 6	NA	word (32 bit)
CLR7	WO	0x229C	Clear port 7	NA	word (32 bit)
NOT0	WO	0x2300	Toggle port 0	NA	word (32 bit)
NOT1	WO	0x2304	Toggle port 1	NA	word (32 bit)

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Table 170. Register overview: GPIO port (base address 0x400F 4000)

Name	Access	Address offset	Description	Reset value	Width
NOT2	WO	0x2308	Toggle port 2	NA	word (32 bit)
NOT3	WO	0x230C	Toggle port 3	NA	word (32 bit)
NOT4	WO	0x2310	Toggle port 4	NA	word (32 bit)
NOT5	WO	0x2314	Toggle port 5	NA	word (32 bit)
NOT6	WO	0x2318	Toggle port 6	NA	word (32 bit)
NOT7	WO	0x231C	Toggle port 7	NA	word (32 bit)

[1] “ext” in this table and subsequent tables indicates that the data read after reset depends on the state of the pin, which in turn may depend on an external source.

15.5.1 GPIO pin interrupts register description

15.5.1.1 Pin interrupt mode register

For each of the 8 pin interrupts selected in Table 130 and Table 131, one bit in the ISEL register determines whether the interrupt is edge or level sensitive.

Table 171. Pin interrupt mode register (ISEL, address 0x4008 7000) bit description

Bit	Symbol	Description	Reset value	Access
7:0	PMODE	Selects the interrupt mode for each pin interrupt. Bit n configures the pin interrupt selected in PINTSELn. 0 = Edge sensitive 1 = Level sensitive	0	R/W
31:8	-	Reserved.	-	-

15.5.1.2 Pin interrupt level (rising edge interrupt) enable register

For each of the 8 pin interrupts selected in the PINTSEL registers (see Table 130 and Table 131), one bit in the IENR register enables the interrupt depending on the pin interrupt mode configured in the ISEL register:

- If the pin interrupt mode is edge sensitive (PMODE = 0), the rising edge interrupt is enabled.
- If the pin interrupt mode is level sensitive (PMODE = 1), the level interrupt is enabled. The PINTEN_F register configures the active level (HIGH or LOW) for this interrupt.

Table 172. Pin interrupt level (rising edge interrupt enable) register (IENR, address 0x4008 7004) bit description

Bit	Symbol	Description	Reset value	Access
7:0	ENRL	Enables the rising edge or level interrupt for each pin interrupt. Bit n configures the pin interrupt selected in PINTSELn. 0 = Disable rising edge or level interrupt. 1 = Enable rising edge or level interrupt.	0	R/W
31:8	-	Reserved.	-	-

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15.5.1.3 Pin interrupt level (rising edge interrupt) set register

For each of the 8 pin interrupts selected in the PINTSEL registers (see Table 130 and Table 131), one bit in the SIENR register sets the corresponding bit in the IENR register depending on the pin interrupt mode configured in the PINTMODE register:

- If the pin interrupt mode is edge sensitive (PMODE = 0), the rising edge interrupt is set.
- If the pin interrupt mode is level sensitive (PMODE = 1), the level interrupt is set.

Table 173. Pin interrupt level (rising edge interrupt) set register (SIENR, address 0x4008 7008) bit description

Bit	Symbol	Description	Reset value	Access
7:0	SETENRL	Ones written to this address set bits in the PINTEN_R, thus enabling interrupts. Bit n sets bit n in the PINTEN_R register. 0 = No operation. 1 = Enable rising edge or level interrupt.	NA	WO
31:8	-	Reserved.	-	-

15.5.1.4 Pin interrupt level (rising edge interrupt) clear register

For each of the 8 pin interrupts selected in the PINTSEL registers (see Table 130 and Table 131), one bit in the CIENR register clears the corresponding bit in the IENR register depending on the pin interrupt mode configured in the ISEL register:

- If the pin interrupt mode is edge sensitive (PMODE = 0), the rising edge interrupt is cleared.
- If the pin interrupt mode is level sensitive (PMODE = 1), the level interrupt is cleared.

Table 174. Pin interrupt level (rising edge interrupt) clear register (PCIENR, address 0x4008 700C) bit description

Bit	Symbol	Description	Reset value	Access
7:0	CENRL	Ones written to this address clear bits in the IENR, thus disabling the interrupts. Bit n clears bit n in the IENR register. 0 = No operation. 1 = Disable rising edge or level interrupt.	NA	WO
31:8	-	Reserved.	-	-

15.5.1.5 Pin interrupt active level (falling edge interrupt enable) register

For each of the 8 pin interrupts selected in the PINTSEL registers (see Table 130 and Table 131), one bit in the PINTSEN_F register enables the falling edge interrupt or the configures the level sensitivity depending on the pin interrupt mode configured in the ISEL register:

- If the pin interrupt mode is edge sensitive (PMODE = 0), the falling edge interrupt is enabled.
- If the pin interrupt mode is level sensitive (PMODE = 1), the active level of the level interrupt (HIGH or LOW) is configured.

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Table 175. Pin interrupt active level (falling edge interrupt enable) register (IENF, address 0x4008 7010) bit description

Bit	Symbol	Description	Reset value	Access
7:0	ENAF	Enables the falling edge or configures the active level interrupt for each pin interrupt. Bit n configures the pin interrupt selected in PINTSELn. 0 = Disable falling edge interrupt or set active interrupt level LOW. 1 = Enable falling edge interrupt enabled or set active interrupt level HIGH.	0	R/W
31:8	-	Reserved.	-	-

15.5.1.6 Pin interrupt active level (falling edge interrupt) set register

For each of the 8 pin interrupts selected in the PINTSEL registers (see Table 130 and Table 131), one bit in the SIENF register sets the corresponding bit in the IENF register depending on the pin interrupt mode configured in the ISEL register:

- If the pin interrupt mode is edge sensitive (PMODE = 0), the falling edge interrupt is set.
- If the pin interrupt mode is level sensitive (PMODE = 1), the HIGH-active interrupt is selected.

Table 176. Pin interrupt active level (falling edge interrupt) set register (SIENF, address 0x4008 7014) bit description

Bit	Symbol	Description	Reset value	Access
7:0	SETENAF	Ones written to this address set bits in the IENF, thus enabling interrupts. Bit n sets bit n in the IENF register. 0 = No operation. 1 = Select HIGH-active interrupt or enable falling edge interrupt.	NA	WO
31:8	-	Reserved.	-	-

15.5.1.7 Pin interrupt active level (falling edge interrupt) clear register

For each of the 8 pin interrupts selected in the PINTSEL registers (see Table 130 and Table 131), one bit in the CIENF register sets the corresponding bit in the IENF register depending on the pin interrupt mode configured in the ISEL register:

- If the pin interrupt mode is edge sensitive (PMODE = 0), the falling edge interrupt is cleared.
- If the pin interrupt mode is level sensitive (PMODE = 1), the LOW-active interrupt is selected.

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Table 177. Pin interrupt active level (falling edge interrupt) clear register (CIENF, address 0x4008 7018) bit description

Bit	Symbol	Description	Reset value	Access
7:0	CENAF	Ones written to this address clears bits in the IENF, thus disabling interrupts. Bit n clears bit n in the IENF register. 0 = No operation. 1 = LOW-active interrupt selected or falling edge interrupt disabled.	NA	WO
31:8	-	Reserved.	-	-

15.5.1.8 Pin interrupt rising edge register

This register contains ones for pin interrupts selected in the PINTSEL registers (see Table 130 and Table 131) on which a rising edge has been detected. Writing ones to this register clears rising edge detection. Ones in this register assert an interrupt request for pins that are enabled for rising-edge interrupts. All edges are detected for all pins selected by the PINTSEL registers, regardless of whether they are interrupt-enabled.

Table 178. Pin interrupt rising edge register (RISE, address 0x4008 701C) bit description

Bit	Symbol	Description	Reset value	Access
7:0	RDET	Rising edge detect. Bit n detects the rising edge of the pin selected in PINTSELn. Read 0: No rising edge has been detected on this pin since Reset or the last time a one was written to this bit. Write 0: no operation. Read 1: a rising edge has been detected since Reset or the last time a one was written to this bit. Write 1: clear rising edge detection for this pin.	0	R/W
31:8	-	Reserved.	-	-

15.5.1.9 Pin interrupt falling edge register

This register contains ones for pin interrupts selected in the PINTSEL registers (see Table 130 and Table 131) on which a falling edge has been detected. Writing ones to this register clears falling edge detection. Ones in this register assert an interrupt request for pins that are enabled for falling-edge interrupts. All edges are detected for all pins selected by the PINTSEL registers, regardless of whether they are interrupt-enabled.

Table 179. Pin interrupt falling edge register (FALL, address 0x4008 7020) bit description

Bit	Symbol	Description	Reset value	Access
7:0	FDET	Falling edge detect. Bit n detects the falling edge of the pin selected in PINTSELn. Read 0: No falling edge has been detected on this pin since Reset or the last time a one was written to this bit. Write 0: no operation. Read 1: a falling edge has been detected since Reset or the last time a one was written to this bit. Write 1: clear falling edge detection for this pin.	0	R/W
31:8	-	Reserved.	-	-

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15.5.1.10 Pin interrupt status register

Reading this register returns ones for pin interrupts that are currently requesting an interrupt. For pins identified as edge-sensitive in the Interrupt Select register, writing ones to this register clears both rising- and falling-edge detection for the pin. For level-sensitive pins, writing ones inverts the corresponding bit in the Active level register, thus switching the active level on the pin.

Table 180. Pin interrupt status register (IST address 0x4008 7024) bit description

Bit	Symbol	Description	Reset value	Access
7:0	PSTAT	Pin interrupt status. Bit n returns the status, clears the edge interrupt, or inverts the active level of the pin selected in PINTSELn. Read 0: interrupt is not being requested for this interrupt pin. Write 0: no operation. Read 1: interrupt is being requested for this interrupt pin. Write 1 (edge-sensitive): clear rising- and falling-edge detection for this pin. Write 1 (level-sensitive): switch the active level for this pin (in the PINTENT_F register).	0	R/W
31:8	-	Reserved.	-	-

15.5.2 GPIO GROUP0/GROUP1 interrupt register description

15.5.2.1 Grouped interrupt control register

Table 181. GPIO grouped interrupt control register (CTRL, addresses 0x4008 8000 (GROUP0 INT) and 0x4008 9000 (GROUP1 INT)) bit description

Bit	Symbol	Value	Description	Reset value
0	INT		Group interrupt status. This bit is cleared by writing a one to it. Writing zero has no effect.	0
		0	No interrupt request is pending.	
		1	Interrupt request is active.	
1	COMB		Combine enabled inputs for group interrupt	0
		0	OR functionality: A grouped interrupt is generated when any one of the enabled inputs is active (based on its programmed polarity).	
		1	AND functionality: An interrupt is generated when all enabled bits are active (based on their programmed polarity).	
2	TRIG		Group interrupt trigger	0
		0	Edge-triggered	
		1	Level-triggered	
31:3	-	-	Reserved	0

15.5.2.2 GPIO grouped interrupt port polarity registers

The grouped interrupt port polarity registers determine how the polarity of each enabled pin contributes to the grouped interrupt. Each port n (n = 0 to 7) is associated with its own port polarity register, and the values of all registers together determine the grouped interrupt.

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Table 182. GPIO grouped interrupt port polarity registers (PORT_POL, addresses 0x4008 8020 (PORT_POL0) to 0x4008 803C (PORT_POL7) (GROUP0 INT) and 0x4008 9020 (PORT_POL0) to 0x4008 903C (PORT_POL7) (GROUP1 INT)) bit description

Bit	Symbol	Description	Reset value	Access
31:0	POL	Configure pin polarity of port n pins for group interrupt. Bit m corresponds to pin GPIOn[m] of port n. 0 = the pin is active LOW. If the level on this pin is LOW, the pin contributes to the group interrupt. 1 = the pin is active HIGH. If the level on this pin is HIGH, the pin contributes to the group interrupt.	1	-

15.5.2.3 GPIO grouped interrupt port enable registers

The grouped interrupt port enable registers enable the pins which contribute to the grouped interrupt. Each port n (n = 0 to 7) is associated with its own port enable register, and the values of all registers together determine which pins contribute to the grouped interrupt.

Table 183. GPIO grouped interrupt port n enable registers (PORT_ENA, addresses 0x4008 8040 (PORT_ENA0) to 0x4008 805C (PORT_ENA7) (GROUP0 INT) and 0x4008 9040 (PORT_ENA0) to 0x4008 905C (PORT_ENA7) (GROUP1 INT)) bit description

Bit	Symbol	Description	Reset value	Access
31:0	ENA	Enable port n pin for group interrupt. Bit m corresponds to pin GPIOPn[m] of port n. 0 = the port n pin is disabled and does not contribute to the grouped interrupt. 1 = the port n pin is enabled and contributes to the grouped interrupt.	0	-

15.5.3 GPIO port register description

15.5.3.1 GPIO port byte pin registers

Each GPIO pin GPIOn[m] has a byte register in this address range. The byte pin registers of GPIO port 0 correspond to registers B0 to B31, the byte pin registers of GPIO port 1 correspond to registers B32 to B63, etc.. Byte addresses are reserved for unused GPIO port pins (see Table 165).

Software typically reads and writes bytes to access individual pins but also can read or write halfwords to sense or set the state of two pins, and read or write words to sense or set the state of four pins.

Table 184. GPIO port byte pin registers (B, addresses 0x400F 4000 (B0) to 0x400F 00FC (B255)) bit description

Bit	Symbol	Description	Reset value	Access
0	PBYTE	Read: state of the pin GPIOn[m], regardless of direction, masking, or alternate function. Pins configured as analog I/O always read as 0. Write: loads the pin's output bit.	ext	R/W
7:1		Reserved (0 on read, ignored on write)	0	-

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15.5.3.2 GPIO port word pin registers

Each GPIO pin GPIOn[m] has a word register in this address range. The word pin registers of GPIO port 0 correspond to registers W0 to W31, the word pin registers of GPIO port 1 correspond to registers W32 to W63, etc.. Word addresses are reserved for unused GPIO port pins (see Table 165).

Any byte, halfword, or word read in this range will be all zeros if the pin is low or all ones if the pin is high, regardless of direction, masking, or alternate function, except that pins configured as analog I/O always read as zeros. Any write will clear the pin's output bit if the value written is all zeros, else it will set the pin's output bit.

Table 185. GPIO port word pin registers (W, addresses 0x400F 5000 (W0) to 0x400F 13FC (W255)) bit description

Bit	Symbol	Description	Reset value	Access
31:0	PWORD	Read 0: pin GPIOn[m] is LOW. Write 0: clear output bit. Read 0xFFFF FFFF: pin is HIGH. Write any value 0x0000 0001 to 0xFFFF FFFF: set output bit. **Remark:** Only 0 or 0xFFFF FFFF can be read. Writing any value other than 0 will set the output bit.	ext	R/W

15.5.3.3 GPIO port direction registers

Each GPIO port n (n = 0 to 7) has one direction register for configuring the port pins as inputs or outputs.

Table 186. GPIO port direction register (DIR, addresses 0x400F 6000 (DIR0) to 0x400F 601C (DIR7)) bit description

Bit	Symbol	Description	Reset value	Access
31:0	DIR	Selects pin direction for pin GPIOn[m] (bit 0 = GPIOn[0], bit 1 = GPIOn[1], ..., bit 31 = GPIOn[31]). 0 = input. 1 = output.	0	R/W

15.5.3.4 GPIO port mask registers

Each GPIO port has one mask register. The mask registers affect writing and reading the MPORT registers. Zeroes in these registers enable reading and writing; ones disable writing and result in zeros in corresponding positions when reading.

Table 187. GPIO port mask register (MASK, addresses 0x400F 6080 (MASK0) to 0x400F 609C (MASK7)) bit description

Bit	Symbol	Description	Reset value	Access
31:0	MASK	Controls which bits corresponding to GPIOn[m] are active in the MPORT register (bit 0 = GPIOn[0], bit 1 = GPIOn[1], ..., bit 31 = GPIOn[31]). 0 = Read MPORT: pin state; write MPORT: load output bit. 1 = Read MPORT: 0; write MPORT: output bit not affected.	0	R/W

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15.5.3.5 GPIO port pin registers

Each GPIO port has one port pin register. Reading these registers returns the current state of the pins read, regardless of direction, masking, or alternate functions, except that pins configured as analog I/O always read as 0s. Writing these registers loads the output bits of the pins written to, regardless of the Mask register.

Table 188. GPIO port pin register (PIN, addresses 0x400F 6100 (PIN0) to 0x400F 611C (PIN7)) bit description

Bit	Symbol	Description	Reset value	Access
31:0	PORT	Reads pin states or loads output bits (bit 0 = GPIOn[0], bit 1 = GPIOn[1], ..., bit 31 = GPIOn[31]). 0 = Read: pin is LOW; write: clear output bit. 1 = Read: pin is HIGH; write: set output bit.	ext	R/W

15.5.3.6 GPIO masked port pin registers

Each GPIO port has one masked port pin register. These registers are similar to the PORT registers, except that the value read is masked by ANDing with the inverted contents of the corresponding MASK register, and writing to one of these registers only affects output register bits that are enabled by zeros in the corresponding MASK register.

Table 189. GPIO masked port pin register (MPIN, addresses 0x400F 6180 (MPIN0) to 0x400F 619C (MPIN7)) bit description

Bit	Symbol	Description	Reset value	Access
31:0	MPORT	Masked port register (bit 0 = GPIOn[0], bit 1 = GPIOn[1], ..., bit 31 = GPIOn[31]). 0 = Read: pin is LOW and/or the corresponding bit in the MASK register is 1; write: clear output bit if the corresponding bit in the MASK register is 0. 1 = Read: pin is HIGH and the corresponding bit in the MASK register is 0; write: set output bit if the corresponding bit in the MASK register is 0.	ext	R/W

15.5.3.7 GPIO port set registers

Each GPIO port has one port set register. Output bits can be set by writing ones to these registers, regardless of MASK registers. Reading from these register returns the port’s output bits, regardless of pin directions.

Table 190. GPIO port set register (SET, addresses 0x400F 6200 (SET0) to 0x400F 621C (SET7)) bit description

Bit	Symbol	Description	Reset value	Access
31:0	SET	Read or set output bits (bit 0 = GPIOn[0], bit 1 = GPIOn[1], ..., bit 31 = GPIOn[31]). 0 = Read: output bit: write: no operation. 1 = Read: output bit; write: set output bit.	0	R/W

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15.5.3.8 GPIO port clear registers

Each GPIO port has one output clear register. Output bits can be cleared by writing ones to these write-only registers, regardless of MASK registers.

Table 191. GPIO port clear register (CLR, addresses 0x400F 6280 (CLR0) to 0x400F 629C (CLR7)) bit description

Bit	Symbol	Description	Reset value	Access
31:0	CLR	Clear output bits (bit 0 = GPIOn[0], bit 1 = GPIOn[1], ..., bit 31 = GPIOn[31]): 0 = No operation. 1 = Clear output bit.	NA	WO

15.5.3.9 GPIO port toggle registers

Each GPIO port has one output toggle register. Output bits can be toggled/inverted/complemented by writing ones to these write-only registers, regardless of MASK registers.

Table 192. GPIO port toggle register (NOT, addresses 0x400F 6300 (NOT0) to 0x400F 632C (NOT7)) bit description

Bit	Symbol	Description	Reset value	Access
31:0	NOTP0	Toggle output bits (bit 0 = GPIOn[0], bit 1 = GPIOn[1], ..., bit 31 = GPIOn[31]): 0 = no operation. 1 = Toggle output bit.	NA	WO

15.6 Functional description

15.6.1 Reading pin state

Software can read the state of all GPIO pins except those selected for analog input or output in the “I/O Configuration” logic. A pin does not have to be selected for GPIO in “I/O Configuration” in order to read its state. There are four ways to read pin state:

- The state of a single pin can be read with 7 high-order zeros from a Byte Pin register.
- The state of a single pin can be read in all bits of a byte, halfword, or word from a Word Pin register.
- The state of multiple pins in a port can be read as a byte, halfword, or word from a PORT register.
- The state of a selected subset of the pins in a port can be read from a Masked Port (MPORT) register. Pins having a 1 in the port’s Mask register will read as 0 from its MPORT register.

15.6.2 GPIO output

Each GPIO pin has an output bit in the GPIO block. These output bits are the targets of write operations “to the pins”. Two conditions must be met in order for a pin’s output bit to be driven onto the pin:

1. The pin must be selected for GPIO operation in the “I/O Configuration” block, and

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2. the pin must be selected for output by a 1 in its port's DIR register.

If either or both of these conditions is (are) not met, "writing to the pin" has no effect.

There are seven ways to change GPIO output bits:

- Writing to a Byte Pin register loads the output bit from the least significant bit.
- Writing to a Word Pin register loads the output bit with the OR of all of the bits written. (This feature follows the definition of "truth" of a multi-bit value in programming languages.)
- Writing to a port's PORT register loads the output bits of all the pins written to.
- Writing to a port's MPORT register loads the output bits of pins identified by zeros in corresponding positions of the port's MASK register.
- Writing ones to a port's SET register sets output bits.
- Writing ones to a port's CLR register clears output bits.
- Writing ones to a port's NOT register toggles/complements/inverts output bits.

The state of a port's output bits can be read from its SET register. Reading any of the registers described in 15.6.1 returns the state of pins, regardless of their direction or alternate functions.

15.6.3 Masked I/O

A port's MASK register defines which of its pins should be accessible in its MPORT register. Zeroes in MASK enable the corresponding pins to be read from and written to MPORT. Ones in MASK force a pin to read as 0 and its output bit to be unaffected by writes to MPORT. When a port's MASK register contains all zeros, its PORT and MPORT registers operate identically for reading and writing.

Users of previous NXP devices with similar GPIO blocks should be aware of an incompatibility: on the LPC11A1x, writing to the SET, CLR, and NOT registers is not affected by the MASK register. On previous devices these registers were masked.

Applications in which interrupts can result in Masked GPIO operation, or in task switching among tasks that do Masked GPIO operation, must treat code that uses the Mask register as a protected/restricted region. This can be done by interrupt disabling or by using a semaphore.

The simpler way to protect a block of code that uses a MASK register is to disable interrupts before setting the MASK register, and re-enable them after the last operation that uses the MPORT or MASK register.

More efficiently, software can dedicate a semaphore to the MASK registers, and set/capture the semaphore controlling exclusive use of the MASK registers before setting the MASK registers, and release the semaphore after the last operation that uses the MPORT or MASK registers.

15.6.4 GPIO Interrupts

Two separate GPIO interrupt facilities are provided. With pin interrupts, up to eight GPIO pins can each have separately-vectored, edge- or level-sensitive interrupts.

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With group interrupts, any subset of the pins in each port can be selected to contribute to a common interrupt. Any of the pin and port interrupts can be enabled to wake the part from Deep-sleep mode or Power-down mode.

15.6.4.1 Pin interrupts

In this interrupt facility, up to 8 pins are identified as interrupt sources by the Pin Interrupt Select registers (PINTSEL0-7). All of the other Pin Interrupt registers contain 8 bits, corresponding to the pins called out by the PINTSEL0-7 registers. The PINTMODE register defines whether each interrupt pin is edge- or level-sensitive. The PINTRISE and PINTFALL registers detect edges on each interrupt pin, and can be written to clear (and set) edge detection. The PINTST register indicates whether each interrupt pin is currently requesting an interrupt, and PINTST can be written to clear interrupts.

The other pin interrupt registers play different roles for edge-sensitive and level-sensitive pins, as described in Table 193.

Table 193. Pin interrupt registers for edge- and level-sensitive pins

Name	Edge-sensitive function	Level-sensitive function
PINTEN_R	Enables rising-edge interrupts.	Enables interrupts.
PINTSEN_R	Write to enable rising-edge interrupts.	Write to enable interrupts.
PINTCEN_R	Write to disable rising-edge interrupts.	Write to disable interrupts.
PINTEN_F	Enables falling-edge interrupts.	Selects active level.
PINTSEN_F	Write to enable falling-edge interrupts.	Write to select high-active.
PINTCEN_F	Write to disable falling-edge interrupts.	Write to select low-active.

15.6.4.2 Group interrupts

In this interrupt facility, an interrupt can be requested for each port, based on any selected subset of pins within each port. The pins that contribute to each port interrupt are selected by 1s in the port’s Enable register, and an interrupt polarity can be selected for each pin in the port’s Polarity register. The level on each pin is exclusive-ORed with its polarity bit and the result is ANDed with its enable bit, and these results are then inclusive-ORed among all the pins in the port, to create the port’s raw interrupt request.

The raw interrupt request from each of the two group interrupts is sent to the NVIC, which can be programmed to treat it as level- or edge-sensitive (see Section 6.8).

15.6.5 Recommended practices

The following lists some recommended uses for using the GPIO port registers:

- For initial setup after Reset or re-initialization, write the PORT registers.
- To change the state of one pin, write a Byte Pin or Word Pin register.
- To change the state of multiple pins at a time, write the SET and/or CLR registers.
- To change the state of multiple pins in a tightly controlled environment like a software state machine, consider using the NOT register. This can require less write operations than SET and CLR.
- To read the state of one pin, read a Byte Pin or Word Pin register.
- To make a decision based on multiple pins, read and mask a PORT register.

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UM10430

Chapter 16: LPC18xx General Purpose DMA (GPDMA) controller

Rev. 00.13 — 20 July 2011 **User manual**

16.1 How to read this chapter

The GPDMA is available on all LPC18xx parts.

See Table 921 for the DMA-to-peripheral connections for parts LPC1850/30/20/10 Rev '-'.

16.2 Basic configuration

The GPDMA is configured as follows:

- See Table 194 for clocking and power control.
- The GPDMA is reset by the DMA_RST (reset # 19).
- The DMAMUX register in the CREG block (see Table 35) selects between up to three peripherals for each GPDMA-to-peripheral line.

Table 194. GPDMA clocking and power control

	Base clock	Branch clock	Maximum frequency
GPDMA	BASE_M3_CLK	CLK_M3_DMA	150 MHz

16.3 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- Two AHB bus masters for transferring data. These interfaces transfer data when a DMA request goes active. Master 1 can access memories and peripherals, master 0 can access memories only.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.

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- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

16.4 General description

The DMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bi-directional port requires one stream for transmit and one for receives. The source and destination areas can each be either a memory region or a peripheral for master 1, but only memory for master 0.

16.5 DMA system connections

The connection of the DMA Controller to supported peripheral devices is shown in Table 195. The LPC18xx supports up to three different muxing options for each channel to connect peripherals to the DMA. The DMAMUX register in the CREG block controls which option is used (see Table 35).

Table 195. Peripheral connections to the DMA controller and matching flow control signals

Peripheral Number	DMA muxing option (see Table 35)	SREQ	BREQ
0	0x0	SPIFI	SPIFI
	0x1	SCT match 2<tbd>	
	0x2	Reserved	Reserved
	0x3	Timer 3 match 1	
1	0x0	n.c.	Timer 0 match 0
	0x1	n.c.	USART0 transmit
	0x2	Reserved	Reserved
	0x3	n.c.	AES input
2	0x0	n.c.	Timer 0 match 1
	0x1	n.c.	USART0 receive
	0x2	Reserved	Reserved
	0x3	n.c.	AES output
3	0x0	n.c.	Timer 1 match 0
	0x1	n.c.	UART1 transmit
	0x2	n.c.	I2S1 channel 0
	0x3	SSP1 transmit	SSP1 transmit

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Table 195. Peripheral connections to the DMA controller and matching flow control signals

Peripheral Number	DMA muxing option (see Table 35)	SREQ	BREQ
4	0x0	n.c.	Timer 1 match 1
	0x1	n.c.	UART 1 receive
	0x2	n.c.	I2S1 channel 1
	0x3	SSP1 receive	SSP1 receive
5	0x0	n.c.	Timer 2 match 0
	0x1	n.c.	USART 2 transmit
	0x2	SSP1 transmit	SSP1 transmit
	0x3	Reserved	Reserved
6	0x0	n.c.	Timer 2 match 1
	0x1	n.c.	USART 2 receive
	0x2	SSP1 receive	SSP1 receive
	0x3	Reserved	Reserved
7	0x0	n.c.	Timer 3 match 0
	0x1	n.c.	USART3 transmit
	0x2	n.c.	SCT DMA request 0
	0x3	Reserved	Reserved
8	0x0	n.c.	Timer 3 match 1
	0x1	n.c.	USART3 receive
	0x2	n.c.	SCT DMA request 1
	0x3	Reserved	Reserved
9	0x0	SSP0 receive	SSP0 receive
	0x1	n.c.	I2S channel 0
	0x2	n.c.	SCT DMA request 1
	0x3	n.c.	n.c.
10	0x0	SSP0 transmit	SSP0 transmit
	0x1	n.c.	I2S channel 1
	0x2	n.c.	SCT DMA request 0
	0x3	n.c.	n.c.
11	0x0	SSP1 receive	SSP1 receive
	0x1	Reserved	Reserved
	0x2	n.c.	USART0 transmit
	0x3	n.c.	n.c.
12	0x0	SSP1 transmit	SSP1 transmit
	0x1	Reserved	Reserved
	0x2	n.c.	USART0 receive
	0x3	n.c.	n.c.

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Table 195. Peripheral connections to the DMA controller and matching flow control signals

Peripheral Number	DMA muxing option (see Table 35)	SREQ	BREQ
13	0x0	n.c.	ADC0
	0x1	n.c.	AES input
	0x2	SSP1 receive	SSP1 receive
	0x3	n.c.	USART3 receive
14	0x0	n.c.	ADC1
	0x1	n.c.	AES output
	0x2	SSP1 transmit	SSP1 transmit
	0x3	n.c.	USART3 transmit
15	0x0	n.c.	DAC
	0x1	<tbd>SCT match 3	<tbd>
	0x2	Reserved	Reserved
	0x3	n.c.	Timer3 match 0

In addition to the peripherals listed in Table 195, the GPIOs, the WWDT, and the timers can be accessed by the GPDMA as a memory-to-memory transaction with no flow control.

16.5.1 DMA request signals

The DMA request signals are used by peripherals to request a data transfer. The DMA request signals indicate whether a single or burst transfer of data is required and whether the transfer is the last in the data packet. The DMA available request signals are:

BREQ[15:0] — Burst request signals. These cause a programmed burst number of data to be transferred.

SREQ[15:0] — Single transfer request signals. These cause a single data to be transferred. The DMA controller transfers a single transfer to or from the peripheral.

LBREQ[15:0] — Last burst request signals.

LSREQ[15:0] — Last single transfer request signals.

Note that most peripherals do not support all request types.

16.5.2 DMA response signals

The DMA response signals indicate whether the transfer initiated by the DMA request signal has completed. The response signals can also be used to indicate whether a complete packet has been transferred. The DMA response signals from the DMA controller are:

CLR[15:0] — DMA clear or acknowledge signals. The CLR signal is used by the DMA controller to acknowledge a DMA request from the peripheral.

TC[15:0] — DMA terminal count signals. The TC signal can be used by the DMA controller to indicate to the peripheral that the DMA transfer is complete.

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16.6 Register description

The DMA Controller supports 8 channels. Each channel has registers specific to the operation of that channel. Other registers controls aspects of how source peripherals relate to the DMA Controller. There are also global DMA control and status registers.

Table 196. Register overview: GPDMA (base address 0x4000 2000)

Name	Access	Address offset	Description	Reset value
General registers				
INTSTAT	RO	0x000	DMA Interrupt Status Register	0x0000 0000
INTTCSTAT	RO	0x004	DMA Interrupt Terminal Count Request Status Register	0x0000 0000
INTTCCLEAR	WO	0x008	DMA Interrupt Terminal Count Request Clear Register	-
INTERRSTAT	RO	0x00C	DMA Interrupt Error Status Register	0x0000 0000
INTERRCLR	WO	0x010	DMA Interrupt Error Clear Register	-
RAWINTTCSTAT	RO	0x014	DMA Raw Interrupt Terminal Count Status Register	0x0000 0000
RAWINTERRSTAT	RO	0x018	DMA Raw Error Interrupt Status Register	0x0000 0000
ENBLDCHNS	RO	0x01C	DMA Enabled Channel Register	0x0000 0000
SOFTBREQ	R/W	0x020	DMA Software Burst Request Register	0x0000 0000
SOFTSREQ	R/W	0x024	DMA Software Single Request Register	0x0000 0000
SOFTLBREQ	R/W	0x028	DMA Software Last Burst Request Register	0x0000 0000
SOFTLSREQ	R/W	0x02C	DMA Software Last Single Request Register	0x0000 0000
CONFIG	R/W	0x030	DMA Configuration Register	0x0000 0000
SYNC	R/W	0x034	DMA Synchronization Register	0x0000 0000
Channel 0 registers				
C0SRCADDR	R/W	0x100	DMA Channel 0 Source Address Register	0x0000 0000
C0DESTADDR	R/W	0x104	DMA Channel 0 Destination Address Register	0x0000 0000
C0LLI	R/W	0x108	DMA Channel 0 Linked List Item Register	0x0000 0000
C0CONTROL	R/W	0x10C	DMA Channel 0 Control Register	0x0000 0000
C0CONFIG	R/W	0x110	DMA Channel 0 Configuration Register	0x0000 0000[1]
Channel 1 registers				
C1SRCADDR	R/W	0x120	DMA Channel 1 Source Address Register	0x0000 0000
C1DESTADDR	R/W	0x124	DMA Channel 1 Destination Address Register	0x0000 0000
C1LLI	R/W	0x128	DMA Channel 1 Linked List Item Register	0x0000 0000
C1CONTROL	R/W	0x12C	DMA Channel 1 Control Register	0x0000 0000
C1CONFIG	R/W	0x130	DMA Channel 1 Configuration Register	0x0000 0000[1]
Channel 2 registers				
C2SRCADDR	R/W	0x140	DMA Channel 2 Source Address Register	0x0000 0000
C2DESTADDR	R/W	0x144	DMA Channel 2 Destination Address Register	0x0000 0000
C2LLI	R/W	0x148	DMA Channel 2 Linked List Item Register	0x0000 0000
C2CONTROL	R/W	0x14C	DMA Channel 2 Control Register	0x0000 0000
C2CONFIG	R/W	0x150	DMA Channel 2 Configuration Register	0x0000 0000[1]

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Table 196. Register overview: GPDMA (base address 0x4000 2000) *…continued*

Name	Access	Address offset	Description	Reset value
Channel 3 registers				
C3SRCADDR	R/W	0x160	DMA Channel 3 Source Address Register	0x0000 0000
C3DESTADDR	R/W	0x164	DMA Channel 3 Destination Address Register	0x0000 0000
C3LLI	R/W	0x168	DMA Channel 3 Linked List Item Register	0x0000 0000
C3CONTROL	R/W	0x16C	DMA Channel 3 Control Register	0x0000 0000
C3CONFIG	R/W	0x170	DMA Channel 3 Configuration Register	0x0000 0000[1]
Channel 4 registers				
C4SRCADDR	R/W	0x180	DMA Channel 4 Source Address Register	0x0000 0000
C4DESTADDR	R/W	0x184	DMA Channel 4 Destination Address Register	0x0000 0000
C4LLI	R/W	0x188	DMA Channel 4 Linked List Item Register	0x0000 0000
C4CONTROL	R/W	0x18C	DMA Channel 4 Control Register	0x0000 0000
C4CONFIG	R/W	0x190	DMA Channel 4 Configuration Register	0x0000 0000[1]
Channel 5 registers				
C5SRCADDR	R/W	0x1A0	DMA Channel 5 Source Address Register	0x0000 0000
C5DESTADDR	R/W	0x1A4	DMA Channel 5 Destination Address Register	0x0000 0000
C5LLI	R/W	0x1A8	DMA Channel 5 Linked List Item Register	0x0000 0000
C5CONTROL	R/W	0x1AC	DMA Channel 5 Control Register	0x0000 0000
C5CONFIG	R/W	0x1B0	DMA Channel 5 Configuration Register	0x0000 0000[1]
Channel 6 registers				
C6SRCADDR	R/W	0x1C0	DMA Channel 6 Source Address Register	0x0000 0000
C6DESTADDR	R/W	0x1C4	DMA Channel 6 Destination Address Register	0x0000 0000
C6LLI	R/W	0x1C8	DMA Channel 6 Linked List Item Register	0x0000 0000
C6CONTROL	R/W	01CC	DMA Channel 6 Control Register	0x0000 0000
C6CONFIG	R/W	0x1D0	DMA Channel 6 Configuration Register	0x0000 0000[1]
Channel 7 registers				
C7SRCADDR	R/W	0x1E0	DMA Channel 7 Source Address Register	0x0000 0000
C7DESTADDR	R/W	0x1E4	DMA Channel 7 Destination Address Register	0x0000 0000
C7LLI	R/W	0x1E8	DMA Channel 7 Linked List Item Register	0x0000 0000
C7CONTROL	R/W	0x1EC	DMA Channel 7 Control Register	0x0000 0000
C7CONFIG	R/W	0x1F0	DMA Channel 7 Configuration Register	0x0000 0000[1]

[1] Bit 17 of this register is a read-only status flag.

16.6.1 DMA Interrupt Status Register

The IntStat Register is read-only and shows the status of the interrupts after masking. A HIGH bit indicates that a specific DMA channel interrupt request is active. The request can be generated from either the error or terminal count interrupt requests.

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Table 197. DMA Interrupt Status register (INTSTAT, address 0x4000 2000) bit description

Bit	Symbol	Description	Reset value	Access
7:0	INTSTAT	Status of DMA channel interrupts after masking. Each bit represents one channel: 0 - the corresponding channel has no active interrupt request. 1 - the corresponding channel does have an active interrupt request.	0x00	RO
31:8	-	Reserved. Read undefined.	-	-

16.6.2 DMA Interrupt Terminal Count Request Status Register

The INTTCSTAT Register is read-only and indicates the status of the terminal count after masking.

Table 198. DMA Interrupt Terminal Count Request Status Register (INTTCSTAT, address 0x4000 2004) bit description

Bit	Symbol	Description	Reset value	Access
7:0	INTTCSTAT	Terminal count interrupt request status for DMA channels. Each bit represents one channel: 0 - the corresponding channel has no active terminal count interrupt request. 1 - the corresponding channel does have an active terminal count interrupt request.	0x00	RO
31:8	-	Reserved. Read undefined.	-	-

16.6.3 DMA Interrupt Terminal Count Request Clear Register

The INTTCCLEAR Register is write-only and clears one or more terminal count interrupt requests. When writing to this register, each data bit that is set HIGH causes the corresponding bit in the status register (IntTCStat) to be cleared. Data bits that are LOW have no effect.

Table 199. DMA Interrupt Terminal Count Request Clear Register (INTTCCLEAR, address 0x4000 2008) bit description

Bit	Symbol	Description	Reset value	Access
7:0	INTTCCLEAR	Allows clearing the Terminal count interrupt request (IntTCStat) for DMA channels. Each bit represents one channel: 0 - writing 0 has no effect. 1 - clears the corresponding channel terminal count interrupt.	0x00	WO
31:8	-	Reserved. Read undefined. Write reserved bits as zero.	-	-

16.6.4 DMA Interrupt Error Status Register

The INTERRSTAT Register is read-only and indicates the status of the error request after masking.

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Table 200. DMA Interrupt Error Status Register (INTERRSTAT, address 0x4000 200C) bit description

Bit	Symbol	Description	Reset value	Access
7:0	INTERRSTAT	Interrupt error status for DMA channels. Each bit represents one channel: 0 - the corresponding channel has no active error interrupt request. 1 - the corresponding channel does have an active error interrupt request.	0x00	RO
31:8	-	Reserved. Read undefined.	-	-

16.6.5 DMA Interrupt Error Clear Register

The INTERRCLR Register is write-only and clears the error interrupt requests. When writing to this register, each data bit that is HIGH causes the corresponding bit in the status register to be cleared. Data bits that are LOW have no effect on the corresponding bit in the register.

Table 201. DMA Interrupt Error Clear Register (INTERRCLR, address 0x4000 2010) bit description

Bit	Symbol	Description	Reset value	Access
7:0	INTERRCLR	Writing a 1 clears the error interrupt request (IntErrStat) for DMA channels. Each bit represents one channel: 0 - writing 0 has no effect. 1 - clears the corresponding channel error interrupt.	0x00	WO
31:8	-	Reserved. Read undefined. Write reserved bits as zero.	-	-

16.6.6 DMA Raw Interrupt Terminal Count Status Register

The RAWINTTCSTAT Register is read-only and indicates which DMA channel is requesting a transfer complete (terminal count interrupt) prior to masking. (Note: the IntTCStat Register contains the same information after masking.) A HIGH bit indicates that the terminal count interrupt request is active prior to masking.

Table 202. DMA Raw Interrupt Terminal Count Status Register (RAWINTTCSTAT, address 0x4000 2014) bit description

Bit	Symbol	Description	Reset value	Access
7:0	RAWINTTCSTAT	Status of the terminal count interrupt for DMA channels prior to masking. Each bit represents one channel: 0 - the corresponding channel has no active terminal count interrupt request. 1 - the corresponding channel does have an active terminal count interrupt request.	0x00	RO
31:8	-	Reserved. Read undefined.	-	-

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16.6.7 DMA Raw Error Interrupt Status Register

The RAWINTERRSTAT Register is read-only and indicates which DMA channel is requesting an error interrupt prior to masking. (Note: the IntErrStat Register contains the same information after masking.) A HIGH bit indicates that the error interrupt request is active prior to masking.

Table 203. DMA Raw Error Interrupt Status Register (RAWINTERRSTAT, address 0x4000 2018) bit description

Bit	Symbol	Description	Reset value	Access
7:0	RAWINTERRSTAT	Status of the error interrupt for DMA channels prior to masking. Each bit represents one channel: 0 - the corresponding channel has no active error interrupt request. 1 - the corresponding channel does have an active error interrupt request.	0x00	RO
31:8	-	Reserved. Read undefined.	-	-

16.6.8 DMA Enabled Channel Register

The ENBLDCHNS Register is read-only and indicates which DMA channels are enabled, as indicated by the Enable bit in the CCONFIG Register. A HIGH bit indicates that a DMA channel is enabled. A bit is cleared on completion of the DMA transfer.

Table 204. DMA Enabled Channel Register (ENBLDCHNS, address 0x4000 201C) bit description

Bit	Symbol	Description	Reset value	Access
7:0	ENABLEDCHANNELS	Enable status for DMA channels. Each bit represents one channel: 0 - DMA channel is disabled. 1 - DMA channel is enabled.	0x00	RO
31:8	-	Reserved. Read undefined.	-	-

16.6.9 DMA Software Burst Request Register

The SOFTBREQ Register is read/write and enables DMA burst requests to be generated by software. A DMA request can be generated for each source by writing a 1 to the corresponding register bit. A register bit is cleared when the transaction has completed. Reading the register indicates which sources are requesting DMA burst transfers. A request can be generated from either a peripheral or the software request register. Each bit is cleared when the related transaction has completed.

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Table 205. DMA Software Burst Request Register (SOFTBREQ, address 0x4000 2020) bit description

Bit	Symbol	Description	Reset value	Access
15:0	SOFTBREQ	Software burst request flags for each of 16 possible sources. Each bit represents one DMA request line or peripheral function (refer to Table 195 for peripheral hardware connections to the DMA controller): 0 - writing 0 has no effect. 1 - writing 1 generates a DMA burst request for the corresponding request line.	0x00	R/W
31:16	-	Reserved. Read undefined. Write reserved bits as zero.	-	-

Note: It is recommended that software and hardware peripheral requests are not used at the same time.

16.6.10 DMA Software Single Request Register

The SOFTSREQ Register is read/write and enables DMA single transfer requests to be generated by software. A DMA request can be generated for each source by writing a 1 to the corresponding register bit. A register bit is cleared when the transaction has completed. Reading the register indicates which sources are requesting single DMA transfers. A request can be generated from either a peripheral or the software request register.

Table 206. DMA Software Single Request Register (SOFTSREQ, address 0x4000 2024) bit description

Bit	Symbol	Description	Reset value	Access
15:0	SOFTSREQ	Software single transfer request flags for each of 16 possible sources. Each bit represents one DMA request line or peripheral function: 0 - writing 0 has no effect. 1 - writing 1 generates a DMA single transfer request for the corresponding request line.	0x00	R/W
31:16	-	Reserved. Read undefined. Write reserved bits as zero.	-	-

16.6.11 DMA Software Last Burst Request Register

The SOFTLBREQ Register is read/write and enables DMA last burst requests to be generated by software. A DMA request can be generated for each source by writing a 1 to the corresponding register bit. A register bit is cleared when the transaction has completed. Reading the register indicates which sources are requesting last burst DMA transfers. A request can be generated from either a peripheral or the software request register.

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Table 207. DMA Software Last Burst Request Register (SOFTLBREQ, address 0x4000 2028) bit description

Bit	Symbol	Description	Reset value	Access
15:0	SOFTLBREQ	Software last burst request flags for each of 16 possible sources. Each bit represents one DMA request line or peripheral function: 0 - writing 0 has no effect. 1 - writing 1 generates a DMA last burst request for the corresponding request line.	0x00	R/W
31:16	-	Reserved. Read undefined. Write reserved bits as zero.	-	-

16.6.12 DMA Software Last Single Request Register

The SOFTLSREQ Register is read/write and enables DMA last single requests to be generated by software. A DMA request can be generated for each source by writing a 1 to the corresponding register bit. A register bit is cleared when the transaction has completed. Reading the register indicates which sources are requesting last single DMA transfers. A request can be generated from either a peripheral or the software request register.

Table 208. DMA Software Last Single Request Register (SOFTLSREQ, address 0x4000 202C) bit description

Bit	Symbol	Description	Reset value	Access
15:0	SOFTLSREQ	Software last single transfer request flags for each of 16 possible sources. Each bit represents one DMA request line or peripheral function: 0 - writing 0 has no effect. 1 - writing 1 generates a DMA last single transfer request for the corresponding request line.	0x00	R/W
31:16	-	Reserved. Read undefined. Write reserved bits as zero.	-	-

16.6.13 DMA Configuration Register

The CONFIG Register is read/write and configures the operation of the DMA Controller. The endianness of the AHB master interface can be altered by writing to the M bit of this register. The AHB master interface is set to little-endian mode on reset.

Table 209. DMA Configuration Register (CONFIG, address 0x4000 2030) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	E		DMA Controller enable:	0x00	R/W
		0	Disabled (default). Disabling the DMA Controller reduces power consumption.		
		1	Enabled		
1	M0		AHB Master 0 endianness configuration:	0x00	R/W
		0	Little-endian mode (default).		
		1	Big-endian mode.		

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Table 209. DMA Configuration Register (CONFIG, address 0x4000 2030) bit description

Bit	Symbol	Value	Description	Reset value	Access
2	M1		AHB Master 1 endianness configuration:	0x00	R/W
		0	Little-endian mode (default).		
		1	Big-endian mode.		
31:3	-		Reserved. Read undefined. Write reserved bits as zero.		

16.6.14 DMA Synchronization Register

The Sync Register is read/write and enables or disables synchronization logic for the DMA request signals. The DMA request signals consist of the BREQ[15:0], SREQ[15:0], LBREQ[15:0], and LSREQ[15:0]. A bit set to 0 enables the synchronization logic for a particular group of DMA requests. A bit set to 1 disables the synchronization logic for a particular group of DMA requests. This register is reset to 0, synchronization logic enabled.

Table 210. DMA Synchronization Register (SYNC, address 0x4000 2034) bit description

Bit	Symbol	Description	Reset value	Access
15:0	DMACSYNC	Controls the synchronization logic for DMA request signals. Each bit represents one set of DMA request lines as described in the preceding text: 0 - synchronization logic for the corresponding DMA request signals are disabled. 1 - synchronization logic for the corresponding request line signals are enabled.	0x00	R/W
31:16	-	Reserved. Read undefined. Write reserved bits as zero.	-	-

16.6.15 DMA Channel registers

The channel registers are used to program the eight DMA channels. These registers consist of:

- Eight CSRCADDR Registers.
- Eight CDESTADDR Registers.
- Eight CLLI Registers.
- Eight CCONTROL Registers.
- Eight CCONFIG Registers.

When performing scatter/gather DMA, the first four of these are automatically updated.

16.6.16 DMA Channel Source Address Registers

The eight read/write CSRCADDR Registers (C0SRCADDR to C7SRCADDR) contain the current source address (byte-aligned) of the data to be transferred. Each register is programmed directly by software before the appropriate channel is enabled. When the DMA channel is enabled this register is updated:

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- As the source address is incremented.
- By following the linked list when a complete packet of data has been transferred.

Reading the register when the channel is active does not provide useful information. This is because by the time software has processed the value read, the address may have progressed. It is intended to be read only when the channel has stopped, in which case it shows the source address of the last item read.

Note: The source and destination addresses must be aligned to the source and destination widths.

Table 211. DMA Channel Source Address Registers (CSRCADDR, 0x4000 2100 (C0SRCADDR) to 0x4000 21E0 (C7SRCADDR)) bit description

Bit	Symbol	Description	Reset value	Access
31:0	SRCADDR	DMA source address. Reading this register will return the current source address.	0x0000 0000	R/W

16.6.17 DMA Channel Destination Address registers

The eight read/write CDESTADDR Registers (C0DESTADDR to C7DESTADDR) contain the current destination address (byte-aligned) of the data to be transferred. Each register is programmed directly by software before the channel is enabled. When the DMA channel is enabled the register is updated as the destination address is incremented and by following the linked list when a complete packet of data has been transferred. Reading the register when the channel is active does not provide useful information. This is because by the time that software has processed the value read, the address may have progressed. It is intended to be read only when a channel has stopped, in which case it shows the destination address of the last item read.

Table 212. DMA Channel Destination Address registers (CDESTADDR, 0x4000 2104 (C0DESTADDR) to 0x4000 21E4 (C7DESTADDR)) bit description

Bit	Symbol	Description	Reset value	Access
31:0	DESTADDR	DMA Destination address. Reading this register will return the current destination address.	0x0000 0000	R/W

16.6.18 DMA Channel Linked List Item registers

The eight read/write CLLI Registers (C0LLI to C7LLI) contain a word-aligned address of the next Linked List Item (LLI). If the LLI is 0, then the current LLI is the last in the chain, and the DMA channel is disabled when all DMA transfers associated with it are completed. Programming this register when the DMA channel is enabled may have unpredictable side effects.

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Table 213. DMA Channel Linked List Item registers (CLLI, 0x4000 2108 (C0LLI) to 0x4000 21E8 (C7LLI)) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	LM		AHB master select for loading the next LLI:	0	R/W
		0	AHB Master 0.		
		1	AHB Master 1.		
1	R		Reserved, and must be written as 0, masked on read.	0	R/W
31:2	LLI		Linked list item. Bits [31:2] of the address for the next LLI. Address bits [1:0] are 0.	0x0000 0000	R/W

16.6.19 DMA channel control registers

The eight read/write CCONTROL Registers (C0CONTROL to C7CONTROL) contain DMA channel control information such as the transfer size, burst size, and transfer width. Each register is programmed directly by software before the DMA channel is enabled. When the channel is enabled the register is updated by following the linked list when a complete packet of data has been transferred. Reading the register while the channel is active does not give useful information. This is because by the time software has processed the value read, the channel may have advanced. It is intended to be read only when a channel has stopped.

Table 214. DMA Channel Control registers (CCONTROL, 0x4000 210C (C0CONTROL) to 0x4000 21EC (C7CONTROL)) bit description

Bit	Symbol	Value	Description	Reset value	Access
11:0	TRANSFERSIZE		Transfer size in number of transfers. A write to this field sets the size of the transfer when the DMA Controller is the flow controller. The transfer size value must be set before the channel is enabled. Transfer size is updated as data transfers are completed. A read from this field indicates the number of transfers completed on the destination bus. Reading the register when the channel is active does not give useful information because by the time that the software has processed the value read, the channel might have progressed. It is intended to be used only when a channel is enabled and then disabled. The transfer size value is not used if the DMA Controller is not the flow controller.	0x0	R/W

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Table 214. DMA Channel Control registers (CCONTROL, 0x4000 210C (C0CONTROL) to 0x4000 21EC (C7CONTROL)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
14:12	SBSIZE		Source burst size. Indicates the number of transfers that make up a source burst. This value must be set to the burst size of the source peripheral, or if the source is memory, to the memory boundary size (see Figure 5). The burst size is the amount of data that is transferred when the BREQ signal goes active in the source peripheral.	0x0	R/W
		0x0	Source burst size = 1		
		0x1	Source burst size = 4		
		0x2	Source burst size = 8		
		0x3	Source burst size = 16		
		0x4	Source burst size = 32		
		0x4	Source burst size = 64		
		0x6	Source burst size = 128		
		0x7	Source burst size = 256		
17:15	DBSIZE		Destination burst size. Indicates the number of transfers that make up a destination burst transfer request. This value must be set to the burst size of the destination peripheral or, if the destination is memory, to the memory boundary size. The burst size is the amount of data that is transferred when the BREQ signal goes active in the destination peripheral.	0x0	R/W
		0x0	Destination burst size = 1		
		0x1	Destination burst size = 4		
		0x2	Destination burst size = 8		
		0x3	Destination burst size = 16		
		0x4	Destination burst size = 32		
		0x4	Destination burst size = 64		
		0x6	Destination burst size = 128		
		0x7	Destination burst size = 256		
20:18	SWIDTH		Source transfer width. Transfers wider than the AHB master bus width are illegal. The source and destination widths can be different from each other. The hardware automatically packs and unpacks the data as required. 0x3 to 0x7 - Reserved.	0x0	R/W
		0x0	Byte (8-bit)		
		0x1	Halfword (16-bit)		
		0x2	Word (32-bit)		
23:21	DWIDTH		Destination transfer width. Transfers wider than the AHB master bus width are not supported. The source and destination widths can be different from each other. The hardware automatically packs and unpacks the data as required. 0x3 to 0x7 - Reserved.	0x0	R/W
		0x0	Byte (8-bit)		
		0x1	Halfword (16-bit)		
		0x2	Word (32-bit)		

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Table 214. DMA Channel Control registers (CCONTROL, 0x4000 210C (C0CONTROL) to 0x4000 21EC (C7CONTROL)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
24	S		Source AHB master select:	0	R/W
		0	AHB Master 0 selected for source transfer.		
		1	AHB Master 1 selected for source transfer.		
25	D		Destination AHB master select: **Remark:** Only Master1 can access a peripheral. Master0 can only access memory.	0	R/W
		0	AHB Master 0 selected for destination transfer.		
		1	AHB Master 1 selected for destination transfer.		
26	SI		Source increment:	0	R/W
		0	The source address is not incremented after each transfer.		
		1	The source address is incremented after each transfer.		
27	DI		Destination increment:	0	R/W
		0	The destination address is not incremented after each transfer.		
		1	The destination address is incremented after each transfer.		
28	PROT1		Indicates that the access is in user mode or privileged mode:	0	R/W
		0	Access is in user mode		
		1	Access is in privileged mode.		
29	PROT2		Indicates that the access is bufferable or not bufferable:	0	R/W
		0	Access is not bufferable.		
		1	Access is bufferable.		
30	PROT3		Indicates that the access is cacheable or not cacheable:	0	R/W
		0	Access is not cacheable.		
		1	Access is cacheable.		
31	I		Terminal count interrupt enable bit.	0	R/W
		0	The terminal count interrupt is disabled.		
		1	The terminal count interrupt is enabled.		

16.6.19.1 Protection and access information

AHB access information is provided to the source and destination peripherals when a transfer occurs. The transfer information is provided by programming the DMA channel (the Prot bits of the CCONTROL Register, and the Lock bit of the CCONFIG Register). These bits are programmed by software. Peripherals can use this information if necessary.

16.6.20 Channel Configuration registers

The eight CCONFIG Registers (C0CONFIG to C7CONFIG) are read/write with the exception of bit[17] which is read-only. Used these to configure the DMA channel. The registers are not updated when a new LLI is requested.

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Table 215. DMA Channel Configuration registers (CCONFIG, 0x4000 2110 (C0CONFIG) to 0x4000 21F0 (C7CONFIG)) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	E		Channel enable. Reading this bit indicates whether a channel is currently enabled or disabled: The Channel Enable bit status can also be found by reading the ENBLDCHNS Register. A channel can be disabled by clearing the Enable bit. This causes the current AHB transfer (if one is in progress) to complete and the channel is then disabled. Any data in the FIFO of the relevant channel is lost. Restarting the channel by setting the Channel Enable bit has unpredictable effects, the channel must be fully re-initialized. The channel is also disabled, and Channel Enable bit cleared, when the last LLI is reached, the DMA transfer is completed, or if a channel error is encountered. If a channel must be disabled without losing data in the FIFO, the Halt bit must be set so that further DMA requests are ignored. The Active bit must then be polled until it reaches 0, indicating that there is no data left in the FIFO. Finally, the Channel Enable bit can be cleared.	0	R/W
		0	Channel disabled.		
		1	Channel enabled.		
5:1	SRCPERIPHERAL		Source peripheral. This value selects the DMA source request peripheral. This field is ignored if the source of the transfer is from memory. See Table 195 for details.		R/W
		0x0	Source = SPIFI		
		0x1	Source = Timer 0 match 0/UART0 transmit		
		0x2	Source = Timer 0 match 1/UART0 receive		
		0x3	Source = Timer 1 match 0/UART1 transmit		
		0x4	Source = Timer 1 match 1/UART 1 receive		
		0x5	Source = Timer 2 match 0/UART 2 transmit		
		0x6	Source = Timer 2 match 1/UART 2 receive		
		0x7	Source = Timer 3 match 0/UART3 transmit/SCT DMA request 0		
		0x8	Source = Timer 3 match 1/UART3 receive/SCT DMA request 1		
		0x9	Source = SSP0 receive/I2S channel 0		
		0xA	Source = SSP0 transmit/I2S channel 1		
		0xB	Source = SSP1 receive		
		0xC	Source = SSP1 transmit		
		0xD	Source = ADC0		
		0xE	Source = ADC1		
		0xF	Source = DAC		

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Table 215. DMA Channel Configuration registers (CCONFIG, 0x4000 2110 (C0CONFIG) to 0x4000 21F0 (C7CONFIG)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
10:6	DESTPERIPHERAL		Destination peripheral. This value selects the DMA destination request peripheral. This field is ignored if the destination of the transfer is to memory. See Table 195 for details.		R/W
		0x0	Destination = SPIFI		
		0x1	Destination = Timer 0 match 0/UART0 transmit		
		0x2	Destination = Timer 0 match 1/UART0 receive		
		0x3	Destination = Timer 1 match 0/UART1 transmit		
		0x4	Destination = Timer 1 match 1/UART 1 receive		
		0x5	Destination = Timer 2 match 0/UART 2 transmit		
		0x6	Destination = Timer 2 match 1/UART 2 receive		
		0x7	Destination = Timer 3 match 0/UART3 transmit/SCT DMA request 0		
		0x8	Destination = Timer 3 match 1/UART3 receive/SCT DMA request 1		
		0x9	Destination = SSP0 receive/I2S channel 0		
		0xA	Destination = SSP0 transmit/I2S channel 1		
		0xB	Destination = SSP1 receive		
		0xC	Destination = SSP1 transmit		
		0xD	Destination = ADC0		
		0xE	Destination = ADC1		
		0xF	Destination = DAC		
13:11	FLOWCNTRL		Flow control and transfer type. This value indicates the flow controller and transfer type. The flow controller can be the DMA Controller, the source peripheral, or the destination peripheral. The transfer type can be memory-to-memory, memory-to-peripheral, peripheral-to-memory, or peripheral-to-peripheral. Refer to Table 216 for the encoding of this field.		R/W
		0x0	Memory to memory (DMA control)		
		0x1	Memory to peripheral (DMA control)		
		0x2	Peripheral to memory (DMA control)		
		0x3	Source peripheral to destination peripheral (DMA control)		
		0x4	Source peripheral to destination peripheral (destination control)		
		0x5	Memory to peripheral (peripheral control)		
		0x6	Peripheral to memory (peripheral control)		
		0x7	Source peripheral to destination peripheral (source control)		
14	IE		Interrupt error mask. When cleared, this bit masks out the error interrupt of the relevant channel.		R/W
15	ITC		Terminal count interrupt mask. When cleared, this bit masks out the terminal count interrupt of the relevant channel.		R/W
16	L		Lock. When set, this bit enables locked transfers.		R/W

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Table 215. DMA Channel Configuration registers (CCONFIG, 0x4000 2110 (C0CONFIG) to 0x4000 21F0 (C7CONFIG)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
17	A		Active: 0 = there is no data in the FIFO of the channel. 1 = the channel FIFO has data. This value can be used with the Halt and Channel Enable bits to cleanly disable a DMA channel. This is a read-only bit.		RO
18	H		Halt: 0 = enable DMA requests. 1 = ignore further source DMA requests. The contents of the channel FIFO are drained. This value can be used with the Active and Channel Enable bits to cleanly disable a DMA channel.		R/W
		0	Enable DMA requests.		
		1	Ignore further source DMA requests.		
31:19	-		Reserved, do not modify, masked on read.		-

16.6.20.1 Lock control

The lock control may set the lock bit by writing a 1 to bit 16 of the CCONFIG Register. When a burst occurs, the AHB arbiter will not de-grant the master during the burst until the lock is deasserted. The DMA Controller can be locked for a a single burst such as a long source fetch burst or a long destination drain burst. The DMA Controller does not usually assert the lock continuously for a source fetch burst followed by a destination drain burst.

There are situations when the DMA Controller asserts the lock for source transfers followed by destination transfers. This is possible when internal conditions in the DMA Controller permit it to perform a source fetch followed by a destination drain back-to-back.

16.6.20.2 Flow control and transfer type

Table 216 lists the bit values of the three flow control and transfer type bits identified in Table Table 215.

Table 216. Flow control and transfer type bits

Bit value	Transfer type	Controller
000	Memory to memory	DMA
001	Memory to peripheral	DMA
010	Peripheral to memory	DMA
011	Source peripheral to destination peripheral	DMA
100	Source peripheral to destination peripheral	Destination peripheral
101	Memory to peripheral	Peripheral
110	Peripheral to memory	Peripheral
111	Source peripheral to destination peripheral	Source peripheral

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16.7 Functional description

16.7.1 DMA controller functional description

The DMA Controller enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receive. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the AHB master. Figure 26 shows a block diagram of the DMA Controller.

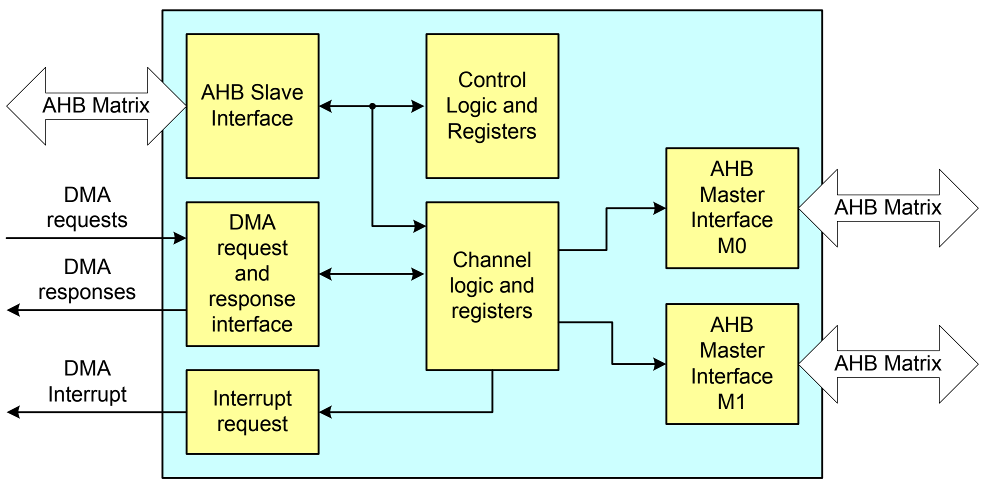


Fig 26. DMA controller block diagram

The functions of the DMA Controller are described in the following sections.

16.7.1.1 AHB slave interface

All transactions to DMA Controller registers on the AHB slave interface are 32 bits wide. Eight bit and 16-bit accesses are not supported and will result in an exception.

16.7.1.2 Control logic and register bank

The register block stores data written or to be read across the AHB interface.

16.7.1.3 DMA request and response interface

See DMA Interface description for information on the DMA request and response interface.

16.7.1.4 Channel logic and channel register bank

The channel logic and channel register bank contains registers and logic required for each DMA channel.

16.7.1.5 Interrupt request

The interrupt request generates the interrupt to the ARM processor.

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16.7.1.6 AHB master interface

The DMA Controller contains two AHB master interfaces. Each AHB master is capable of dealing with all types of AHB transactions, including:

- Split, retry, and error responses from slaves. If a peripheral performs a split or retry, the DMA Controller stalls and waits until the transaction can complete.
- Locked transfers for source and destination of each stream.
- Setting of protection bits for transfers on each stream.

16.7.1.6.1 Bus and transfer widths

The physical width of the AHB bus is 32 bits. Source and destination transfers can be of differing widths and can be the same width or narrower than the physical bus width. The DMA Controller packs or unpacks data as appropriate.

16.7.1.6.2 Endian behavior

The DMA Controller can cope with both little-endian and big-endian addressing. Software can set the endianness of each AHB master individually.

Internally the DMA Controller treats all data as a stream of bytes instead of 16-bit or 32-bit quantities. This means that when performing mixed-endian activity, where the endianness of the source and destination are different, byte swapping of the data within the 32-bit data bus is observed.

Note: If byte swapping is not required, then use of different endianness between the source and destination addresses must be avoided. Table 217 shows endian behavior for different source and destination combinations.

Table 217. Endian behavior

Source endian	Destination endian	Source width	Destination width	Source transfer no/byte lane	Source data	Destination transfer no/byte lane	Destination data
Little	Little	8	8	1/[7:0]	21	1/[7:0]	21212121
				2/[15:8]	43	2/[15:8]	43434343
				3/[23:16]	65	3/[23:16]	65656565
				4/[31:24]	87	4/[31:24]	87878787
Little	Little	8	16	1/[7:0]	21	1/[15:0]	43214321
				2/[15:8]	43	2/[31:16]	87658765
				3/[23:16]	65		
				4/[31:24]	87		
Little	Little	8	32	1/[7:0]	21	1/[31:0]	87654321
				2/[15:8]	43		
				3/[23:16]	65		
				4/[31:24]	87		
Little	Little	16	8	1/[7:0]	21	1/[7:0]	21212121
				1/[15:8]	43	2/[15:8]	43434343
				2/[23:16]	65	3/[23:16]	65656565
				2/[31:24]	87	4/[31:24]	87878787

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Table 217. Endian behavior *…continued*

Source endian	Destination endian	Source width	Destination width	Source transfer no/byte lane	Source data	Destination transfer no/byte lane	Destination data
Little	Little	16	16	1/[7:0]	21	1/[15:0]	43214321
				1/[15:8]	43	2/[31:16]	87658765
				2/[23:16]	65		
				2/[31:24]	87		
Little	Little	16	32	1/[7:0]	21	1/[31:0]	87654321
				1/[15:8]	43		
				2/[23:16]	65		
				2/[31:24]	87		
Little	Little	32	8	1/[7:0]	21	1/[7:0]	21212121
				1/[15:8]	43	2/[15:8]	43434343
				1/[23:16]	65	3/[23:16]	65656565
				1/[31:24]	87	4/[31:24]	87878787
Little	Little	32	16	1/[7:0]	21	1/[15:0]	43214321
				1/[15:8]	43	2/[31:16]	87658765
				1/[23:16]	65		
				1/[31:24]	87		
Little	Little	32	32	1/[7:0]	21	1/[31:0]	87654321
				1/[15:8]	43		
				1/[23:16]	65		
				1/[31:24]	87		
Big	Big	8	8	1/[31:24]	12	1/[31:24]	12121212
				2/[23:16]	34	2/[23:16]	34343434
				3/[15:8]	56	3/[15:8]	56565656
				4/[7:0]	78	4/[7:0]	78787878
Big	Big	8	16	1/[31:24]	12	1/[15:0]	12341234
				2/[23:16]	34	2/[31:16]	56785678
				3/[15:8]	56		
				4/[7:0]	78		
Big	Big	8	32	1/[31:24]	12	1/[31:0]	12345678
				2/[23:16]	34		
				3/[15:8]	56		
				4/[7:0]	78		
Big	Big	16	8	1/[31:24]	12	1/[31:24]	12121212
				1/[23:16]	34	2/[23:16]	34343434
				2/[15:8]	56	3/[15:8]	56565656
				2/[7:0]	78	4/[7:0]	78787878
Big	Big	16	16	1/[31:24]	12	1/[15:0]	12341234
				1/[23:16]	34	2/[31:16]	56785678
				2/[15:8]	56		
				2/[7:0]	78		

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Table 217. Endian behavior *…continued*

Source endian	Destination endian	Source width	Destination width	Source transfer no/byte lane	Source data	Destination transfer no/byte lane	Destination data
Big	Big	16	32	1/[31:24]	12	1/[31:0]	12345678
				1/[23:16]	34		
				2/[15:8]	56		
				2/[7:0]	78		
Big	Big	32	8	1/[31:24]	12	1/[31:24]	12121212
				1/[23:16]	34	2/[23:16]	34343434
				1/[15:8]	56	3/[15:8]	56565656
				1/[7:0]	78	4/[7:0]	78787878
Big	Big	32	16	1/[31:24]	12	1/[15:0]	12341234
				1/[23:16]	34	2/[31:16]	56785678
				1/[15:8]	56		
				1/[7:0]	78		
Big	Big	32	32	1/[31:24]	12	1/[31:0]	12345678
				1/[23:16]	34		
				1/[15:8]	56		
				1/[7:0]	78		

16.7.1.6.3 Error conditions

An error during a DMA transfer is flagged directly by the peripheral by asserting an Error response on the AHB bus during the transfer. The DMA Controller automatically disables the DMA stream after the current transfer has completed, and can optionally generate an error interrupt to the CPU. This error interrupt can be masked.

16.7.1.7 Channel hardware

Each stream is supported by a dedicated hardware channel, including source and destination controllers, as well as a FIFO. This enables better latency than a DMA controller with only a single hardware channel shared between several DMA streams and simplifies the control logic.

16.7.1.8 DMA request priority

DMA channel priority is fixed. DMA channel 0 has the highest priority and DMA channel 7 has the lowest priority.

If the DMA Controller is transferring data for the lower priority channel and then the higher priority channel goes active, it completes the number of transfers delegated to the master interface by the lower priority channel before switching over to transfer data for the higher priority channel. In the worst case this is as large as a one quadword.

It is recommended that memory-to-memory transactions use the lowest priority channel. Otherwise other AHB bus masters are prevented from accessing the bus during DMA Controller memory-to-memory transfer.

16.7.1.9 Interrupt generation

A combined interrupt output is generated as an OR function of the individual interrupt requests of the DMA Controller and is connected to the interrupt controller.

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16.8 Using the DMA controller

16.8.1 Programming the DMA controller

All accesses to the DMA Controller internal register must be word (32-bit) reads and writes.

16.8.1.1 Enabling the DMA controller

To enable the DMA controller set the Enable bit in the CONFIG register.

16.8.1.2 Disabling the DMA controller

To disable the DMA controller:

- Read the ENBLDCHNS register and ensure that all the DMA channels have been disabled. If any channels are active, see Disabling a DMA channel.
- Disable the DMA controller by writing 0 to the DMA Enable bit in the CONFIG register.

16.8.1.3 Enabling a DMA channel

To enable the DMA channel set the channel enable bit in the relevant DMA channel configuration register. Note that the channel must be fully initialized before it is enabled.

16.8.1.4 Disabling a DMA channel

A DMA channel can be disabled in three ways:

- By writing directly to the channel enable bit. Any outstanding data in the FIFO's is lost if this method is used.
- By using the active and halt bits in conjunction with the channel enable bit.
- By waiting until the transfer completes. This automatically clears the channel.

Disabling a DMA channel and losing data in the FIFO

Clear the relevant channel enable bit in the relevant channel configuration register. The current AHB transfer (if one is in progress) completes and the channel is disabled. Any data in the FIFO is lost.

Disabling the DMA channel without losing data in the FIFO

- Set the halt bit in the relevant channel configuration register. This causes any future DMA request to be ignored.
- Poll the active bit in the relevant channel configuration register until it reaches 0. This bit indicates whether there is any data in the channel that has to be transferred.
- Clear the channel enable bit in the relevant channel configuration register

16.8.1.5 Setting up a new DMA transfer

To set up a new DMA transfer:

If the channel is not set aside for the DMA transaction:

1. Read the ENBLDCHNS controller register and find out which channels are inactive.
2. Choose an inactive channel that has the required priority.

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3. Program the DMA controller

16.8.1.6 Halting a DMA channel

Set the halt bit in the relevant DMA channel configuration register. The current source request is serviced. Any further source DMA request is ignored until the halt bit is cleared.

16.8.1.7 Programming a DMA channel

1. Choose a free DMA channel with the priority needed. DMA channel 0 has the highest priority and DMA channel 7 the lowest priority.
2. Clear any pending interrupts on the channel to be used by writing to the IntTCClear and INTERRCLEAR register. The previous channel operation might have left interrupt active.
3. Write the source address into the CSRCADDR register.
4. Write the destination address into the CDESTADDR register.
5. Write the address of the next LLI into the CLLI register. If the transfer comprises of a single packet of data then 0 must be written into this register.
6. Write the control information into the CCONTROL register.
7. Write the channel configuration information into the CCONFIG register. If the enable bit is set then the DMA channel is automatically enabled.

16.8.2 Flow control

The peripheral that controls the length of the packet is known as the flow controller. The flow controller is usually the DMA Controller where the packet length is programmed by software before the DMA channel is enabled. If the packet length is unknown when the DMA channel is enabled, either the source or destination peripherals can be used as the flow controller.

For simple or low-performance peripherals that know the packet length (that is, when the peripheral is the flow controller), a simple way to indicate that a transaction has completed is for the peripheral to generate an interrupt and enable the processor to reprogram the DMA channel.

The transfer size value (in the CCONTROL register) is ignored if a peripheral is configured as the flow controller.

When the DMA transfer is completed:

1. The DMA Controller issues an acknowledge to the peripheral in order to indicate that the transfer has finished.
2. A TC interrupt is generated, if enabled.
3. The DMA Controller moves on to the next LLI.

The following sections describe the DMA Controller data flow sequences for the four allowed transfer types:

- Memory-to-peripheral (master 1 only).
- Peripheral-to-memory (master 1 only).
- Memory-to-memory.

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- Peripheral-to-peripheral (master 1 only).

Each transfer type can have either the peripheral or the DMA Controller as the flow controller so there are eight possible control scenarios.

Table 218 indicates the request signals used for each type of transfer.

Table 218. DMA request signal usage

Transfer direction	Request generator	Flow controller
Memory-to-peripheral	Peripheral	DMA Controller
Memory-to-peripheral	Peripheral	Peripheral
Peripheral-to-memory	Peripheral	DMA Controller
Peripheral-to-memory	Peripheral	Peripheral
Memory-to-memory	DMA Controller	DMA Controller
Source peripheral to destination peripheral	Source peripheral and destination peripheral	Source peripheral
Source peripheral to destination peripheral	Source peripheral and destination peripheral	Destination peripheral
Source peripheral to destination peripheral	Source peripheral and destination peripheral	DMA Controller

16.8.2.1 Peripheral-to-memory or memory-to-peripheral DMA flow

For a peripheral-to-memory or memory-to-peripheral DMA flow, the following sequence occurs:

1. Program and enable the DMA channel.
2. Wait for a DMA request.
3. The DMA Controller starts transferring data when:
   - The DMA request goes active.
   - The DMA stream has the highest pending priority.
   - The DMA Controller is the bus master of the AHB bus.
4. If an error occurs while transferring the data, an error interrupt is generated and disables the DMA stream, and the flow sequence ends.
5. Decrement the transfer count if the DMA Controller is performing the flow control.
6. If the transfer has completed (indicated by the transfer count reaching 0, if the DMA Controller is performing flow control, or by the peripheral sending a DMA request, if the peripheral is performing flow control):
   - The DMA Controller responds with a DMA acknowledge.
   - The terminal count interrupt is generated (this interrupt can be masked).
   - If the CLLI Register is not 0, then reload the CSRCADDR, CDESTADDR, CLLI, and CCONTROL registers and go to back to step 2. However, if CLLI is 0, the DMA stream is disabled and the flow sequence ends.

16.8.2.2 Peripheral-to-peripheral DMA flow

For a peripheral-to-peripheral DMA flow, the following sequence occurs:

1. Program and enable the DMA channel.
2. Wait for a source DMA request.
3. The DMA Controller starts transferring data when:

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   – The DMA request goes active.
   – The DMA stream has the highest pending priority.
   – The DMA Controller is the bus master of the AHB bus.
4. If an error occurs while transferring the data an error interrupt is generated, the DMA stream is disabled, and the flow sequence ends.
5. Decrement the transfer count if the DMA Controller is performing the flow control.
6. If the transfer has completed (indicated by the transfer count reaching 0 if the DMA Controller is performing flow control, or by the peripheral sending a DMA request if the peripheral is performing flow control):
   – The DMA Controller responds with a DMA acknowledge to the source peripheral.
   – Further source DMA requests are ignored.
7. When the destination DMA request goes active and there is data in the DMA Controller FIFO, transfer data into the destination peripheral.
8. If an error occurs while transferring the data, an error interrupt is generated, the DMA stream is disabled, and the flow sequence ends.
9. If the transfer has completed it is indicated by the transfer count reaching 0 if the DMA Controller is performing flow control, or by the sending a DMA request if the peripheral is performing flow control. The following happens:
   – The DMA Controller responds with a DMA acknowledge to the destination peripheral.
   – The terminal count interrupt is generated (this interrupt can be masked).
   – If the CLLI Register is not 0, then reload the CSRCADDR, CDESTADDR, CLLI, and CCONTROL Registers and go to back to step 2. However, if CLLI is 0, the DMA stream is disabled and the flow sequence ends.

16.8.2.3 Memory-to-memory DMA flow

For a memory-to-memory DMA flow the following sequence occurs:

1. Program and enable the DMA channel.
2. Transfer data whenever the DMA channel has the highest pending priority and the DMA Controller gains mastership of the AHB bus.
3. If an error occurs while transferring the data, generate an error interrupt and disable the DMA stream.
4. Decrement the transfer count.
5. If the count has reached zero:
   – Generate a terminal count interrupt (the interrupt can be masked).
   – If the CLLI Register is not 0, then reload the CSRCADDR, CDESTADDR, CLLI, and CCONTROL Registers and go to back to step 2. However, if CLLI is 0, the DMA stream is disabled and the flow sequence ends.

Note: Memory-to-memory transfers should be programmed with a low channel priority, otherwise other DMA channels cannot access the bus until the memory-to-memory transfer has finished, or other AHB masters cannot perform any transaction.

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16.8.3 Interrupt requests

Interrupt requests can be generated when an AHB error is encountered or at the end of a transfer (terminal count), after all the data corresponding to the current LLI has been transferred to the destination. The interrupts can be masked by programming bits in the relevant CCONTROL and CCONFIG Channel Registers. Interrupt status registers are provided which group the interrupt requests from all the DMA channels prior to interrupt masking (RAWINTTCSTAT and RAWINTERRSTAT), and after interrupt masking (INTTCSTAT and INTERRSTAT). The INTSTAT Register combines both the INTTCSTAT and INTERRSTAT requests into a single register to enable the source of an interrupt to be quickly found. Writing to the INTTCCLEAR or the INTERRCLR Registers with a bit set HIGH enables selective clearing of interrupts.

16.8.3.1 Hardware interrupt sequence flow

When a DMA interrupt request occurs, the Interrupt Service Routine needs to:

1. Read the INTTCSTAT Register to determine whether the interrupt was generated due to the end of the transfer (terminal count). A HIGH bit indicates that the transfer completed. If more than one request is active, it is recommended that the highest priority channels be checked first.
2. Read the INTERRSTAT Register to determine whether the interrupt was generated due to an error occurring. A HIGH bit indicates that an error occurred.
3. Service the interrupt request.
4. For a terminal count interrupt, write a 1 to the relevant bit of the INTTCCLR Register. For an error interrupt write a 1 to the relevant bit of the INTERRCLR Register to clear the interrupt request.

16.8.4 Address generation

Address generation can be either incrementing or non-incrementing (address wrapping is not supported).

Some devices, especially memories, disallow burst accesses across certain address boundaries. The DMA controller assumes that this is the case with any source or destination area, which is configured for incrementing addressing. This boundary is assumed to be aligned with the specified burst size. For example, if the channel is set for 16-transfer burst to a 32-bit wide device then the boundary is 64-bytes aligned (that is address bits [5:0] equal 0). If a DMA burst is to cross one of these boundaries, then, instead of a burst, that transfer is split into separate AHB transactions.

Note: When transferring data to or from the SDRAM, the SDRAM access must always be programmed to 32 bit accesses. The SDRAM memory controller does not support AHB-INCR4 or INCR8 bursts using halfword or byte transfer-size. Start address in SDRAM should always be aligned to a burst boundary address.

16.8.4.1 Word-aligned transfers across a boundary

The channel is configured for 16-transfer bursts, each transfer 32-bits wide, to a destination for which address incrementing is enabled. The start address for the current burst is 0x0C000024, the next boundary (calculated from the burst size and transfer width) is 0x0C000040.

The transfer will be split into two AHB transactions:

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- a 7-transfer burst starting at address 0x0C000024
- a 9-transfer burst starting at address 0x0C000040.

16.8.5 Scatter/gather

Scatter/gather is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas in memory. Where scatter/gather is not required, the CLLI Register must be set to 0.

The source and destination data areas are defined by a series of linked lists. Each Linked List Item (LLI) controls the transfer of one block of data, and then optionally loads another LLI to continue the DMA operation, or stops the DMA stream. The first LLI is programmed into the DMA Controller.

The data to be transferred described by a LLI (referred to as the packet of data) usually requires one or more DMA bursts (to each of the source and destination).

16.8.5.1 Linked list items

A Linked List Item (LLI) consists of four words. These words are organized in the following order:

1. CSRCADDR
2. CDESTADDR
3. CLLI
4. CCONTROL

Note: The CCONFIG DMA channel Configuration Register is not part of the linked list item.

16.8.5.1.1 Programming the DMA controller for scatter/gather DMA

To program the DMA Controller for scatter/gather DMA:

1. Write the LLIs for the complete DMA transfer to memory. Each linked list item contains four words:
   - Source address.
   - Destination address.
   - Pointer to next LLI.
   - Control word.

   The last LLI has its linked list word pointer set to 0.
2. Choose a free DMA channel with the priority required. DMA channel 0 has the highest priority and DMA channel 7 the lowest priority.
3. Write the first linked list item, previously written to memory, to the relevant channel in the DMA Controller.
4. Write the channel configuration information to the channel Configuration Register and set the Channel Enable bit. The DMA Controller then transfers the first and then subsequent packets of data as each linked list item is loaded.

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5. An interrupt can be generated at the end of each LLI depending on the Terminal Count bit in the CCONTROL Register. If this bit is set an interrupt is generated at the end of the relevant LLI. The interrupt request must then be serviced and the relevant bit in the INTTCCLEAR Register must be set to clear the interrupt.

16.8.5.1.2 Example of scatter/gather DMA

See Figure 27 for an example of an LLI. A section of memory is to be transferred to a peripheral. The addresses of each LLI entry are given, in hexadecimal, at the left-hand side of the figure. The right side of the figure shows the memory containing the data to be transferred.

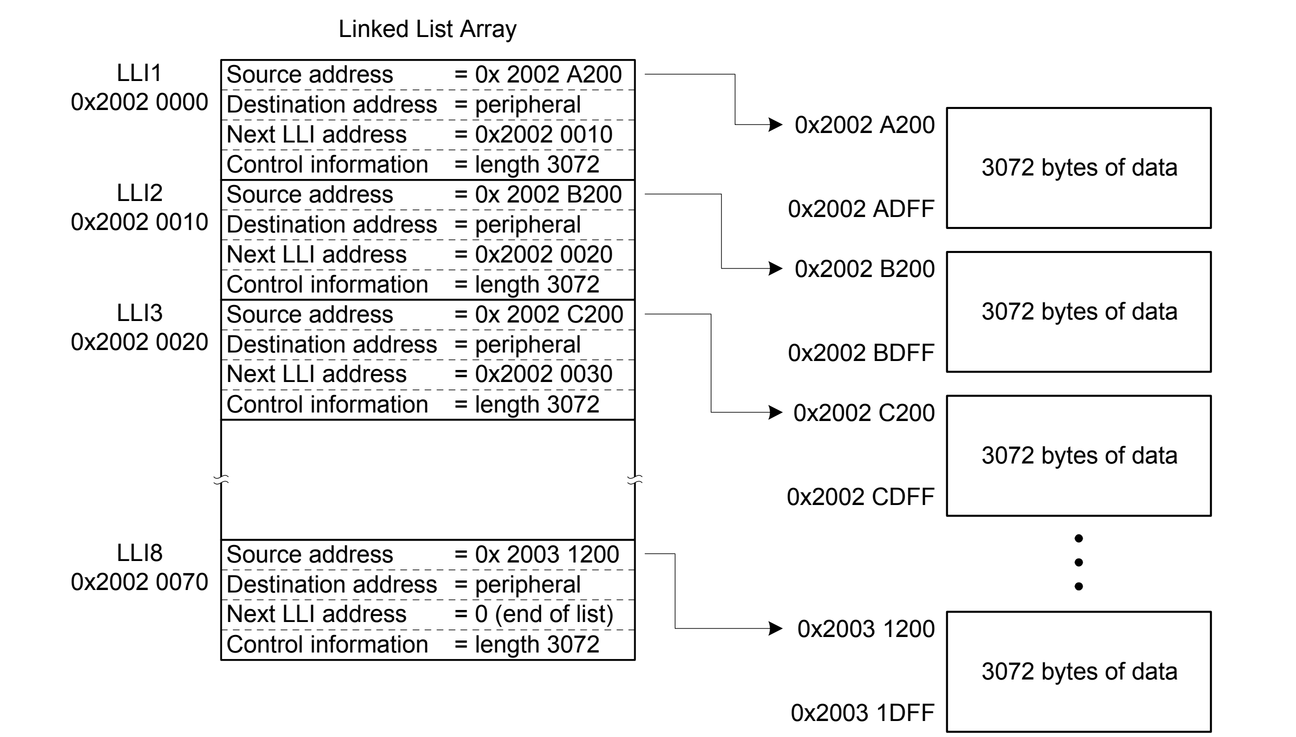


Fig 27. LLI example

The first LLI, stored at 0x2002 0000, defines the first block of data to be transferred, which is the data stored from address 0x2002 A200 to 0x2002 ADFF:

- Source start address 0x2002 A200.
- Destination address set to the destination peripheral address.
- Transfer width, word (32-bit).
- Transfer size, 3072 bytes (0xC00).
- Source and destination burst sizes, 16 transfers.
- Next LLI address, 0x2002 0010.

The second LLI, stored at 0x2002 0010, describes the next block of data to be transferred:

- Source start address 0x2002 B200.
- Destination address set to the destination peripheral address.

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- Transfer width, word (32-bit).
- Transfer size, 3072 bytes (0xC00).
- Source and destination burst sizes, 16 transfers.
- Next LLI address, 0x2002 0020.

A chain of descriptors is built up, each one pointing to the next in the series. To initialize the DMA stream, the first LLI, 0x2002 0000, is programmed into the DMA Controller. When the first packet of data has been transferred the next LLI is automatically loaded.

The final LLI is stored at 0x2002 0070 and contains:

- Source start address 0x2003 1200.
- Destination address set to the destination peripheral address.
- Transfer width, word (32-bit).
- Transfer size, 3072 bytes (0xC00).
- Source and destination burst sizes, 16 transfers.
- Next LLI address, 0x0.

Because the next LLI address is set to zero, this is the last descriptor, and the DMA channel is disabled after transferring the last item of data. The channel is probably set to generate an interrupt at this point to indicate to the ARM processor that the channel can be reprogrammed.

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17.1 How to read this chapter

The SPIFI is available on all LPC18xx parts.

17.2 Basic configuration

The SPIFI is configured as follows:

- See Table 219 for clocking and power control.
- The SPIFI is reset by the SPIFI_RST (reset # 53).

Table 219. SPIFI clocking and power control

	Base clock	Branch clock	Maximum frequency
SPIFI AHB register clock (HCLK)	BASE_M3_CLK	CLK_M3_SPIFI	150 MHz
SPIFI serial clock input (SCKI)	BASE_SPIFI_CLK	SPIFI_CLK	132 MHz

17.3 Features

- Interfaces to serial flash memory in the main memory map.
- Supports 1-, 2-, and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Data rates of up to 66 MB per second.

17.4 General description

The SPI Flash Interface (SPIFI) allows low-cost serial flash memories to be connected to the Cortex-M3 processor with little performance penalty compared to parallel flash devices with higher pin count.

A driver API included in on-chip ROM handles setup, programming and erasure. After an initialize call to the SPIFI driver, the flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization. Quad devices then use a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices, and includes extensions to help insure compatibility with future devices.

Serial flash devices respond to commands sent by software or automatically sent by the SPIFI when software reads either of the two read-only serial flash regions in the memory map (see Table 220).

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Table 220. SPIFI flash memory map

Memory	Address
SPIFI data	0x1400 0000 to 0x17FF FFFF 0x8000 0000 to 0x87FF FFFF **Remark:** These are the spaces allocated to the SPIFI in the LPC18xx. The same data appears in the first area and the first half of the second area. These areas allow maxima of 64 and 128 MB of SPI flash (respectively) to be mapped into the Cortex-M3 memory space. In practice, the usable space is limited to the size of the connected device

Commands are divided into fields called opcode, address, intermediate, and data. The address, intermediate, and data fields are optional depending on the opcode. Some devices include a mode in which the opcode can be implied in read commands for higher performance. Data fields are further divided into input and output data fields depending on the opcode.

Remark: Flashless parts (LPC1850/30/20/10) can use the SPIFI for booting. See Section 3.3.4.3.

17.5 Pin description

Table 221. SPIFI Pin description

Pin	Direction	Description
SPIFI_SCK	O	Serial clock for the flash memory, switched only during active bits on the MOSI/IO0, MISO/IO1, and IO3:2 lines.
$\overline{\text{SPIFI_CS}}$	O	Chip select for the flash memory, driven low while a command is in progress, and high between commands. In the typical case of one serial slave, this signal can be connected directly to the device. If more than one serial slave is connected, software and off-chip hardware should use general-purpose I/O signals in combination with this signal to generate the chip selects for the various slaves.
SPIFI_MOSI or IO0	I/O	This is an output except in quad/dual input data fields. After a quad/dual input data field, it becomes an output again one serial clock period after $\overline{\text{CS}}$ goes high.
SPIFI_MISO or IO1	I/O	This is an output in quad/dual opcode, address, intermediate, and output data fields, and an input in SPI mode and in quad/dual input data fields. After an input data field in quad/dual mode, it becomes an output again one serial clock period after $\overline{\text{CS}}$ goes high.
SPIFI_SIO[3:2]	I/O	These are outputs in quad opcode, address, intermediate, and output data fields, and inputs in quad input data fields. If the flash memory does not have quad capability, these pins can be assigned to GPIO or other functions.

17.6 SPIFI API calls

The SPIFI interface is controlled through a set of simple API calls located in the LPC18xx ROM.

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18.1 How to read this chapter

The SD/MMC card interface is available on LPC18xx Rev ‘A’.

18.2 Basic configuration

Table 222. SDIO clocking and power control

	Base clock	Branch clock	Maximum frequency
SDIO register interface	BASE_M3_CLK	CLK_M3_SDIO	150 MHz
SDIO bit rate clock	BASE_SDIO_CLK	CLK_SDIO	<tbd>

The SDIO is reset by the SD_RST (reset # 20).

18.3 Features

The SD/MMC card interface supports the following modes:

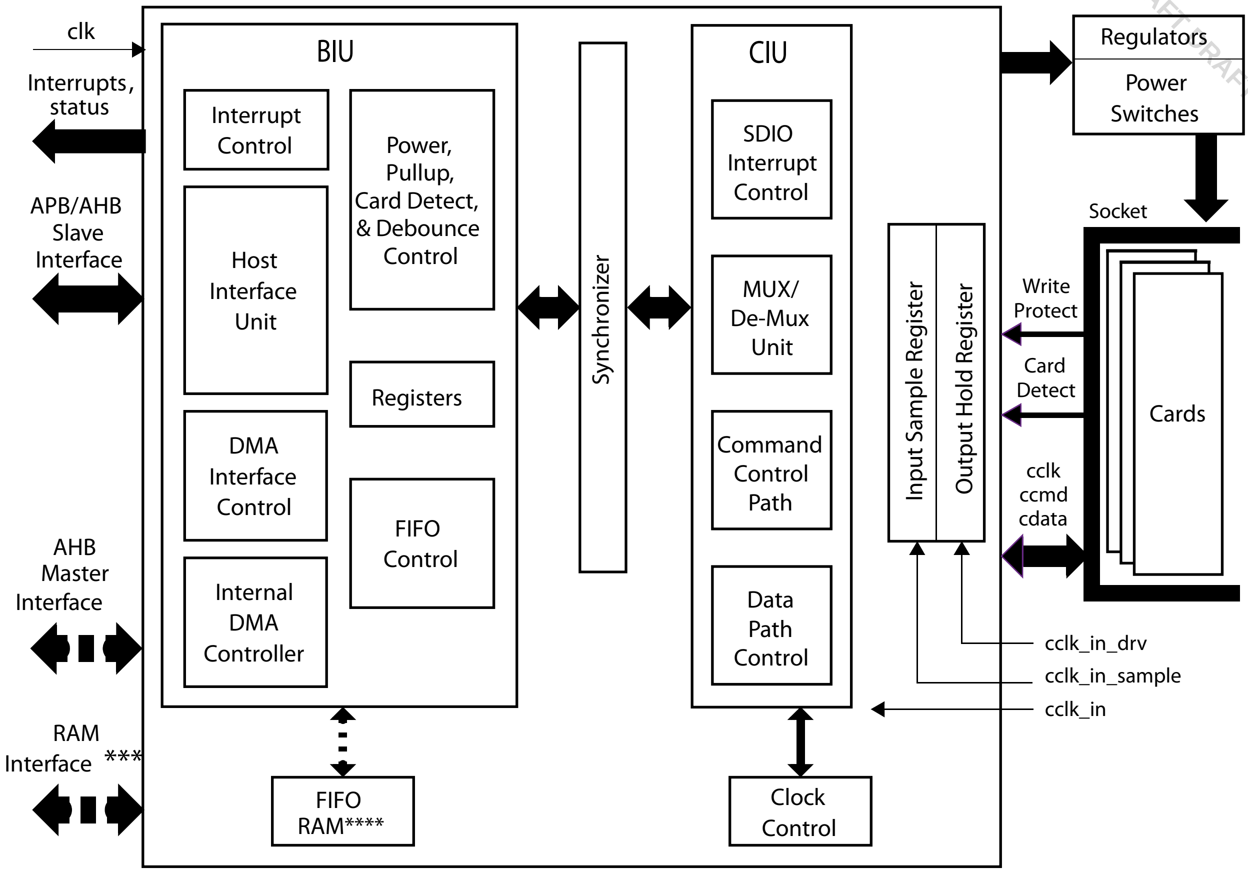
- Secure Digital memory (SD version 3.0)
- Secure Digital I/O (SDIO version 2.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.1)
- Multimedia Cards (MMC version 4.4)

18.4 General description

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*** Optional RAM Interface
**** FIFO RAM can be chosen as either internal or external RAM

Note: The card_detect and write-protect signals are from the SD/MMC card socket and not from the SD/MMC card.

Fig 28. SD/MMC block diagram

18.5 Pin description

Table 223. SDIO pin description

Pin name	Direction	Description
SD_CLK	O	SD/SDIO/MMC clock
SD_CD	O	SDIO card detect for single slot
SD_WP	O	SDIO card write protect
SD_LED	O	LED On signal. This signal cautions the user not to remove the SD card while it is accessed.
SD_CMD	I/O	Command input/output
SD_D[7:0]	I/O	Data input/output for data lines DAT[7:0]
SD_POW		
SD_VOLT[2:0]		

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<tbd>

18.6 Register description

Table 224. Register overview: SDMMC (base address: 0x4000 4000)

Name	Access	Address offset	Description	Reset value
CTRL	R/W	0x000	Control Register	
PWREN	R/W	0x004	Power Enable Register	
CLKDIV	R/W	0x008	Clock Divider Register	
CLKSRC	R/W	0x00C	SD Clock Source Register	
CLKENA	R/W	0x010	Clock Enable Register	
TMOUT	R/W	0x014	Time-out Register	
CTYPE	R/W	0x018	Card Type Register	
BLKSIZ	R/W	0x01C	Block Size Register	
BYTCNT	R/W	0x020	Byte Count Register	
INTMASK	R/W	0x024	Interrupt Mask Register	
CMDARG	R/W	0x028	Command Argument Register	0x00000000
CMD	R/W	0x02C	Command Register	0x00000000
RESP0	R	0x030	Response Register 0	0x00000000
RESP1	R	0x034	Response Register 1	0x00000000
RESP2	R	0x038	Response Register 2	0
RESP3	R	0x03C	Response Register 3	0
MINTSTS	r	0x040	Masked Interrupt Status Register	Reset value
RINTSTS	R/W	0x044	Raw Interrupt Status Register	0
STATUS	R	0x048	Status Register	
FIFOTH	R/W	0x04C	FIFO Threshold Watermark Register	
CDETECT	R	0x050	Card Detect Register	
WRTPRT	R	0x054	Write Protect Register	
GPIO	R/W	0x058	General Purpose Input/Output Register	
TCBCNT	R	0x05C	Transferred CIU Card Byte Count Register	0x00000000
TBBCNT	R	0x060	Transferred Host to BIU-FIFO Byte Count Register	0
DEBNCE	R/W	0x064	Debounce Count Register	
USRID	R/W	0x068	User ID Register	
VERID	R	0x06C	Version ID Register	0x5342230a
UHS_REG	R/W	0x074	UHS-1 Register	0x00000000
RST_N	R/W	0x078	Hardware Reset	
BMOD	R/W	0x080	Bus Mode Register	0x00000000
PLDMND	W	0x084	Poll Demand Register	0x00000000
DBADDR	R/W	0x088	Descriptor List Base Address Register	0x00000000
IDSTS	R/W	0x08C	Internal DMAC Status Register	0x00000000

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Table 224. Register overview: SDMMC (base address: 0x4000 4000)

Name	Access	Address offset	Description	Reset value
IDINTEN	R/W	0x090	Internal DMAC Interrupt Enable Register	0x00000000
DSCADDR	R	0x094	Current Host Descriptor Address Register	0x00000000
BUFADDR	R	0x098	Current Buffer Descriptor Address Register	0x00000000

18.6.1 Control Register (CTRL)

Table 225. Control Register (CTRL, address 0x4000 4000) bit description

Bit	Symbol	Value	Description	Reset value
0	CONTROLLER_RESET		Controller reset. To reset controller, firmware should set bit to 1. This bit is auto-cleared after two AHB and two cclk_in clock cycles. This resets: - BIU/CIU interface - CIU and state machines - abort_read_data, send_irq_response, and read_wait bits of Control register - start_cmd bit of Command register Does not affect any registers or DMA interface, or FIFO or host interrupts	0
		0	No change	
		1	Reset DWC_mobile_storage controller	
1	FIFO_RESET		Fifo reset. To reset FIFO, firmware should set bit to 1. This bit is auto-cleared after completion of reset operation. auto-cleared after two AHB clocks.	0
		0	No change	
		1	Reset to data FIFO To reset FIFO pointers	
2	DMA_RESET		dma_reset. To reset DMA interface, firmware should set bit to 1. This bit is auto-cleared after two AHB clocks.	0
		0	No change	
		1	Reset internal DMA interface control logic	
3	-		Reserved	-
4	INT_ENABLE		Global interrupt enable/disable bit. The int port is 1 only when this bit is 1 and one or more unmasked interrupts are set.	0
		0	Disable interrupts	
		1	Enable interrupts	
5	DMA_ENABLE		DMA enable. Valid only if DWC_mobile_storage configured for External DMA interface. Even when DMA mode is enabled, host can still push/pop data into or from FIFO; this should not happen during the normal operation. If there is simultaneous FIFO access from host/DMA, the data coherency is lost. Also, there is no arbitration inside DWC_mobile_storage to prioritize simultaneous host/DMA access.	0
		0	Disable DMA transfer mode	
		1	Enable DMA transfer mode	

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Table 225. Control Register (CTRL, address 0x4000 4000) bit description

Bit	Symbol	Value	Description	Reset value
6	READ_WAIT		read_wait. For sending read-wait to SDIO cards.	0
		0	Clear read wait	
		1	Assert read wait	
7	SEND_IRQ_RESPONSE		Send irq response. Bit automatically clears once response is sent. To wait for MMC card interrupts, host issues CMD40, and DWC_mobile_storage waits for interrupt response from MMC card(s). In meantime, if host wants DWC_mobile_storage to exit waiting for interrupt state, it can set this bit, at which time DWC_mobile_storage command state-machine sends CMD40 response on bus and returns to idle state.	0
		0	No change	
		1	Send auto IRQ response	
8	ABORT_READ_DATA		Abort read data. Used in SDIO card suspend sequence.	0
		0	No change	
		1	After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Bit automatically clears once data state machine resets to idle.	
9	SEND_CCSD		Send ccsd. When set, DWC_mobile_storage sends CCSD to CE-ATA device. Software sets this bit only if current command is expecting CCS (that is, RW_BLK) and interrupts are enabled in CE-ATA device. Once the CCSD pattern is sent to device, DWC_mobile_storage automatically clears send_ccsd bit. It also sets Command Done (CD) bit in RINTSTS register and generates interrupt to host if Command Done interrupt is not masked. NOTE: Once send_ccsd bit is set, it takes two card clock cycles to drive the CCSD on the CMD line. Due to this, during the boundary conditions it may happen that CCSD is sent to the CE-ATA device, even if the device signalled CCS.	0
		0	Clear bit if DWC_mobile_storage does not reset the bit.	
		1	Send Command Completion Signal Disable (CCSD) to CE-ATA device	
10	SEND_AUTO_STOP_CCSD		Send auto stop ccsd. NOTE: Always set send_auto_stop_ccsd and send_ccsd bits together; send_auto_stop_ccsd should not be set independent of send_ccsd. When set, DWC_Mobile_Storage automatically sends internallygenerated STOP command (CMD12) to CE-ATA device. After sending internally-generated STOP command, Auto Command Done (ACD) bit in RINTSTS is set and generates interrupt to host if Auto Command Done interrupt is not masked. After sending the CCSD, DWC_mobile_storage automatically clears send_auto_stop_ccsd bit.	0
		0	Clear bit if DWC_mobile_storage does not reset the bit.	
		1	Send internally generated STOP after sending CCSD to CE-ATA device.	

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Table 225. Control Register (CTRL, address 0x4000 4000) bit description

Bit	Symbol	Value	Description	Reset value
11	CEATA_DEVICE_INTE RRUPT _STATUS		CEATA device interrupt status. Software should appropriately write to this bit after power-on reset or any other reset to CE-ATA device. After reset, usually CE-ATA device interrupt is disabled (nIEN = 1). If the host enables CE-ATA device interrupt, then software should set this bit.	0
		0	Interrupts not enabled in CE-ATA device (nIEN = 1 in ATA control register)	
		1	Interrupts are enabled in CE-ATA device (nIEN = 0 in ATA control register)	
15:12	-		Reserved	
19:16	CARD_VOLTAGE_A		Card regulator-A voltage setting; output to card_volt_a port. Optional feature; ports can be used as general-purpose outputs.	0
23:20	CARD_VOLTAGE_B		Card regulator-B voltage setting; output to card_volt_b port. Optional feature; ports can be used as general-purpose outputs.	0
24	ENABLE_OD_PULLUP		External open-drain pull up. Inverted value of this bit is output to ccmd_od_pullup_en_n port. When bit is set, command output always driven in open-drive mode; that is, DWC_mobile_storage drives either 0 or high impedance, and does not drive hard 1.	1
		0	Disable	
		1	Enable	
25	USE_INTERNAL_DMA C		Present only for the Internal DMAC configuration; else, it is reserved.	0
		0	The host performs data transfers through the slave interface	
		1	Internal DMAC used for data transfer	
31:26	-		Reserved	

18.6.2 Power Enable Register (PWREN)

Table 226. Power Enable Register (PWREN, address 0x4000 4004) bit description

Bit	Symbol	Description	Reset value
29:0	POWER_ENABLE	Power on/off switch for up to 16 cards; for example, bit[0] controls card 0. Once power is turned on, firmware should wait for regulator/switch ramp-up time before trying to initialize card. 0 - power off 1 - power on Only NUM_CARDS number of bits are implemented. Bit values output to card_power_en port. Optional feature; ports can be used as general-purpose outputs.	0
31:30	-	Reserved	

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18.6.3 Clock Divider Register (CLKDIV)

Table 227. Clock Divider Register (CLKDIV, address 0x4000 4008) bit description

Bit	Symbol	Description	Reset value
7:0	CLK_DIVIDER0	Clock divider-0 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), value of 1 means divide by 2*1 = 2, value of ff means divide by 2*255 = 510, and so on.	0
15:8	CLK_DIVIDER1	Clock divider-1 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), value of 1 means divide by 2*1 = 2, value of ff means divide by 2*255 = 510, and so on. In MMC-Ver3.3-only mode, bits not implemented because only one clock divider is supported.	0
23:16	CLK_DIVIDER2	Clock divider-2 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), value of 1 means divide by 2*1 = 2, value of ff means divide by 2*255 = 510, and so on. In MMC-Ver3.3-only mode, bits not implemented because only one clock divider is supported.	0
31:24	CLK_DIVIDER3	Clock divider-3 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), a value of 1 means divide by 2*1 = 2, a value of ff means divide by 2*255 = 510, and so on. In MMC-Ver3.3-only mode, bits not implemented because only one clock divider is supported. divide by 2*0 = 0 (no division, bypass), value of 1 means divide by 2*1 = 2, value of ff means divide by 2*255 = 510, and so on. In MMC-Ver3.3-only mode, bits not implemented because only one clock divider is supported.	0

18.6.4 SD Clock Source Register (CLKSRC)

Table 228. SD Clock Source Register (CLKSRC, address 0x4000 400C) bit description

Bit	Symbol	Description	Reset value
31:0	CLK_SOURCE	Clock divider source for up to 16 SD cards supported. Each card has two bits assigned to it. For example, bits[1:0] assigned for card-0, which maps and internally routes clock divider[3:0] outputs to cclk_out[15:0] pins, depending on bit value. 00 - Clock divider 0 01 - Clock divider 1 10 - Clock divider 2 11 - Clock divider 3 In MMC-Ver3.3-only controller, only one clock divider supported. The cclk_out is always from clock divider 0, and this register is not implemented.	0

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18.6.5 Clock Enable Register (CLKENA)

Table 229. Clock Enable Register (CLKENA, address 0x4000 4010) bit description

Bit	Symbol	Description	Reset value
15:0	CCLK_ENABLE	Low-power control for up to 16 SD card clocks and one MMC card clock supported. 0 - Non-low-power mode 1 - Low-power mode; stop clock when card in IDLE (should be normally set to only MMC and SD memory cards; for SDIO cards, if interrupts must be detected, clock should not be stopped). In MMC-Ver3.3-only mode, since there is only one cclk_out, only cclk_low_power[0] is used. supported. 0 - Clock disabled 1 - Clock enabled In MMC-Ver3.3-only mode, since there is only one cclk_out, only cclk_enable[0] is used.	0
31:16	CCLK_LOW_POWER	Clock-enable control for up to 16 SD card clocks and one MMC card clock supported. 0 - Clock disabled 1 - Clock enabled In MMC-Ver3.3-only mode, since there is only one cclk_out, only cclk_enable[0] is used. supported. 0 - Non-low-power mode 1 - Low-power mode; stop clock when card in IDLE (should be normally set to only MMC and SD memory cards; for SDIO cards, if interrupts must be detected, clock should not be stopped). In MMC-Ver3.3-only mode, since there is only one cclk_out, only cclk_low_power[0] is used.	0

18.6.6 Time-out Register (TMOUT)

Table 230. Time-out Register (TMOUT, address 0x4000 4014) bit description

Bit	Symbol	Description	Reset value
7:0	RESPONSE_TIMEOUT	Response time-out value. Value is in number of card output clocks - cclk_out.	0x40
31:8	DATA_TIMEOUT	Value for card Data Read time-out; same value also used for Data Starvation by Host time-out. Value is in number of card output clocks - cclk_out of selected card. Starvation by Host time-out. Value is in number of card output clocks - cclk_out of selected card.	0xFFFFFF

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18.6.7 Card Type Register (CTYPE)

Table 231. Card Type Register (CTYPE, address 0x4000 4018) bit description

Bit	Symbol	Description	Reset value
15:0	CARD_WIDTH	One bit per card indicates if card is 1-bit or 4-bit: 0 - 1-bit mode 1 - 4-bit mode Bit[15] corresponds to card[15], bit[0] corresponds to card[0]. Only NUM_CARDS*2 number of bits are implemented.	0
31:16	CARD_WIDTH	One bit per card indicates if card is 8-bit: 0 - Non 8-bit mode 1 - 8-bit mode Bit[31] corresponds to card[15]; bit[16] corresponds to card[0].	0

18.6.8 Block Size Register (BLKSIZ)

Table 232. Block Size Register (BLKSIZ, address 0x4000 401C) bit description

Bit	Symbol	Description	Reset value
15:0	BLOCK_SIZE	Block size	0x200
31:16	-	Reserved	

18.6.9 Byte Count Register (BYTCNT)

Table 233. Byte Count Register (BYTCNT, address 0x4000 4020) bit description

Bit	Symbol	Description	Reset value
31:0	BYTE_COUNT	Number of bytes to be transferred; should be integer multiple of Block Size for block transfers. For undefined number of byte transfers, byte count should be set to 0. When byte count is set to 0, it is responsibility of host to explicitly send stop/abort command to terminate data transfer.	0x200

18.6.10 Interrupt Mask Register (INTMASK)

Table 234. Interrupt Mask Register (INTMASK, address 0x4000 4024) bit description

Bit	Symbol	Description	Reset value
0	CD	Card detect. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
1	RE	Response error. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
2	CD	Command done. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
3	DTO	Data transfer over. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
4	TXDR	Transmit FIFO data request. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0

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Table 234. Interrupt Mask Register (INTMASK, address 0x4000 4024) bit description

Bit	Symbol	Description	Reset value
5	RXDR	Receive FIFO data request. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
6	RCRC	Response CRC error. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
7	DCRC	Data CRC error. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
8	RTO	Response time-out. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
9	DRTO	Data read time-out. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
10	HTO	Data starvation-by-host time-out (HTO) /Volt_switch_int. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
11	FRUN	FIFO underrun/overrun error. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
12	HLE	Hardware locked write error. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
13	SBE	Start-bit error. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
14	ACD	Auto command done. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
15	EBE	End-bit error (read)/Write no CRC. Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt.	0
31:16	SDIO_INT_MASK	Mask SDIO interrupts One bit for each card. Bit[31] corresponds to card[15], and bit[16] corresponds to card[0]. When masked, SDIO interrupt detection for that card is disabled. A 0 masks an interrupt, and 1 enables an interrupt. In MMC-Ver3.3-only mode, these bits are always 0.	0

18.6.11 Command Argument Register (CMDARG)

Table 235. Command Argument Register (CMDARG, address 0x4000 4028) bit description

Bit	Symbol	Description	Reset value
31:0	CMD_ARG	Value indicates command argument to be passed to card.	0

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18.6.12 Command Register (CMD)

Table 236. Command Register (CMD, address 0x4000 402C) bit description

Bit	Symbol	Value	Description	Reset value
5:0	CMD_INDEX		Command index	0
6	RESPONSE_EXPECT		response expect	0
		0	No response expected from card	
		1	Response expected from card	
7	RESPONSE_ LENGTH		response length	0
		0	Short response expected from card	
		1	Long response expected from card	
8	CHECK_RESPONSE_CRC		check response crc Some of command responses do not return valid CRC bits. Software should disable CRC checks for those commands in order to disable CRC checking by controller.	0
		0	Do not check response CRC	
		1	Check response CRC	
9	DATA_EXPECTED		data expected	0
		0	No data transfer expected (read/write)	
		1	Data transfer expected (read/write)	
10	READ_WRITE		read/write. Don't care if no data expected from card.	0
		0	Read from card	
		1	Data transfer expected (read/write)	
11	TRANSFER_MODE		transfer mode. Don't care if no data expected.	0
		0	Block data transfer command	
		1	Stream data transfer command	
12	SEND_AUTO_STOP		send auto stop. When set, DWC_mobile_storage sends stop command to SD_MMC_CEATA cards at end of data transfer. Refer to <tbd> to determine: - when send_auto_stop bit should be set, since some data transfers do not need explicit stop commands - open-ended transfers that software should explicitly send to stop command Additionally, when resume is sent to resume - suspended memory access of SD-Combo card - bit should be set correctly if suspended data transfer needs send_auto_stop. Don't care if no data expected from card.	0
		0	No stop command sent at end of data transfer	
		1	Send stop command at end of data transfer	
13	WAIT_PRVDATA_COMPLETE		wait prvdata complete. The wait_prvdata_complete = 0 option typically used to query status of card during data transfer or to stop current data transfer; card_number should be same as in previous command.	0
		0	Send command at once, even if previous data transfer has not completed.	
		1	Wait for previous data transfer completion before sending command.	

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Table 236. Command Register (CMD, address 0x4000 402C) bit description

Bit	Symbol	Value	Description	Reset value
14	STOP_ABORT_CMD		stop abort cmd. When open-ended or predefined data transfer is in progress, and host issues stop or abort command to stop data transfer, bit should be set so that command/data state-machines of CIU can return correctly to idle state. This is also applicable for Boot mode transfers. To Abort boot mode, this bit should be set along with CMD[26] = disable_boot.	0
		0	Neither stop nor abort command to stop current data transfer in progress. If abort is sent to function-number currently selected or not in data-transfer mode, then bit should be set to 0.	
		1	Stop or abort command intended to stop current data transfer in progress.	
15	SEND_INITIALIZATION		send initialization. After power on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit should be set while sending first command to card so that controller will initialize clocks before sending command to card. This bit should not be set for either of the boot modes (alternate or mandatory).	0
		0	Do not send initialization sequence (80 clocks of 1) before sending this command.	
		1	Send initialization sequence before sending this command.	
20:16	CARD_NUMBER		card number. Card number in use. Represents physical slot number of card being accessed. In MMC-Ver3.3-only mode, up to 30 cards are supported; in SD-only mode, up to 16 cards are supported. Registered version of this is reflected on dw_dma_card_num and ge_dma_card_num ports, which can be used to create separate DMA requests, if needed. In addition, in SD mode this is used to mux or demux signals from selected card because each card is interfaced to DWC_mobile_storage by separate bus.	0
21	UPDATE_CLOC_REGISTERS_ONLY		update clock registers only. Following register values transferred into card clock domain: CLKDIV, CLRSRC, CLKENA. Changes card clocks (change frequency, truncate off or on, and set low-frequency mode); provided in order to change clock frequency or stop clock without having to send command to cards. During normal command sequence, when update_clock_registers_only = 0, following control registers are transferred from BIU to CIU: CMD, CMDARG, TMOUT, CTYPE, BLKSIZ, BYTCNT. CIU uses new register values for new command sequence to card(s). When bit is set, there are no Command Done interrupts because no command is sent to SD_MMC_CEATA cards. registers_only.	0
		0	Normal command sequence	
		1	Do not send commands, just update clock register value into card clock domain	

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Table 236. Command Register (CMD, address 0x4000 402C) bit description

Bit	Symbol	Value	Description	Reset value
22	READ_CEATA_DEVICE		read ceata device. Software should set this bit to indicate that CE-ATA device is being accessed for read transfer. This bit is used to disable read data time-out indication while performing CE-ATA read transfers. Maximum value of I/O transmission delay can be no less than 10 seconds. DWC_mobile_storage should not indicate read data time-out while waiting for data from CE-ATA device.	0
		0	Host is not performing read access (RW_REG or RW_BLK) towards CE-ATA device.	
		1	Host is performing read access (RW_REG or RW_BLK) towards CE-ATA device.	
23	CCS_EXPECTED		ccs expected. If the command expects Command Completion Signal (CCS) from the CE-ATA device, the software should set this control bit. DWC_mobile_storage sets Data Transfer Over (DTO) bit in RINTSTS register and generates interrupt to host if Data Transfer Over interrupt is not masked.	0
		0	Interrupts are not enabled in CE-ATA device (nIEN = 1 in ATA control register), or command does not expect CCS from device.	
		1	Interrupts are enabled in CE-ATA device (nIEN = 0), and RW_BLK command expects command completion signal from CE-ATA device.	
24	ENABLE_BOOT		Enable Boot - this bit should be set only for mandatory boot mode. When Software sets this bit along with start_cmd, CIU starts the boot sequence for the corresponding card by asserting the CMD line low. Do NOT set disable_boot and enable_boot together.	0
25	EXPECT_BOOT_ACK		Expect Boot Acknowledge. When Software sets this bit along with enable_boot, CIU expects a boot acknowledge start pattern of 0-1-0 from the selected card.	0
26	DISABLE_BOOT		Disable Boot. When software sets this bit along with start_cmd, CIU terminates the boot operation. Do NOT set disable_boot and enable_boot together.	0
27	BOOT_MODE		Boot Mode	0
		0	Mandatory Boot operation	
		1	Alternate Boot operation	
28	VOLT_SWITCH		Voltage switch bit	0
		0	No voltage switching	
		1	Voltage switching enabled; must be set for CMD11 only	
30:29	-		Reserved	
31	START_CMD		Start command. Once command is taken by CIU, bit is cleared. When bit is set, host should not attempt to write to any command registers. If write is attempted, hardware lock error is set in raw interrupt register. Once command is sent and response is received from SD_MMC_CEATA cards, Command Done bit is set in raw interrupt register.	

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18.6.13 Response Register 0 (RESP0)

Table 237. Response Register 0 (RESP0, address 0x4000 4030) bit description

Bit	Symbol	Description	Reset value
31:0	RESPONSE0	Bit[31:0] of response	0

18.6.14 Response Register 1 (RESP1)

Table 238. Response Register 1 (RESP1, address 0x4000 4034) bit description

Bit	Symbol	Description	Reset value
31:0	RESPONSE1	Register represents bit[63:32] of long response. When CIU sends auto-stop command, then response is saved in register. Response for previous command sent by host is still preserved in Response 0 register. Additional auto-stop issued only for data transfer commands, and response type is always short for them. For information on when CIU sends auto-stop commands, refer to Auto-Stop <tbd>.	0

18.6.15 Response Register 2 (RESP2)

Table 239. Response Register 2 (RESP2, address 0x4000 4038) bit description

Bit	Symbol	Description	Reset value
31:0	RESPONSE2	Bit[95:64] of long response	0

18.6.16 Response Register 3 (RESP3)

Table 240. Response Register 3 (RESP3, address 0x4000 403C) bit description

Bit	Symbol	Description	Reset value
31:0	RESPONSE3	Bit[127:96] of long response	0

18.6.17 Masked Interrupt Status Register (MINTSTS)

Table 241. Masked Interrupt Status Register (MINTSTS, address 0x4000 4040) bit description

Bit	Symbol	Description	Reset value
0	CD	Card detect. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
1	RE	Response error. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
2	CD	Command done. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
3	DTO	Data transfer over. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
4	TXDR	Transmit FIFO data request. Interrupt enabled only if corresponding bit in interrupt mask register is set.	

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Table 241. Masked Interrupt Status Register (MINTSTS, address 0x4000 4040) bit description

Bit	Symbol	Description	Reset value
5	RXDR	Receive FIFO data request. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
6	RCRC	Response CRC error. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
7	DCRC	Data CRC error. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
8	RTO	Response time-out. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
9	DRTO	Data read time-out. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
10	HTO	Data starvation-by-host time-out (HTO). Interrupt enabled only if corresponding bit in interrupt mask register is set.	
11	FRUN	FIFO underrun/overrun error. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
12	HLE	Hardware locked write error. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
13	SBE	Start-bit error. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
14	ACD	Auto command done. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
15	EBE	End-bit error (read)/write no CRC. Interrupt enabled only if corresponding bit in interrupt mask register is set.	
31:16	SDIO_INTERRUPT	Interrupt from SDIO card; one bit for each card. Bit[31] corresponds to Card[15], and bit[16] is for Card[0]. SDIO interrupt for card enabled only if corresponding sdio_int_mask bit is set in Interrupt mask register (mask bit 1 enables interrupt; 0 masks interrupt). 0 - No SDIO interrupt from card 1 - SDIO interrupt from card In MMC-Ver3.3-only mode, bits always 0.	

18.6.18 Raw Interrupt Status Register (RINTSTS)

Table 242. Raw Interrupt Status Register (RINTSTS, address 0x4000 4044) bit description

Bit	Symbol	Description	Reset value
0	CD	Card detect. Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
1	RE	Response error. Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
2	CD	Command done. Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
3	DTO	Data transfer over. Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0

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Table 242. Raw Interrupt Status Register (RINTSTS, address 0x4000 4044) bit description

Bit	Symbol	Description	Reset value
4	TXDR	Transmit FIFO data request. Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
5	RXDR	Receive FIFO data request. Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
6	RCRC	Response CRC error. Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
7	DCRC	Data CRC error. Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
8	RTO_BAR	Response time-out (RTO)/Boot Ack Received (BAR). Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
9	DRTO_BDS	Data read time-out (DRTO)/Boot Data Start (BDS). Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
10	HTO	Data starvation-by-host time-out (HTO). Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status./Volt_switch_int	0
11	FRUN	FIFO underrun/overrun error. Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
12	HLE	Hardware locked write error. Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
13	SBE	Start-bit error. Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
14	ACD	Auto command done. Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
15	EBE	End-bit error (read)/write no CRC. Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status.	0
31:16	SDIO_INTERRUPT	Interrupt from SDIO card; one bit for each card. Bit[31] corresponds to Card[15], and bit[16] is for Card[0]. Writes to these bits clear them. Value of 1 clears bit and 0 leaves bit intact. 0 - No SDIO interrupt from card 1 - SDIO interrupt from card In MMC-Ver3.3-only mode, bits always 0. Bits are logged regardless of interrupt-mask status.	0

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18.6.19 Status Register (STATUS)

Table 243. Status Register (STATUS, address 0x4000 4048) bit description

Bit	Symbol	Description	Reset value
0	FIFO_RX_WATERMARK	FIFO reached Receive watermark level; not qualified with data	0
1	FIFO_TX_WATERMARK	FIFO reached Transmit watermark level; not qualified with data transfer.	1
2	FIFO_EMPTY	FIFO is empty status	1
3	FIFO_FULL	FIFO is full status	0
7:4	CMDFSMSTATES	Command FSM states: 0 - Idle 1 - Send init sequence 2 - Tx cmd start bit 3 - Tx cmd tx bit 4 - Tx cmd index + arg 5 - Tx cmd crc7 6 - Tx cmd end bit 7 - Rx resp start bit 8 - Rx resp IRQ response 9 - Rx resp tx bit 10 - Rx resp cmd idx 11 - Rx resp data 12 - Rx resp crc7 13 - Rx resp end bit 14 - Cmd path wait NCC 15 - Wait; CMD-to-response turnaround NOTE: The command FSM state is represented using 19 bits. The STATUS Register(7:4) has 4 bits to represent the command FSM states. Using these 4 bits, only 16 states can be represented. Thus three states cannot be represented in the STATUS(7:4) register. The three states that are not represented in the STATUS Register(7:4) are: - Bit 16 - Wait for CCS - Bit 17 - Send CCSD - Bit 18 - Boot Mode Due to this, while command FSM is in Wait for CCS state or Send CCSD or Boot Mode?, the Status register indicates status as 0 for the bit field 7:4.	0
8	DATA_3_STATUS	Raw selected card_data[3]; checks whether card is present 0 - card not present 1 - card present	
9	DATA_BUSY	Inverted version of raw selected card_data[0] 0 - card data not busy 1 - card data busy	
10	DATA_STATE_MC_BUSY	Data transmit or receive state-machine is busy	1
16:11	RESPONSE_INDEX	Index of previous response, including any auto-stop sent by core.	0
29:17	FIFO_COUNT	FIFO count - Number of filled locations in FIFO	0
30	DMA_ACK	DMA acknowledge signal state; either dw_dma_ack or ge_dma_ack, depending on DW-DMA or Generic-DMA selection.	0
31	DMA_REQ	DMA request signal state; either dw_dma_req or ge_dma_req, depending on DW-DMA or Generic-DMA selection.	0

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18.6.20 FIFO Threshold Watermark Register (FIFOTH)

Table 244. FIFO Threshold Watermark Register (FIFOTH, address 0x4000 404C) bit description

Bit	Symbol	Value	Description	Reset value
11:0	TX_WMARK		FIFO threshold watermark level when transmitting data to card. When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. If Interrupt is enabled, then interrupt occurs. During end of packet, request or interrupt is generated, regardless of threshold programming. In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty). In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. 12 bits - 1 bit less than FIFO-count of status register, which is 13 bits. Limitation: TX_WMark >= 1; Recommended: FIFO_DEPTH/2; (means less than or equal to FIFO_DEPTH/2).	
15:12	-		Reserved.	
27:16	RX_WMARK		FIFO threshold watermark level when receiving data to card. When FIFO data count reaches greater than this number, DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data. In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt. In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set. 12 bits - 1 bit less than FIFO-count of status register, which is 13 bits. Limitation: RX_WMark less than FIFO_DEPTH-2 Recommended: (FIFO_DEPTH/2) - 1; (means greater than (FIFO_DEPTH/2) - 1) NOTE: In DMA mode during CCS time-out, the DMA does not generate the request at the end of packet, even if remaining bytes are less than threshold. In this case, there will be some data left in the FIFO. It is the responsibility of the application to reset the FIFO after the CCS time-out.	

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Table 244. FIFO Threshold Watermark Register (FIFOTH, address 0x4000 404C) bit description

Bit	Symbol	Value	Description	Reset value
30:28	DW_DMA_MUTIPLE_ TRANSACTION_ SIZE		Burst size of multiple transaction; should be programmed same as DW-DMA controller multiple-transaction-size SRC/DEST_MSIZE.The units for transfers is the H_DATA_WIDTH parameter. A single transfer (dw_dma_single assertion in case of Non DW DMA interface) would be signalled based on this value. Value should be sub-multiple of (RX_WMark + 1)* (F_DATA_WIDTH/H_DATA_WIDTH) and (FIFO_DEPTH - TX_WMark)* (F_DATA_WIDTH/ H_DATA_WIDTH) For example, if FIFO_DEPTH = 16, FDATA_WIDTH == H_DATA_WIDTH Allowed combinations for MSize and TX_WMark are: MSize = 1, TX_WMARK = 1-15 MSize = 4, TX_WMark = 8 MSize = 4, TX_WMark = 4 MSize = 4, TX_WMark = 12 MSize = 8, TX_WMark = 8 MSize = 8, TX_WMark = 4. Allowed combinations for MSize and RX_WMark are: MSize = 1, RX_WMARK = 0-14 MSize = 4, RX_WMark = 3 MSize = 4, RX_WMark = 7 MSize = 4, RX_WMark = 11 MSize = 8, RX_WMark = 7 MSize = 8, RX_WMark = 11 Recommended: MSize = 8, TX_WMark = 8, RX_WMark = 7	0
		0x0	1 transfer	
		0x1	4 transfers	
		0x2	8 transfers	
		0x3	16 transfers	
		0x4	32 transfers	
		0x5	64 transfers	
		0x6	128 transfers	
		0x7	256 transfers	
31	-		Reserved	

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18.6.21 Card Detect Register (CDETECT)

Table 245. Card Detect Register (CDETECT, address 0x4000 4050) bit description

Bit	Symbol	Description	Reset value
29:0	CARD_DETECT_N	Value on card_detect_n input ports (1 bit per card); read-only bits. 0 represents presence of card. Only NUM_CARDS number of bits are implemented.	
31:30	-	Reserved	

18.6.22 Write Protect Register (WRTPRT)

Table 246. Write Protect Register (WRTPRT, address 0x4000 4054) bit description

Bit	Symbol	Description	Reset value
29:0	WRITE_PROTECT	Value on card_write_prt input ports (1 bit per card). 1 represents write protection. Only NUM_CARDS number of bits are implemented.	
31:30	-	Reserved	

18.6.23 General Purpose Input/Output Register (GPIO)

Table 247. General Purpose Input/Output Register (GPIO, address 0x4000 4058) bit description

Bit	Symbol	Description	Reset value
7:0	GPI	Value on gpi input ports; this portion of register is read-only. Valid only when AREA_OPTIMIZED parameter is 0.	
23:8	GPO	Value needed to be driven to gpo pins; this portion of register is read/write. Valid only when AREA_OPTIMIZED parameter is 0.	0
31:24	-	Reserved	

18.6.24 Transferred CIU Card Byte Count Register (TCBCNT)

Table 248. Transferred CIU Card Byte Count Register (TCBCNT, address 0x4000 405C) bit description

Bit	Symbol	Description	Reset value
31:0	TRANS_CARD_BYTE_COUNT	Number of bytes transferred by CIU unit to card. In 32-bit or 64-bit AMBA data-bus-width modes, register should be accessed in full to avoid read-coherency problems. In 16-bit AMBA data-bus-width mode, internal 16-bit coherency register is implemented. User should first read lower 16 bits and then higher 16 bits. When reading lower 16 bits, higher 16 bits of counter are stored in temporary register. When higher 16 bits are read, data from temporary register is supplied. Both TCBCNT and TBBCNT share same coherency register. When AREA_OPTIMIZED parameter is 1, register should be read only after data transfer completes; during data transfer, register returns 0.	0

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18.6.25 Transferred Host to BIU-FIFO Byte Count Register (TBBCNT)

Table 249. Transferred Host to BIU-FIFO Byte Count Register (TBBCNT, address 0x4000 4060) bit description

Bit	Symbol	Description	Reset value
31:0	TRANS_FIFO_BYTE_COUNT	Number of bytes transferred between Host/DMA memory and BIU FIFO. In 32-bit or 64-bit AMBA data-bus-width modes, register should be accessed in full to avoid read-coherency problems. In 16-bit AMBA data-bus-width mode, internal 16-bit coherency register is implemented. User should first read lower 16 bits and then higher 16 bits. When reading lower 16 bits, higher 16 bits of counter are stored in temporary register. When higher 16 bits are read, data from temporary register is supplied. Both TCBCNT and TBBCNT share same coherency register.	0

18.6.26 Debounce Count Register (DEBNCE)

Table 250. Debounce Count Register (DEBNCE, address 0x4000 4064) bit description

Bit	Symbol	Description	Reset value
23:0	DEBOUNCE_COUNT	Number of host clocks (clk) used by debounce filter logic; typical debounce time is 5-25 ms.	0xFFFFFF
31:24	-	Reserved	

18.6.27 User ID Register (USRID)

Table 251. User ID Register (USRID, address 0x4000 4068) bit description

Bit	Symbol	Description	Reset value
31:0	USRID	User identification register; value set by user. Default reset value can be picked by user while configuring core before synthesis. Can also be used as scratch pad register by user.	NA

18.6.28 Version ID Register (VERID)

Table 252. Version ID Register (VERID, address 0x4000 406C) bit description

Bit	Symbol	Description	Reset value
31:0	VERID	Version identification register; register value is hard-wired. Can be read by firmware to support different versions of core.	0x5342230a

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18.6.29 UHS-1 Register (UHS_REG)

Table 253. UHS-1 Register (UHS_REG, address 0x4000 4074) bit description

Bit	Symbol	Description	Reset value
15:0	VOLT_REG	High Voltage mode. Determines the voltage fed to the buffers by an external voltage regulator. 0 - Buffers supplied with 3.3V Vdd 1 - Buffers supplied with 1.8V Vdd These bits function as the output of the host controller and are fed to an external voltage regulator. The voltage regulator must switch the voltage of the buffers of a particular card to either 3.3V or 1.8V, depending on the value programmed in the register. VOLT_REG[0] should be set to 1 for card number 0 in order to make it operate for 1.8V.	0
31:16	DDR_REG	DDR mode. Determines the voltage fed to the buffers by an external voltage regulator. 0 - Non-DDR mode 1 - DDR mode UHS_REG [16] should be set for card number 0, UHS_REG [17] for card number 1 and so on.	0

18.6.30 Hardware Reset (RST_N)

Table 254. Hardware Reset (RST_N, address 0x4000 4078) bit description

Bit	Symbol	Description	Reset value
15:0	CARD_RESET	Hardware reset. 1 - Active mode 0 - Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized. CARD_RESET[0] should be set to 1 to reset card number 0, and CARD_RESET[15] should be set to reset card number 15. The number of bits implemented is restricted to NUM_CARDS.	1
31:16	-	Reserved	

18.6.31 Bus Mode Register (BMOD)

Table 255. Bus Mode Register (BMOD, address 0x4000 4080) bit description

Bit	Symbol	Value	Description	Reset value
0	SWR		Software Reset. When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.	0
1	FB		Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations. FB is read/write.	0
6:2	DSL		Descriptor Skip Length. Specifies the number of HWord/Word/Dword (depending on 16/32/64-bit bus) to skip between two unchained descriptors. This is applicable only for dual buffer structure. DSL is read/write.	0
7	DE		IDMAC Enable. When set, the IDMAC is enabled. DE is read/write.	

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Table 255. Bus Mode Register (BMOD, address 0x4000 4080) bit description

Bit	Symbol	Value	Description	Reset value
10:8	PBL		Programmable Burst Length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of FIFOTH register. In order to change this value, write the required value to FIFOTH register. This is an encode value as follows.Transfer unit is either 16, 32, or 64 bits, based on HDATA_WIDTH. PBL is a read-only value.	0
		0x0	1 transfer	
		0x1	4 transfers	
		0x2	8 transfers	
		0x3	16 transfers	
		0x4	32 transfers	
		0x5	64 transfers	
		0x6	128 transfers	
		0x7	256 transfers	
31:11	-		Reserved	

18.6.32 Poll Demand Register (PLDMND)

Table 256. Poll Demand Register (PLDMND, address 0x4000 4084) bit description

Bit	Symbol	Description	Reset value
31:0	PD	Poll Demand. If the OWN bit of a descriptor is not set, the FSM goes to the Suspend state. The host needs to write any value into this register for the IDMAC FSM to resume normal descriptor fetch operation. This is a write only register. PD bit is write-only.	

18.6.33 Descriptor List Base Address Register (DBADDR)

Table 257. Descriptor List Base Address Register (DBADDR, address 0x4000 4088) bit description

Bit	Symbol	Description	Reset value
31:0	SDL	Start of Descriptor List. Contains the base address of the First Descriptor. The LSB bits [0/1/2:0] for 16/32/64-bit bus-width) are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.	0

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18.6.34 Internal DMAC Status Register (IDSTS)

Table 258. Internal DMAC Status Register (IDSTS, address 0x4000 408C) bit description

Bit	Symbol	Description	Reset value
0	TI	Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing a 1 clears this bit.	0
1	RI	Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.	0
2	FBE	Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.	0
3	-	Reserved	
4	DU	Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.	0
5	CES	Card Error Summary. Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE - End Bit Error RTO - Response Time-out/Boot Ack Time-out RCRC - Response CRC SBE - Start Bit Error DRTO - Data Read Time-out/BDS time-out DCRC - Data CRC for Receive RE - Response Error Writing a 1 clears this bit.	0
7:6	-	Reserved	
8	NIS	Normal Interrupt Summary. Logical OR of the following: IDSTS[0] - Transmit Interrupt IDSTS[1] - Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.	0
9	AIS	Abnormal Interrupt Summary. Logical OR of the following: IDSTS[2] - Fatal Bus Interrupt IDSTS[4] - DU bit Interrupt IDSTS[5] - Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.	0
12:10	EB	Error Bits. Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (IDSTS[2]) set. This field does not generate an interrupt. 001 - Host Abort received during transmission 010 - Host Abort received during reception Others: Reserved EB is read-only.	0
16:13	FSM	DMAC FSM present state. 0 - DMA_IDLE 1 - DMA_SUSPEND 2 - DESC_RD 3 - DESC_CHK 4 - DMA_RD_REQ_WAIT 5 - DMA_WR_REQ_WAIT 6 - DMA_RD 7 - DMA_WR 8 - DESC_CLOSE This bit is read-only.	0
31:16	-	Reserved	

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18.6.35 Internal DMAC Interrupt Enable Register (IDINTEN)

Table 259. Internal DMAC Interrupt Enable Register (IDINTEN, address 0x4000 4090) bit description

Bit	Symbol	Description	Reset value
0	TI	Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.	0
1	RI	Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.	0
2	FBE	Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.	0
3	-	Reserved	
4	DU	Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the DU interrupt is enabled.	0
5	CES	Card Error summary Interrupt Enable. When set, it enables the Card Interrupt summary.	0
7:6	-	Reserved	
8	NIS	Normal Interrupt Summary Enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: IDINTEN[0] - Transmit Interrupt IDINTEN[1] - Receive Interrupt	0
9	AIS	Abnormal Interrupt Summary Enable. When set, an abnormal interrupt is enabled. This bit enables the following bits: IDINTEN[2] - Fatal Bus Error Interrupt IDINTEN[4] - DU Interrupt IDINTEN[5] - Card Error Summary Interrupt	0
31:10	-	Reserved	

18.6.36 Current Host Descriptor Address Register (DSCADDR)

Table 260. Current Host Descriptor Address Register (DSCADDR, address 0x4000 4094) bit description

Bit	Symbol	Description	Reset value
31:0	HDA	Host Descriptor Address Pointer. Cleared on reset. Pointer updated by IDMAC during operation. This register points to the start address of the current descriptor read by the IDMAC.	0

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18.6.37 Current Buffer Descriptor Address Register (BUFADDR)

Table 261. Current Buffer Descriptor Address Register (BUFADDR, address 0x4000 4098) bit description

Bit	Symbol	Description	Reset value
31:0	HBA	Host Buffer Address Pointer. Cleared on Reset. Pointer updated by IDMAC during operation. This register points to the current Data Buffer Address being accessed by the IDMAC.	0

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19.1 How to read this chapter

The EMC is available on all LPC18xx parts.

The reset value of the EMCSTATICWAITRD0 register varies with the part revision:

- LPC1850/30/20/10 Rev ‘A’: Reset value of the EMCSTATICWAITRD0 register is 0x0000 000E.
- LPC1850/30/20/10 Rev ‘-’: Reset value of the EMCSTATICWAITRD0 register is 0x0000 0007.

For LPC1850/30/20/10 Rev ‘A’ only: The EMC supports a CCLK clock which is half of the frequency of the BASE_M3_CLK. The EMC divided clock must be configured for half-frequency clock operation in both the CREG6 register (Table 37) and the CCU1 CLK_EMCDIV_CFG register (Table 84).

19.2 Basic configuration

The External Memory Controller is configured as follows:

- See Table 262 for clocking and power control.
- If the EMC CCLK is using the divided clock, the CLK_M3_EMC_DIV branch clock must be configured for half-frequency clock operation in both the CREG6 register (Table 37) and the CCU1 CLK_EMCDIV_CFG register (Table 84).
- The EMC is reset by the EMC_RST (reset # 21).
- Delay value for address, data, and command lines can be programmed through registers in the SCU block. (See Section 19.4.4 to Section 19.4.12.)

Table 262. EMC clocking and power control

	Base clock	Branch clock	Maximum frequency	Notes
EMC registers	BASE_M3_CLK	CLK_M3_EMC	120 MHz	-
EMC CCLK	BASE_M3_CLK	CLK_M3_EMC_DIV	120 MHz	This is the CCLK clock for the EMC timing.

19.3 Features

- Dynamic chip selects each support up to 256 MB of data.
- Dynamic memory interface support including Single Data Rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and NOR Flash, with or without asynchronous page mode.
- Low transaction latency.

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- Read and write buffers to reduce latency and to improve performance.
- 8-bit, 16-bit, and 32-bit wide static memory support.
- 16-bit and 32-bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read
  - Programmable wait states
  - Bus turnaround delay
  - Output enable and write enable delays
  - Extended wait
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2 kbit, 4 kbit, and 8 kbit row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.
- Programmable delay elements allow fine-tuning EMC timing.

Remark: Synchronous static memory devices (synchronous burst mode) are not supported.

19.4 General description

The LPC18xx External Memory Controller (EMC) is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM and Flash, as well as dynamic memories such as Single Data Rate SDRAM. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

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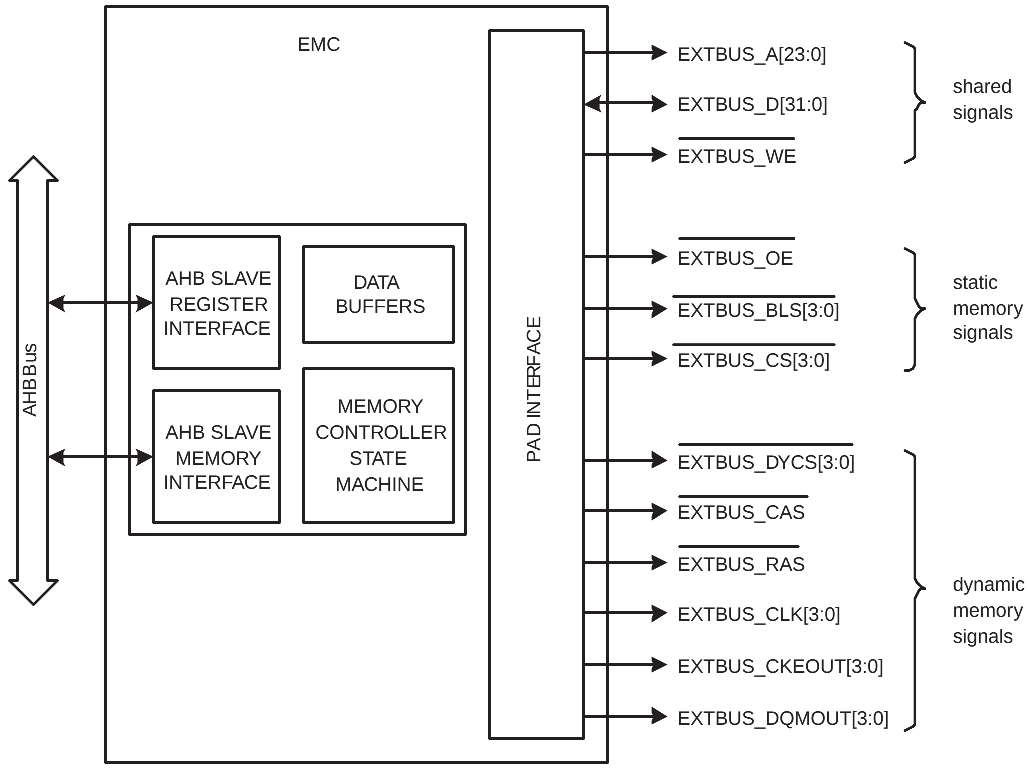


Fig 29. EMC block diagram

19.5 Memory bank select

Eight independently-configurable memory chip selects are supported:

- Pins EMC_CS3 to EMC_CS0 are used to select static memory devices.
- Pins EMC_DYCS3 to EMC_DYCS0 are used to select dynamic memory devices.

Static memory chip select ranges are each 16 Megabytes in size, while dynamic memory chip selects cover a range of 256 megabytes each. Table 263 shows the address ranges of the chip selects.

Table 263. Memory bank selection

Chip select pin	Address range	Memory type	Size of range
EMC_CS0	0x1C00 0000 - 0x1CFF FFFF	Static	16 MB
EMC_CS1	0x1D00 0000 - 01DFF FFFF	Static	16 MB
EMC_CS2	0x1E00 0000 - 0x1EFF FFFF	Static	16 MB
EMC_CS3	0x1F00 0000 - 0x1FFF FFFF	Static	16 MB
EMC_DYCS0	0x2800 0000 - 0x2FFF FFFF	Dynamic	128 MB
EMC_DYCS1	0x3000 0000 - 0x3FFF FFFF	Dynamic	256 MB
EMC_DYCS2	0x6000 0000 - 0x6FFF FFFF	Dynamic	256 MB
EMC_DYCS3	0x7000 0000 - 0x7FFF FFFF	Dynamic	256 MB

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19.6 Pin description

Table 264. EMC pin description

Function pinned out	Direction	Description
EMC_A[22:0]	O	Address bus
EMC_D[31:0]	I/O	Data bus
EMC_BLS[3:0]	O	Byte lane select
EMC_CS[3:0]	O	Static RAM memory bank select
EMC_OE	O	Output enable
EMC_WE	O	Write enable
EMC_CKEOUT[3:0]	O	SDRAM clock enable signals
EMC_CLK[3:0]	O	SDRAM clock signals
EMC_DQMOUT[3:0]	O	Data mask output to SDRAM memory banks
EMC_DYCS[3:0]	O	SDRAM memory bank select
EMC_CAS	O	Column address strobe
EMC_RAS	O	Row address strobe

19.7 Register description

This chapter describes the EMC registers and provides details required when programming the microcontroller. The EMC registers are shown in Table 265.
Reset value reflects the data stored in used bits only. It does not include the content of reserved bits.

Table 265. Register overview: External memory controller (base address 0x4000 5000)

Name	Access	Address offset	Description	Reset value
CONTROL	R/W	0x000	Controls operation of the memory controller.	0x0000 0003[1]
STATUS	RO	0x004	Provides EMC status information.	0x0000 0005
CONFIG	R/W	0x008	Configures operation of the memory controller.	0x0
-	-	0x00C - 0x01C	Reserved.	-
DYNAMICCONTROL	R/W	0x020	Controls dynamic memory operation.	0x0000 0006
DYNAMICREFRESH	R/W	0x024	Configures dynamic memory refresh operation.	0x0
DYNAMICREADCONFIG	R/W	0x028	Configures the dynamic memory read strategy.	0x0
-	-	0x02C	Reserved.	-
DYNAMICRP	R/W	0x030	Selects the precharge command period.	0x0000 000F
DYNAMICRAS	R/W	0x034	Selects the active to precharge command period.	0x0000 000F
DYNAMICSREX	R/W	0x038	Selects the self-refresh exit time.	0x0000 000F
DYNAMICAPR	R/W	0x03C	Selects the last-data-out to active command time.	0x0000 000F
DYNAMICDAL	R/W	0x040	Selects the data-in to active command time.	0x0000 000F
DYNAMICWR	R/W	0x044	Selects the write recovery time.	0x0000 000F
DYNAMICRC	R/W	0x048	Selects the active to active command period.	0x0000 001F
DYNAMICRFC	R/W	0x04C	Selects the auto-refresh period.	0x0000 001F

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Table 265. Register overview: External memory controller (base address 0x4000 5000) *…continued*

Name	Access	Address offset	Description	Reset value
DYNAMICXSR	R/W	0x050	Selects the exit self-refresh to active command time.	0x0000 001F
DYNAMICRRD	R/W	0x054	Selects the active bank A to active bank B latency.	0x0000 000F
DYNAMICMRD	R/W	0x058	Selects the load mode register to active command time.	0x0000 000F
-	R/W	0x05C - 0x07C	Reserved.	-
STATICEXTENDEDWAIT	R/W	0x080	Selects time for long static memory read and write transfers.	0x0
-	R/W	-	Reserved.	-
DYNAMICCONFIG0	R/W	0x100	Selects the configuration information for dynamic memory chip select 0.	0x0
DYNAMICRASCAS0	R/W	0x104	Selects the RAS and CAS latencies for dynamic memory chip select 0.	0x0000 0303
-		0x108 - 0x11C	Reserved.	-
DYNAMICCONFIG1	R/W	0x120	Selects the configuration information for dynamic memory chip select 1.	0x0
DYNAMICRASCAS1	R/W	0x124	Selects the RAS and CAS latencies for dynamic memory chip select 1.	0x0000 0303
-	-	0x128 - 0x13C	Reserved.	-
DYNAMICCONFIG2	R/W	0x140	Selects the configuration information for dynamic memory chip select 2.	0x0
DYNAMICRASCAS2	R/W	0x144	Selects the RAS and CAS latencies for dynamic memory chip select 2.	0x0000 0303
-	-	0x148 - 0x15C	Reserved.	-
DYNAMICCONFIG3	R/W	0x160	Selects the configuration information for dynamic memory chip select 3.	0x0
DYNAMICRASCAS3	R/W	0x164	Selects the RAS and CAS latencies for dynamic memory chip select 3.	0x0000 0303
-	-	0x168 - 0x1FC	Reserved.	-
STATICCONFIG0	R/W	0x200	Selects the memory configuration for static chip select 0.	0x0
STATICWAITWEN0	R/W	0x204	Selects the delay from chip select 0 to write enable.	0x0
STATICWAITOEN0	R/W	0x208	Selects the delay from chip select 0 or address change, whichever is later, to output enable.	0x0
STATICWAITRD0	R/W	0x20C	Selects the delay from chip select 0 to a read access.	0x0000 0007
STATICWAITPAGE0	R/W	0x210	Selects the delay for asynchronous page mode sequential accesses for chip select 0.	0x0000 001F
STATICWAITWR0	R/W	0x214	Selects the delay from chip select 0 to a write access.	0x0000 001F
STATICWAITTURN0	R/W	0x218	Selects the number of bus turnaround cycles for chip select 0.	0x0000 000F
STATICCONFIG1	R/W	0x220	Selects the memory configuration for static chip select 1.	0x0
STATICWAITWEN1	R/W	0x224	Selects the delay from chip select 1 to write enable.	0x0

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Table 265. Register overview: External memory controller (base address 0x4000 5000) *…continued*

Name	Access	Address offset	Description	Reset value
STATICWAITOEN1	R/W	0x228	Selects the delay from chip select 1 or address change, whichever is later, to output enable.	0x0
STATICWAITRD1	R/W	0x22C	Selects the delay from chip select 1 to a read access.	0x0000 001F
STATICWAITPAGE1	R/W	0x230	Selects the delay for asynchronous page mode sequential accesses for chip select 1.	0x0000 001F
STATICWAITWR1	R/W	0x234	Selects the delay from chip select 1 to a write access.	0x0000 001F
STATICWAITTURN1	R/W	0x238	Selects the number of bus turnaround cycles for chip select 1.	0x0000 000F
-	-	0x23C	Reserved.	-
STATICCONFIG2	R/W	0x240	Selects the memory configuration for static chip select 2.	0x0
STATICWAITWEN2	R/W	0x244	Selects the delay from chip select 2 to write enable.	0x0
STATICWAITOEN2	R/W	0x248	Selects the delay from chip select 2 or address change, whichever is later, to output enable.	0x0
STATICWAITRD2	R/W	0x24C	Selects the delay from chip select 2 to a read access.	0x0000 001F
STATICWAITPAGE2	R/W	0x250	Selects the delay for asynchronous page mode sequential accesses for chip select 2.	0x0000 001F
STATICWAITWR2	R/W	0x254	Selects the delay from chip select 2 to a write access.	0x0000 001F
STATICWAITTURN2	R/W	0x258	Selects the number of bus turnaround cycles for chip select 2.	0x0000 000F
-	-	0x25C	Reserved.	-
STATICCONFIG3	R/W	0x260	Selects the memory configuration for static chip select 3.	0x0
STATICWAITWEN3	R/W	0x264	Selects the delay from chip select 3 to write enable.	0x0
STATICWAITOEN3	R/W	0x268	Selects the delay from chip select 3 or address change, whichever is later, to output enable.	0x0
STATICWAITRD3	R/W	0x26C	Selects the delay from chip select 3 to a read access.	0x0000 001F
STATICWAITPAGE3	R/W	0x270	Selects the delay for asynchronous page mode sequential accesses for chip select 3.	0x0000 001F
STATICWAITWR3	R/W	0x274	Selects the delay from chip select 3 to a write access.	0x0000 001F
STATICWAITTURN3	R/W	0x278	Selects the number of bus turnaround cycles for chip select 3.	0x0000 000F

[1] The reset value after warm reset for the CONTROL register is 0x0000 0001.

19.7.1 EMC Control register

The Control register is a read/write register that controls operation of the memory controller. The control bits can be altered during normal operation.

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Table 266. EMC Control register (CONTROL - address 0x4000 5000) bit description

Bit	Symbol	Value	Description	Reset value
0	E		EMC Enable. Indicates if the EMC is enabled or disabled.Disabling the EMC reduces power consumption. When the memory controller is disabled the memory is not refreshed. The memory controller is enabled by setting the enable bit, or by reset. This bit must only be modified when the EMC is in idle state.[1]	1
		0	Disabled	
		1	Enabled (POR and warm reset value).	
1	M		Address mirror. Indicates normal or reset memory map. On POR, CS1 is mirrored to both CS0 and DYCS0 memory areas. Clearing the M bit enables CS0 and DYCS0 memory to be accessed.	1
		0	Normal memory map.	
		1	Reset memory map. Static memory CS1 is mirrored onto CS0 and DYCS0 (POR reset value).	
2	L		Low-power mode. Indicates normal, or low-power mode. Entering low-power mode reduces memory controller power consumption. Dynamic memory is refreshed as necessary. The memory controller returns to normal functional mode by clearing the low-power mode bit (L), or by POR. This bit must only be modified when the EMC is in idle state.[1]	0
		0	Normal mode (warm reset value).	
		1	Low-power mode.	
31:3	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] The external memory cannot be accessed in low-power or disabled state. If a memory access is performed an AHB error response is generated. The EMC registers can be programmed in low-power and/or disabled state.

19.7.2 EMC Status register

The read-only Status register provides EMC status information.

Table 267. EMC Status register (STATUS - address 0x4000 5008) bit description

Bit	Symbol	Value	Description	Reset value
0	B		Busy. This bit is used to ensure that the memory controller enters the low-power or disabled mode cleanly by determining if the memory controller is busy or not:	1
		0	EMC is idle (warm reset value).	
		1	EMC is busy performing memory transactions, commands, auto-refresh cycles, or is in self-refresh mode (POR reset value).	
1	S		Write buffer status. This bit enables the EMC to enter low-power mode or disabled mode cleanly:	0
		0	Write buffers empty (POR reset value)	
		1	Write buffers contain data.	

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Table 267. EMC Status register (STATUS - address 0x4000 5008) bit description

Bit	Symbol	Value	Description	Reset value
2	SA		Self-refresh acknowledge. This bit indicates the operating mode of the EMC:	1
		0	Normal mode	
		1	Self-refresh mode (POR reset value).	
31:3	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.3 EMC Configuration register

The Config register configures the operation of the memory controller. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This register is accessed with one wait state.

Table 268. EMC Configuration register (CONFIG - address 0x4000 5008) bit description

Bit	Symbol	Value	Description	Reset value
0	EM		Endian mode.	0
		0	Little-endian mode (POR reset value).	
		1	Big-endian mode.	
			On power-on reset, the value of the endian bit is 0. All data must be flushed in the EMC before switching between little-endian and big-endian modes.	
7:1	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
8	CR		Clock Ratio. CCLK: CLKOUT[1:0] ratio:	0
		0	1:1 (POR reset value)	
		1	1:2	
			This bit must contain 0 for proper operation of the EMC.	
31:9	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.4 Dynamic Memory Control register

The DynamicControl register controls dynamic memory operation. The control bits can be altered during normal operation.

Table 269. Dynamic Control register (DYNAMICCONTROL - address 0x4000 5020) bit description

Bit	Symbol	Value	Description	Reset value
0	CE		Dynamic memory clock enable.	0
		0	Clock enable of idle devices are deasserted to save power (POR reset value).	
		1	All clock enables are driven HIGH continuously.[1]	

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Table 269. Dynamic Control register (DYNAMICCONTROL - address 0x4000 5020) bit description

Bit	Symbol	Value	Description	Reset value
1	CS		Dynamic memory clock control. When clock control is LOW the output clock CLKOUT is stopped when there are no SDRAM transactions. The clock is also stopped during self-refresh mode.	1
		0	CLKOUT stops when all SDRAMs are idle and during self-refresh mode.	
		1	CLKOUT runs continuously (POR reset value).	
2	SR		Self-refresh request, EMCSREFREQ. By writing 1 to this bit self-refresh can be entered under software control. Writing 0 to this bit returns the EMC to normal mode. The self-refresh acknowledge bit in the Status register must be polled to discover the current operating mode of the EMC.[2]	1
		0	Normal mode.	
		1	Enter self-refresh mode (POR reset value).	
4:3	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
5	MMC		Memory clock control.	0
		0	CLKOUT enabled (POR reset value).	
		1	CLKOUT disabled.[3]	
6	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
8:7	I		SDRAM initialization.	00
		0x0	Issue SDRAM NORMAL operation command (POR reset value).	
		0x1	Issue SDRAM MODE command.	
		0x2	Issue SDRAM PALL (precharge all) command.	
		0x3	Issue SDRAM NOP (no operation) command)	
12:9	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
13	DP		Low-power SDRAM deep-sleep mode.	0
		0	Normal operation (POR reset value).	
		1	Enter Deep-sleep mode.	
31:14	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] Clock enable must be HIGH during SDRAM initialization.

[2] The memory controller exits from power-on reset with the self-refresh bit HIGH. To enter normal functional mode set this bit LOW.

[3] Disabling CLKOUT can be performed if there are no SDRAM memory transactions. When enabled this bit can be used in conjunction with the dynamic memory clock control (CS) field.

Remark: Deep-sleep mode can be entered by setting the deep-sleep mode (DP) bit, the dynamic memory clock enable bit (CE), and the dynamic clock control bit (CS) to one. The device is then put into a low-power mode where the device is powered down and no longer refreshed. All data in the memory is lost.

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19.7.5 Dynamic Memory Refresh Timer register

The DynamicRefresh register configures dynamic memory operation. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. However, these control bits can, if necessary, be altered during normal operation. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

Table 270. Dynamic Memory Refresh Timer register (DYNAMICREFRESH - address 0x4000 5024) bit description

Bit	Symbol	Description	Reset value
10:0	REFRESH	Refresh timer. Indicates the multiple of 16 CCLKs between SDRAM refresh cycles. 0x0 = Refresh disabled (POR reset value). 0x1 - 0x7FF = n x16 = 16n CCLKs between SDRAM refresh cycles. For example: 0x1 = 1 x 16 = 16 CCLKs between SDRAM refresh cycles. 0x8 = 8 x 16 = 128 CCLKs between SDRAM refresh cycles	0
31:11	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

For example, for the refresh period of 16 μs, and a CCLK frequency of 50 MHz, the following value must be programmed into this register:

$(16 \times 10^{-6} \times 50 \times 10^{6}) / 16 = 50$ or 0x32

If auto-refresh through warm reset is requested (by setting the EMC_Reset_Disable bit), the timing of auto-refresh must be adjusted to allow a sufficient refresh rate when the clock rate is reduced during the wake-up period of a reset cycle. During this period, the EMC (and all other portions of the chip that are being clocked) run from the IRC oscillator at 12 MHz. The IRC oscillator frequency must be used as the CCLK rate for refresh calculations if auto-refresh through warm reset is requested.

Note: The refresh cycles are evenly distributed. However, there might be slight variations when the auto-refresh command is issued depending on the status of the memory controller.

19.7.6 Dynamic Memory Read Configuration register

The DynamicReadConfig register configures the dynamic memory read strategy. This register must only be modified during system initialization. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

Important: It should be highlighted that the default clock delay methodology requires the output clock to be delayed **externally** to the chip to avoid hold time issue for the SDRAM. In most application boards, there will be no such external delay circuit and the application should write correct value to the DynamicReadConfig register to use Command Delay Strategy. The Clock Delay Strategy is the default setting on reset!

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See Section 19.4.4 to Section 19.4.12 for programming delay value for address, data, and command lines.

Table 271. Dynamic Memory Read Configuration register (DYNAMICREADCONFIG - address 0x4000 5028) bit description

Bit	Symbol	Value	Description	Reset value
1:0	RD		Read data strategy.	0x0
		0x0	Clock out delayed strategy, using CLKOUT (command not delayed, clock out delayed). POR reset value.	
		0x1	Command delayed strategy, using CCLKDELAY (command delayed, clock out not delayed).	
		0x2	Command delayed strategy plus one clock cycle, using CCLKDELAY (command delayed, clock out not delayed).	
		0x3	Command delayed strategy plus two clock cycles, using CCLKDELAY (command delayed, clock out not delayed).	
31:2	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.7 Dynamic Memory Precharge Command Period register

The DynamicTRP register enables you to program the precharge command period, tRP. This register must only be modified during system initialization. This value is normally found in SDRAM data sheets as tRP. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

Table 272. Dynamic Memory Precharge Command Period register (DYNAMICRP - address 0x4000 5030) bit description

Bit	Symbol	Description	Reset value
3:0	tRP	Precharge command period. 0x0 - 0xE = n + 1 clock cycles. The delay is in CCLK cycles. 0xF = 16 clock cycles (POR reset value).	0xF
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.8 Dynamic Memory Active to Precharge Command Period register

The DynamicTRAS register enables you to program the active to precharge command period, tRAS. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This value is normally found in SDRAM data sheets as tRAS. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

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Table 273. Dynamic Memory Active to Precharge Command Period register (DYNAMICRAS - address 0x4000 5034) bit description

Bit	Symbol	Description	Reset value
3:0	tRAS	Active to precharge command period. 0x0 - 0xE = n + 1 clock cycles. The delay is in CCLK cycles. 0xF = 16 clock cycles (POR reset value).	0xF
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.9 Dynamic Memory Self Refresh Exit Time register

The DynamicTSREX register enables you to program the self-refresh exit time, tSREX. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This value is normally found in SDRAM data sheets as tSREX, for devices without this parameter you use the same value as tXSR. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

Table 274. Dynamic Memory Self Refresh Exit Time register (DYNAMICSREX - address 0x4000 5038) bit description

Bit	Symbol	Description	Reset value
3:0	tSREX	Self-refresh exit time. 0x0 - 0xE = n + 1 clock cycles. The delay is in CCLK cycles. 0xF = 16 clock cycles (POR reset value).	0xF
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.10 Dynamic Memory Last Data Out to Active Time register

The DynamicTAPR register enables you to program the last-data-out to active command time, tAPR. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This value is normally found in SDRAM data sheets as tAPR. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

Table 275. Dynamic Memory Last Data Out to Active Time register (DYNAMICAPR - address 0x4000 503C) bit description

Bit	Symbol	Description	Reset value
3:0	tAPR	Last-data-out to active command time. 0x0 - 0xE = n + 1 clock cycles. The delay is in CCLK cycles. 0xF = 16 clock cycles (POR reset value).	0xF
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

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19.7.11 Dynamic Memory Data In to Active Command Time register

The DynamicTDAL register enables you to program the data-in to active command time, tDAL. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This value is normally found in SDRAM data sheets as tDAL, or tAPW. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

Table 276. Dynamic Memory Data In to Active Command Time register (DYNAMICDAL - address 0x4000 5040) bit description

Bit	Symbol	Description	Reset value
3:0	tDAL	Data-in to active command. 0x0 - 0xE = n clock cycles. The delay is in CCLK cycles. 0xF = 15 clock cycles (POR reset value).	0xF
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.12 Dynamic Memory Write Recovery Time register

The DynamicTWR register enables you to program the write recovery time, tWR. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This value is normally found in SDRAM data sheets as tWR, tDPL, tRWL, or tRDL. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

Table 277. Dynamic Memory Write Recovery Time register (DYNAMICWR - address 0x4000 5044) bit description

Bit	Symbol	Description	Reset value
3:0	tWR	Write recovery time. 0x0 - 0xE = n + 1 clock cycles. The delay is in CCLK cycles. 0xF = 16 clock cycles (POR reset value).	0xF
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.13 Dynamic Memory Active to Active Command Period register

The DynamicTRC register enables you to program the active to active command period, tRC. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This value is normally found in SDRAM data sheets as tRC. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

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Table 278. Dynamic Memory Active to Active Command Period register (DYNAMICRC - address 0x4000 5048) bit description

Bit	Symbol	Description	Reset value
4:0	tRC	Active to active command period. 0x0 - 0x1E = n + 1 clock cycles. The delay is in CCLK cycles. 0x1F = 32 clock cycles (POR reset value).	0x1F
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.14 Dynamic Memory Auto-refresh Period register

The DynamicTRFC register enables you to program the auto-refresh period, and auto-refresh to active command period, tRFC. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This value is normally found in SDRAM data sheets as tRFC, or sometimes as tRC. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

Table 279. Dynamic Memory Auto Refresh Period register (DYNAMICRFC - address 0x4000 504C) bit description

Bit	Symbol	Description	Reset value
4:0	tRFC	Auto-refresh period and auto-refresh to active command period. 0x0 - 0x1E = n + 1 clock cycles. The delay is in CCLK cycles. 0x1F = 32 clock cycles (POR reset value).	0x1F
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.15 Dynamic Memory Exit Self Refresh register

The DynamicTXSR register enables you to program the exit self-refresh to active command time, tXSR. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This value is normally found in SDRAM data sheets as tXSR. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

Table 280. Dynamic Memory Exit Self Refresh register (DYNAMICXSR - address 0x4000 5050) bit description

Bit	Symbol	Description	Reset value
4:0	tXSR	Exit self-refresh to active command time. 0x0 - 0x1E = n + 1 clock cycles. The delay is in CCLK cycles. 0x1F = 32 clock cycles (POR reset value).	0x1F
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

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19.7.16 Dynamic Memory Active Bank A to Active Bank B Time register

The DynamicTRRD register enables you to program the active bank A to active bank B latency, tRRD. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This value is normally found in SDRAM data sheets as tRRD. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

Table 281. Dynamic Memory Active Bank A to Active Bank B Time register (DYNAMICRRD - address 0x4000 5054) bit description

Bit	Symbol	Description	Reset value
3:0	tRRD	Active bank A to active bank B latency 0x0 - 0xE = n + 1 clock cycles. The delay is in CCLK cycles. 0xF = 16 clock cycles (POR reset value).	0xF
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.17 Dynamic Memory Load Mode register to Active Command Time

The DynamicTMRD register enables you to program the load mode register to active command time, tMRD. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This value is normally found in SDRAM data sheets as tMRD, or tRSA. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

Table 282. Dynamic Memory Load Mode register to Active Command Time (DYNAMICMRD - address 0x4000 5058) bit description

Bit	Symbol	Description	Reset value
3:0	tMRD	Load mode register to active command time. 0x0 - 0xE = n + 1 clock cycles. The delay is in CCLK cycles. 0xF = 16 clock cycles (POR reset value).	0xF
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.18 Static Memory Extended Wait register

ExtendedWait (EW) bit in the StaticConfig register is set. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. However, if necessary, these control bits can be altered during normal operation. This register is accessed with one wait state.

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Table 283. Static Memory Extended Wait register (STATICEXTENDEDWAIT - address 0x4000 5080) bit description

Bit	Symbol	Description	Reset value
9:0	EXTENDEDWAIT	Extended wait time out. 16 clock cycles (POR reset value). The delay is in CCLK cycles. 0x0 = 16 clock cycles. 0x1 - 0x3FF = (n+1) x16 clock cycles.	0x0
31:10	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

For example, for a static memory read/write transfer time of 16 μs, and a CCLK frequency of 50 MHz, the following value must be programmed into this register:
$(16 \times 10^{-6} \times 50 \times 10^{6}) / 16 - 1 = 49$

19.7.19 Dynamic Memory Configuration registers

The DynamicConfig registers enable you to program the configuration information for the relevant dynamic memory chip select. These registers are normally only modified during system initialization. These registers are accessed with one wait state.

Table 284. Dynamic Memory Configuration registers (DYNAMICCONFIG, address 0x4000 5100 (DYNAMICCONFIG0), 0x4000 5120 (DYNAMICCONFIG1), 0x4000 5140 (DYNAMICCONFIG2), 0x4000 5160 (DYNAMICCONFIG3)) bit description

Bit	Symbol	Value	Description	Reset value
2:0	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
4:3	MD		Memory device.	00
		0x0	SDRAM (POR reset value).	
		0x1	Low-power SDRAM.	
		0x2	Reserved.	
		0x3	Reserved.	
6:5	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
12:7	AM0		Address mapping. See Table 285. 000000 = reset value.[1]	0
13	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
14	AM1		Address mapping See Table 285. 0 = reset value.	0
18:15	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
19	B		Buffer enable.	
		0	Buffer disabled for accesses to this chip select (POR reset value).	
		1	Buffer enabled for accesses to this chip select. After configuration of the dynamic memory, the buffer must be enabled for normal operation. [2]	

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Table 284. Dynamic Memory Configuration registers (DYNAMICCONFIG, address 0x4000 5100 (DYNAMICCONFIG0), 0x4000 5120 (DYNAMICCONFIG1), 0x4000 5140 (DYNAMICCONFIG2), 0x4000 5160 (DYNAMICCONFIG3)) bit description

Bit	Symbol	Value	Description	Reset value
20	P		Write protect.	0
		0	Writes not protected (POR reset value).	
		1	Writes protected.	
31:21	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] The SDRAM column and row width and number of banks are computed automatically from the address mapping.

[2] The buffers must be disabled during SDRAM and SyncFlash initialization. They must also be disabled when performing SyncFlash commands. The buffers must be enabled during normal operation.

Address mappings that are not shown in Table 285 are reserved.

Table 285. Address mapping

14	12	11:9	8:7	Description
16 bit external bus high-performance address mapping (Row, Bank, Column)				
0	0	000	00	16 Mb (2Mx8), 2 banks, row length = 11, column length = 9
0	0	000	01	16 Mb (1Mx16), 2 banks, row length = 11, column length = 8
0	0	001	00	64 Mb (8Mx8), 4 banks, row length = 12, column length = 9
0	0	001	01	64 Mb (4Mx16), 4 banks, row length = 12, column length = 8
0	0	010	00	128 Mb (16Mx8), 4 banks, row length = 12, column length = 10
0	0	010	01	128 Mb (8Mx16), 4 banks, row length = 12, column length = 9
0	0	011	00	256 Mb (32Mx8), 4 banks, row length = 13, column length = 10
0	0	011	01	256 Mb (16Mx16), 4 banks, row length = 13, column length = 9
0	0	100	00	512 Mb (64Mx8), 4 banks, row length = 13, column length = 11
0	0	100	01	512 Mb (32Mx16), 4 banks, row length = 13, column length = 10
16 bit external bus low-power SDRAM address mapping (Bank, Row, Column)				
0	1	000	00	16 Mb (2Mx8), 2 banks, row length = 11, column length = 9
0	1	000	01	16 Mb (1Mx16), 2 banks, row length = 11, column length = 8
0	1	001	00	64 Mb (8Mx8), 4 banks, row length = 12, column length = 9
0	1	001	01	64 Mb (4Mx16), 4 banks, row length = 12, column length = 8
0	1	010	00	128 Mb (16Mx8), 4 banks, row length = 12, column length = 10
0	1	010	01	128 Mb (8Mx16), 4 banks, row length = 12, column length = 9
0	1	011	00	256 Mb (32Mx8), 4 banks, row length = 13, column length = 10
0	1	011	01	256 Mb (16Mx16), 4 banks, row length = 13, column length = 9
0	1	100	00	512 Mb (64Mx8), 4 banks, row length = 13, column length = 11
0	1	100	01	512 Mb (32Mx16), 4 banks, row length = 13, column length = 10
32 bit external bus high-performance address mapping (Row, Bank, Column)				
1	0	000	00	16 Mb (2Mx8), 2 banks, row length = 11, column length = 9
1	0	000	01	16 Mb (1Mx16), 2 banks, row length = 11, column length = 8
1	0	001	00	64 Mb (8Mx8), 4 banks, row length = 12, column length = 9

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Table 285. Address mapping

14	12	11:9	8:7	Description
1	0	001	01	64 Mb (4Mx16), 4 banks, row length = 12, column length = 8
1	0	001	10	64 Mb (2Mx32), 4 banks, row length = 11, column length = 8
1	0	010	00	128 Mb (16Mx8), 4 banks, row length = 12, column length = 10
1	0	010	01	128 Mb (8Mx16), 4 banks, row length = 12, column length = 9
1	0	010	10	128 Mb (4Mx32), 4 banks, row length = 12, column length = 8
1	0	011	00	256 Mb (32Mx8), 4 banks, row length = 13, column length = 10
1	0	011	01	256 Mb (16Mx16), 4 banks, row length = 13, column length = 9
1	0	011	10	256 Mb (8Mx32), 4 banks, row length = 13, column length = 8
1	0	100	00	512 Mb (64Mx8), 4 banks, row length = 13, column length = 11
1	0	100	01	512 Mb (32Mx16), 4 banks, row length = 13, column length = 10
32 bit external bus low-power SDRAM address mapping (Bank, Row, Column)				
1	1	000	00	16 Mb (2Mx8), 2 banks, row length = 11, column length = 9
1	1	000	01	16 Mb (1Mx16), 2 banks, row length = 11, column length = 8
1	1	001	00	64 Mb (8Mx8), 4 banks, row length = 12, column length = 9
1	1	001	01	64 Mb (4Mx16), 4 banks, row length = 12, column length = 8
1	1	001	10	64 Mb (2Mx32), 4 banks, row length = 11, column length = 8
1	1	010	00	128 Mb (16Mx8), 4 banks, row length = 12, column length = 10
1	1	010	01	128 Mb (8Mx16), 4 banks, row length = 12, column length = 9
1	1	010	10	128 Mb (4Mx32), 4 banks, row length = 12, column length = 8
1	1	011	00	256 Mb (32Mx8), 4 banks, row length = 13, column length = 10
1	1	011	01	256 Mb (16Mx16), 4 banks, row length = 13, column length = 9
1	1	011	10	256 Mb (8Mx32), 4 banks, row length = 13, column length = 8
1	1	100	00	512 Mb (64Mx8), 4 banks, row length = 13, column length = 11
1	1	100	01	512 Mb (32Mx16), 4 banks, row length = 13, column length = 10

A chip select can be connected to a single memory device, in this case the chip select data bus width is the same as the device width. Alternatively the chip select can be connected to a number of external devices. In this case the chip select data bus width is the sum of the memory device data bus widths.

For example, for a chip select connected to:

- a 32-bit wide memory device, choose a 32-bit wide address mapping.
- a 16-bit wide memory device, choose a 16-bit wide address mapping.
- four x 8-bit wide memory devices, choose a 32-bit wide address mapping.
- two x 8-bit wide memory devices, choose a 16-bit wide address mapping.

The SDRAM bank select pins BA1 and BA0 are connected to address lines A14 and A13, respectively.

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19.7.20 Dynamic Memory RAS & CAS Delay registers

The DynamicRasCas0:3 registers enable you to program the RAS and CAS latencies for the relevant dynamic memory. It is recommended that these registers are modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. These registers are accessed with one wait state.

Note: The values programmed into these registers must be consistent with the values used to initialize the SDRAM memory device.

Table 286. Dynamic Memory RASCAS Delay registers (DYNAMICRASCAS, address 0x4000 5104 (DYNAMICRASCAS0), 0x4000 5124 (DYNAMICRASCAS1), 0x4000 5144 (DYNAMICRASCAS2), 0x4000 5164 (DYNAMICRASCAS3)) bit description

Bit	Symbol	Value	Description	Reset value
1:0	RAS		RAS latency (active to read/write delay).	11
		0x0	Reserved.	
		0x1	One CCLK cycle.	
		0x2	Two CCLK cycles.	
		0x3	Three CCLK cycles (POR reset value).	
7:2	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
9:8	CAS		CAS latency.	11
		0x0	Reserved.	
		0x1	One CCLK cycle.	
		0x2	Two CCLK cycles.	
		0x3	Three CCLK cycles (POR reset value).	
31:10	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.21 Static Memory Configuration registers

The StaticConfig registers configure the static memory configuration. It is recommended that these registers are modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. These registers are accessed with one wait state.

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Table 287. Static Memory Configuration registers (STATICCONFIG, address 0x4000 5200 (STATICCONFIG0), 0x4000 5220 (STATICCONFIG1), 0x4000 5240 (STATICCONFIG2), 0x4000 5260 (STATICCONFIG3)) bit description

Bit	Symbol	Value	Description	Reset value
1:0	MW		Memory width.	0
		0x0	8 bit (POR reset value).	
		0x1	16 bit.	
		0x2	32 bit.	
		0x3	Reserved.	
2	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
3	PM		Page mode. In page mode the EMC can burst up to four external accesses. Therefore devices with asynchronous page mode burst four or higher devices are supported. Asynchronous page mode burst two devices are not supported and must be accessed normally.	0
		0	Disabled (POR reset value).	
		1	Async page mode enabled (page length four).	
5:4	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
6	PC		Chip select polarity. The value of the chip select polarity on power-on reset is 0.	0
		0	Active LOW chip select.	
		1	Active HIGH chip select.	
7	PB		Byte lane state. The byte lane state bit, PB, enables different types of memory to be connected. For byte-wide static memories the BLSn[3:0] signal from the EMC is usually connected to $\overline{WE}$ (write enable). In this case for reads all the BLSn[3:0] bits must be HIGH. This means that the byte lane state (PB) bit must be LOW. 16 bit wide static memory devices usually have the BLSn[3:0] signals connected to the UBn and LBn (upper byte and lower byte) signals in the static memory. In this case a write to a particular byte must assert the appropriate UBn or LBn signal LOW. For reads, all the $\overline{UB}$ and $\overline{LB}$ signals must be asserted LOW so that the bus is driven. In this case the byte lane state (PB) bit must be HIGH. **Remark:** When PB is set to 0, the WE signal is undefined or 0. You must set PB to 1, to use the WE signal.	0
		0	For reads all the bits in BLSn[3:0] are HIGH. For writes the respective active bits in BLSn[3:0] are LOW (POR reset value).	
		1	For reads the respective active bits in BLSn[3:0] are LOW. For writes the respective active bits in BLSn[3:0] are LOW.	

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Table 287. Static Memory Configuration registers (STATICCONFIG, address 0x4000 5200 (STATICCONFIG0), 0x4000 5220 (STATICCONFIG1), 0x4000 5240 (STATICCONFIG2), 0x4000 5260 (STATICCONFIG3)) bit description

Bit	Symbol	Value	Description	Reset value
8	EW		Extended wait. Extended wait (EW) uses the StaticExtendedWait register to time both the read and write transfers rather than the StaticWaitRd and StaticWaitWr registers. This enables much longer transactions.[1]	0
		0	Extended wait disabled (POR reset value).	
		1	Extended wait enabled.	
18:9	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
19	B		Buffer enable[2].	0
		0	Buffer disabled (POR reset value).	
		1	Buffer enabled.	
20	P		Write protect.	0
		0	Writes not protected (POR reset value).	
		1	Write protected.	
31:21	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] Extended wait and page mode cannot be selected simultaneously.

[2] EMC may perform burst read access even when the buffer enable bit is cleared.

19.7.22 Static Memory Write Enable Delay registers

The StaticWaitWen registers enable you to program the delay from the chip select to the write enable. It is recommended that these registers are modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. These registers are accessed with one wait state.

Table 288. Static Memory Write Enable Delay registers (STATICWAITWEN, address 0x4000 5204 (STATICWAITWEN0), 0x4000 5224 (STATICWAITWEN1), 0x4000 5244 (STATICWAITWEN2), 0x4000 5264 (STATICWAITWEN3)) bit description

Bit	Symbol	Description	Reset value
3:0	WAITWEN	Wait write enable. Delay from chip select assertion to write enable. 0x0 = One CCLK cycle delay between assertion of chip select and write enable (POR reset value). 0x1 - 0xF = (n + 1) CCLK cycle delay. The delay is (WAITWEN +1) x tCCLK.	0x0
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

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19.7.23 Static Memory Output Enable Delay registers

The StaticWaitOen registers enable you to program the delay from the chip select or address change, whichever is later, to the output enable. It is recommended that these registers are modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. These registers are accessed with one wait state.

Table 289. Static Memory Output Enable delay registers (STATICWAITOEN, address 0x4000 5208 (STATICWAITOEN0), 0x4000 5228 (STATICWAITOEN1), 0x4000 5248 (STATICWAITOEN2), 0x4000 5268 (STATICWAITOEN3)) bit description

Bit	Symbol	Description	Reset value
3:0	WAITOEN	Wait output enable. Delay from chip select assertion to output enable. 0x0 = No delay (POR reset value). 0x1 - 0xF = n cycle delay. The delay is WAITOEN x tCCLK.	0x0
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.24 Static Memory Read Delay registers

The StaticWaitRd registers enable you to program the delay from the chip select to the read access. It is recommended that these registers are modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. It is not used if the extended wait bit is enabled in the StaticConfig registers. These registers are accessed with one wait state.

Table 290. Static Memory Read Delay registers (STATICWAITRD, address 0x4000 520C (STATICWAITRD0), 0x4000 522C (STATICWAITRD1), 0x4000 524C (STATICWAITRD2), 0x4000 526C (STATICWAITRD3)) bit description

Bit	Symbol	Description	Reset value
4:0	WAITRD	Non-page mode read wait states or asynchronous page mode read first access wait state. Non-page mode read or asynchronous page mode read, first read only: 0x0 - 0x1E = (n + 1) CCLK cycles for read accesses. For non-sequential reads, the wait state time is (WAITRD + 1) x tCCLK. 0x1F = 32 CCLK cycles for read accesses (POR reset value).	0xB [1]
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] The reset value is 0x0B for the STATICWAITRD0 register only.

19.7.25 Static Memory Page Mode Read Delay registers

The StaticWaitPage registers enable you to program the delay for asynchronous page mode sequential accesses. It is recommended that these registers are modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This register is accessed with one wait state.

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Table 291. Static Memory Page Mode Read Delay registers (STATICWAITPAGE, address 0x4000 5210 (STATICWAITPAGE0), 0x4000 5230 (STATICWAITPAGE1), 0x4000 5250 (STATICWAITPAGE2), 0x4000 5270 (STATICWAITPAGE3)) bit description

Bit	Symbol	Description	Reset value
4:0	WAITPAGE	Asynchronous page mode read after the first read wait states. Number of wait states for asynchronous page mode read accesses after the first read: 0x0 - 0x1E = (n+ 1) CCLK cycle read access time. For asynchronous page mode read for sequential reads, the wait state time for page mode accesses after the first read is (WAITPAGE + 1) x tCCLK. 0x1F = 32 CCLK cycle read access time (POR reset value).	0x1F
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.26 Static Memory Write Delay registers

The StaticWaitWr registers enable you to program the delay from the chip select to the write access. It is recommended that these registers are modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode.These registers are not used if the extended wait (EW) bit is enabled in the StaticConfig register. These registers are accessed with one wait state.

Table 292. Static Memory Write Delay registers (STATICWAITWR, address 0x4000 5214 (STATICWAITWR0), 0x4000 5234 (STATICWAITWR1), 0x4000 5254 (STATICWAITWR2), 0x4000 5274 (STATICWAITWR3)) bit description

Bit	Symbol	Description	Reset value
4:0	WAITWR	Write wait states. SRAM wait state time for write accesses after the first read: 0x0 - 0x1E = (n + 2) CCLK cycle write access time. The wait state time for write accesses after the first read is WAITWR (n + 2) x tCCLK. 0x1F = 33 CCLK cycle write access time (POR reset value).	0x1F
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

19.7.27 Static Memory Turn Round Delay registers

The StaticWaitTurn registers enable you to program the number of bus turnaround cycles. It is recommended that these registers are modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. These registers are accessed with one wait state.

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Table 293. Static Memory Turn Round Delay registers (STATICWAITTURN, address 0x4000 5218 (STATICWAITTURN0), 0x4000 5238 (STATICWAITTURN1), 0x4000 5258 (STATICWAITTURN2), 0x4000 5278 (STATICWAITTURN3)) bit description

Bit	Symbol	Description	Reset value
3:0	WAITTURN	Bus turnaround cycles. 0x0 - 0xE = (n + 1) CCLK turnaround cycles. Bus turnaround time is (WAITTURN + 1) x tCCLK. 0xF = 16 CCLK turnaround cycles (POR reset value).	0xF
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

To prevent bus contention on the external memory data bus, the WAITTURN field controls the number of bus turnaround cycles added between static memory read and write accesses. The WAITTURN field also controls the number of turnaround cycles between static memory and dynamic memory accesses.

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19.8 Functional description

Figure 30 shows a block diagram of the EMC.

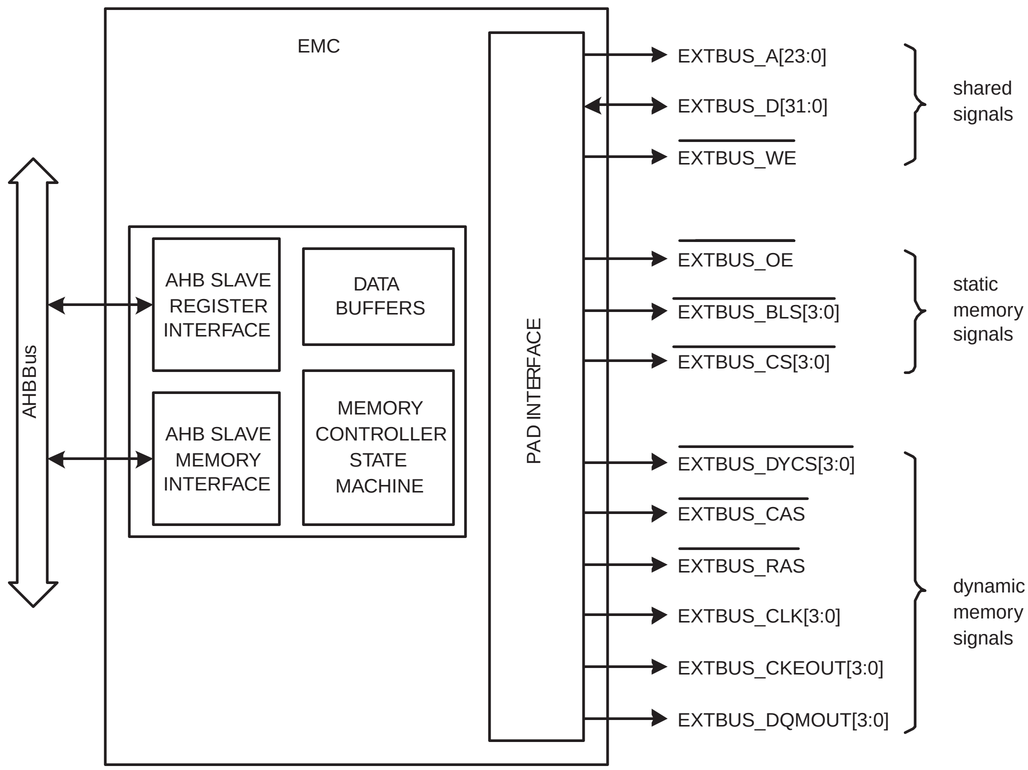


Fig 30. EMC block diagram

The functions of the EMC blocks are described in the following sections:

- AHB slave register interface.
- AHB slave memory interfaces.
- Data buffers.
- Memory controller state machine.
- Pad interface.

Note: For 32 bit wide chip selects data is transferred to and from dynamic memory in SDRAM bursts of four. For 16 bit wide chip selects SDRAM bursts of eight are used.

19.8.1 AHB slave register interface

The AHB slave register interface block enables the registers of the EMC to be programmed. This module also contains most of the registers and performs the majority of the register address decoding.

To eliminate the possibility of endianness problems, all data transfers to and from the registers of the EMC must be 32 bits wide.

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Note: If an access is attempted with a size other than a word (32 bits), it causes an ERROR response to the AHB bus and the transfer is terminated.

19.8.2 AHB slave memory interface

The AHB slave memory interface allows access to external memories.

19.8.2.1 Memory transaction endianness

The endianness of the data transfers to and from the external memories is determined by the Endian mode (N) bit in the Config register.

Note: The memory controller must be idle (see the busy field of the Status Register) before endianness is changed, so that the data is transferred correctly.

19.8.2.2 Memory transaction size

Memory transactions can be 8, 16, or 32 bits wide. Any access attempted with a size greater than a word (32 bits) causes an ERROR response to the AHB bus and the transfer is terminated.

19.8.2.3 Write protected memory areas

Write transactions to write-protected memory areas generate an ERROR response to the AHB bus and the transfer is terminated.

19.8.3 Pad interface

The pad interface block provides the interface to the pads. The pad interface uses one feedback clock per lane, FBCLKIN[3:0], from the CLKOUT[3:0] outputs of the EMC to resynchronize SDRAM read data from the off-chip to on-chip domains.

The EMC dynamic memory requires 2 CLKOUT signals for 16-bit memory and 4 CLKOUT signals for 32-bit memory.

19.8.4 Data buffers

The AHB interface reads and writes via buffers to improve memory bandwidth and reduce transaction latency. The EMC contains four 16-word buffers. The buffers can be used as read buffers, write buffers, or a combination of both. The buffers are allocated automatically.

The buffers must be disabled during SDRAM and SyncFlash initialization. They must also be disabled when performing SyncFlash commands. The buffers must be enabled during normal operation.

The buffers can be enabled or disabled for static memory using the StaticConfig Registers.

19.8.4.1 Write buffers

Write buffers are used to:

- Merge write transactions so that the number of external transactions are minimized.

  Buffer data until the EMC can complete the write transaction, improving AHB write latency.

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Convert all dynamic memory write transactions into quadword bursts on the external memory interface. This enhances transfer efficiency for dynamic memory.

- Reduce external memory traffic. This improves memory bandwidth and reduces power consumption.

Write buffer operation:

- If the buffers are enabled, an AHB write operation writes into the Least Recently Used (LRU) buffer, if empty.

  If the LRU buffer is not empty, the contents of the buffer are flushed to memory to make space for the AHB write data.
- If a buffer contains write data it is marked as dirty, and its contents are written to memory before the buffer can be reallocated.

The write buffers are flushed whenever:

- The memory controller state machine is not busy performing accesses to external memory.

  The memory controller state machine is not busy performing accesses to external memory, and an AHB interface is writing to a different buffer.

Note: For dynamic memory, the smallest buffer flush is a quadword of data. For static memory, the smallest buffer flush is a byte of data.

19.8.4.2 Read buffers

Read buffers are used to:

- Buffer read requests from memory. Future read requests that hit the buffer read the data from the buffer rather than memory, reducing transaction latency.

  Convert all read transactions into quadword bursts on the external memory interface. This enhances transfer efficiency for dynamic memory.
- Reduce external memory traffic. This improves memory bandwidth and reduces power consumption.

Read buffer operation:

- If the buffers are enabled and the read data is contained in one of the buffers, the read data is provided directly from the buffer.
- If the read data is not contained in a buffer, the LRU buffer is selected. If the buffer is dirty (contains write data), the write data is flushed to memory. When an empty buffer is available the read command is posted to the memory.

A buffer filled by performing a read from memory is marked as not-dirty (not containing write data) and its contents are not flushed back to the memory controller unless a subsequent AHB transfer performs a write that hits the buffer.

19.9 Low-power operation

In many systems, the contents of the memory system have to be maintained during low-power sleep modes. The EMC provides a mechanism to place the dynamic memories into self-refresh mode.

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Self-refresh mode can be entered by software by setting the SREFREQ bit in the DynamicControl Register and polling the SREFACK bit in the Status Register.

Any transactions to memory that are generated while the memory controller is in self-refresh mode are rejected and an error response is generated to the AHB bus. Clearing the SREFREQ bit in the DynamicControl Register returns the memory to normal operation. See the memory data sheet for refresh requirements.

Note: The static memory can be accessed as normal when the SDRAM memory is in self-refresh mode.

19.9.1 Low-power SDRAM Deep-sleep Mode

The EMC supports JEDEC low-power SDRAM deep-sleep mode. Deep-sleep mode can be entered by setting the deep-sleep mode (DP) bit, the dynamic memory clock enable bit (CE), and the dynamic clock control bit (CS) in the DynamicControl register. The device is then put into a low-power mode where the device is powered down and no longer refreshed. All data in the memory is lost.

19.9.2 Low-power SDRAM partial array refresh

The EMC supports JEDEC low-power SDRAM partial array refresh. Partial array refresh can be programmed by initializing the SDRAM memory device appropriately. When the memory device is put into self-refresh mode only the memory banks specified are refreshed. The memory banks that are not refreshed lose their data contents.

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19.10 External static memory interface

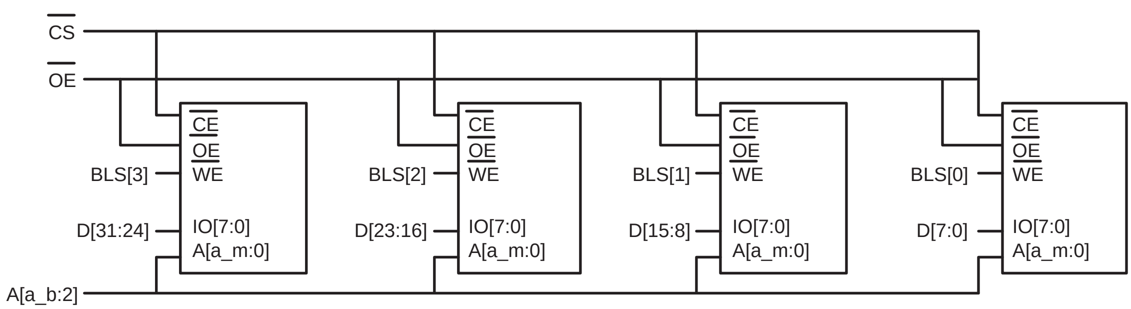
External memory interfacing depends on the bank width (32, 16 or 8 bit selected via MW bits in corresponding StaticConfig register).

If a memory bank is configured to be 32 bits wide, address lines A0 and A1 can be used as non-address lines. If a memory bank is configured to 16 bits wide, A0 is not required. However, 8 bit wide memory banks do require all address lines down to A0. Configuring A1 and/or A0 line(s) to provide address or non-address function is accomplished using the SYSCON registers.

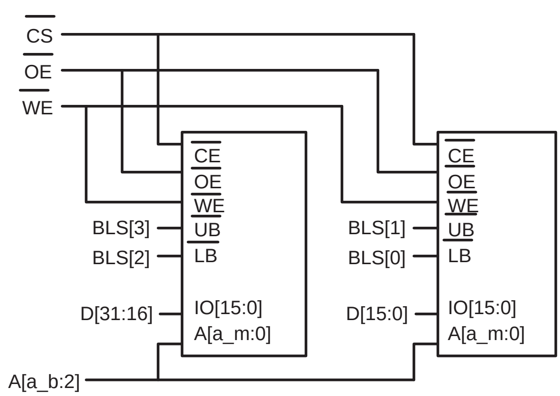
Symbol "a_b" in the following figures refers to the highest order address line in the data bus. Symbol "a_m" refers to the highest order address line of the memory chip used in the external memory interface.

If the external memory is used as external boot memory for flashless devices, refer to Section 3.2 on how to connect the EMC. The memory bank width for memory banks 1 and 2 is determined by the setting of the BOOT pins.

19.10.1 32-bit wide memory bank connection



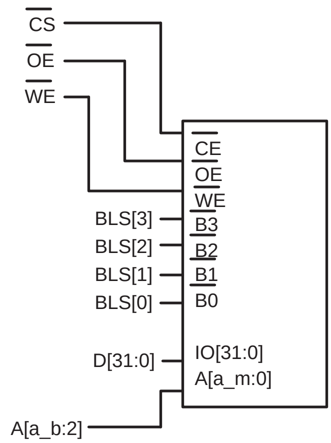
a. 32 bit wide memory bank interfaced to four 8 bit memory chips



b. 32 bit wide memory bank interfaced to two 16 bit memory chips

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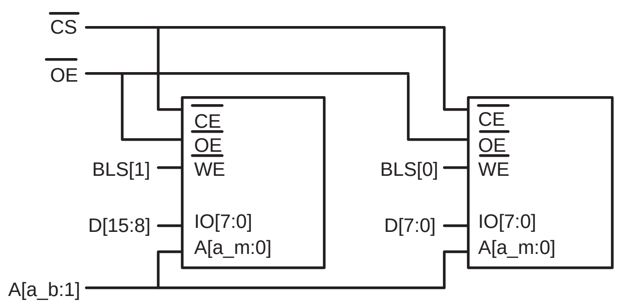
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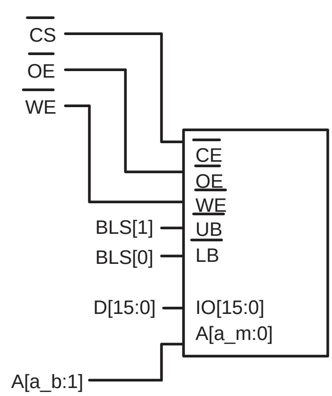
c. 32 bit wide memory bank interfaced to one 8 bit memory chip

Fig 31. 32 bit bank external memory interfaces (bits MW = 10)

19.10.2 16-bit wide memory bank connection



a. 16 bit wide memory bank interfaced to two 8 bit memory chips



b. 16 bit wide memory bank interfaced to a 16 bit memory chip

Fig 32. 16 bit bank external memory interfaces (bits MW = 01)

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19.10.3 8-bit wide memory bank connection

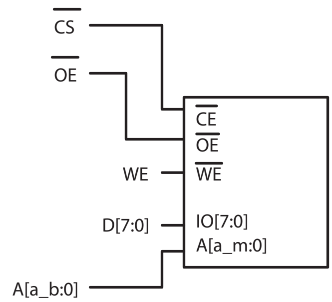


Fig 33. 8 bit bank external memory interface (bits MW = 00)

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19.10.4 Memory configuration example

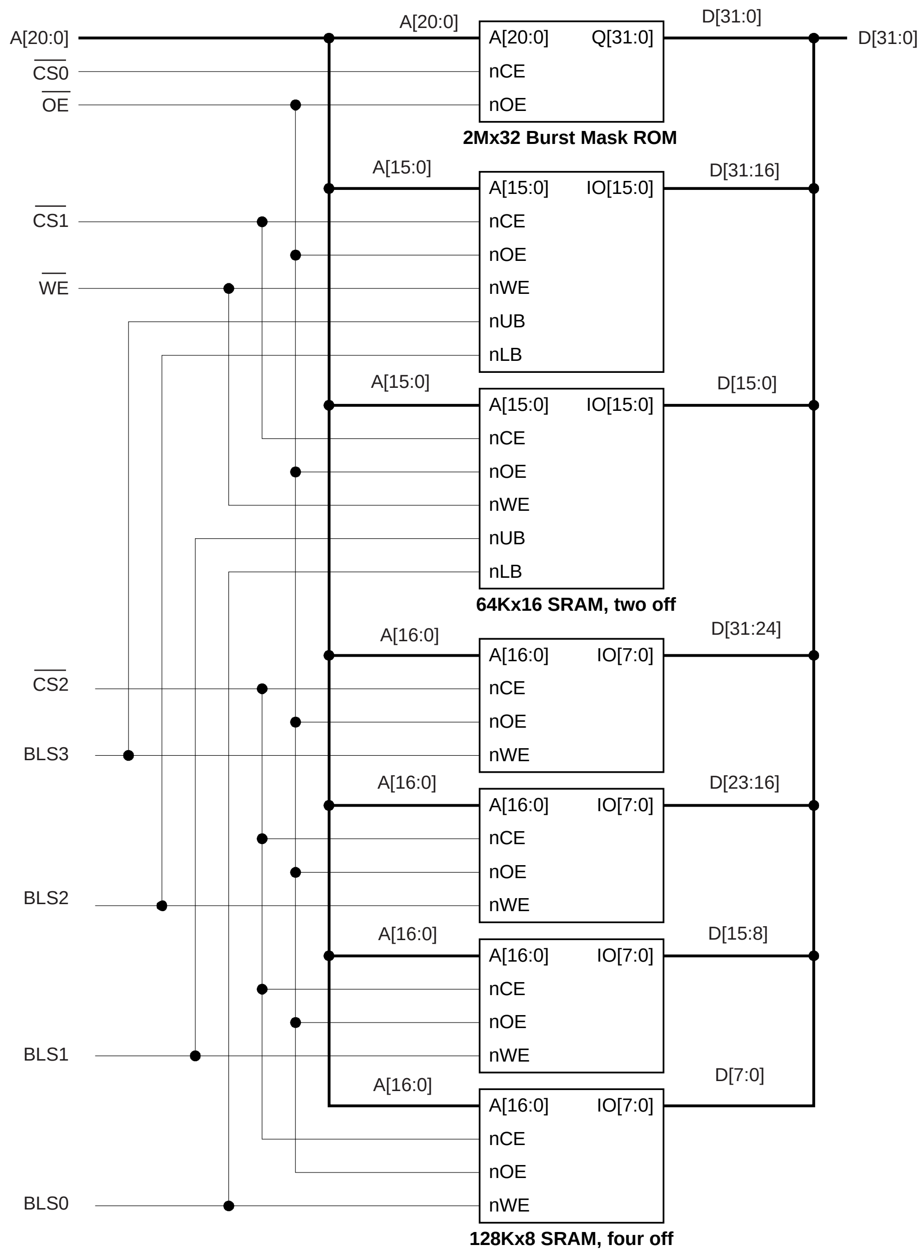


Fig 34. Typical memory configuration diagram

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20.1 How to read this chapter

The USB0 Host/Device/OTG controller is available on parts LPC1850, LPC1830, and LPC1820.

20.2 Basic configuration

The USB0 Host/Device/OTG controller is configured as follows:

- See Table 294 for clocking and power control.
- The USB0 is reset by the USB0_RST (reset # 17).
- The USB0 <tbd> is connected to interrupt slot # 8 in the NVIC, and the <tbd> is connected to slot # 9 in the Event router.

Table 294. USB0 clocking and power control

	Base clock	Branch clock	Maximum frequency	Notes
USB0 clock	BASE_USB0_CLK	CLK_USB0	480 MHz	Uses PLL0 dedicated to USB0. CLK_USB0 must be 480 MHz clock for the USB0 to operate in all three modes (low-speed, full-speed, and high-speed modes).
USB0 register interface clock	BASE_M3_CLK	CLK_M3_USB0	150 MHz	Uses PLL1.

20.3 Features

- Complies with Universal Serial Bus specification 2.0.
- Complies with USB On-The-Go supplement.
- Complies with Enhanced Host Controller Interface Specification.
- Complies with AMBA specification.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports all low-speed USB-compliant peripherals.
- Supports software HNP and SRP for OTG peripherals.
- Contains UTMI+ compliant transceiver (PHY).
- Supports power management.
- Supports six endpoints, control endpoint included.

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20.4 Introduction

Universal Serial Bus (USB) is a standard protocol developed to connect several types of devices to each other in order to exchange data or for other purposes. Many portable devices can benefit from the ability to communicate to each other over the USB interface without intervention of a host PC. The addition of the On-The-Go functionality to USB makes this possible without losing the benefits of the standard USB protocol. Examples of USB devices are: PC, mouse, keyboard, MP3 player, digital camera, USB storage device (USB stick).

20.4.1 Block diagram

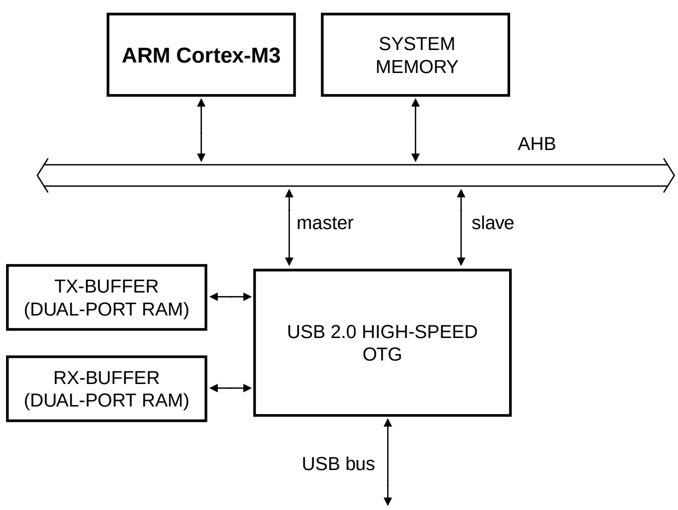


Fig 35. High-speed USB OTG block diagram

20.4.2 About USB On-The-Go

The USB On-The-Go block enables usage in both device mode and in host mode. This means that you can connect to a PC to exchange data, but also to another USB device such as a digital camera or MP3 player.

20.4.3 USB acronyms and abbreviations

Table 295. USB related acronyms

Acronym	Description
ATX	Analog Transceiver
DCD	Device Controller Driver
dQH	device Endpoint Queue Head
dTD	device Transfer Descriptor
EOP	End Of Packet
EP	End Point
FS	Full Speed
HCD	Host Controller Driver

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Table 295. USB related acronyms

Acronym	Description
HS	High Speed
LS	Low Speed
MPS	Maximum Packet Size
NAK	Negative Acknowledge
OTG	On-The-Go
PID	Packet Identifier
QH	Queue Head
SE0	Single Ended 0
SOF	Start Of Frame
TT	Transaction Translator
USB	Universal Serial Bus

20.4.4 Transmit and receive buffers

The USB OTG controller contains a Tx buffer to store data to be transmitted on the USB and an Rx buffer to store data received from the USB. The Rx buffer contains 256 words, and the Tx buffer contains 128 words for each endpoint in device mode and 512 words in host mode.

20.4.5 Fixed endpoint configuration

Table 296 shows the supported endpoint configurations. The Maximum Packet Size (MPS) (see Table 297) is dependent on the type of endpoint and the device configuration (low-speed, full-speed, or high-speed).

Table 296. Fixed endpoint configuration

Logical endpoint	Physical endpoint	Endpoint type	Direction
0	0	Control	Out
0	1	Control	In
1	2	Interrupt/Bulk/Isochronous	Out
1	3	Interrupt/Bulk/Isochronous	In
2	4	Interrupt/Bulk/Isochronous	Out
2	5	Interrupt/Bulk/Isochronous	In
3	6	Interrupt/Bulk/Isochronous	Out
3	7	Interrupt/Bulk/Isochronous	In
4	8	Interrupt/Bulk/Isochronous	Out
4	9	Interrupt/Bulk/Isochronous	In
5	10	Interrupt/Bulk/Isochronous	Out
5	11	Interrupt/Bulk/Isochronous	In

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Table 297. USB Packet size

Endpoint type	Speed	Packet size (byte)
Control	Low-speed	8
	Full-speed	8, 16, 32, or 64
	High-speed	64
Isochronous	Low-speed	n/a
	Full-speed	up to 1023
	High-speed	up to 1024
Interrupt	Low-speed	up to 8
	Full-speed	up to 64
	High-speed	up to 1024
Bulk	Low-speed	n/a
	Full-speed	8, 16, 32, or 64
	High-speed	8, 16, 32, 64 or 512

20.5 Pin description

Table 298. USB0 pin description

Function pinned out	Direction	Description
USB0_IND0	O	Port indicator LED control output.
USB0_IND1	O	Port indicator LED control output.
USB0_PWR_FAULT	O	Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
USB0_PWR_EN	O	VBUS drive signal (towards external charge pump or power management unit); indicates that Vbus must be driven (active high).
USB0_DP	I/O	USB0 bidirectional D+ line.
USB0_DM	I/O	USB0 bidirectional D− line.
USB0_VBUS	I	VBUS pin (power on USB cable).
USB0_ID	I	Indicates to the transceiver whether connected a A-device (ID LOW) or B-device (ID HIGH).
USB0_RREF		12.0 kOhm (accuracy 1%) on-board resistor to ground for current reference;
USB0_VDDA3V3_ DRIVER		Separate analog power supply for driver, 3.3V.
USB0_VDDA3V3		USB 3.3 V separate power supply voltage
USB0_VSSA_TERM		Dedicated analog ground for clean reference for termination resistors.
USB0_VSSA_REF		Dedicated clean analog ground for generation of reference currents and voltages.

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20.6 Register description

Table 299. Register access abbreviations

Abbreviation	Description
R/W	Read/Write
R/WC	Read/Write one to Clear
R/WO	Read/Write Once
RO	Read Only
WO	Write Only

Table 300. Register overview: USB0 OTG controller (register base address 0x4000 6000)

Name	Access	Address offset	Description	Reset value
-	-	0x000 - 0x0FF	Reserved	
Device/host capability registers				
CAPLENGTH	RO	0x100	Capability register length	0x0100 0040
HCSPARAMS	RO	0x104	Host controller structural parameters	0x0001 0011
HCCPARAMS	RO	0x108	Host controller capability parameters	0x0000 0006
DCIVERSION	RO	0x120	Device interface version number	0x0000 0001
DCCPARAMS	RO	0x124	Device controller capability parameters	0x0000 0186
-	-	0x128 - 0x13C	Reserved	
Device/host operational registers				
USBCMD_D	R/W	0x140	USB command (device mode)	0x0008 0000
USBCMD_H	R/W	0x140	USB command (host mode)	0x0008 0000
USBSTS_D	R/W	0x144	USB status (device mode)	0x0000 0000
USBSTS_H	R/W	0x144	USB status (host mode)	0x0000 0000
USBINTR_D	R/W	0x148	USB interrupt enable (device mode)	0x0000 0000
USBINTR_H	R/W	0x148	USB interrupt enable (host mode)	0x0000 0000
FRINDEX_D	R/W	0x14C	USB frame index (device mode)	0x0000 0000
FRINDEX_H	R/W	0x14C	USB frame index (host mode)	0x0000 0000
-	-	0x150	Reserved	
DEVICEADDR	R/W	0x154	USB device address (device mode)	0x0000 0000
PERIODICLISTBASE	R/W	0x154	Frame list base address (host mode)	0x0000 0000
ENDPOINTLISTADDR	R/W	0x158	Address of endpoint list in memory	0x0000 0000
ASYNCLISTADDR	R/W	0x158	Address of endpoint list in memory	0x0000 0000
TTCTRL	R/W	0x15C	Asynchronous buffer status for embedded TT (host mode)	0x0000 0000
BURSTSIZE	R/W	0x160	Programmable burst size	0x0000 0000
TXFILLTUNING	R/W	0x164	Host transmit pre-buffer packet tuning (host mode)	0x0000 0000
-	-	0x168 - 0x170	Reserved	-

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Table 300. Register overview: USB0 OTG controller (register base address 0x4000 6000)

Name	Access	Address offset	Description	Reset value
BINTERVAL	R/W	0x174	Length of virtual frame	0x0000 0000
ENDPTNAK	R/W	0x178	Endpoint NAK (device mode)	0x0000 0000
ENDPTNAKEN	R/W	0x17C	Endpoint NAK Enable (device mode)	0x0000 0000
-	-	0x180	Reserved	-
PORTSC1_D	R/W	0x184	Port 1 status/control (device mode)	0x0000 0000
PORTSC1_H	R/W	0x184	Port 1 status/control (host mode)	0x0000 0000
-	-	0x188 - 0x1A0		
OTGSC	R/W	0x1A4	OTG status and control	0x0000 0000
USBMODE_D	R/W	0x1A8	USB device mode (device mode)	0x0000 0000
USBMODE_H	R/W	0x1A8	USB device mode (host mode)	0x0000 0000
Device endpoint registers				
ENDPTSETUPSTAT	R/W	0x1AC	Endpoint setup status	0x0000 0000
ENDPTPRIME	R/W	0x1B0	Endpoint initialization	0x0000 0000
ENDPTFLUSH	R/W	0x1B4	Endpoint de-initialization	0x0000 0000
ENDPTSTAT	RO	0x1B8	Endpoint status	0x0000 0000
ENDPTCOMPLETE	R/W	0x1BC	Endpoint complete	0x0000 0000
ENDPTCTRL0	R/W	0x1C0	Endpoint control 0	0x0000 0000
ENDPTCTRL1	R/W	0x1C4	Endpoint control 1	0x0000 0000
ENDPTCTRL2	R/W	0x1C8	Endpoint control 2	0x0000 0000
ENDPTCTRL3	R/W	0x1CC	Endpoint control 3	0x0000 0000
ENDPTCTRL4	R/W	0x1D0	Endpoint control 4	0x0000 0000
ENDPTCTRL5	R/W	0x1D4	Endpoint control 5	0x0000 0000

20.6.1 Use of registers

The register interface has bit functions described for device mode and bit functions described for host mode. However, during OTG operations it is necessary to perform tasks independent of the controller mode.

The only way to transition the controller mode out of host or device mode is by setting the controller reset bit. Therefore, it is also necessary for the OTG tasks to be performed independently of a controller reset as well as independently of the controller mode.

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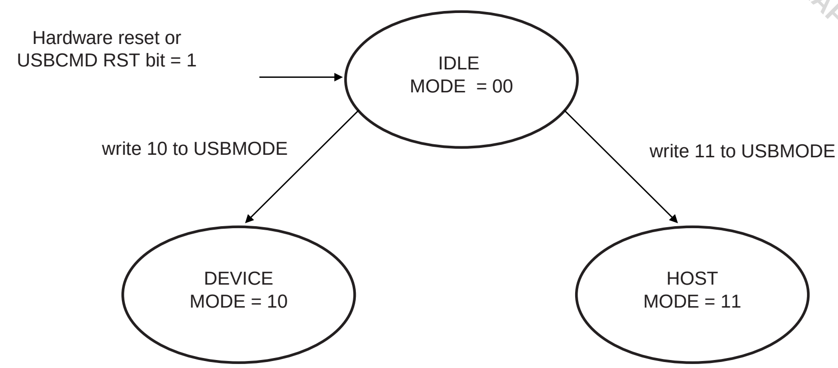


Fig 36. USB controller modes

The following registers and register bits are used for OTG operations. The values of these register bits are independent of the controller mode and are not affected by a write to the RESET bit in the USBCMD register.

- All identification registers
- All device/host capabilities registers
- All bits of the OTGSC register (Section 20.6.16)
- The following bits of the PORTSC register (Section 20.6.15):
  - PTS (parallel interface select)
  - STS (serial transceiver select)
  - PTW (parallel transceiver width)
  - PHCD (PHY low power suspend)
  - WKOC, WKDC, WKCN (wake signals)
  - PIC[1:0] (port indicators)
  - PP (port power)

20.6.2 Device/host capability registers

Table 301. CAPLENGTH register (CAPLENGTH - address 0x4000 6100) bit description

Bit	Symbol	Description	Reset value	Access
7:0	CAPLENGTH	Indicates offset to add to the register base address at the beginning of the Operational Register	0x40	RO
23:8	HCIVERSION	BCD encoding of the EHCI revision number supported by this host controller.	0x100	RO
31:24	-	These bits are reserved and should be set to zero.	-	-

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Table 302. HCSPARAMS register (HCSPARAMS - address 0x4000 6104) bit description

Bit	Symbol	Description	Reset value	Access
3:0	N_PORTS	Number of downstream ports. This field specifies the number of physical downstream ports implemented on this host controller.	0x1	RO
4	PPC	Port Power Control. This field indicates whether the host controller implementation includes port power control.	0x1	RO
7:5	-	These bits are reserved and should be set to zero.	-	-
11:8	N_PCC	Number of Ports per Companion Controller. This field indicates the number of ports supported per internal Companion Controller.	0x0	RO
15:12	N_CC	Number of Companion Controller. This field indicates the number of companion controllers associated with this USB2.0 host controller.	0x0	RO
16	PI	Port indicators. This bit indicates whether the ports support port indicator control.	0x1	RO
19:17	-	These bits are reserved and should be set to zero.	-	-
23:20	N_PTT	Number of Ports per Transaction Translator. This field indicates the number of ports assigned to each transaction translator within the USB2.0 host controller.	0x0	RO
27:24	N_TT	Number of Transaction Translators. This field indicates the number of embedded transaction translators associated with the USB2.0 host controller.	0x0	RO
31:28	-	These bits are reserved and should be set to zero.	-	-

Table 303. HCCPARAMS register (HCCPARAMS - address 0x4000 6108) bit description

Bit	Symbol	Description	Reset value	Access
0	ADC	64-bit Addressing Capability. If zero, no 64-bit addressing capability is supported.	0	RO
1	PFL	Programmable Frame List Flag. If set to one, then the system software can specify and use a smaller frame list and configure the host controller via the USBCMD register Frame List Size field. The frame list must always be aligned on a 4K-boundary. This requirement ensures that the frame list is always physically contiguous.	1	RO
2	ASP	Asynchronous Schedule Park Capability. If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule.The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.	1	RO

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Table 303. HCCPARAMS register (HCCPARAMS - address 0x4000 6108) bit description

Bit	Symbol	Description	Reset value	Access
7:4	IST	Isochronous Scheduling Threshold. This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule.	0	RO
15:8	EECP	EHCI Extended Capabilities Pointer. This optional field indicates the existence of a capabilities list.	0	RO
31:9	-	These bits are reserved and should be set to zero.	-	-

Table 304. DCIVERSION register (DCIVERSION - address 0x4000 6120) bit description

Bit	Symbol	Description	Reset value	Access
15:0	DCIVERSION	The device controller interface conforms to the two-byte BCD encoding of the interface version number contained in this register.	0x1	RO

Table 305. DCCPARAMS (address 0x4000 6124)

Bit	Symbol	Description	Reset value	Access
4:0	DEN	Device Endpoint Number.	0x4	RO
6:5	-	These bits are reserved and should be set to zero.	-	-
7	DC	Device Capable.	0x1	RO
8	HC	Host Capable.	0x1	RO
31:9	-	These bits are reserved and should be set to zero.	-	-

20.6.3 USB Command register (USBCMD)

The host/device controller executes the command indicated in this register.

20.6.3.1 Device mode

Table 306. USB Command register in device mode (USBCMD_D - address 0x4000 6140) bit description

Bit	Symbol	Value	Description	Access	Reset value
0	RS		Run/Stop	R/W	0
		0	Writing a 0 to this bit will cause a detach event.		
		1	Writing a one to this bit will cause the device controller to enable a pull-up on USB_DP and initiate an attach event. This control bit is not directly connected to the pull-up enable, as the pull-up will become disabled upon transitioning into high-speed mode. Software should use this bit to prevent an attach event before the device controller has been properly initialized.		

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Table 306. USB Command register in device mode (USBCMD_D - address 0x4000 6140) bit description *...continued*

Bit	Symbol	Value	Description	Access	Reset value
1	RST		Controller reset. Software uses this bit to reset the controller. This bit is set to zero by the Host/Device Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register.	R/W	0
		0	Set to 0 by hardware when the reset process is complete.		
		1	When software writes a one to this bit, the Device Controller resets its internal pipelines, timers, counters, state machines etc. to their initial values. Writing a one to this bit when the device is in the attached state is not recommended, since the effect on an attached host is undefined. In order to ensure that the device is not in an attached state before initiating a device controller reset, all primed endpoints should be flushed and the USBCMD Run/Stop bit should be set to 0.		
3:2	-	-	Not used in device mode.	-	0
4	-	-	Not used in device mode.	-	0
5	-	-	Not used in device mode.	-	0
6	-	-	Not used in device mode. Writing a one to this bit when the device mode is selected, will have undefined results.	-	-
7	-	-	Reserved. These bits should be set to 0.	-	-
9:8	-	-	Not used in Device mode.	-	-
10	-		Reserved.These bits should be set to 0.	-	0
11	-	-	Not used in Device mode.	-	
12	-		Reserved.These bits should be set to 0.	-	0
13	SUTW		Setup trip wire During handling a setup packet, this bit is used as a semaphore to ensure that the setup data payload of 8 bytes is extracted from a QH by the DCD without being corrupted. If the setup lockout mode is off (see USBMODE register) then there exists a hazard when new setup data arrives while the DCD is copying the setup data payload from the QH for a previous setup packet. This bit is set and cleared by software and will be cleared by hardware when a hazard exists. (See Section 20.10).	R/W	0
14	ATDTW		Add dTD trip wire This bit is used as a semaphore to ensure the to proper addition of a new dTD to an active (primed) endpoint's linked list. This bit is set and cleared by software during the process of adding a new dTD. See also Section 20.10. This bit shall also be cleared by hardware when its state machine is hazard region for which adding a dTD to a primed endpoint may go unrecognized.	R/W	0

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Table 306. USB Command register in device mode (USBCMD_D - address 0x4000 6140) bit description *...continued*

Bit	Symbol	Value	Description	Access	Reset value
15	-		Not used in device mode.	-	-
23:16	ITC		Interrupt threshold control. The system software uses this field to set the maximum rate at which the host/device controller will issue interrupts. ITC contains the maximum interrupt interval measured in micro-frames. Valid values are shown below. All other values are reserved. 0x0 = Immediate (no threshold) 0x1 = 1 micro frame. 0x2 = 2 micro frames. 0x8 = 8 micro frames. 0x10 = 16 micro frames. 0x20 = 32 micro frames. 0x40 = 64 micro frames.	R/W	0x8
31:24	-		Reserved		0

20.6.3.2 Host mode

Table 307. USB Command register in host mode (USBCMD_H - address 0x4000 6140) bit description - host mode

Bit	Symbol	Value	Description	Access	Reset value
0	RS		Run/Stop	R/W	0
		0	When this bit is set to 0, the Host Controller completes the current transaction on the USB and then halts. The HC Halted bit in the status register indicates when the Host Controller has finished the transaction and has entered the stopped state. Software should not write a one to this field unless the host controller is in the Halted state (i.e. HCHalted in the USBSTS register is a one).		
		1	When set to a 1, the Host Controller proceeds with the execution of the schedule. The Host Controller continues execution as long as this bit is set to a one.		
1	RST		Controller reset. Software uses this bit to reset the controller. This bit is set to zero by the Host/Device Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register.	R/W	0
		0	This bit is set to zero by hardware when the reset process is complete.		
		1	When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. Software should not set this bit to a one when the HCHalted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.		
2	FS0		Bit 0 of the Frame List Size bits. See Table 308. This field specifies the size of the frame list that controls which bits in the Frame Index Register should be used for the Frame List Current index. Note that this field is made up from USBCMD bits 15, 3, and 2.		0
3	FS1		Bit 1 of the Frame List Size bits. See Table 308.		0

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Table 307. USB Command register in host mode (USBCMD_H - address 0x4000 6140) bit description - host mode

Bit	Symbol	Value	Description	Access	Reset value
4	PSE		This bit controls whether the host controller skips processing the periodic schedule.	R/W	0
		0	Do not process the periodic schedule.		
		1	Use the PERIODICLISTBASE register to access the periodic schedule.		
5	ASE		This bit controls whether the host controller skips processing the asynchronous schedule.	R/W	0
		0	Do not process the asynchronous schedule.		
		1	Use the ASYNCLISTADDR to access the asynchronous schedule.		
6	IAA		This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule.	R/W	0
		0	The host controller sets this bit to zero after it has set the Interrupt on Sync Advance status bit in the USBSTS register to one.		
		1	Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule states, it sets the Interrupt on Async Advance status bit in the USBSTS register. If the Interrupt on Sync Advance Enable bit in the USBINTR register is one, then the host controller will assert an interrupt at the next interrupt threshold. Software should not write a one to this bit when the asynchronous schedule is inactive. Doing so will yield undefined results.		
7	-	-	Reserved		0
9:8	ASP1_0		Asynchronous schedule park mode Contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid values are 0x1 to 0x3. **Remark:** Software must not write 00 to this bit when Park Mode Enable is one as this will result in undefined behavior.	R/W	11
10	-	-	Reserved.	-	0
11	ASPE		Asynchronous Schedule Park Mode Enable	R/W	1
		0	Park mode is disabled.		
		1	Park mode is enabled.		
12	-	-	Reserved.	-	0
13	-	-	Not used in Host mode.	-	
14	-	-	Reserved.	-	0

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Table 307. USB Command register in host mode (USBCMD_H - address 0x4000 6140) bit description - host mode

Bit	Symbol	Value	Description	Access	Reset value
15	FS2		Bit 2 of the Frame List Size bits. See Table 308.	-	0
23:16	ITC		Interrupt threshold control. The system software uses this field to set the maximum rate at which the host/device controller will issue interrupts. ITC contains the maximum interrupt interval measured in micro-frames. Valid values are shown below. All other values are reserved. 0x0 = Immediate (no threshold) 0x1 = 1 micro frame. 0x2 = 2 micro frames. 0x8 = 8 micro frames. 0x10 = 16 micro frames. 0x20 = 32 micro frames. 0x40 = 64 micro frames.	R/W	0x8
31:24	-		Reserved		0

Table 308. Frame list size values

USBCMD bit 15	USBCMD bit 3	USBCMD bit 2	Frame list size
0	0	0	1024 elements (4096 bytes) - default value
0	0	1	512 elements (2048 bytes)
0	1	0	256 elements (1024 bytes)
0	1	1	128 elements (512 bytes)
1	0	0	64 elements (256 bytes)
1	0	1	32 elements (128 bytes)
1	1	0	16 elements (64 bytes)
1	1	1	8 elements (32 bytes)

20.6.4 USB Status register (USBSTS)

This register indicates various states of the Host/Device controller and any pending interrupts. Software sets a bit to zero in this register by writing a one to it.

Remark: This register does not indicate status resulting from a transaction on the serial bus.

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20.6.4.1 Device mode

Table 309. USB Status register in device mode (USBSTS_D - address 0x4000 6144) register bit description

Bit	Symbol	Value	Description	Reset value	Access
0	UI		USB interrupt	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	This bit is set by the Host/Device Controller when the cause of an interrupt is a completion of a USB transaction where the Transfer Descriptor (TD) has an interrupt on complete (IOC) bit set. This bit is also set by the Host/Device Controller when a short packet is detected. A short packet is when the actual number of bytes received was less than the expected number of bytes.		
1	UEI		USB error interrupt	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	When completion of a USB transaction results in an error condition, this bit is set by the Host/Device Controller. This bit is set along with the USBINT bit, if the TD on which the error interrupt occurred also had its interrupt on complete (IOC) bit set. The device controller detects resume signaling only (see Section 20.10.11.6).		
2	PCI		Port change detect.	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	The Device Controller sets this bit to a one when the port controller enters the full or high-speed operational state. When the port controller exits the full or high-speed operation states due to Reset or Suspend events, the notification mechanisms are the USB Reset Received bit (URI) and the DCSuspend bits (SLI) respectively.		
3	-		Not used in Device mode.		-
4	-		Reserved.	0	-
5	AAI		Not used in Device mode.	0	-
6	URI		USB reset received	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	When the device controller detects a USB Reset and enters the default state, this bit will be set to a one.		

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Table 309. USB Status register in device mode (USBSTS_D - address 0x4000 6144) register bit description

Bit	Symbol	Value	Description	Reset value	Access
7	SRI		SOF received	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	When the device controller detects a Start Of (micro) Frame, this bit will be set to a one. When a SOF is extremely late, the device controller will automatically set this bit to indicate that an SOF was expected. Therefore, this bit will be set roughly every 1 ms in device FS mode and every 125 μs in HS mode and will be synchronized to the actual SOF that is received. Since the device controller is initialized to FS before connect, this bit will be set at an interval of 1ms during the prelude to connect and chirp.		
8	SLI		DCSuspend	0	R/WC
		0	The device controller clears the bit upon exiting from a suspend state. This bit is cleared by software writing a one to it.		
		1	When a device controller enters a suspend state from an active state, this bit will be set to a one.		
11:9	-	-	Reserved. Software should only write 0 to reserved bits.		
12	-	-	Not used in Device mode.	0	
13	-	-	Not used in Device mode.	0	
14	-	-	Not used in Device mode.	0	
15	-	-	Not used in Device mode.	0	
16	NAKI		NAK interrupt bit	0	RO
		0	This bit is automatically cleared by hardware when the all the enabled TX/RX Endpoint NAK bits are cleared.		
		1	It is set by hardware when for a particular endpoint both the TX/RX Endpoint NAK bit and the corresponding TX/RX Endpoint NAK Enable bit are set.		
17	-	-	Reserved. Software should only write 0 to reserved bits.	0	-
18	-		Not used in Device mode.	0	-
19	-		Not used in Device mode.	0	-
31:20	-	-	Reserved. Software should only write 0 to reserved bits.		-

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20.6.4.2 Host mode

Table 310. USB Status register in host mode (USBSTS_H - address 0x4000 6144) register bit description

Bit	Symbol	Value	Description	Reset value	Access
0	UI		USB interrupt (USBINT)	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	This bit is set by the Host/Device Controller when the cause of an interrupt is a completion of a USB transaction where the Transfer Descriptor (TD) has an interrupt on complete (IOC) bit set. This bit is also set by the Host/Device Controller when a short packet is detected. A short packet is when the actual number of bytes received was less than the expected number of bytes.		
1	UEI		USB error interrupt (USBERRINT)	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	When completion of a USB transaction results in an error condition, this bit is set by the Host/Device Controller. This bit is set along with the USBINT bit, if the TD on which the error interrupt occurred also had its interrupt on complete (IOC) bit set.		
2	PCI		Port change detect.	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	The Host Controller sets this bit to a one when on any port a Connect Status occurs, a Port Enable/Disable Change occurs, or the Force Port Resume bit is set as the result of a J-K transition on the suspended port.		
3	FRI		Frame list roll-over	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the Frame List Size field of the USBCMD register) is 1024, the Frame Index Register rolls over every time FRINDEX bit 13 toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX bit 12 toggles (see Section 20.6.6).		
4	-		Reserved.		
5	AAI		Interrupt on async advance	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.		
6	-	-	Not used by the Host controller.	0	R/WC
7	SRI		SOF received	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	In host mode, this bit will be set every 125 μs and can be used by host controller driver as a time base.		
8	-	-	Not used by the Host controller.	-	-
11:9	-	-	Reserved.		

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Table 310. USB Status register in host mode (USBSTS_H - address 0x4000 6144) register bit description *...continued*

Bit	Symbol	Value	Description	Reset value	Access
12	HCH		HCHalted	1	RO
		0	The RS bit in USBCMD is set to zero. Set by the host controller.		
		1	The Host Controller sets this bit to one after it has stopped executing because of the Run/Stop bit being set to 0, either by software or by the Host Controller hardware (e.g. because of an internal error).		
13	RCL		Reclamation	0	RO
		0	No empty asynchronous schedule detected.		
		1	An empty asynchronous schedule is detected. Set by the host controller.		
14	PS		Periodic schedule status This bit reports the current real status of the Periodic Schedule. The Host Controller is not required to immediately disable or enable the Periodic Schedule when software transitions the Periodic Schedule Enable bit in the USBCMD register. When this bit and the Periodic Schedule Enable bit are the same value, the Periodic Schedule is either enabled (if both are 1) or disabled (if both are 0).	0	RO
		0	The periodic schedule status is disabled.		
		1	The periodic schedule status is enabled.		
15	AS		Asynchronous schedule status This bit reports the current real status of the Asynchronous Schedule. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (if both are 1) or disabled (if both are 0).	0	
		0	Asynchronous schedule status is disabled.		
		1	Asynchronous schedule status is enabled.		
16	-		Not used on Host mode.	0	-
17	-		Reserved.		
18	UAI		USB host asynchronous interrupt (USBHSTASYNCINT)	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	This bit is set by the Host Controller when the cause of an interrupt is a completion of a USB transaction where the Transfer Descriptor (TD) has an interrupt on complete (IOC) bit set **and** the TD was from the asynchronous schedule. This bit is also set by the Host when a short packet is detected **and** the packet is on the asynchronous schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes.		
19	UPI		USB host periodic interrupt (USBHSTPERINT)	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	This bit is set by the Host Controller when the cause of an interrupt is a completion of a USB transaction where the Transfer Descriptor (TD) has an interrupt on complete (IOC) bit set **and** the TD was from the periodic schedule. This bit is also set by the Host Controller when a short packet is detected **and** the packet is on the periodic schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes.		
31:20	-				

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20.6.5 USB Interrupt register (USBINTR)

The software interrupts are enabled with this register. An interrupt is generated when a bit is set and the corresponding interrupt is active. The USB Status register (USBSTS) still shows interrupt sources even if they are disabled by the USBINTR register, allowing polling of interrupt events by the software. All interrupts must be acknowledged by software by clearing (that is writing a 1 to) the corresponding bit in the USBSTS register.

20.6.5.1 Device mode

Table 311. USB Interrupt register in device mode (USBINTR_D - address 0x4000 6148) bit description

Bit	Symbol	Description	Reset value	Access
0	UE	USB interrupt enable When this bit is one, and the USBINT bit in the USBSTS register is one, the host/device controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit in USBSTS.	0	R/W
1	UEE	USB error interrupt enable When this bit is a one, and the USBERRINT bit in the USBSTS register is a one, the host/device controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit in the USBSTS register.	0	R/W
2	PCE	Port change detect enable When this bit is a one, and the Port Change Detect bit in the USBSTS register is a one, the host/device controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit in USBSTS.	0	R/W
3	-	Not used by the Device controller.		
4	-	Reserved	0	-
5	-	Not used by the Device controller.		
6	URE	USB reset enable When this bit is a one, and the USB Reset Received bit in the USBSTS register is a one, the device controller will issue an interrupt. The interrupt is acknowledged by software clearing the USB Reset Received bit.	0	R/W
7	SRE	SOF received enable When this bit is a one, and the SOF Received bit in the USBSTS register is a one, the device controller will issue an interrupt. The interrupt is acknowledged by software clearing the SOF Received bit.	0	R/W
8	SLE	Sleep enable When this bit is a one, and the DCSuspend bit in the USBSTS register transitions, the device controller will issue an interrupt. The interrupt is acknowledged by software writing a one to the DCSuspend bit.	0	R/W
15:9	-	Reserved	-	-
16	NAKE	NAK interrupt enable This bit is set by software if it wants to enable the hardware interrupt for the NAK Interrupt bit. If both this bit and the corresponding NAK Interrupt bit are set, a hardware interrupt is generated.	0	R/W
17	-	Reserved		
18	-	Not used by the Device controller.		
19	-	Not used by the Device controller.		
31:20	-	Reserved		

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20.6.5.2 Host mode

Table 312. USB Interrupt register in host mode (USBINTR_H - address 0x4000 6148) bit description

Bit	Symbol	Description	Access	Reset value
0	UE	USB interrupt enable When this bit is one, and the USBINT bit in the USBSTS register is one, the host/device controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit in USBSTS.	R/W	0
1	UEE	USB error interrupt enable When this bit is a one, and the USBERRINT bit in the USBSTS register is a one, the host/device controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit in the USBSTS register.	R/W	0
2	PCE	Port change detect enable When this bit is a one, and the Port Change Detect bit in the USBSTS register is a one, the host/device controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit in USBSTS.	R/W	0
3	FRE	Frame list rollover enable When this bit is a one, and the Frame List Rollover bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.		
4	-	Reserved	-	0
5	AAE	Interrupt on asynchronous advance enable When this bit is a one, and the Interrupt on Async Advance bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.	R/W	0
6	-	Not used by the Host controller.	-	0
7	SRE	If this bit is one and the SRI bit in the USBSTS register is one, the host controller will issue an interrupt. In host mode, the SRI bit will be set every 125 μs and can be used by the host controller as a time base. The interrupt is acknowledged by software clearing the SRI bit in the USBSTS register.	-	0
8	-	Not used by the Host controller.	-	0
15:9	-	Reserved		
16	-	Not used by the host controller.	R/W	0
17	-	Reserved		
18	UAIE	USB host asynchronous interrupt enable When this bit is a one, and the USBHSTASYNCINT bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBHSTASYNCINT bit.	R/W	0
19	UPIA	USB host periodic interrupt enable When this bit is a one, and the USBHSTPERINT bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBHSTPERINT bit.	R/W	0
31:20	-	Reserved		

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20.6.6 Frame index register (FRINDEX)

20.6.6.1 Device mode

In Device mode this register is read only, and the device controller updates the FRINDEX[13:3] register from the frame number indicated by the SOF marker. Whenever a SOF is received by the USB bus, FRINDEX[13:3] will be checked against the SOF marker. If FRINDEX[13:3] is different from the SOF marker, FRINDEX[13:3] will be set to the SOF value and FRINDEX[2:0] will be set to zero (i.e. SOF for 1 ms frame). If FRINDEX [13:3] is equal to the SOF value, FRINDEX[2:0] will be incremented (i.e. SOF for 125 μs micro-frame) by hardware.

Table 313. USB frame index register in device mode (FRINDEX_D - address 0x4000 614C) bit description

Bit	Symbol	Description	Reset value	Access
2:0	FRINDEX2_0	Current micro frame number	N/A	RO
13:3	FRINDEX13_3	Current frame number of the last frame transmitted	N/A	RO
31:14	-	Reserved	N/A	

20.6.6.2 Host mode

This register is used by the host controller to index the periodic frame list. The register updates every 125 μs (once each micro-frame). Bits[N: 3] are used to select a particular entry in the Periodic Frame List during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by system software in the Frame List Size field in the USBCMD register.

This register must be written as a DWord. Byte writes produce undefined results. This register cannot be written unless the Host Controller is in the 'Halted' state as indicated by the HCHalted bit in the USBSTS register (host mode). A write to this register while the Run/Stop bit is set to a one produces undefined results. Writes to this register also affect the SOF value.

Table 314. USB frame index register in host (FRINDEX_H - address 0x4000 614C) bit description

Bit	Symbol	Description	Reset value	Access
2:0	FRINDEX2_0	Current micro frame number	N/A	R/W
12:3	FRINDEX12_3	Frame list current index.	N/A	R/W
31:13	-	Reserved	N/A	

Table 315. Number of bits used for the frame list index

USBCMD bit 15	USBCMD bit 3	USBCMD bit 2	Frame list size	N
0	0	0	1024 elements (4096 bytes). Default value.	12
0	0	1	512 elements (2048 bytes)	11
0	1	0	256 elements (1024 bytes)	10
0	1	1	128 elements (512 bytes)	9
1	0	0	64 elements (256 bytes)	8

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Table 315. Number of bits used for the frame list index

USBCMD bit 15	USBCMD bit 3	USBCMD bit 2	Frame list size	N
1	0	1	32 elements (128 bytes)	7
1	1	0	16 elements (64 bytes)	6
1	1	1	8 elements (32 bytes)	5

20.6.7 Device address (DEVICEADDR - device) and Periodic List Base (PERIODICLISTBASE- host) registers

20.6.7.1 Device mode

The upper seven bits of this register represent the device address. After any controller reset or a USB reset, the device address is set to the default address (0). The default address will match all incoming addresses. Software shall reprogram the address after receiving a SET_ADDRESS descriptor.

The USBADRA bit is used to accelerate the SET_ADDRESS sequence by allowing the DCD to preset the USBADR register bits before the status phase of the SET_ADDRESS descriptor.

Table 316. USB Device Address register in device mode (DEVICEADDR - address 0x4000 6154) bit description

Bit	Symbol	Value	Description	Reset value	Access
23:0	-		Reserved	0	-
24	USBADRA		Device address advance		
		0	Any write to USBADR are instantaneous.		
		1	When the user writes a one to this bit at the same time or before USBADR is written, the write to USBADR fields is staged and held in a hidden register. After an IN occurs on endpoint 0 and is acknowledged, USBADR will be loaded from the holding register. Hardware will automatically clear this bit on the following conditions: • IN is ACKed to endpoint 0. USBADR is updated from the staging register. • OUT/SETUP occurs on endpoint 0. USBADR is **not** updated. • Device reset occurs. USBADR is set to 0. **Remark:** After the status phase of the SET_ADDRESS descriptor, the DCD has 2 ms to program the USBADR field. This mechanism will ensure this specification is met when the DCD can not write the device address within 2 ms from the SET_ADDRESS status phase. If the DCD writes the USBADR with USBADRA=1 after the SET_ADDRESS data phase (before the prime of the status phase), the USBADR will be programmed instantly at the correct time and meet the 2 ms USB requirement.		
31:25	USBADR		USB device address	0	R/W

20.6.7.2 Host mode

This 32-bit register contains the beginning address of the Periodic Frame List in the system memory. The host controller driver (HCD) loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this

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physical memory pointer is assumed to be 4 kB aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.

Table 317. USB Periodic List Base register in host mode (PERIODICLISTBASE - address 0x4000 6154) bit description

Bit	Symbol	Description	Reset value	Access
11:0	-	Reserved	-	-
31:12	PERBASE31_12	Base Address (Low) These bits correspond to the memory address signals 31:12.	-	R/W

20.6.8 Endpoint List Address register (ENDPOINTLISTADDR - device) and Asynchronous List Address (ASYNCLISTADDR - host) registers

20.6.8.1 Device mode

In device mode, this register contains the address of the top of the endpoint list in system memory. Bits[10:0] of this register cannot be modified by the system software and will always return a zero when read.The memory structure referenced by this physical memory pointer is assumed 64 byte aligned.

Table 318. USB Endpoint List Address register in device mode (ENDPOINTLISTADDR - address 0x4000 6158) bit description

Bit	Symbol	Description	Reset value	Access
10:0	-	reserved	0	-
31:11	EPBASE31_11	Endpoint list pointer (low) These bits correspond to memory address signals 31:11, respectively. This field will reference a list of up to 4 Queue Heads (QH). (i.e. one queue head per endpoint and direction.)	-	R/W

20.6.8.2 Host mode

This 32-bit register contains the address of the next asynchronous queue head to be executed by the host. Bits [4:0] of this register cannot be modified by the system software and will always return a zero when read.

Table 319. USB Asynchronous List Address register in host mode (ASYNCLISTADDR- address 0x4000 6158) bit description

Bit	Symbol	Description	Reset value	Access
4:0	-	Reserved	0	-
31:5	ASYBASE31_5	Link pointer (Low) LPL These bits correspond to memory address signals 31:5, respectively. This field may only reference a Queue Head (OH).	-	R/W

20.6.9 TT Control register (TTCTRL)

20.6.9.1 Device mode

This register is not used in device mode.

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20.6.9.2 Host mode

This register contains parameters needed for internal TT operations. This register is used by the host controller only. Writes must be in Dwords.

Table 320. USB TT Control register in host mode (TTCTRL - address 0x4000 615C) bit description

Bit	Symbol	Description	Reset value	Access
23:0	-	Reserved.	0	-
30:24	TTHA	Hub address when FS or LS device are connected directly.	N/A	R/W
31	-	Reserved.	0	

20.6.10 Burst Size register (BURSTSIZE)

This register is used to control and dynamically change the burst size used during data movement on the master interface of the USB DMA controller. Writes must be in Dwords.

The default for the length of a burst of 32-bit words for RX and TX DMA data transfers is 16 words each.

Table 321. USB burst size register (BURSTSIZE - address 0x4000 6160) bit description - device/host mode

Bit	Symbol	Description	Reset value	Access
7:0	RXPBURST	Programmable RX burst length This register represents the maximum length of a burst in 32-bit words while moving data from the USB bus to system memory.	0x10	R/W
15:8	TXPBURST	Programmable TX burst length This register represents the maximum length of a burst in 32-bit words while moving data from system memory to the USB bus.	0x10	R/W
31:16	-	Reserved.	-	-

20.6.11 Transfer buffer Fill Tuning register (TXFILLTUNING)

20.6.11.1 Device controller

This register is not used in device mode.

20.6.11.2 Host controller

The fields in this register control performance tuning associated with how the host controller posts data to the TX latency FIFO before moving the data onto the USB bus. The specific areas of performance include the how much data to post into the FIFO and an estimate for how long that operation should take in the target system.

Definitions:

T_0 = Standard packet overhead

T_1 = Time to send data payload

T_{ff} = Time to fetch packet into TX FIFO up to specified level

T_s = Total packet flight time (send-only) packet; $T_s = T_0 + T_1$

T_p = Total packet time (fetch and send) packet; $T_p = T_{ff} + T_0 + T_1$

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Upon discovery of a transmit (OUT/SETUP) packet in the data structures, host controller checks to ensure T_p remains before the end of the (micro) frame. If so it proceeds to pre-fill the TX FIFO. If at anytime during the pre-fill operation the time remaining the [micro]frame is < T_s then the packet attempt ceases and the packet is tried at a later time. Although this is not an error condition and the host controller will eventually recover, a mark will be made the scheduler health counter to note the occurrence of a “backoff” event. When a back-off event is detected, the partial packet fetched may need to be discarded from the latency buffer to make room for periodic traffic that will begin after the next SOF. Too many back-off events can waste bandwidth and power on the system bus and thus should be minimized (not necessarily eliminated). Backoffs can be minimized with use of the TSCHHEALTH (T_{ff}) described below.

Table 322. USB Transfer buffer Fill Tuning register in host mode (TXFILLTUNING - address 0x4000 6164) bit description

Bit	Symbol	Description	Reset value	Access
7:0	TXSCHOH	FIFO burst threshold This register controls the number of data bursts that are posted to the TX latency FIFO in host mode before the packet begins on to the bus. The minimum value is 2 and this value should be a low as possible to maximize USB performance. A higher value can be used in systems with unpredictable latency and/or insufficient bandwidth where the FIFO may underrun because the data transferred from the latency FIFO to USB occurs before it can be replenished from system memory. This value is ignored if the Stream Disable bit in USBMODE register is set.	0x2	R/W
12:8	TXSCHEATLTH	Scheduler health counter This register increments when the host controller fails to fill the TX latency FIFO to the level programmed by TXFIFOTHRES before running out of time to send the packet before the next Start-Of-Frame . This health counter measures the number of times this occurs to provide feedback to selecting a proper TXSCHOH. Writing to this register will clear the counter. The maximum value is 31.	0x0	R/W
15:13	-	reserved	-	-
21:16	TXFIFOTHRES	Scheduler overhead This register adds an additional fixed offset to the schedule time estimator described above as T_{ff}. As an approximation, the value chosen for this register should limit the number of back-off events captured in the TXSCHHEALTH to less than 10 per second in a highly utilized bus. Choosing a value that is too high for this register is not desired as it can needlessly reduce USB utilization. The time unit represented in this register is 1.267 μs when a device is connected in High-Speed Mode for OTG and SPH. The time unit represented in this register is 6.333 μs when a device is connected in Low/Full Speed Mode for OTG and SPH.	0x0	R/W
31:22	-	reserved		

20.6.12 BINTERVAL register

This register defines the bInterval value which determines the length of the virtual frame (see Section 20.7.7).

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Table 323. USB BINTERVAL register (BINTERVAL - address 0x4000 6174) bit description

Bit	Symbol	Description	Reset value	Access
3:0	BINT	bInterval value (see Section 20.7.7)	0x00	R/W
31:4	-	reserved	-	-

20.6.13 USB Endpoint NAK register (ENDPTNAK)

20.6.13.1 Device mode

This register indicates when the device sends a NAK handshake on an endpoint. Each Tx and Rx endpoint has a bit in the EPTN and EPRN field respectively.

A bit in this register is cleared by writing a 1 to it.

Table 324. USB endpoint NAK register (ENDPTNAK - address 0x4000 6178) bit description

Bit	Symbol	Description	Reset value	Access
5:0	EPRN	Rx endpoint NAK Each RX endpoint has one bit in this field. The bit is set when the device sends a NAK handshake on a received OUT or PING token for the corresponding endpoint. Bit 5 corresponds to endpoint 5. ... Bit 1 corresponds to endpoint 1. Bit 0 corresponds to endpoint 0.	0x00	R/WC
15:6	-	Reserved	-	-
21:16	EPTN	Tx endpoint NAK Each TX endpoint has one bit in this field. The bit is set when the device sends a NAK handshake on a received IN token for the corresponding endpoint. Bit 3 corresponds to endpoint 3. ... Bit 1 corresponds to endpoint 1. Bit 0 corresponds to endpoint 0.	0x00	R/WC
31:22	-	reserved	-	-

20.6.13.2 Host mode

This register is not used in host mode.

20.6.14 USB Endpoint NAK Enable register (ENDPTNAKEN)

20.6.14.1 Device mode

Each bit in this register enables the corresponding bit in the ENDPTNAK register. Each Tx and Rx endpoint has a bit in the EPTNE and EPRNE field respectively.

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Table 325. USB Endpoint NAK Enable register (ENDPTNAKEN - address 0x4000 617C) bit description

Bit	Symbol	Description	Reset value	Access
5:0	EPRNE	Rx endpoint NAK enable Each bit enables the corresponding RX NAK bit. If this bit is set and the corresponding RX endpoint NAK bit is set, the NAK interrupt bit is set. Bit 5 corresponds to endpoint 5. ... Bit 1 corresponds to endpoint 1. Bit 0 corresponds to endpoint 0.	0x00	R/W
15:6	-	Reserved	-	-
21:16	EPTNE	Tx endpoint NAK Each bit enables the corresponding TX NAK bit. If this bit is set and the corresponding TX endpoint NAK bit is set, the NAK interrupt bit is set. Bit 5 corresponds to endpoint 5. ... Bit 1 corresponds to endpoint 1. Bit 0 corresponds to endpoint 0.	0x00	R/W
31:22	-	Reserved	-	-

20.6.14.2 Host mode

This register is not used in host mode.

20.6.15 Port Status and Control register (PORTSC1)

20.6.15.1 Device mode

The device controller implements one port register, and it does not support power control. Port control in device mode is used for status port reset, suspend, and current connect status. It is also used to initiate test mode or force signaling. This register allows software to put the PHY into low-power Suspend mode and disable the PHY clock.

Table 326. Port Status and Control register in device mode (PORTSC1_D - address 0x4000 6184) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	CCS		Current connect status	0	RO
		0	Device not attached A zero indicates that the device did not attach successfully or was forcibly disconnected by the software writing a zero to the Run bit in the USBCMD register. It does not state the device being disconnected or suspended.		
		1	Device attached. A one indicates that the device successfully attached and is operating in either high-speed mode or full-speed mode as indicated by the High Speed Port bit in this register.		
1	-	-	Not used in device mode	0	-
2	PE		Port enable. This bit is always 1. The device port is always enabled.	1	RO
3	PEC		Port enable/disable change This bit is always 0. The device port is always enabled.	0	RO

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Table 326. Port Status and Control register in device mode (PORTSC1_D - address 0x4000 6184) bit description

Bit	Symbol	Value	Description	Reset value	Access
5:4	-	-	Reserved	0	RO
6	FPR		Force port resume After the device has been in Suspend State for 5 ms or more, software must set this bit to one to drive resume signaling before clearing. The Device Controller will set this bit to one if a J-to-K transition is detected while the port is in the Suspend state. The bit will be cleared when the device returns to normal operation. When this bit transitions to a one because a J-to-K transition detected, the Port Change Detect bit in the USBSTS register is set to one as well.	0	R/W
		0	No resume (K-state) detected/driven on port.		
		1	Resume detected/driven on port.		
7	SUSP		Suspend In device mode, this is a read-only status bit .	0	RO
		0	Port not in suspend state		
		1	Port in suspend state		
8	PR		Port reset In device mode, this is a read-only status bit. A device reset from the USB bus is also indicated in the USBSTS register.	0	RO
		0	Port is not in the reset state.		
		1	Port is in the reset state.		
9	HSP		High-speed status **Remark:** This bit is redundant with bits 27:26 (PSPD) in this register. It is implemented for compatibility reasons.	0	RO
		0	Host/device connected to the port is not in High-speed mode.		
		1	Host/device connected to the port is in High-speed mode.		
11:10	-	-	Not used in device mode.		
12	-	-	Not used in device mode.		
13	-	-	Reserved	-	-
15:14	PIC1_0		Port indicator control Writing to this field effects the value of the USB0_IND[1:0] pins.	00	R/W
		0x0	Port indicators are off.		
		0x1	amber		
		0x2	green		
		0x3	undefined		

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Table 326. Port Status and Control register in device mode (PORTSC1_D - address 0x4000 6184) bit description

Bit	Symbol	Value	Description	Reset value	Access
19:16	PTC3_0		Port test control Any value other than 0000 indicates that the port is operating in test mode. The FORCE_ENABLE_FS and FORCE ENABLE_LS are extensions to the test mode support specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_HS/FS/LS values will force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. Values 0111 to 1111 are not valid.	0000	R/W
		0x0	TEST_MODE_DISABLE		
		0x1	J_STATE		
		0x2	K_STATE		
		0x3	SE0 (host)/NAK (device)		
		0x4	Packet		
		0x5	FORCE_ENABLE_HS		
		0x6	FORCE_ENABLE_FS		
20	-	-	Not used in device mode. This bit is always 0 in device mode.	0	-
21	-	-	Not used in device mode. This bit is always 0 in device mode.	0	-
22	-		Not used in device mode. This bit is always 0 in device mode.	0	-
23	PHCD		PHY low power suspend - clock disable (PLPSCD) In device mode, The PHY can be put into Low Power Suspend – Clock Disable when the device is not running (USBCMD Run/Stop = 0) or the host has signaled suspend (PORTSC SUSPEND = 1). Low power suspend will be cleared automatically when the host has signaled resume. Before forcing a resume from the device, the device controller driver must clear this bit.	0	R/W
		0	Writing a 0 enables the PHY clock. Reading a 0 indicates the status of the PHY clock (enabled).		
		1	Writing a 1 disables the PHY clock. Reading a 1 indicates the status of the PHY clock (disabled).		
24	PFSC		Port force full speed connect	0	R/W
		0	Port connects at any speed.		
		1	Writing this bit to a 1 will force the port to only connect at full speed. It disables the chirp sequence that allows the port to identify itself as High-speed. This is useful for testing FS configurations with a HS host, hub or device.		
25	-	-	reserved		
27:26	PSPD		Port speed This register field indicates the speed at which the port is operating.	0	RO
		0x0	Full-speed		
		0x1	invalid in device mode		
		0x2	High-speed		
31:28	-	-	Reserved	-	-

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20.6.15.2 Host mode

The host controller uses one port. The register is only reset when power is initially applied or in response to a controller reset. The initial conditions of the port are:

- No device connected
- Port disabled

If the port has power control, this state remains until software applies power to the port by setting port power to one in the PORTSC register.

Table 327. Port Status and Control register in host mode (PORTSC1_H - address 0x4000 6184) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	CCS		Current connect status This value reflects the current state of the port and may not correspond directly to the event that caused the CSC bit to be set. This bit is 0 if PP (Port Power bit) is 0. Software clears this bit by writing a 1 to it.	0	R/WC
		0	No device is present.		
		1	Device is present on the port.		
1	CSC		Connect status change Indicates a change has occurred in the port's Current Connect Status. The host/device controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be setting an already-set bit (i.e., the bit will remain set). Software clears this bit by writing a one to it. This bit is 0 if PP (Port Power bit) is 0	0	R/WC
		0	No change in current status.		
		1	Change in current status.		
2	PE		Port enable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by the host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled. downstream propagation of data is blocked except for reset. This bit is 0 if PP (Port Power bit) is 0.	0	R/W
		0	Port disabled.		
		1	Port enabled.		

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Table 327. Port Status and Control register in host mode (PORTSC1_H - address 0x4000 6184) bit description

Bit	Symbol	Value	Description	Reset value	Access
3	PEC		Port disable/enable change For the root hub, this bit gets set to a one only when a port is disabled due to disconnect on the port or due to the appropriate conditions existing at the EOF2 point (See *Chapter 11 of the USB Specification*). Software clears this by writing a one to it. This bit is 0 if PP (Port Power bit) is 0,	0	R/WC
		0	No change.		
		1	Port enabled/disabled status has changed.		
4	OCA		Over-current active This bit will automatically transition from 1 to 0 when the over-current condition is removed.	0	RO
		0	The port does not have an over-current condition.		
		1	The port has currently an over-current condition.		
5	OCC		Over-current change This bit gets set to one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.	0	R/WC
6	FPR		Force port resume Software sets this bit to one to drive resume signaling. The Host Controller sets this bit to one if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to one. This bit will automatically change to zero after the resume sequence is complete. This behavior is different from EHCI where the host controller driver is required to set this bit to a zero after the resume duration is timed in the driver. Note that when the Host controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed K) is driven on the port as long as this bit remains a one. This bit will remain a one until the port has switched to the high-speed idle. Writing a zero has no affect because the port controller will time the resume operation clear the bit the port control state switches to HS or FS idle. This bit is 0 if PP (Port Power bit) is 0.	0	R/W
		0	No resume (K-state) detected/driven on port.		
		1	Resume detected/driven on port.		

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Table 327. Port Status and Control register in host mode (PORTSC1_H - address 0x4000 6184) bit description

Bit	Symbol	Value	Description	Reset value	Access
7	SUSP		Suspend Together with the PE (Port enabled bit), this bit describes the port states, see Table 328. The host controller will unconditionally set this bit to zero when software sets the Force Port Resume bit to zero. The host controller ignores a write of zero to this bit. If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined. This bit is 0 if PP (Port Power bit) is 0.	0	R/W
		0	Port not in suspend state		
		1	Port in suspend state When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB.		
8	PR		Port reset When software writes a one to this bit the bus-reset sequence as defined in the USB Specification Revision 2.0 is started. This bit will automatically change to zero after the reset sequence is complete. This behavior is different from EHCI where the host controller driver is required to set this bit to a zero after the reset duration is timed in the driver. This bit is 0 if PP (Port Power bit) is 0.	0	R/W
		0	Port is not in the reset state.		
		1	Port is in the reset state.		
9	HSP		High-speed status	0	RO
		0	Host/device connected to the port is not in High-speed mode.		
		1	Host/device connected to the port is in High-speed mode.		
11:10	LS		Line status These bits reflect the current logical levels of the USB_DP and USB_DM signal lines. USB_DP corresponds to bit 11 and USB_DM to bit 10. In host mode, the use of linestate by the host controller driver is not necessary for this controller (unlike EHCI) because the controller hardware manages the connection of LS and FS.	0x3	RO
		0x0	SE0 (USB_DP and USB_DM LOW)		
		0x1	J-state (USB_DP HIGH and USB_DM LOW)		
		0x2	K-state (USB_DP LOW and USB_DM HIGH)		
		0x3	Undefined		

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Table 327. Port Status and Control register in host mode (PORTSC1_H - address 0x4000 6184) bit description

Bit	Symbol	Value	Description	Reset value	Access
12	PP	-	Port power control Host/OTG controller requires port power control switches. This bit represents the current setting of the switch (0=off, 1=on). When power is not available on a port (i.e. PP equals a 0), the port is non-functional and will not report attaches, detaches, etc. When an over-current condition is detected on a powered port and PPC is a one, the PP bit in each affected port may be transitioned by the host controller driver from a one to a zero (removing power from the port).	0	R/W
		0	Port power off.		
		1	Port power on.		
13	-	-	Reserved	0	-
15:14	PIC1_0		Port indicator control Writing to this field effects the value of the pins USB0_IND1 and USB0_IND0.	00	R/W
		0x0	Port indicators are off.		
		0x1	Amber		
		0x2	Green		
		0x3	Undefined		
19:16	PTC3_0		Port test control Any value other than 0000 indicates that the port is operating in test mode. The FORCE_ENABLE_FS and FORCE ENABLE_LS are extensions to the test mode support specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values will force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. Values 0x8 to 0xF are reserved.	0000	R/W
		0x0	TEST_MODE_DISABLE		
		0x1	J_STATE		
		0x2	K_STATE		
		0x3	SE0 (host)/NAK (device)		
		0x4	Packet		
		0x5	FORCE_ENABLE_HS		
		0x6	FORCE_ENABLE_FS		
		0x7	FORCE_ENABLE_LS		
20	WKCN		Wake on connect enable (WKCNNT_E) This bit is 0 if PP (Port Power bit) is 0	0	R/W
		0	Disables the port to wake up on device connects.		
		1	Writing this bit to a one enables the port to be sensitive to device connects as wake-up events.		
21	WKDC		Wake on disconnect enable (WKDSCNNT_E) This bit is 0 if PP (Port Power bit) is 0.	0	R/W
		0	Disables the port to wake up on device disconnects.		
		1	Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events.		

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Table 327. Port Status and Control register in host mode (PORTSC1_H - address 0x4000 6184) bit description

Bit	Symbol	Value	Description	Reset value	Access
22	WKOC		Wake on over-current enable (WKOC_E)	0	R/W
		0	Disables the port to wake up on over-current events.		
		1	Writing a one to this bit enabled the port to be sensitive to over-current conditions as wake-up events.		
23	PHCD		PHY low power suspend - clock disable (PLPSCD) In host mode, the PHY can be put into Low Power Suspend – Clock Disable when the downstream device has been put into suspend mode or when no downstream device is connected. Low power suspend is completely under the control of software.	0	R/W
		0	Writing a 0 enables the PHY clock. Reading a 0 indicates the status of the PHY clock (enabled).		
		1	Writing a 1 disables the PHY clock. Reading a 1 indicates the status of the PHY clock (disabled).		
24	PFSC		Port force full speed connect	0	R/W
		0	Port connects at any speed.		
		1	Writing this bit to a 1 will force the port to only connect at Full Speed. It disables the chirp sequence that allows the port to identify itself as High Speed. This is useful for testing FS configurations with a HS host, hub or device.		
25	-	-	Reserved		
27:26	PSPD		Port speed This register field indicates the speed at which the port is operating. For HS mode operation in the host controller and HS/FS operation in the device controller the port routing steers data to the Protocol engine. For FS and LS mode operation in the host controller, the port routing steers data to the Protocol Engine w/ Embedded Transaction Translator.	0	RO
		0x0	Full-speed		
		0x1	Low-speed		
		0x2	High-speed		
31:28	-		Reserved	-	-

Table 328. Port states as described by the PE and SUSP bits in the PORTSC1 register

PE bit	SUSP bit	Port state
0	0 or 1	disabled
1	0	enabled
1	1	suspend

20.6.16 OTG Status and Control register (OTGSC)

The OTG register has four sections:

- OTG interrupt enables (R/W)
- OTG Interrupt status (R/WC)
- OTG status inputs (RO)
- OTG controls (R/W)

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The status inputs are debounced using a 1 msec time constant. Values on the status inputs that do not persist for more than 1 msec will not cause an update of the status input register or cause an OTG interrupt.

Table 329. OTG Status and Control register (OTGSC - address 0x4000 61A4) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	VD		VBUS_Discharge Setting this bit to 1 causes VBUS to discharge through a resistor.	0	R/W
1	VC		VBUS_Charge Setting this bit to 1 causes the VBUS line to be charged. This is used for VBUS pulsing during SRP.	0	R/W
2	HAAR		Hardware assist auto_reset	0	R/W
		0	Disabled		
		1	Enable automatic reset after connect on host port.		
3	OT		OTG termination This bit must be set to 1 when the OTG controller is in device mode. This controls the pull-down on USB_DM.	0	R/W
4	DP		Data pulsing Setting this bit to 1 causes the pull-up on USB_DP to be asserted for data pulsing during SRP.	0	R/W
5	IDPU		ID pull-up. This bit provides control over the pull-up resistor.	1	R/W
		0	Pull-up off. The ID bit will not be sampled.		
		1	Pull-up on.		
6	HADP		Hardware assist data pulse Write a 1 to start data pulse sequence.	0	R/W
7	HABA		Hardware assist B-disconnect to A-connect	0	R/W
		0	Disabled.		
		1	Enable automatic B-disconnect to A-connect sequence.		
8	ID		USB ID	0	RO
		0	A-device		
		1	B-device		
9	AVV		A-VBUS valid Reading 1 indicates that VBUS is above the A-VBUS valid threshold.	0	RO
10	ASV		A-session valid Reading 1 indicates that VBUS is above the A-session valid threshold.	0	RO
11	BSV		B-session valid Reading 1 indicates that VBUS is above the B-session valid threshold.	0	RO
12	BSE		B-session end Reading 1 indicates that VBUS is below the B-session end threshold.	0	RO
13	MS1T		1 millisecond timer toggle This bit toggles once per millisecond.	0	RO
14	DPS		Data bus pulsing status Reading a 1 indicates that data bus pulsing is detected on the port.	0	RO
15	-	-	reserved	0	

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Table 329. OTG Status and Control register (OTGSC - address 0x4000 61A4) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
16	IDIS		USB ID interrupt status This bit is set when a change on the ID input has been detected. Software must write a 1 to this bit to clear it.	0	R/WC
17	AVVIS		A-VBUS valid interrupt status This bit is set then VBUS has either risen above or fallen below the A-VBUS valid threshold (4.4 V on an A-device). Software must write a 1 to this bit to clear it.	0	R/WC
18	ASVIS		A-Session valid interrupt status This bit is set then VBUS has either risen above or fallen below the A-session valid threshold (0.8 V). Software must write a 1 to this bit to clear it.	0	R/WC
19	BSVIS		B-Session valid interrupt status This bit is set then VBUS has either risen above or fallen below the B-session valid threshold (0.8 V). Software must write a 1 to this bit to clear it.	0	R/WC
20	BSEIS		B-Session end interrupt status This bit is set then VBUS has fallen below the B-session end threshold. Software must write a 1 to this bit to clear it.	0	R/WC
21	ms1S		1 millisecond timer interrupt status This bit is set once every millisecond. Software must write a 1 to this bit to clear it.	0	R/WC
22	DPIS		Data pulse interrupt status This bit is set when data bus pulsing occurs on DP or DM. Data bus pulsing is only detected when the CM bit in USBMODE = Host (11) and the PortPower bit in PORTSC = Off (0). Software must write a 1 to this bit to clear it.	0	R/WC
23	-	-	reserved	0	
24	IDIE		USB ID interrupt enable Setting this bit enables the interrupt. Writing a 0 disables the interrupt.	0	R/W
25	AVVIE		A-VBUS valid interrupt enable Setting this bit enables the A-VBUS valid interrupt. Writing a 0 disables the interrupt.	0	R/W
26	ASVIE		A-session valid interrupt enable Setting this bit enables the A-session valid interrupt. Writing a 0 disables the interrupt	0	R/W
27	BSVIE		B-session valid interrupt enable Setting this bit enables the B-session valid interrupt. Writing a 0 disables the interrupt.	0	R/W
28	BSEIE		B-session end interrupt enable Setting this bit enables the B-session end interrupt. Writing a 0 disables the interrupt.	0	R/W

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Table 329. OTG Status and Control register (OTGSC - address 0x4000 61A4) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
29	MS1E		1 millisecond timer interrupt enable Setting this bit enables the 1 millisecond timer interrupt. Writing a 0 disables the interrupt.	0	R/W
30	DPIE		Data pulse interrupt enable Setting this bit enables the data pulse interrupt. Writing a 0 disables the interrupt	0	R/W
31	-	-	Reserved	0	-

20.6.17 USB Mode register (USBMODE)

The USBMODE register sets the USB mode for the OTG controller. The possible modes are Device, Host, and Idle mode for OTG operations.

20.6.17.1 Device mode

Table 330. USB Mode register in device mode (USBMODE_D - address 0x4000 61A8) bit description

Bit	Symbol	Value	Description	Reset value	Access
1:0	CM1_0		Controller mode The controller defaults to an idle state and needs to be initialized to the desired operating mode after reset. This register can only be written once after reset. If it is necessary to switch modes, software must reset the controller by writing to the RESET bit in the USBCMD register before reprogramming this register.	00	R/ WO
		0x0	Idle		
		0x1	Reserved		
		0x2	Device controller		
		0x3	Host controller		
2	ES		Endian select This bit can change the byte ordering of the transfer buffers to match the host microprocessor bus architecture. The bit fields in the microprocessor interface and the DMA data structures (including the setup buffer within the device QH) are unaffected by the value of this bit, because they are based upon 32-bit words.	0	R/W
		0	Little endian: first byte referenced in least significant byte of 32-bit word.		
		1	Big endian: first byte referenced in most significant byte of 32-bit word.		
3	SLOM		Setup Lockout mode In device mode, this bit controls behavior of the setup lock mechanism. See Section 20.10.8.	0	R/W
		0	Setup Lockouts on		
		1	Setup Lockouts Off (DCD requires the use of Setup Buffer Tripwire in USBCMD)		

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Table 330. USB Mode register in device mode (USBMODE_D - address 0x4000 61A8) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
4	SDIS		Stream disable mode **Remark:** The use of this feature substantially limits the overall USB performance that can be achieved.	0	R/W
		0	Not disabled		
		1	Disabled. Setting this bit to one disables double priming on both RX and TX for low bandwidth systems. This mode ensures that when the RX and TX buffers are sufficient to contain an entire packet that the standard double buffering scheme is disabled to prevent overruns/underruns in bandwidth limited systems. Note: In High Speed Mode, all packets received will be responded to with a NYET handshake when stream disable is active.		
5	-		Not used in device mode.	0	-
31:6	-	-	reserved		

20.6.17.2 Host mode

Table 331. USB Mode register in host mode (USBMODE_H - address 0x4000 61A8) bit description

Bit	Symbol	Value	Description	Reset value	Access
1:0	CM		Controller mode The controller defaults to an idle state and needs to be initialized to the desired operating mode after reset. This register can only be written once after reset. If it is necessary to switch modes, software must reset the controller by writing to the RESET bit in the USBCMD register before reprogramming this register.	00	R/ WO
		0x0	Idle		
		0x1	Reserved		
		0x2	Device controller		
		0x3	Host controller		
2	ES		Endian select This bit can change the byte ordering of the transfer buffers. The bit fields in the microprocessor interface and the DMA data structures (including the setup buffer within the device QH) are unaffected by the value of this bit, because they are based upon 32-bit words.	0	R/W
		0	Little endian: first byte referenced in least significant byte of 32-bit word.		
		1	Big endian: first byte referenced in most significant byte of 32-bit word.		
3	-		Not used in host mode	0	-

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Table 331. USB Mode register in host mode (USBMODE_H - address 0x4000 61A8) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
4	SDIS		Stream disable mode **Remark:** The use of this feature substantially limits the overall USB performance that can be achieved.	0	R/W
		0	Not disabled		
		1	Disabled. Setting to a ‘1’ ensures that overruns/underruns of the latency FIFO are eliminated for low bandwidth systems where the RX and TX buffers are sufficient to contain the entire packet. Enabling stream disable also has the effect of ensuring the the TX latency is filled to capacity before the packet is launched onto the USB. Note: Time duration to pre-fill the FIFO becomes significant when stream disable is active. See TXFILLTUNING to characterize the adjustments needed for the scheduler when using this feature.		
5	VBPS		VBUS power select	0	R/WO
		0	vbus_pwr_select is set LOW.		
		1	vbus_pwr_select is set HIGH		
31:6	-	-	reserved	-	-

20.6.18 USB Endpoint Setup Status register (ENDPSETUPSTAT)

Table 332. USB Endpoint Setup Status register (ENDPTSETUPSTAT - address 0x4000 61AC) bit description

Bit	Symbol	Description	Reset value	Access
5:0	ENDPTSET UPSTAT	Setup endpoint status for logical endpoints 0 to 5. For every setup transaction that is received, a corresponding bit in this register is set to one. Software must clear or acknowledge the setup transfer by writing a one to a respective bit after it has read the setup data from Queue head. The response to a setup packet as in the order of operations and total response time is crucial to limit bus time outs while the setup lockout mechanism is engaged.	0	R/WC
31:6	-	reserved	-	-

20.6.19 USB Endpoint Prime register (ENDPTPRIME)

For each endpoint, software should write a one to the corresponding bit whenever posting a new transfer descriptor to an endpoint. Hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a receive buffer. Hardware will clear this bit when the associated endpoint(s) is (are) successfully primed.

Remark: These bits will be momentarily set by hardware during hardware endpoint re-priming operations when a dTD is retired and the dQH is updated.

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Table 333. USB Endpoint Prime register (ENDPTPRIME - address 0x4000 61B0) bit description

Bit	Symbol	Description	Reset value	Access
5:0	PERB	Prime endpoint receive buffer for physical OUT endpoints 5 to 0. For each OUT endpoint, a corresponding bit is set to 1 by software to request a buffer be prepared for a receive operation for when a USB host initiates a USB OUT transaction. Software should write a one to the corresponding bit whenever posting a new transfer descriptor to an endpoint. Hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a receive buffer. Hardware will clear this bit when the associated endpoint(s) is (are) successfully primed. PERB0 = endpoint 0 ... PERB5 = endpoint 5	0	R/WS
15:6	-	reserved	-	-
21:16	PETB	Prime endpoint transmit buffer for physical IN endpoints 5 to 0. For each IN endpoint a corresponding bit is set to one by software to request a buffer be prepared for a transmit operation in order to respond to a USB IN/INTERRUPT transaction. Software should write a one to the corresponding bit when posting a new transfer descriptor to an endpoint. Hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a transmit buffer. Hardware will clear this bit when the associated endpoint(s) is (are) successfully primed. PETB0 = endpoint 0 ... PETB5 = endpoint 5	0	R/WS
31:22	-	reserved	-	-

20.6.20 USB Endpoint Flush register (ENDPTFLUSH)

Writing a one to a bit(s) in this register will cause the associated endpoint(s) to clear any primed buffers. If a packet is in progress for one of the associated endpoints, then that transfer will continue until completion. Hardware will clear this register after the endpoint flush operation is successful.

Table 334. USB Endpoint Flush register (ENDPTFLUSH - address 0x4000 61B4) bit description

Bit	Symbol	Description	Reset value	Access
5:0	FERB	Flush endpoint receive buffer for physical OUT endpoints 5 to 0. Writing a one to a bit(s) will clear any primed buffers. FERB0 = endpoint 0 ... FERB5 = endpoint 5	0	R/WS

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Table 334. USB Endpoint Flush register (ENDPTFLUSH - address 0x4000 61B4) bit description

Bit	Symbol	Description	Reset value	Access
15:6	-	reserved	-	-
21:16	FETB	Flush endpoint transmit buffer for physical IN endpoints 5 to 0. Writing a one to a bit(s) will clear any primed buffers. FETB0 = endpoint 0 ... FETB5 = endpoint 5	0	R/WS
31:22	-	reserved	-	-

20.6.21 USB Endpoint Status register (ENDPTSTAT)

One bit for each endpoint indicates status of the respective endpoint buffer. This bit is set by hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. There will always be a delay between setting a bit in the ENDPTPRIME register and endpoint indicating ready. This delay time varies based upon the current USB traffic and the number of bits set in the ENDPTPRIME register. Buffer ready is cleared by USB reset, by the USB DMA system, or through the ENDPTFLUSH register.

Remark: These bits will be momentarily cleared by hardware during hardware endpoint re-priming operations when a dTD is retired and the dQH is updated.

Table 335. USB Endpoint Status register (ENDPTSTAT - address 0x4000 61B8) bit description

Bit	Symbol	Description	Reset value	Access
5:0	ERBR	Endpoint receive buffer ready for physical OUT endpoints 5 to 0. This bit is set to 1 by hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. ERBR0 = endpoint 0 ... ERBR5 = endpoint 5	0	RO
15:6	-	reserved	-	-
21:16	ETBR	Endpoint transmit buffer ready for physical IN endpoints 3 to 0. This bit is set to 1 by hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. ETBR0 = endpoint 0 ... ETBR5 = endpoint 5	0	RO
31:22	-	reserved	-	-

20.6.22 USB Endpoint Complete register (ENDPTCOMPLETE)

Each bit in this register indicates that a received/transmit event occurred and software should read the corresponding endpoint queue to determine the transfer status. If the corresponding IOC bit is set in the Transfer Descriptor, then this bit will be set simultaneously with the USBINT.

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Writing a one will clear the corresponding bit in this register.

Table 336. USB Endpoint Complete register (ENDPTCOMPLETE - address 0x4000 61BC) bit description

Bit	Symbol	Description	Reset value	Access
5:0	ERCE	Endpoint receive complete event for physical OUT endpoints 5 to 0. This bit is set to 1 by hardware when receive event (OUT/SETUP) occurred. ERCE0 = endpoint 0 ... ERCE5 = endpoint 5	0	R/WC
15:6	-	reserved	-	-
21:16	ETCE	Endpoint transmit complete event for physical IN endpoints 5 to 0. This bit is set to 1 by hardware when a transmit event (IN/INTERRUPT) occurred. ETCE0 = endpoint 0 ... ETCE5 = endpoint 5	0	R/WC
31:21	-	reserved	-	-

20.6.23 USB Endpoint 0 Control register (ENDPTCTRL0)

This register initializes endpoint 0 for control transfer. Endpoint 0 is always a control endpoint.

Table 337. USB Endpoint 0 Control register (ENDPTCTRL0 - address 0x4000 61C0) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	RXS		Rx endpoint stall	0	R/W
		0	Endpoint ok.		
		1	Endpoint stalled Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It will continue returning STALL until the bit is cleared by software, or it will automatically be cleared upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared by hardware until the associated ENDSETUPSTAT bit is cleared.[1]		
1	-	-	reserved		
3:2	RXT1_0		Endpoint type Endpoint 0 is always a control endpoint.	00	R/W
6:4	-	-	reserved	-	-
7	RXE		Rx endpoint enable Endpoint enabled. Control endpoint 0 is always enabled. This bit is always 1.	1	RO
15:8	-	-	reserved	-	-

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Table 337. USB Endpoint 0 Control register (ENDPTCTRL0 - address 0x4000 61C0) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
16	TXS		Tx endpoint stall		R/W
		0	Endpoint ok.		
		1	Endpoint stalled Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It will continue returning STALL until the bit is cleared by software, or it will automatically be cleared upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared by hardware until the associated ENDSETUPSTAT bit is cleared.[1]		
17	-	-	reserved		
19:18	TXT1_0		Endpoint type Endpoint 0 is always a control endpoint.	00	RO
22:20	-	-	reserved		
23	TXE		Tx endpoint enable Endpoint enabled. Control endpoint 0 is always enabled. This bit is always 1.	1	RO
31:24	-	-	reserved		

[1] There is a slight delay (50 clocks max) between the ENPTSETUPSTAT being cleared and hardware continuing to clear this bit. In most systems it is unlikely that the DCD software will observe this delay. However, should the DCD notice that the stall bit is not set after writing a one to it, software should continually write this stall bit until it is set or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.

20.6.24 Endpoint 1 to 5 control registers

Each endpoint that is not a control endpoint has its own register to set the endpoint type and enable or disable the endpoint.

Remark: The reset value for all endpoint types is the control endpoint. If one endpoint direction is enabled and the paired endpoint of opposite direction is disabled, then the endpoint type of the unused direction must be changed from the control type to any other type (e.g. bulk). Leaving an unconfigured endpoint control will cause undefined behavior for the data PID tracking on the active endpoint.

Table 338. USB Endpoint 1 to 5 control registers (ENDPTCTRL - address 0x4000 61C4 (ENDPTCTRL1) to 0x4000 61D4 (ENDPTCTRL5)) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	RXS		Rx endpoint stall	0	R/W
		0	Endpoint ok. This bit will be cleared automatically upon receipt of a SETUP request if this Endpoint is configured as a Control Endpoint and this bit will continue to be cleared by hardware until the associated ENDPTSETUPSTAT bit is cleared.		
		1	Endpoint stalled Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It will continue returning STALL until the bit is cleared by software, or it will automatically be cleared upon receipt of a new SETUP request.		

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Table 338. USB Endpoint 1 to 5 control registers (ENDPTCTRL - address 0x4000 61C4 (ENDPTCTRL1) to 0x4000 61D4 (ENDPTCTRL5)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
1	-		Reserved	0	R/W
3:2	RXT		Endpoint type	00	R/W
		0x0	Control		
		0x1	Isochronous		
		0x2	Bulk		
		0x3	Reserved		
4	-	-	Reserved		
5	RXI		Rx data toggle inhibit This bit is only used for test and should always be written as zero. Writing a one to this bit will cause this endpoint to ignore the data toggle sequence and always accept data packets regardless of their data PID.	0	R/W
		0	Disabled		
		1	Enabled		
6	RXR		Rx data toggle reset Write 1 to reset the PID sequence. Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PIDs between the host and device.	0	WS
7	RXE		Rx endpoint enable **Remark:** An endpoint should be enabled only after it has been configured.	0	R/W
		0	Endpoint disabled.		
		1	Endpoint enabled.		
15:8	-	-	reserved		
16	TXS		Tx endpoint stall	0	R/W
		0	Endpoint ok. This bit will be cleared automatically upon receipt of a SETUP request if this Endpoint is configured as a Control Endpoint, and this bit will continue to be cleared by hardware until the associated ENDPTSETUPSTAT bit is cleared.		
		1	Endpoint stalled Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It will continue returning STALL until the bit is cleared by software, or it will automatically be cleared upon receipt of a new SETUP request.		
17	-	-	Reserved	0	-
19:18	TXT1_0		Tx endpoint type	00	R/W
		0x0	Control		
		0x1	Isochronous		
		0x2	Bulk		
		0x3	Interrupt		
20	-	-	reserved		

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Table 338. USB Endpoint 1 to 5 control registers (ENDPTCTRL - address 0x4000 61C4 (ENDPTCTRL1) to 0x4000 61D4 (ENDPTCTRL5)) bit description *...continued*

Bit	Symbol	Value	Description	Reset value	Access
21	TXI		Tx data toggle inhibit This bit is only used for test and should always be written as zero. Writing a one to this bit will cause this endpoint to ignore the data toggle sequence and always accept data packets regardless of their data PID.	0	R/W
		0	Enabled		
		1	Disabled		
22	TXR		Tx data toggle reset Write 1 to reset the PID sequence. Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the host and device.	1	WS
23	TXE		Tx endpoint enable **Remark:** An endpoint should be enabled only after it has been configured	0	R/W
		0	Endpoint disabled.		
		1	Endpoint enabled.		
31:24	-	-	reserved	0	

20.7 Functional description

20.7.1 OTG core

The OTG core forms the main digital part of the USB-OTG. See the *USB EHCI specification* for details about this core.

20.7.2 Host data structures

See *Chapter 4 of Enhanced Host Controller Interface Specification for Universal Serial Bus 1.0.*

20.7.3 Host operational model

See *Chapter 3 of Enhanced Host Controller Interface Specification for Universal Serial Bus 1.0*.

20.7.4 ATX_RGEN module

There are a number of requirements for the reset signal towards the ATX transceiver, these are as follows:

- it requires the clocks to be running for a reset to occur correctly.
- it must see a rising edge of reset to correctly reset the clock generation module.
- the reset must be a minimum of 133 ns (4 $\times$ 30 MHz clock cycles) in duration to reset all logic correctly.

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The ATX_RGEN module generates a reset signal towards the ATX fulfilling above 3 requirements, no matter how the AHB reset looks like.

20.7.5 ATX transceiver

The USB-OTG has a USB transceiver with UTMI+ interface. It contains the required transceiver OTG functionality; this includes:

- VBUS sensing for producing the session-valid and VBUS-valid signals.
- sampling of the USB_ID input for detection of A-device or B-device connection.
- charging and discharging of VBUS for starting and ending a session as B-device.

20.7.6 Modes of operation

In general, the USB-OTG can be operating either in host mode or in device mode. Software must put the core in the appropriate mode by setting the USBMODE.CM field (‘11’ for host mode, ‘10’ for device mode).

The USBMODE.CM field can also be equal to ‘00’, which means that the core is in idle mode (neither host nor device mode). This will happen after the following:

- a hardware reset.
- a software reset via the USBCMD.RST bit; e.g. when switching from host mode to device mode as part of the HNP protocol (or vice versa), software must issue a software reset by which the core will be to the idle state; this will happen in a time frame dependent on the software.

20.7.7 SOF/VF indicator

The USB-OTG generates a SOF/VF indicator signal, which can be used by user specific external logic.

In FS mode, the SOF/VF indicator signal has a frequency equal to the frame frequency, which is about 1 kHz. The signal is high for half of the frame period and low for the other half of the frame period. The positive edge is aligned with the start of a frame (= SOF).

In HS mode, the SOF/VF indicator signal has a frequency equal to the virtual frame frequency. The signal is high for half of the virtual frame period and low for the other half of the virtual frame period. The positive edge is aligned with the start of a virtual frame (= VF).

The length of the virtual frame is defined as: VF = microframe $\times$ $2^{\mathrm{bInterval}}$;

bInterval is specified in the 4-bit programmable BINTERVAL.BINT register field. The minimum value of bInterval is 0, the maximum value is 15.

In suspend mode the SOF/VF indicator signal is turned off (= remains low).

20.7.8 Hardware assist

The hardware assist provides automated response and sequencing that may not be possible in software if there are significant interrupt latency response times. The use of this additional circuitry is optional and can be used to assist the following three state transitions by setting the appropriate bits in the OTGSC register:

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- Auto reset (set bit HAAR).
- Data pulse (set bit HADP).
- B-disconnect to A-connect (set bit HABA).

20.7.8.1 Auto reset

When the HAAR in the OTGSC register is set to one, the host will automatically start a reset after a connect event. This shortcuts the normal process where software is notified of the connect event and starts the reset. Software will still receive notification of the connect event (CCS bit in the PORTSC register) but should not write the reset bit in the USBCMD register when the HAAR is set. Software will be notified again after the reset is complete via the enable change bit in the PORTSC register which causes a port change interrupt.

This assist will ensure the OTG parameter TB_ACON_BSE0_MAX = 1 ms is met (see *OTG specification* for an explanation of the OTG timing requirements).

20.7.8.2 Data pulse

Writing a one to HADP in the OTGSC register will start a data pulse of approximately 7 ms in duration and then automatically cease the data pulsing. During the data pulse, the DP bit will be set and then cleared. This automation relieves software from accurately controlling the data-pulse duration. During the data pulse, the HCD can poll to see that the HADP and DP bit have returned low to recognize the completion, or the HCD can simply launch the data pulse and wait to see if a VBUS Valid interrupt occurs when the A-side supplies bus power.

This assist will ensure data pulsing meets the OTG requirement of > 5 ms and < 10 ms.

20.7.8.3 B-disconnect to A-connect (Transition to the A-peripheral state)

During HNP, the B-disconnect occurs from the OTG A_suspend state, and within 3 ms, the A-device must enable the pull-up on the DP leg in the A-peripheral state. For the hardware assist to begin the following conditions must be met:

- HABA is set.
- Host controller is in suspend mode.
- Device is disconnecting.

The hardware assist consists of the following steps:

1. Hardware resets the OTG controller (writes 1 to the RST bit in USBCMD).
2. Hardware selects the device mode (writes 10 to bits CM[1:0] in USBMODE).
3. Hardware sets the RS bit in USBCMD and enables the necessary interrupts:
   – USB reset enable (URE) - enables interrupt on USB bus reset to device.
   – Sleep enable (SLE) - enables interrupt on device suspend.
   – Port change detect enable (PCE) - enables interrupt on device connect.

When software has enabled this hardware assist, it must not interfere during the transition and should not write any register in the OTG core until it gets an interrupt from the device controller signifying that a reset interrupt has occurred or until it has verified that the core has entered device mode. HCD/DCD must not activate the core soft reset at any time

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since this action is performed by hardware. During the transition, the software may see an interrupt from the disconnect and/or other spurious interrupts (i.e. SOF/etc.) that may or may not cascade and my be cleared by the soft reset depending on the software response time.

After the core has entered device mode with help of the hardware assist, the DCD must ensure that the ENDPTLISTADDR is programmed properly before the host sends a setup packet. Since the end of the reset duration, which may be initiated quickly (a few microseconds) after connect, will require at a minimum 50 ms, this is the time for which the DCD must be ready to accept setup packets after having received notification that the reset has been detected or simply that the OTG is in device mode which ever occurs first.

If the A-peripheral fails to see a reset after the controller enters device mode and engages the D+-pull-up, the device controller interrupts the DCD signifying that a suspend has occurred. This assist will ensure the parameter TA_BDIS_ACON_MAX = 3ms is met.

20.8 Deviations from EHCI standard

For the purposes of a dual-role Host/Device controller with support for On-The-Go applications, it is necessary to deviate from the EHCI specification. Device operation and On-The-Go operation is not specified in the EHCI and thus the implementation supported in this core is specific to the LPC18xx. The host mode operation of the core is near EHCI compatible with few minor differences documented in this section.

The particulars of the deviations occur in the areas summarized here:

- Embedded Transaction Translator – Allows direct attachment of FS and LS devices in host mode without the need for a companion controller.
- Device operation - In host mode the device operational registers are generally disabled and thus device mode is mostly transparent when in host mode. However, there are a couple exceptions documented in the following sections.
- On-The-Go Operation - This design includes an On-The-Go controller.

20.8.1 Embedded Transaction Translator function

The USB-HS OTG controller supports directly connected full and low speed devices without requiring a companion controller by including the capabilities of a USB 2.0 high speed hub transaction translator. Although there is no separate Transaction Translator block in the system, the transaction translator function normally associated with a high speed hub has been implemented within the DMA and Protocol engine blocks. The embedded transaction translator function is an extension to EHCI interface but makes use of the standard data structures and operational models that exist in the EHCI specification to support full and low speed devices.

20.8.1.1 Capability registers

The following items have been added to the capability registers to support the embedded Transaction Translator Function:

- N_TT bits added to HCSPARAMS – Host Control Structural Parameters (see Table 302).
- N_PTT added to HCSPARAMS – Host Control Structural Parameters (see Table 302).

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20.8.1.2 Operational registers

The following items have been added to the operational registers to support the embedded TT:

- New register TTCTRL (see Section 20.6.9).
- Two-bit Port Speed (PSPD) bits added to the PORTSC1 register (see Section 20.6.15).

20.8.1.3 Discovery

In a standard EHCI controller design, the EHCI host controller driver detects a Full speed (FS) or Low speed (LS) device by noting if the port enable bit is set after the port reset operation. The port enable will only be set in a standard EHCI controller implementation after the port reset operation and when the host and device negotiate a High-Speed connection (i.e. Chirp completes successfully). Since this controller has an embedded Transaction Translator, the port enable will always be set after the port reset operation regardless of the result of the host device chirp result and the resulting port speed will be indicated by the PSPD field in PORTSC1 (see Section 20.6.15).

Table 339. Handling of directly connected full-speed and low-speed devices

Standard EHCI model	EHCI with embedded Transaction Translator
After the port enable bit is set following a connection and reset sequence, the device/hub is assumed to be HS.	After the port enable bit is set following a connection and reset sequence, the device/hub speed is noted from PORTSC1.
FS and LS devices are assumed to be downstream from a HS hub thus, all port-level control is performed through the Hub Class to the nearest Hub.	FS and LS device can be either downstream from a HS hub or directly attached. When the FS/LS device is downstream from a HS hub, then port-level control is done using the Hub Class through the nearest Hub. When a FS/LS device is directly attached, then port-level control is accomplished using PORTSC1.
FS and LS devices are assumed to be downstream from a HS hub with HubAddr=X, where HubAddr > 0 and HubAddr is the address of the Hub where the bus transitions from HS to FS/LS (i.e. Split target hub).	FS and LS device can be either downstream from a HS hub with HubAddr = X [HubAddr > 0] or directly attached, where HubAddr = TTHA (TTHA is programmable and defaults to 0) and HubAddr is the address of the Root Hub where the bus transitions from HS to FS/LS (i.e. Split target hub is the root hub).

20.8.1.4 Data structures

The same data structures used for FS/LS transactions though a HS hub are also used for transactions through the Root Hub with sm embedded Transaction Translator. Here it is demonstrated how the Hub Address and Endpoint Speed fields should be set for directly attached FS/LS devices and hubs:

1. QH (for direct attach FS/LS) – Async. (Bulk/Control Endpoints) Periodic (Interrupt)
   - Hub Address = TTHA (default TTHA = 0)
   - Transactions to direct attached device/hub: QH.EPS = Port Speed
   - Transactions to a device downstream from direct attached FS hub: QH.EPS = Downstream Device Speed

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Remark: When QH.EPS = 01 (LS) and PORTSCx.PSPD = 00 (FS), a LS-pre-pid will be sent before the transmitting LS traffic.

Maximum Packet Size must be less than or equal 64 or undefined behavior may result.

2. siTD (for direct attach FS) – Periodic (ISO Endpoint)

   all FS ISO transactions:

   Hub Address = (default TTHA = 0)

   siTD.EPS = 00 (full speed)

   Maximum Packet Size must less than or equal to 1023 or undefined behavior may result.

20.8.1.5 Operational model

The operational models are well defined for the behavior of the Transaction Translator (see USB 2.0 specification) and for the EHCI controller moving packets between system memory and a USB-HS hub. Since the embedded Transaction Translator exists within the host controller there is no physical bus between EHCI host controller driver and the USB FS/LS bus. These sections will briefly discuss the operational model for how the EHCI and Transaction Translator operational models are combined without the physical bus between. The following sections assume the reader is familiar with both the EHCI and USB 2.0 Transaction Translator operational models.

20.8.1.5.1 Micro-frame pipeline

The EHCI operational model uses the concept of H-frames and B-frames to describe the pipeline between the Host (H) and the Bus (B). The embedded Transaction Translator shall use the same pipeline algorithms specified in the USB 2.0 specification for a Hub-based Transaction Translator.

It is important to note that when programming the S-mask and C-masks in the EHCI data structures to schedule periodic transfers for the embedded Transaction Translator, the EHCI host controller driver must follow the same rules specified in EHCI for programming the S-mask and C-mask for downstream Hub-based Transaction Translators. Once periodic transfers are exhausted, any stored asynchronous transfer will be moved. Asynchronous transfers are opportunistic in that they shall execute whenever possible and their operation is not tied to H-frame and B-frame boundaries with the exception that an asynchronous transfer can not babble through the SOF (start of B-frame 0.)

20.8.1.6 Split state machines

The start and complete split operational model differs from EHCI slightly because there is no bus medium between the EHCI controller and the embedded Transaction Translator. Where a start or complete-split operation would occur by requesting the split to the HS hub, the start/complete split operation is simple an internal operation to the embedded Transaction Translator. The following table summarizes the conditions where handshakes are emulated from internal state instead of actual handshakes to HS split bus traffic.

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Table 340. Split state machine properties

	Condition	Emulate TT response
Start-split	All asynchronous buffers full.	NAK
	All periodic buffers full.	ERR
	Success for start of Async. Transaction.	ACK
	Start Periodic Transaction.	No Handshake (Ok)
Complete-split	Failed to find transaction in queue.	Bus Time Out
	Transaction in Queue is Busy.	NYET
	Transaction in Queue is Complete.	[Actual Handshake from LS/FS device]

20.8.1.7 Asynchronous Transaction scheduling and buffer management

The following USB 2.0 specification items are implemented in the embedded Transaction Translator:

1. *USB 2.0 specification, section 11.17.3*: Sequencing is provided & a packet length estimator ensures no full-speed/low-speed packet babbles into SOF time.
2. *USB 2.0 specification, section 11.17.4*: Transaction tracking for 2 data pipes.
3. *USB 2.0 specification, section 11.17.5*: Clear_TT_Buffer capability provided though the use of the TTCTRL register.

20.8.1.8 Periodic Transaction scheduling and buffer management

The following USB 2.0 specification items are implemented in the embedded Transaction Translator:

1. *USB 2.0 specs, section 11.18.6.[1-2]*:
   - Abort of pending start-splits:

     EOF (and not started in micro-frames 6)

     Idle for more than 4 micro-frames
   - Abort of pending complete-splits:

     EOF

     Idle for more than 4 micro-frames
2. *USB 2.0 specs, section 11.18.6.[7-8]*:
   - Transaction tracking for up to 16 data pipes:

     Some applications may not require transaction tracking up to a maximum of 16 periodic data pipes. The option to limit the tracking to only 4 periodic data pipes exists in the by changing the configuration constant VUSB_HS_TT_PERIODIC_CONTEXTS to 4. The result is a significant gate count savings to the core given the limitations implied.

     Remark: Limiting the number of tracking pipes in the EMBedded TT to four (4) will impose the restriction that no more than 4 periodic transactions (INTERRUPT/ISOCHRONOUS) can be scheduled through the embedded TT per frame. The number 16 was chosen in the USB specification because it is sufficient to ensure that the high-speed to full- speed periodic pipeline can remain full.

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keeping the pipeline full puts no constraint on the number of periodic transactions that can be scheduled in a frame and the only limit becomes the flight time of the packets on the bus.

– Complete-split transaction searching:

There is no data schedule mechanism for these transactions other than micro-frame pipeline. The embedded TT assumes the number of packets scheduled in a frame does not exceed the frame duration (1 ms) or else undefined behavior may result.

20.8.1.9 Multiple Transaction Translators

The maximum number of embedded Transaction Translators that is currently supported is one as indicated by the N_TT field in the HCSPARAMS – Host Control Structural Parameters register.

20.8.2 Device operation

The co-existence of a device operational controller within the host controller has little effect on EHCI compatibility for host operation except as noted in this section.

20.8.2.1 USBMODE register

Given that the dual-role controller is initialized in neither host nor device mode, the USBMODE register must be programmed for host operation before the EHCI host controller driver can begin EHCI host operations.

20.8.2.2 Non-Zero Fields the register file

Some of the reserved fields and reserved addresses in the capability registers and operational register have use in device mode, the following must be adhered to:

- Write operations to all EHCI reserved fields (some of which are device fields) with the operation registers should always be written to zero. This is an EHCI requirement of the device controller driver that must be adhered to.
- Read operations by the host controller must properly mask EHCI reserved fields (some of which are device fields) because fields that are used exclusive for device are undefined in host mode.

20.8.2.3 SOF interrupt

This SOF Interrupt used for device mode is shared as a free running 125us interrupt for host mode. EHCI does not specify this interrupt but it has been added for convenience and as a potential software time base. See USBSTS (Section 20.6.4) and USBINTR (Section 20.6.5) registers.

20.8.3 Miscellaneous variations from EHCI

20.8.3.1 Discovery

20.8.3.1.1 Port reset

The port connect methods specified by EHCI require setting the port reset bit in the PORTSCx register for a duration of 10 ms. Due to the complexity required to support the attachment of devices that are not high speed there are counter already present in the

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design that can count the 10ms reset pulse to alleviate the requirement of the software to measure this duration. Therefore, the basic connection is then summarized as the following:

- [Port Change Interrupt] Port connect change occurs to notify the host controller driver that a device has attached.
- Software shall write a ‘1’ to the reset the device.
- Software shall write a ‘0’ to the reset the device after 10 ms.

  This step, which is necessary in a standard EHCI design, may be omitted with this implementation. Should the EHCI host controller driver attempt to write a ‘0’ to the reset bit while a reset is in progress the write will simple be ignored and the reset will continue until completion.
- [Port Change Interrupt] Port enable change occurs to notify the host controller that the device in now operational and at this point the port speed has been determined.

20.8.3.1.2 Port speed detection

After the port change interrupt indicates that a port is enabled, the EHCI stack should determine the port speed. Unlike the EHCI implementation which will re-assign the port owner for any device that does not connect at High-Speed, this host controller supports direct attach of non High-Speed devices. Therefore, the following differences are important regarding port speed detection:

- Port Owner is read-only and always reads 0.
- A 2-bit Port Speed indicator has been added to PORTSC to provide the current operating speed of the port to the host controller driver.
- A 1-bit High Speed indicator has been added to PORTSC to signify that the port is in High-Speed vs. Full/Low Speed – This information is redundant with the 2-bit Port Speed indicator above.

20.9 Device data structures

This section defines the interface data structures used to communicate control, status, and data between Device Controller Driver (DCD) Software and the Device Controller. The data structure definitions in this chapter support a 32-bit memory buffer address space.

Remark: The Software must ensure that no interface data structure reachable by the Device controller crosses a 4k-page boundary

The data structures defined in the chapter are (from the device controller’s perspective) a mix of read-only and read/ writable fields. The device controller must preserve the read-only fields on all data structure writes.

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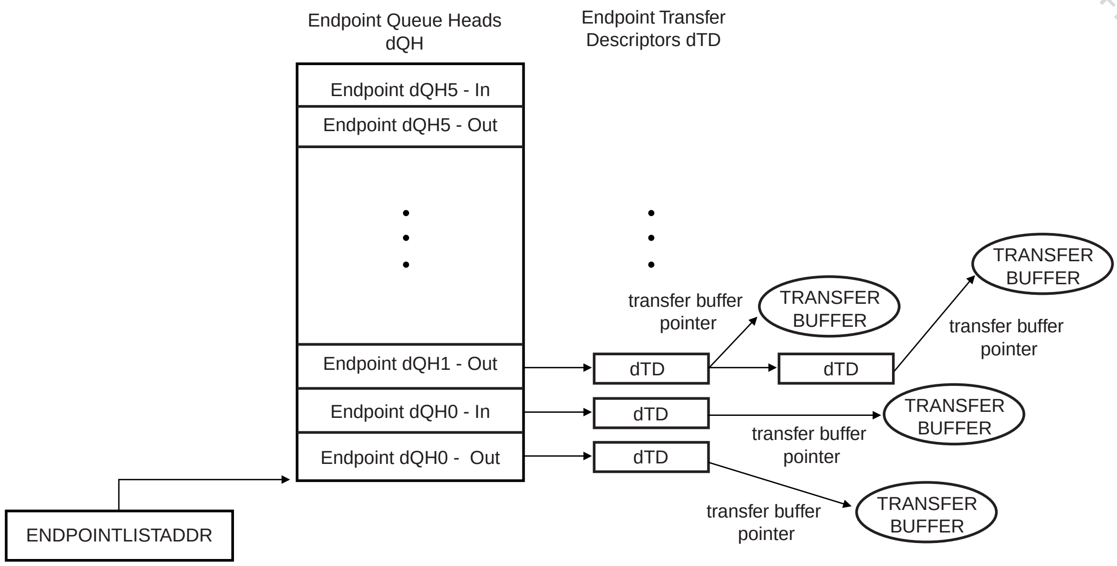


Fig 37. Endpoint queue head organization

Device queue heads are arranged in an array in a continuous area of memory pointed to by the ENDPOINTLISTADDR pointer. The even –numbered device queue heads in the list support receive endpoints (OUT/SETUP) and the odd-numbered queue heads in the list are used for transmit endpoints (IN/INTERRUPT). The device controller will index into this array based upon the endpoint number received from the USB bus. All information necessary to respond to transactions for all primed transfers is contained in this list so the Device Controller can readily respond to incoming requests without having to traverse a linked list.

Remark: The Endpoint Queue Head List must be aligned to a 2k boundary.

20.9.1 Endpoint queue head (dQH)

The device Endpoint Queue Head (dQH) is where all transfers are managed. The dQH is a 48-byte data structure, but must be aligned on 64-byte boundaries. During priming of an endpoint, the dTD (device transfer descriptor) is copied into the overlay area of the dQH, which starts at the nextTD pointer DWord and continues through the end of the buffer pointers DWords. After a transfer is complete, the dTD status DWord is updated in the dTD pointed to by the currentTD pointer. While a packet is in progress, the overlay area of the dQH is used as a staging area for the dTD so that the Device Controller can access needed information with little minimal latency.

20.9.1.1 Endpoint capabilities and characteristics

This DWord specifies static information about the endpoint, in other words, this information does not change over the lifetime of the endpoint. Device Controller software should not attempt to modify this information while the corresponding endpoint is enabled.

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Table 341. Endpoint capabilities and characteristics

Access	Bit	Name	Description
RO	31:30	MULT	Number of packets executed per transaction descriptor 00 - Execute N transactions as demonstrated by the USB variable length protocol where N is computed using Max_packet_length and the Total_bytes field in the dTD. 01 - Execute one transaction 10 - Execute two transactions 11 - Execute three transactions **Remark:** Non-isochronous endpoints must set MULT = 00. **Remark:** Isochronous endpoints must set MULT = 01, 10, or 11 as needed.
RO	29	ZLT	Zero length termination select This bit is used for non-isochronous endpoints to indicate when a zero-length packet is received to terminate transfers in case the total transfer length is “multiple”. 0 - Enable zero-length packet to terminate transfers equal to a multiple of Max_packet_length (default). 1 - Disable zero-length packet on transfers that are equal in length to a multiple Max_packet_length.
RO	28:27	-	reserved
RO	26:16	Max_packet_length	Maximum packet size of the associated endpoint (< 1024)
RO	15	IOS	Interrupt on setup This bit is used on control type endpoints to indicate if USBINT is set in response to a setup being received.
RO	14:0	-	reserved

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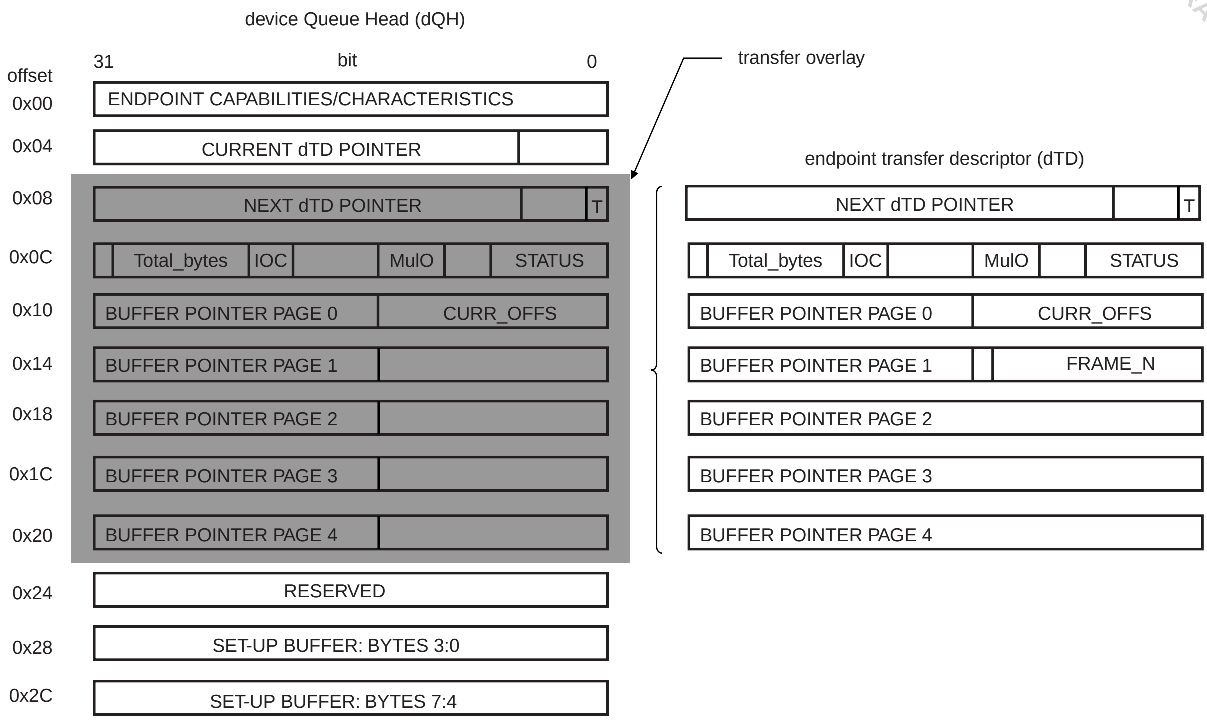


Fig 38. Endpoint queue head data structure

20.9.1.2 Transfer overlay

The seven DWords in the overlay area represent a transaction working space for the device controller. The general operational model is that the device controller can detect whether the overlay area contains a description of an active transfer. If it does not contain an active transfer, then it will not read the associated endpoint.

After an endpoint is readied, the dTD will be copied into this queue head overlay area by the device controller. Until a transfer is expired, software must not write the queue head overlay area or the associated transfer descriptor. When the transfer is complete, the device controller will write the results back to the original transfer descriptor and advance the queue. See dTD for a description of the overlay fields.

20.9.1.3 Current dTD pointer

The current dTD pointer is used by the device controller to locate the transfer in progress. This word is for Device Controller (hardware) use only and should not be modified by DCD software.

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Table 342. Current dTD pointer

Access	Bit	Name	Description
R/W (hardware only)	31:5	Current_TD_pointer	Current dTD pointer This field is a pointer to the dTD that is represented in the transfer overlay area. This field will be modified by the device controller to the next dTD pointer during endpoint priming or queue advance.
-	4:0	-	reserved

20.9.1.4 Set-up buffer

The set-up buffer is dedicated storage for the 8-byte data that follows a set-up PID.

Remark: Each endpoint has a TX and an RX dQH associated with it, and only the RX queue head is used for receiving setup data packets.

Table 343. Set-up buffer

Dword	Access	Bit	Name	Description
1	R/W	31:0	BUF0	Setup buffer 0 This buffer contains bytes 3 to 0 of an incoming setup buffer packet and is written by the device controller to be read by software.
2	R/W	31:0	BUF1	Setup buffer 1 This buffer contains bytes 7 to 4 of an incoming setup buffer packet and is written by the device controller to be read by software.

20.9.2 Endpoint transfer descriptor (dTD)

The dTD describes to the device controller the location and quantity of data to be sent/received for given transfer. The DCD should not attempt to modify any field in an active dTD except the Next Link Pointer, which should only be modified as described in Section 20.10.11.

Table 344. Next dTD pointer

Access	Bit	Name	Description
RO	31:5	Next_link_pointer	Next link pointer This field contains the physical memory address of the next dTD to be processed. The field corresponds to memory address signals [31:5], respectively.
	4:1	-	reserved
	0	T	Terminate This bit indicates to the device controller when there are no more valid entries in the queue. 1 - pointer is invalid 0 - Pointer is valid, i.e. pointer points to a valid transfer element descriptor.

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Table 345. dTD token

Access	Bit	Name	Description
-	31	-	reserved
R/W	30:16	Total_bytes	Total bytes This field specifies the total number of bytes to be moved with this transfer descriptor. This field is decremented by the number of bytes actually moved during the transaction and it is decremented only when the transaction has been completed successfully. The maximum value software can write into this field is 0x5000 (5 x 4 kB) for the maximum number of bytes five page pointers can access. Although it is possible to create a transfer up to 20 kB this assumes that the first offset into the first page is zero. When the offset cannot be predetermined, crossing past the fifth page can be guaranteed by limiting the total bytes to 16 kB. Therefore, the maximum recommended Total-Bytes = 16 kB (0x4000). If Total_bytes = 0 when the host controller fetches this transfer descriptor and the active bit is set in the Status field of this dTD, the device controller executes a zero-length transaction and retires the dTD. **Remark:** For IN transfers, it is not a requirement that Total_bytes is an even multiple of Max_packet_length. If software builds such a dTD, the last transaction will always be less than Max_packet_length.
RO	15	IOC	Interrupt on complete This bit is used to indicate if USBINT will be set when the device controller is finished with this dTD. 1 - USBINT set. 0 - USBINT not set.
-	14:12	-	reserved

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Table 345. dTD token *…continued*

Access	Bit	Name	Description
RO	11:10	MultO	Multiplier Override (see Section 20.9.2.1 for an example) This field can be used for transmit ISOs to override the MULT field in the dQH. This field must be zero for all packet types that are not transmit-ISO. 00 - Execute N transactions as demonstrated by the USB variable length protocol where N is computed using Max_packet_length and the Total_bytes field in the dTD. 01 - Execute one transaction 10 - Execute two transactions 11 - Execute three transactions **Remark:** Non-ISO and Non-TX endpoints must set MultO="00".
	9:8	-	reserved
R/W	7:0	Status	Status This field is used by the device controller to communicate individual execution states back to the software. This field contains the status of the last transaction performed on this dTD. Bit 7 = 1 - status: Active Bit 6 = 1 - status: Halted Bit 5 = 1 - status: Buffer Error Bit 4 - reserved Bit 3 = 1 - status: Transaction Error Bit 2 - reserved Bit 1 - reserved Bit 0 - reserved

Table 346. dTD buffer page pointer list

Access	Bit	Name	Description
RO	31:12	BUFF_P	Selects the page offset in memory for the packet buffer. Non-virtual memory systems will typically set the buffer pointers to a series of incrementing integers.
	page 0: 11:0	CURR_OFFS	Offset into the 4 kB buffer where the packet is to begin.
	page 1: 10:0	FRAME_N	Written by the device controller to indicate the frame number in which a packet finishes. This is typically used to correlate relative completion times of packets on an isochronous endpoint.

20.9.2.1 Determining the number of packets for Isochronous IN endpoints

The following examples show how the MULT field in the dQH and the MultO in the dTD are used to control the number of packets sent in an In-transaction for an isochronous endpoint:

Example 1

MULT = 3; Max_packet_size = 8; Total_bytes = 15; MultO = 0 (default)

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In this case three packets are sent: Data2 (8 bytes), Data1 (7 bytes), Data0 (0 bytes).

Example 2

MULT = 3; Max_packet_size = 8; Total_bytes = 15; MultO = 2

In this case two packets are sent: Data1 (8 bytes), Data0 (7 bytes).

To optimize efficiency for IN transfers, software should compute MultO = greatest integer of (Total_bytes/Max_packet_size). If Total_bytes = 0, then MultO should be 1.

20.10 Device operational model

The function of the device operation is to transfer a request in the memory image to and from the Universal Serial Bus. Using a set of linked list transfer descriptors, pointed to by a queue head, the device controller will perform the data transfers. The following sections explain the use of the device controller from the device controller driver (DCD) point-of-view and further describe how specific USB bus events relate to status changes in the device controller programmer's interface.

20.10.1 Device controller initialization

After hardware reset, the device is disabled until the Run/Stop bit is set to a ‘1’. In the disabled state, the pull-up on the USB_DM is not active which prevents an attach event from occurring. At a minimum, it is necessary to have the queue heads setup for endpoint zero before the device attach occurs. Shortly after the device is enabled, a USB reset will occur followed by setup packet arriving at endpoint 0. A Queue head must be prepared so that the device controller can store the incoming setup packet.

In order to initialize a device, the software should perform the following steps:

1. Set Controller Mode in the USBMODE register to device mode.

   Remark: Transitioning from host mode to device mode requires a device controller reset before modifying USBMODE.

2. Allocate and Initialize device queue heads in system memory (see Section 20.9).

   Minimum: Initialize device queue heads 0 Tx & 0 Rx.

   Remark: All device queue heads associated with control endpoints must be initialized before the control endpoint is enabled. Non-Control device queue heads must be initialized before the endpoint is used and not necessarily before the endpoint is enabled.

3. Configure ENDPOINTLISTADDR Pointer (see Section 20.6.8).

4. Enable the microprocessor interrupt associated with the USB-HS core.

   Recommended: enable all device interrupts including: USBINT, USBERRINT, Port Change Detect, USB Reset Received, DCSuspend (see Table 311).

5. Set Run/Stop bit to Run Mode.

   After the Run bit is set, a device reset will occur. The DCD must monitor the reset event and adjust the software state as described in the Bus Reset section of the following Port State and Control section below.

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Remark: Endpoint 0 is designed as a control endpoint only and does not need to be configured using ENDPTCTRL0 register.

It is also not necessary to initially prime Endpoint 0 because the first packet received will always be a setup packet. The contents of the first setup packet will require a response in accordance with USB device framework command set (see *USB Specification Rev. 2.0*, *chapter 9*).

20.10.2 Port state and control

From a chip or system reset, the device controller enters the powered state. A transition from the powered state to the attach state occurs when the Run/Stop bit is set to a ‘1’. After receiving a reset on the bus, the port will enter the defaultFS or defaultHS state in accordance with the reset protocol described in *Appendix C.2 of the USB Specification Rev. 2.0*. The following state diagram depicts the state of a USB 2.0 device.

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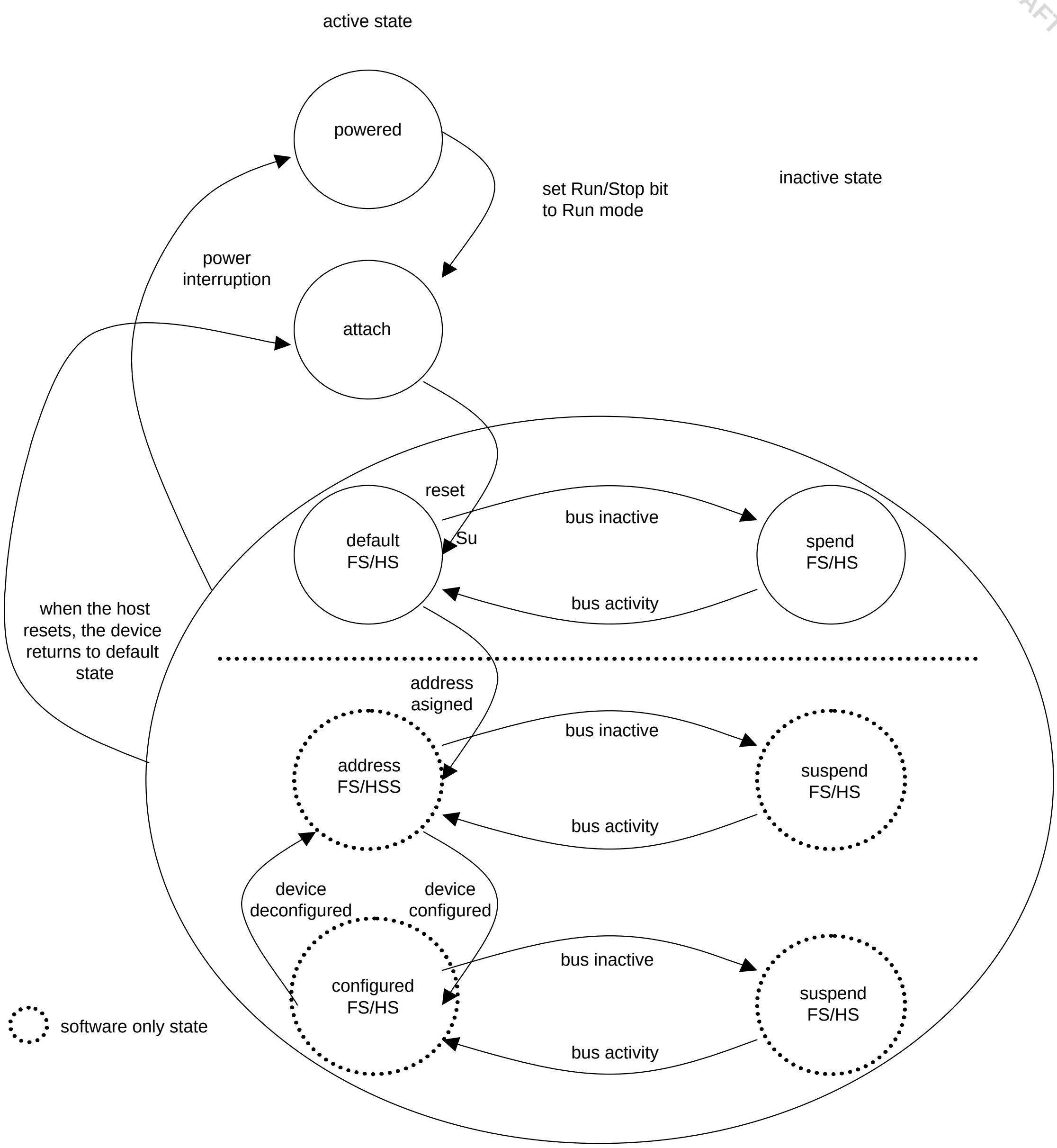


Fig 39. Device state diagram

The states powered, attach, default FS/HS, suspend FS/HS are implemented in the device controller and are communicated to the DCD using the following status bits:

- DCSuspend - see Table 309.
- USB reset received - see Table 309.
- Port change detect - see Table 309.
- High-speed port - see Table 326.

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It is the responsibility of the DCD to maintain a state variable to differentiate between the DefaultFS/HS state and the Address/Configured states. Change of state from Default to Address and the configured states is part of the enumeration process described in the *device framework section of the USB 2.0 Specification*.

As a result of entering the Address state, the device address register (DEVICEADDR) must be programmed by the DCD.

Entry into the Configured indicates that all endpoints to be used in the operation of the device have been properly initialized by programming the ENDPTCTRLx registers and initializing the associated queue heads.

20.10.3 Bus reset

A bus reset is used by the host to initialize downstream devices. When a bus reset is detected, the device controller will renegotiate its attachment speed, reset the device address to 0, and notify the DCD by interrupt (assuming the USB Reset Interrupt Enable is set). After a reset is received, all endpoints (except endpoint 0) are disabled and any primed transactions will be cancelled by the device controller. The concept of priming will be clarified below, but the DCD must perform the following tasks when a reset is received:

- Clear all setup token semaphores by reading the ENDPTSETUPSTAT register and writing the same value back to the ENDPTSETUPSTAT register.
- Clear all the endpoint complete status bits by reading the ENDPTCOMPLETE register and writing the same value back to the ENDPTCOMPLETE register.
- Cancel all primed status by waiting until all bits in the ENDPTPRIME are 0 and then writing 0xFFFFFFFF to ENDPTFLUSH.
- Read the reset bit in the PORTSCx register and make sure that it is still active. A USB reset will occur for a minimum of 3 ms and the DCD must reach this point in the reset cleanup before end of the reset occurs, otherwise a hardware reset of the device controller is recommended (rare).

  Remark: A hardware reset can be performed by writing a one to the device controller reset bit in the USBCMD reset. Note: a hardware reset will cause the device to detach from the bus by clearing the Run/Stop bit. Thus, the DCD must completely re-initialize the device controller after a hardware reset.
- Free all allocated dTDs because they will no longer be executed by the device controller. If this is the first time the DCD is processing a USB reset event, then it is likely that no dTDs have been allocated. At this time, the DCD may release control back to the OS because no further changes to the device controller are permitted until a Port Change Detect is indicated.
- After a Port Change Detect, the device has reached the default state and the DCD can read the PORTSCx to determine if the device is operating in FS or HS mode. At this time, the device controller has reached normal operating mode and DCD can begin enumeration according to the *USB2.0 specification Chapter 9 - Device Framework*.

  Remark: The device DCD may use the FS/HS mode information to determine the bandwidth mode of the device.

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In some applications, it may not be possible to enable one or more pipes while in FS mode. Beyond the data rate issue, there is no difference in DCD operation between FS and HS modes.

20.10.4 Suspend/resume

20.10.4.1 Suspend

In order to conserve power, USB devices automatically enter the suspended state when the device has observed no bus traffic for a specified period. When suspended, the USB device maintains any internal status, including its address and configuration. Attached devices must be prepared to suspend at any time they are powered, regardless of if they have been assigned a non-default address, are configured, or neither Bus activity may cease due to the host entering a suspend mode of its own. In addition, a USB device shall also enter the suspended state when the hub port it is attached to is disabled.

A USB device exits suspend mode when there is bus activity. A USB device may also request the host to exit suspend mode or selective suspend by using electrical signaling to indicate remote wake-up. The ability of a device to signal remote wake-up is optional. If the USB device is capable of remote wake-up signaling, the device must support the ability of the host to enable and disable this capability. When the device is reset, remote wake-up signaling must be disabled.

20.10.4.1.1 Operational model

The device controller moves into the suspend state when suspend signaling is detected or activity is missing on the upstream port for more than a specific period. After the device controller enters the suspend state, the DCD is notified by an interrupt (assuming DC Suspend Interrupt is enabled). When the DCSuspend bit in the PORTSCx is set to a ‘1’, the device controller is suspended.

DCD response when the device controller is suspended is application specific and may involve switching to low power operation. Information on the bus power limits in suspend state can be found in *USB 2.0 specification*.

20.10.4.2 Resume

If the device controller is suspended, its operation is resumed when any non-idle signaling is received on its upstream facing port. In addition, the device can signal the system to resume operation by forcing resume signaling to the upstream port. Resume signaling is sent upstream by writing a ‘1’ to the Resume bit in the in the PORTSCx while the device is in suspend state. Sending resume signal to an upstream port should cause the host to issue resume signaling and bring the suspended bus segment (one more devices) back to the active condition.

Remark: Before resume signaling can be used, the host must enable it by using the Set Feature command defined in *device framework (chapter 9) of the USB 2.0 Specification*.

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20.10.5 Managing endpoints

The *USB 2.0 specification* defines an endpoint, also called a device endpoint or an address endpoint as a uniquely addressable portion of a USB device that can source or sink data in a communications channel between the host and the device. The endpoint address is specified by the combination of the endpoint number and the endpoint direction.

The channel between the host and an endpoint at a specific device represents a data pipe. Endpoint 0 for a device is always a control type data channel used for device discovery and enumeration. Other types of endpoints support by USB include bulk, interrupt, and isochronous. Each endpoint type has specific behavior related to packet response and error handling. More detail on endpoint operation can be found in the *USB 2.0 specification*.

The LPC18xx supports up to six endpoints.

Each endpoint direction is essentially independent and can be configured with differing behavior in each direction. For example, the DCD can configure endpoint 1-IN to be a bulk endpoint and endpoint 1- OUT to be an isochronous endpoint. This helps to conserve the total number of endpoints required for device operation. The only exception is that control endpoints must use both directions on a single endpoint number to function as a control endpoint. Endpoint 0 is, for example, is always a control endpoint and uses the pair of directions.

Each endpoint direction requires a queue head allocated in memory. If the maximum of 4 endpoint numbers, one for each endpoint direction are being used by the device controller, then 8 queue heads are required. The operation of an endpoint and use of queue heads are described later in this document.

20.10.5.1 Endpoint initialization

After hardware reset, all endpoints except endpoint zero are un-initialized and disabled. The DCD must configure and enable each endpoint by writing to configuration bit in the ENDPTCTRLx register (see Table 338). Each 32-bit ENDPTCTRLx is split into an upper and lower half. The lower half of ENDPTCTRLx is used to configure the receive or OUT endpoint and the upper half is likewise used to configure the corresponding transmit or IN endpoint. Control endpoints must be configured the same in both the upper and lower half of the ENDPTCTRLx register otherwise the behavior is undefined. The following table shows how to construct a configuration word for endpoint initialization.

Table 347. Device controller endpoint initialization

Field	Value
Data Toggle Reset	1
Data Toggle Inhibit	0
Endpoint Type	00 - control
	01 - isochronous
	10 - bulk
	11 - interrupt
Endpoint Stall	0

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20.10.5.2 Stalling

There are two occasions where the device controller may need to return to the host a STALL:

1. The first occasion is the **functional stall**, which is a condition set by the DCD as described in the *USB 2.0 device framework (chapter 9)*. A functional stall is only used on non-control endpoints and can be enabled in the device controller by setting the endpoint stall bit in the ENDPTCTRLx register associated with the given endpoint and the given direction. In a functional stall condition, the device controller will continue to return STALL responses to all transactions occurring on the respective endpoint and direction until the endpoint stall bit is cleared by the DCD.
2. A **protocol stal**l, unlike a function stall, is used on control endpoints is automatically cleared by the device controller at the start of a new control transaction (setup phase). When enabling a protocol stall, the DCD should enable the stall bits (both directions) as a pair. A single write to the ENDPTCTRLx register can ensure that both stall bits are set at the same instant.

Remark: Any write to the ENDPTCTRLx register during operational mode must preserve the endpoint type field (i.e. perform a read-modify-write).

Table 348. Device controller stall response matrix

USB packet	Endpoint STALL bit	Effect on STALL bit	USB response
SETUP packet received by a non-control endpoint.	N/A	None	STALL
IN/OUT/PING packet received by a non-control endpoint.	1	None	STALL
IN/OUT/PING packet received by a non-control endpoint.	0	None	ACK/NAK/NYET
SETUP packet received by a control endpoint.	N/A	Cleared	ACK
IN/OUT/PING packet received by a control endpoint.	1	None	STALL
IN/OUT/PING packet received by a control endpoint.	0	None	ACK/NAK/NYET

20.10.5.3 Data toggle

Data toggle is a mechanism to maintain data coherency between host and device for any given data pipe. For more information on data toggle, refer *to the USB 2.0 specification.*

20.10.5.3.1 Data toggle reset

The DCD may reset the data toggle state bit and cause the data toggle sequence to reset in the device controller by writing a ‘1’ to the data toggle reset bit in the ENDPTCTRLx register. This should only be necessary when configuring/initializing an endpoint or returning from a STALL condition.

20.10.5.3.2 Data toggle inhibit

Remark: This feature is for test purposes only and should never be used during normal device controller operation.

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Setting the data toggle Inhibit bit active (‘1’) causes the device controller to ignore the data toggle pattern that is normally sent and accept all incoming data packets regardless of the data toggle state. In normal operation, the device controller checks the DATA0/DATA1 bit against the data toggle to determine if the packet is valid. If Data PID does not match the data toggle state bit maintained by the device controller for that endpoint, the Data toggle is considered not valid. If the data toggle is not valid, the device controller assumes the packet was already received and discards the packet (not reporting it to the DCD). To prevent the host controller from re-sending the same packet, the device controller will respond to the error packet by acknowledging it with either an ACK or NYET response.

20.10.6 Operational model for packet transfers

All transactions on the USB bus are initiated by the host and in turn, the device must respond to any request from the host within the turnaround time stated in the USB 2.0 Specification. At USB 1.1 Full or Low Speed rates, this turnaround time was significant and the USB 1.1 device controllers were designed so that the device controller could access main memory or interrupt a host protocol processor in order to respond to the USB 1.1 transaction. The architecture of the USB 2.0 device controller must be different because same methods will not meet USB 2.0 High-speed turnaround time requirements by simply increasing clock rate.

A USB host will send requests to the device controller in an order that can not be precisely predicted as a single pipeline, so it is not possible to prepare a single packet for the device controller to execute. However, the order of packet requests is predictable when the endpoint number and direction is considered. For example, if endpoint 3 (transmit direction) is configured as a bulk pipe, then we can expect the host will send IN requests to that endpoint. This device controller is designed in such a way that it can prepare packets for each endpoint/direction in anticipation of the host request. The process of preparing the device controller to send or receive data in response to host initiated transaction on the bus is referred to as “priming” the endpoint. This term will be used throughout the following documentation to describe the device controller operation so the DCD can be designed properly to use priming. Further, note that the term “flushing” is used to describe the action of clearing a packet that was queued for execution.

20.10.6.1 Priming transmit endpoints

Priming a transmit endpoint will cause the device controller to fetch the device transfer descriptor (dTD) for the transaction pointed to by the device queue head (dQH). After the dTD is fetched, it will be stored in the dQH until the device controller completes the transfer described by the dTD. Storing the dTD in the dQH allows the device controller to fetch the operating context needed to handle a request from the host without the need to follow the linked list, starting at the dQH when the host request is received. After the device has loaded the dTD, the leading data in the packet is stored in a FIFO in the device controller. This FIFO is split into virtual channels so that the leading data can be stored for any endpoint up to four endpoints.

After a priming request is complete, an endpoint state of primed is indicated in the ENDPTSTATUS register. For a primed transmit endpoint, the device controller can respond to an IN request from the host and meet the stringent bus turnaround time of High Speed USB. Since only the leading data is stored in the device controller FIFO, it is necessary for the device controller to begin filling in behind leading data after the

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transaction starts. The FIFO must be sized to account for the maximum latency that can be incurred by the system memory bus. On the LPC18xx, 128 x 36 bit dual port memory FIFOs are used for each IN endpoint.

20.10.6.2 Priming receive endpoints

Priming receive endpoints is identical to priming of transmit endpoints from the point of view of the DCD. At the device controller the major difference in the operational model is that there is no data movement of the leading packet data simply because the data is to be received from the host. Note as part of the architecture, the FIFO for the receive endpoints is not partitioned into multiple channels like the transmit FIFO. Thus, the size of the RX FIFO does not scale with the number of endpoints.

20.10.7 Interrupt/bulk endpoint operational model

The behaviors of the device controller for interrupt and bulk endpoints are identical. All valid IN and OUT transactions to bulk pipes will handshake with a NAK unless the endpoint had been primed. Once the endpoint has been primed, data delivery will commence.

A dTD will be retired by the device controller when the packets described in the transfer descriptor have been completed. Each dTD describes N packets to be transferred according to the USB Variable Length transfer protocol. The formula and table on the following page describe how the device controller computes the number and length of the packets to be sent/received by the USB vary according to the total number of bytes and maximum packet length.

With Zero Length Termination (ZLT) = 0

N = INT(Number Of Bytes/Max. Packet Length) + 1

With Zero Length Termination (ZLT) = 1

N = MAXINT(Number Of Bytes/Max. Packet Length)

Table 349. Variable length transfer protocol example (ZLT = 0)

Bytes (dTD)	Max Packet Length (dQH)	N	P1	P2	P3
511	256	2	256	255	-
512	256	3	256	256	0
512	512	2	512	0	-

Table 350. Variable length transfer protocol example (ZLT = 1)

Bytes (dTD)	Max Packet Length (dQH)	N	P1	P2	P3
511	256	2	256	255	-
512	256	2	256	256	-
512	512	1	512	-	-

Remark: The MULT field in the dQH must be set to “00” for bulk, interrupt, and control endpoints.

TX-dTD is complete when all packets described dTD were successfully transmitted.Total bytes in dTD will equal zero when this occurs.

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RX-dTD is complete when:

- All packets described in dTD were successfully received. Total bytes in dTD will equal zero when this occurs.
- A short packet (number of bytes < maximum packet length) was received. This is a successful transfer completion; DCD must check Total Bytes in dTD to determine the number of bytes that are remaining. From the total bytes remaining in the dTD, the DCD can compute the actual bytes received.
- A long packet was received (number of bytes > maximum packet size) OR (total bytes received > total bytes specified). This is an error condition. The device controller will discard the remaining packet, and set the Buffer Error bit in the dTD. In addition, the endpoint will be flushed and the USBERR interrupt will become active.

On the successful completion of the packet(s) described by the dTD, the active bit in the dTD will be cleared and the next pointer will be followed when the Terminate bit is clear. When the Terminate bit is set, the device controller will flush the endpoint/direction and cease operations for that endpoint/direction. On the unsuccessful completion of a packet (see long packet above), the dQH will be left pointing to the dTD that was in error. In order to recover from this error condition, the DCD must properly reinitialize the dQH by clearing the active bit and update the nextTD pointer before attempting to re-prime the endpoint.

Remark: All packet level errors such as a missing handshake or CRC error will be retried automatically by the device controller.

There is no required interaction with the DCD for handling such errors.

20.10.7.1 Interrupt/bulk endpoint bus response matrix

Table 351. Interrupt/bulk endpoint bus response matrix

Token type	STALL	Not primed	Primed	Underflow	Overflow
Setup	Ignore	Ignore	Ignore	n/a	n/a
In	STALL	NAK	Transmit	BS error	n/a
Out	STALL	NAK	Receive and NYET/ACK	n/a	NAK
Ping	STALL	NAK	ACK	n/a	n/a
Invalid	Ignore	Ignore	Ignore	Ignore	Ignore

[1] BS error = Force Bit Stuff Error

[2] NYET/ACK – NYET unless the Transfer Descriptor has packets remaining according to the USB variable length protocol then ACK.

[3] SYSERR – System error should never occur when the latency FIFOs are correctly sized and the DCD is responsive.

20.10.8 Control endpoint operational model

20.10.8.1 Setup phase

All requests to a control endpoint begin with a setup phase followed by an optional data phase and a required status phase. The device controller will always accept the setup phase unless the setup lockout is engaged.

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The setup lockout will engage so that future setup packets are ignored. Lockout of setup packets ensures that while software is reading the setup packet stored in the queue head, that data is not written as it is being read potentially causing an invalid setup packet.

In hardware the setup lockout mechanism can be disabled and a new tripwire type semaphore will ensure that the setup packet payload is extracted from the queue head without being corrupted by an incoming setup packet. This is the preferred behavior because ignoring repeated setup packets due to long software interrupt latency would be a compliance issue.

20.10.8.1.1 Setup Packet Handling using setup lockout mechanism

After receiving an interrupt and inspecting USBMODE to determine that a setup packet was received on a particular pipe:

1. Duplicate contents of dQH.SsetupBuffer into local software byte array.
2. Write '1' to clear corresponding ENDPTSETUPSTAT bit and thereby disabling Setup Lockout (i.e. the Setup Lockout activates as soon as a setup arrives. By writing to the ENDPTSETUPSTAT, the device controller will accept new setup packets.).
3. Process setup packet using local software byte array copy and execute status/handshake phases.

   Remark: After receiving a new setup packet the status and/or handshake phases may still be pending from a previous control sequence. These should be flushed & deallocated before linking a new status and/or handshake dTD for the most recent setup packet.
4. Before priming for status/handshake phases ensure that ENDPTSETUPSTAT is ‘0’. The time from writing a ‘1’ to ENDPTSETUPSTAT and reading back a ‘0’ may vary according to the type of traffic on the bus up to nearly a 1ms, however the it is absolutely necessary to ensure ENDPTSETUPSTAT has transitioned to ‘0’ after step 1) and before priming for the status/handshake phases.

Remark: To limit the exposure of setup packets to the setup lockout mechanism (if used), the DCD should designate the priority of responding to setup packets above responding to other packet completions

20.10.8.1.2 Setup Packet Handling using trip wire mechanism

- Disable Setup Lockout by writing ‘1’ to Setup Lockout Mode (SLOM) in USBMODE. (once at initialization). Setup lockout is not necessary when using the tripwire as described below.

  Remark: Leaving the Setup Lockout Mode As ‘0’ will result in pre-2.3 hardware behavior.
- After receiving an interrupt and inspecting ENDPTSETUPSTAT to determine that a setup packet was received on a particular pipe:
  a. Write '1' to clear corresponding bit ENDPTSETUPSTAT.
  b. Duplicate contents of dQH.SetupBuffer into local software byte array.
  c. Write ‘1’ to Setup Tripwire (SUTW) in USBCMD register.
  d. Read Setup TripWire (SUTW) in USBCMD register. (if set - continue; if cleared - go to b).
  e. Write '0' to clear Setup Tripwire (SUTW) in USBCMD register.

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f. Process setup packet using local software byte array copy and execute status/handshake phases.

g. Before priming for status/handshake phases ensure that ENDPTSETUPSTAT is '0'.

- A poll loop should be used to wait until ENDPTSETUPSTAT transitions to '0' after step a) above and before priming for the status/handshake phases.
- The time from writing a '1' to ENDPTSETUPSTAT and reading back a '0' is very short (~1-2 us) so a poll loop in the DCD will not be harmful.

Remark: After receiving a new setup packet the status and/or handshake phases may still be pending from a previous control sequence. These should be flushed & deallocated before linking a new status and/or handshake dTD for the most recent setup packet.

20.10.8.2 Data phase

Following the setup phase, the DCD must create a device transfer descriptor for the data phase and prime the transfer.

After priming the packet, the DCD must verify a new setup packet has not been received by reading the ENDPTSETUPSTAT register immediately verifying that the prime had completed. A prime will complete when the associated bit in the ENDPTPRIME register is zero and the associated bit in the ENDPTSTATUS register is a one. If a prime fails, i.e. The ENDPTPRIME bit goes to zero and the ENDPTSTATUS bit is not set, then the prime has failed. This can only be due to improper setup of the dQH, dTD or a setup arriving during the prime operation. If a new setup packet is indicated after the ENDPTPRIME bit is cleared, then the transfer descriptor can be freed and the DCD must reinterpret the setup packet.

Should a setup arrive after the data stage is primed, the device controller will automatically clear the prime status (ENDPTSTATUS) to enforce data coherency with the setup packet.

Remark: The MULT field in the dQH must be set to "00" for bulk, interrupt, and control endpoints.

Remark: Error handling of data phase packets is the same as bulk packets described previously.

20.10.8.3 Status phase

Similar to the data phase, the DCD must create a transfer descriptor (with byte length equal zero) and prime the endpoint for the status phase. The DCD must also perform the same checks of the ENDPTSETUPSTAT as described above in the data phase.

Remark: The MULT field in the dQH must be set to "00" for bulk, interrupt, and control endpoints.

Remark: Error handling of data phase packets is the same as bulk packets described previously.

20.10.8.4 Control endpoint bus response matrix

Shown in the following table is the device controller response to packets on a control endpoint according to the device controller state.

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Table 352. Control endpoint bus response matrix

Token type	Endpoint sate					Setup lockout
	STALL	Not primed	Primed	Underflow	Overflow	
Setup	ACK	ACK	ACK	n/a	SYSERR	-
In	STALL	NAK	Transmit	BS error	n/a	n/a
Out	STALL	NAK	Receive and NYET/ACK	n/a	NAK	n/a
Ping	STALL	NAK	ACK	n/a	n/a	n/a
Invalid	Ignore	Ignore	Ignore	Ignore	Ignore	ignore

[1] BS error = Force Bit Stuff Error

[2] NYET/ACK – NYET unless the Transfer Descriptor has packets remaining according to the USB variable length protocol then ACK.

[3] SYSERR – System error should never occur when the latency FIFOs are correctly sized and the DCD is responsive.

20.10.9 Isochronous endpoint operational model

Isochronous endpoints are used for real-time scheduled delivery of data, and their operational model is significantly different than the host throttled Bulk, Interrupt, and Control data pipes. Real time delivery by the device controller is accomplished by the following:

- Exactly MULT Packets per (micro) Frame are transmitted/received. Note: MULT is a two-bit field in the device Queue Head. The variable length packet protocol is not used on isochronous endpoints.
- NAK responses are not used. Instead, zero length packets are sent in response to an IN request to an unprimed endpoints. For unprimed RX endpoints, the response to an OUT transaction is to ignore the packet within the device controller.
- Prime requests always schedule the transfer described in the dTD for the next (micro) frame. If the ISO-dTD is still active after that frame, then the ISO-dTD will be held ready until executed or canceled by the DCD.

An EHCI compatible host controller uses the periodic frame list to schedule data exchanges to Isochronous endpoints. The operational model for device mode does not use such a data structure. Instead, the same dTD used for Control/Bulk/Interrupt endpoints is also used for isochronous endpoints. The difference is in the handling of the dTD.

The first difference between bulk and ISO-endpoints is that priming an ISO-endpoint is a delayed operation such that an endpoint will become primed only after a SOF is received. After the DCD writes the prime bit, the prime bit will be cleared as usual to indicate to software that the device controller completed a priming the dTD for transfer. Internal to the design, the device controller hardware masks that prime start until the next frame boundary. This behavior is hidden from the DCD but occurs so that the device controller can match the dTD to a specific (micro) frame.

Another difference with isochronous endpoints is that the transaction must wholly complete in a (micro) frame. Once an ISO transaction is started in a (micro) frame it will retire the corresponding dTD when MULT transactions occur or the device controller finds

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a fulfillment condition. The transaction error bit set in the status field indicates a fulfillment error condition. When a fulfillment error occurs, the frame after the transfer failed to complete wholly, the device controller will force retire the ISO-dTD and move to the next ISO-dTD.

It is important to note that fulfillment errors are only caused due to partially completed packets. If no activity occurs to a primed ISO-dTD, the transaction will stay primed indefinitely. This means it is up to software discard transmit ISO-dTDs that pile up from a failure of the host to move the data. Finally, the last difference with ISO packets is in the data level error handling. When a CRC error occurs on a received packet, the packet is not retried similar to bulk and control endpoints. Instead, the CRC is noted by setting the Transaction Error bit and the data is stored as usual for the application software to sort out.

TX packet retired

- MULT counter reaches zero.
- Fulfillment Error [Transaction Error bit is set].
- # Packets Occurred > 0 AND # Packets Occurred < MULT.

Remark: For TX-ISO, MULT Counter can be loaded with a lesser value in the dTD Multiplier Override field. If the Multiplier Override is zero, the MULT Counter is initialized to the Multiplier in the QH.

RX packet retired

- MULT counter reaches zero.
- Non-MDATA Data PID is received.

  Remark: Exit criteria only valid in hardware version 2.3 or later. Previous to hardware version 2.3, any PID sequence that did not match the MULT field exactly would be flagged as a transaction error due to PID mismatch or fulfillment error.
- Overflow Error:
  - Packet received is > maximum packet length. [Buffer Error bit is set].
  - Packet received exceeds total bytes allocated in dTD. [Buffer Error bit is set].
- Fulfillment error [Transaction Error bit is set]:

  # Packets Occurred > 0 AND # Packets Occurred < MULT.
- CRC Error [Transaction Error bit is set]

Remark: For ISO, when a dTD is retired, the next dTD is primed for the next frame. For continuous (micro) frame to (micro) frame operation the DCD should ensure that the dTD linked-list is out ahead of the device controller by at least two (micro) frames.

20.10.9.1 Isochronous pipe synchronization

When it is necessary to synchronize an isochronous data pipe to the host, the (micro) frame number (FRINDEX register) can be used as a marker. To cause a packet transfer to occur at a specific (micro) frame number [N], the DCD should interrupt on SOF during frame N-1. When the FRINDEX=N–1, the DCD must write the prime bit. The device controller will prime the isochronous endpoint in (micro) frame N–1 so that the device controller will execute delivery during (micro) frame N.

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Remark: Priming an endpoint towards the end of (micro) frame N-1 will not guarantee delivery in (micro) frame N. The delivery may actually occur in (micro) frame N+1 if device controller does not have enough time to complete the prime before the SOF for packet N is received.

20.10.9.2 Isochronous endpoint bus response matrix

Table 353. Isochronous endpoint bus response matrix

Token type	STALL	Not primed	Primed	Underflow	Overflow
Setup	STALL	STALL	STALL	n/a	n/a
In	NULL packet	NULL packet	Transmit	BS error	n/a
Out	Ignore	Ignore	Receive	n/a	Drop packet
Ping	Ignore	Ignore	Ignore	Ignore	Ignore
Invalid	Ignore	Ignore	Ignore	Ignore	Ignore

[1] BS error = Force Bit Stuff Error

[2] NULL packet = Zero length packet.

20.10.10 Managing queue heads

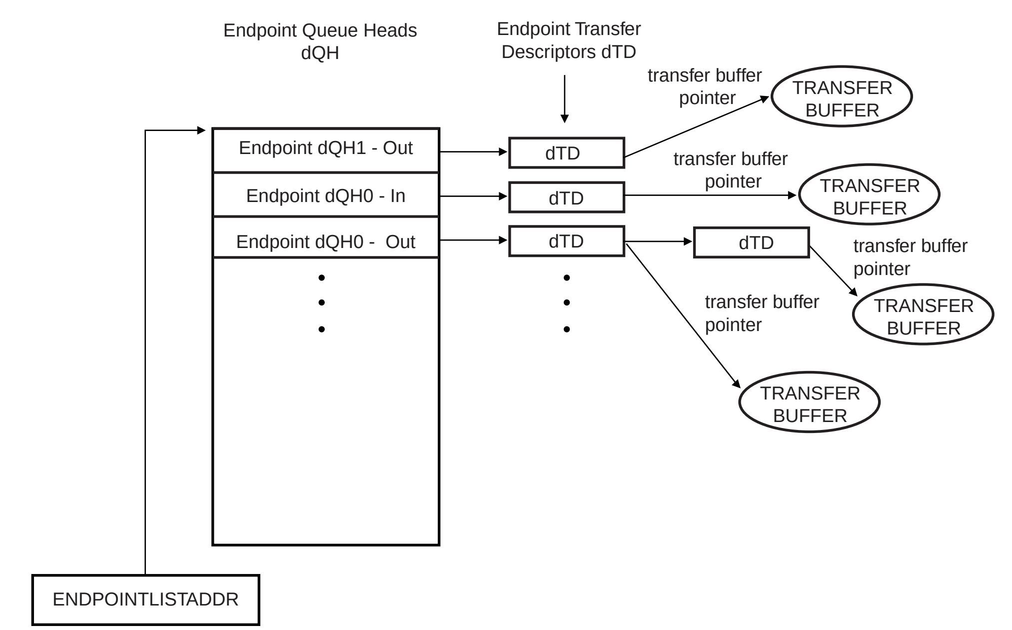


Fig 40. Endpoint queue head diagram

The device queue head (dQH) points to the linked list of transfer tasks, each depicted by the device Transfer Descriptor (dTD). An area of memory pointed to by ENDPOINTLISTADDR contains a group of all dQH's in a sequential list as shown Figure 40. The even elements in the list of dQH's are used for receive endpoints (OUT/SETUP) and the odd elements are used for transmit endpoints (IN/INTERRUPT). Device transfer descriptors are linked head to tail starting at the queue head and ending at a terminate bit. Once the dTD has been retired, it will no longer be part of the linked list

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from the queue head. Therefore, software is required to track all transfer descriptors since pointers will no longer exist within the queue head once the dTD is retired (see Section 20.10.11.1).

In addition to the current and next pointers and the dTD overlay examined in section Operational Model For Packet Transfers, the dQH also contains the following parameters for the associated endpoint: Multiplier, Maximum Packet Length, Interrupt On Setup. The complete initialization of the dQH including these fields is demonstrated in the next section.

20.10.10.1 Queue head initialization

One pair of device queue heads must be initialized for each active endpoint. To initialize a device queue head:

- Write the wMaxPacketSize field as required by the *USB Chapter 9* or application specific protocol.
- Write the multiplier field to 0 for control, bulk, and interrupt endpoints. For ISO endpoints, set the multiplier to 1,2, or 3 as required bandwidth and in conjunction with the *USB Chapter 9 protocol*. Note: In FS mode, the multiplier field can only be 1 for ISO endpoints.
- Write the next dTD Terminate bit field to “1”.
- Write the Active bit in the status field to “0”.
- Write the Halt bit in the status field to “0”.

Remark: The DCD must only modify dQH if the associated endpoint is not primed and there are no outstanding dTD’s.

20.10.10.2 Operational model for setup transfers

As discussed in section Control Endpoint Operational Model (Section 20.10.8), setup transfer requires special treatment by the DCD. A setup transfer does not use a dTD but instead stores the incoming data from a setup packet in an 8-byte buffer within the dQH.

Upon receiving notification of the setup packet, the DCD should handle the setup transfer as demonstrated here:

1. Copy setup buffer contents from dQH - RX to software buffer.
2. Acknowledge setup backup by writing a “1” to the corresponding bit in ENDPTSETUPSTAT.

   Remark: The acknowledge must occur before continuing to process the setup packet.

   Remark: After the acknowledge has occurred, the DCD must not attempt to access the setup buffer in the dQH – RX. Only the local software copy should be examined.
3. Check for pending data or status dTD’s from previous control transfers and flush if any exist as discussed in section Flushing/De-priming an Endpoint.

   Remark: It is possible for the device controller to receive setup packets before previous control transfers complete. Existing control packets in progress must be flushed and the new control packet completed.
4. Decode setup packet and prepare data phase [optional] and status phase transfer as require by the *USB Specification Chapter 9* or application specific protocol.

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20.10.11 Managing transfers with transfer descriptors

20.10.11.1 Software link pointers

It is necessary for the DCD software to maintain head and tail pointers to the linked list of dTDs for each respective queue head. This is necessary because the dQH only maintains pointers to the current working dTD and the next dTD to be executed. The operations described in next section for managing dTD will assume the DCD can use reference the head and tail of the dTD linked list.

Remark: To conserve memory, the reserved fields at the end of the dQH can be used to store the Head & Tail pointers but it still remains the responsibility of the DCD to maintain the pointers.

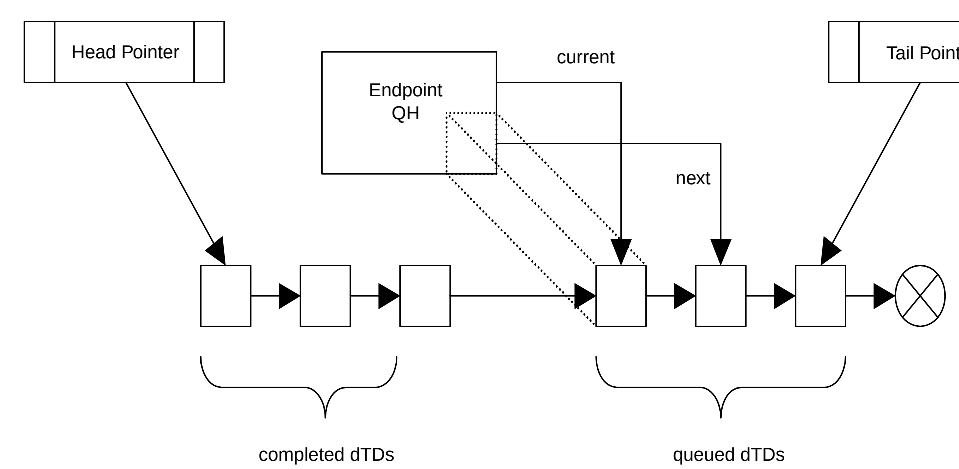


Fig 41. Software link pointers

20.10.11.2 Building a transfer descriptor

Before a transfer can be executed from the linked list, a dTD must be built to describe the transfer. Use the following procedure for building dTDs:

Allocate 8-DWord dTD block of memory aligned to 8-DWord boundaries. Example: bit address 4:0 would be equal to “00000”.

Write the following fields:

1. Initialize first 7 DWords to 0.
2. Set the terminate bit to “1”.
3. Fill in total bytes with transfer size.
4. Set the interrupt on complete if desired.
5. Initialize the status field with the active bit set to “1” and all remaining status bits set to “0”.
6. Fill in buffer pointer page 0 and the current offset to point to the start of the data buffer.
7. Initialize buffer pointer page 1 through page 4 to be one greater than each of the previous buffer pointer.

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20.10.11.3 Executing a transfer descriptor

To safely add a dTD, the DCD must follow this procedure which will handle the event where the device controller reaches the end of the dTD list at the same time a new dTD is being added to the end of the list.

Determine whether the link list is empty: Check DCD driver to see if pipe is empty (internal representation of linked-list should indicate if any packets are outstanding).

Link list is empty

1. Write dQH next pointer AND dQH terminate bit to 0 as a single DWord operation.
2. Clear active and halt bits in dQH (in case set from a previous error).
3. Prime endpoint by writing ‘1’ to correct bit position in ENDPTPRIME.

Link list is not empty

1. Add dTD to end of the linked list.
2. Read correct prime bit in ENDPTPRIME – if ‘1’ DONE.
3. Set ATDTW bit in USBCMD register to ‘1’.
4. Read correct status bit in ENDPTSTAT. (Store in temp variable for later).
5. Read ATDTW bit in USBCMD register.
   - If ‘0’ go to step 3.
   - If ‘1’ continue to step 6.
6. Write ATDTW bit in USBCMD register to ‘0’.
7. If status bit read in step 4 (ENDPSTAT reg) indicates endpoint priming is DONE (corresponding ERBRx or ETBRx is one): DONE.
8. If status bit read in step 4 is 0 then go to Linked list is empty: Step 1.

20.10.11.4 Transfer completion

After a dTD has been initialized and the associated endpoint primed the device controller will execute the transfer upon the host-initiated request. The DCD will be notified with a USB interrupt if the Interrupt On Complete bit was set or alternately, the DCD can poll the endpoint complete register to find when the dTD had been executed. After a dTD has been executed, DCD can check the status bits to determine success or failure.

Remark: Multiple dTD can be completed in a single endpoint complete notification. After clearing the notification, DCD must search the dTD linked list and retire all dTDs that have finished (Active bit cleared).

By reading the status fields of the completed dTDs, the DCD can determine if the transfers completed successfully. Success is determined with the following combination of status bits:

Active = 0

Halted = 0

Transaction Error = 0

Data Buffer Error = 0

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Should any combination other than the one shown above exist, the DCD must take proper action. Transfer failure mechanisms are indicated in the Device Error Matrix (see Table 354).

In addition to checking the status bit, the DCD must read the Transfer Bytes field to determine the actual bytes transferred. When a transfer is complete, the Total Bytes transferred is decremented by the actual bytes transferred. For Transmit packets, a packet is only complete after the actual bytes reaches zero, but for receive packets, the host may send fewer bytes in the transfer according the USB variable length packet protocol.

20.10.11.5 Flushing/De-priming an endpoint

It is necessary for the DCD to flush to de-prime one more endpoints on a USB device reset or during a broken control transfer. There may also be application specific requirements to stop transfers in progress. The following procedure can be used by the DCD to stop a transfer in progress:

1. Write a ‘1’ to the corresponding bit(s) in ENDPTFLUSH.
2. Wait until all bits in ENDPTFLUSH are ‘0’.

   Remark: Software note: This operation may take a large amount of time depending on the USB bus activity. It is not desirable to have this wait loop within an interrupt service routine.
3. Read ENDPTSTAT to ensure that for all endpoints commanded to be flushed, that the corresponding bits are now ‘0’. If the corresponding bits are ‘1’ after step #2 has finished, then the flush failed as described in the following:

   In very rare cases, a packet is in progress to the particular endpoint when commanded flush using ENDPTFLUSH. A safeguard is in place to refuse the flush to ensure that the packet in progress completes successfully. The DCD may need to repeatedly flush any endpoints that fail to flush by repeating steps 1-3 until each endpoint is successfully flushed.

20.10.11.6 Device error matrix

The Table 354 summarizes packet errors that are not automatically handled by the Device Controller.

The following errors can occur:

Overflow: Number of bytes received exceeded max. packet size or total buffer length. This error will also set the Halt bit in the dQH, and if there are dTDs remaining in the linked list for the endpoint, then those will not be executed.

ISO packet error: CRC Error on received ISO packet. Contents not guaranteed to be correct.

ISO fulfillment error: Host failed to complete the number of packets defined in the dQH mult field within the given (micro) frame. For scheduled data delivery the DCD may need to readjust the data queue because a fulfillment error will cause Device Controller to cease data transfers on the pipe for one (micro) frame. During the “dead” (micro) frame, the Device Controller reports error on the pipe and primes for the following frame

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Table 354. Device error matrix

Error	Direction	Packet type	Data buffer error bit	Transaction error bit
Overflow	Rx	Any	1	0
ISO packet error	Rx	ISO	0	1
ISO fulfillment error	Both	ISO	0	1

20.10.12 Servicing interrupts

The interrupt service routine must consider that there are high-frequency, low-frequency operations, and error operations and order accordingly.

20.10.12.1 High-frequency interrupts

High frequency interrupts in particular should be handed in the order below. The most important of these is listed first because the DCD must acknowledge a setup buffer in the timeliest manner possible.

Table 355. High-frequency interrupt events

Execution order	Interrupt	Action
1a	USB interrupt: ENDPTSETUPSTATUS [1]	Copy contents of setup buffer and acknowledge setup packet (as indicated in Section 20.10.10). Process setup packet according to *USB 2.0 Chapter 9* or application specific protocol.
1b	USB interrupt: ENDPTCOMPLETE[1]	Handle completion of dTD as indicated in Section 20.10.10.
2	SOF interrupt	Action as deemed necessary by application. This interrupt may not have a use in all applications.

[1] It is likely that multiple interrupts to stack up on any call to the Interrupt Service Routine AND during the Interrupt Service Routine.

20.10.12.2 Low-frequency interrupts

The low frequency events include the following interrupts. These interrupt can be handled in any order since they don't occur often in comparison to the high-frequency interrupts.

Table 356. Low-frequency interrupt events

Interrupt	Action
Port change	Change software state information.
Sleep enable (Suspend)	Change software state information. Low power handling as necessary.
Reset Received	Change software state information. Abort pending transfers.

20.10.12.3 Error interrupts

Error interrupts will be least frequent and should be placed last in the interrupt service routine.

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Table 357. Error interrupt events

Interrupt	Action
USB error interrupt	This error is redundant because it combines USB Interrupt and an error status in the dTD. The DCD will more aptly handle packet-level errors by checking dTD status field upon receipt of USB Interrupt (w/ ENDPTCOMPLETE).
System error	Unrecoverable error. Immediate Reset of core; free transfers buffers in progress and restart the DCD.

20.11 USB power optimization

The USB-HS core is a fully synchronous static design. The power used by the design is dependent on the implementation technology used to fabricate the design and on the application usage of the core. Applications that transfer more data or use a greater number of packets to be sent will consume a greater amount of power.

Because the design is synchronous and static, power may be conserved by reducing the transitions of the clock net. This may be done in several ways.

1. Reduce the clock frequency to the core. The clock frequency may not be reduced below the minimum recommended operating frequency of the core without first disabling the USB operation.
2. Reduce transition on the clock net through the use of clock gating methods. (The LPC18xx is synthesized using this mechanism).
3. The clock may be shut off to the core entirely to conserve power. Again this may only be done after the USB operations on the bus have been disabled.

A device may suspend operations autonomously by disconnecting from the USB, or, in response to the suspend signaling, the USB has moved it into the suspend state. A host can suspend operation autonomously, or it can command portions or the entire USB to transition into the suspend state.

20.11.1 USB power states

The USB provides a mechanism to place segments of the USB or the entire USB into a low-power suspend state. USB bus powered devices are required to respond to a 3ms lack of activity on the USB bus by going into a suspend state. In the USB-HS core software is notified of the suspend condition via the transition in the PORTSC register. Optionally an interrupt can be generated which is controlled by the port change Detect Enable bit in the USBINTR control register. Software then has 7 ms to transition a bus powered device into the suspend state. In the suspend state, a USB device has a maximum USB bus power budget of 500μA. In general, to achieve that level of power conservation, most of the device circuits will need to be switched off, or clock at an extremely low frequency. This can be accomplished by suspending the clock.

The implementation of low power states in the USB-HS core is dependant on the use of the device role (host or peripheral), whether the device is bus powered, and the selected clock architecture of the core.

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Bus powered peripheral devices are required by the USB specification to support a low power suspend state. Self powered peripheral devices and hosts set their own power management strategies based on their system level requirements. The clocking architecture selected is important to consider as it determines what portions of the design will remain active when transitioned into the low power state.

Before the system clock is suspended or set to a frequency that is below the operational frequency of the USB-HS core, the core must be moved from the operational state to a low power state. The power strategies designed into the USB-HS core allow for the most challenging case, a self powered device that is clocked entirely by the transceiver clock.

20.11.2 Device power states

A bus powered peripheral device must move through the power states as directed by the host. Optionally autonomously directed low power states may be implemented.

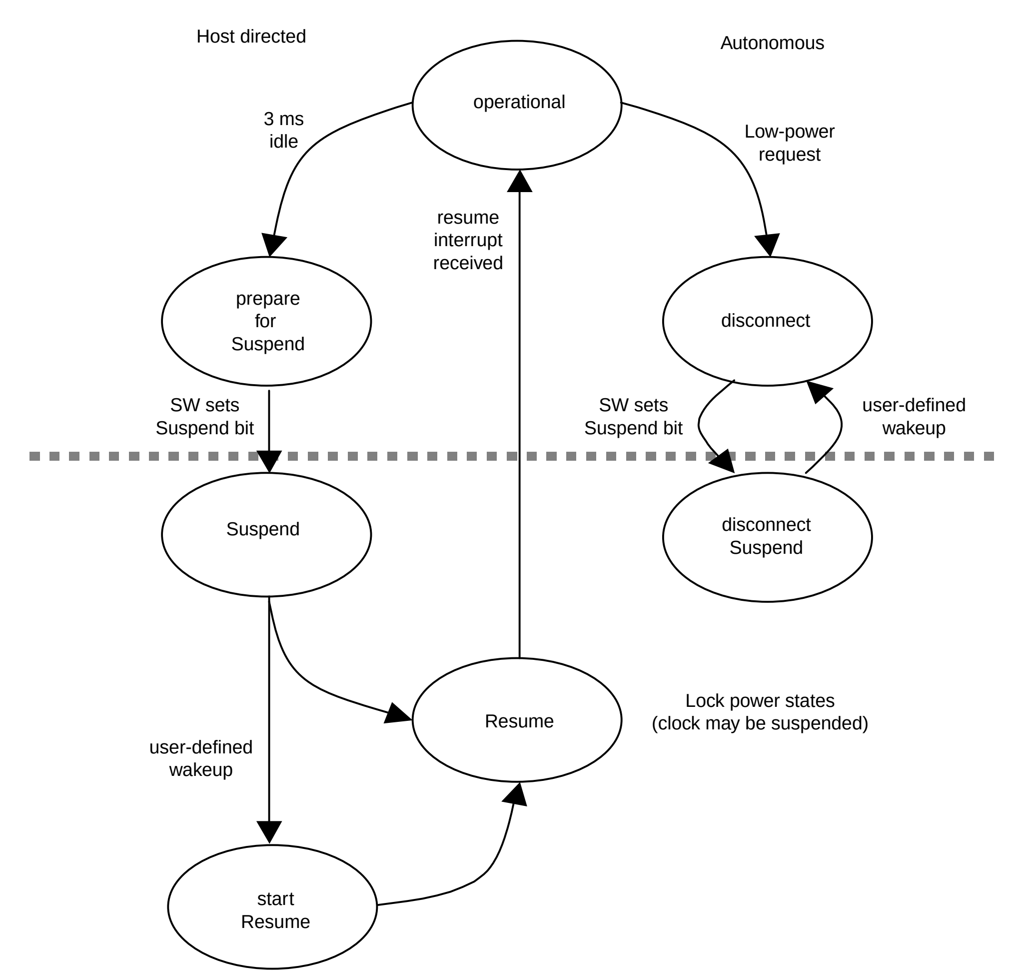


Fig 42. Device power state diagram

In the operational state both the transceiver clock and system clocks are running. Software can initiate a low power mode autonomously by disconnecting from the host to go into the disconnect state. Once in this state, the software can set the Suspend bit to

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turn off the transceiver clock putting the system in to the disconnect-suspend state. Since software cannot depend on the presents of a clock to clear the Suspend bit, a wake-up event must be defined which would clear the Suspend bit and allow the transceiver clock to resume.

The device can also go into suspend mode as a result of a suspend command from the host. Suspend is signaled on the bus by 3ms of idle time on the bus. This will generate a suspend interrupt to the software at which point the software must prepare to go into suspend then set the suspend bit. Once the Suspend bit is set the transceiver clock may turn off and the device will be in the suspended state. The device has two ways of getting out of suspend.

1. If remote wake-up is enabled, a wake-up event could be defined which would clear the Suspend bit. The software would then initiate the resume by setting the Resume bit in the port controller then waiting for a port change interrupt indicating that the port is in an operational state.
2. If the host puts resume signaling on the bus, it will clear the Suspend bit and generate a port change interrupt when the resume is finished.

In either case the system designer must insure an orderly restoration of the power and clocks to the suspended circuitry.

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20.11.3 Host power states

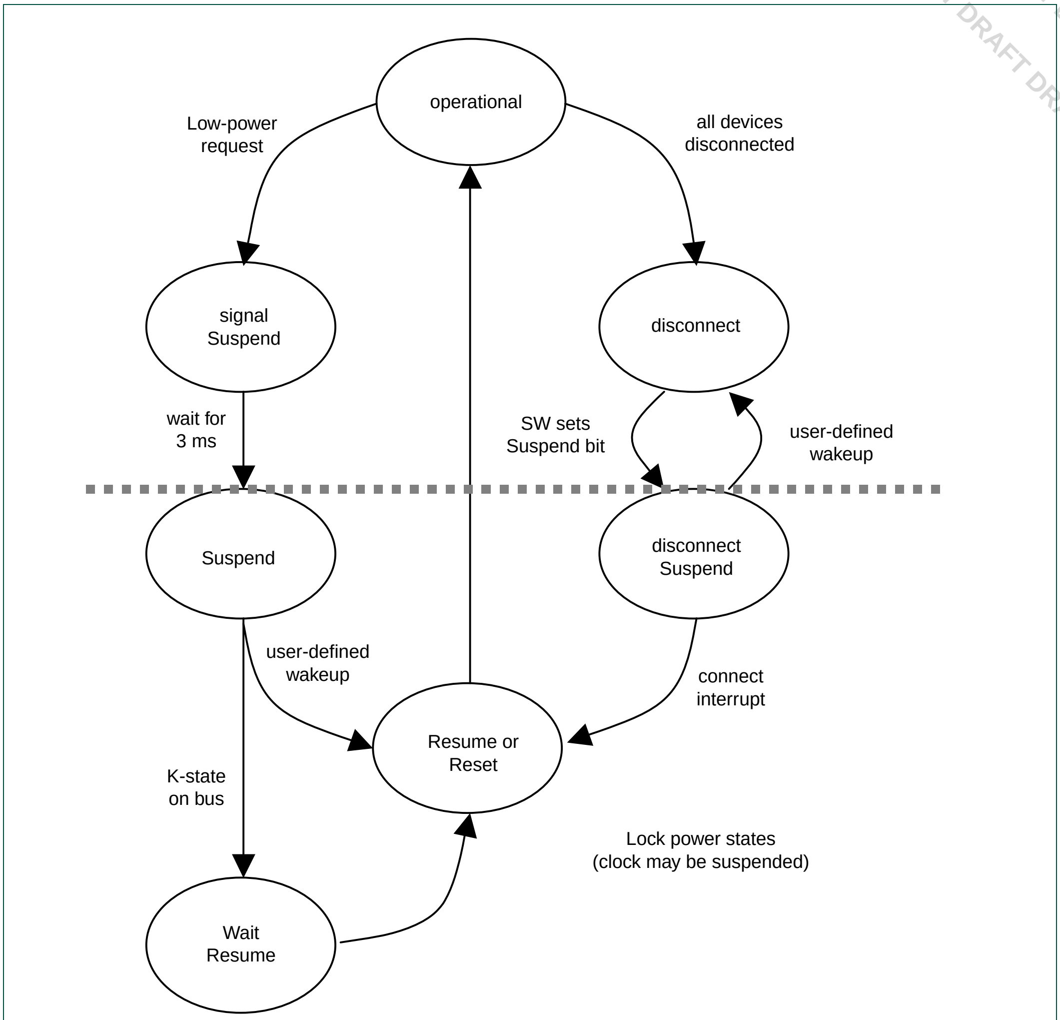


Fig 43. Host/OTG power state diagram

From an operational state when a host gets a low power request, it must set the suspend bit in the port controller. This will put an idle on the bus, block all traffic through the port, and turn off the transceiver clock. There are two ways for a host controller to get out of the suspend state. If it has enabled remote wake-up, a K-state on the bus will turn the transceiver clock and generate an interrupt. The software will then have to wait 20 ms for the resume to complete and the port to go back to an active state. Alternatively an external event could clear the suspend bit and start the transceiver clock running again. The software can then initiate a resume by setting the resume bit in the port controller, or force a reconnect by setting the reset bit in the port controller.

If all devices have disconnected from the host, the host can go into a low power mode by the software setting the suspend bit. From the disconnect-suspend state a connect event would start the transceiver clock and interrupt the software. The software would then need to set the reset bit to start the connect process.

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20.11.4 Susp_CTRL module

The SUSP_CTRL module implements the power management logic of USB-OTG. It controls the suspend input of the transceiver. Asserting this suspend signal will put the transceiver in suspend mode and the generation of the 30 MHz clock and 60 MHz clock will be switched off.

A suspend control input of the transceiver (otg_on) that was previously tied high and prevented the transceiver to go into full suspend mode, has been connected to <tbd>. This bit is low by default and only needs to be set high in OTG Host mode operation.

In suspend mode, the transceiver will raise an output signal indicating that the PLL generating the 480 MHz clock can be switched off.

The SUSP_CTRL module also generates an output signal indicating whether the AHB clock is needed or not. If '0' the AHB clock is allowed to be switched off or reduced in frequency in order to save power.

The core will enter the low power state if:

- Software sets the PORTSC.PHCD bit.

When operating in host mode, the core will leave the low power state on one of the following conditions:

- software clears the PORTSC.PHCD bit
- a device is connected and the PORTSC.WKCN bit is set
- a device is disconnected an the PORTSC.WKDC bit is set
- an over-current condition occurs and the PORTSC.WKOC bit is set
- a remote wake-up from the attached device occurs (when USB bus was in suspend)
- a change on vbusvalid occurs (= VBUS threshold at 4.4 V is crossed)
- a change on bvalid occurs (=VBUS threshold at 4.0 V is crossed).

When operating in device mode, the core will leave the low power state on one of the following conditions:

- software clears the PORTSC.PHCD bit.
- a change on the USB data lines (dp/dm) occurs.
- a change on vbusvalid occurs (= VBUS threshold at 4.4 V is crossed).
- a change on bvalid occurs (= VBUS threshold at 4.0 V is crossed).

The vbusvalid and bvalid signals coming from the transceiver are not filtered in the SUSP_CTRL module. Any change on those signals will cause a wake-up event.

Input signals 'host_wakeup_n' and 'dev_wakeup_n' are extra external wake-up signals (for host mode and device mode respectively). However the detection of all USB related wake-up events is already handled in the SUSP_CTRL mode. Therefore in normal situations these signals can be tied high (= inactive).

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21.1 How to read this chapter

The USB1 Host/Device controller is available on parts LPC1850 and LPC1830.

21.2 Basic configuration

The USB1 controller is configured as follows:

- See Table 358 for clocking and power control.
- The USB1 is reset by a USB1_RST (reset # 18).
- The USB1 OTG interrupt is connected to interrupt slot # 9 in the NVIC. The USB wake-up interrupt is connected to slot # 10 in the event router.
- In the SFSUSB register, the USB_ESEA bit must be set to 1 for the USB1 to operate (see Table 204).

Table 358. USB1 clocking and power control

	Base clock	Branch clock	Maximum frequency	Notes
USB1 clock	BASE_USB1_CLK	CLK_USB1	150 MHz	Uses PLL1 only. CLK_USB1 must be 60 MHz when the USB1 is operated at low-speed and full-speed modes. In high-speed mode, the clock is provided by the ULPI PHY.
USB1 register interface clock	BASE_M3_CLK	CLK_M3_USB1	150 MHz	

21.2.1 Full-speed mode without external PHY

In Full-speed mode, use CLK_USB1 to generate a clock for the USB1 interface.

21.2.2 High-speed mode with ULPI interface

In High-speed mode, the external PHY generates the clock for the USB1 interface, and the USB1_ULPI_CLK must be enabled on pins PC_0 or P8_8 through their respective pin configuration registers in the system configuration block. The USB1 branch clock CLK_USB1 must be disabled.

21.3 Features

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals if connected to external ULPI PHY.

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- Supports all full-speed USB-compliant peripherals.
- Supports interrupts.
- This module has its own, integrated DMA engine.

21.4 General description

The High Speed-On-The-Go Controller is a peripheral for embedded applications containing digital circuitry to provide USB2.0 On-The-Go functionality.

USB2.0 provides plug-and-play connection of peripheral devices to a host with three different data speeds: High-Speed with a data rate of 480 Mbps, Full-Speed with a data rate of 12 Mbps, Low-Speed with a data rate of 1.5 Mbps. Many portable devices can benefit from the ability to communicate to each other over the USB interface without intervention of a host PC. The addition of the On-The-Go functionality to USB makes this possible without losing the benefits of the standard USB protocol.

Support of the High-Speed data rate and the OTG functionality requires an external USB HS OTG PHY that connects to the USB controller via the ULPI interface. Full-Speed or Low-Speed is supported through the on-chip Full-speed PHY.

21.5 Pin description

Table 359. USB1 pin description

Function name	Direction	Description
USB1_DP	I/O	USB1 bidirectional D+ line.
USB1_DM	I/O	USB1 bidirectional D− line.
USB1_VBUS	I	VBUS pin (power on USB cable).
USB1_VBUS_EN	O	VBUS power enable.
USB1_IND0	O	Port indicator LED control output 0.
USB1_IND1	O	Port indicator LED control output 1.
USB1_PWR_FAULT	I	Port power fault signal indicating over-current condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
ULPI pins		
ULPI_DATA[7:0]	I/O	ULPI link 8-bit bidirectional data bus timed on the rising clock edge.
ULPI_STP	O	ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
ULPI_NXT	I	ULPI link NXT signal. Data flow control signal from the PHY.
ULPI_DIR	I	ULPI link DIR signal. Controls the DATA bus direction.
ULPI_CLK	I	ULPI link CLK signal. 60 MHz clock generated by the PHY.

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21.6 Register description

Remark: For Full-speed operation with on-chip Full-speed PHY, the pads of the PHY need to be configured. For configuration of these pads see Section 19.3.4 “USB1 DP1/DM1 pins”.

Remark: For operations with an external PHY connected through the ULPI interface the interface needs to be selected in the PTS bits of the PORTSC1 register (Section 21.6.15).

Table 360. Register access abbreviations

Abbreviation	Description
R/W	Read/Write
R/WC	Read/Write one to Clear
R/WO	Read/Write Once
RO	Read Only
WO	Write Only

Table 361. Register overview: USB1 host/device controller (register base address 0x4000 7000)

Name	Access	Address offset	Description	Reset value
-	-	0x000 - 0x0FF	Reserved	
Device/host capability registers				
CAPLENGTH	RO	0x100	Capability register length	0x0001 0040
HCSPARAMS	RO	0x104	Host controller structural parameters	0x0001 0011
HCCPARAMS	RO	0x108	Host controller capability parameters	0x0000 0005
DCIVERSION	RO	0x120	Device interface version number	0x0000 0001
DCCPARAMS	RO	0x124	Device controller capability parameters	0x0000 0184
-	-	0x128 - 0x13C	Reserved	
Device/host operational registers				
USBCMD_D	R/W	0x140	USB command (device mode)	0x0004 0000
USBCMD_H	R/W	0x140	USB command (host mode)	0x0004 00B0
USBSTS_D	R/W	0x144	USB status (device mode)	0x0000 0000
USBSTS_H	R/W	0x144	USB status (host mode)	0x0000 1000
USBINTR_D	R/W	0x148	USB interrupt enable (device mode)	0x0000 0000
USBINTR_H	R/W	0x148	USB interrupt enable (host mode)	0x0000 0000
FRINDEX_D	RO	0x14C	USB frame index (device mode)	0x0000 0000
FRINDEX_H	R/W	0x14C	USB frame index (host mode)	0x0000 0000
-	-	0x150	Reserved	
DEVICEADDR	R/W	0x154	USB device address	0x0000 0000
PERIODICLISTBASE	R/W	0x154	Frame list base address	0x0000 0000
ENDPOINTLISTADDR	R/W	0x158	Address of endpoint list in memory (device mode)	0x0000 0000
ASYNCLISTADDR	R/W	0x158	Address of endpoint list in memory (host mode)	0x0000 0000

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Table 361. Register overview: USB1 host/device controller (register base address 0x4000 7000) *…continued*

Name	Access	Address offset	Description	Reset value
TTCTRL	R/W	0x15C	Asynchronous buffer status for embedded TT (host mode)	0x0000 0000
BURSTSIZE	R/W	0x160	Programmable burst size	0x0000 0000
TXFILLTUNING	R/W	0x164	Host transmit pre-buffer packet tuning (host mode)	0x0000 0000
-	-	0x168 - 0x16C	Reserved	
ULPIVIEWPORT	R/W	0x170	ULPI viewport	0x0000 0000
BINTERVAL	R/W	0x174	Length of virtual frame	0x0000 0000
ENDPTNAK	R/W	0x178	Endpoint NAK (device mode)	0x0000 0000
ENDPTNAKEN	R/W	0x17C	Endpoint NAK Enable (device mode)	0x0000 0000
CONFIGFLAG	RO	0x180	Configured flag register	0x0000 0000
PORTSC1_D	R/W	0x184	Port 1 status/control (device mode)	0x0000 0000
PORTSC1_H	R/W	0x184	Port 1 status/control (host mode)	0x0000 0000
-	-	0x188 - 0x1A0	-	
-	-	0x1A4	-	
USBMODE_D	R/W	0x1A8	USB mode (device mode)	0x0000 0000
USBMODE_H	R/W	0x1A8	USB mode (host mode)	0x0000 0000
Device endpoint registers				
ENDPTSETUPSTAT	R/W	0x1AC	Endpoint setup status	0x0000 0000
ENDPTPRIME	R/W	0x1B0	Endpoint initialization	0x0000 0000
ENDPTFLUSH	R/W	0x1B4	Endpoint de-initialization	0x0000 0000
ENDPTSTAT	RO	0x1B8	Endpoint status	0x0000 0000
ENDPTCOMPLETE	R/W	0x1BC	Endpoint complete	0x0000 0000
ENDPTCTRL0	R/W	0x1C0	Endpoint control 0	0x0000 0000
ENDPTCTRL1	R/W	0x1C4	Endpoint control 1	0x0000 0000
ENDPTCTRL2	R/W	0x1C8	Endpoint control 2	0x0000 0000
ENDPTCTRL3	R/W	0x1CC	Endpoint control 3	0x0000 0000

21.6.1 Device/host capability registers

Table 362. CAPLENGTH register (CAPLENGTH - address 0x4000 7100) bit description

Bit	Symbol	Description	Reset value	Access
7:0	CAPLENGTH	Indicates offset to add to the register base address at the beginning of the Operational Register	0x40	RO
23:8	HCIVERSION	BCD encoding of the EHCI revision number supported by this host controller.	0x100	RO
31:24	-	These bits are reserved and should be set to zero.	-	-

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Table 363. HCSPARAMS register (HCSPARAMS - address 0x4000 7104) bit description

Bit	Symbol	Description	Reset value	Access
3:0	N_PORTS	Number of downstream ports. This field specifies the number of physical downstream ports implemented on this host controller.	0x1	RO
4	PPC	Port Power Control. This field indicates whether the host controller implementation includes port power control.	0x1	RO
7:5	-	These bits are reserved and should be set to zero.	-	-
11:8	N_PCC	Number of Ports per Companion Controller. This field indicates the number of ports supported per internal Companion Controller.	0x0	RO
15:12	N_CC	Number of Companion Controller. This field indicates the number of companion controllers associated with this USB2.0 host controller.	0x0	RO
16	PI	Port indicators. This bit indicates whether the ports support port indicator control.	0x1	RO
19:17	-	These bits are reserved and should be set to zero.	-	-
23:20	N_PTT	Number of Ports per Transaction Translator. This field indicates the number of ports assigned to each transaction translator within the USB2.0 host controller.	0x0	RO
27:24	N_TT	Number of Transaction Translators. This field indicates the number of embedded transaction translators associated with the USB2.0 host controller.	0x0	RO
31:28	-	These bits are reserved and should be set to zero.	-	-

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Table 364. HCCPARAMS register (HCCPARAMS - address 0x4000 7108) bit description

Bit	Symbol	Description	Reset value	Access
0	ADC	64-bit Addressing Capability. If zero, no 64-bit addressing capability is supported.	0	RO
1	PFL	Programmable Frame List Flag. If set to one, then the system software can specify and use a smaller frame list and configure the host controller via the USBCMD register Frame List Size field. The frame list must always be aligned on a 4K-boundary. This requirement ensures that the frame list is always physically contiguous.	1	RO
2	ASP	Asynchronous Schedule Park Capability. If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule.The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.	1	RO
7:4	IST	Isochronous Scheduling Threshold. This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule.	0	RO
15:8	EECP	EHCI Extended Capabilities Pointer. This optional field indicates the existence of a capabilities list.	0	RO
31:9	-	These bits are reserved and should be set to zero.	-	-

Table 365. DCIVERSION register (DCIVERSION - address 0x4000 7120) bit description

Bit	Symbol	Description	Reset value	Access
15:0	DCIVERSION	The device controller interface conforms to the two-byte BCD encoding of the interface version number contained in this register.	0x1	RO
31:16	-	These bits are reserved and should be set to zero.	-	-

Table 366. DCCPARAMS (address 0x4000 7124)

Bit	Symbol	Description	Reset value	Access
4:0	DEN	Device Endpoint Number.	0x4	RO
6:5	-	These bits are reserved and should be set to zero.	-	-
7	DC	Device Capable.	0x1	RO
8	HC	Host Capable.	0x1	RO
31:9	-	These bits are reserved and should be set to zero.	-	-

21.6.2 USB Command register (USBCMD)

The host/device controller executes the command indicated in this register.

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21.6.2.1 Device mode

Table 367. USB Command register in device mode (USBCMD_D - address 0x4000 7140) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	RS		Run/Stop	0	R/W
		0	Writing a 0 to this bit will cause a detach event.		
		1	Writing a one to this bit will cause the device controller to enable a pull-up on USB_DP and initiate an attach event. This control bit is not directly connected to the pull-up enable, as the pull-up will become disabled upon transitioning into high-speed mode. Software should use this bit to prevent an attach event before the device controller has been properly initialized.		
1	RST		Controller reset. Software uses this bit to reset the controller. This bit is set to zero by the Host/Device Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register.	0	R/W
		0	Set to 0 by hardware when the reset process is complete.		
		1	When software writes a one to this bit, the Device Controller resets its internal pipelines, timers, counters, state machines etc. to their initial values. Writing a one to this bit when the device is in the attached state is not recommended, since the effect on an attached host is undefined. In order to ensure that the device is not in an attached state before initiating a device controller reset, all primed endpoints should be flushed and the USBCMD Run/Stop bit should be set to 0.		
3:2	-		Not used in device mode.	0	-
4	-		Not used in device mode.	0	-
5	-		Not used in device mode.	0	-
6	-		Not used in device mode. Writing a one to this bit when the device mode is selected, will have undefined results.	-	-
7	-	-	Reserved. These bits should be set to 0.	-	-
9:8	-	-	Not used in Device mode.	-	-
10	-		Reserved.These bits should be set to 0.	0	-
11	-	-	Not used in Device mode.		-
12	-		Reserved.These bits should be set to 0.	0	-
13	SUTW		Setup trip wire During handling a setup packet, this bit is used as a semaphore to ensure that the setup data payload of 8 bytes is extracted from a QH by the DCD without being corrupted. If the setup lockout mode is off (see USBMODE register) then there exists a hazard when new setup data arrives while the DCD is copying the setup data payload from the QH for a previous setup packet. This bit is set and cleared by software and will be cleared by hardware when a hazard exists. (See Section 20.10).	0	R/W
14	ATDTW		Add dTD trip wire This bit is used as a semaphore to ensure the to proper addition of a new dTD to an active (primed) endpoint's linked list. This bit is set and cleared by software during the process of adding a new dTD. See also Section 20.10. This bit shall also be cleared by hardware when its state machine is hazard region for which adding a dTD to a primed endpoint may go unrecognized.	0	R/W

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Table 367. USB Command register in device mode (USBCMD_D - address 0x4000 7140) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
15	FS2		Not used in device mode.	-	-
23:16	ITC		Interrupt threshold control. The system software uses this field to set the maximum rate at which the host/device controller will issue interrupts. ITC contains the maximum interrupt interval measured in micro-frames. Valid values are shown below. All other values are reserved. 0x0 = Immediate (no threshold) 0x1 = 1 micro frame. 0x2 = 2 micro frames. 0x8 = 8 micro frames. 0x10 = 16 micro frames. 0x20 = 32 micro frames. 0x40 = 64 micro frames.	0x8	R/W
31:24	-		Reserved	0	

21.6.2.2 Host mode

Table 368. USB Command register in host mode (USBCMD_H - address 0x4000 7140) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	RS		Run/Stop	0	R/W
		0	When this bit is set to 0, the Host Controller completes the current transaction on the USB and then halts. The HC Halted bit in the status register indicates when the Host Controller has finished the transaction and has entered the stopped state. Software should not write a one to this field unless the host controller is in the Halted state (i.e. HCHalted in the USBSTS register is a one).		
		1	When set to a 1, the Host Controller proceeds with the execution of the schedule. The Host Controller continues execution as long as this bit is set to a one.		
1	RST		Controller reset. Software uses this bit to reset the controller. This bit is set to zero by the Host/Device Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register.	0	R/W
		0	This bit is set to zero by hardware when the reset process is complete.		
		1	When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. Software should not set this bit to a one when the HCHalted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.		
2	FS0		Bit 0 of the Frame List Size bits. See Table 369. This field specifies the size of the frame list that controls which bits in the Frame Index Register should be used for the Frame List Current index. Note that this field is made up from USBCMD bits 15, 3, and 2.	0	
3	FS1		Bit 1 of the Frame List Size bits. See Table 369	0	

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Table 368. USB Command register in host mode (USBCMD_H - address 0x4000 7140) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
4	PSE		This bit controls whether the host controller skips processing the periodic schedule.	0	R/W
		0	Do not process the periodic schedule.		
		1	Use the PERIODICLISTBASE register to access the periodic schedule.		
5	ASE		This bit controls whether the host controller skips processing the asynchronous schedule.	0	R/W
		0	Do not process the asynchronous schedule.		
		1	Use the ASYNCLISTADDR to access the asynchronous schedule.		
6	IAA		This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule.	0	R/W
		0	The host controller sets this bit to zero after it has set the Interrupt on Sync Advance status bit in the USBSTS register to one.		
		1	Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule states, it sets the Interrupt on Async Advance status bit in the USBSTS register. If the Interrupt on Sync Advance Enable bit in the USBINTR register is one, then the host controller will assert an interrupt at the next interrupt threshold. Software should not write a one to this bit when the asynchronous schedule is inactive. Doing so will yield undefined results.		
7	-	-	Reserved	0	
9:8	ASP1_0		Asynchronous schedule park mode. Contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid values are 0x1 to 0x3. **Remark:** Software must not write 00 to this bit when Park Mode Enable is one as this will result in undefined behavior.	11	R/W
10	-	-	Reserved.	0	-
11	ASPE		Asynchronous Schedule Park Mode Enable	1	R/W
		0	Park mode is disabled.		
		1	Park mode is enabled.		
12	-	-	Reserved.	0	-
13	-	-	Not used in Host mode.		-
14	-	-	Reserved.	0	-

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Table 368. USB Command register in host mode (USBCMD_H - address 0x4000 7140) bit description ...continued

Bit	Symbol	Value	Description	Reset value	Access
15	FS2		Bit 2 of the Frame List Size bits. See Table 369.	0	-
23:16	ITC		Interrupt threshold control. The system software uses this field to set the maximum rate at which the host/device controller will issue interrupts. ITC contains the maximum interrupt interval measured in micro-frames. Valid values are shown below. All other values are reserved. 0x0 = Immediate (no threshold) 0x1 = 1 micro frame. 0x2 = 2 micro frames. 0x8 = 8 micro frames. 0x10 = 16 micro frames. 0x20 = 32 micro frames. 0x40 = 64 micro frames.	0x8	R/W
31:24	-		Reserved	0	

Table 369. Frame list size values

USBCMD bit 15	USBCMD bit 3	USBCMD bit 2	Frame list size
0	0	0	1024 elements (4096 bytes) - default value
0	0	1	512 elements (2048 bytes)
0	1	0	256 elements (1024 bytes)
0	1	1	128 elements (512 bytes)
1	0	0	64 elements (256 bytes)
1	0	1	32 elements (128 bytes)
1	1	0	16 elements (64 bytes)
1	1	1	8 elements (32 bytes)

21.6.3 USB Status register (USBSTS)

This register indicates various states of the Host/Device controller and any pending interrupts. Software sets a bit to zero in this register by writing a one to it.

Remark: This register does not indicate status resulting from a transaction on the serial bus.

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21.6.3.1 Device mode

Table 370. USB Status register in device mode (USBSTS_D - address 0x4000 7144) register bit description

Bit	Symbol	Value	Description	Reset value	Access
0	UI		USB interrupt	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	This bit is set by the Host/Device Controller when the cause of an interrupt is a completion of a USB transaction where the Transfer Descriptor (TD) has an interrupt on complete (IOC) bit set. This bit is also set by the Host/Device Controller when a short packet is detected. A short packet is when the actual number of bytes received was less than the expected number of bytes.		
1	UEI		USB error interrupt	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	When completion of a USB transaction results in an error condition, this bit is set by the Host/Device Controller. This bit is set along with the USBINT bit, if the TD on which the error interrupt occurred also had its interrupt on complete (IOC) bit set. The device controller detects resume signaling only (see Section 20.10.11.6).		
2	PCI		Port change detect.	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	The Device Controller sets this bit to a one when the port controller enters the full or high-speed operational state. When the port controller exits the full or high-speed operation states due to Reset or Suspend events, the notification mechanisms are the USB Reset Received bit (URI) and the DCSuspend bits (SLI) respectively.		
3	-		Not used in Device mode.		
4	-	0	Reserved.		
5	-		Not used in Device mode.	0	-
6	URI		USB reset received	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	When the device controller detects a USB Reset and enters the default state, this bit will be set to a one.		

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Table 370. USB Status register in device mode (USBSTS_D - address 0x4000 7144) register bit description

Bit	Symbol	Value	Description	Reset value	Access
7	SRI		SOF received	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	When the device controller detects a Start Of (micro) Frame, this bit will be set to a one. When a SOF is extremely late, the device controller will automatically set this bit to indicate that an SOF was expected. Therefore, this bit will be set roughly every 1 ms in device FS mode and every 125 μs in HS mode and will be synchronized to the actual SOF that is received. Since the device controller is initialized to FS before connect, this bit will be set at an interval of 1ms during the prelude to connect and chirp.		
8	SLI		DCSuspend	0	R/WC
		0	The device controller clears the bit upon exiting from a suspend state. This bit is cleared by software writing a one to it.		
		1	When a device controller enters a suspend state from an active state, this bit will be set to a one.		
11:9	-	-	Reserved. Software should only write 0 to reserved bits.	0	
12	-	-	Not used in Device mode.	0	
13	-	-	Not used in Device mode.	0	
14	-	-	Not used in Device mode.	0	
15	-	-	Not used in Device mode.	0	
16	NAKI		NAK interrupt bit	0	RO
		0	This bit is automatically cleared by hardware when the all the enabled TX/RX Endpoint NAK bits are cleared.		
		1	It is set by hardware when for a particular endpoint both the TX/RX Endpoint NAK bit and the corresponding TX/RX Endpoint NAK Enable bit are set.		
17	-	-	Reserved. Software should only write 0 to reserved bits.	0	-
18	-		Not used in Device mode.	0	-
19	-		Not used in Device mode.	0	-
31:20	-	-	Reserved. Software should only write 0 to reserved bits.		-

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21.6.3.2 Host mode

Table 371. USB Status register in host mode (USBSTS_H - address 0x4000 7144) register bit description

Bit	Symbol	Value	Description	Reset value	Access
0	UI		USB interrupt (USBINT)	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	This bit is set by the Host/Device Controller when the cause of an interrupt is a completion of a USB transaction where the Transfer Descriptor (TD) has an interrupt on complete (IOC) bit set. This bit is also set by the Host/Device Controller when a short packet is detected. A short packet is when the actual number of bytes received was less than the expected number of bytes.		
1	UEI		USB error interrupt (USBERRINT)	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	When completion of a USB transaction results in an error condition, this bit is set by the Host/Device Controller. This bit is set along with the USBINT bit, if the TD on which the error interrupt occurred also had its interrupt on complete (IOC) bit set.		
2	PCI		Port change detect.	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	The Host Controller sets this bit to a one when on any port a Connect Status occurs, a Port Enable/Disable Change occurs, or the Force Port Resume bit is set as the result of a J-K transition on the suspended port.		
3	FRI		Frame list roll-over	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the Frame List Size field of the USBCMD register) is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX bit 12 toggles (see Section 21.6.5).		
4	-	0	Reserved.		
5	AAI		Interrupt on async advance	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.		
6	-	-	Not used by the Host controller.	0	R/WC
7	SRI		SOF received	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	In host mode, this bit will be set every 125 μs and can be used by host controller driver as a time base.		
8	SLI	-	Not used by the Host controller.	-	-
11:9	-	-	Reserved.		

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Table 371. USB Status register in host mode (USBSTS_H - address 0x4000 7144) register bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
12	HCH		HCHalted	1	RO
		0	The RS bit in USBCMD is set to zero. Set by the host controller.		
		1	The Host Controller sets this bit to one after it has stopped executing because of the Run/Stop bit being set to 0, either by software or by the Host Controller hardware (e.g. because of an internal error).		
13	RCL		Reclamation	0	RO
		0	No empty asynchronous schedule detected.		
		1	An empty asynchronous schedule is detected. Set by the host controller.		
14	PS		Periodic schedule status This bit reports the current real status of the Periodic Schedule. The Host Controller is not required to immediately disable or enable the Periodic Schedule when software transitions the Periodic Schedule Enable bit in the USBCMD register. When this bit and the Periodic Schedule Enable bit are the same value, the Periodic Schedule is either enabled (if both are 1) or disabled (if both are 0).	0	RO
		0	The periodic schedule status is disabled.		
		1	The periodic schedule status is enabled.		
15	AS		Asynchronous schedule status This bit reports the current real status of the Asynchronous Schedule. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (if both are 1) or disabled (if both are 0).	0	
		0	Asynchronous schedule status is disabled.		
		1	Asynchronous schedule status is enabled.		
16	-		Not used on Host mode.	0	-
17	-		Reserved.		
18	UAI		USB host asynchronous interrupt (USBHSTASYNCINT)	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	This bit is set by the Host Controller when the cause of an interrupt is a completion of a USB transaction where the Transfer Descriptor (TD) has an interrupt on complete (IOC) bit set **and** the TD was from the asynchronous schedule. This bit is also set by the Host when a short packet is detected **and** the packet is on the asynchronous schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes.		
19	UPI		USB host periodic interrupt (USBHSTPERINT)	0	R/WC
		0	This bit is cleared by software writing a one to it.		
		1	This bit is set by the Host Controller when the cause of an interrupt is a completion of a USB transaction where the Transfer Descriptor (TD) has an interrupt on complete (IOC) bit set **and** the TD was from the periodic schedule. This bit is also set by the Host Controller when a short packet is detected **and** the packet is on the periodic schedule. A short packet is when the actual number of bytes received was less than the expected number of bytes.		
31:20	-		Reserved.	-	-

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21.6.4 USB Interrupt register (USBINTR)

The software interrupts are enabled with this register. An interrupt is generated when a bit is set and the corresponding interrupt is active. The USB Status register (USBSTS) still shows interrupt sources even if they are disabled by the USBINTR register, allowing polling of interrupt events by the software. All interrupts must be acknowledged by software by clearing (that is writing a 1 to) the corresponding bit in the USBSTS register.

21.6.4.1 Device mode

Table 372. USB Interrupt register in device mode (USBINTR_D - address 0x4000 7148) bit description

Bit	Symbol	Description	Reset value	Access
0	UE	USB interrupt enable When this bit is one, and the USBINT bit in the USBSTS register is one, the host/device controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit in USBSTS.	0	R/W
1	UEE	USB error interrupt enable When this bit is a one, and the USBERRINT bit in the USBSTS register is a one, the host/device controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit in the USBSTS register.	0	R/W
2	PCE	Port change detect enable When this bit is a one, and the Port Change Detect bit in the USBSTS register is a one, the host/device controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit in USBSTS.	0	R/W
3	-	Not used by the Device controller.		
4	-	Reserved	0	-
5	-	Not used by the Device controller.		
6	URE	USB reset enable When this bit is a one, and the USB Reset Received bit in the USBSTS register is a one, the device controller will issue an interrupt. The interrupt is acknowledged by software clearing the USB Reset Received bit.	0	R/W
7	SRE	SOF received enable When this bit is a one, and the SOF Received bit in the USBSTS register is a one, the device controller will issue an interrupt. The interrupt is acknowledged by software clearing the SOF Received bit.	0	R/W
8	SLE	Sleep enable When this bit is a one, and the DCSuspend bit in the USBSTS register transitions, the device controller will issue an interrupt. The interrupt is acknowledged by software writing a one to the DCSuspend bit.	0	R/W
15:9	-	Reserved	-	-
16	NAKE	NAK interrupt enable This bit is set by software if it wants to enable the hardware interrupt for the NAK Interrupt bit. If both this bit and the corresponding NAK Interrupt bit are set, a hardware interrupt is generated.	0	R/W
17	-	Reserved		
18	UAIE	Not used by the Device controller.		
19	UPIA	Not used by the Device controller.		
31:20	-	Reserved		

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21.6.4.2 Host mode

Table 373. USB Interrupt register in host mode (USBINTR_H - address 0x4000 7148) bit description

Bit	Symbol	Description	Access	Reset value
0	UE	USB interrupt enable When this bit is one, and the USBINT bit in the USBSTS register is one, the host/device controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit in USBSTS.	R/W	0
1	UEE	USB error interrupt enable When this bit is a one, and the USBERRINT bit in the USBSTS register is a one, the host/device controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit in the USBSTS register.	R/W	0
2	PCE	Port change detect enable When this bit is a one, and the Port Change Detect bit in the USBSTS register is a one, the host/device controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit in USBSTS.	R/W	0
3	FRE	Frame list rollover enable When this bit is a one, and the Frame List Rollover bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.		
4	-	Reserved	-	0
5	AAE	Interrupt on asynchronous advance enable When this bit is a one, and the Interrupt on Async Advance bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.	R/W	0
6	-	Not used by the Host controller.	-	0
7	SRE	If this bit is one and the SRI bit in the USBSTS register is one, the host controller will issue an interrupt. In host mode, the SRI bit will be set every 125 μs and can be used by the host controller as a time base. The interrupt is acknowledged by software clearing the SRI bit in the USBSTS register.	-	0
8	-	Not used by the Host controller.	-	0
15:9	-	Reserved		
16	-	Not used by the host controller.	R/W	0
17	-	Reserved		
18	UAIE	USB host asynchronous interrupt enable When this bit is a one, and the USBHSTASYNCINT bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBHSTASYNCINT bit.	R/W	0
19	UPIA	USB host periodic interrupt enable When this bit is a one, and the USBHSTPERINT bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBHSTPERINT bit.	R/W	0
31:20	-	Reserved		

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21.6.5 Frame index register (FRINDEX)

21.6.5.1 Device mode

In Device mode this register is read only, and the device controller updates the FRINDEX[13:3] register from the frame number indicated by the SOF marker. Whenever a SOF is received by the USB bus, FRINDEX[13:3] will be checked against the SOF marker. If FRINDEX[13:3] is different from the SOF marker, FRINDEX[13:3] will be set to the SOF value and FRINDEX[2:0] will be set to zero (i.e. SOF for 1 ms frame). If FRINDEX [13:3] is equal to the SOF value, FRINDEX[2:0] will be incremented (i.e. SOF for 125 μs micro-frame) by hardware.

Table 374. USB frame index register in device mode (FRINDEX_D - address 0x4000 714C) bit description

Bit	Symbol	Description	Reset value	Access
2:0	FRINDEX2_0	Current micro frame number	-	RO
13:3	FRINDEX13_3	Current frame number of the last frame transmitted	-	RO
31:14	-	Reserved	-	

21.6.5.2 Host mode

This register is used by the host controller to index the periodic frame list. The register updates every 125 μs (once each micro-frame). Bits[N: 3] are used to select a particular entry in the Periodic Frame List during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by system software in the Frame List Size field in the USBCMD register.

This register must be written as a DWord. Byte writes produce undefined results. This register cannot be written unless the Host Controller is in the 'Halted' state as indicated by the HCHalted bit in the USBSTS register (host mode). A write to this register while the Run/Stop bit is set to a one produces undefined results. Writes to this register also affect the SOF value.

Table 375. USB frame index register in host mode (FRINDEX_H - address 0x4000 714C) bit description

Bit	Symbol	Description	Reset value	Access
2:0	FRINDEX2_0	Current micro frame number	-	R/W
12:3	FRINDEX12_3	Frame list current index for 1024 elements.	-	R/W
31:13	-	Reserved	-	

Table 376. Number of bits used for the frame list index

USBCMD bit 15	USBCMD bit 3	USBCMD bit 2	Frame list size	Size of FRINDEX12_3 bit field
0	0	0	1024 elements (4096 bytes). Default value.	12
0	0	1	512 elements (2048 bytes)	11
0	1	0	256 elements (1024 bytes)	10
0	1	1	128 elements (512 bytes)	9
1	0	0	64 elements (256 bytes)	8

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Table 376. Number of bits used for the frame list index

USBCMD bit 15	USBCMD bit 3	USBCMD bit 2	Frame list size	Size of FRINDEX12_3 bit field
1	0	1	32 elements (128 bytes)	7
1	1	0	16 elements (64 bytes)	6
1	1	1	8 elements (32 bytes)	5

21.6.6 Device address (DEVICEADDR) and Periodic List Base (PERIODICLISTBASE) registers

21.6.6.1 Device mode

The upper seven bits of this register represent the device address. After any controller reset or a USB reset, the device address is set to the default address (0). The default address will match all incoming addresses. Software shall reprogram the address after receiving a SET_ADDRESS descriptor.

The USBADRA bit is used to accelerate the SET_ADDRESS sequence by allowing the DCD to preset the USBADR register bits before the status phase of the SET_ADDRESS descriptor.

Table 377. USB Device Address register in device mode (DEVICEADDR - address 0x4000 7154) bit description

Bit	Symbol	Value	Description	Reset value	Access
23:0	-		reserved	0	-
24	USBADRA		Device address advance		
		0	Any write to USBADR are instantaneous.		
		1	When the user writes a one to this bit at the same time or before USBADR is written, the write to USBADR fields is staged and held in a hidden register. After an IN occurs on endpoint 0 and is acknowledged, USBADR will be loaded from the holding register. Hardware will automatically clear this bit on the following conditions: • IN is ACKed to endpoint 0. USBADR is updated from the staging register. • OUT/SETUP occurs on endpoint 0. USBADR is **not** updated. • Device reset occurs. USBADR is set to 0. **Remark:** After the status phase of the SET_ADDRESS descriptor, the DCD has 2 ms to program the USBADR field. This mechanism will ensure this specification is met when the DCD can not write the device address within 2 ms from the SET_ADDRESS status phase. If the DCD writes the USBADR with USBADRA=1 after the SET_ADDRESS data phase (before the prime of the status phase), the USBADR will be programmed instantly at the correct time and meet the 2 ms USB requirement.		
31:25	USBADR		USB device address	0	R/W

21.6.6.2 Host mode

This 32-bit register contains the beginning address of the Periodic Frame List in the system memory. The host controller driver (HCD) loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this

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physical memory pointer is assumed to be 4 kB aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.

Table 378. USB Periodic List Base register in host mode (PERIODICLISTBASE - address 0x4000 7154) bit description

Bit	Symbol	Description	Reset value	Access
11:0	-	Reserved	N/A	-
31:12	PERBASE31_12	Base Address (Low) These bits correspond to the memory address signals[31:12].	N/A	R/W

21.6.7 Endpoint List Address register (ENDPOINTLISTADDR) and Asynchronous List Address (ASYNCLISTADDR) registers

21.6.7.1 Device mode

In device mode, this register contains the address of the top of the endpoint list in system memory. Bits[10:0] of this register cannot be modified by the system software and will always return a zero when read.The memory structure referenced by this physical memory pointer is assumed 64 byte aligned.

Table 379. USB Endpoint List Address register in device mode (ENDPOINTLISTADDR - address 0x4000 7158) bit description

Bit	Symbol	Description	Reset value	Access
10:0	-	reserved	0	-
31:11	EPBASE31_11	Endpoint list pointer (low) These bits correspond to memory address signals 31:11, respectively. This field will reference a list of up to 4 Queue Heads (QH). (i.e. one queue head per endpoint and direction.)	N/A	R/W

21.6.7.2 Host mode

This 32-bit register contains the address of the next asynchronous queue head to be executed by the host. Bits [4:0] of this register cannot be modified by the system software and will always return a zero when read.

Table 380. USB Asynchronous List Address register in host mode (ASYNCLISTADDR- address 0x4000 7158) bit description

Bit	Symbol	Description	Reset value	Access
4:0	-	Reserved	0	-
31:5	ASYBASE31_5	Link pointer (Low) LPL These bits correspond to memory address signals 31:5, respectively. This field may only reference a Queue Head (OH).	-	R/W

21.6.8 TT Control register (TTCTRL)

21.6.8.1 Device mode

This register is not used in device mode.

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21.6.8.2 Host mode

This register contains parameters needed for internal TT operations. This register is used by the host controller only. Writes must be in Dwords.

Table 381. USB TT Control register in host mode (TTCTRL - address 0x4000 715C) bit description

Bit	Symbol	Description	Reset value	Access
23:0	-	Reserved.	0	-
30:24	TTHA	Hub address when FS or LS device are connected directly.	N/A	R/W
31	-	Reserved.	0	

21.6.9 Burst Size register (BURSTSIZE)

This register is used to control and dynamically change the burst size used during data movement on the master interface of the USB DMA controller. Writes must be in Dwords.

The default for the length of a burst of 32-bit words for RX and TX DMA data transfers is 16 words each.

Table 382. USB burst size register in device/host mode (BURSTSIZE - address 0x4000 7160) bit description

Bit	Symbol	Description	Reset value	Access
7:0	RXPBURST	Programmable RX burst length This register represents the maximum length of a burst in 32-bit words while moving data from the USB bus to system memory.	0x10	R/W
15:8	TXPBURST	Programmable TX burst length This register represents the maximum length of a burst in 32-bit words while moving data from system memory to the USB bus.	0x10	R/W
31:16	-	reserved	-	-

21.6.10 Transfer buffer Fill Tuning register (TXFILLTUNING)

21.6.10.1 Device controller

This register is not used in device mode.

21.6.10.2 Host controller

The fields in this register control performance tuning associated with how the host controller posts data to the TX latency FIFO before moving the data onto the USB bus. The specific areas of performance include the how much data to post into the FIFO and an estimate for how long that operation should take in the target system.

Definitions:

T_0 = Standard packet overhead

T_1 = Time to send data payload

T_{ff} = Time to fetch packet into TX FIFO up to specified level

T_s = Total packet flight time (send-only) packet; $T_s = T_0 + T_1$

T_p = Total packet time (fetch and send) packet; $T_p = T_{ff} + T_0 + T_1$

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Upon discovery of a transmit (OUT/SETUP) packet in the data structures, host controller checks to ensure T_p remains before the end of the (micro) frame. If so it proceeds to pre-fill the TX FIFO. If at anytime during the pre-fill operation the time remaining the [micro]frame is < T_s then the packet attempt ceases and the packet is tried at a later time. Although this is not an error condition and the host controller will eventually recover, a mark will be made the scheduler health counter to note the occurrence of a “backoff” event. When a back-off event is detected, the partial packet fetched may need to be discarded from the latency buffer to make room for periodic traffic that will begin after the next SOF. Too many back-off events can waste bandwidth and power on the system bus and thus should be minimized (not necessarily eliminated). Backoffs can be minimized with use of the TSCHHEALTH (T_{ff}) described below.

Table 383. USB Transfer buffer Fill Tuning register in host mode (TXFILLTUNING - address 0x4000 7164) bit description

Bit	Symbol	Description	Reset value	Access
7:0	TXSCHOH	FIFO burst threshold This register controls the number of data bursts that are posted to the TX latency FIFO in host mode before the packet begins on to the bus. The minimum value is 2 and this value should be a low as possible to maximize USB performance. A higher value can be used in systems with unpredictable latency and/or insufficient bandwidth where the FIFO may underrun because the data transferred from the latency FIFO to USB occurs before it can be replenished from system memory. This value is ignored if the Stream Disable bit in USBMODE register is set.	0x2	R/W
12:8	TXSCHEATLTH	Scheduler health counter This register increments when the host controller fails to fill the TX latency FIFO to the level programmed by TXFIFOTHRES before running out of time to send the packet before the next Start-Of-Frame . This health counter measures the number of times this occurs to provide feedback to selecting a proper TXSCHOH. Writing to this register will clear the counter. The maximum value is 31.	0x0	R/W
15:13	-	Reserved	-	-
21:16	TXFIFOTHRES	Scheduler overhead This register adds an additional fixed offset to the schedule time estimator described above as T_{ff}. As an approximation, the value chosen for this register should limit the number of back-off events captured in the TXSCHHEALTH to less than 10 per second in a highly utilized bus. Choosing a value that is too high for this register is not desired as it can needlessly reduce USB utilization. The time unit represented in this register is 1.267 μs when a device is connected in High-Speed Mode. The time unit represented in this register is 6.333 μs when a device is connected in Low/Full Speed Mode.	0x0	R/W
31:22	-	Reserved		

21.6.11 USB ULPI viewport register (ULPIVIEWPORT)

The register provides indirect access to the ULPI PHY register set. Although the core performs access to the ULPI PHY register set, there may be extraordinary circumstances where software may need direct access.

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Remark: WRITES TO THE ULPI THROUGH THE VIEWPORT CAN SUBSTANTIALLY HARM STANDARD USB OPERATIONS. CURRENTLY NO USAGE MODEL HAS BEEN DEFINED WHERE SOFTWARE SHOULD NEED TO EXECUTE WRITES DIRECTLY TO THE ULPI – SEE EXCEPTION REGARDING OPTIONAL FEATURES BELOW.

Remark: EXECUTING READ OPERATIONS THOUGH THE ULPI VIEWPORT SHOULD HAVE NO HARMFUL SIDE EFFECTS TO STANDARD USB OPERATIONS.

There are two operations that can be performed with the ULPI Viewport, wakeup and read /write operations. The wakeup operation is used to put the ULPI interface into normal operation mode and reenable the clock if necessary. A wakeup operation is required before accessing the registers when the ULPI interface is operating in low power mode, serial mode, or carkit mode. The ULPI state can be determined by reading the sync. state bit (ULPISS). If this bit is a one, then ULPI interface is running in normal operation mode and can accept read/write operations. If the ULPISS indicates a 0 then then read/write operations will not be able execute. Undefined behavior will result if ULPISS = 0 and a read or write operation is performed. To execute a wakeup operation, write all 32-bits of the ULPI Viewport where ULPIPORT is constructed appropriately and the ULPIWU bit is a 1 and ULPIRUN bit is a 0. Poll the ULPI Viewport until ULPIWU is zero for the operation to complete.

To execute a read or write operation, write all 32-bits of the ULPI Viewport where ULPIDATWR, ULPIADDR, ULPIPORT, ULPIRW are constructed appropriately and the ULPIRUN bit is a 1. Poll the ULPI Viewport until ULPIRUN is zero for the operation to complete. Once ULPIRUN is zero, the ULPIDATRD will be valid if the operation was a read.

The polling method above could also be replaced and interrupt driven using the ULPI interrupt defined in the USBSTS and USBINTR registers. When a wakeup or read/write operation complete, the ULPI interrupt will be set.

Table 384. USB ULPI viewport register (ULPIVIEWPORT - address 0x4000 7170) bit description

Bit	Symbol	Value	Description	Access	Reset value
7:0	ULPIDATWR		When a write operation is commanded, the data to be sent is written to this field.	R/W	0
15:8	ULPIDATRD		After a read operation completes, the result is placed in this field.	R	0
23:16	ULPIADDR		When a read or write operation is commanded, the address of the operation is written to this field.	R/W	0
26:24	ULPIPORT		For the wakeup or read/write operation to be executed, this value must be written as 0.	R/W	000
27	ULPISS		ULPI sync state. This bit represents the state of the ULPI interface.	R	0
		0	In another state (ie. carkit, serial, low power)		
		1	Normal Sync. State.		
28	-	-	Reserved	-	-

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Table 384. USB ULPI viewport register (ULPIVIEWPORT - address 0x4000 7170) bit description *…continued*

Bit	Symbol	Value	Description	Access	Reset value
29	ULPIRW		ULPI Read/Write control. This bit selects between running a read or write operation.	R/W	0
		0	Read		
		1	Write		
30	ULPIRUN		ULPI Read/Write Run. Writing the 1 to this bit will begin the read/write operation. The bit will automatically transition to 0 after the read/write is complete. Once this bit is set, the driver can not set it back to 0. **Remark:** The driver must never executue a wakeup and a read/write operation at the same time.	R/W	-
31	ULPIWU		ULPI Wake-up. Writing the 1 to this bit will begin the wakeup operation. The bit will automatically transition to 0 after the wakeup is complete. Once this bit is set, the driver can not set it back to 0. **Remark:** The driver must never executue a wakeup and a read/write operation at the same time.	R/W	0

21.6.12 BINTERVAL register

This register defines the bInterval value which determines the length of the virtual frame (see Section 20.7.7).

Table 385. USB BINTERVAL register (BINTERVAL - address 0x4000 7174) bit description in device/host mode

Bit	Symbol	Description	Reset value	Access
3:0	BINT	bInterval value	0x00	R/W
31:4	-	Reserved	-	-

21.6.13 USB Endpoint NAK register (ENDPTNAK)

21.6.13.1 Device mode

This register indicates when the device sends a NAK handshake on an endpoint. Each Tx and Rx endpoint has a bit in the EPTN and EPRN field respectively.

A bit in this register is cleared by writing a 1 to it.

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Table 386. USB endpoint NAK register in device mode (ENDPTNAK - address 0x4000 7178) bit description

Bit	Symbol	Description	Reset value	Access
3:0	EPRN	Rx endpoint NAK Each RX endpoint has one bit in this field. The bit is set when the device sends a NAK handshake on a received OUT or PING token for the corresponding endpoint. Bit 3 corresponds to endpoint 3. ... Bit 1 corresponds to endpoint 1. Bit 0 corresponds to endpoint 0.	0x00	R/WC
15:6	-	Reserved	-	-
19:16	EPTN	Tx endpoint NAK Each TX endpoint has one bit in this field. The bit is set when the device sends a NAK handshake on a received IN token for the corresponding endpoint. Bit 3 corresponds to endpoint 3. ... Bit 1 corresponds to endpoint 1. Bit 0 corresponds to endpoint 0.	0x00	R/WC
31:20	-	Reserved	-	-

21.6.13.2 Host mode

This register is not used in host mode.

21.6.14 USB Endpoint NAK Enable register (ENDPTNAKEN)

21.6.14.1 Device mode

Each bit in this register enables the corresponding bit in the ENDPTNAK register. Each Tx and Rx endpoint has a bit in the EPTNE and EPRNE field respectively.

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Table 387. USB Endpoint NAK Enable register in device mode (ENDPTNAKEN - address 0x4000 717C) bit description

Bit	Symbol	Description	Reset value	Access
3:0	EPRNE	Rx endpoint NAK enable Each bit enables the corresponding RX NAK bit. If this bit is set and the corresponding RX endpoint NAK bit is set, the NAK interrupt bit is set. Bit 3 corresponds to endpoint 3. ... Bit 1 corresponds to endpoint 1. Bit 0 corresponds to endpoint 0.	0x00	R/W
15:4	-	Reserved	-	-
19:16	EPTNE	Tx endpoint NAK Each bit enables the corresponding TX NAK bit. If this bit is set and the corresponding TX endpoint NAK bit is set, the NAK interrupt bit is set. Bit 3 corresponds to endpoint 3. ... Bit 1 corresponds to endpoint 1. Bit 0 corresponds to endpoint 0.	0x00	R/W
31:20	-	Reserved	-	-

21.6.14.2 Host mode

This register is not used in host mode.

21.6.15 Port Status and Control register (PORTSC1)

21.6.15.1 Device mode

The device controller implements one port register, and it does not support power control. Port control in device mode is used for status port reset, suspend, and current connect status. It is also used to initiate test mode or force signaling. This register allows software to put the PHY into low-power Suspend mode and disable the PHY clock.

Table 388. Port Status and Control register in device mode (PORTSC1_D - address 0x4000 7184) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	CCS		Current connect status	0	RO
		0	Device not attached A zero indicates that the device did not attach successfully or was forcibly disconnected by the software writing a zero to the Run bit in the USBCMD register. It does not state the device being disconnected or suspended.		
		1	Device attached. A one indicates that the device successfully attached and is operating in either high-speed mode or full-speed mode as indicated by the High Speed Port bit in this register.		
1	CSC	-	Not used in device mode	0	-
2	PE	1	Port enable. This bit is always 1. The device port is always enabled.	1	RO

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Table 388. Port Status and Control register in device mode (PORTSC1_D - address 0x4000 7184) bit description

Bit	Symbol	Value	Description	Reset value	Access
3	PEC	0	Port enable/disable change This bit is always 0. The device port is always enabled.	0	RO
5:4	-	-	Reserved	0	RO
6	FPR		Force port resume After the device has been in Suspend State for 5 ms or more, software must set this bit to one to drive resume signaling before clearing. The Device Controller will set this bit to one if a J-to-K transition is detected while the port is in the Suspend state. The bit will be cleared when the device returns to normal operation. When this bit transitions to a one because a J-to-K transition detected, the Port Change Detect bit in the USBSTS register is set to one as well.	0	R/W
		0	No resume (K-state) detected/driven on port.		
		1	Resume detected/driven on port.		
7	SUSP		Suspend In device mode, this is a read-only status bit .	0	RO
		0	Port not in suspend state		
		1	Port in suspend state		
8	PR		Port reset In device mode, this is a read-only status bit. A device reset from the USB bus is also indicated in the USBSTS register.	0	RO
		0	Port is not in the reset state.		
		1	Port is in the reset state.		
9	HSP		High-speed status **Remark:** This bit is redundant with bits 27:26 (PSPD) in this register. It is implemented for compatibility reasons.	0	RO
		0	Host/device connected to the port is not in High-speed mode.		
		1	Host/device connected to the port is in High-speed mode.		
11:10	LS	-	Not used in device mode.		
12	PP	-	Not used in device mode.		
13	-	-	Reserved	-	-
15:14	PIC1_0		Port indicator control Writing to this field effects the value of the USB1_IND1:0 pins.	00	R/W
		0x0	Port indicators are off.		
		0x1	amber		
		0x2	green		
		0x3	undefined		

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Table 388. Port Status and Control register in device mode (PORTSC1_D - address 0x4000 7184) bit description

Bit	Symbol	Value	Description	Reset value	Access
19:16	PTC3_0		Port test control Any value other than 0000 indicates that the port is operating in test mode. The FORCE_ENABLE_FS and FORCE ENABLE_LS are extensions to the test mode support specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_HS/FS/LS values will force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. Values 0x7 to 0xF are reserved.	0000	R/W
		0x0	TEST_MODE_DISABLE		
		0x1	J_STATE		
		0x2	K_STATE		
		0x3	SE0 (host)/NAK (device)		
		0x4	Packet		
		0x5	FORCE_ENABLE_HS		
		0x6	FORCE_ENABLE_FS		
20	-	-	Not used in device mode. This bit is always 0 in device mode.	0	-
21	-	-	Not used in device mode. This bit is always 0 in device mode.	0	-
22	-		Not used in device mode. This bit is always 0 in device mode.	0	-
23	PHCD		PHY low power suspend - clock disable (PLPSCD) In device mode, The PHY can be put into Low Power Suspend – Clock Disable when the device is not running (USBCMD Run/Stop = 0) or the host has signaled suspend (PORTSC SUSPEND = 1). Low power suspend will be cleared automatically when the host has signaled resume. Before forcing a resume from the device, the device controller driver must clear this bit.	0	R/W
		0	Writing a 0 enables the PHY clock. Reading a 0 indicates the status of the PHY clock (enabled).		
		1	Writing a 1 disables the PHY clock. Reading a 1 indicates the status of the PHY clock (disabled).		
24	PFSC		Port force full speed connect	0	R/W
		0	Port connects at any speed.		
		1	Writing this bit to a 1 will force the port to only connect at full speed. It disables the chirp sequence that allows the port to identify itself as High-speed. This is useful for testing FS configurations with a HS host, hub or device.		
25	-	-	Reserved		
27:26	PSPD		Port speed This register field indicates the speed at which the port is operating.	0	RO
		0x1	Full-speed		
		0x2	invalid in device mode		
		0x3	High-speed		
29:28	-	-	Reserved	-	-
31:30	PTS		Parallel transceiver select. All other values are reserved.	<tbd>	R/W
		0x2	ULPI		
		0x3	Serial/ 1.1 PHY (Full-speed only)		

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21.6.15.2 Host mode

The host controller uses one port. The register is only reset when power is initially applied or in response to a controller reset. The initial conditions of the port are:

- No device connected
- Port disabled

If the port has power control, this state remains until software applies power to the port by setting port power to one in the PORTSC register.

Table 389. Port Status and Control register in host mode (PORTSC1_H - address 0x4000 7184) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	CCS		Current connect status This value reflects the current state of the port and may not correspond directly to the event that caused the CSC bit to be set. This bit is 0 if PP (Port Power bit) is 0. Software clears this bit by writing a 1 to it.	0	R/WC
		0	No device is present.		
		1	Device is present on the port.		
1	CSC		Connect status change Indicates a change has occurred in the port's Current Connect Status. The host/device controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software clears this bit by writing a one to it. This bit is 0 if PP (Port Power bit) is 0	0	R/WC
		0	No change in current status.		
		1	Change in current status.		
2	PE		Port enable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by the host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled. downstream propagation of data is blocked except for reset. This bit is 0 if PP (Port Power bit) is 0.	0	R/W
		0	Port disabled.		
		1	Port enabled.		

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Table 389. Port Status and Control register in host mode (PORTSC1_H - address 0x4000 7184) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
3	PEC	0	Port disable/enable change For the root hub, this bit gets set to a one only when a port is disabled due to disconnect on the port or due to the appropriate conditions existing at the EOF2 point (See *Chapter 11 of the USB Specification*). Software clears this by writing a one to it. This bit is 0 if PP (Port Power bit) is 0,	0	R/WC
		0	No change.		
		1	Port enabled/disabled status has changed.		
4	OCA		Over-current active This bit will automatically transition from 1 to 0 when the over-current condition is removed.	0	RO
		0	The port does not have an over-current condition.		
		1	The port has currently an over-current condition.		
5	OCC		Over-current change This bit gets set to one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.	0	R/WC
6	FPR		Force port resume Software sets this bit to one to drive resume signaling. The Host Controller sets this bit to one if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to one. This bit will automatically change to zero after the resume sequence is complete. This behavior is different from EHCI where the host controller driver is required to set this bit to a zero after the resume duration is timed in the driver. Note that when the Host controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed ‘K’) is driven on the port as long as this bit remains a one. This bit will remain a one until the port has switched to the high-speed idle. Writing a zero has no affect because the port controller will time the resume operation clear the bit the port control state switches to HS or FS idle. This bit is 0 if PP (Port Power bit) is 0.	0	R/W
		0	No resume (K-state) detected/driven on port.		
		1	Resume detected/driven on port.		

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Table 389. Port Status and Control register in host mode (PORTSC1_H - address 0x4000 7184) bit description
…continued

Bit	Symbol	Value	Description	Reset value	Access
7	SUSP		Suspend Together with the PE (Port enabled bit), this bit describes the port states, see Table 390 "Port states as described by the PE and SUSP bits in the PORTSC1 register". The host controller will unconditionally set this bit to zero when software sets the Force Port Resume bit to zero. The host controller ignores a write of zero to this bit. If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined. This bit is 0 if PP (Port Power bit) is 0.	0	R/W
		0	Port not in suspend state		
		1	Port in suspend state When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB.		
8	PR		Port reset When software writes a one to this bit the bus-reset sequence as defined in the USB Specification Revision 2.0 is started. This bit will automatically change to zero after the reset sequence is complete. This behavior is different from EHCI where the host controller driver is required to set this bit to a zero after the reset duration is timed in the driver. This bit is 0 if PP (Port Power bit) is 0.	0	R/W
		0	Port is not in the reset state.		
		1	Port is in the reset state.		
9	HSP		High-speed status	0	RO
		0	Host/device connected to the port is not in High-speed mode.		
		1	Host/device connected to the port is in High-speed mode.		
11:10	LS		Line status These bits reflect the current logical levels of the USB_DP and USB_DM signal lines. USB_DP corresponds to bit 11 and USB_DM to bit 10. In host mode, the use of linestate by the host controller driver is not necessary for this controller (unlike EHCI) because the controller hardware manages the connection of LS and FS.	0x3	RO
		0x0	SE0 (USB_DP and USB_DM LOW)		
		0x1	J-state (USB_DP HIGH and USB_DM LOW)		
		0x2	K-state (USB_DP LOW and USB_DM HIGH)		
		0x3	Undefined		

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Table 389. Port Status and Control register in host mode (PORTSC1_H - address 0x4000 7184) bit description
…continued

Bit	Symbol	Value	Description	Reset value	Access
12	PP	-	Port power control Host controller requires port power control switches. This bit represents the current setting of the switch (0=off, 1=on). When power is not available on a port (i.e. PP equals a 0), the port is non-functional and will not report attaches, detaches, etc. When an over-current condition is detected on a powered port and PPC is a one, the PP bit in each affected port may be transitioned by the host controller driver from a one to a zero (removing power from the port).	0	R/W
		0	Port power off.		
		1	Port power on.		
13	-	-	Reserved	0	-
15:14	PIC1_0		Port indicator control Writing to this field controls the value of the pins USB1_IND1 and USB1_IND0.	00	R/W
		0x0	Port indicators are off.		
		0x1	Amber		
		0x2	Green		
		0x3	Undefined		
19:16	PTC3_0		Port test control Any value other than 0000 indicates that the port is operating in test mode. The FORCE_ENABLE_FS and FORCE ENABLE_LS are extensions to the test mode support specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values will force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. Values 0x8 to 0xF are reserved.	0000	R/W
		0x0	TEST_MODE_DISABLE		
		0x1	J_STATE		
		0x2	K_STATE		
		0x3	SE0 (host)/NAK (device)		
		0x4	Packet		
		0x5	FORCE_ENABLE_HS		
		0x6	FORCE_ENABLE_FS		
		0x7	FORCE_ENABLE_LS		
20	WKCN		Wake on connect enable (WKCNNT_E) This bit is 0 if PP (Port Power bit) is 0	0	R/W
		0	Disables the port to wake up on device connects.		
		1	Writing this bit to a one enables the port to be sensitive to device connects as wake-up events.		

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Table 389. Port Status and Control register in host mode (PORTSC1_H - address 0x4000 7184) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
21	WKDC		Wake on disconnect enable (WKDSCNNT_E) This bit is 0 if PP (Port Power bit) is 0.	0	R/W
		0	Disables the port to wake up on device disconnects.		
		1	Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events.		
22	WKOC		Wake on over-current enable (WKOC_E)	0	R/W
		0	Disables the port to wake up on over-current events.		
		1	Writing a one to this bit enabled the port to be sensitive to over-current conditions as wake-up events.		
23	PHCD		PHY low power suspend - clock disable (PLPSCD) In host mode, the PHY can be put into Low Power Suspend – Clock Disable when the downstream device has been put into suspend mode or when no downstream device is connected. Low power suspend is completely under the control of software.	0	R/W
		0	Writing a 0 enables the PHY clock. Reading a 0 indicates the status of the PHY clock (enabled).		
		1	Writing a 1 disables the PHY clock. Reading a 1 indicates the status of the PHY clock (disabled).		
24	PFSC		Port force full speed connect	0	R/W
		0	Port connects at any speed.		
		1	Writing this bit to a 1 will force the port to only connect at Full Speed. It disables the chirp sequence that allows the port to identify itself as High Speed. This is useful for testing FS configurations with a HS host, hub or device.		
25	-	-	Reserved		
27:26	PSPD		Port speed This register field indicates the speed at which the port is operating. For HS mode operation in the host controller and HS/FS operation in the device controller the port routing steers data to the Protocol engine. For FS and LS mode operation in the host controller, the port routing steers data to the Protocol Engine w/ Embedded Transaction Translator.	0	RO
		0x0	Full-speed		
		0x1	Low-speed		
		0x2	High-speed		
29:28	-	-	Reserved	-	-
31:30	PTS		Parallel transceiver select. All other values are reserved.	<tbd>	R/W
		0x2	ULPI		
		0x3	Serial/ 1.1 PHY (Full-speed only)		

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Table 390. Port states as described by the PE and SUSP bits in the PORTSC1 register

PE bit	SUSP bit	Port state
0	0 or 1	disabled
1	0	enabled
1	1	suspend

21.6.16 USB Mode register (USBMODE)

The USBMODE register sets the USB mode for the USB controller. The possible modes are Device, Host, and Idle mode.

21.6.16.1 Device mode

Table 391. USB Mode register in device mode (USBMODE_D - address 0x4000 71A8) bit description

Bit	Symbol	Value	Description	Reset value	Access
1:0	CM1_0		Controller mode The controller defaults to an idle state and needs to be initialized to the desired operating mode after reset. This register can only be written once after reset. If it is necessary to switch modes, software must reset the controller by writing to the RESET bit in the USBCMD register before reprogramming this register.	00	R/ WO
		0x0	Idle		
		0x1	Reserved		
		0x2	Device controller		
		0x3	Host controller		
2	ES		Endian select This bit can change the byte ordering of the transfer buffers to match the host microprocessor bus architecture. The bit fields in the microprocessor interface and the DMA data structures (including the setup buffer within the device QH) are unaffected by the value of this bit, because they are based upon 32-bit words.	0	R/W
		0	Little endian: first byte referenced in least significant byte of 32-bit word.		
		1	Big endian: first byte referenced in most significant byte of 32-bit word.		
3	SLOM		Setup Lockout mode In device mode, this bit controls behavior of the setup lock mechanism. See Section 20.10.8.	0	R/W
		0	Setup Lockouts on		
		1	Setup Lockouts Off (DCD requires the use of Setup Buffer Tripwire in USBCMD)		

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Table 391. USB Mode register in device mode (USBMODE_D - address 0x4000 71A8) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
4	SDIS		Stream disable mode **Remark:** The use of this feature substantially limits the overall USB performance that can be achieved.	0	R/W
		0	Not disabled		
		1	Disabled. Setting this bit to one disables double priming on both RX and TX for low bandwidth systems. This mode ensures that when the RX and TX buffers are sufficient to contain an entire packet that the standard double buffering scheme is disabled to prevent overruns/underruns in bandwidth limited systems. Note: In High Speed Mode, all packets received will be responded to with a NYET handshake when stream disable is active.		
5	-		Not used in device mode.	0	-
31:6	-	-	Reserved		

21.6.16.2 Host mode

Table 392. USB Mode register in host mode (USBMODE_H - address 0x4000 71A8) bit description

Bit	Symbol	Value	Description	Reset value	Access
1:0	CM1_0		Controller mode The controller defaults to an idle state and needs to be initialized to the desired operating mode after reset. This register can only be written once after reset. If it is necessary to switch modes, software must reset the controller by writing to the RESET bit in the USBCMD register before reprogramming this register.	00	R/ WO
		0x0	Idle		
		0x1	Reserved		
		0x2	Device controller		
		0x3	Host controller		
2	ES		Endian select This bit can change the byte ordering of the transfer buffers. The bit fields in the microprocessor interface and the DMA data structures (including the setup buffer within the device QH) are unaffected by the value of this bit, because they are based upon 32-bit words.	0	R/W
		0	Little endian: first byte referenced in least significant byte of 32-bit word.		
		1	Big endian: first byte referenced in most significant byte of 32-bit word.		
3	-		Not used in host mode	0	-

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Table 392. USB Mode register in host mode (USBMODE_H - address 0x4000 71A8) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
4	SDIS		Stream disable mode **Remark:** The use of this feature substantially limits the overall USB performance that can be achieved.	0	R/W
		0	Not disabled		
		1	Disabled. Setting to a 1 ensures that overruns/underruns of the latency FIFO are eliminated for low bandwidth systems where the RX and TX buffers are sufficient to contain the entire packet. Enabling stream disable also has the effect of ensuring the the TX latency is filled to capacity before the packet is launched onto the USB. Note: Time duration to pre-fill the FIFO becomes significant when stream disable is active. See TXFILLTUNING to characterize the adjustments needed for the scheduler when using this feature.		
5	VBPS		VBUS power select	0	R/WO
		0	vbus_pwr_select is set LOW.		
		1	vbus_pwr_select is set HIGH		
31:6	-	-	Reserved	-	-

21.6.17 USB Endpoint Setup Status register (ENDPSETUPSTAT)

Table 393. USB Endpoint Setup Status register (ENDPTSETUPSTAT - address 0x4000 71AC) bit description

Bit	Symbol	Description	Reset value	Access
3:0	ENDPT SETUP STAT	Setup endpoint status for logical endpoints. For every setup transaction that is received, a corresponding bit in this register is set to one. Software must clear or acknowledge the setup transfer by writing a one to a respective bit after it has read the setup data from Queue head. The response to a setup packet as in the order of operations and total response time is crucial to limit bus time outs while the setup lockout mechanism is engaged.	0	R/WC
31:4	-	Reserved	-	-

21.6.18 USB Endpoint Prime register (ENDPTPRIME)

For each endpoint, software should write a one to the corresponding bit whenever posting a new transfer descriptor to an endpoint. Hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a receive buffer. Hardware will clear this bit when the associated endpoint(s) is (are) successfully primed.

Remark: These bits will be momentarily set by hardware during hardware endpoint re-priming operations when a dTD is retired and the dQH is updated.

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Table 394. USB Endpoint Prime register (ENDPTPRIME - address 0x4000 71B0) bit description

Bit	Symbol	Description	Reset value	Access
3:0	PERB	Prime endpoint receive buffer for physical OUT endpoints. For each OUT endpoint, a corresponding bit is set to 1 by software to request a buffer be prepared for a receive operation for when a USB host initiates a USB OUT transaction. Software should write a one to the corresponding bit whenever posting a new transfer descriptor to an endpoint. Hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a receive buffer. Hardware will clear this bit when the associated endpoint(s) is (are) successfully primed. PERB0 = endpoint 0 ... PERB3 = endpoint 3	0	R/WS
15:4	-	Reserved	-	-
19:16	PETB	Prime endpoint transmit buffer for physical IN endpoints. For each IN endpoint a corresponding bit is set to one by software to request a buffer be prepared for a transmit operation in order to respond to a USB IN/INTERRUPT transaction. Software should write a one to the corresponding bit when posting a new transfer descriptor to an endpoint. Hardware will automatically use this bit to begin parsing for a new transfer descriptor from the queue head and prepare a transmit buffer. Hardware will clear this bit when the associated endpoint(s) is (are) successfully primed. PETB0 = endpoint 0 ... PETB3 = endpoint 3	0	R/WS
31:20	-	Reserved	-	-

21.6.19 USB Endpoint Flush register (ENDPTFLUSH)

Writing a one to a bit(s) in this register will cause the associated endpoint(s) to clear any primed buffers. If a packet is in progress for one of the associated endpoints, then that transfer will continue until completion. Hardware will clear this register after the endpoint flush operation is successful.

Table 395. USB Endpoint Flush register (ENDPTFLUSH - address 0x4000 71B4) bit description

Bit	Symbol	Description	Reset value	Access
3:0	FERB	Flush endpoint receive buffer for physical OUT endpoints. Writing a one to a bit(s) will clear any primed buffers. FERB0 = endpoint 0 ... FERB3 = endpoint 3	0	R/WS

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Table 395. USB Endpoint Flush register (ENDPTFLUSH - address 0x4000 71B4) bit description

Bit	Symbol	Description	Reset value	Access
15:4	-	Reserved	-	-
19:16	FETB	Flush endpoint transmit buffer for physical IN endpoints. Writing a one to a bit(s) will clear any primed buffers. FETB0 = endpoint 0 ... FETB3 = endpoint 3	0	R/WS
31:20	-	Reserved	-	-

21.6.20 USB Endpoint Status register (ENDPTSTAT)

One bit for each endpoint indicates status of the respective endpoint buffer. This bit is set by hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. There will always be a delay between setting a bit in the ENDPTPRIME register and endpoint indicating ready. This delay time varies based upon the current USB traffic and the number of bits set in the ENDPTPRIME register. Buffer ready is cleared by USB reset, by the USB DMA system, or through the ENDPTFLUSH register.

Remark: These bits will be momentarily cleared by hardware during hardware endpoint re-priming operations when a dTD is retired and the dQH is updated.

Table 396. USB Endpoint Status register (ENDPTSTAT - address 0x4000 71B8) bit description

Bit	Symbol	Description	Reset value	Access
3:0	ERBR	Endpoint receive buffer ready for physical OUT endpoints. This bit is set to 1 by hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. ERBR0 = endpoint 0 ... ERBR3 = endpoint 3	0	RO
15:4	-	Reserved	-	-
19:16	ETBR	Endpoint transmit buffer ready for physical IN endpoints 3 to 0. This bit is set to 1 by hardware as a response to receiving a command from a corresponding bit in the ENDPTPRIME register. ETBR0 = endpoint 0 ... ETBR3 = endpoint 3	0	RO
31:20	-	Reserved	-	-

21.6.21 USB Endpoint Complete register (ENDPTCOMPLETE)

Each bit in this register indicates that a received/transmit event occurred and software should read the corresponding endpoint queue to determine the transfer status. If the corresponding IOC bit is set in the Transfer Descriptor, then this bit will be set simultaneously with the USBINT.

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Writing a one will clear the corresponding bit in this register.

Table 397. USB Endpoint Complete register (ENDPTCOMPLETE - address 0x4000 71BC) bit description

Bit	Symbol	Description	Reset value	Access
3:0	ERCE	Endpoint receive complete event for physical OUT endpoints. This bit is set to 1 by hardware when receive event (OUT/SETUP) occurred. ERCE0 = endpoint 0 ... ERCE3 = endpoint 3	0	R/WC
15:4	-	Reserved	-	-
19:16	ETCE	Endpoint transmit complete event for physical IN endpoints. This bit is set to 1 by hardware when a transmit event (IN/INTERRUPT) occurred. ETCE0 = endpoint 0 ... ETCE3 = endpoint 3	0	R/WC
31:20	-	Reserved	-	-

21.6.22 USB Endpoint 0 Control register (ENDPTCTRL0)

This register initializes endpoint 0 for control transfer. Endpoint 0 is always a control endpoint.

Table 398. USB Endpoint 0 Control register (ENDPTCTRL0 - address 0x4000 71C0) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	RXS		Rx endpoint stall	0	R/W
		0	Endpoint ok.		
		1	Endpoint stalled Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It will continue returning STALL until the bit is cleared by software, or it will automatically be cleared upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared by hardware until the associated ENDSETUPSTAT bit is cleared.[1]		
1	-	-	Reserved		
3:2	RXT	0x0	Endpoint type Endpoint 0 is always a control endpoint.	0	R/W
6:4	-	-	Reserved	-	-
7	RXE	1	Rx endpoint enable Endpoint enabled. Control endpoint 0 is always enabled. This bit is always 1.	1	RO
15:8	-	-	Reserved	-	-

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Table 398. USB Endpoint 0 Control register (ENDPTCTRL0 - address 0x4000 71C0) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
16	TXS		Tx endpoint stall		R/W
		0	Endpoint ok.		
		1	Endpoint stalled Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It will continue returning STALL until the bit is cleared by software, or it will automatically be cleared upon receipt of a new SETUP request. After receiving a SETUP request, this bit will continue to be cleared by hardware until the associated ENDSETUPSTAT bit is cleared.[1]		
17	-	-	Reserved		
19:18	TXT	0x0	Endpoint type Endpoint 0 is always a control endpoint.	0	RO
22:20	-	-	Reserved		
23	TXE	1	Tx endpoint enable Endpoint enabled. Control endpoint 0 is always enabled. This bit is always 1.	1	RO
31:24	-	-	Reserved		

[1] There is a slight delay (50 clocks max) between the ENPTSETUPSTAT being cleared and hardware continuing to clear this bit. In most systems it is unlikely that the DCD software will observe this delay. However, should the DCD notice that the stall bit is not set after writing a one to it, software should continually write this stall bit until it is set or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.

21.6.23 Endpoint 1 to 3 control registers

Each endpoint that is not a control endpoint has its own register to set the endpoint type and enable or disable the endpoint.

Remark: The reset value for all endpoint types is the control endpoint. If one endpoint direction is enabled and the paired endpoint of opposite direction is disabled, then the endpoint type of the unused direction must be changed from the control type to any other type (e.g. bulk). Leaving an unconfigured endpoint control will cause undefined behavior for the data PID tracking on the active endpoint.

Table 399. USB Endpoint 1 to 3 control registers (ENDPTCTRL - address 0x4000 71C4 (ENDPTCTRL1) to 0x4000 71CC (ENDPTCTRL3)) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	RXS		Rx endpoint stall	0	R/W
		0	Endpoint ok. This bit will be cleared automatically upon receipt of a SETUP request if this Endpoint is configured as a Control Endpoint and this bit will continue to be cleared by hardware until the associated ENDPTSETUPSTAT bit is cleared.		
		1	Endpoint stalled Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It will continue returning STALL until the bit is cleared by software, or it will automatically be cleared upon receipt of a new SETUP request.[1]		

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Table 399. USB Endpoint 1 to 3 control registers (ENDPTCTRL - address 0x4000 71C4 (ENDPTCTRL1) to 0x4000 71CC (ENDPTCTRL3)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
1	-		Reserved	0	R/W
3:2	RXT		Endpoint type	00	R/W
		0x0	Control		
		0x1	Isochronous		
		0x2	Bulk		
		0x3	Reserved		
4	-	-	Reserved		
5	RXI		Rx data toggle inhibit This bit is only used for test and should always be written as zero. Writing a one to this bit will cause this endpoint to ignore the data toggle sequence and always accept data packets regardless of their data PID.	0	R/W
		0	Disabled		
		1	Enabled		
6	RXR		Rx data toggle reset Write 1 to reset the PID sequence. Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PIDs between the host and device.	0	WS
7	RXE		Rx endpoint enable **Remark:** An endpoint should be enabled only after it has been configured.	0	R/W
		0	Endpoint disabled.		
		1	Endpoint enabled.		
15:8	-	-	Reserved		
16	TXS		Tx endpoint stall	0	R/W
		0	Endpoint ok. This bit will be cleared automatically upon receipt of a SETUP request if this Endpoint is configured as a Control Endpoint, and this bit will continue to be cleared by hardware until the associated ENDPTSETUPSTAT bit is cleared.		
		1	Endpoint stalled Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. It will continue returning STALL until the bit is cleared by software, or it will automatically be cleared upon receipt of a new SETUP request.[1]		
17	-	-	Reserved	0	-
19:18	TXT		Tx endpoint type	00	R/W
		0x0	Control		
		0x1	Isochronous		
		0x2	Bulk		
		0x3	Interrupt		
20	-	-	Reserved		

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Table 399. USB Endpoint 1 to 3 control registers (ENDPTCTRL - address 0x4000 71C4 (ENDPTCTRL1) to 0x4000 71CC (ENDPTCTRL3)) bit description …*continued*

Bit	Symbol	Value	Description	Reset value	Access
21	TXI		Tx data toggle inhibit This bit is only used for test and should always be written as zero. Writing a one to this bit will cause this endpoint to ignore the data toggle sequence and always accept data packets regardless of their data PID.	0	R/W
		0	Enabled		
		1	Disabled		
22	TXR		Tx data toggle reset Write 1 to reset the PID sequence. Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the host and device.	1	WS
23	TXE		Tx endpoint enable **Remark:** An endpoint should be enabled only after it has been configured	0	R/W
		0	Endpoint disabled.		
		1	Endpoint enabled.		
31:24	-	-	Reserved	0	

[1] For control endpoints only: There is a slight delay (50 clocks max) between the ENPTSETUPSTAT being cleared and hardware continuing to clear this bit. In most systems it is unlikely that the DCD software will observe this delay. However, should the DCD notice that the stall bit is not set after writing a one to it, software should continually write this stall bit until it is set or until a new setup has been received by checking the associated ENDPTSETUPSTAT bit.

21.7 Functional description

For details on the device data structures, see Section 20.9. For the device operational model, see Section 20.10.

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22.1 How to read this chapter

The Ethernet controller is available on parts LPC1850 and LPC1830.

22.2 Basic configuration

The Ethernet controller is configured as follows:

- See Table 400 for clocking and power control.
- The Ethernet is reset by the ETHERNET_RST (reset # 22).
- The Ethernet interrupt is connected to interrupt slot # 5 in the NVIC, and the is connected to slot # 8 in the event router.
- Set the Ethernet mode to RMII or MII in the CREG6 register in the CREG block (see Table 37).

Table 400. Ethernet clocking and power control

	Base clock	Branch clock	Maximum frequency	Notes
Ethernet register interface clock	BASE_M3_CLK	CLK_M3_ ETHERNET	150 MHz	-
Ethernet PHY clock	BASE_PHY_ RX_CLK	-	75 MHz	Select the clock pin ENET_RX_CLK as clock source for this base clock in the OUTCLK_7_CTRL register in the CGU.
Ethernet PHY clock	BASE_PHY_ TX_CLK	-	75 MHz	Select the clock pin ENET_TX_CLK as clock source for this base clock in the OUTCLK_8_CTRL register in the CGU.

22.3 Features

- 10/100 Mbit/s
- TCP/IP hardware checksum
- IP checksum
- DMA support
- IEEE 1588 time stamping block
- IEEE 1588 advanced time stamp support (IEEE 1588-2008 v2)
- Power management remote wake-up frame and magic packet detection
- Supports both full-duplex and half-duplex operation
  – Supports CSMA/CD Protocol for half-duplex operation.

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– Supports IEEE 802.3x flow control for full-duplex operation.
– Optional forwarding of received pause control frames to the user application in full-duplex operation.
– Back-pressure support for half-duplex operation.
– Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.

22.4 General description

22.5 Pin description

Table 401. Ethernet pin description

Function name	Direction	Description
MIIM interface		
ENET_MDIO	I/O	Ethernet MIIM Data Input and Iutput.
ENET_MDC	O	Ethernet MIIM Clock.
RMII interface (also used for MII interface)		
ENET_RXD[1:0]	I	Ethernet Receive Data.
ENET_TXD[1:0]	O	Ethernet Transmit Tata.
ENET_RX_DV	I	Ethernet Receive Data Valid.
ENET_REF_CLK	I	Ethernet Reference Clock.
ENET_TX_EN	O	Ethernet Transmit Data Enable.
MII interface		
ENET_RXD[3:2]	I	Ethernet Receive Data.
ENET_TXD[3:2]	O	Ethernet Transmit Tata.
ENET_COL	I	Ethernet Collision detect.
ENET_CRS	I	Ethernet Carrier Sense.
ENET_TX_ER	O	Ethernet Transmit Error.
ENET_TX_CLK	I	Ethernet Transmit Clock.
ENET_RX_CLK	I/O	Ethernet Receive Clock.
ENET_RX_DV	I	Ethernet Receive Data Valid.
ENET_RX_ER	I	Ethernet Receive Error.

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22.6 Register description

Table 402. Register overview: Ethernet MAC and DMA (base address 0x4001 0000)

Name	Access	Address offset	Description	Reset value
MAC_CONFIG		0x0000	MAC configuration register	0x0000 8000
MAC_FRAME_FILTER		0x0004	MAC frame filter	0x0000 0000
MAC_HASHTABLE_HIGH		0x0008	Hash table high register	0x0000 0000
MAC_HASHTABLE_LOW		0x000C	Hash table low register	0x0000 0000
MAC_MII_ADDR		0x0010	MII address register	0x0000 0000
MAC_MII_DATA		0x0014	MII data register	0x0000 0000
MAC_FLOW_CTRL		0x0018	Flow control register	0x0000 0000
MAC_VLAN_TAG		0x001C	VLAN tag register	0x0000 0000
MAC_VER		0x0020	Version register	0x0000 1036
MAC_DEBUG		0x0024	Debug register	0x0000 0000
MAC_RWAKE_FRFLT		0x0028	Remote wake-up frame filter	0x0000 0000
MAC_PMT_CTRL_STAT		0x002C	PMT control and status	0x0000 0000
-	-	0x0030 - 0x0034	Reserved	
MAC_INTR		0x0038	Interrupt status register	0x0000 0000
MAC_INTR_MASK		0x003C	Interrupt mask register	0x0000 0000
MAC_ADDR0_HIGH		0x0040	MAC address 0 high register	0x8000 FFFF
MAC_ADDR0_LOW		0x0044	MAC address 0 low register	0xFFFF FFFF
-	-	0x0048 - 0x06FC	Reserved	-
MAC_TIMESTP_CTRL		0x0700	Time stamp control register	0x0000 2000
-		0x0704 - 0x0FFC	Reserved	
DMA_BUS_MODE		0x1000	Bus Mode Register	0x0002 0100
DMA_TRANS_POLL_DEMAND		0x1004	Transmit poll demand register	0x0000 0000
DMA_REC_POLL_DEMAND		0x1008	Receive poll demand register	0x0000 0000
DMA_REC_DES_ADDR		0x100C	Receive descriptor list address register	0x0000 0000
DMA_TRANS_DES_ADDR		0x1010	Transmit descriptor list address register	0x0000 0000
DMA_STAT		0x1014	Status register	0x0000 0000
DMA_OP_MODE		0x1018	Operation mode register	0x0000 0000
DMA_INT_EN		0x101C	Interrupt enable register	0x0000 0000
DMA_MFRM_BUFOF		0x1020	Missed frame and buffer overflow register	0x0000 0000
DMA_REC_INT_WDT		0x1024	Receive interrupt watchdog timer register	0x0000 0000
-	-	0x1028 - 0x1044	Reserved	
DMA_CURHOST_TRANS_DES		0x1048	Current host transmit descriptor register	0x0000 0000
DMA_CURHOST_REC_DES		0x104C	Current host receive descriptor register	0x0000 0000

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Table 402. Register overview: Ethernet MAC and DMA (base address 0x4001 0000)

Name	Access	Address offset	Description	Reset value
DMA_CURHOST_TRANS_BUF		0x1050	Current host transmit buffer address register	0x0000 0000
DMA_CURHOST_REC_BUF		0x1054	Current host receive buffer address register	0x0000 0000
DMA_HW_FEATURE		0x1058	HW feature register	0x0105 2715

22.6.1 MAC Configuration register

The MAC Configuration register establishes receive and transmit operating modes.

Table 403. MAC Configuration register (MAC_CONFIG, address 0x4001 0000) bit description

Bit	Symbol	Description	Reset value	Access
1:0	-	Reserved	00	RO
2	RE	Receiver enable When this bit is set, the receiver state machine of the MAC is enabled for receiving frames from the MII. When this bit is reset, the MAC receive state machine is disabled after the completion of the reception of the current frame, and will not receive any further frames from the MII.	0	R/W
3	TE	Transmitter Enable When this bit is set, the transmit state machine of the MAC is enabled for transmission on the MII. When this bit is reset, the MAC transmit state machine is disabled after the completion of the transmission of the current frame, and will not transmit any further frames.	0	R/W
4	DF	Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC will issue a Frame Abort status, along with the excessive deferral error bit set in the transmit frame status when the transmit state machine is deferred for more than 24,288 bit times in 10/100-Mbps mode. If the Core is configured for 1000 Mbps operation, or if the Jumbo frame mode is enabled in 10/100-Mbps mode, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but is prevented because of an active CRS (carrier sense) signal on the MII. Defer time is not cumulative. If the transmitter defers for 10,000 bit times, then transmits, collides, backs off, and then has to defer again after completion of back-off, the deferral timer resets to 0 and restarts. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in Half-Duplex mode and is reserved (RO) in Full-Duplex-only configuration.	0	R/W

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Table 403. MAC Configuration register (MAC_CONFIG, address 0x4001 0000) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
6:5	BL	Back-Off Limit The Back-Off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000 Mbps and 512 bit times for 10/100 Mbps) the MAC waits before rescheduling a transmission attempt during retries after a collision. This bit is applicable only to Half-Duplex mode and is reserved (RO) in Full-Duplex-only configuration. • 00: k = min (n, 10) • 01: k = min (n, 8) • 10: k = min (n, 4) • 11: k = min (n, 1) where n = retransmission attempt. The random integer r takes the value in the range $0 \le r \le 2^k$.	0	R/W
7	ACS	Automatic Pad/CRC Stripping When this bit is set, the MAC strips the Pad/FCS field on incoming frames only if the length's field value is less than or equal to 1,500 bytes. All received frames with length field greater than or equal to 1,501 bytes are passed to the application without stripping the Pad/FCS field. When this bit is reset, the MAC will pass all incoming frames to the Host unmodified.	0	R/W
8	-	Link Up/Down Indicates whether the link is up or down during the transmission of configuration in SMII interface: 0 = Link down 1 = Link up	0	R/W
9	DR	Disable Retry When this bit is set, the MAC will attempt only 1 transmission. When a collision occurs on the MII, the MAC will ignore the current frame transmission and report a Frame Abort with excessive collision error in the transmit frame status. When this bit is reset, the MAC will attempt retries based on the settings of BL. This bit is applicable only to Half-Duplex mode and is reserved (RO with default value) in Full- Duplex-only configuration.	0	R/W
10	IPC	Checksum Offload When this bit is set, the MAC calculates the 16-bit one's complement of the one's complement sum of all received Ethernet frame payloads. It also checks whether the IPv4 Header checksum (assumed to be bytes 25–26 or 29–30 (VLAN-tagged) of the received Ethernet frame) is correct for the received frame and gives the status in the receive status word. The MAC core also appends the 16-bit checksum calculated for the IP header datagram payload (bytes after the IPv4 header) and appends it to the Ethernet frame transferred to the application (when Type 2 COE is deselected). When this bit is reset, this function is disabled. When Type 2 COE is selected, this bit, when set, enables IPv4 checksum checking for received frame payload's TCP/UDP/ICMP headers. When this bit is reset, the COE function in the receiver is disabled and the corresponding PCE and IP HCE status bits (see <tbd>) are always cleared.	0	R/W
11	DM	Duplex Mode When this bit is set, the MAC operates in a Full-Duplex mode where it can transmit and receive simultaneously.	0	R/W

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Table 403. MAC Configuration register (MAC_CONFIG, address 0x4001 0000) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
12	LM	Loopback Mode When this bit is set, the MAC operates in loopback mode at MII. The (G)MII Receive clock input is required for the loopback to work properly, as the Transmit clock is not looped-back internally.	0	R/W
13	DO	Disable Receive Own When this bit is set, the MAC disables the reception of frames in Half-Duplex mode. When this bit is reset, the MAC receives all packets that are given by the PHY while transmitting. This bit is not applicable if the MAC is operating in Full-Duplex mode.	0	R/W
14	FES	Speed Indicates the speed in Fast Ethernet (MII) mode: 0 = 10 Mbps 1 = 100 Mbps .	0	
15	PS	Port select 1 = MII (100 Mbp) - this is the only allowed value.	1	RO
16	DCRS	Disable carrier sense during transmission When set high, this bit makes the MAC transmitter ignore the (G)MII CRS signal during frame transmission in Half-Duplex mode. This request results in no errors generated due to Loss of Carrier or No Carrier during such transmission. When this bit is low, the MAC transmitter generates such errors due to Carrier Sense and will even abort the transmissions.	0	R/W
19:17	IFG	Inter-frame gap These bits control the minimum IFG between frames during transmission. 000 = 96 bit times 001 = 88 bit times 010 = 80 bit times ... 000 = 40 bit times Note that in Half-Duplex mode, the minimum IFG can be configured for 64 bit times (IFG = 100) only. Lower values are not considered	000	R//W
20	JE	Jumbo Frame Enable When this bit is set, MAC allows Jumbo frames of 9,018 bytes (9,022 bytes for VLAN tagged frames) without reporting a giant frame error in the receive frame status.	0	R/W
21	-	Reserved.	0	RO

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Table 403. MAC Configuration register (MAC_CONFIG, address 0x4001 0000) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
22	JD	Jabber Disable When this bit is set, the MAC disables the jabber timer on the transmitter, and can transfer frames of up to 16,384 bytes. When this bit is reset, the MAC cuts off the transmitter if the application sends out more than 2,048 bytes of data (10,240 if JE is set high) during transmission.	0	R/W
23	WD	Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver, and can receive frames of up to 16,384 bytes. When this bit is reset, the MAC allows no more than 2,048 bytes (10,240 if JE is set high) of the frame being received and cuts off any bytes received after that.	0	R/W
31:24	-	Reserved.	0x00	RO

22.6.2 MAC Frame filter register

The MAC Frame Filter register contains the filter controls for receiving frames. Some of the controls from this register go to the address check block of the MAC, which performs the first level of address filtering. The second level of filtering is performed on the incoming frame, based on other controls such as Pass Bad Frames and Pass Control Frames.

Table 404. MAC Frame filter register (MAC_FRAME_FILTER, address 0x4001 0004) bit description

Bit	Symbol	Description	Reset value	Access
0	PR	Promiscuous Mode When this bit is set, the Address Filter module passes all incoming frames regardless of its destination or source address. The SA/DA Filter Fails status bits of the Receive Status Word will always be cleared when PR is set.	0	R/W
1	-	reserved	0	RO
2	-	reserved	0	RO
3	DAIF	DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast frames. When reset, normal filtering of frames is performed.	0	R/W
4	PM	Pass All Multicast When set, this bit indicates that all received frames with a multicast destination address (first bit in the destination address field is '1') are passed. When reset, filtering of multicast frame depends on HMC bit.	0	R/W
5	DBF	Disable Broadcast Frames When this bit is set, the AFM module filters all incoming broadcast frames. When this bit is reset, the AFM module passes all received broadcast frames.	0	R/W

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Table 404. MAC Frame filter register (MAC_FRAME_FILTER, address 0x4001 0004) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
7:6	PCF	Pass Control Frames These bits control the forwarding of all control frames (including unicast and multicast PAUSE frames). Note that the processing of PAUSE control frames depends only on RFE of Flow Control Register[2]. 00 = MAC filters all control frames from reaching the application. 01 = MAC forwards all control frames except PAUSE control frames to application even if they fail the Address filter. 10 = MAC forwards all control frames to application even if they fail the Address Filter. 11 = MAC forwards control frames that pass the Address Filter.	00	R/W
8	SAIF	SA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the SA address comparison. The frames whose SA matches the SA registers will be marked as failing the SA Address filter. When this bit is reset, frames whose SA does not match the SA registers will be marked as failing the SA Address filter.	0	R/W
9	SAF	Source Address Filter Enable The MAC core compares the SA field of the received frames with the values programmed in the enabled SA registers. If the comparison matches, then the SAMatch bit of RxStatus Word is set high. When this bit is set high and the SA filter fails, the MAC drops the frame. When this bit is reset, then the MAC Core forwards the received frame to the application and with the updated SA Match bit of the RxStatus depending on the SA address comparison.	0	R/W
30:10	-	Reserved	0	RO
31	RA	Receive all When this bit is set, the MAC Receiver module passes to the Application all frames received irrespective of whether they pass the address filter. The result of the SA/DA filtering is updated (pass or fail) in the corresponding bits in the Receive Status Word. When this bit is reset, the Receiver module passes to the Application only those frames that pass the SA/DA address filter.	0	R/W

22.6.3 MAC Hash table high register

The 64-bit Hash table is used for group address filtering. For hash filtering, the contents of the destination address in the incoming frame is passed through the CRC logic, and the upper 6 bits of the CRC register are used to index the contents of the Hash table. The most significant bit determines the register to be used (Hash Table High/Hash Table Low), and the other 5 bits determine which bit within the register. A hash value of 00000 selects Bit 0 of the selected register, and a value of 11111 selects Bit 31 of the selected register.

For example, if the DA of the incoming frame is received as 0x1F52419CB6AF (0x1F is the first byte received on MII interface), then the internally calculated 6-bit Hash value is 0x2C and the HTH register bit[12] is checked for filtering. If the DA of the incoming frame is received as 0xA00A98000045, then the calculated 6- bit Hash value is 0x07 and the HTL register bit[7] is checked for filtering.

If the corresponding bit value of the register is 1, the frame is accepted. Otherwise, it is rejected. If the PM (Pass All Multicast) bit is set in the MAC_CONFIG register, then all multicast frames are accepted regardless of the multicast hash values.

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If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (in Little-Endian mode) or Bits[7:0] (in Big-Endian mode) of the Hash Table High/Low registers are written to. Please note that consecutive writes to these register should be performed only after at least 4 clock cycles in the destination clock domain when double synchronization is enabled.

The Hash Table High register contains the higher 32 bits of the Hash table.

Table 405. MAC Hash table high register (MAC_HASHTABLE_HIGH, address 0x4001 0008) bit description

Bit	Symbol	Description	Reset value	Access
31:0	HTH	Hash table high This field contains the upper 32 bits of Hash table.	0	R/W

22.6.4 MAC Hash table low register

The Hash Table Low register contains the lower 32 bits of the Hash table.

Table 406. MAC Hash table low register (MAC_HASHTABLE_LOW, address 0x4001 0008) bit description

Bit	Symbol	Description	Reset value	Access
31:0	HTL	Hash table low This field contains the upper 32 bits of Hash table.	0	R/W

22.6.5 MAC MII Address register

The MII Address register controls the management cycles to the external PHY through the management interface.

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Table 407. MAC MII Address register (MAC_MII_ADDR, address 0x4001 0010) bit description

Bit	Symbol	Description	Reset value	Access
0	GB	MII busy This bit should read a logic 0 before writing to this register and the MAC_MII_DATA register. This bit must also be set to 0 during a Write to this register. During a PHY register access, this bit will be set to 1 by the Application to indicate that a Read or Write access is in progress. The MAC_MII_DATA register should be kept valid until this bit is cleared by the MAC during a PHY Write operation. The MAC_MII_DATA register is invalid until this bit is cleared by the MAC during a PHY Read operation. This register should not be written to until this bit is cleared.	0	R_WS_SC
1	W	MII write When set, this bit tells the PHY that this will be a Write operation using the MII Data register. If this bit is not set, this will be a Read operation, placing the data in the MII Data register.	0	R/W
5:2	CR	CSR clock range The CSR Clock Range selection determines the frequency of the MDC clock . The suggested range of clk_csr_i frequency applicable for each value below (when Bit[5] = 0) ensures that the MDC clock is approximately between the frequency range 1.0 MHz - 2.5 MHz. When bit 5 is set, you can achieve MDC clock of frequency higher than the IEEE 802.3 specified frequency limit of 2.5 MHz and program a clock divider of lower value. For example, when clk_csr_i is of frequency 100 Mhz and you program these bits as 1010, then the resultant MDC clock will be of 12.5 Mhz which is outside the limit of IEEE 802.3 specified range. Please program the values given below only if the interfacing chips supports faster MDC clocks. See Table 408 for bit values.	0	R/W
10:6	GR	MII register These bits select the desired MII register in the selected PHY device.	0	R/W
15:11	PA	Physical layer address This field tells which of the 32 possible PHY devices are being accessed.	0	R/W
31:16	-	Reserved	0	RO

Table 408. CSR clock range values

Bits 5:2	clk_csr_i	MDC clock
0000	60 - 100 MHz	clk_csr_i/42
0001	100 - 150 MHz	clk_csr_i/62
0010	20 - 35 MHz	clk_csr_i/16
0011	35 - 60 MHz	clk_csr_i/26
0100	150 - 250 MHz	clk_csr_i/102
0101	250 - 300 MHz	clk_csr_i/124
0110, 0111	Reserved	-
1000	-	clk_csr_i/42
1001	-	clk_csr_i/62
1010	-	clk_csr_i/16
1011	-	clk_csr_i/26
1100	-	clk_csr_i/102

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Table 408. CSR clock range values

Bits 5:2	clk_csr_i	MDC clock
1101	-	clk_csr_i/124
1110	-	clk_csr_i/42
1111	-	clk_csr_i/62

22.6.6 MAC MII Data register

The MII Data register stores Write data to be written to the PHY register located at the address specified in the MAC_MII_ADDR register. This register also stores Read data from the PHY register located at the address specified by the MAC_MII_ADDR register.

Table 409. MII Data register (MAC_MII_DATA, address 0x4001 0014) bit description

Bit	Symbol	Description	Reset value	Access
15:0	GD	MII data This contains the 16-bit data value read from the PHY after a Management Read operation or the 16-bit data value to be written to the PHY before a Management Write operation.	0	R/W
31:16	-	Reserved	0	RO

22.6.7 MAC Flow control register

The Flow Control register controls the generation and reception of the Control (Pause Command) frames by the MAC’s Flow control module. A Write to a register with the Busy bit set to 1 triggers the Flow Control block to generate a Pause Control frame. The fields of the control frame are selected as specified in the 802.3x specification, and the Pause Time value from this register is used in the Pause Time field of the control frame. The Busy bit remains set until the control frame is transferred onto the cable. The Host must make sure that the Busy bit is cleared before writing to the register.

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Table 410. MAC Flow control register (MAC_FLOW_CTRL, address 0x4001 0018) bit description

Bit	Symbol	Description	Reset value	Access
0	FCB	Flow Control Busy/Backpressure Activate This bit initiates a Pause Control frame in Full-Duplex mode. In Full-Duplex mode, this bit should be read as 0 before writing to the Flow Control register. To initiate a Pause control frame, the Application must set this bit to 1. During a transfer of the Control Frame, this bit will continue to be set to signify that a frame transmission is in progress. After the completion of Pause control frame transmission, the MAC will reset this bit to 0. The Flow Control register should not be written to until this bit is cleared. In Half-Duplex mode, when this bit is set (and TFE is set), then backpressure is asserted by the MAC Core. During backpressure, when the MAC receives a new frame, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically OR'ed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured to Full- Duplex mode, the BPA is automatically disabled.	0	R/WS/ SC
1	TFE	Transmit Flow Control Enable In Full-Duplex mode, when this bit is set, the MAC enables the flow control operation to transmit Pause frames. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC will not transmit any Pause frames. In Half-Duplex mode, when this bit is set, the MAC enables the back-pressure operation. When this bit is reset, the backpressure feature is disabled.	0	R/W
2	RFE	Receive Flow Control Enable When this bit is set, the MAC will decode the received Pause frame and disable its transmitter for a specified (Pause Time) time. When this bit is reset, the decode function of the Pause frame is disabled.	0	R/W
3	UP	Unicast Pause Frame Detect When this bit is set, the MAC will detect the Pause frames with the station's unicast address specified in MAC Address0 High Register and MAC Address0 Low Register, in addition to the detecting Pause frames with the unique multicast address. When this bit is reset, the MAC will detect only a Pause frame with the unique multicast address specified in the 802.3x standard.	0	R/W
5:4	PLT	Pause Low Threshold This field configures the threshold of the PAUSE timer at which the input flow control is checked for automatic retransmission of PAUSE Frame. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = Ox100 (256 slot-times), and PLT = 01, then a second PAUSE frame is automatically transmitted if the flow control signal is asserted at 228 (256 – 28) slot-times after the first PAUSE frame is transmitted.	00	R/W
6	-	Reserved	0x000	RO
7	DZPQ	Disable Zero-Quanta Pause When set, this bit disables the automatic generation of Zero-Quanta Pause Control frames on the deassertion of the flow-control signal from the FIFO layer . When this bit is reset, normal operation with automatic Zero-Quanta Pause Control frame generation is enabled.	0	R/W
15:8	-	Reserved	0	RO
31:16	PT	Pause time This field holds the value to be used in the Pause Time field in the transmit control frame. If the Pause Time bits is configured to be double-synchronized to the (G)MII clock domain, then consecutive writes to this register should be performed only after at least 4 clock cycles in the destination clock domain.	0x000 0	R/W

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22.6.8 MAC VLAN tag register

The VLAN Tag register contains the IEEE 802.1Q VLAN Tag to identify the VLAN frames. The MAC compares the 13th and 14th bytes of the receiving frame (Length/Type) with 0x8100, and the following 2 bytes are compared with the VLAN tag; if a match occurs, it sets the received VLAN bit in the receive frame status. The legal length of the frame is increased from 1518 bytes to 1522 bytes.

If the VLAN Tag register is configured to be double-synchronized to the MII clock domain, then consecutive writes to these register should be performed only after at least 4 clock cycles in the destination clock domain.

Table 411. MAC VLAN tag register (MAC_VLAN_TAG, address 0x4001 01C) bit description

Bit	Symbol	Description	Reset value	Access
15:0	VL	VLAN Tag Identifier for Receive Frames This contains the 802.1Q VLAN tag to identify VLAN frames, and is compared to the fifteenth and sixteenth bytes of the frames being received for VLAN frames. Bits[15:13] are the User Priority, Bit[12] is the Canonical Format Indicator (CFI) and bits[11:0] are the VLAN tag's VLAN Identifier (VID) field. When the ETV bit is set, only the VID (Bits[11:0]) is used for comparison. If VL (VL[11:0] if ETV is set) is all zeros, the MAC does not check the fifteenth and sixteenth bytes for VLAN tag comparison, and declares all frames with a Type field value of 0x8100 to be VLAN frames.	0x000 0	R/W
16	ETV	Enable 12-Bit VLAN Tag Comparison When this bit is set, a 12-bit VLAN identifier, rather than the complete 16-bit VLAN tag, is used for comparison and filtering. Bits[11:0] of the VLAN tag are compared with the corresponding field in the received VLAN-tagged frame. When this bit is reset, all 16 bits of the received VLAN frame's fifteenth and sixteenth bytes are used for comparison.	0	R/W
31:17	-	Reserved	0x000 0	RO

22.6.9 MAC Debug register

This debug register gives the status of all the main modules of the transmit and receive data-paths and the FIFOs. An all-zero status indicates that the MAC core is in idle state (and FIFOs are empty) and no activity is going on in the data-paths.

Table 412. MAC Debug register (MAC_DEBUG, address 0x4001 0024) bit description

Bit	Symbol	Description	Reset value	Access
0	RXIDLESTAT	When high, it indicates that the MAC MII receive protocol engine is actively receiving data and not in IDLE state.		
2:1	FIFOSTAT0	When high, it indicates the active state of the small FIFO Read and Write controllers respectively of the MAC receive Frame Controller module.		
3	-	Reserved		
4	RXFIFOSTAT1	When high, it indicates that the MTL RxFIFO Write Controller is active and transferring a received frame to the FIFO.		

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Table 412. MAC Debug register (MAC_DEBUG, address 0x4001 0024) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
6:5	RXFIFOSTAT	State of the RxFIFO read Controller: 00 = idle state 01 = reading frame data 10 = reading frame status (or time stamp) 11 = flushing the frame data and status		
7	-	Reserved		
9:8	RXFIFOLVL	Status of the RxFIFO Fill-level 00 = RxFIFO Empty 01 = RxFIFO fill-level below flow-control de-activate threshold 10 = RxFIFO fill-level above flow-control activate threshold 11 = RxFIFO Full		
15:10	-	Reserved	-	RO
16	TXIDLESTAT	When high, it indicates that the MAC MII transmit protocol engine is actively transmitting data and not in IDLE state.		
18:17	TXSTAT	State of the MAC Transmit Frame Controller module: 00 = idle 01 = Waiting for Status of previous frame or IFG/backoff period to be over 10 = Generating and transmitting a PAUSE control frame (in full duplex mode) 11 = Transferring input frame for transmission		
19	PAUSE	When high, it indicates that the MAC transmitter is in PAUSE condition (in full-duplex only) and hence will not schedule any frame for transmission.		
21:20	TXFIFOSTAT	State of the TxFIFO read Controller 00 = idle state 01 = READ state (transferring data to MAC transmitter) 10 = Waiting for TxStatus from MAC transmitter 11 = Writing the received TxStatus or flushing the TxFIFO		
22	TXFIFOSTAT1	When high, it indicates that the MTL TxFIFO Write Controller is active and transferring data to the TxFIFO.		
23	-	Reserved		
24	TXFIFOLVL	When high, it indicates that the MTL TxFIFO is not empty and has some data left for transmission.		
25	TXFIFOFULL	When high, it indicates that the MTL TxStatus FIFO is full and hence the MTL will not be accepting any more frames for transmission.		
31:26				

22.6.10 MAC Remote wake-up frame filter register

This is the address through which the remote Wake-up Frame Filter registers (WKUPFMFILTER) are written/read by the Application. WKUPFMFILTER is actually a pointer to eight (not transparent) such WKUPFMFILTER registers. Eight sequential Writes to this address (0x028) will write all WKUPFMFILTER registers. Eight sequential Reads from this address (0x028) will read all WKUPFMFILTER registers. See Section 22.7.1.1 for details.

Remark: Do not use bit-banding for this register.

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Table 413. MAC Remote wake-up frame filter register (MAC_RWAKE_FRFLT, address 0x4001 0028) bit description

Bit	Symbol	Description	Reset value	Access
31:0	ADDR	WKUPFMFILTER address	-	R/W

22.6.11 MAC PMT control and status register

The PMT control and status registers programs the request wake-up events and monitors the wake-up events. See Section 22.7.1 for details.

Table 414. MAC PMT control and status register (MAC_PMT_CTRL_STAT, address 0x4001 002C) bit description

Bit	Symbol	Description	Reset value	Access
0	PD	Power-down When set, all received frames will be dropped. This bit is cleared automatically when a magic packet or Wake-Up frame is received, and Power-Down mode is disabled. Frames received after this bit is cleared are forwarded to the application.This bit must only be set when either the Magic Packet Enable or Wake- Up Frame Enable bit is set high.	0	R/WS/ SC
1	MPE	Magic packet enable When set, enables generation of a power management event due to Magic Packet reception.	0	R/W
2	WFE	Wake-up frame enable When set, enables generation of a power management event due to wake-up frame reception.	0	R/W
4:3	-	Reserved	00	RO
5	MPR	Magic Packet Received When set, this bit indicates the power management event was generated by the reception of a Magic Packet. This bit is cleared by a Read into this register.	0	R/SS/R C
6	WFR	Wake-up Frame Received When set, this bit indicates the power management event was generated due to reception of a wake-up frame. This bit is cleared by a Read into this register.	0	R/SS/R C
8:7	-	Reserved	0	RO
9	GU	Global Unicast When set, enables any unicast packet filtered by the MAC (DAF) address recognition to be a wake-up frame.	0	R/W
30:10	-	Reserved	0x00 0000	RO
31	WFFRPR	Wake-up Frame Filter Register Pointer Reset When set, resets the Remote Wake-up Frame Filter register pointer to 000. It is automatically cleared after 1 clock cycle.	0	R/WS/ SC

22.6.12 MAC Interrupt status register

The Interrupt Status register contents identify the events in the MAC-CORE that can generate interrupt.

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Table 415. MAC Interrupt status register (MAC_INTR, address 0x4001 0038) bit description

Bit	Symbol	Description	Reset value	Access
31:0	-	Reserved	0	RO

22.6.13 MAC Interrupt mask register

The Interrupt Mask Register bits enables the user to mask the interrupt signal due to the corresponding event in the Interrupt Status Register.

Table 416. MAC Interrupt mask register (MAC_INTR_MASK, address 0x4001 003C) bit description

Bit	Symbol	Description	Reset value	Access
2:0	-	Reserved	0	RO
3	PMTMSK	PMT Interrupt Mask This bit when set, will disable the assertion of the interrupt signal due to the setting of PMT Interrupt Status bit in Table 415.	0	R/W
31:4		Reserved	0	R/W

22.6.14 MAC Address 0 high register

The MAC Address 0 High register holds the upper 16 bits of the 6-byte first MAC address of the station. Note that the first DA byte that is received on the (G)MII interface corresponds to the LS Byte (Bits [7:0]) of the MAC Address Low register. For example, if 0x112233445566 is received (0x11 is the first byte) on the (G)MII as the destination address, then the MacAddress0 Register [47:0] is compared with 0x665544332211.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, then the synchronization is triggered only when Bits[31:24] (in Little-Endian mode) or Bits[7:0] (in Big-Endian mode) of the MAC Address Low Register (Register 17) are written to. Please note that consecutive writes to this Address Low Register should be performed only after at least 4 clock cycles in the destination clock domain for proper synchronization updates.

Table 417. MAC Address 0 high register (MAC_ADDR0_HIGH, address 0x4001 0040) bit description

Bit	Symbol	Description	Reset value	Access
15:0	A47_32	MAC Address0 [47:32] This field contains the upper 16 bits (47:32) of the 6-byte first MAC address. This is used by the MAC for filtering for received frames and for inserting the MAC address in the Transmit Flow Control (PAUSE) Frames.	0xFFFF	R/W
30:16	-	Reserved	0x0000	RO
31	MO	Always 1	1	RO

22.6.15 MAC Address 0 low register

The MAC Address 0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station.

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Table 418. MAC Address 0 low register (MAC_ADDR0_LOW, address 0x4001 0044) bit description

Bit	Symbol	Description	Reset value	Access
31:0	A31_0	MAC Address0 [31:0] This field contains the lower 32 bits of the 6-byte first MAC address. This is used by the MAC for filtering for received frames and for inserting the MAC address in the Transmit Flow Control (PAUSE) Frames.	0xFFFF FFFF	R/W

22.6.16 MAC IEEE1588 time stamp control register

This register controls the operation of the System Time generator and the snooping of PTP packets for time-stamping in the Receiver.

Table 419. MAC IEEE1588 time stamp control register (MAC_TIMESTP_CTRL, address 0x4001 0700) bit description

Bit	Symbol	Description	Reset value	Access
0	TSENA	Time Stamp Enable When this bit, is set the timestamping is enabled for transmit and receive frames. When disabled timestamp is not added for transmit and receive frames and the TimeStamp Generator is also suspended. User has to always initialize the TimeStamp (system time) after enabling this mode.	0	R/W
1	TSCFUPDT	Time Stamp Fine or Coarse Update When set, indicates that the system times update to be done using fine update method. When reset it indicates the system time stamp update to be done using Coarse method. This bit is reserved if the fine correction option is not enabled.	0	R/W
2	TSINIT	Time Stamp Initialize When set, the system time is initialized (over-written) with the value specified in the Time Stamp High Update and Time Stamp Low Update registers. This register bit should be read zero before updating it. This bit is reset once the initialize is complete.	0	R/W/SC
3	TSUPDT	Time Stamp Update When set, the system time is updated (added/subtracted) with the value specified in the Time Stamp High Update and Time Stamp Low Update registers. This register bit should be read zero before updating it. This bit is reset once the update is completed in hardware.	0	R/W/SC
4	TSTRIG	Time Stamp Interrupt Trigger Enable When set, the Time Stamp interrupt is generated when the System Time becomes greater than the value written in Target Time register. This bit is reset after the generation of Time Stamp Trigger Interrupt.	0	R/WSC
5	TSADDREG	Addend Reg Update When set, the contents of the Time Stamp Addend register is updated in the PTP block for fine correction. This is cleared when the update is completed. This register bit should be zero before setting it. This is a reserved bit when only coarse correction option is selected.		
7:6	-	Reserved		
8	TSENALL	Enable Time Stamp for All Frames When set, the time stamp snapshot is enabled for all frames received by the core.	0	R/W

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Table 419. MAC IEEE1588 time stamp control register (MAC_TIMESTP_CTRL, address 0x4001 0700) bit description

Bit	Symbol	Description	Reset value	Access
9	TSCTRLSSR	Time Stamp Digital or Binary rollover control When set, the Time Stamp Low register rolls over after 0x3B9A_C9FF value (i.e., 1 nanosecond accuracy) and increments the Time Stamp (High) seconds. When reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment has to be programmed correctly depending on the PTP reference clock frequency and this bit value.	0	R/W
10	TSVER2ENA	Enable PTP packet snooping for version 2 format When set, the PTP packets are snooped using the 1588 version 2 format else snooped using the version 1 format.	0	R/W
11	TSIPENA	Enable Time Stamp Snapshot for PTP over Ethernet frames When set, the time stamp snapshot is taken for frames which have PTP messages in Ethernet frames (PTP over Ethernet) also. By default snapshots are taken for UDP-IP-Ethernet PTP packets.	0	R/W
12	TSIPV6ENA	Enable Time Stamp Snapshot for IPv6 frames When set, the time stamp snapshot is taken for IPv6 frames.	0	R/W
13	TSIPV4ENA	Enable Time Stamp Snapshot for IPv4 frames When set, the time stamp snapshot is taken for IPv4 frames.	1	R/W
14	TSEVNTENA	Enable Time Stamp Snapshot for Event Messages When set, the time stamp snapshot is taken for event messages only . When reset snapshot is taken for all other messages except Announce, Management and Signaling.	0	R/W
15	TSMSTRENA	Enable Snapshot for Messages Relevant to Master When set, the snapshot is taken for messages relevant to master node only else snapshot is taken for messages relevant to slave node. This is valid only for ordinary clock and boundary clock node.	0	R/W
17:16	TSCLKTYPE	Select the type of clock node The following are the options to select the type of clock node: 00 = ordinary clock 01 = boundary clock 10 = end-to-end transparent clock 11 = peer-to-peer transparent clock	00	R/W
18	TSENMACADDR	Enable MAC address for PTP frame filtering When set, uses the DA MAC address (that matches any MAC Address register except the default MAC address 0) to filter the PTP frames when PTP is sent directly over Ethernet.	0	R/W
31:19				

Table 420 indicates the messages, for which a snapshot is taken depending on the clock, enable master and enable snapshot for event message register settings.

Table 420. Time stamp snapshot dependency on register bits

TSCLKTYPE	TSMSTRENA	TSEVNTENA	Messages for which snapshot is taken
00 or 01	x	0	SYNC, Follow_Up, Delay_Req, Delay_Resp
00 or 01	1	1	Delay_req
00 or 01	0	1	SYNC
10	N/A	0	SYNC, Follow_Up, Delay_Req, Delay_Resp

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Table 420. Time stamp snapshot dependency on register bits

TSCLKTYPE	TSMSTRENA	TSEVNTENA	Messages for which snapshot is taken
10	N/A	1	SYNC, Follow_Up
11	N/A	0	SYNC, Follow_Up, Delay_Req, Delay_Resp, Pdelay_Req, Pdelay_Resp
11	N/A	1	SYNC, Pdelay_Req, Pdelay_Resp

22.6.17 DMA Bus mode register

The Bus Mode register establishes the bus operating modes for the DMA.

Table 421. DMA Bus mode register (DMA_BUS_MODE, address 0x4001 1000) bit description

Bit	Symbol	Description	Reset value	Access
0	SWR	Software reset When this bit is set, the MAC DMA Controller resets all MAC Subsystem internal registers and logic. It is cleared automatically after the reset operation has completed in all of the core clock domains. Read a 0 value in this bit before re-programming any register of the core. **Remark:** The reset operation is completed only when all the resets in all the active clock domains are de-asserted. Hence it is essential that all the PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion.	0	R/WS/SC
1	DA	DMA arbitration scheme 0 = Round-robin with Rx:Tx priority given in bits [15:14] 1 = Rx has priority over Tx	0	R/W
6:2	DSL	Descriptor skip length This bit specifies the number of Word/Dword/Lword (depending on 32/64/128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of current descriptor to the start of next descriptor. When DSL value equals zero, then the descriptor table is taken as contiguous by the DMA, in Ring mode.	0	R/W
7	ATDS	Alternate (Enhanced) descriptor size When set, the alternate (enhanced) descriptor (see Section 22.9) size is increased to 32 bytes (8 DWORDS). This is required when the Advanced Time-Stamp feature or Full IPC Offload Engine is enabled in the receiver. When reset, the descriptor size reverts back to 4 DWORDs (16 bytes). This bit is present only when Alternate Descriptor feature is selected and either Advanced Time Stamp or IPC Full Checksum Offload (type 2) feature is selected during configuration. Otherwise, this bit is reserved and read-only.	0	R/W

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Table 421. DMA Bus mode register (DMA_BUS_MODE, address 0x4001 1000) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
13:8	PBL	Programmable burst length These bits indicate the maximum number of beats to be transferred in one DMA transaction. This will be the maximum value that is used in a single block Read/Write. The DMA will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. PBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value will result in undefined behavior. When USP is set high, this PBL value is applicable for TxDMA transactions only. The PBL values have the following limitations. The maximum number of beats (PBL) possible is limited by the size of the Tx FIFO and Rx FIFO in the MTL layer and the data bus width on the DMA. The FIFO has a constraint that the maximum beat supported is half the depth of the FIFO, except when specified (as given below). For different data bus widths and FIFO sizes, the valid PBL range (including x8 mode) is provided in the following table. If the PBL is common for both transmit and receive DMA, the minimum Rx FIFO and Tx FIFO depths must be considered. Do not program out-of-range PBL values, because the system may not behave properly.	1	R/W
15:14	PR	Rx-to-Tx priority ratio RxDMA requests given priority over TxDMA requests in the following ratio. This is valid only when the DA bit is reset. 00 = 1-to-1 01 = 2-to-1 10 = 3-to-1 11 = 4-to-1	00	R/W
16	FB	Fixed burst This bit controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.	0	R/W
22:17	RPBL	RxDMA PBL These bits indicate the maximum number of beats to be transferred in one RxDMA transaction. This will be the maximum value that is used in a single block Read/Write. The RxDMA will always attempt to burst as specified in RPBL each time it starts a Burst transfer on the host bus. RPBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value will result in undefined behavior. These bits are valid and applicable only when USP is set high.	1	R/W
23	USP	Use separate PBL When set high, it configures the RxDMA to use the value configured in bits [22:17] as PBL while the PBL value in bits [13:8] is applicable to TxDMA operations only. When reset to low, the PBL value in bits [13:8] is applicable for both DMA engines.	0	R/W
24	PBL8X	8 x PBL mode When set high, this bit multiplies the PBL value programmed (bits [22:17] and bits [13:8]) eight times. Thus the DMA will transfer data in to a maximum of 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. **Remark:** This bit function is not backward compatible. Before version 3.50a, this bit was 4xPBL.	0	R/W

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Table 421. DMA Bus mode register (DMA_BUS_MODE, address 0x4001 1000) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
25	AAL	Address-aligned beats When this bit is set high and the FB bit equals 1, the AHB interface generates all bursts aligned to the start address LS bits. If the FB bit equals 0, the first burst (accessing the data buffer's start address) is not aligned, but subsequent bursts are aligned to the address.	0	R/W
26	MB	Mixed burst When this bit is set high and FB bit is low, the AHB master interface will start all bursts of length more than 16 with INCR (undefined burst) whereas it will revert to fixed burst transfers (INCRx and SINGLE) for burst-length of 16 and below.	0	R/W
27	TXPR	When set, this bit indicates that the transmit DMA has higher priority than the receive DMA during arbitration for the system-side bus.	0	R/W
29:28	-		0	RO
31:30	-	Reserved	0	RO

Table 422. Programmable burst length settings

Data bus width	FIFO depth	Valid PBL range in full duplex mode
32 bit	128 bytes	8 or less
	256 bytes	32 or less
	512 bytes	64 or less
	1 kB	128 or less
	2 kB and above	all

22.6.18 DMA Transmit poll demand register

The Transmit Poll Demand register enables the Transmit DMA to check whether or not the current descriptor is owned by DMA. The Transmit Poll Demand command is given to wake up the TxDMA if it is in Suspend mode. The TxDMA can go into Suspend mode due to an Underflow error in a transmitted frame or due to the unavailability of descriptors owned by Transmit DMA. You can give this command anytime and the TxDMA will reset this command once it starts re-fetching the current descriptor from host memory.

Table 423. DMA Transmit poll demand register (DMA_TRANS_POLL_DEMAND, address 0x4001 1004) bit description

Bit	Symbol	Description	Reset value	Access
31:0	TPD	Transmit poll demand When these bits are written with any value, the DMA reads the current descriptor pointed to by the Current Host Transmit Descriptor register (Section 22.6.27). If that descriptor is not available (owned by Host), transmission returns to the Suspend state and bit 2 in the DMA_STAT Register is asserted. If the descriptor is available, transmission resumes.	0	RO/WT

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22.6.19 DMA Receive poll demand register

The Receive Poll Demand register enables the receive DMA to check for new descriptors. This command is given to wake up the RxDMA from SUSPEND state. The RxDMA can go into SUSPEND state only due to the unavailability of descriptors owned by it.

Table 424. DMA Receive poll demand register (DMA_REC_POLL_DEMAND, address 0x4001 1008) bit description

Bit	Symbol	Description	Reset value	Access
31:0	RPD	Receive poll demand When these bits are written with any value, the DMA reads the current descriptor pointed to by the Current Host Receive Descriptor register (Section 22.6.28). If that descriptor is not available (owned by Host), reception returns to the Suspended state and bit 7 in the DMA_STAT Register is not asserted. If the descriptor is available, the Receive DMA returns to active state.	0	RO/WT

22.6.20 DMA Receive descriptor list address register

The Receive Descriptor List Address register points to the start of the Receive Descriptor List. The descriptor lists reside in the host’s physical memory space and must be Word/Dword/Lword-aligned (for 32/64/128- bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given.

Table 425. DMA Receive descriptor list address register (DMA_REC_DES_ADDR, address 0x4001 100C) bit description

Bit	Symbol	Description	Reset value	Access
31:0	SRL	Start of receive list This field contains the base address of the First Descriptor in the Receive Descriptor list. The LSB bits [1/2/3:0] for 32/64/128-bit bus width) will be ignored and taken as all-zero by the DMA internally. Hence these LSB bits are Read Only.	0	R/W

22.6.21 DMA Transmit descriptor list address register

The Transmit Descriptor List Address register points to the start of the Transmit Descriptor List. The descriptor lists reside in the host’s physical memory space and must be Word/DWORD/LWORD-aligned (for 32/64/128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. Writing to this register is permitted only when transmission has stopped. When stopped, this register can be written before the transmission Start command is given.

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Table 426. DMA Transmit descriptor list address register (DMA_TRANS_DES_ADDR, address 0x4001 1010) bit description

Bit	Symbol	Description	Reset value	Access
31:0	SRL	Start of transmit list This field contains the base address of the First Descriptor in the Transmit Descriptor list. The LSB bits [1/2/3:0] for 32/64/128-bit bus width) will be ignored and taken as all-zero by the DMA internally. Hence these LSB bits are Read Only.	0	R/W

22.6.22 DMA Status register

The Status register contains all the status bits that the DMA reports to the host. This register is usually read by the Software driver during an interrupt service routine or polling. Most of the fields in this register cause the host to be interrupted. The bits in this register are not cleared when read. Writing 1 to (unreserved) bits in this register (bits [16:0]) clears them and writing 0 has no effect. Each field (bits[16:0]) can be masked by masking the appropriate bit in the DMA_INT_EN register.

Table 427. DMA Status register (DMA_STAT, address 0x4001 1014) bit description

Bit	Symbol	Description	Reset value	Access
0	TI	Transmit interrupt This bit indicates that frame transmission is finished and TDES1[31] is set in the First Descriptor.	0	R/SS/WC
1	TPS	Transmit process stopped This bit is set when the transmission is stopped.	0	R/SS/WC
2	TU	Transmit buffer unavailable This bit indicates that the Next Descriptor in the Transmit List is owned by the host and cannot be acquired by the DMA. Transmission is suspended. Bits[22:20] explain the Transmit Process state transitions. To resume processing transmit descriptors, the host should change the ownership of the bit of the descriptor and then issue a Transmit Poll Demand command.	0	R/SS/WC
3	TJT	Transmit jabber timeout This bit indicates that the Transmit Jabber Timer expired, meaning that the transmitter had been excessively active. The transmission process is aborted and placed in the Stopped state. This causes the Transmit Jabber Timeout TDES0[14] flag to assert.	0	R/SS/WC
4	OVF	Receive overflow This bit indicates that the Receive Buffer had an Overflow during frame reception. If the partial frame is transferred to application, the overflow status is set in RDES0[11].	0	R/SS/WC
5	UNF	Transmit underflow This bit indicates that the Transmit Buffer had an Underflow during frame transmission. Transmission is suspended and an Underflow Error TDES0[1] is set.	0	R/SS/WC
6	RI	Receive interrupt This bit indicates the completion of frame reception. Specific frame status information has been posted in the descriptor. Reception remains in the Running state.	0	R/SS/WC

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Table 427. DMA Status register (DMA_STAT, address 0x4001 1014) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
7	RU	Receive buffer unavailable This bit indicates that the Next Descriptor in the Receive List is owned by the host and cannot be acquired by the DMA. Receive Process is suspended. To resume processing Receive descriptors, the host should change the ownership of the descriptor and issue a Receive Poll Demand command. If no Receive Poll Demand is issued, Receive Process resumes when the next recognized incoming frame is received. This bit is set only when the previous Receive Descriptor was owned by the DMA.	0	R/SS/WC
8	RPS	Received process stopped This bit is asserted when the Receive Process enters the Stopped state.	0	R/SS/WC
9	RWT	Receive watchdog timeout This bit is asserted when a frame with a length greater than 2,048 bytes is received (10,240 when Jumbo Frame mode is enabled).	0	R/SS/WC
10	ETI	Early transmit interrupt This bit indicates that the frame to be transmitted was fully transferred to the MTL Transmit FIFO.	0	R/SS/WC
12:11	-	Reserved	0	RO
13	FBI	Fatal bus error interrupt This bit indicates that a bus error occurred, as detailed in bits [25:23]. When this bit is set, the corresponding DMA engine disables all its bus accesses.	0	R/SS/WC
14	ERI	Early receive interrupt This bit indicates that the DMA had filled the first data buffer of the packet. Receive Interrupt bit 6 in this register automatically clears this bit.	0	R/SS/WC

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Table 427. DMA Status register (DMA_STAT, address 0x4001 1014) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
15	AIE	Abnormal interrupt summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_INT_EN register: DMA_STAT register, bit 1: Transmit process stopped DMA_STAT register, bit 3: Transmit jabber timeout DMA_STAT register, bit 4: Receive overflow DMA_STAT register, bit 5: Transmit underflow DMA_STAT register, bit 7: Receiver buffer unavailable DMA_STAT register, bit 8: Receive process stopped DMA_STAT register, bit 9: Receive watchdog timeout DMA_STAT register, bit 10: Early transmit interrupt DMA_STAT register, bit 13: Fatal bus error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared.	0	R/SS/ WC
16	NIS	Normal interrupt summary Normal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_INT_EN register: DMA_STAT register, bit 0: Transmit interrupt DMA_STAT register, bit 2: Transmit buffer unavailable DMA_STAT register, bit 6: Receive interrupt DMA_STAT register, bit 14: Early receive interrupt Only unmasked bits affect the Normal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing a 1 to this bit) each time a corresponding bit that causes NIS to be set is cleared.	0	R/SS/ WC
31:17	-	Reserved	0	RO

22.6.23 DMA Operation mode register

The Operation Mode register establishes the Transmit and Receive operating modes and commands. This register should be the last CSR to be written as part of DMA initialization.

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Table 428. DMA operation mode register (DMA_OP_MODE, address 0x4001 1018) bit description

Bit	Symbol	Description	Reset value	Access
0	-	Reserved	0	RO
1	SR	Start/stop receive When this bit is set, the Receive process is placed in the Running state. The DMA attempts to acquire the descriptor from the Receive list and processes incoming frames. Descriptor acquisition is attempted from the current position in the list, which is the address set by the DMA_REC_DES_ADDR register or the position retained when the Receive process was previously stopped. If no descriptor is owned by the DMA, reception is suspended and Receive Buffer Unavailable bit (bit 7 in DMA_STAT register) is set. The Start Receive command is effective only when reception has stopped. If the command was issued before setting the DMA_REC_DES_ADDR, DMA behavior is unpredictable.	0	R/W
2	OSF	Operate on second frame When this bit is set, this bit instructs the DMA to process a second frame of Transmit data even before status for first frame is obtained.	0	R/W
4:3	RTC	Receive threshold control These two bits control the threshold level of the MTL Receive FIFO. Transfer (request) to DMA starts when the frame size within the MTL Receive FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are transferred automatically. Note that value of 11 is not applicable if the configured Receive FIFO size is 128 bytes. These bits are valid only when the RSF bit is zero, and are ignored when the RSF bit is set to 1. 00 = 64 01 = 32 10 = 96 11 = 128	0	R/W
5	-	Reserved	0	RO
6	FUF	Forward undersized good frames When set, the Rx FIFO will forward Undersized frames (frames with no Error and length less than 64 bytes) including pad-bytes and CRC). When reset, the Rx FIFO will drop all frames of less than 64 bytes, unless it is already transferred due to lower value of Receive Threshold (e.g., RTC = 01).	0	R/W
7	FEF	Forward error frames When this bit is reset, the Rx FIFO drops frames with error status (CRC error, collision error, GMII_ER, giant frame, watchdog timeout, overflow). However, if the frame's start byte (write) pointer is already transferred to the read controller side (in Threshold mode), then the frames are not dropped. . When FEF is set, all frames except runt error frames are forwarded to the DMA. But when RxFIFO overflows when a partial frame is written, then such frames are dropped even when FEF is set.	0	R/W
12:8	-	Reserved	0	RO

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Table 428. DMA operation mode register (DMA_OP_MODE, address 0x4001 1018) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
13	ST	Start/Stop Transmission Command When this bit is set, transmission is placed in the Running state, and the DMA checks the Transmit List at the current position for a frame to be transmitted. Descriptor acquisition is attempted either from the current position in the list, which is the Transmit List Base Address set by the DMA_TRANS_DES_ADDR register or from the position retained when transmission was stopped previously. If the current descriptor is not owned by the DMA, transmission enters the Suspended state and Transmit Buffer Unavailable (DMA_STAT register, bit 2) is set. The Start Transmission command is effective only when transmission is stopped. If the command is issued before setting the DMA_TRANS_DES_ADDR register, then the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current frame. The Next Descriptor position in the Transmit List is saved, and becomes the current position when transmission is restarted. The stop transmission command is effective only the transmission of the current frame is complete or when the transmission is in the Suspended state.	0	R/W
16:14	TTC	Transmit threshold control These three bits control the threshold level of the MTL Transmit FIFO. Transmission starts when the frame size within the MTL Transmit FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are also transmitted. These bits are used only when the TSF bit (Bit 21) is reset. 000 = 64 001 = 128 010 = 192 011 = 256 100 = 40 101 = 32 110 = 24 111 = 16	0	R/W
19:17	-	Reserved	0	RO
20	FTF	Flush transmit FIFO When this bit is set, the transmit FIFO controller logic is reset to its default values and thus all data in the Tx FIFO is lost/flushed. This bit is cleared internally when the flushing operation is completed fully. The Operation Mode register should not be written to until this bit is cleared. The data which is already accepted by the MAC transmitter will not be flushed. It will be scheduled for transmission and will result in underflow and runt frame transmission. **Remark:** The flush operation completes only after emptying the TxFIFO of its contents and all the pending Transmit Status of the transmitted frames are accepted by the host. In order to complete this flush operation, the PHY transmit clock is required to be active.	0	R/WS/ SC
21	TSF	Transmit store and forward When this bit is set, transmission starts when a full frame resides in the MTL Transmit FIFO. When this bit is set, the TTC values specified in this register (bits [16:14]) are ignored. This bit should be changed only when transmission is stopped.	0	R/W
23:22	-	Reserved	0	RO

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Table 428. DMA operation mode register (DMA_OP_MODE, address 0x4001 1018) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
24	DFF	Disable flushing of received frames When this bit is set, the RxDMA does not flush any frames due to the unavailability of receive descriptors/buffers as it does normally when this bit is reset. (See).	0	R/W
25	RSF	Receive store and forward When this bit is set, the MTL only reads a frame from the Rx FIFO after the complete frame has been written to it, ignoring RTC bits. When this bit is reset, the Rx FIFO operates in Cut-Through mode, subject to the threshold specified by the RTC bits.	0	R/W
26	DT	Disable Dropping of TCP/IP Checksum Error Frames When this bit is set, the core does not drop frames that only have errors detected by the Receive Checksum Offload engine. Such frames do not have any errors (including FCS error) in the Ethernet frame received by the MAC but have errors in the encapsulated payload only. When this bit is reset, all error frames are dropped if the FEF bit is reset.	0	R/W
31:27	-	Reserved	0	RO

22.6.24 DMA Interrupt enable register

The Interrupt Enable register enables the interrupts reported by the DMA_STAT register. Setting a bit to 1 enables a corresponding interrupt. After a hardware or software reset, all interrupts are disabled.

Table 429. DMA Interrupt enable register (DMA_INT_EN, address 0x4001 101C) bit description

Bit	Symbol	Description	Reset value	Access
0	TIE	Transmit interrupt enable When this bit is set with Normal Interrupt Summary Enable (bit 16 in this register), Transmit Interrupt is enabled. When this bit is reset, Transmit Interrupt is disabled.	0	R/W
1	TSE	Transmit stopped enable When this bit is set with Abnormal Interrupt Summary Enable (bit 15 in this register), Transmission Stopped Interrupt is enabled. When this bit is reset, Transmission Stopped Interrupt is disabled.	0	R/W
2	TUE	Transmit buffer unavailable enable When this bit is set with Normal Interrupt Summary Enable (bit 16 in this register), Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, Transmit Buffer Unavailable Interrupt is disabled.	0	R/W
3	TJE	Transmit jabber timeout enable When this bit is set with Abnormal Interrupt Summary Enable (bit 15 in this register), Transmit Jabber Timeout Interrupt is enabled. When this bit is reset, Transmit Jabber Timeout Interrupt is disabled.	0	R/W
4	OVE	Overflow interrupt enable When this bit is set with Abnormal Interrupt Summary Enable (bit 15 in this register), Receive Overflow Interrupt is enabled. When this bit is reset, Overflow Interrupt is disabled.	0	R/W
5	UNE	Underflow interrupt enable When this bit is set with Abnormal Interrupt Summary Enable (bit 15 in this register), Transmit Underflow Interrupt is enabled. When this bit is reset, Underflow Interrupt is disabled.	0	R/W

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Table 429. DMA Interrupt enable register (DMA_INT_EN, address 0x4001 101C) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
6	RIE	Receive interrupt enable When this bit is set with Normal Interrupt Summary Enable (bit 16 in this register), Receive Interrupt is enabled. When this bit is reset, Receive Interrupt is disabled.	0	R/W
7	RUE	Receive buffer unavailable enable When this bit is set with Abnormal Interrupt Summary Enable (bit 15 in this register), Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable Interrupt is disabled.	0	R/W
8	RSE	Received stopped enable When this bit is set with Abnormal Interrupt Summary Enable (bit 15 in this register), Receive Stopped Interrupt is enabled. When this bit is reset, Receive Stopped Interrupt is disabled.	0	R/W
9	RWE	Receive watchdog timeout enable When this bit is set with Abnormal Interrupt Summary Enable (bit 15 in this register), the Receive Watchdog Timeout Interrupt is enabled. When this bit is reset, Receive Watchdog Timeout Interrupt is disabled.	0	R/W
10	ETE	Early transmit interrupt enable When this bit is set with an Abnormal Interrupt Summary Enable (bit 15 in this register), Early Transmit Interrupt is enabled. When this bit is reset, Early Transmit Interrupt is disabled.	0	R/W
12:11	-	Reserved	0	RO
13	FBE	Fatal bus error enable When this bit is set with Abnormal Interrupt Summary Enable (bit 15 in this register), the Fatal Bus Error Interrupt is enabled. When this bit is reset, Fatal Bus Error Enable Interrupt is disabled.	0	R/W
14	ERE	Early receive interrupt enable When this bit is set with Normal Interrupt Summary Enable (bit 16 in this register), Early Receive Interrupt is enabled. When this bit is reset, Early Receive Interrupt is disabled.	0	R/W

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Table 429. DMA Interrupt enable register (DMA_INT_EN, address 0x4001 101C) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
15	AIE	Abnormal interrupt summary enable When this bit is set, an Abnormal Interrupt is enabled. When this bit is reset, an Abnormal Interrupt is disabled. This bit enables the following bits DMA_STAT register, bit 1: Transmit process stopped DMA_STAT register, bit 3: Transmit jabber timeout DMA_STAT register, bit 4: Receive overflow DMA_STAT register, bit 5: Transmit underflow DMA_STAT register, bit 7: Receiver buffer unavailable DMA_STAT register, bit 8: Receive process stopped DMA_STAT register, bit 9: Receive watchdog timeout DMA_STAT register, bit 10: Early transmit interrupt DMA_STAT register, bit 13: Fatal bus error	0	R/W
16	NIE	Normal interrupt summary enable When this bit is set, a normal interrupt is enabled. When this bit is reset, a normal interrupt is disabled. This bit enables the following bits: DMA_STAT register, bit 0: Transmit interrupt DMA_STAT register, bit 2: Transmit buffer unavailable DMA_STAT register, bit 6: Receive interrupt DMA_STAT register, bit 14: Early receive interrupt	0	R/W
31:17	-	Reserved	0	RO

The interrupt (sbd_intr_o_interrupt) is generated as shown in Figure 44. It is asserted when the NIS/AIS Status bit is asserted and the corresponding Interrupt Enable bits (NIE/AIE) are enabled.

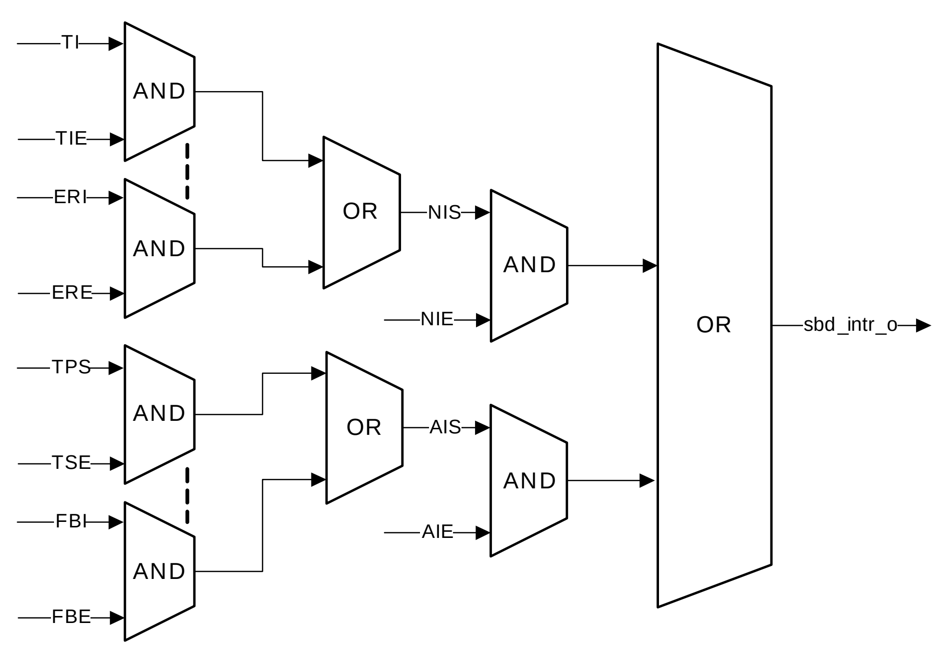


Fig 44. Interrupt generation

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22.6.25 DMA Missed frame and buffer overflow counter register

The DMA maintains two counters to track the number of missed frames during reception. This register reports the current value of the counter. The counter is used for diagnostic purposes. Bits[15:0] indicate missed frames due to the host buffer being unavailable. Bits[27:17] indicate missed frames due to buffer overflow conditions (MTL and MAC) and runt frames (good frames of less than 64 bytes) dropped by the MTL.

Table 430. DMA Missed frame and buffer overflow counter register (DMA_MFRM_BUFOF, address 0x4001 1020) bit description

Bit	Symbol	Description	Reset value	Access
15:0	FMC	Number of frames missed Indicates the number of frames missed by the controller due to the Host Receive Buffer being unavailable. This counter is incremented each time the DMA discards an incoming frame. The counter is cleared when this register is read with .	0	R/SS/RC
16	OC	Overflow bit for missed frame counter	0	R/SS/RC
27:17	FMA	Number of frames missed by the application Indicates the number of frames missed by the application. This counter is incremented each time the MTL asserts the sideband signal mtl_rxoverflow_o. The counter is cleared when this register is read with <tbd> .	0	R/SS/RC
28	OF	Overflow bit for FIFO overflow counter	0	R/SS/RC
31:29	-	Reserved	0	RO

22.6.26 DMA Receive interrupt watchdog timer register

This register, when written with non-zero value, will enable the watchdog timer for RI (bit 6 in the DMA_STAT register).

Table 431. DMA Receive interrupt watchdog timer register (DMA_REC_INT_WDT, address 0x4001 1024) bit description

Bit	Symbol	Description	Reset value	Access
7:0	RIWT	RI watchdog timeout Indicates the number of system clock cycles multiplied by 256 for which the watchdog timer is set. The watchdog timer gets triggered with the programmed value after the RxDMA completes the transfer of a frame for which the RI status bit is not set due to the setting in the corresponding descriptor RDES1[31]. When the watch-dog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when RI bit is set high due to automatic setting of RI as per RDES1[31] of any received frame.	0	R/W
31:8	-	Reserved	0	RO

22.6.27 DMA Current host transmit descriptor register

The Current Host Transmit Descriptor register points to the start address of the current Transmit Descriptor read by the DMA.

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Table 432. DMA Current host transmit descriptor register (DMA_CURHOST_TRANS_DES, address 0x4001 1048) bit description

Bit	Symbol	Description	Reset value	Access
31:0	HTD	Host Transmit Descriptor Address Pointer Cleared on Reset. Pointer updated by DMA during operation.	0	RO

22.6.28 DMA Current host receive descriptor register

The Current Host Receive Descriptor register points to the start address of the current Receive Descriptor read by the DMA.

Table 433. DMA Current host receive descriptor register (DMA_CURHOST_REC_DES, address 0x4001 104C) bit description

Bit	Symbol	Description	Reset value	Access
31:0	HRD	Host Receive Descriptor Address Pointer Cleared on Reset. Pointer updated by DMA during operation.	0	RO

22.6.29 DMA Current host transmit buffer address register

The Current Host Transmit Buffer Address register points to the current Transmit Buffer Address being read by the DMA.

Table 434. DMA Current host transmit buffer address register (DMA_CURHOST_TRANS_BUF, address 0x4001 1050) bit description

Bit	Symbol	Description	Reset value	Access
31:0	HTB	Host Transmit Buffer Address Pointer Cleared on Reset. Pointer updated by DMA during operation.	0	RO

22.6.30 DMA Current host receive buffer address register

The Current Host Receive Buffer Address register points to the current Receive Buffer address being read by the DMA.

Table 435. DMA Current host receive buffer address register (DMA_CURHOST_REC_BUF, address 0x4001 1054) bit description

Bit	Symbol	Description	Reset value	Access
31:0	HRB	Host Receive Buffer Address Pointer Cleared on Reset. Pointer updated by DMA during operation.	0	RO

22.7 Functional description

<tbd>

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22.7.1 Power management block

This section describes the power management (PMT) mechanisms supported by the MAC. PMT supports the reception of network (remote) wake-up frames and Magic Packet frames. PMT does not perform the clock gate function, but generates interrupts for wake-up frames and Magic Packets received by the MAC. The PMT block sits on the receiver path of the MAC and is enabled with remote wake-up frame enable and Magic Packet enable. These enables are in the PMT Control and Status register and are programmed by the Application.

When the power-down mode is enabled in the PMT, then all received frames are dropped by the core and they are not forwarded to the application. The core comes out of the power down mode only when either a Magic Packet or a Remote Wake-up frame is received and the corresponding detection is enabled.

22.7.1.1 Remote wake-up frame registers

The register wkupfmfilter_reg, address (0x028), loads the Wake-up Frame Filter register. To load values in a Wake-up Frame Filter register, the entire register (WKUPFMFILTER_REG) must be written. The WKUPFMFILTER_REG register is loaded by sequentially loading the eight register values in address (0x028) for WKUPFMFILTER_REG0, WKUPFMFILTER_REG1,... WKUPFMFILTER_REG7, respectively. WKUPFMFILTER_REG is read in the same way.

Remark: The internal counter to access the appropriate WKUPFMFILTER_REG is incremented when lane 3 (or lane 0 in big-endian) is accessed by the CPU. This should be kept in mind if you are accessing these registers in byte or half-word mode.

WKUPFMFILTER0	Filter 0 Byte Mask							
WKUPFMFILTER1	Filter 1 Byte Mask							
WKUPFMFILTER2	Filter 2 Byte Mask							
WKUPFMFILTER3	Filter 3 Byte Mask							
WKUPFMFILTER4	RSVD	Filter 3 Command	RSVD	Filter 2 Command	RSVD	Filter 1 Command	RSVD	Filter 0 Command
WKUPFMFILTER5	Filter 3 Offset		Filter 2 Offset		Filter 1 Offset		Filter 0 Offset	
WKUPFMFILTER6	Filter 1 CRC - 16				Filter 0 CRC - 16			
WKUPFMFILTER7	Filter 3 CRC - 16				Filter 2 CRC - 16			

Fig 45. Wake-up frame filter register

Filter i byte mask

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This register defines which bytes of the frame are examined by filter i (0, 1, 2, and 3) in order to determine whether or not the frame is a wake-up frame. The MSB (thirty-first bit) must be zero. Bit j [30:0] is the Byte Mask. If bit j (byte number) of the Byte Mask is set, then Filter i Offset + j of the incoming frame is processed by the CRC block; otherwise Filter i Offset + j is ignored.

Filter i command

This 4-bit command controls the filter i operation. Bit 3 specifies the address type, defining the pattern's destination address type. When the bit is set, the pattern applies to only multicast frames; when the bit is reset, the pattern applies only to unicast frame. Bit 2 and Bit 1 are reserved. Bit 0 is the enable for filter i; if Bit 0 is not set, filter i is disabled.

Filter i offset

This register defines the offset (within the frame) from which filter i examines the frames. This 8-bit pattern offset is the offset for the filter i first byte to be examined. The minimum allowed is 12, which refers to the 13th byte of the frame. The offset value 0 refers to the first byte of the frame.

Filter i CRC-16

This register contains the CRC_16 value calculated from the pattern, as well as the byte mask programmed to the wake-up filter register block.

22.7.1.2 Remote wake-up detection

When the MAC is in sleep mode and the remote wake-up bit is enabled in PMT Control and Status register (0x002C), normal operation is resumed after receiving a remote wake-up frame. The Application writes all eight wake-up filter registers by performing a sequential Write to address (0x0028). The Application enables remote wake-up by writing a 1 to Bit 2 of the PMT Control and Status register.

PMT supports four programmable filters that allow support of different receive frame patterns. If the incoming frame passes the address filtering of Filter Command, and if Filter CRC-16 matches the incoming examined pattern, then the wake-up frame is received.

Filter_offset (minimum value 12, which refers to the 13th byte of the frame) determines the offset from which the frame is to be examined. Filter Byte Mask determines which bytes of the frame must be examined. The thirty-first bit of Byte Mask must be set to zero.

The remote wake-up CRC block determines the CRC value that is compared with Filter CRC-16. The wake-up frame is checked only for length error, FCS error, dribble bit error, MII error, collision, and to ensure that it is not a runt frame. Even if the wake-up frame is more than 512 bytes long, if the frame has a valid CRC value, it is considered valid. Wake-up frame detection is updated in the PMT Control and Status register for every remote Wake-up frame received. A PMT interrupt to the Application triggers a Read to the PMT Control and Status register to determine reception of a wake-up frame.

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22.7.1.3 Magic packet detection

The Magic Packet frame is based on a method that uses Advanced Micro Device's Magic Packet technology to power up the sleeping device on the network. The MAC receives a specific packet of information, called a Magic Packet, addressed to the node on the network.

Only Magic Packets that are addressed to the device or a broadcast address will be checked to determine whether they meet the wake-up requirements. Magic Packets that pass the address filtering (unicast or broadcast) will be checked to determine whether they meet the remote Wake-on-LAN data format of 6 bytes of all ones followed by a MAC Address appearing 16 times.

The application enables Magic Packet wake-up by writing a 1 to Bit 1 of the PMT Control and Status register. The PMT block constantly monitors each frame addressed to the node for a specific Magic Packet pattern. Each frame received is checked for a 0xFFFF FFFF FFFF pattern following the destination and source address field. The PMT block then checks the frame for 16 repetitions of the MAC address without any breaks or interruptions. In case of a break in the 16 repetitions of the address, the 0xFFFF FFFF FFFF pattern is scanned for again in the incoming frame. The 16 repetitions can be anywhere in the frame, but must be preceded by the synchronization stream (0xFFFF FFFF FFFF). The device will also accept a multicast frame, as long as the 16 duplications of the MAC address are detected.

If the MAC address of a node is 0x0011 2233 4455, then the MAC scans for the data sequence:

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

...CRC

Magic Packet detection is updated in the PMT Control and Status register for Magic Packet received. A PMT interrupt to the Application triggers a read to the PMT CSR to determine whether a Magic Packet frame has been received.

22.7.1.4 System considerations during power-down

MAC neither gates nor stops clocks when Power-down mode is enabled. Power saving by clock gating must be done outside the core by the application. The receive data path must be clocked with ENET_RX_CLK during Power-down mode because it is involved in magic packet/wake-on-LAN frame detection. However, the transmit path and the application path clocks can be gated off during Power-down mode.

The PMT interrupt is asserted when a valid wake-up frame is received. This signal is generated in the receive clock domain

The recommended power-down and wake-up sequence is as follows.

1. Disable the Transmit DMA and wait for any previous frame transmissions to complete. These transmissions can be detected when Transmit Interrupt (see DMA_STAT register bit NIS; Table 427) is received.

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2. Disable the MAC transmitter and MAC receiver by clearing the appropriate bits in the MAC Configuration register.
3. Wait until the Receive DMA empties all the frames from the Rx FIFO (a software timer may be required).
4. Enable Power-Down mode by appropriately configuring the PMT registers.
5. Enable the MAC Receiver and enter Power-Down mode.
6. Gate the application and transmit clock inputs to the core (and other relevant clocks in the system) to reduce power and enter Sleep mode.
7. On receiving a valid wake-up frame, the MAC PMT interrupt signal and exits Power-Down mode.
8. On receiving the interrupt, the system must enable the application and transmit clock inputs to the core.
9. Read the PMT Status register to clear the interrupt, then enable the other modules in the system and resume normal operation.

Remark:

22.7.2 DMA arbiter functions

If you have enabled the transmit (Tx) DMA and receive (Rx) DMA of a channel, you can specify which DMA gets the bus when the channel gets the control of the bus. You can set the priority between the corresponding Tx DMA and Rx DMA by using the bit 27 (TXPR: Transmit Priority) of the DMA Bus Mode Register). For round-robin arbitration, you can use the bits [15:14] (PR: Priority Ratio) of the Bus Mode Register to specify the weighted priority between the Tx DMA and Rx DMA. Table 436 provides information about the priority scheme between Tx DMA and Rx DMA.

Table 436. Priority scheme for transmit and receive DMA

Bit 27	Bit 15	Bit 14	Bit 1	Priority scheme
0	x	x	x	Rx always has priority over Tx
0	0	0	0	Tx and Rx have equal priority. Rx gets the access first on simultaneous requests.
0	0	1	0	Rx has priority over Tx in the ratio 2:1.
0	1	0	0	Rx has priority over Tx in the ratio 3:1.
0	1	1	0	Rx has priority over Tx in the ratio 4:1.
1	x	x	1	Tx always has priority over Rx.
1	0	0	0	Tx and Rx have equal priority. Tx gets the access first on simultaneous requests.
1	0	1	0	Tx has priority over Rx in the ratio 2:1.
1	1	0	0	Tx has priority over Rx in the ratio 3:1.
1	1	1	0	Tx has priority over Rx in the ratio 4:1.

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22.7.3 IPC Receive checksum offload engine

In this mode, both IPv4 and IPv6 frames in the received Ethernet frames are detected and processed for data integrity.You can enable this module by setting the bit 10 (IPC) of the MAC configuration registe (Section 22.6.1). The MAC receiver identifies IPv4 or IPv6 frames by checking for value 0x0800 or 0x86DD, respectively, in the received Ethernet frames. Type field. This identification applies to VLAN-tagged frames as well.

The Receive Checksum Offload engine calculates IPv4 header checksums and checks that they match the received IPv4 header checksums. The result of this operation (pass or fail) is given to the RFC module for insertion into the receive status word. The IP Header Error bit is set for any mismatch between the indicated payload type (Ethernet Type field) and the IP header version, or when the received frame does not have enough bytes, as indicated by the IPv4 header.s Length field (or when fewer than 20 bytes are available in an IPv4 or IPv6 header).

This engine also identifies a TCP, UDP, or ICMP payload in the received IP datagrams (IPv4 or IPv6) and calculates the checksum of such payloads properly, as defined in the TCP, UDP, or ICMP specifications. This engine includes the TCP/UDP/ICMPv6 pseudo-header bytes for checksum calculation and checks whether the received checksum field matches the calculated value. The result of this operation is given as a Payload Checksum Error bit in the receive status word. This status bit is also set if the length of the TCP, UDP, or ICMP payload does not match the expected payload length given in the IP header.

This engine bypasses the payload of fragmented IP datagrams, IP datagrams with security features, IPv6 routing headers, and payloads other than TCP, UDP or ICMP.

22.8 DMA controller description

The DMA has independent Transmit and Receive engines and a CSR space. The Transmit engine transfers data from system memory to the device port (MTL), while the Receive engine transfers data from the device port to the system memory. The controller use descriptors to efficiently move data from source to destination with minimal Host CPU intervention. The DMA is designed for packet-oriented data transfers such as frames in Ethernet. The controller can be programmed to interrupt the Host CPU for situations such as Frame Transmit and Receive transfer completion, and other normal/error conditions.

The DMA and the Host driver communicate through two data structures:

- Control and Status registers (CSR). See Section 22.6.
- Descriptor lists and data buffers. See Section 22.9.

The DMA transfers data frames received by the core to the Receive Buffer in the Host memory, and Transmit data frames from the Transmit Buffer in the Host memory. Descriptors that reside in the Host memory act as pointers to these buffers. There are two descriptor lists; one for reception, and one for transmission. The base address of each list is written into DMA Registers Table 425 and Table 426. A descriptor list is forward linked (either implicitly or explicitly). The last descriptor may point back to the first entry to create a ring structure. Explicit chaining of descriptors is accomplished by setting the second address chained in both Receive and Transmit descriptors (RDES1[24] and TDES1[24]). The descriptor lists resides in the Host physical memory address space. Each descriptor can point to a maximum of two buffers. This enables two buffers to be used, physically

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addressed, rather than contiguous buffers in memory.

A data buffer resides in the Host physical memory space, and consists of an entire frame or part of a frame, but cannot exceed a single frame. Buffers contain only data, buffer status is maintained in the descriptor. Data chaining refers to frames that span multiple data buffers. However, a single descriptor cannot span multiple frames. The DMA skips to the next frame buffer when end-of-frame is detected. Data chaining can be enabled or disabled.

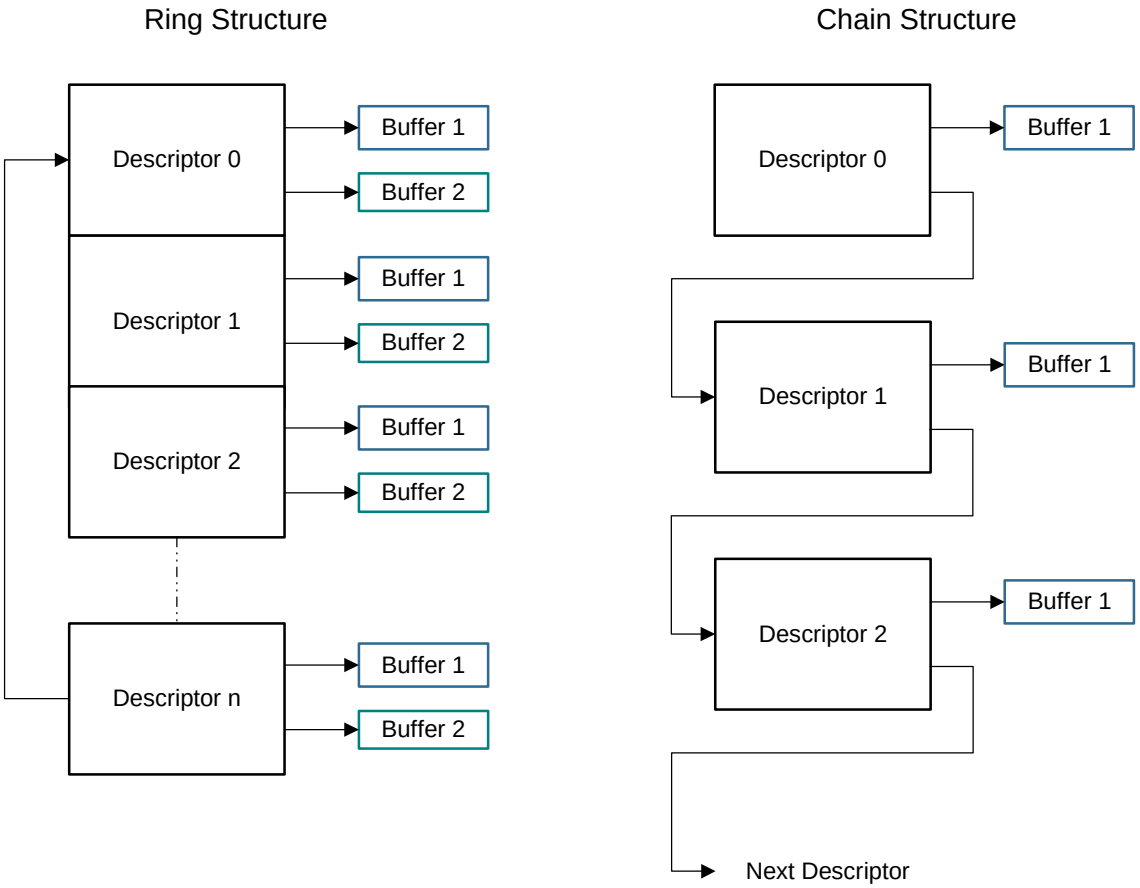


Fig 46. Descriptor ring and chain structure

22.8.1 Initialization

Follow these steps to initialize the ethernet controller:

1. Write to DMA Register Table 421 to set Host bus access parameters.
2. Write to DMA Register Table 429 to mask unnecessary interrupt causes.
3. The software driver creates the Transmit and Receive descriptor lists. Then it writes to both DMA Register Table 425 and DMA Register Table 426, providing the DMA with the starting address of each list.
4. Write to MAC Registers Table 404, Table 406, and Table 405 for desired filtering options.

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5. Write to MAC Register Table 403 to configure the operating mode and enable the transmit operation (bit 3: Transmitter Enable). The PS and DM bits are set based on the auto-negotiation result (read from the PHY).
6. Write to DMA Register Table 428 to set bits 13 and 1 to start transmission and reception.
7. Write to MAC Register Table 403 to enable the Receive operation (bit 2: Receiver Enable).

The Transmit and Receive engines enter the Running state and attempt to acquire descriptors from the respective descriptor lists. The Receive and Transmit engines then begin processing Receive and Transmit operations. The Transmit and Receive processes are independent of each other and can be started or stopped separately.

22.8.1.1 Host bus burst access

The DMA attempts to execute fixed-length Burst transfers on the AHB Master interface if configured to do so (FB bit of DMA Register 0). The maximum Burst length is indicated and limited by the PBL field (DMA Register 0[13:8]). The Receive and Transmit descriptors are always accessed in the maximum possible (limited by PBL or 16 x 8/bus width) burst-size for the 16-bytes to be read.

The Transmit DMA initiates a data transfer only when sufficient space to accommodate the configured burst is available in MTL Transmit FIFO or the number of bytes till the end of frame (when it is less than the configured burst-length). The DMA indicates the start address and the number of transfers required to the AHB Master Interface. When the AHB Interface is configured for fixed-length burst, then it transfers data using the best combination of INCR4/8/16 and SINGLE transactions. Otherwise (no fixed-length burst), it transfers data using INCR (undefined length) and SINGLE transactions.

The Receive DMA initiates a data transfer only when sufficient data to accommodate the configured burst is available in MTL Receive FIFO or when the end of frame (when it is less than the configured burst-length) is detected in the Receive FIFO. The DMA indicates the start address and the number of transfers required to the AHB Master Interface. When the AHB Interface is configured for fixed-length burst, then it transfers data using the best combination of INCR4/8/16 and SINGLE transactions. If the end-of frame is reached before the fixed-burst ends on the AHB interface, then dummy transfers are performed in order to complete the fixed-burst. Otherwise (FB bit of DMA Register Table 421 is reset), it transfers data using INCR (undefined length) and SINGLE transactions.

When the AHB interface is configured for address-aligned beats, both DMA engines ensure that the first burst transfer the AHB initiates is less than or equal to the size of the configured PBL. Thus, all subsequent beats start at an address that is aligned to the configured PBL. The DMA can only align the address for beats up to size 16 (for PBL > 16), because the AHB interface does not support more than INCR16.

22.8.1.2 Host data buffer alignment

The Transmit and Receive data buffers do not have any restrictions on start address alignment. For example, in systems with 32-bit memory, the start address for the buffers can be aligned to any of the four bytes. However, the DMA always initiates transfers with address aligned to the bus width with dummy data for the byte lanes not required. This typically happens during the transfer of the beginning or end of an Ethernet frame.

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Example: Buffer read

If the Transmit buffer address is 0x00000FF2 (for 32-bit data bus), and 15 bytes need to be transferred, then the DMA reads five full words from address 0x00000FF0, but when transferring data to the MTL Transmit FIFO, the extra bytes (the first two bytes) are dropped or ignored. Similarly, the last 3 bytes of the last transfer are also ignored. The DMA always ensures it transfers a full 32-bit data to the MTL Transmit FIFO, unless it is the end-of-frame.

Example: Buffer write

If the Receive buffer address is 0x0000FF2 (for 64-bit data bus) and 16 bytes of a received frame need to be transferred, then the DMA writes 3 full words from address 0x00000FF0. But the first 2 bytes of first transfer and the last 6 bytes of the third transfer have dummy data.

22.8.1.3 Buffer size calculations

The DMA does not update the size fields in the Transmit and Receive descriptors. The DMA updates only the status fields (RDES and TDES) of the descriptors. The driver has to perform the size calculations.

The transmit DMA transfers the exact number of bytes (indicated by buffer size field of TDES1) towards the MAC core. If a descriptor is marked as first (FS bit of TDES1 is set), then the DMA marks the first transfer from the buffer as the start of frame. If a descriptor is marked as last (LS bit of TDES1), then the DMA marks the last transfer from that data buffer as the end-of frame to the MTL.

The Receive DMA transfers data to a buffer until the buffer is full or the end-of frame is received from the MTL. If a descriptor is not marked as last (LS bit of RDES0), then the descriptor's corresponding buffer(s) are full and the amount of valid data in a buffer is accurately indicated by its buffer size field minus the data buffer pointer offset when the FS bit of that descriptor is set. The offset is zero when the data buffer pointer is aligned to the data bus width. If a descriptor is marked as last, then the buffer may not be full (as indicated by the buffer size in RDES1). To compute the amount of valid data in this final buffer, the driver must read the frame length (FL bits of RDES0[29:16]) and subtract the sum of the buffer sizes of the preceding buffers in this frame. The Receive DMA always transfers the start of next frame with a new descriptor.

Remark: Even when the start address of a receive buffer is not aligned to the system bus's data width, the system should allocate a receive buffer of a size aligned to the system bus width. For example, if the system allocates a 1,024-byte (1 KB) receive buffer starting from address 0x1000, the software can program the buffer start address in the Receive descriptor to have a 0x1002 offset. The Receive DMA writes the frame to this buffer with dummy data in the first two locations (0x1000 and 0x1001). The actual frame is written from location 0x1002. Thus, the actual useful space in this buffer is 1,022 bytes, even though the buffer size is programmed as 1,024 bytes, because of the start address offset.

22.8.1.4 DMA arbiter for MAC-DMA and MAC-AHB cores

The arbiter inside the DMA module performs the arbitration between the Transmit and Receive channel accesses to the AHB Master interface. Two types of arbitrations are possible: round-robin, and fixed-priority.

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When round-robin arbitration is selected (DA bit of Register Table 421 (Bus Mode Register) is reset), the arbiter allocates the data bus in the ratio set by the PR bits of DMA Register Table 421, when both Transmit and Receive DMAs are requesting for access simultaneously. When the DA bit is set, the Receive DMA always gets priority over the Transmit DMA for data access by default. When the TXPR bit (bit 27 of DMA register Table 421) is also set, then the Transmit DMA gets priority over the Receive DMA as .

22.8.2 Transmission

22.8.2.1 TxDMA operation: Default (non-OSF) mode

The transmit DMA engine in default mode proceeds as follows:

1. The Host sets up the transmit descriptor (TDES0-TDES3) and sets the Own bit (TDES0[31]) after setting up the corresponding data buffer(s) with Ethernet Frame data.
2. Once the ST bit (DMA Register) is set, the DMA enters the Run state.
3. While in the Run state, the DMA polls the Transmit Descriptor list for frames requiring transmission. After polling starts, it continues in either sequential descriptor ring order or chained order. If the DMA detects a descriptor flagged as owned by the Host, or if an error condition occurs, transmission is suspended and both the Transmit Buffer Unavailable (DMA Register Table 427) and Normal Interrupt Summary (DMA Register Table 427) bits are set. The Transmit Engine proceeds to Step 9.
4. If the acquired descriptor is flagged as owned by DMA (TDES0[31] = 1), the DMA decodes the Transmit Data Buffer address from the acquired descriptor.
5. The DMA fetches the Transmit data from the Host memory and transfers the data to the MTL for transmission.
6. If an Ethernet frame is stored over data buffers in multiple descriptors, the DMA closes the intermediate descriptor and fetches the next descriptor. Steps 3, 4, and 5 are repeated until the end-of-Ethernet-frame data is transferred to the MTL.
7. When frame transmission is complete, if IEEE 1588 time stamping was enabled for the frame (as indicated in the transmit status) the timestamp value obtained from MTL is written to the transmit descriptor (TDES2 and TDES3) that contains the end-of-frame buffer. The status information is then written to this transmit descriptor (TDES0). Because the Own bit is cleared during this step, the Host now owns this descriptor. If time stamping was not enabled for this frame, the DMA does not alter the contents of TDES2 and TDES3.
8. Transmit Interrupt (DMA Register Table 427) is set after completing transmission of a frame that has Interrupt on Completion (TDES1[31]) set in its Last Descriptor. The DMA engine then returns to Step 3.
9. In the Suspend state, the DMA tries to re-acquire the descriptor (and thereby return to Step 3) when it receives a Transmit Poll demand and the Underflow Interrupt Status bit is cleared.

The TxDMA transmission flow in default mode is shown in Figure 47.

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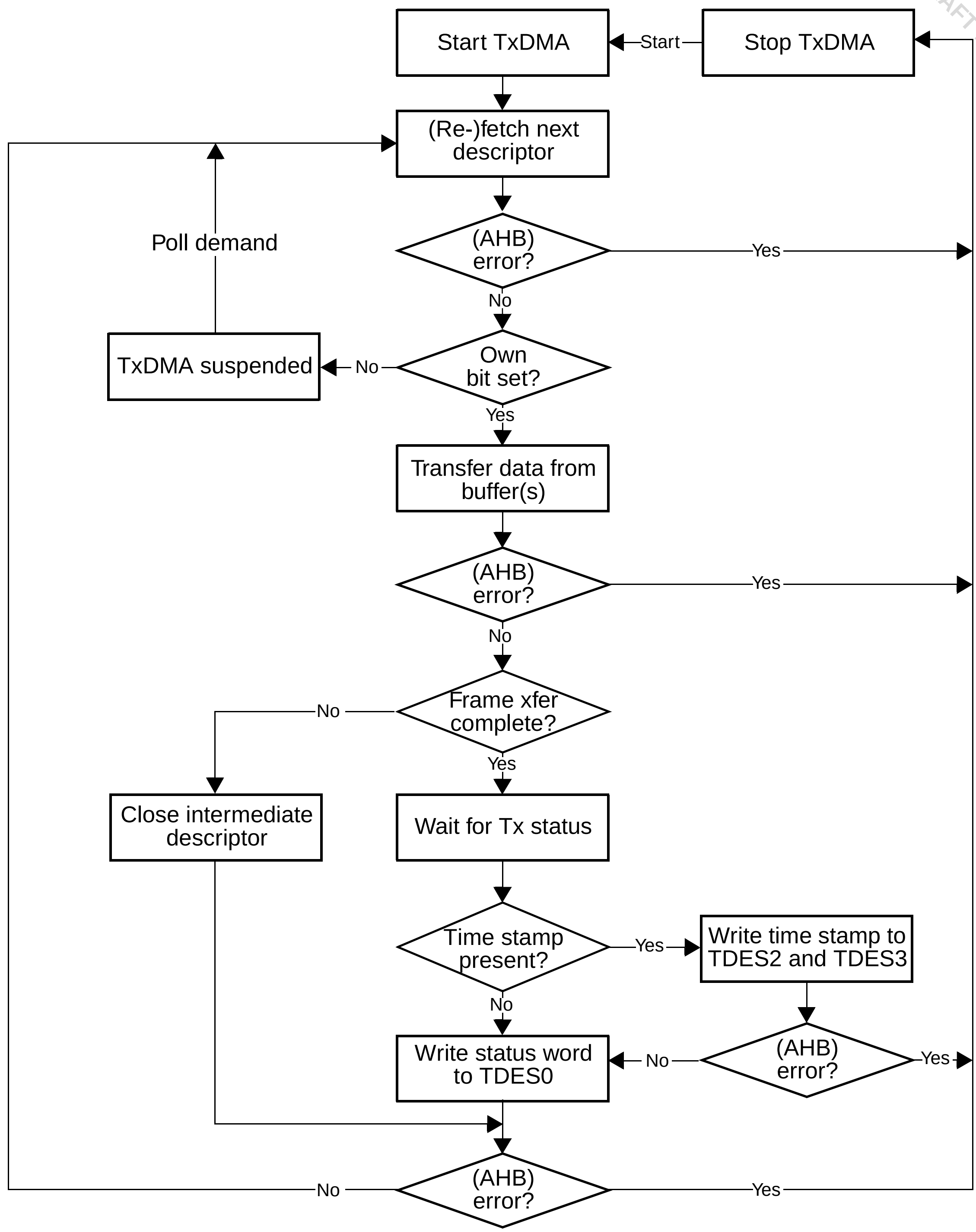


Fig 47. TxDMA operation in default mode

22.8.2.2 TxDMA operation: OSF mode

While in the Run state, the transmit process can simultaneously acquire two frames without closing the Status descriptor of the first (if the OSF bit is set in DMA Operation mode register, bit 2). As the transmit process finishes transferring the first frame, it

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immediately polls the Transmit Descriptor list for the second frame. If the second frame is valid, the transmit process transfers this frame before writing the first frame's status information.

In OSF mode, the Run state Transmit DMA operates in the following sequence:

1. The DMA operates as described in steps 1 to 6 of the TxDMA (default mode).
2. Without closing the previous frame's last descriptor, the DMA fetches the next descriptor.
3. If the DMA owns the acquired descriptor, the DMA decodes the transmit buffer address in this descriptor. If the DMA does not own the descriptor, the DMA goes into Suspend mode and skips to Step 7.
4. The DMA fetches the Transmit frame from the Host memory and transfers the frame to the MTL until the End-of-Frame data is transferred, closing the intermediate descriptors if this frame is split across multiple descriptors.
5. The DMA waits for the previous frame's frame transmission status and time stamp. Once the status is available, the DMA writes the time stamp to TDES2 and TDES3, if such time stamp was captured (as indicated by a status bit). The DMA then writes the status, with a cleared Own bit, to the corresponding TDES0, thus closing the descriptor. If time stamping was not enabled for the previous frame, the DMA does not alter the contents of TDES2 and TDES3.
6. If enabled, the Transmit interrupt is set, the DMA fetches the next descriptor, then proceeds to Step 3 (when Status is normal). If the previous transmission status shows an underflow error, the DMA goes into Suspend mode (Step 7).
7. In Suspend mode, if a pending status and time stamp are received from the MTL, the DMA writes the time stamp (if enabled for the current frame) to TDES2 and TDES3, then writes the status to the corresponding TDES0. It then sets relevant interrupts and returns to Suspend mode.
8. The DMA can exit Suspend mode and enter the Run state (go to Step 1 or Step 2 depending on pending status) only after receiving a Transmit Poll demand (DMA Transmit Poll Demand register).

Remark: As the DMA fetches the next descriptor in advance before closing the current descriptor, the descriptor chain should have more than 2 different descriptors for correct and proper operation.

The basic flow is described in Figure 48.

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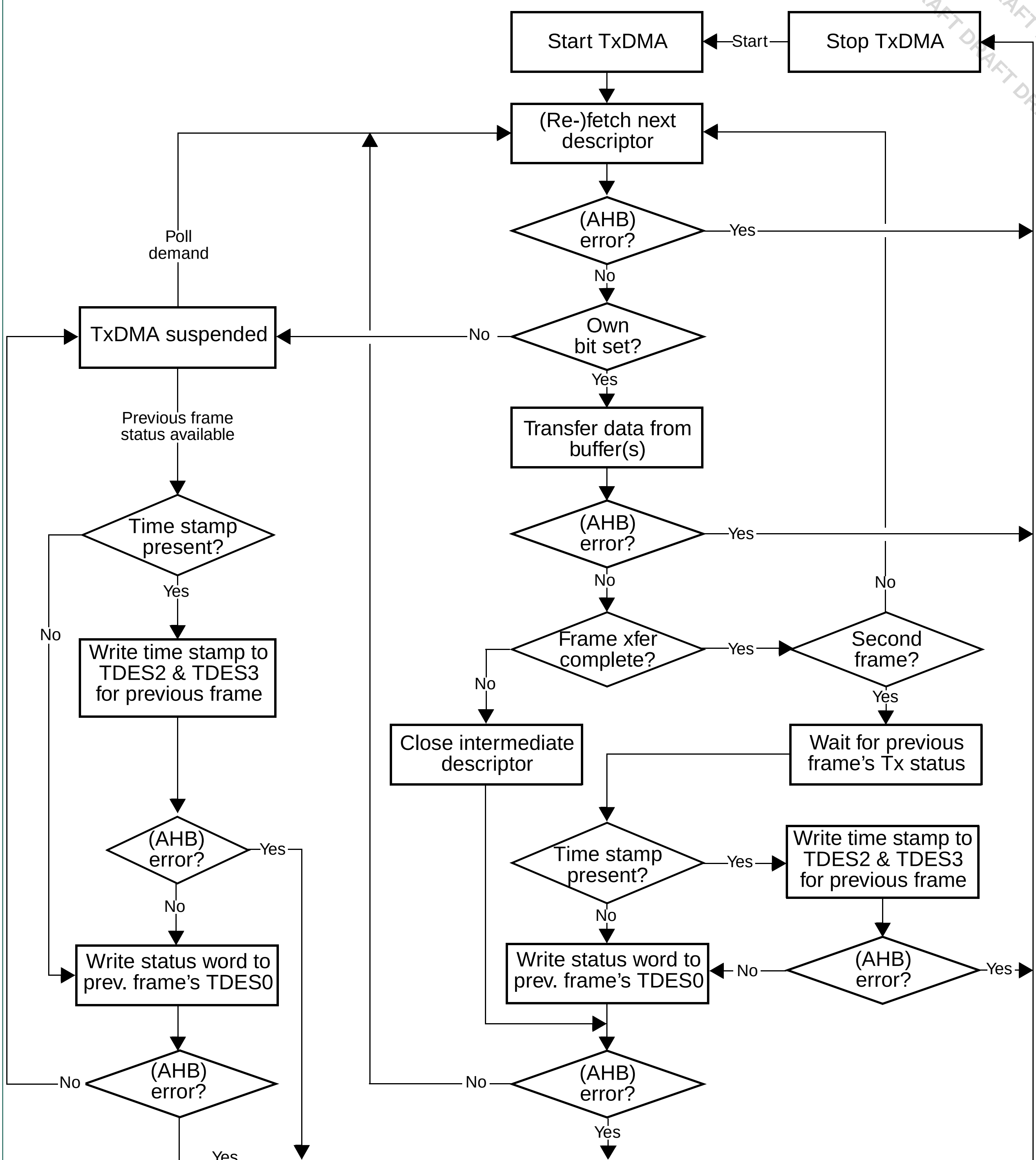


Fig 48. TxDMA operation in OSF mode

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22.8.2.3 Transmit frame processing

The Transmit DMA expects that the data buffers contain complete Ethernet frames, excluding preamble, pad bytes, and FCS fields. The DA, SA, and Type/Len fields contain valid data. If the Transmit Descriptor indicates that the MAC core must disable CRC or PAD insertion, the buffer must have complete Ethernet frames (excluding preamble), including the CRC bytes.

Frames can be data-chained and can span several buffers. Frames must be delimited by the First Descriptor (TDES1[29]) and the Last Descriptor (TDES1[30]), respectively.

As transmission starts, the First Descriptor must have (TDES1[29]) set. When this occurs, frame data transfers from the Host buffer to the MTL Transmit FIFO. Concurrently, if the current frame has the Last Descriptor (TDES1[30]) clear, the Transmit Process attempts to acquire the Next Descriptor. The Transmit Process expects this descriptor to have TDES1[29] clear. If TDES1[30] is clear, it indicates an intermediary buffer. If TDES1[30] is set, it indicates the last buffer of the frame.

After the last buffer of the frame has been transmitted, the DMA writes back the final status information to the Transmit Descriptor 0 (TDES0) word of the descriptor that has the last segment set in Transmit Descriptor 1 (TDES1[30]). At this time, if Interrupt on Completion (TDES1[31]) was set, Transmit Interrupt (DMA Status register, bit 0) is set, the Next Descriptor is fetched, and the process repeats.

The actual frame transmission begins after the MTL Transmit FIFO has reached either a programmable transmit threshold (DMA Operation Mode register, bits [16:14]), or a full frame is contained in the FIFO. There is also an option for Store and Forward Mode (DMA Operation Mode register, bit [21]). Descriptors are released (Own bit TDES0[31] clears) when the DMA finishes transferring the frame.

Remark: To ensure proper transmission of a frame and the next frame, you must specify a non-zero buffer size for the transmit descriptor that has the Last Descriptor (TDES1[30]) set.

22.8.2.4 Transmit polling suspended

Transmit polling can be suspended by either of the following conditions:

- The DMA detects a descriptor owned by the Host (TDES0[31]=0). To resume, the driver must give descriptor ownership to the DMA and then issue a Poll Demand command.
- A frame transmission is aborted when a transmit error because of underflow is detected. The appropriate Transmit Descriptor 0 (TDES0) bit is set.

If the second condition occur, both Abnormal Interrupt Summary (DMA Status register Table 427) and Transmit Underflow bits (DMA Status register Table 427) are set, and the information is written to Transmit Descriptor 0, causing the suspension. If the DMA goes into SUSPEND state because of the first condition, then both Normal Interrupt Summary (DMA Status register Table 427) and Transmit Buffer Unavailable (DMA Status register Table 427) are set.

In both cases, the position in the Transmit List is retained. The retained position is that of the descriptor following the Last Descriptor closed by the DMA.

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The driver must explicitly issue a Transmit Poll Demand command after rectifying the suspension cause.

22.8.2.5 Reception

The Receive DMA engine's reception sequence is shown in Figure 49 and proceeds as follows:

1. The host sets up Receive descriptors (RDES0-RDES3) and sets the Own bit (RDES0[31]).
2. Once the SR (DMA Operation Mode register Table 428) bit is set, the DMA enters the Run state. While in the Run state, the DMA polls the Receive Descriptor list, attempting to acquire free descriptors. If the fetched descriptor is not free (is owned by the host), the DMA enters the Suspend state and jumps to Step 9.
3. The DMA decodes the receive data buffer address from the acquired descriptors.
4. Incoming frames are processed and placed in the acquired descriptor's data buffers.
5. When the buffer is full or the frame transfer is complete, the Receive engine fetches the next descriptor.
6. If the current frame transfer is complete, the DMA proceeds to Step 7. If the DMA does not own the next fetched descriptor and the frame transfer is not complete (EOF is not yet transferred), the DMA sets the Descriptor Error bit in the RDES0 (unless flushing is disabled). The DMA closes the current descriptor (clears the Own bit) and marks it as intermediate by clearing the Last Segment (LS) bit in the RDES0 value (marks it as Last Descriptor if flushing is not disabled), then proceeds to Step 8. If the DMA does own the next descriptor but the current frame transfer is not complete, the DMA closes the current descriptor as intermediate and reverts to Step 4.
7. If IEEE 1588 time stamping is enabled, the DMA writes the timestamp (if available) to the current descriptor's RDES2 and RDES3. It then takes the receive frame's status from the MTL and writes the status word to the current descriptor's RDES0, with the Own bit cleared and the Last Segment bit set.
8. The Receive engine checks the latest descriptor's Own bit. If the host owns the descriptor (Own bit is 0) the Receive Buffer Unavailable bit (DMA Status register Table 427) is set and the DMA Receive engine enters the Suspended state (Step 9). If the DMA owns the descriptor, the engine returns to Step 4 and awaits the next frame.
9. Before the Receive engine enters the Suspend state, partial frames are flushed from the Receive FIFO (You can control flushing using Bit 24 of DMA Operation MOde register Table 428).
10. The Receive DMA exits the Suspend state when a Receive Poll demand is given or the start of next frame is available from the MTL's Receive FIFO. The engine proceeds to Step 2 and refetches the next descriptor.

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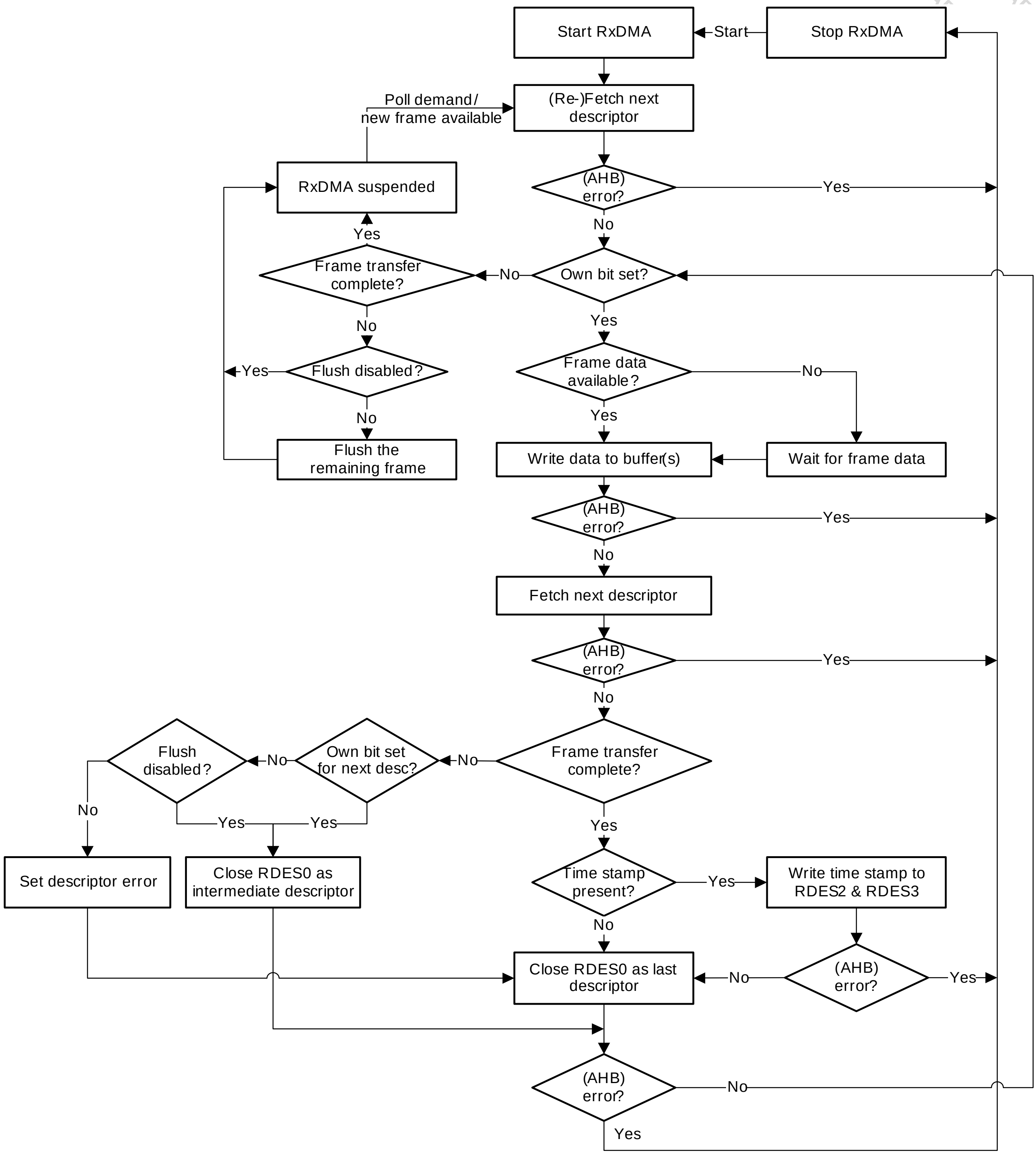


Fig 49. Receive DMA operation

The DMA does not acknowledge accepting the status from the MTL until it has completed the time stamp write-back and is ready to perform status write-back to the descriptor.

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If software has enabled time stamping through CSR, when a valid time stamp value is not available for the frame (for example, because the receive FIFO was full before the time stamp could be written to it), the DMA writes all-ones to RDES2 and RDES3. Otherwise (that is, if time stamping is not enabled), the RDES2 and RDES3 remain unchanged.

22.8.2.6 Receive descriptor acquisition

The Receive Engine always attempts to acquire an extra descriptor in anticipation of an incoming frame. Descriptor acquisition is attempted if any of the following conditions is satisfied:

- The receive Start/Stop bit (DMA Operation Mode register Table 428) has been set immediately after being placed in the Run state.
- The data buffer of current descriptor is full before the frame ends for the current transfer.
- The controller has completed frame reception, but the current Receive Descriptor is not yet closed.
- The receive process has been suspended because of a host-owned buffer (RDES0[31] = 0) and a new frame is received.
- A Receive poll demand has been issued.

22.8.2.7 Receive frame processing

The MAC transfers the received frames to the Host memory only when the frame passes the address filter and frame size is greater than or equal to configurable threshold bytes set for the Receive FIFO of MTL, or when the complete frame is written to the FIFO in Store-and-Forward mode.

If the frame fails the address filtering, it is dropped in the MAC block itself (unless Receive All bit 3 is set in the MAC Frame Filter register; Table 404). Frames that are shorter than 64 bytes, because of collision or premature termination, can be purged from the MTL Receive FIFO.

After 64 (configurable threshold) bytes have been received, the MTL block requests the DMA block to begin transferring the frame data to the Receive Buffer pointed to by the current descriptor. The DMA sets First Descriptor (RDES0[9]) after the DMA Host Interface (AHB or MDC) becomes ready to receive a data transfer (if DMA is not fetching transmit data from the host), to delimit the frame. The descriptors are released when the Own (RDES[31]) bit is reset to 0, either as the Data buffer fills up or as the last segment of the frame is transferred to the Receive buffer. If the frame is contained in a single descriptor, both Last Descriptor (RDES[8]) and First Descriptor (RDES[9]) are set.

The DMA fetches the next descriptor, sets the Last Descriptor (RDES[8]) bit, and releases the RDES0 status bits in the previous frame descriptor. Then the DMA sets Receive Interrupt (Register 5[6]). The same process repeats unless the DMA encounters a descriptor flagged as being owned by the host. If this occurs, the Receive Process sets Receive Buffer Unavailable (DMA Status register Table 427) and then enters the Suspend state. The position in the receive list is retained.

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22.8.2.8 Receive process suspended

If a new Receive frame arrives while the Receive Process is in Suspend state, the DMA refetches the current descriptor in the Host memory. If the descriptor is now owned by the DMA, the Receive Process re-enters the Run state and starts frame reception. If the descriptor is still owned by the host, by default, the DMA discards the current frame at the top of the MTL Rx FIFO and increments the missed frame counter. If more than one frame is stored in the MTL Rx FIFO, the process repeats.

The discarding or flushing of the frame at the top of the MTL Rx FIFO can be avoided by setting Operation Mode register bit 24 (DFF) in Table 428. In such conditions, the receive process sets the Receive Buffer Unavailable status and returns to the Suspend state.

22.8.2.9 Interrupts

Interrupts can be generated as a result of various events. The DMA Status register (Table 427) contains all the bits that might cause an interrupt. Table 429 contains an enable bit for each of the events that can cause an interrupt.

There are two groups of interrupts, Normal and Abnormal, as described in DMA Status register (Table 427). Interrupts are cleared by writing a 1 to the corresponding bit position. When all the enabled interrupts within a group are cleared, the corresponding summary bit is cleared. When both the summary bits are cleared, the interrupt signal is de-asserted. If the MAC core is the cause for assertion of the interrupt, then any of the GLI, GMI, or GPI bits of DMA Status register (Table 427) are set HIGH.

Remark: The DMA Status register (Table 427) is the (interrupt) status register. The interrupt pin is asserted because of any event in this status register only if the corresponding interrupt enable bit is set in DMA Interrupt Enable Register (Table 429).

Interrupts are not queued and if the interrupt event occurs before the driver has responded to it, no additional interrupts are generated. For example, the Receive Interrupt (bit 6 of the DMA Status Register (Table 427) indicates that one or more frames were transferred to the Host buffer. The driver must scan all descriptors, from the last recorded position to the first one owned by the DMA.

An interrupt is generated only once for simultaneous, multiple events. The driver must scan the DMA Status register (Table 427) for the cause of the interrupt. The interrupt is not generated again unless a new interrupting event occurs, after the driver has cleared the appropriate bit in DMA Status register. For example, the controller generates a DMA Receive interrupt (bit 6 of the DMA Status register), and the driver begins reading DMA Status register . Next, Receive Buffer Unavailable (bit 7 of DMA Status register (Status Register)) occurs. The driver clears the Receive interrupt. Even then, the sbd_intr_o signal is not de-asserted, because of the active or pending Receive Buffer Unavailable interrupt.

An interrupt timer RIWT (bits 7:0 in Receive Interrupt Watchdog Timer Register (Table 431)) is given for flexible control of Receive Interrupt. When this Interrupt timer is programmed with a non-zero value, it gets activated as soon as the RxDMA completes a transfer of a received frame to system memory without asserting the Receive Interrupt because it is not enabled in the corresponding Receive Descriptor (RDES1[31]. When this timer runs out as per the programmed value, RI bit is set and the interrupt is asserted if

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the corresponding RI is enabled in DMA Interrupt Enable register (Table 429). This timer gets disabled before it runs out, when a frame is transferred to memory and the RI is set because it is enabled for that descriptor.

22.8.2.10 Error response to DMA

For any data transfer initiated by a DMA channel, if the slave replies with an error response, that DMA stops all operations and updates the error bits and the Fatal Bus Error bit in the DMA Status register (Table 427). That DMA controller can resume operation only after soft resetting or hard resetting the core and re-initializing the DMA. This DMA behavior is true for non-AHB interfaced DMAs that receive an error response.

22.9 Ethernet descriptors (enhanced format)

The enhanced descriptor structure supports up to 8 DWORDS (32 bytes) and the IEEE 1588-2008 Advanced Timestamp feature or the AV feature. The features of the enhanced descriptor structure are:

- Enhanced descriptor size can be 4 DWORDS (16 bytes) or 8 DWORDS (32 bytes) depending on the setting of the ATDS bit in the DMA Bus Mode register (Table 421).
- Support buffers of up to 8 KB (useful for Jumbo frames).
- The transmit descriptor stores the timestamp in TDES6 and TDES7 when you select the Advanced Timestamp.
- This receive descriptor structure is also used for storing the extended status (RDES4) and timestamp (RDES6 and RDES7) when advanced timestamp feature or IPC full offload is selected.
- When the enhanced descriptor mode is selected, and the Timestamp feature is enabled, the software needs to allocate 32-bytes (8 DWORDS) of memory for every descriptor. When Timestamping or Receive IPC FullOffload engine are not enabled, the extended descriptors are not required and the SW can use alternate descriptors with the default size of 16 bytes. The core also needs to be configured for this change using the bit 7 (ATDS: Alternate Descriptor Size) of DMA Bus Mode register (Table 421).
- When an enhanced descriptor is chosen without Timestamp or Full IPC Offload feature, the descriptor size is always 4 DWORDs (DES0-DES3).

The description or bit-mapping alternate descriptor structure (in little-endian mode) is given below.

22.9.1 Transmit descriptor

The transmit descriptor structure is shown in Figure 50. The application software must program the control bits TDES0[31:20] during descriptor initialization. When the DMA updates the descriptor, it write backs all the control bits except the OWN bit (which it clears) and updates the status bits[19:0]. The contents of the transmitter descriptor word 0 (TDES0) through word 3 (TDES3) are given in Table 437 through Table 440, respectively.

With the advance timestamp support, the snapshot of the timestamp to be taken can be enabled for a given frame by setting bit TTSE: Transmit Timestamp Enable. (bit-25 of TDES0). When the descriptor is closed (i.e. when the OWN bit is cleared), the time-stamp

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is written into TDES6 and TDES7. This is indicated by the status bit TTSS: Transmit Timestamp Status. (bit-17 of TDES0). This is shown in Figure 50. The contents of TDES6 and TDES7 are mentioned in Table 441 to Table 442.

When either Advanced Timestamp or IPC Offload (Type 2) features is enabled, the SW should set the DMA Bus Mode register[7], so that the DMA operates with extended descriptor size. When this control bit is reset, the TDES4-TDES7 descriptor space are not valid.

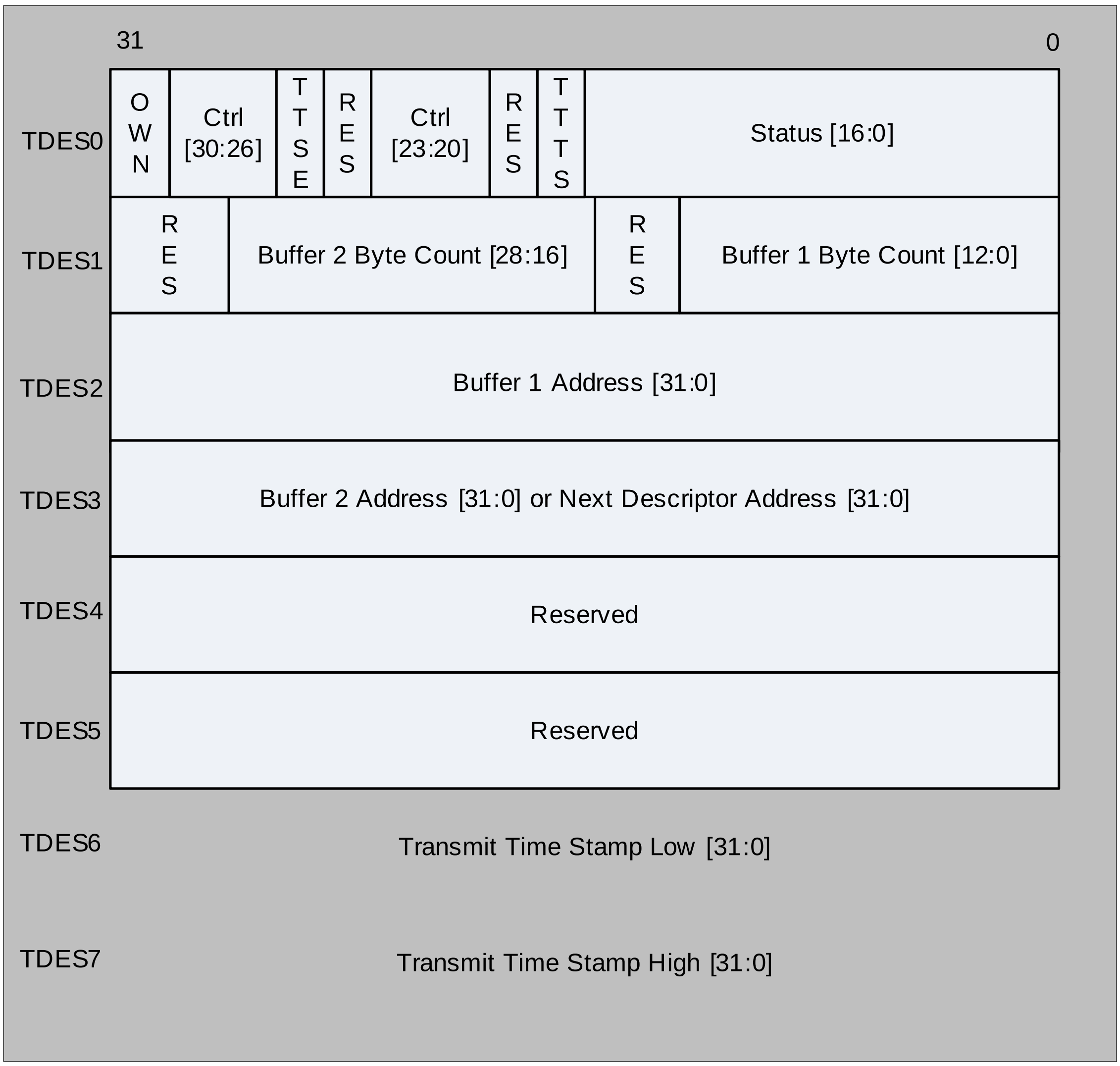


Fig 50. Transmitter descriptor fields - enhanced format

The DMA always reads or fetches four DWORDS of the descriptor from system memory to obtain the buffer and control information as shown in Figure 51. When Advanced timestamp feature support is enabled, TDES0 has additional control bits[6:3] for channel 1 and channel 2. For channel 0, the bits 6:3 are ignored. The bits 6:3 are described in Table 437.

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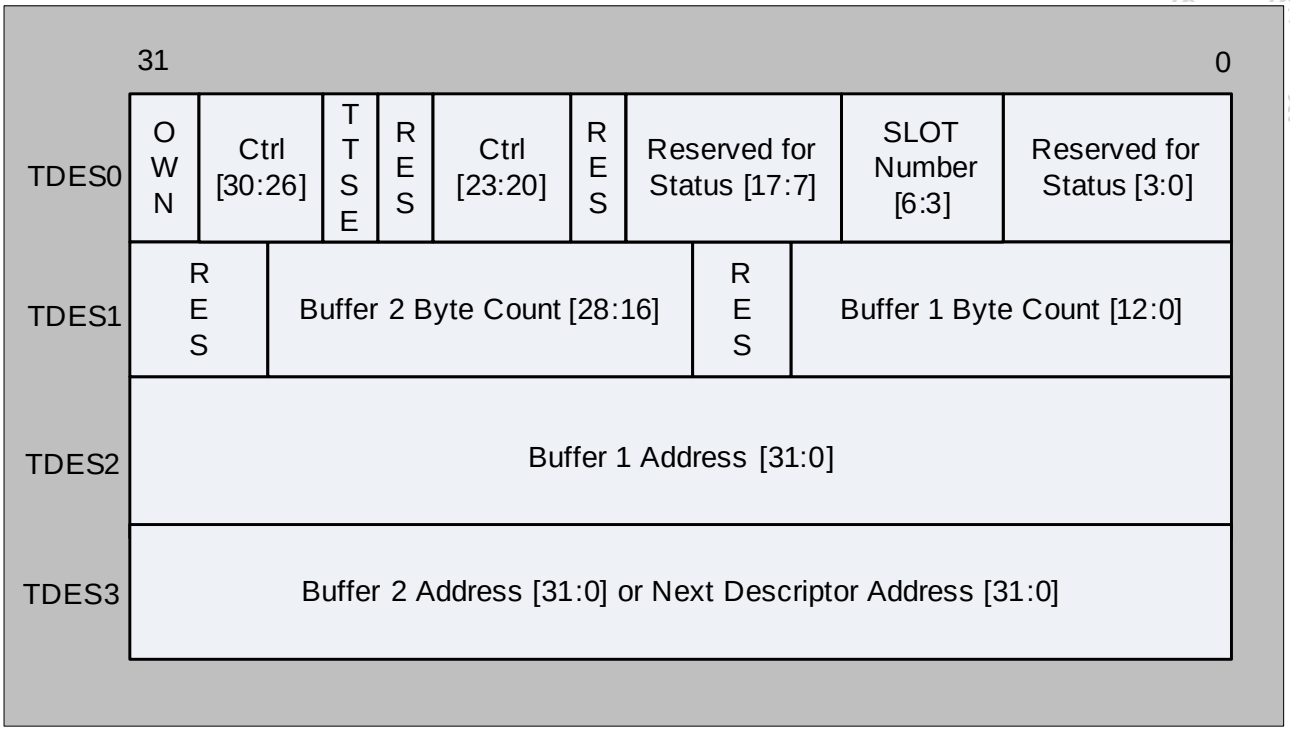


Fig 51. Transmit descriptor fetch (read) for enhanced format

Table 437. Transmit descriptor word 0 (TDES0)

Bit	Symbol	Description
0	DB	Deferred Bit When set, this bit indicates that the MAC defers before transmission because of the presence of carrier. This bit is valid only in Half-Duplex mode.
1	UF	Underflow Error When set, this bit indicates that the MAC aborted the frame because data arrived late from the Host memory. Underflow Error indicates that the DMA encountered an empty transmit buffer while transmitting the frame. The transmission process enters the Suspended state and sets both Transmit Underflow (Register 5[5]) and Transmit Interrupt (Register 5[0]).
2	ED	Excessive Deferral When set, this bit indicates that the transmission has ended because of excessive deferral of over 24,288 bit times (155,680 bits times in 1,000-Mbps mode or if Jumbo Frame is enabled) if the Deferral Check (DC) bit in the MAC Control register is set high.

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Table 437. Transmit descriptor word 0 (TDES0)

Bit	Symbol	Description
6:3	CC/ SLOTNUM	CC: Collision Count (Status field) These status bits indicate the number of collisions that occurred before the frame was transmitted. This count is not valid when the Excessive Collisions bit (TDES0[8]) is set. The core updates this status field only in the half-duplex mode. SLOTNUM: Slot Number Control Bits in AV Mode These bits indicate the slot interval in which the data should be fetched from the corresponding buffers addressed by TDES2 or TDES3. When the transmit descriptor is fetched, the DMA compares the slot number value in this field with the slot interval maintained in the core (Register 11xx). It fetches the data from the buffers only if there is a match in values. These bits are valid only for the AV channels (not channel 0).
7	VF	VLAN Frame When set, this bit indicates that the transmitted frame was a VLAN-type frame.
8	EC	Excessive Collision When set, this bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current frame. If the DR (Disable Retry) bit in the MAC Configuration register is set, this bit is set after the first collision, and the transmission of the frame is aborted.
9	LC	Late Collision When set, this bit indicates that frame transmission was aborted due to a collision occurring after the collision window (64 byte-times, including preamble, in MII mode and 512 byte-times, including preamble and carrier extension, in MII mode). This bit is not valid if the Underflow Error bit is set.
10	NC	No Carrier When set, this bit indicates that the Carrier Sense signal form the PHY was not asserted during transmission.
11	LC	Loss of Carrier When set, this bit indicates that a loss of carrier occurred during frame transmission (that is, the gmii_crs_i signal was inactive for one or more transmit clock periods during frame transmission). This is valid only for the frames transmitted without collision when the MAC operates in Half-Duplex mode.
12	IPE	IP Payload Error When set, this bit indicates that MAC transmitter detected an error in the TCP, UDP, or ICMP IP datagram payload. The transmitter checks the payload length received in the IPv4 or IPv6 header against the actual number of TCP, UDP, or ICMP packet bytes received from the application and issues an error status in case of a mismatch.
13	FF	Frame Flushed When set, this bit indicates that the DMA/MTL flushed the frame due to a software Flush command given by the CPU.
14	JT	Jabber Timeout When set, this bit indicates the MAC transmitter has experienced a jabber time-out. This bit is only set when the MAC configuration register's JD bit is not set.

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Table 437. Transmit descriptor word 0 (TDES0)

Bit	Symbol	Description
15	ES	Error Summary Indicates the logical OR of the following bits: • TDES0[14]: Jabber Timeout • TDES0[13]: Frame Flush • TDES0[11]: Loss of Carrier • TDES0[10]: No Carrier • TDES0[9]: Late Collision • TDES0[8]: Excessive Collision • TDES0[2]: Excessive Deferral • TDES0[1]: Underflow Error • TDES0[16]: IP Header Error • TDES0[12]: IP Payload Error
16	IHE	IP Header Error When set, this bit indicates that the MAC transmitter detected an error in the IP datagram header. The transmitter checks the header length in the IPv4 packet against the number of header bytes received from the application and indicates an error status if there is a mismatch. For IPv6 frames, a header error is reported if the main header length is not 40 bytes. Furthermore, the Ethernet Length/Type field value for an IPv4 or IPv6 frame must match the IP header version received with the packet. For IPv4 frames, an error status is also indicated if the Header Length field has a value less than 0x5.
17	TTSS	Transmit Timestamp Status This field is used as a status bit to indicate that a timestamp was captured for the described transmit frame. When this bit is set, TDES2 and TDES3 have a timestamp value captured for the transmit frame. This field is only valid when the descriptor’s Last Segment control bit (TDES0[29]) is set.
19:18	-	Reserved
20	TCH	Second Address Chained When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When TDES0[20] is set, TBS2 (TDES1[28:16]) is a “don’t care” value. TDES0[21] takes precedence over TDES0[20].
21	TER	Transmit End of Ring When set, this bit indicates that the descriptor list reached its final descriptor. The DMA returns to the base address of the list, creating a descriptor ring.
23:22	CIC	Checksum Insertion Control These bits control the checksum calculation and insertion. Bit encodings are as shown below. • 00: Checksum Insertion Disabled. • 01: Only IP header checksum calculation and insertion are enabled. • 10: IP header checksum and payload checksum calculation and insertion are enabled, but pseudo-header checksum is not calculated in hardware. • 11: IP Header checksum and payload checksum calculation and insertion are enabled, and pseudo-header checksum is calculated in hardware. This field is reserved when the IPC_FULL_OFFLOAD configuration parameter is not selected.
24	-	Reserved
25	TTSE	Transmit Timestamp Enable When set, this bit enables IEEE1588 hardware time stamping for the transmit frame referenced by the descriptor. This field is valid only when the First Segment control bit (TDES0[28]) is set.

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Table 437. Transmit descriptor word 0 (TDES0)

Bit	Symbol	Description
26	DP	Disable Pad When set, the MAC does not automatically add padding to a frame shorter than 64 bytes. When this bit is reset, the DMA automatically adds padding and CRC to a frame shorter than 64 bytes, and the CRC field is added despite the state of the DC (TDES0[27]) bit. This is valid only when the first segment (TDES0[28]) is set.
27	DC	Disable CRC When this bit is set, the MAC does not append a cyclic redundancy check (CRC) to the end of the transmitted frame. This is valid only when the first segment (TDES0[28]) is set.
28	FS	First Segment When set, this bit indicates that the buffer contains the first segment of a frame.
29	LS	Last Segment When set, this bit indicates that the buffer contains the last segment of the frame. When this bit is set, the TBS1: Transmit Buffer 1 Size or TBS2: Transmit Buffer 2 Size field in TDES1 should have a non-zero value.
30	IC	Interrupt on Completion When set, this bit sets the Transmit Interrupt (Register 5[0]) after the present frame has been transmitted.
31	OWN	Own Bit When set, this bit indicates that the descriptor is owned by the DMA. When this bit is reset, it indicates that the descriptor is owned by the Host. The DMA clears this bit either when it completes the frame transmission or when the buffers allocated in the descriptor are read completely. The ownership bit of the frame’s first descriptor must be set after all subsequent descriptors belonging to the same frame have been set. This avoids a possible race condition between fetching a descriptor and the driver setting an ownership bit.

Table 438. Transmit descriptor word 1 (TDES1)

Bit	Symbol	Description
12:0	TBS1	Transmit buffer 1 size These bits indicate the first data buffer byte size, in bytes. If this field is 0, the DMA ignores this buffer and uses Buffer 2 or the next descriptor, depending on the value of TCH (TDES0[20]).
15:13	-	Reserved
28:16	TBS2	These bits indicate the second data buffer size in bytes. This field is not valid if TDES0[20] is set. See Section 22.8.1.3.
31:29	-	Reserved

Table 439. Transmit descriptor word 2 (TDES2)

Bit	Symbol	Description
31:0	B1ADD	Buffer 1 Address Pointer These bits indicate the physical address of Buffer 1. There is no limitation on the buffer address alignment. See Section 22.8.1.2 for further detail on buffer address alignment.

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Table 440. Transmit descriptor word 3 (TDES3)

Bit	Symbol	Description
31:0	B2ADD	Buffer 2 Address Pointer (Next Descriptor Address) Indicates the physical address of Buffer 2 when a descriptor ring structure is used. If the Second Address Chained (TDES1[24]) bit is set, this address contains the pointer to the physical memory where the Next Descriptor is present. The buffer address pointer must be aligned to the bus width only when TDES1[24] is set. (LSBs are ignored internally.)

Table 441. Transmit descriptor word 6 (TDES6)

Bit	Symbol	Description
31:0	TTSL	Transmit Frame Timestamp Low This field is updated by DMA with the least significant 32 bits of the timestamp captured for the corresponding transmit frame. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and Timestamp status (TTSS) bit is set.

Table 442. Transmit descriptor word 7 (TDES7)

Bit	Symbol	Description
31:0	TTSH	Transmit Frame Timestamp High This field is updated by DMA with the most significant 32 bits of the timestamp captured for the corresponding receive frame. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and Timestamp status (TTSS) bit is set.

22.9.2 Receive descriptor

The structure of the received descriptor is shown in Figure 52. This can have 32 bytes of descriptor data (8 DWORDs) when Advanced Timestamp or IPC Full Offload feature is selected.

Remark: When either of these features is enabled, the SW should set the DMA Bus Mode register[7] so that the DMA operates with extended descriptor size. When this control bit is reset, RDES0[7] and RDES0[0] is always cleared and the RDES4-RDES7 descriptor space are not valid.

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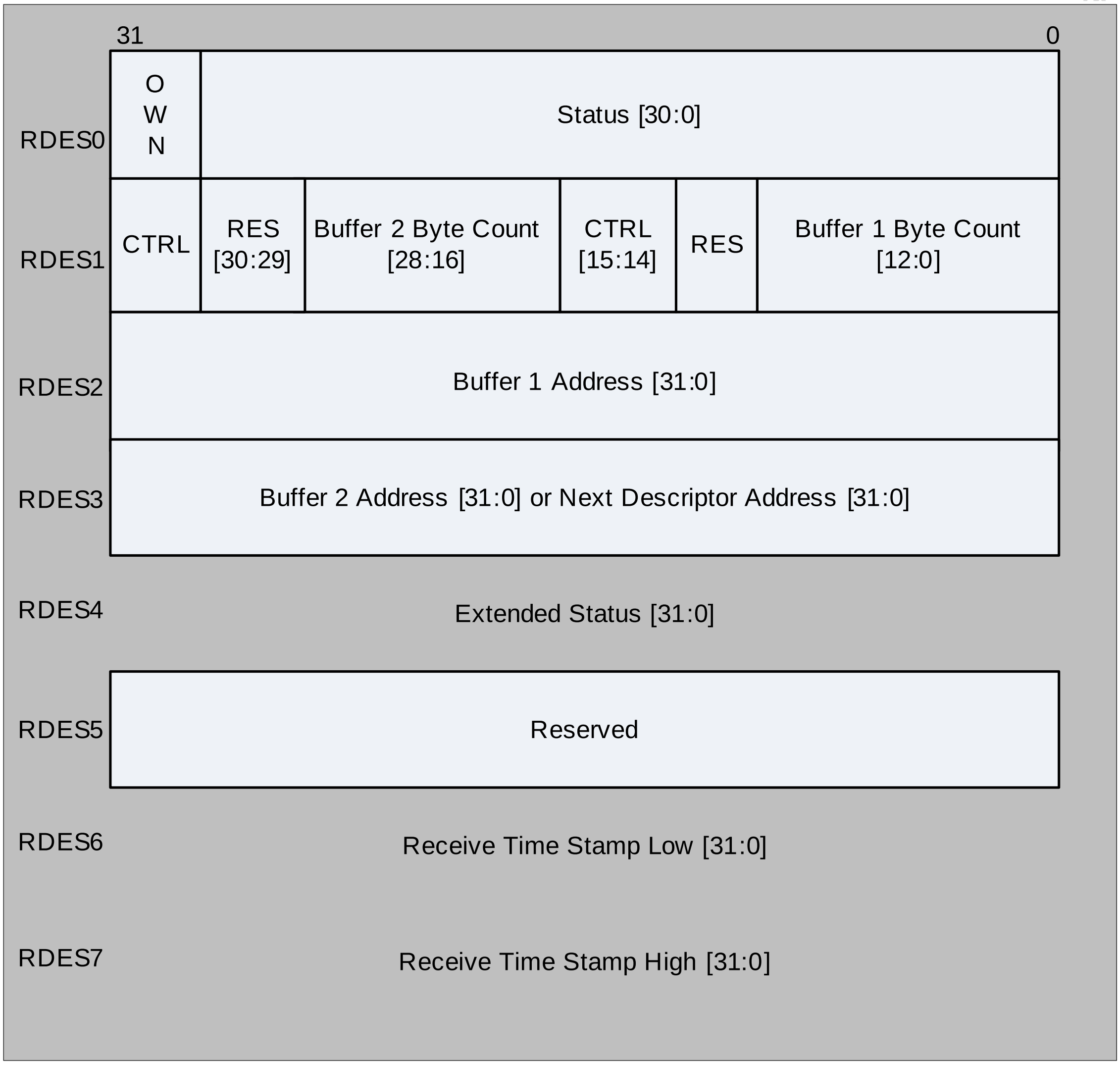


Fig 52. Receive descriptor fields - alternate (enhanced format)

The contents of RDES0 are identified in Table 443. The contents of RDES1 through RDES3 are identified in Table 444 to Table 446.

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Table 443. Receive descriptor fields 0 (RDES0)

Bit	Symbol	Description
0	ESA	Extended Status Available/Rx MAC Address When either Advanced Timestamp or IP Checksum Offload (Type 2) is present, this bit, when set, indicates that the extended status is available in descriptor word 4 (RDES4). This is valid only when the Last Descriptor bit (RDES0[8]) is set. When Advance Timestamp Feature or IPC Full Offload is not selected, this bit indicates Rx MAC Address status. When set, this bit indicates that the Rx MAC Address registers value (1 to 31) matched the frame's DA field. When reset, this bit indicates that the Rx MAC Address Register 0 value matched the DA field.
1	CE	CRC Error When set, this bit indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received frame. This field is valid only when the Last Descriptor (RDES0[8]) is set.
2	DE	Dribble Bit Error When set, this bit indicates that the received frame has a non-integer multiple of bytes (odd nibbles). This bit is valid only in MII Mode.
3	RE	Receive Error When set, this bit indicates that the gmii_rxer_i signal is asserted while gmii_rxdv_i is asserted during frame reception. This error also includes carrier extension error in MII and Half-duplex mode. Error can be of less/no extension, or error (rxd $\neq$ 0f) during extension.
4	RWT	Receive Watchdog Timeout When set, this bit indicates that the Receive Watchdog Timer has expired while receiving the current frame and the current frame is truncated after the Watchdog Timeout.
5	FT	Frame Type When set, this bit indicates that the Receive Frame is an Ethernet-type frame (the LT field is greater than or equal to 0x0600). When this bit is reset, it indicates that the received frame is an IEEE802.3 frame. This bit is not valid for Runt frames less than 14 bytes.
6	LC	Late Collision When set, this bit indicates that a late collision has occurred while receiving the frame in Half-Duplex mode.
7	TSA	Timestamp Available/IP Checksum Error (Type1) /Giant Frame When Advanced Timestamp feature is present, when set, this bit indicates that a snapshot of the Timestamp is written in descriptor words 6 (RDES6) and 7 (RDES7). This is valid only when the Last Descriptor bit (RDES0[8]) is set. When IP Checksum Engine (Type 1) is selected, this bit, when set, indicates that the 16-bit IPv4 Header checksum calculated by the core did not match the received checksum bytes. Otherwise, this bit, when set, indicates the Giant Frame Status. Giant frames are larger-than-1,518-byte (or 1,522-byte for VLAN) normal frames and larger-than-9,018-byte (9,022-byte for VLAN) frame when Jumbo Frame processing is enabled.
8	LS	Last Descriptor When set, this bit indicates that the buffers pointed to by this descriptor are the last buffers of the frame
9	FS	First Descriptor When set, this bit indicates that this descriptor contains the first buffer of the frame. If the size of the first buffer is 0, the second buffer contains the beginning of the frame. If the size of the second buffer is also 0, the next Descriptor contains the beginning of the frame.

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Table 443. Receive descriptor fields 0 (RDES0)

Bit	Symbol	Description
10	VLAN	VLAN Tag When set, this bit indicates that the frame pointed to by this descriptor is a VLAN frame tagged by the MAC Core.
11	OE	Overflow Error When set, this bit indicates that the received frame was damaged due to buffer overflow in MTL.
12	LE	Length Error When set, this bit indicates that the actual length of the frame received and that the Length/ Type field does not match. This bit is valid only when the Frame Type (RDES0[5]) bit is reset.
13	SAF	Source Address Filter Fail When set, this bit indicates that the SA field of frame failed the SA Filter in the MAC Core.
14	DE	Descriptor Error When set, this bit indicates a frame truncation caused by a frame that does not fit within the current descriptor buffers, and that the DMA does not own the Next Descriptor. The frame is truncated. This field is valid only when the Last Descriptor (RDES0[8]) is set.
15	ES	ES: Error Summary Indicates the logical OR of the following bits: • RDES0[1]: CRC Error • RDES0[3]: Receive Error • RDES0[4]: Watchdog Timeout • RDES0[6]: Late Collision • RDES0[7]: Giant Frame • RDES4[4:3]: IP Header/Payload Error • RDES0[11]: Overflow Error • RDES0[14]: Descriptor Error This field is valid only when the Last Descriptor (RDES0[8]) is set.
29:16	FL	Frame Length These bits indicate the byte length of the received frame that was transferred to host memory (including CRC). This field is valid when Last Descriptor (RDES0[8]) is set and either the Descriptor Error (RDES0[14]) or Overflow Error bits are reset. The frame length also includes the two bytes appended to the Ethernet frame when IP checksum calculation (Type 1) is enabled and the received frame is not a MAC control frame. This field is valid when Last Descriptor (RDES0[8]) is set. When the Last Descriptor and Error Summary bits are not set, this field indicates the accumulated number of bytes that have been transferred for the current frame.
30	AFM	Destination Address Filter Fail When set, this bit indicates a frame that failed in the DA Filter in the MAC Core.
31	OWN	Own Bit When set, this bit indicates that the descriptor is owned by the DMA of the MAC Subsystem. When this bit is reset, this bit indicates that the descriptor is owned by the Host. The DMA clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.

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Table 444. Receive descriptor fields 1 (RDES1)

Bit	Symbol	Description
12:0	RBS1	Receive Buffer 1 Size Indicates the first data buffer size in bytes. The buffer size must be a multiple of 4, 8, or 16, depending upon the bus widths (32, 64, or 128), even if the value of RDES2 (buffer1 address pointer) is not aligned. When the buffer size is not a multiple of 4, 8, or 16, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and uses Buffer 2 or next descriptor depending on the value of RCH (Bit 14). See Section 22.8.1.3 for further details on calculating buffer sizes.
13	-	Reserved
14	RCH	Second Address Chained When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When this bit is set, RBS2 (RDES1[28:16]) is a “don’t care” value. RDES1[15] takes precedence over RDES1[14].
15	RER	Receive End of Ring When set, this bit indicates that the descriptor list reached its final descriptor. The DMA returns to the base address of the list, creating a descriptor ring.
28:16	RBS2	Receive Buffer 2 Size These bits indicate the second data buffer size, in bytes. The buffer size must be a multiple of 4, 8, or 16, depending on the bus widths (32, 64, or 128, respectively), even if the value of RDES3 (buffer2 address pointer) is not aligned to bus width. If the buffer size is not an appropriate multiple of 4, 8, or 16, the resulting behavior is undefined. This field is not valid if RDES1[14] is set. See Section 22.8.1.3 for further details on calculating buffer sizes.

Table 445. Receive descriptor fields 2 (RDES2)

Bit	Symbol	Description
31:0	B1ADD	Address Pointer These bits indicate the physical address of Buffer 1. There are no limitations on the buffer address alignment except for the following condition: The DMA uses the configured value for its address generation when the RDES2 value is used to store the start of frame. Note that the DMA performs a write operation with the RDES2[3/2/1:0] bits as 0 during the transfer of the start of frame but the frame data is shifted as per the actual Buffer address pointer. The DMA ignores RDES2[3/2/1:0] (corresponding to bus width of 128/64/32) if the address pointer is to a buffer where the middle or last part of the frame is stored. See Section 22.8.1.2for further details on buffer address alignment.

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Table 446. Receive descriptor fields 3 (RDES3)

Bit	Symbol	Description
31:0	B2ADD	Buffer 2 Address Pointer (Next Descriptor Address) These bits indicate the physical address of Buffer 2 when a descriptor ring structure is used. If the Second Address Chained (RDES1[24]) bit is set, this address contains the pointer to the physical memory where the Next Descriptor is present. If RDES1[24] is set, the buffer (Next Descriptor) address pointer must be bus width-aligned (RDES3[3, 2, or 1:0] = 0, corresponding to a bus width of 128, 64, or 32. LSBs are ignored internally.) However, when RDES1[24] is reset, there are no limitations on the RDES3 value, except for the following condition: The DMA uses the configured value for its buffer address generation when the RDES3 value is used to store the start of frame. The DMA ignores RDES3 [3, 2, or 1:0] (corresponding to a bus width of 128, 64, or 32) if the address pointer is to a buffer where the middle or last part of the frame is stored.

The extended status written is as shown in Table 447. The extended status is written only when there is status related to IPC or timestamp available. The availability of extended status is indicated by bit-0 of RDES0. This status is available only when Advance Timestamp or IPC Full Offload feature is selected.

Table 447. Receive descriptor fields 4 (RDES4)

Bit	Symbol	Description
2:0	IPPL	IP Payload Type These bits indicate the type of payload encapsulated in the IP datagram processed by the Receive Checksum Offload Engine (COE). The COE also sets these bits to 00 if it does not process the IP datagram's payload due to an IP header error or fragmented IP. • 000: Unknown or did not process IP payload • 001: UDP • 010: TCP • 011: ICMP • 1xx: Reserved
3	IPHE	IP Header Error When set, this bit indicates either that the 16-bit IPv4 header checksum calculated by the core does not match the received checksum bytes, or that the IP datagram version is not consistent with the Ethernet Type value.
4	IPPLE	IP Payload Error When set, this bit indicates that the 16-bit IP payload checksum (that is, the TCP, UDP, or ICMP checksum) that the core calculated does not match the corresponding checksum field in the received segment. It is also set when the TCP, UDP, or ICMP segment length does not match the payload length value in the IP Header field.
5	IPCSB	IP Checksum Bypassed When set, this bit indicates that the checksum offload engine is bypassed.

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Table 447. Receive descriptor fields 4 (RDES4)

Bit	Symbol	Description
6	IPv4	IPv4 Packet Received When set, this bit indicates that the received packet is an IPv4 packet.
7	IPv6	IPv6 Packet Received When set, this bit indicates that the received packet is an IPv6 packet.
11:8	MT	Message Type These bits are encoded to give the type of the message received. • 0000: No PTP message received • 0001: SYNC (all clock types) • 0010: Follow_Up (all clock types) • 0011: Delay_Req (all clock types) • 0100: Delay_Resp (all clock types) • 0101: Pdelay_Req (in peer-to-peer transparent clock) • 0110: Pdelay_Resp (in peer-to-peer transparent clock) • 0111: Pdelay_Resp_Follow_Up (in peer-to-peer transparent clock) • 1000: Announce • 1001: Management • 1010: Signaling • 1011-1110: Reserved • 1111: PTP packet with Reserved message type These bits are valid only when you select the Advance Timestamp feature.

RDES6 and RDES7 contain the snapshot of the time-stamp. The availability of the snapshot of the time-stamp in RDES6 and RDES7 is indicated by bit-7 in the RDES0 descriptor. The contents of RDES6 and RDES7 are identified in Table 448 and Table 449.

Table 448. Receive descriptor fields 6 (RDES6)

Bit	Symbol	Description
31:0	RTSL	Receive Frame Timestamp Low This field is updated by DMA with the least significant 32 bits of the timestamp captured for the corresponding receive frame. This field is updated by DMA only for the last descriptor of the receive frame which is indicated by Last Descriptor status bit (RDES0[8]).

Table 449. Receive descriptor fields 7 (RDES7)

Bit	Symbol	Description
31:0	RTSH	Receive Frame Timestamp High This field is updated by DMA with the most significant 32 bits of the timestamp captured for the corresponding receive frame. This field is updated by DMA only for the last descriptor of the receive frame which is indicated by Last Descriptor status bit (RDES0[8]).

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23.1 How to read this chapter

The LCD controller is available on part LPC1850.

23.2 Basic configuration

The LCD controller is configured as follows:

- See Table 450 for clocking and power control.
- The LCD is reset by the LCD_RST (reset # 16).
- The LCD interrupt is connected to interrupt slot # 7 in the NVIC.

Table 450. LCD clocking and power control

	Base clock	Branch clock	Maximum frequency	Notes
LCD register interface clock	BASE_M3_CLK	CLK_M3_LCD	150 MHz	-

23.3 Features

- AHB bus master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4 or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320x200, 320x240, 640x200, 640x240, 640x480, 800x600, and 1024x768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized, for color STN and TFT.
- 24 bpp true-color non-palettized, for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128x32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.

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- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

23.4 General description

23.4.1 Programmable parameters

The following key display and controller parameters can be programmed:

- Horizontal front and back porch
- Horizontal synchronization pulse width
- Number of pixels per line
- Vertical front and back porch
- Vertical synchronization pulse width
- Number of lines per panel
- Number of pixel clocks per line
- Hardware cursor control.
- Signal polarity, active HIGH or LOW
- AC panel bias
- Panel clock frequency
- Bits-per-pixel
- Display type: STN monochrome, STN color, or TFT
- STN 4 or 8-bit interface mode
- STN dual or single panel mode
- Little-endian, big-endian, or Windows CE mode
- Interrupt generation event

23.4.2 Hardware cursor support

The hardware cursor feature reduces software overhead associated with maintaining a cursor image in the LCD frame buffer.

Without this feature, software needed to:

- Save an image of the area under the next cursor position.
- Update the area with the cursor image.
- Repair the last cursor position with a previously saved image.

In addition, the LCD driver had to check whether the graphics operation had overwritten the cursor, and correct it. With a cursor size of 64x64 and 24-bit color, each cursor move involved reading and writing approximately 75 kB of data.

The hardware cursor removes the requirement for this management by providing a completely separate image buffer for the cursor, and superimposing the cursor image on the LCD output stream at the current cursor (X,Y) coordinate.

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To move the hardware cursor, the software driver supplies a new cursor coordinate. The frame buffer requires no modification. This significantly reduces software overhead.

The cursor image is held in the LCD controller in an internal 256x32-bit buffer memory.

23.4.3 Types of LCD panels supported

The LCD controller supports the following types of LCD panel:

- Active matrix TFT panels with up to 24-bit bus interface.
- Single-panel monochrome STN panels (4-bit and 8-bit bus interface).
- Dual-panel monochrome STN panels (4-bit and 8-bit bus interface per panel).
- Single-panel color STN panels, 8-bit bus interface.
- Dual-panel color STN panels, 8-bit bus interface per panel.

23.4.3.1 TFT panels

TFT panels support one or more of the following color modes:

- 1 bpp, palettized, 2 colors selected from available colors.
- 2 bpp, palettized, 4 colors selected from available colors.
- 4 bpp, palettized, 16 colors selected from available colors.
- 8 bpp, palettized, 256 colors selected from available colors.
- 12 bpp, direct 4:4:4 RGB.
- 16 bpp, direct 5:5:5 RGB, with 1 bpp not normally used. This pixel is still output, and can be used as a brightness bit to connect to the Least Significant Bit (LSB) of RGB components of a 6:6:6 TFT panel.
- 16 bpp, direct 5:6:5 RGB.
- 24 bpp, direct 8:8:8 RGB, providing over 16 million colors.

Each 16-bit palette entry is composed of 5 bpp (RGB), plus a common intensity bit. This provides better memory utilization and performance compared with a full 6 bpp structure. The total number of colors supported can be doubled from 32K to 64K if the intensity bit is used and applied to all three color components simultaneously.

Alternatively, the 16 signals can be used to drive a 5:6:5 panel with the extra bit only applied to the green channel.

23.4.3.2 Color STN panels

Color STN panels support one or more of the following color modes:

- 1 bpp, palettized, 2 colors selected from 3375.
- 2 bpp, palettized, 4 colors selected from 3375.
- 4 bpp, palettized, 16 colors selected from 3375.
- 8 bpp, palettized, 256 colors selected from 3375.
- 16 bpp, direct 4:4:4 RGB, with 4 bpp not being used.

23.4.3.3 Monochrome STN panels

Monochrome STN panels support one or more of the following modes:

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- 1 bpp, palettized, 2 gray scales selected from 15.
- 2 bpp, palettized, 4 gray scales selected from 15.
- 4 bpp, palettized, 16 gray scales selected from 15.

More than 4 bpp for monochrome panels can be programmed, but using these modes has no benefit because the maximum number of gray scales supported on the display is 15.

23.5 Pin description

The largest configuration for the LCD controller uses 31 pins. There are many variants using as few as 10 pins for a monochrome STN panel. Pins are allocated in groups based on the selected configuration. All LCD functions are shared with other chip functions. In Table 451, only the LCD related portion of the pin name is shown.

Table 451. LCD controller pins

Pin name	Type	Function
LCDPWR	Output	LCD panel power enable.
LCDCLK	Output	LCD panel clock.
LCDENAB/LCDM (LCDAC)	Output	STN AC bias drive or TFT data enable output.
LCDFP	Output	Frame pulse (STN). Vertical synchronization pulse (TFT)
LCDLE	Output	Line end signal
LCDLP	Output	Line synchronization pulse (STN). Horizontal synchronization pulse (TFT)
LCDVD[23:0]	Output	LCD panel data. Bits used depend on the panel configuration.
GP_CLKIN	Input	General purpose CGU input clock. Can be used as the LCD external clock LCDCLKIN.

23.5.1 Signal usage

The signals that are used for various display types are identified in the following sections.

23.5.1.1 Signals used for single panel STN displays

The signals used for single panel STN displays are shown in Table 452. UD refers to upper panel data.

Table 452. Pins used for single panel STN displays

Pin name	4-bit Monochrome (10 pins)	8-bit Monochrome (14 pins)	Color (14 pins)
LCDPWR	Y	Y	Y
LCDDCLK	Y	Y	Y
LCDENAB/ LCDM	Y	Y	Y
LCDFP	Y	Y	Y
LCDLE	Y	Y	Y
LCDLP	Y	Y	Y

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Table 452. Pins used for single panel STN displays

Pin name	4-bit Monochrome (10 pins)	8-bit Monochrome (14 pins)	Color (14 pins)
LCDVD[3:0]	UD[3:0]	UD[3:0]	UD[3:0]
LCDVD[7:4]	-	UD[7:4]	UD[7:4]
LCDVD[23:8]	-	-	-

23.5.1.2 Signals used for dual panel STN displays

The signals used for dual panel STN displays are shown in Table 453. UD refers to upper panel data, and LD refers to lower panel data.

Table 453. Pins used for dual panel STN displays

Pin name	4-bit Monochrome (14 pins)	8-bit Monochrome (22 pins)	Color (22 pins)
LCDPWR	Y	Y	Y
LCDDCLK	Y	Y	Y
LCDENAB/ LCDM	Y	Y	Y
LCDFP	Y	Y	Y
LCDLE	Y	Y	Y
LCDLP	Y	Y	Y
LCDVD[3:0]	UD[3:0]	UD[3:0]	UD[3:0]
LCDVD[7:4]	-	UD[7:4]	UD[7:4]
LCDVD[11:8]	LD[3:0]	LD[3:0]	LD[3:0]
LCDVD[15:12]	-	LD[7:4]	LD[7:4]
LCDVD[23:16]	-	-	-

23.5.1.3 Signals used for TFT displays

The signals used for TFT displays are shown in Table 454.

Table 454. Pins used for TFT displays

Pin name	12-bit, 4:4:4 mode (18 pins)	16-bit, 5:6:5 mode (22 pins)	16-bit, 1:5:5:5 mode (24 pins)	24-bit (30 pins)
LCDPWR	Y	Y	Y	Y
LCDDCLK	Y	Y	Y	Y
LCDENAB/ LCDM	Y	Y	Y	Y
LCDFP	Y	Y	Y	Y
LCDLE	Y	Y	Y	Y
LCDLP	Y	Y	Y	Y
LCDVD[1:0]	-	-	-	RED[1:0]
LCDVD[2]	-	-	Intensity	RED[2]
LCDVD[3]	-	RED[0]	RED[0]	RED[3]
LCDVD[7:4]	RED[3:0]	RED[4:1]	RED[4:1]	RED[7:4]
LCDVD[9:8]	-	-	-	GREEN[1:0]
LCDVD[10]	-	GREEN[0]	Intensity	GREEN[2]

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Table 454. Pins used for TFT displays

Pin name	12-bit, 4:4:4 mode (18 pins)	16-bit, 5:6:5 mode (22 pins)	16-bit, 1:5:5:5 mode (24 pins)	24-bit (30 pins)
LCDVD[11]	-	GREEN[1]	GREEN[0]	GREEN[3]
LCDVD[15:12]	GREEN[3:0]	GREEN[5:2]	GREEN[4:1]	GREEN[7:4]
LCDVD[17:16]	-	-	-	BLUE[1:0]
LCDVD[18]	-	-	Intensity	BLUE[2]
LCDVD[19]	-	BLUE[0]	BLUE[0]	BLUE[3]
LCDVD[23:20]	BLUE[3:0]	BLUE[4:1]	BLUE[4:1]	BLUE[7:4]

23.6 Register description

Table 455 shows the registers associated with the LCD controller and a summary of their functions. Following the table are details for each register.

Table 455. Register overview: LCD controller (base address: 0x4000 8000)

Name	Access	Address offset	Description	Reset value [1]
TIMH	R/W	0x000	Horizontal Timing Control register	0x0
TIMV	R/W	0x004	Vertical Timing Control register	0x0
POL	R/W	0x008	Clock and Signal Polarity Control register	0x0
LE	R/W	0x00C	Line End Control register	0x0
UPBASE	R/W	0x010	Upper Panel Frame Base Address register	0x0
LPBASE	R/W	0x014	Lower Panel Frame Base Address register	0x0
CTRL	R/W	0x018	LCD Control register	0x0
INTMSK	R/W	0x01C	Interrupt Mask register	0x0
INTRAW	RO	0x020	Raw Interrupt Status register	0x0
INTSTAT	RO	0x024	Masked Interrupt Status register	0x0
INTCLR	WO	0x028	Interrupt Clear register	0x0
UPCURR	RO	0x02C	Upper Panel Current Address Value register	0x0
LPCURR	RO	0x030	Lower Panel Current Address Value register	0x0
-	-	0x034 to 0x1FC	Reserved	-
PAL	R/W	0x200 to 0x3FC	256x16-bit Color Palette registers	0x0
-	-	0x400 to 0x7FC	Reserved	-
CRSR_IMG	R/W	0x800 to 0xBFC	Cursor Image registers	0x0
CRSR_CTRL	R/W	0xC00	Cursor Control register	0x0
CRSR_CFG	R/W	0xC04	Cursor Configuration register	0x0
CRSR_PAL0	R/W	0xC08	Cursor Palette register 0	0x0
CRSR_PAL1	R/W	0xC0C	Cursor Palette register 1	0x0
CRSR_XY	R/W	0xC10	Cursor XY Position register	0x0
CRSR_CLIP	R/W	0xC14	Cursor Clip Position register	0x0
CRSR_INTMSK	R/W	0xC20	Cursor Interrupt Mask register	0x0

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Table 455. Register overview: LCD controller (base address: 0x4000 8000) *…continued*

Name	Access	Address offset	Description	Reset value [1]
CRSR_INTCLR	WO	0xC24	Cursor Interrupt Clear register	0x0
CRSR_INTRAW	RO	0xC28	Cursor Raw Interrupt Status register	0x0
CRSR_INTSTAT	RO	0xC2C	Cursor Masked Interrupt Status register	0x0

[1] Reset Value reflects the data stored in used bits only. It does not include reserved bits content.

23.6.1 Horizontal Timing register

The TIMH register controls the Horizontal Synchronization pulse Width (HSW), the Horizontal Front Porch (HFP) period, the Horizontal Back Porch (HBP) period, and the Pixels-Per-Line (PPL).

Table 456. Horizontal Timing register (TIMH, address 0x4000 8000) bit description

Bits	Symbol	Description	Reset value
1:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
7:2	PPL	Pixels-per-line. The PPL bit field specifies the number of pixels in each line or row of the screen. PPL is a 6-bit value that represents between 16 and 1024 pixels per line. PPL counts the number of pixel clocks that occur before the HFP is applied. Program the value required divided by 16, minus 1. Actual pixels-per-line = 16 * (PPL + 1). For example, to obtain 320 pixels per line, program PPL as (320/16) -1 = 19.	0x0
15:8	HSW	Horizontal synchronization pulse width. The 8-bit HSW field specifies the pulse width of the line clock in passive mode, or the horizontal synchronization pulse in active mode. Program with desired value minus 1.	0x0
23:16	HFP	Horizontal front porch. The 8-bit HFP field sets the number of pixel clock intervals at the end of each line or row of pixels, before the LCD line clock is pulsed. When a complete line of pixels is transmitted to the LCD driver, the value in HFP counts the number of pixel clocks to wait before asserting the line clock. HFP can generate a period of 1-256 pixel clock cycles. Program with desired value minus 1.	0x0
31:24	HBP	Horizontal back porch. The 8-bit HBP field is used to specify the number of pixel clock periods inserted at the beginning of each line or row of pixels. After the line clock for the previous line has been deasserted, the value in HBP counts the number of pixel clocks to wait before starting the next display line. HBP can generate a delay of 1-256 pixel clock cycles. Program with desired value minus 1.	0x0

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23.6.1.1 Horizontal timing restrictions

DMA requests new data at the start of a horizontal display line. Some time must be allowed for the DMA transfer and for data to propagate down the FIFO path in the LCD interface. The data path latency forces some restrictions on the usable minimum values for horizontal porch width in STN mode. The minimum values are HSW = 2 and HBP = 2.

Single panel mode:

- HSW = 3 pixel clock cycles
- HBP = 5 pixel clock cycles
- HFP = 5 pixel clock cycles
- Panel Clock Divisor (PCD) = 1 (LCDCLK / 3)

Dual panel mode:

- HSW = 3 pixel clock cycles
- HBP = 5 pixel clock cycles
- HFP = 5 pixel clock cycles
- PCD = 5 (LCDCLK / 7)

If enough time is given at the start of the line, for example, setting HSW = 6, HBP = 10, data does not corrupt for PCD = 4, the minimum value.

23.6.2 Vertical Timing register

The TIMV register controls the Vertical Synchronization pulse Width (VSW), the Vertical Front Porch (VFP) period, the Vertical Back Porch (VBP) period, and the Lines-Per-Panel (LPP).

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Table 457. Vertical Timing register (TIMV, address 0x4000 8004) bit description

Bits	Symbol	Description	Reset value
9:0	LPP	Lines per panel. This is the number of active lines per screen. The LPP field specifies the total number of lines or rows on the LCD panel being controlled. LPP is a 10-bit value allowing between 1 and 1024 lines. Program the register with the number of lines per LCD panel, minus 1. For dual panel displays, program the register with the number of lines on each of the upper and lower panels.	0x0
15:10	VSW	Vertical synchronization pulse width. This is the number of horizontal synchronization lines. The 6-bit VSW field specifies the pulse width of the vertical synchronization pulse. Program the register with the number of lines required, minus one. The number of horizontal synchronization lines must be small (for example, program to zero) for passive STN LCDs. The higher the value the worse the contrast on STN LCDs.	0x0
23:16	VFP	Vertical front porch. This is the number of inactive lines at the end of a frame, before the vertical synchronization period. The 8-bit VFP field specifies the number of line clocks to insert at the end of each frame. When a complete frame of pixels is transmitted to the LCD display, the value in VFP is used to count the number of line clock periods to wait. After the count has elapsed, the vertical synchronization signal, LCDFP, is asserted in active mode, or extra line clocks are inserted as specified by the VSW bit-field in passive mode. VFP generates 0–255 line clock cycles. Program to zero on passive displays for improved contrast.	0x0
31:24	VBP	Vertical back porch. This is the number of inactive lines at the start of a frame, after the vertical synchronization period. The 8-bit VBP field specifies the number of line clocks inserted at the beginning of each frame. The VBP count starts immediately after the vertical synchronization signal for the previous frame has been negated for active mode, or the extra line clocks have been inserted as specified by the VSW bit field in passive mode. After this has occurred, the count value in VBP sets the number of line clock periods inserted before the next frame. VBP generates 0–255 extra line clock cycles. Program to zero on passive displays for improved contrast.	0x0

23.6.3 Clock and Signal Polarity register

The POL register controls various details of clock timing and signal polarity.

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Table 458. Clock and Signal Polarity register (POL, address 0x4000 8008) bit description

Bits	Symbol	Description	Reset value
4:0	PCD_LO	Lower five bits of panel clock divisor. The ten-bit PCD field, comprising PCD_HI (bits 31:27 of this register) and PCD_LO, is used to derive the LCD panel clock frequency LCDDCLK from the input clock, LCDDCLK = LCDCLK/(PCD+2). For monochrome STN displays with a 4 or 8-bit interface, the panel clock is a factor of four and eight down from the actual individual pixel clock rate. For color STN displays, 22/3 pixels are output per LCDDCLK cycle, so the panel clock is 0.375 times the pixel rate. For TFT displays, the pixel clock divider can be bypassed by setting the BCD bit in this register. **Note:** data path latency forces some restrictions on the usable minimum values for the panel clock divider in STN modes: Single panel color mode, PCD = 1 (LCDDCLK = LCDCLK/3). Dual panel color mode, PCD = 4 (LCDDCLK = LCDCLK/6). Single panel monochrome 4-bit interface mode, PCD = 2(LCDDCLK = LCDCLK/4). Dual panel monochrome 4-bit interface mode and single panel monochrome 8-bit interface mode, PCD = 6(LCDDCLK = LCDCLK/8). Dual panel monochrome 8-bit interface mode, PCD = 14(LCDDCLK = LCDCLK/16).	0x0
5	CLKSEL	Clock Select. This bit controls the selection of the source for LCDCLK. 0 = the clock source for the LCD block is CCLK. 1 = the clock source for the LCD block is LCDCLKIN (external clock input for the LVD).	0x0
10:6	ACB	AC bias pin frequency. The AC bias pin frequency is only applicable to STN displays. These require the pixel voltage polarity to periodically reverse to prevent damage caused by DC charge accumulation. Program this field with the required value minus one to apply the number of line clocks between each toggle of the AC bias pin, LCDENAB. This field has no effect if the LCD is operating in TFT mode, when the LCDENAB pin is used as a data enable signal.	0x0
11	IVS	Invert vertical synchronization. The IVS bit inverts the polarity of the LCDFP signal. 0 = LCDFP pin is active HIGH and inactive LOW. 1 = LCDFP pin is active LOW and inactive HIGH.	0x0
12	IHS	Invert horizontal synchronization. The IHS bit inverts the polarity of the LCDLP signal. 0 = LCDLP pin is active HIGH and inactive LOW. 1 = LCDLP pin is active LOW and inactive HIGH.	0x0

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Table 458. Clock and Signal Polarity register (POL, address 0x4000 8008) bit description

Bits	Symbol	Description	Reset value
13	IPC	Invert panel clock. The IPC bit selects the edge of the panel clock on which pixel data is driven out onto the LCD data lines. 0 = Data is driven on the LCD data lines on the rising edge of LCDDCLK. 1 = Data is driven on the LCD data lines on the falling edge of LCDDCLK.	0x0
14	IOE	Invert output enable. This bit selects the active polarity of the output enable signal in TFT mode. In this mode, the LCDENAB pin is used as an enable that indicates to the LCD panel when valid display data is available. In active display mode, data is driven onto the LCD data lines at the programmed edge of LCDDCLK when LCDENAB is in its active state. 0 = LCDENAB output pin is active HIGH in TFT mode. 1 = LCDENAB output pin is active LOW in TFT mode.	0x0
15	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
25:16	CPL	Clocks per line. This field specifies the number of actual LCDDCLK clocks to the LCD panel on each line. This is the number of PPL divided by either 1 (for TFT), 4 or 8 (for monochrome passive), 2 2/3 (for color passive), minus one. This must be correctly programmed in addition to the PPL bit in the TIMH register for the LCD display to work correctly.	0x0
26	BCD	Bypass pixel clock divider. Setting this to 1 bypasses the pixel clock divider logic. This is mainly used for TFT displays.	0x0
31:27	PCD_HI	Upper five bits of panel clock divisor. See description for PCD_LO, in bits [4:0] of this register.	0x0

23.6.4 Line End Control register

The LE register controls the enabling of line-end signal LCDLE. When enabled, a positive pulse, four LCDCLK periods wide, is output on LCDLE after a programmable delay, LED, from the last pixel of each display line. If the line-end signal is disabled it is held permanently LOW.

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Table 459. Line End Control register (LE, address 0x4000 800C) bit description

Bits	Symbol	Description	Reset value
6:0	LED	Line-end delay. Controls Line-end signal delay from the rising-edge of the last panel clock, LCDDCLK. Program with number of LCDCLK clock periods minus 1.	0x0
15:7	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
16	LEE	LCD Line end enable. 0 = LCDLE disabled (held LOW). 1 = LCDLE signal active.	0x0
31:17	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

23.6.5 Upper Panel Frame Base Address register

The UPBASE register is the color LCD upper panel DMA base address register, and is used to program the base address of the frame buffer for the upper panel. LCDUPBase (and LCDLPBase for dual panels) must be initialized before enabling the LCD controller. The base address must be doubleword aligned.

Optionally, the value may be changed mid-frame to create double-buffered video displays. These registers are copied to the corresponding current registers at each LCD vertical synchronization. This event causes the LNBU bit and an optional interrupt to be generated. The interrupt can be used to reprogram the base address when generating double-buffered video.

Table 460. Upper Panel Frame Base register (UPBASE, address 0x4000 8010) bit description

Bits	Symbol	Description	Reset value
2:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
31:3	LCDUPBASE	LCD upper panel base address. This is the start address of the upper panel frame data in memory and is doubleword aligned.	0x0

23.6.6 Lower Panel Frame Base Address register

The LPBASE register is the color LCD lower panel DMA base address register, and is used to program the base address of the frame buffer for the lower panel. LCDLPBase must be initialized before enabling the LCD controller. The base address must be doubleword aligned.

Optionally, the value may be changed mid-frame to create double-buffered video displays. These registers are copied to the corresponding current registers at each LCD vertical synchronization. This event causes the LNBU bit and an optional interrupt to be generated. The interrupt can be used to reprogram the base address when generating double-buffered video.

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Table 461. Lower Panel Frame Base register (LPBASE, address 0x4000 8014) bit description

Bits	Symbol	Description	Reset value
2:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
31:3	LCDLPBASE	LCD lower panel base address. This is the start address of the lower panel frame data in memory and is doubleword aligned.	0x0

23.6.7 LCD Control register

The CTRL register controls the LCD operating mode and the panel pixel parameters.

Table 462. LCD Control register (CTRL, address 0x4000 8018) bit description

Bits	Symbol	Description	Reset value
0	LCDEN	LCD enable control bit. 0 = LCD disabled. Signals LCDLP, LCDDCLK, LCDFP, LCDENAB, and LCDLE are low. 1 = LCD enabled. Signals LCDLP, LCDDCLK, LCDFP, LCDENAB, and LCDLE are high. See LCD power-up and power-down sequence for details on LCD power sequencing.	0x0
3:1	LCDBPP	LCD bits per pixel: Selects the number of bits per LCD pixel: 000 = 1 bpp. 001 = 2 bpp. 010 = 4 bpp. 011 = 8 bpp. 100 = 16 bpp. 101 = 24 bpp (TFT panel only). 110 = 16 bpp, 5:6:5 mode. 111 = 12 bpp, 4:4:4 mode.	0x0
4	LCDBW	STN LCD monochrome/color selection. 0 = STN LCD is color. 1 = STN LCD is monochrome. This bit has no meaning in TFT mode.	0x0
5	LCDTFT	LCD panel TFT type selection. 0 = LCD is an STN display. Use gray scaler. 1 = LCD is a TFT display. Do not use gray scaler.	0x0
6	LCDMONO8	Monochrome LCD interface width. This bit controls whether a monochrome STN LCD uses a 4 or 8-bit parallel interface. It has no meaning in other modes and must be programmed to zero. 0 = monochrome LCD uses a 4-bit interface. 1 = monochrome LCD uses a 8-bit interface.	0x0

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Table 462. LCD Control register (CTRL, address 0x4000 8018) bit description *…continued*

Bits	Symbol	Description	Reset value
7	LCDDUAL	Single or Dual LCD panel selection. STN LCD interface is: 0 = single-panel. 1 = dual-panel.	0x0
8	BGR	Color format selection. 0 = RGB: normal output. 1 = BGR: red and blue swapped.	0x0
9	BEBO	Big-endian Byte Order. Controls byte ordering in memory: 0 = little-endian byte order. 1 = big-endian byte order.	0x0
10	BEPO	Big-Endian Pixel Ordering. Controls pixel ordering within a byte: 0 = little-endian ordering within a byte. 1 = big-endian pixel ordering within a byte. The BEPO bit selects between little and big-endian pixel packing for 1, 2, and 4 bpp display modes, it has no effect on 8 or 16 bpp pixel formats. See Pixel serializer for more information on the data format.	0x0
11	LCDPWR	LCD power enable. 0 = power not gated through to LCD panel and LCDV[23:0] signals disabled, (held LOW). 1 = power gated through to LCD panel and LCDV[23:0] signals enabled, (active). See LCD power-up and power-down sequence for details on LCD power sequencing.	0x0
13:12	LCDVCOMP	LCD Vertical Compare Interrupt. Generate VComp interrupt at: 00 = start of vertical synchronization. 01 = start of back porch. 10 = start of active video. 11 = start of front porch.	0x0
15:14	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
16	WATERMARK	LCD DMA FIFO watermark level. Controls when DMA requests are generated: 0 = An LCD DMA request is generated when either of the DMA FIFOs have four or more empty locations. 1 = An LCD DMA request is generated when either of the DMA FIFOs have eight or more empty locations.	0x0
31:17	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

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23.6.8 Interrupt Mask register

The INTMSK register controls whether various LCD interrupts occur.Setting bits in this register enables the corresponding raw interrupt INTRAW status bit values to be passed to the INTSTAT register for processing as interrupts.

Table 463. Interrupt Mask register (INTMSK, address 0x4000 801C) bit description

Bits	Function	Description	Reset value
0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
1	FUFIM	FIFO underflow interrupt enable. 0: The FIFO underflow interrupt is disabled. 1: Interrupt will be generated when the FIFO underflows.	0x0
2	LNBUIM	LCD next base address update interrupt enable. 0: The base address update interrupt is disabled. 1: Interrupt will be generated when the LCD base address registers have been updated from the next address registers.	0x0
3	VCOMPIM	Vertical compare interrupt enable. 0: The vertical compare time interrupt is disabled. 1: Interrupt will be generated when the vertical compare time (as defined by LcdVComp field in the CTRL register) is reached.	0x0
4	BERIM	AHB master error interrupt enable. 0: The AHB Master error interrupt is disabled. 1: Interrupt will be generated when an AHB Master error occurs.	0x0
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

23.6.9 Raw Interrupt Status register

The INTRAW register contains status flags for various LCD controller events. These flags can generate an interrupts if enabled by mask bits in the INTMSK register.

Table 464. Raw Interrupt Status register (INTRAW, address 0x4000 8020) bit description

Bits	Function	Description	Reset value
0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
1	FUFRIS	FIFO underflow raw interrupt status. Set when either the upper or lower DMA FIFOs have been read accessed when empty causing an underflow condition to occur. Generates an interrupt if the FUFIM bit in the INTMSK register is set.	
2	LNBURIS	LCD next address base update raw interrupt status. Mode dependent. Set when the current base address registers have been successfully updated by the next address registers. Signifies that a new next address can be loaded if double buffering is in use. Generates an interrupt if the LNBUIM bit in the INTMSK register is set.	0x0

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Table 464. Raw Interrupt Status register (INTRAW, address 0x4000 8020) bit description

Bits	Function	Description	Reset value
3	VCOMPRIS	Vertical compare raw interrupt status. Set when one of the four vertical regions is reached, as selected by the LcdVComp bits in the CTRL register. Generates an interrupt if the VCompIM bit in the INTMSK register is set.	0x0
4	BERRAW	AHB master bus error raw interrupt status. Set when the AHB master interface receives a bus error response from a slave. Generates an interrupt if the BERIM bit in the INTMSK register is set.	0x0
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

23.6.10 Masked Interrupt Status register

The INTSTAT register is Read-Only, and contains a bit-by-bit logical AND of the INTRAW register and the INTMASK register. A logical OR of all interrupts is provided to the system interrupt controller.

Table 465. Masked Interrupt Status register (INTSTAT, address 0x4000 8024) bit description

Bits	Function	Description	Reset value
0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
1	FUFMIS	FIFO underflow masked interrupt status. Set when the both the FUFRIS bit in the INTRAW register and the FUFIM bit in the INTMSK register are set.	0x0
2	LNBUMIS	LCD next address base update masked interrupt status. Set when the both the LNBURIS bit in the INTRAW register and the LNBUIM bit in the INTMSK register are set.	0x0
3	VCOMPMIS	Vertical compare masked interrupt status. Set when the both the VCompRIS bit in the INTRAW register and the VCompIM bit in the INTMSK register are set.	0x0
4	BERMIS	AHB master bus error masked interrupt status. Set when the both the BERRAW bit in the INTRAW register and the BERIM bit in the INTMSK register are set.	0x0
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

23.6.11 Interrupt Clear register

The INTCLR register is Write-Only. Writing a logic 1 to the relevant bit clears the corresponding interrupt.

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Table 466. Interrupt Clear register (INTCLR, address 0x4000 8028) bit description

Bits	Function	Description	Reset value
0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
1	FUFIC	FIFO underflow interrupt clear. Writing a 1 to this bit clears the FIFO underflow interrupt.	0x0
2	LNBUIC	LCD next address base update interrupt clear. Writing a 1 to this bit clears the LCD next address base update interrupt.	0x0
3	VCOMPIC	Vertical compare interrupt clear. Writing a 1 to this bit clears the vertical compare interrupt.	0x0
4	BERIC	AHB master error interrupt clear. Writing a 1 to this bit clears the AHB master error interrupt.	0x0
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

23.6.12 Upper Panel Current Address register

The UPCURR register is Read-Only, and contains an approximate value of the upper panel data DMA address when read.

Note: This register can change at any time and therefore can only be used as a rough indication of display position.

The contents of the UPCURR register are described in Table 467.

Table 467. Upper Panel Current Address register (UPCURR, address 0x4000 802C) bit description

Bits	Function	Description	Reset value
31:0	LCDUPCURR	LCD Upper Panel Current Address. Contains the current LCD upper panel data DMA address.	0x0

23.6.13 Lower Panel Current Address register

The LPCURR register is Read-Only, and contains an approximate value of the lower panel data DMA address when read.

Note: This register can change at any time and therefore can only be used as a rough indication of display position.

Table 468. Lower Panel Current Address register (LPCURR, address 0x4000 8030) bit description

Bits	Function	Description	Reset value
31:0	LCDLPCURR	LCD Lower Panel Current Address. Contains the current LCD lower panel data DMA address.	0x0

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23.6.14 Color Palette registers

The PAL register contain 256 palette entries organized as 128 locations of two entries per word.

Each word location contains two palette entries. This means that 128 word locations are used for the palette. When configured for little-endian byte ordering, bits [15:0] are the lower numbered palette entry and [31:16] are the higher numbered palette entry. When configured for big-endian byte ordering this is reversed, because bits [31:16] are the low numbered palette entry and [15:0] are the high numbered entry.

Note: Only TFT displays use all of the palette entry bits.

The contents of the PAL register are described in Table 469.

Table 469. Color Palette registers (PAL, address 0x4000 8200 (PAL0) to 0x4000 83FC (PAL255)) bit description

Bits	Function	Description	Reset value
4:0	R04_0	Red palette data. For STN displays, only the four MSBs, bits [4:1], are used. For monochrome displays only the red palette data is used. All of the palette registers have the same bit fields.	0x0
9:5	G04_0	Green palette data.	0x0
14:10	B04_0	Blue palette data.	0x0
15	I0	Intensity / unused bit. Can be used as the LSB of the R, G, and B inputs to a 6:6:6 TFT display, doubling the number of colors to 64K, where each color has two different intensities.	0x0
20:16	R14_0	Red palette data. For STN displays, only the four MSBs, bits [4:1], are used. For monochrome displays only the red palette data is used. All of the palette registers have the same bit fields.	0x0
25:21	G14_0	Green palette data.	0x0
30:26	B14_0	Blue palette data.	0x0
31	I1	Intensity / unused bit. Can be used as the LSB of the R, G, and B inputs to a 6:6:6 TFT display, doubling the number of colors to 64K, where each color has two different intensities.	0x0

23.6.15 Cursor Image registers

The CRSR_IMG register area contains 256-word wide values which are used to define the image or images overlaid on the display by the hardware cursor mechanism. The image must always be stored in LBBP mode (little-endian byte, big-endian pixel) mode, as described in Section 23.7.5.6. Two bits are used to encode color and transparency for each pixel in the cursor.

Depending on the state of bit 0 in the CRSR_CFG register (see Cursor Configuration register description), the cursor image RAM contains either four 32x32 cursor images, or a single 64x64 cursor image.

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The two colors defined for the cursor are mapped onto values from the CRSR_PAL0 and CRSR_PAL0 registers (see Cursor Palette register descriptions).

The contents of the CRSR_IMG register are described in Table 470.

Table 470. Cursor Image registers (CRSR_IMG, address 0x4000 8800 (CRSR_IMG0) to 0x4000 8BFC (CRSR_IMG1)) bit description

Bits	Function	Description	Reset value
31:0	CRSR_IMG	Cursor Image data. The 256 words of the cursor image registers define the appearance of either one 64x64 cursor or 4 32x32 cursors.	0x0

23.6.16 Cursor Control register

The CRSR_CTRL register provides access to frequently used cursor functions, such as the display on/off control for the cursor, and the cursor number.

If a 32x32 cursor is selected, one of four 32x32 cursors can be enabled. The images each occupy one quarter of the image memory, with Cursor0 from location 0, followed by Cursor1 from address 0x100, Cursor2 from 0x200 and Cursor3 from 0x300. If a 64x64 cursor is selected only one cursor fits in the image buffer, and no selection is possible.

Similar frame synchronization rules apply to the cursor number as apply to the cursor coordinates. If CrsrFramesync is 1, the displayed cursor image is only changed during the vertical frame blanking period. If CrsrFrameSync is 0, the cursor image index is changed immediately, even if the cursor is currently being scanned.

The contents of the CRSR_CTRL register are described in Table 471.

Table 471. Cursor Control register (CRSR_CTRL, address 0x4000 8C00) bit description

Bits	Function	Description	Reset value
0	CrsrOn	Cursor enable. 0 = Cursor is not displayed. 1 = Cursor is displayed.	0x0
3:1	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0x0
5:4	CRSRNUM1_0	Cursor image number. If the selected cursor size is 6x64, this field has no effect. If the selected cursor size is 32x32: 00 = Cursor0. 01 = Cursor1. 10 = Cursor2. 11 = Cursor3.	0x0
31:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0x0

23.6.17 Cursor Configuration register

The CRSR_CFG register provides overall configuration information for the hardware cursor.

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The contents of the CRSR_CFG register are described in Table 472.

Table 472. Cursor Configuration register (CRSR_CFG, address 0x4000 8C04) bit description

Bits	Function	Description	Reset value
0	CrsrSize	Cursor size selection. 0 = 32x32 pixel cursor. Allows for 4 defined cursors. 1 = 64x64 pixel cursor.	0x0
1	FRAMESYNC	Cursor frame synchronization type. 0 = Cursor coordinates are asynchronous. 1 = Cursor coordinates are synchronized to the frame synchronization pulse.	0x0
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

23.6.18 Cursor Palette register 0

The cursor palette registers provide color palette information for the visible colors of the cursor. Color0 maps through CRSR_PAL0.

The register provides 24-bit RGB values that are displayed according to the abilities of the LCD panel in the same way as the frame-buffers palette output is displayed.

In monochrome STN mode, only the upper 4 bits of the Red field are used. In STN color mode, the upper 4 bits of the Red, Blue, and Green fields are used. In 24 bits per pixel mode, all 24 bits of the palette registers are significant.

The contents of the CRSR_PAL0 register are described in Table 473.

Table 473. Cursor Palette register 0 (CRSR_PAL0, address 0x4000 8C08) bit description

Bits	Function	Description	Reset value
7:0	RED	Red color component	0x0
15:8	GREEN	Green color component	0x0
23:16	BLUE	Blue color component.	0x0
31:24	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

23.6.19 Cursor Palette register 1

The cursor palette registers provide color palette information for the visible colors of the cursor. Color1 maps through CRSR_PAL1.

The register provides 24-bit RGB values that are displayed according to the abilities of the LCD panel in the same way as the frame-buffers palette output is displayed.

In monochrome STN mode, only the upper 4 bits of the Red field are used. In STN color mode, the upper 4 bits of the Red, Blue, and Green fields are used. In 24 bits per pixel mode, all 24 bits of the palette registers are significant.

The contents of the CRSR_PAL1 register are described in Table 474.

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Table 474. Cursor Palette register 1 (CRSR_PAL1, address 0x4000 8C0C) bit description

Bits	Function	Description	Reset value
7:0	RED	Red color component	0x0
15:8	GREEN	Green color component	0x0
23:16	BLUE	Blue color component.	0x0
31:24	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

23.6.20 Cursor XY Position register

The CRSR_XY register defines the distance of the top-left edge of the cursor from the top-left side of the cursor overlay. Refer to the section on Cursor Clipping for more details.

If the FrameSync bit in the CRSR_CFG register is 0, the cursor position changes immediately, even if the cursor is currently being scanned. If Framesync is 1, the cursor position is only changed during the next vertical frame blanking period.

The contents of the CRSR_XY register are described in Table 475.

Table 475. Cursor XY Position register (CRSR_XY, address 0x4000 8C10) bit description

Bits	Function	Description	Reset value
9:0	CRSRX	X ordinate of the cursor origin measured in pixels. When 0, the left edge of the cursor is at the left of the display.	0x0
15:10	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
25:16	CRSRY	Y ordinate of the cursor origin measured in pixels. When 0, the top edge of the cursor is at the top of the display.	0x0
31:26	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

23.6.21 Cursor Clip Position register

The CRSR_CLIP register defines the distance from the top-left edge of the cursor image, to the first displayed pixel in the cursor image.

Different synchronization rules apply to the Cursor Clip registers than apply to the cursor coordinates. If the FrameSync bit in the CRSR_CFG register is 0, the cursor clip point is changed immediately, even if the cursor is currently being scanned.

If the Framesync bit in the CRSR_CFG register is 1, the displayed cursor image is only changed during the vertical frame blanking period, providing that the cursor position has been updated since the Clip register was programmed. When programming, the Clip register must be written before the Position register (ClcdCrsrXY) to ensure that in a given frame, the clip and position information is coherent.

The contents of the CRSR_CLIP register are described in Table 476.

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Table 476. Cursor Clip Position register (CRSR_CLIP, address 0x4000 8C14) bit description

Bits	Function	Description	Reset value
5:0	CRSRCLIPX	Cursor clip position for X direction. Distance from the left edge of the cursor image to the first displayed pixel in the cursor. When 0, the first pixel of the cursor line is displayed.	0x0
7:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
13:8	CRSRCLIPY	Cursor clip position for Y direction. Distance from the top of the cursor image to the first displayed pixel in the cursor. When 0, the first displayed pixel is from the top line of the cursor image.	0x0
31:14	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

23.6.22 Cursor Interrupt Mask register

The CRSR_INTMSK register is used to enable or disable the cursor from interrupting the processor.

The contents of the CRSR_INTMSK register are described in Table 477.

Table 477. Cursor Interrupt Mask register (CRSR_INTMSK, address 0x4000 8C20) bit description

Bits	Function	Description	Reset value
0	CRSRIM	Cursor interrupt mask. When clear, the cursor never interrupts the processor. When set, the cursor interrupts the processor immediately after reading of the last word of cursor image.	0x0
31:1	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

23.6.23 Cursor Interrupt Clear register

The CRSR_INTCLR register is used by software to clear the cursor interrupt status and the cursor interrupt signal to the processor.

The contents of the CRSR_INTCLR register are described in Table 478.

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Table 478. Cursor Interrupt Clear register (CRSR_INTCLR, address 0x4000 8C24) bit description

Bits	Function	Description	Reset value
0	CRSRIC	Cursor interrupt clear. Writing a 0 to this bit has no effect. Writing a 1 to this bit causes the cursor interrupt status to be cleared.	0x0
31:1	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

23.6.24 Cursor Raw Interrupt Status register

The CRSR_INTRAW register is set to indicate a cursor interrupt. When enabled via the CrsrIM bit in the CRSR_INTMSK register, provides the interrupt to the system interrupt controller.

The contents of the CRSR_INTRAW register are described in Table 479.

Table 479. Cursor Raw Interrupt Status register (CRSR_INTRAW, address 0x4000 8C28) bit description

Bits	Function	Description	Reset value
0	CRSRRIS	Cursor raw interrupt status. The cursor interrupt status is set immediately after the last data is read from the cursor image for the current frame. This bit is cleared by writing to the CrsrIC bit in the CRSR_INTCLR register.	0x0
31:1	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

23.6.25 Cursor Masked Interrupt Status register

The CRSR_INTSTAT register is set to indicate a cursor interrupt providing that the interrupt is not masked in the CRSR_INTMSK register.

The contents of the CRSR_INTSTAT register are described in Table 480.

Table 480. Cursor Masked Interrupt Status register (CRSR_INTSTAT, address 0x4000 8C2C) bit description

Bits	Function	Description	Reset value
0	CRSRMIS	Cursor masked interrupt status. The cursor interrupt status is set immediately after the last data read from the cursor image for the current frame, providing that the corresponding bit in the CRSR_INTMSK register is set. The bit remains clear if the CRSR_INTMSK register is clear. This bit is cleared by writing to the CRSR_INTCLR register.	0x0
31:1	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

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23.7 LCD controller functional description

The LCD controller performs translation of pixel-coded data into the required formats and timings to drive a variety of single or dual panel monochrome and color LCDs.

Packets of pixel coded data are fed using the AHB interface, to two independent, programmable, 32-bit wide, DMA FIFOs that act as input data flow buffers.

The buffered pixel coded data is then unpacked using a pixel serializer.

Depending on the LCD type and mode, the unpacked data can represent:

- An actual true display gray or color value.
- An address to a 256x16 bit wide palette RAM gray or color value.

In the case of STN displays, either a value obtained from the addressed palette location, or the true value is passed to the gray scaling generators. The hardware-coded gray scale algorithm logic sequences the activity of the addressed pixels over a programmed number of frames to provide the effective display appearance.

For TFT displays, either an addressed palette value or true color value is passed directly to the output display drivers, bypassing the gray scaling algorithmic logic.

In addition to data formatting, the LCD controller provides a set of programmable display control signals, including:

- LCD panel power enable
- Pixel clock
- Horizontal and vertical synchronization pulses
- Display bias

The LCD controller generates individual interrupts for:

- Upper or lower panel DMA FIFO underflow
- Base address update signification
- Vertical compare
- Bus error

There is also a single combined interrupt that is asserted when any of the individual interrupts become active.

Figure 53 shows a simplified block diagram of the LCD controller.

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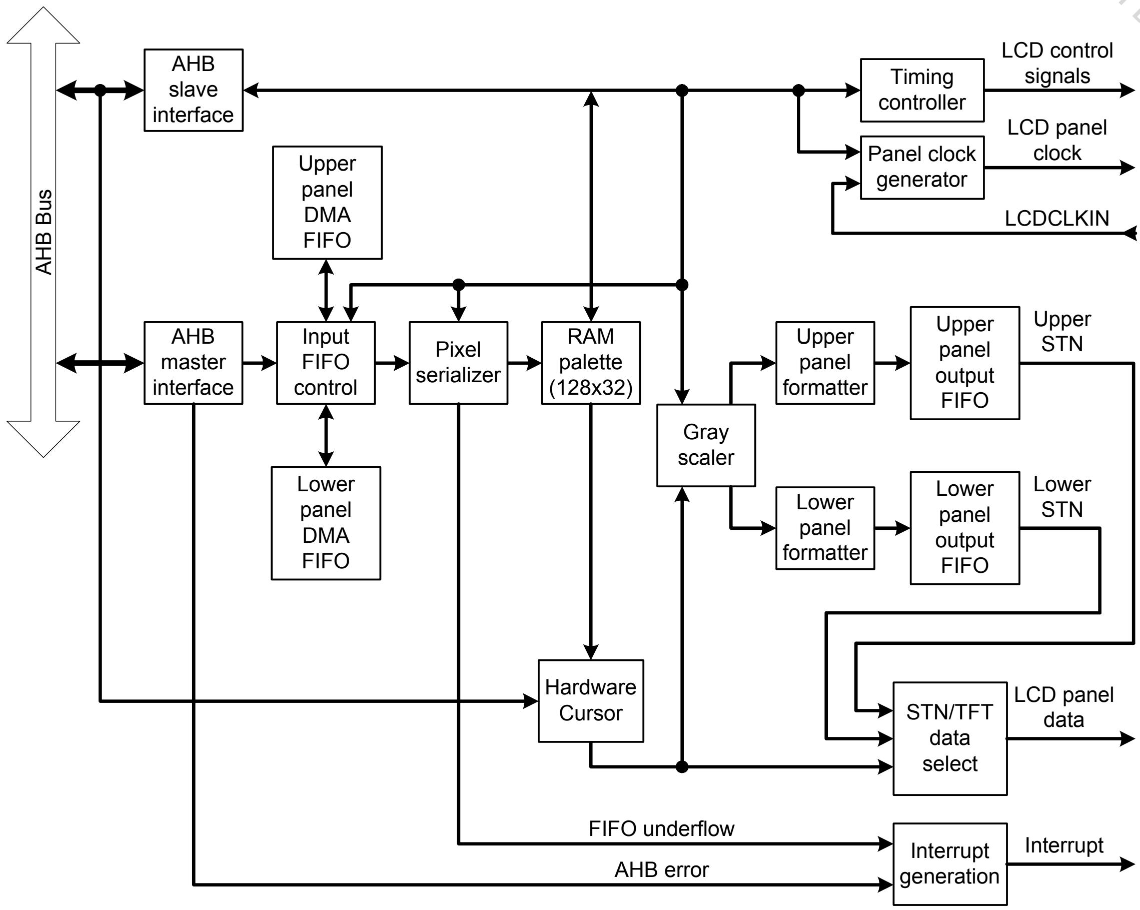


Fig 53. LCD controller block diagram

23.7.1 AHB interfaces

The LCD controller includes two separate AHB interfaces. The first, an AHB slave interface, is used primarily by the CPU to access control and data registers within the LCD controller. The second, an AHB master interface, is used by the LCD controller for DMA access to display data stored in memory elsewhere in the system. The LCD DMA controller can access any SRAM on AHB and the external memory.

23.7.1.1 AMBA AHB slave interface

The AHB slave interface connects the LCD controller to the AHB bus and provides CPU accesses to the registers and palette RAM.

23.7.1.2 AMBA AHB master interface

The AHB master interface transfers display data from a selected slave (memory) to the LCD controller DMA FIFOs. It can be configured to obtain data from any on-chip SRAM on AHB, various types of off-chip static memory, or off-chip SDRAM.

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In dual panel mode, the DMA FIFOs are filled up in an alternating fashion via a single DMA request. In single panel mode, the DMA FIFOs are filled up in a sequential fashion from a single DMA request.

The inherent AHB master interface state machine performs the following functions:

- Loads the upper panel base address into the AHB address incrementer on recognition of a new frame.
- Monitors both the upper and lower DMA FIFO levels and asserts a DMA request to request display data from memory, filling them to above the programmed watermark. the DMA request is reasserted when there are at least four locations available in either FIFO (dual panel mode).
- Checks for 1 kB boundaries during fixed-length bursts, appropriately adjusting the address in such occurrences.
- Generates the address sequences for fixed-length and undefined bursts.
- Controls the handshaking between the memory and DMA FIFOs. It inserts busy cycles if the FIFOs have not completed their synchronization and updating sequence.
- Fills up the DMA FIFOs, in dual panel mode, in an alternating fashion from a single DMA request.
- Asserts the a bus error interrupt if an error occurs during an active burst.
- Responds to retry commands by restarting the failed access. This introduces some busy cycles while it re-synchronizes.

23.7.2 Dual DMA FIFOs and associated control logic

The pixel data accessed from memory is buffered by two DMA FIFOs that can be independently controlled to cover single and dual-panel LCD types. Each FIFO is 16 words deep by 64 bits wide and can be cascaded to form an effective 32-Dword deep FIFO in single panel mode.

Synchronization logic transfers the pixel data from the AHB clock domain to the LCD controller clock domain. The water level marks in each FIFO are set such that each FIFO requests data when at least four locations become available.

An interrupt signal is asserted if an attempt is made to read either of the two DMA FIFOs when they are empty (an underflow condition has occurred).

23.7.3 Pixel serializer

This block reads the 32-bit wide LCD data from the output port of the DMA FIFO and extracts 24, 16, 8, 4, 2, or 1 bpp data, depending on the current mode of operation. The LCD controller supports big-endian, little-endian, and Windows CE data formats.

Depending on the mode of operation, the extracted data can be used to point to a color or gray scale value in the palette RAM or can actually be a true color value that can be directly applied to an LCD panel input.

Table 481 through Table 483 show the structure of the data in each DMA FIFO word corresponding to the endianness and bpp combinations. For each of the three supported data formats, the required data for each panel display pixel must be extracted from the data word.

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Table 481. FIFO bits for Little-endian Byte, Little-endian Pixel order

<table>
<tr><th>FIFO bit</th><th>1 bpp</th><th>2 bpp</th><th>4 bpp</th><th>8 bpp</th><th>16 bpp</th><th>24 bpp</th></tr>
<tr><td>31</td><td>p31</td><td rowspan="2">p15</td><td rowspan="4">p7</td><td rowspan="8">p3</td><td rowspan="16">p1</td><td rowspan="8"></td></tr>
<tr><td>30</td><td>p30</td></tr>
<tr><td>29</td><td>p29</td><td rowspan="2">p14</td></tr>
<tr><td>28</td><td>p28</td></tr>
<tr><td>27</td><td>p27</td><td rowspan="2">p13</td><td rowspan="4">p6</td></tr>
<tr><td>26</td><td>p26</td></tr>
<tr><td>25</td><td>p25</td><td rowspan="2">p12</td></tr>
<tr><td>24</td><td>p24</td></tr>
<tr><td>23</td><td>p23</td><td rowspan="2">p11</td><td rowspan="4">p5</td><td rowspan="8">p2</td><td rowspan="24">p0</td></tr>
<tr><td>22</td><td>p22</td></tr>
<tr><td>21</td><td>p21</td><td rowspan="2">p10</td></tr>
<tr><td>20</td><td>p20</td></tr>
<tr><td>19</td><td>p19</td><td rowspan="2">p9</td><td rowspan="4">p4</td></tr>
<tr><td>18</td><td>p18</td></tr>
<tr><td>17</td><td>p17</td><td rowspan="2">p8</td></tr>
<tr><td>16</td><td>p16</td></tr>
<tr><td>15</td><td>p15</td><td rowspan="2">p7</td><td rowspan="4">p3</td><td rowspan="8">p1</td><td rowspan="16">p0</td></tr>
<tr><td>14</td><td>p14</td></tr>
<tr><td>13</td><td>p13</td><td rowspan="2">p6</td></tr>
<tr><td>12</td><td>p12</td></tr>
<tr><td>11</td><td>p11</td><td rowspan="2">p5</td><td rowspan="4">p2</td></tr>
<tr><td>10</td><td>p10</td></tr>
<tr><td>9</td><td>p9</td><td rowspan="2">p4</td></tr>
<tr><td>8</td><td>p8</td></tr>
<tr><td>7</td><td>p7</td><td rowspan="2">p3</td><td rowspan="4">p1</td><td rowspan="8">p0</td></tr>
<tr><td>6</td><td>p6</td></tr>
<tr><td>5</td><td>p5</td><td rowspan="2">p2</td></tr>
<tr><td>4</td><td>p4</td></tr>
<tr><td>3</td><td>p3</td><td rowspan="2">p1</td><td rowspan="4">p0</td></tr>
<tr><td>2</td><td>p2</td></tr>
<tr><td>1</td><td>p1</td><td rowspan="2">p0</td></tr>
<tr><td>0</td><td>p0</td></tr>
</table>

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Table 482. FIFO bits for Big-endian Byte, Big-endian Pixel order

<table>
<tr><th>FIFO bit</th><th>1 bpp</th><th>2 bpp</th><th>4 bpp</th><th>8 bpp</th><th>16 bpp</th><th>24 bpp</th></tr>
<tr><td>31</td><td>p0</td><td rowspan="2">p0</td><td rowspan="4">p0</td><td rowspan="8">p0</td><td rowspan="16">p0</td><td rowspan="8"></td></tr>
<tr><td>30</td><td>p1</td></tr>
<tr><td>29</td><td>p2</td><td rowspan="2">p1</td></tr>
<tr><td>28</td><td>p3</td></tr>
<tr><td>27</td><td>p4</td><td rowspan="2">p2</td><td rowspan="4">p1</td></tr>
<tr><td>26</td><td>p5</td></tr>
<tr><td>25</td><td>p6</td><td rowspan="2">p3</td></tr>
<tr><td>24</td><td>p7</td></tr>
<tr><td>23</td><td>p8</td><td rowspan="2">p4</td><td rowspan="4">p2</td><td rowspan="8">p1</td><td rowspan="24">p0</td></tr>
<tr><td>22</td><td>p9</td></tr>
<tr><td>21</td><td>p10</td><td rowspan="2">p5</td></tr>
<tr><td>20</td><td>p11</td></tr>
<tr><td>19</td><td>p12</td><td rowspan="2">p6</td><td rowspan="4">p3</td></tr>
<tr><td>18</td><td>p13</td></tr>
<tr><td>17</td><td>p14</td><td rowspan="2">p7</td></tr>
<tr><td>16</td><td>p15</td></tr>
<tr><td>15</td><td>p16</td><td rowspan="2">p8</td><td rowspan="4">p4</td><td rowspan="8">p2</td><td rowspan="16">p1</td></tr>
<tr><td>14</td><td>p17</td></tr>
<tr><td>13</td><td>p18</td><td rowspan="2">p9</td></tr>
<tr><td>12</td><td>p19</td></tr>
<tr><td>11</td><td>p20</td><td rowspan="2">p10</td><td rowspan="4">p5</td></tr>
<tr><td>10</td><td>p21</td></tr>
<tr><td>9</td><td>p22</td><td rowspan="2">p11</td></tr>
<tr><td>8</td><td>p23</td></tr>
<tr><td>7</td><td>p24</td><td rowspan="2">p12</td><td rowspan="4">p6</td><td rowspan="8">p3</td></tr>
<tr><td>6</td><td>p25</td></tr>
<tr><td>5</td><td>p26</td><td rowspan="2">p13</td></tr>
<tr><td>4</td><td>p27</td></tr>
<tr><td>3</td><td>p28</td><td rowspan="2">p14</td><td rowspan="4">p7</td></tr>
<tr><td>2</td><td>p29</td></tr>
<tr><td>1</td><td>p30</td><td rowspan="2">p15</td></tr>
<tr><td>0</td><td>p31</td></tr>
</table>

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Table 483. FIFO bits for Little-endian Byte, Big-endian Pixel order

FIFO bit	1 bpp	2 bpp	4 bpp	8 bpp	16 bpp	24 bpp
31	p24	p12	p6	p3	p1	
30	p25					
29	p26	p13				
28	p27					
27	p28	p14	p7			
26	p29					
25	p30	p15				
24	p31					
23	p16	p8	p4	p2		p0
22	p17					
21	p18	p9				
20	p19					
19	p20	p10	p5			
18	p21					
17	p22	p11				
16	p23					
15	p8	p4	p2	p1	p0	
14	p9					
13	p10	p5				
12	p11					
11	p12	p6	p3			
10	p13					
9	p14	p7				
8	p15					
7	p0	p0	p0	p0		
6	p1					
5	p2	p1				
4	p3					
3	p4	p2	p1			
2	p5					
1	p6	p3				
0	p7					

Table 484 shows the structure of the data in each DMA FIFO word in RGB mode.

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Table 484. RGB mode data formats

FIFO data	24-bit RGB	16-bit (1:5:5:5 RGB)	16-bit (5:6:5 RGB)	16-bit (4:4:4 RGB)
31	-	p1 intensity bit	p1, Blue 4	-
30	-	p1, Blue 4	p1, Blue 3	-
29	-	p1, Blue 3	p1, Blue 2	-
28	-	p1, Blue 2	p1, Blue 1	-
27	-	p1, Blue 1	p1, Blue 0	p1, Blue 3
26	-	p1, Blue 0	p1, Green 5	p1, Blue 2
25	-	p1, Green 4	p1, Green 4	p1, Blue 1
24	-	p1, Green 3	p1, Green 3	p1, Blue 0
23	p0, Blue 7	p1, Green 2	p1, Green 2	p1, Green 3
22	p0, Blue 6	p1, Green 1	p1, Green 1	p1, Green 2
21	p0, Blue 5	p1, Green 0	p1, Green 0	p1, Green 1
20	p0, Blue 4	p1, Red 4	p1, Red 4	p1, Green 0
19	p0, Blue 3	p1, Red 3	p1, Red 3	p1, Red 3
18	p0, Blue 2	p1, Red 2	p1, Red 2	p1, Red 2
17	p0, Blue 1	p1, Red 1	p1, Red 1	p1, Red 1
16	p0, Blue 0	p1, Red 0	p1, Red 0	p1, Red 0
15	p0, Green 7	p0 intensity bit	p0, Blue 4	-
14	p0, Green 6	p0, Blue 4	p0, Blue 3	-
13	p0, Green 5	p0, Blue 3	p0, Blue 2	-
12	p0, Green 4	p0, Blue 2	p0, Blue 1	-
11	p0, Green 3	p0, Blue 1	p0, Blue 0	p0, Blue 3
10	p0, Green 2	p0, Blue 0	p0, Green 5	p0, Blue 2
9	p0, Green 1	p0, Green 4	p0, Green 4	p0, Blue 1
8	p0, Green 0	p0, Green 3	p0, Green 3	p0, Blue 0
7	p0, Red 7	p0, Green 2	p0, Green 2	p0, Green 3
6	p0, Red 6	p0, Green 1	p0, Green 1	p0, Green 2
5	p0, Red 5	p0, Green 0	p0, Green 0	p0, Green 1
4	p0, Red 4	p0, Red 4	p0, Red 4	p0, Green 0
3	p0, Red 3	p0, Red 3	p0, Red 3	p0, Red 3
2	p0, Red 2	p0, Red 2	p0, Red 2	p0, Red 2
1	p0, Red 1	p0, Red 1	p0, Red 1	p0, Red 1
0	p0, Red 0	p0, Red 0	p0, Red 0	p0, Red 0

23.7.4 RAM palette

The RAM-based palette is a 256 x 16 bit dual-port RAM physically structured as 128 x 32 bits. Two entries can be written into the palette from a single word write access. The Least Significant Bit (LSB) of the serialized pixel data selects between upper and lower halves of the palette RAM. The half that is selected depends on the byte ordering mode. In little-endian mode, setting the LSB selects the upper half, but in big-endian mode, the lower half of the palette is selected.

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Pixel data values can be written and verified through the AHB slave interface. For information on the supported colors, refer to the section on the related panel type earlier in this chapter.

The palette RAM is a dual port RAM with independent controls and addresses for each port. Port1 is used as a read/write port and is connected to the AHB slave interface. The palette entries can be written and verified through this port. Port2 is used as a read-only port and is connected to the unpacker and gray scaler. For color modes of less than 16 bpp, the palette enables each pixel value to be mapped to a 16-bit color:

- For TFT displays, the 16-bit value is passed directly to the pixel serializer.
- For STN displays, the 16-bit value is first converted by the gray scaler.

Table 485 shows the bit representation of the palette data. The palette 16-bit output uses the TFT 1:5:5:5 data format. In 16 and 24 bpp TFT mode, the palette is bypassed and the output of the pixel serializer is used as the TFT panel data.

Table 485. Palette data storage for TFT modes.

Bit(s)	Name (RGB format)	Description (RGB format)	Name (BGR format)	Description (BGR format)
31	I	Intensity / unused	I	Intensity / unused
30:26	B[4:0]	Blue palette data	R[4:0]	Red palette data
25:21	G[4:0]	Green palette data	G[4:0]	Green palette data
20:16	R[4:0]	Red palette data	B[4:0]	Blue palette data
15	I	Intensity / unused	I	Intensity / unused
14:10	B[4:0]	Blue palette data	R[4:0]	Red palette data
9:5	G[4:0]	Green palette data	G[4:0]	Green palette data
4:0	R[4:0]	Red palette data	B[4:0]	Blue palette data

The red and blue pixel data can be swapped to support BGR data format using a control register bit (bit 8 = BGR). See the CTRL register description for more information. Table 486 shows the bit representation of the palette data for the STN color modes.

Table 486. Palette data storage for STN color modes.

Bit(s)	Name (RGB format)	Description (RGB format)	Name (BGR format)	Description (BGR format)
31	-	Unused	-	Unused
30:27	B[3:0]	Blue palette data	R[3:0]	Red palette data
26	-	Unused	-	Unused
25:22	G[3:0]	Green palette data	G[3:0]	Green palette data
21	-	Unused	-	Unused
20:17	R[3:0]	Red palette data	B[3:0]	Blue palette data
16	-	Unused	-	Unused
15	I	Unused	I	Unused
14:11	B[4:1]	Blue palette data	R[4:1]	Red palette data
10	B[0]	Unused	R[0]	Unused
9:6	G[4:1]	Green palette data	G[4:1]	Green palette data

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Table 486. Palette data storage for STN color modes.

Bit(s)	Name (RGB format)	Description (RGB format)	Name (BGR format)	Description (BGR format)
5	G[0]	Unused	G[0]	Unused
4:1	R[4:1]	Red palette data	B[4:1]	Blue palette data
0	R[0]	Unused	B[0]	Unused

For monochrome STN mode, only the red palette field bits [4:1] are used. However, in STN color mode the green and blue [4:1] are also used. Only 4 bits per color are used, because the gray scaler only supports 16 different shades per color.

Table 487 shows the bit representation of the palette data for the STN monochrome mode.

Table 487. Palette data storage for STN monochrome mode.

Bit(s)	Name	Description
31	-	Unused
30:27	-	Unused
26	-	Unused
25:22	-	Unused
21	-	Unused
20:17	Y[3:0]	Intensity data
16	-	Unused
15	-	Unused
14:11	-	Unused
10	-	Unused
9:6	-	Unused
5	-	Unused
4:1	Y[3:0]	Intensity data
0	-	Unused

23.7.5 Hardware cursor

The hardware cursor is an integral part of the LCD controller. It uses the LCD timing module to provide an indication of the current scan position coordinate, and intercepts the pixel stream between the palette logic and the gray scale/output multiplexer.

All cursor programming registers are accessed through the LCD slave interface. This also provides a read/write port to the cursor image RAM.

23.7.5.1 Cursor operation

The hardware cursor is contained in a dual port RAM. It is programmed by software through the AHB slave interface. The AHB slave interface also provides access to the hardware cursor control registers. These registers enable you to modify the cursor position and perform various other functions.

When enabled, the hardware cursor uses the horizontal and vertical synchronization signals, along with a pixel clock enable and various display parameters to calculate the current scan coordinate.

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When the display point is inside the bounds of the cursor image, the cursor replaces frame buffer pixels with cursor pixels.

When the last cursor pixel is displayed, an interrupt is generated that software can use as an indication that it is safe to modify the cursor image. This enables software controlled animations to be performed without flickering for frame synchronized cursors.

23.7.5.2 Cursor sizes

Two cursor sizes are supported, as shown in Table 488.

Table 488. Palette data storage for STN monochrome mode.

X Pixels	Y Pixels	Bits per pixel	Words per line	Words in cursor image
32	32	2	2	64
64	64	2	4	256

23.7.5.3 Cursor movement

The following descriptions assume that both the screen and cursor origins are at the top left of the visible screen (the first visible pixel scanned each frame). Figure 54 shows how each pixel coordinate is assumed to be the top left corner of the pixel.

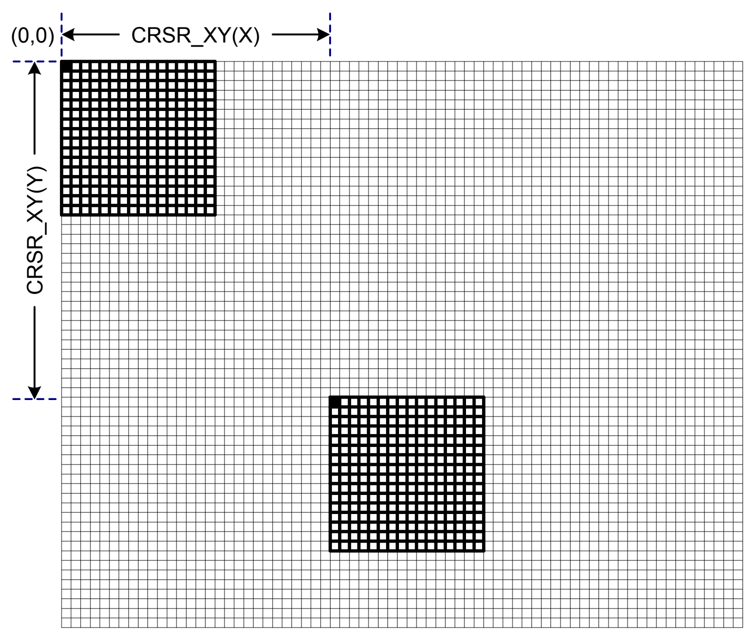


Fig 54. Cursor movement

23.7.5.4 Cursor XY positioning

The CRSR_XY register controls the cursor position on the cursor overlay (see Cursor XY Position register). This provides separate fields for X and Y ordinates.

The CRSR_CFG register (see Cursor Configuration register) provides a FrameSync bit controlling the visible behavior of the cursor.

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With FrameSync inactive, the cursor responds immediately to any change in the programmed CRSR_XY value. Some transient smearing effects may be visible if the cursor is moved across the LCD scan line.

With FrameSync active, the cursor only updates its position after a vertical synchronization has occurred. This provides clean cursor movement, but the cursor position only updates once a frame.

23.7.5.5 Cursor clipping

The CRSR_XY register (see Cursor XY Position register) is programmed with positive binary values that enable the cursor image to be located anywhere on the visible screen image. The cursor image is clipped automatically at the screen limits when it extends beyond the screen image to the right or bottom (see X1,Y1 in Figure 55). The checked pattern shows the visible portion of the cursor.

Because the CRSR_XY register values are positive integers, to emulate cursor clipping on the left and top of screen, a Clip Position register, CRSR_CLIP, is provided. This controls which point of the cursor image is positioned at the CRSR_CLIP coordinate. For clipping functions on the Y axis, CRSR_XY(X) is zero, and Clip(X) is programmed to provide the offset into the cursor image (X2 and X3). The equivalent function is provided to clip on the X axis at the top of the display (Y2).

For cursors that are not clipped at the X=0 or Y=0 lines, program the Clip Position register X and Y fields with zero to display the cursor correctly. See Clip(X4,Y4) for the effect of incorrect programming.

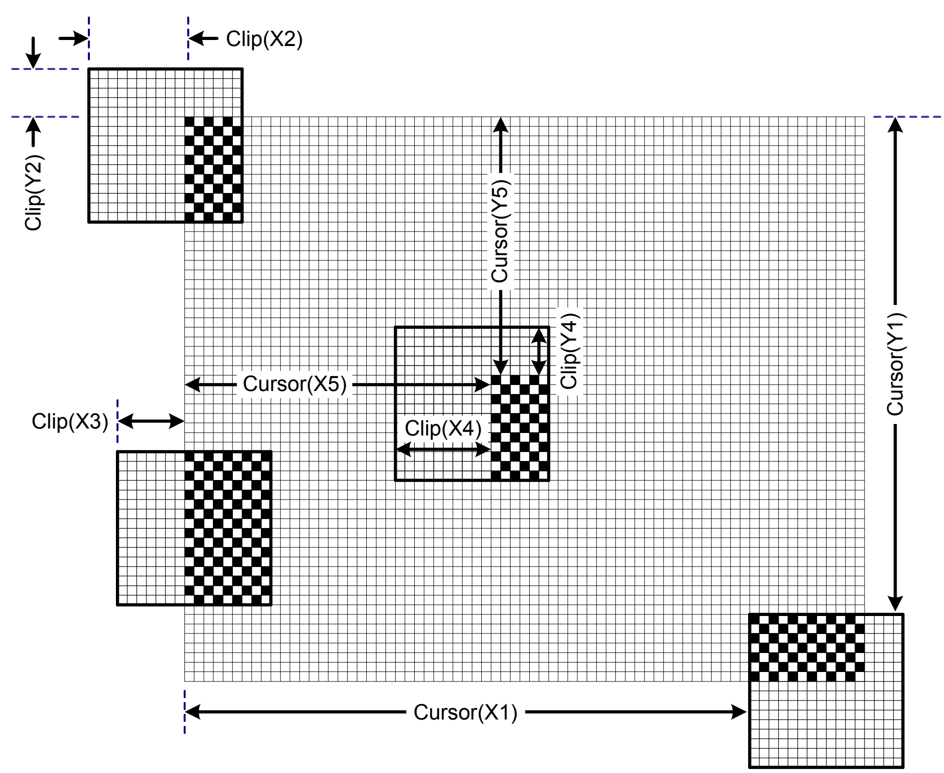


Fig 55. Cursor clipping

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23.7.5.6 Cursor image format

The LCD frame buffer supports three packing formats, but the hardware cursor image requirement has been simplified to support only LBBP. This is little-endian byte, big-endian pixel for Windows CE mode.

The Image RAM start address is offset by 0x800 from the LCD base address, as shown in the register description in this chapter.

The displayed cursor coordinate system is expressed in terms of (X,Y). 64 x 64 is an extension of the 32 x 32 format shown in Figure 56.

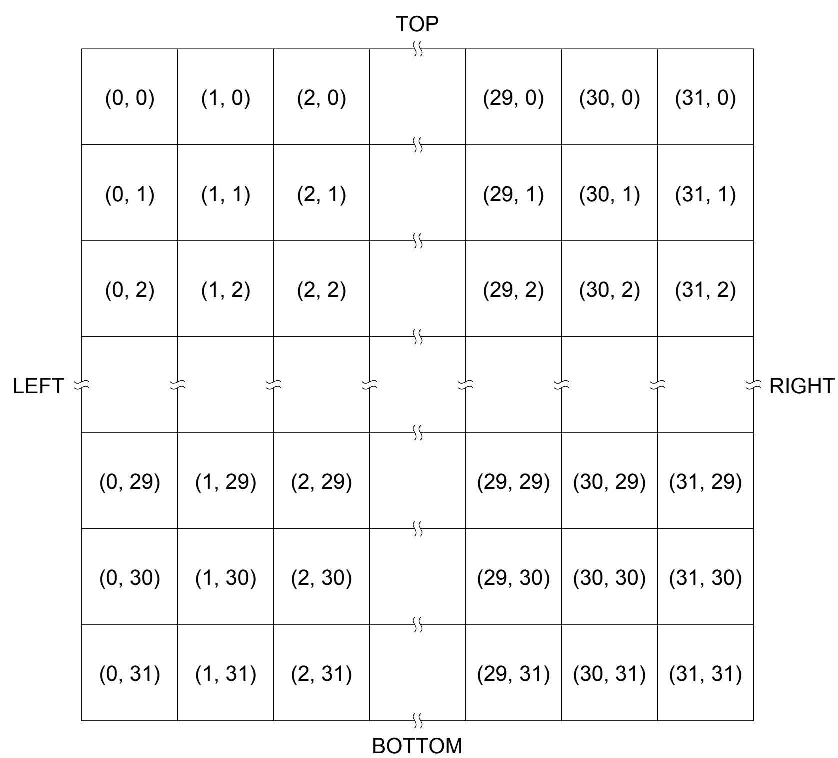


Fig 56. Cursor image format

32 by 32 pixel format

Four cursors are held in memory, each with the same pixel format. Table 489 lists the base addresses for the four cursors.

Table 489. Addresses for 32 x 32 cursors

Address	Description
0x4000 8800	Cursor 0 start address.
0x4000 8900	Cursor 1 start address.
0x4000 8A00	Cursor 2 start address.
0x4000 8B00	Cursor 3 start address.

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Table 490 shows the buffer to pixel mapping for Cursor 0.

Table 490. Buffer to pixel mapping for 32 x 32 pixel cursor format

Data bits	Offset into cursor memory					
	0	4	(8 * y)	(8 * y) +4	F8	FC
31:30	(12, 0)	(28, 0)	(12, y)	(28, y)	(12, 31)	(28,31)
29:28	(13, 0)	(29, 0)	(13, y)	(29, y)	(13, 31)	(29, 31)
27:26	(14, 0)	(30, 0)	(14, y)	(30, y)	(14, 31)	(30, 31)
25:24	(15, 0)	(31, 0)	(15, y)	(31, y)	(15, 31)	(31, 31)
23:22	(8, 0)	(24, 0)	(8, y)	(24, y)	(8, 31)	(24, 31)
21:20	(9, 0)	(25, 0)	(9, y)	(25, y)	(9, 31)	(25, 31)
19:18	(10, 0)	(26, 0)	(10, y)	(26, y)	(10, 31)	(26, 31)
17:16	(11, 0)	(27, 0)	(11, y)	(27, y)	(11, 31)	(27, 31)
15:14	(4, 0)	(20, 0)	(4, y)	(20, y)	(4, 31)	(20, 31)
13:12	(5, 0)	(21, 0)	(5, y)	(21, y)	(5, 31)	(21, 31)
11:10	(6, 0)	(22, 0)	(6, y)	(22, y)	(6, 31)	(22, 31)
9:8	(7, 0)	(23, 0)	(7, y)	(23, y)	(7, 31)	(23, 31)
7:6	(0, 0)	(16, 0)	(0, y)	(16, y)	(0, 31)	(16, 31)
5:4	(1, 0)	(17, 0)	(1, y)	(17, y)	(1, 31)	(17, 31)
3:2	(2, 0)	(18, 0)	(2, y)	(18, y)	(2, 31)	(18, 31)
1:0	(3, 0)	(19, 0)	(3, y)	(19, y)	(3, 31)	(19, 31)

64 by 64 pixel format

Only one cursor fits in the memory space in 64 x 64 mode. Table 491 shows the 64 x 64 cursor format.

Table 491. Buffer to pixel mapping for 64 x 64 pixel cursor format

Data bits	Offset into cursor memory							
	0	4	8	12	(16 * y)	(16 * y) +4	(16 * y) + 8	(16 * y) + 12	FC
31:30	(12, 0)	(28, 0)	(44, 0)	(60, 0)	(12, y)	(28, y)	(44, y)	(60, y)	(60, 63)
29:28	(13, 0)	(29, 0)	(45, 0)	(61, 0)	(13, y)	(29, y)	(45, y)	(61, y)	(61, 63)
27:26	(14, 0)	(30, 0)	(46, 0)	(62, 0)	(14, y)	(30, y)	(46, y)	(62, y)	(62, 63)
25:24	(15, 0)	(31, 0)	(47, 0)	(63, 0)	(15, y)	(31, y)	(47, y)	(63, y)	(63, 63)
23:22	(8, 0)	(24, 0)	(40, 0)	(56, 0)	(8, y)	(24, y)	(40, y)	(56, y)	(56, 63)
21:20	(9, 0)	(25, 0)	(41, 0)	(57, 0)	(9, y)	(25, y)	(41, y)	(57, y)	(57, 63)
19:18	(10, 0)	(26, 0)	(42, 0)	(58, 0)	(10, y)	(26, y)	(42, y)	(58, y)	(58, 63)
17:16	(11, 0)	(27, 0)	(43, 0)	(59, 0)	(11, y)	(27, y)	(43, y)	(59, y)	(59, 63)
15:14	(4, 0)	(20, 0)	(36, 0)	(52, 0)	(4, y)	(20, y)	(36, y)	(52, y)	(52, 63)
13:12	(5, 0)	(21, 0)	(37, 0)	(53, 0)	(5, y)	(21, y)	(37, y)	(53, y)	(53, 63)
11:10	(6, 0)	(22, 0)	(38, 0)	(54, 0)	(6, y)	(22, y)	(38, y)	(54, y)	(54, 63)
9:8	(7, 0)	(23, 0)	(39, 0)	(55, 0)	(7, y)	(23, y)	(39, y)	(55, y)	(55, 63)
7:6	(0, 0)	(16, 0)	(32, 0)	(48, 0)	(0, y)	(16, y)	(32, y)	(48, y)	(48, 63)

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Table 491. Buffer to pixel mapping for 64 x 64 pixel cursor format

Data bits	Offset into cursor memory								
	0	4	8	12	(16 * y)	(16 * y) +4	(16 * y) + 8	(16 * y) + 12	FC
5:4	(1, 0)	(17, 0)	(33, 0)	(49, 0)	(1, y)	(17, y)	(33, y)	(49, y)	(49, 63)
3:2	(2, 0)	(18, 0)	(34, 0)	(50, 0)	(2, y)	(18, y)	(34, y)	(50, y)	(50, 63)
1:0	(3, 0)	(19, 0)	(35, 0)	(51, 0)	(3, y)	(19, y)	(35, y)	(51, y)	(51, 63)

Cursor pixel encoding

Each pixel of the cursor requires two bits of information. These are interpreted as Color0, Color1, Transparent, and Transparent inverted.

In the coding scheme, bit 1 selects between color and transparent (AND mask) and bit 0 selects variant (XOR mask).

Table 492 shows the pixel encoding bit assignments.

Table 492. Pixel encoding

Value	Description
00	Color0. The cursor color is displayed according to the Red-Green-Blue (RGB) value programmed into the CRSR_PAL0 register.
01	Color1. The cursor color is displayed according to the RGB value programmed into the CRSR_PAL1 register.
10	Transparent. The cursor pixel is transparent, so is displayed unchanged. This enables the visible cursor to assume shapes that are not square.
11	Transparent inverted. The cursor pixel assumes the complementary color of the frame pixel that is displayed. This can be used to ensure that the cursor is visible regardless of the color of the frame buffer image.

23.7.6 Gray scaler

A patented gray scale algorithm drives monochrome and color STN panels. This provides 15 gray scales for monochrome displays. For STN color displays, the three color components (RGB) are gray scaled simultaneously. This results in 3375 (15x15x15) colors being available. The gray scaler transforms each 4-bit gray value into a sequence of activity-per-pixel over several frames, relying to some degree on the display characteristics, to give the representation of gray scales and color.

23.7.7 Upper and lower panel formatters

Formatters are used in STN mode to convert the gray scaler output to a parallel format as required by the display. For monochrome displays, this is either 4 or 8 bits wide, and for color displays, it is 8 bits wide. Table 493 shows a color display driven with 2 2/3 pixels worth of data in a repeating sequence.

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Table 493. Color display driven with 2 2/3 pixel data

Byte	CLD[7]	CLD[6]	CLD[5]	CLD[4]	CLD[3]	CLD[2]	CLD[1]	CLD[0]
0	P2[Green]	P2[Red]	P1[Blue]	P1[Green]	P1[Red]	P0[Blue]	P0[Green]	P0[Red]
1	P5[Red]	P4q[Blue]	P4[Green]	P4[Red]	P3[Blue]	P3[Green]	P3[Red]	P2[Blue]
2	P7[Blue]	P7[Green]	P7[Red]	P6[Blue]	P6[Green]	P6[Red]	P5[Blue]	P5[Green]

Each formatter consists of three 3-bit (RGB) shift left registers. RGB pixel data bit values from the gray scaler are concurrently shifted into the respective registers. When enough data is available, a byte is constructed by multiplexing the registered data to the correct bit position to satisfy the RGB data pattern of LCD panel. The byte is transferred to the 3-byte FIFO, which has enough space to store eight color pixels.

23.7.8 Panel clock generator

The output of the panel clock generator block is the panel clock, pin LCDDCLK. The panel clock can be based on either the peripheral clock for the LCD block or the external clock input for the LCD, pin LCDCLKIN. Whichever source is selected can be divided down in order to produce the internal LCD clock, LCDCLK.

The panel clock generator can be programmed to output the LCD panel clock in the range of LCDCLK/2 to LCDCLK/1025 to match the bpp data rate of the LCD panel being used.

The CLKSEL bit in the POL register determines whether the base clock used is CCLK or the LCDCLKIN pin.

23.7.9 Timing controller

The primary function of the timing controller block is to generate the horizontal and vertical timing panel signals. It also provides the panel bias and enable signals. These timings are all register-programmable.

23.7.10 STN and TFT data select

Support is provided for passive Super Twisted Nematic (STN) and active Thin Film Transistor (TFT) LCD display types:

23.7.10.1 STN displays

STN display panels require algorithmic pixel pattern generation to provide pseudo gray scaling on monochrome displays, or color creation on color displays.

23.7.10.2 TFT displays

TFT display panels require the digital color value of each pixel to be applied to the display data inputs.

23.7.11 Interrupt generation

Four interrupts are generated by the LCD controller, and a single combined interrupt. The four interrupts are:

- Master bus error interrupt.
- Vertical compare interrupt.

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- Next base address update interrupt.
- FIFO underflow interrupt.

Each of the four individual maskable interrupts is enabled or disabled by changing the mask bits in the INT_MSK register. These interrupts are also combined into a single overall interrupt, which is asserted if any of the individual interrupts are both asserted and unmasked. Provision of individual outputs in addition to a combined interrupt output enables use of either a global interrupt service routine, or modular device drivers to handle interrupts.

The status of the individual interrupt sources can be read from the INTRAW register.

23.7.11.1 Master bus error interrupt

The master bus error interrupt is asserted when an ERROR response is received by the master interface during a transaction with a slave. When such an error is encountered, the master interface enters an error state and remains in this state until clearance of the error has been signaled to it. When the respective interrupt service routine is complete, the master bus error interrupt may be cleared by writing a 1 to the BERIC bit in the INTCLR register. This action releases the master interface from its ERROR state to the start of FRAME state, and enables fresh frame of data display to be initiated.

23.7.11.2 Vertical compare interrupt

The vertical compare interrupt asserts when one of four vertical display regions, selected using the CTRL register, is reached. The interrupt can be made to occur at the start of:

- Vertical synchronization.
- Back porch.
- Active video.
- Front porch.

The interrupt may be cleared by writing a 1 to the VcompIC bit in the INTCLR register.

23.7.11.2.1 Next base address update interrupt

The LCD next base address update interrupt asserts when either the LCDUPBASE or LCDLPBASE values have been transferred to the LCDUPCURR or LCDLPCURR incrementers respectively. This signals to the system that it is safe to update the LCDUPBASE or the LCDLPBASE registers with new frame base addresses if required.

The interrupt can be cleared by writing a 1 to the LNBUIC bit in the INTCLR register

23.7.11.2.2 FIFO underflow interrupt

The FIFO underflow interrupt asserts when internal data is requested from an empty DMA FIFO. Internally, upper and lower panel DMA FIFO underflow interrupt signals are generated.

The interrupt can be cleared by writing a 1 to the FUFIC bit in the INTCLR register.

23.7.12 LCD power-up and power-down sequence

The LCD controller requires the following power-up sequence to be performed:

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1. When power is applied, the following signals are held LOW:

- LCDLP
- LCDDCLK
- LCDFP
- LCDENAB/ LCDM
- LCDVD[23:0]
- LCDLE

2. When LCD power is stabilized, a 1 is written to the LcdEn bit in the CTRL register. This enables the following signals into their active states:

- LCDLP
- LCDDCLK
- LCDFP
- LCDENAB/ LCDM
- LCDLE

The LCDV[23:0] signals remain in an inactive state.

3. When the signals in step 2 have stabilized, the contrast voltage (not controlled or supplied by the LCD controller) is applied to the LCD panel.

4. If required, a software or hardware timer can be used to provide the minimum display specific delay time between application of the control signals and power to the panel display. On completion of the time interval, power is applied to the panel by writing a 1 to the LcdPwr bit within the CTRL register that, in turn, sets the LCDPWR signal high and enables the LCDV[23:0] signals into their active states. The LCDPWR signal is intended to be used to gate the power to the LCD panel.

The power-down sequence is the reverse of the above four steps and must be strictly followed, this time, writing the respective register bits with 0.

Figure 57 shows the power-up and power-down sequences.

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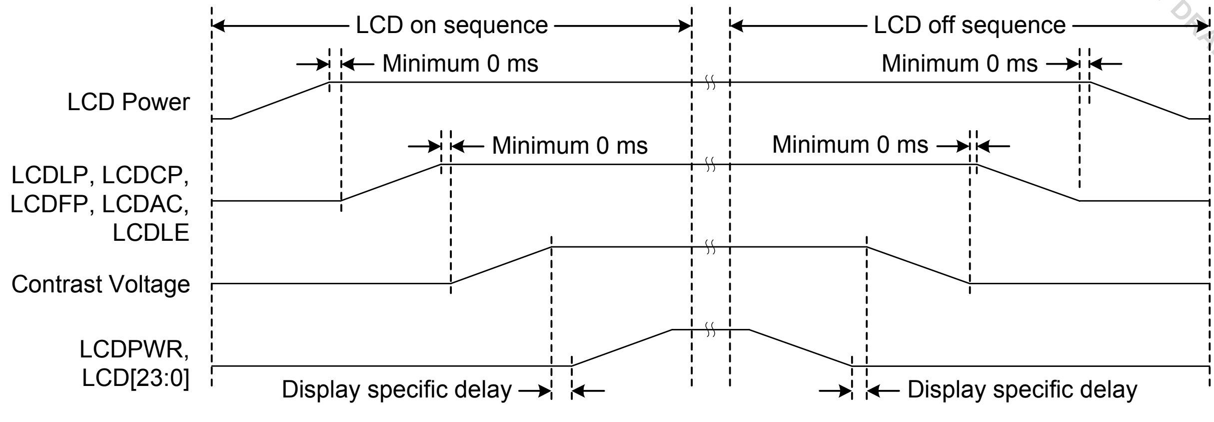
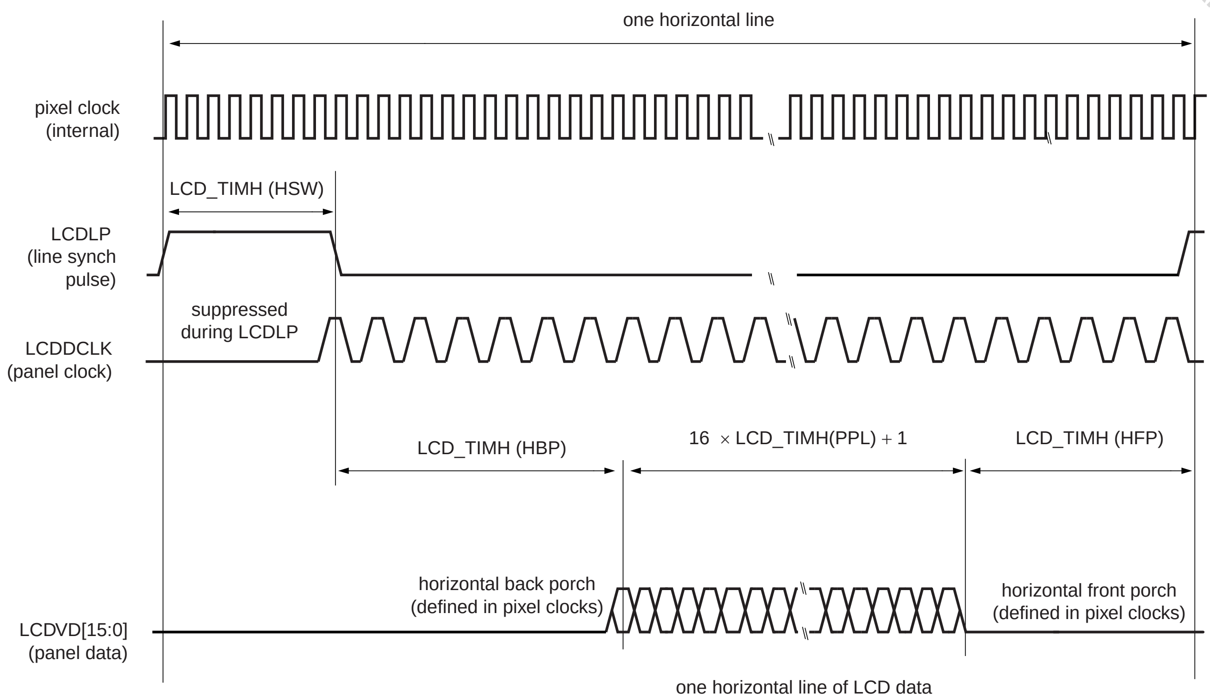


Fig 57. Power-up and power-down sequences

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23.8 LCD timing diagrams



(1) The active data lines will vary with the type of STN panel (4-bit, 8-bit, color, mono) and with single or dual frames.

(2) The LCD panel clock is selected and scaled by the LCD controller and used to produce LCDCLK.

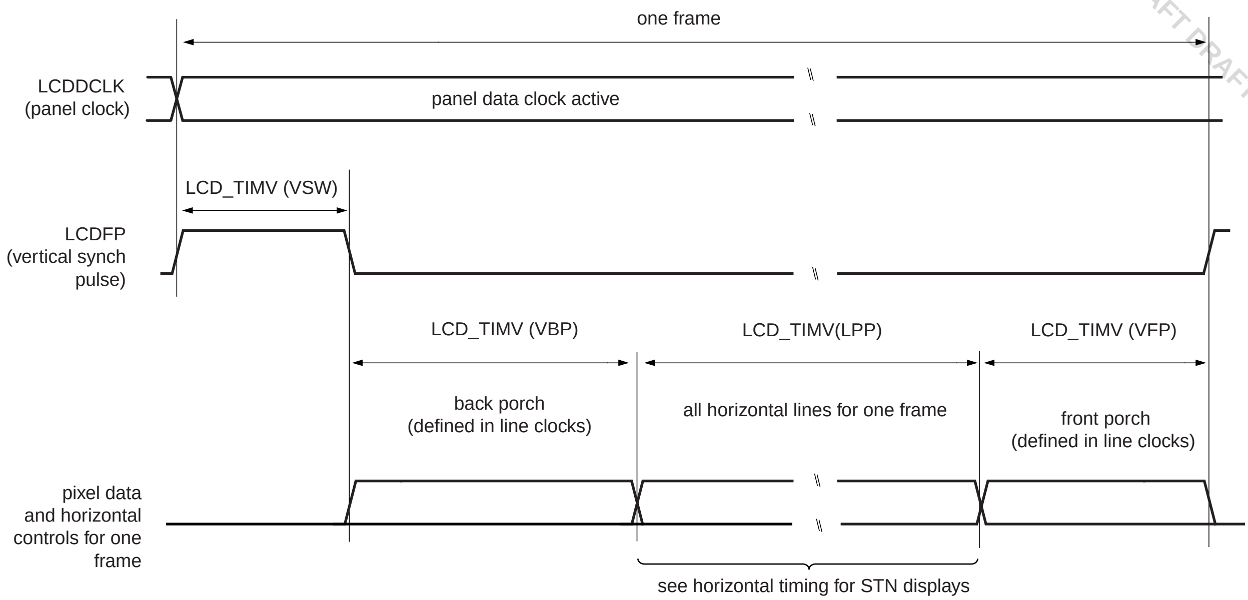
(3) The duration of the LCDLP signal is controlled by the HSW field in the TIMH register.

(4) The Polarity of the LCDLP signal is determined by the IHS bit in the POL register.

Fig 58. Horizontal timing for STN displays

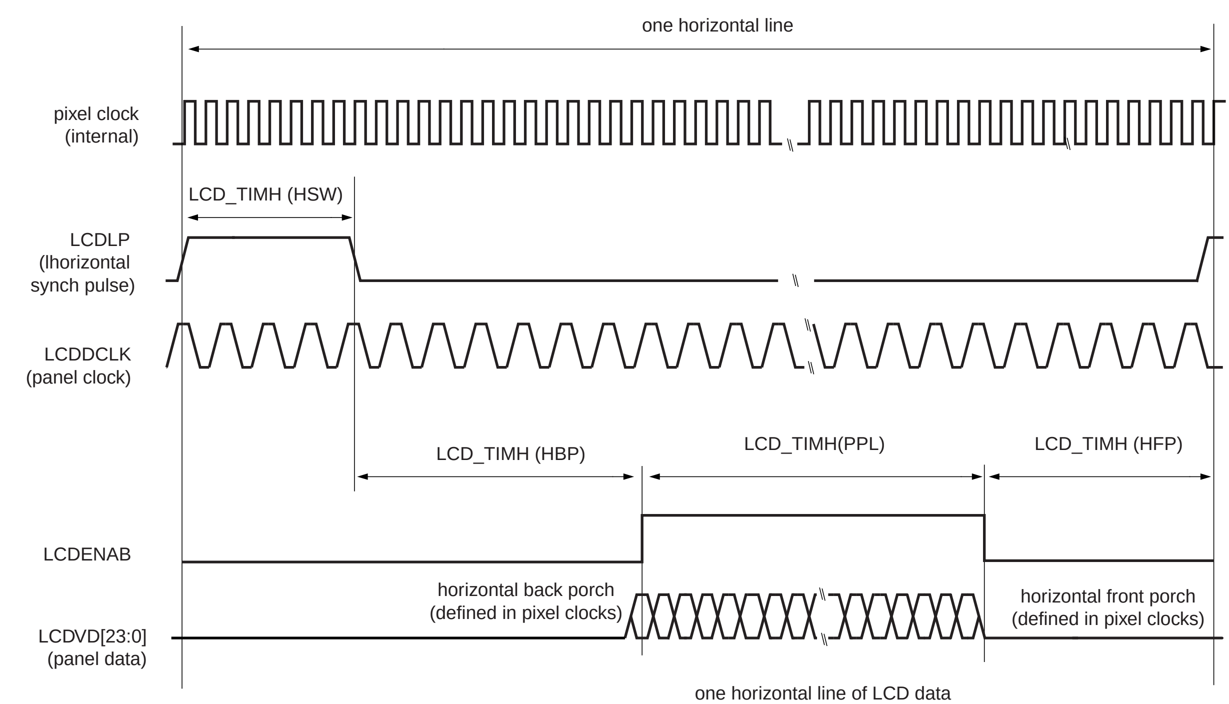
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(1) Signal polarities may vary for some displays.

Fig 59. Vertical timing for STN displays



(1) The active data lines will vary with the type of TFT panel.

(2) The LCD panel clock is selected and scaled by the LCD controller and used to produce LCDCLK.

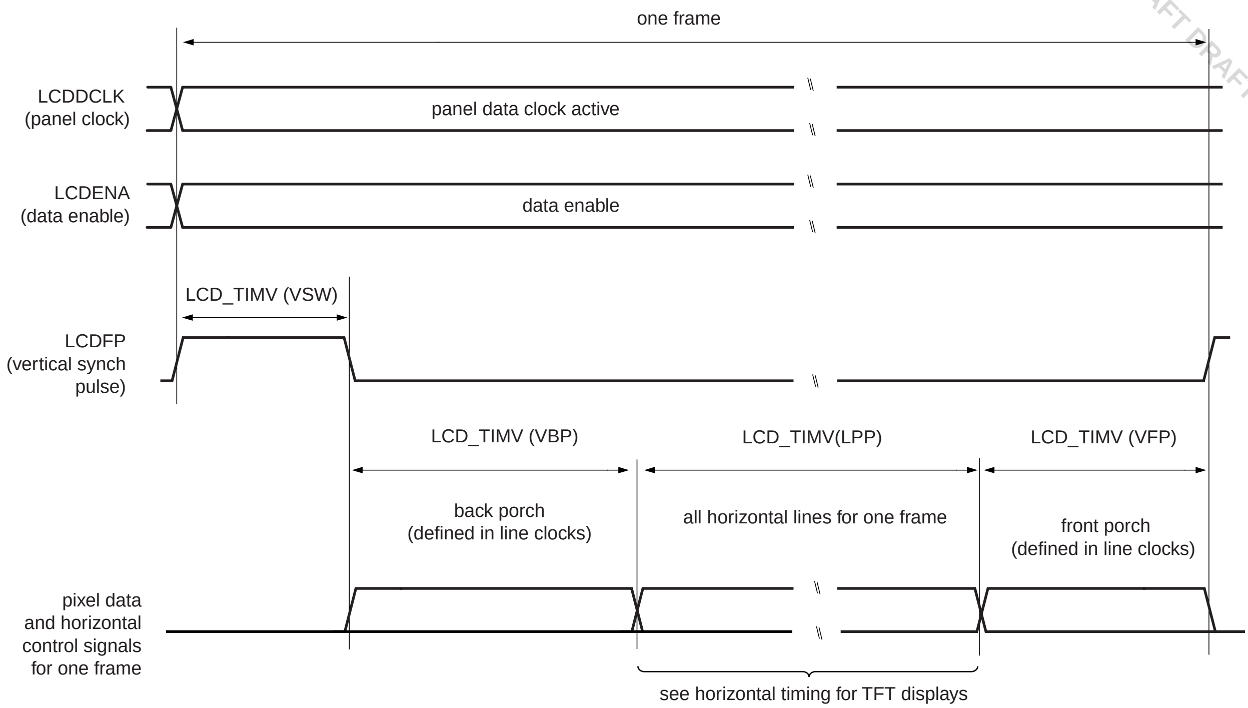
(3) The duration of the LCDLP is controlled by the HSW field in the TIMH register.

(4) The polarity of the LCDLP signal is determined by the IHS bit in the POL register.

Fig 60. Horizontal timing for TFT displays

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(1) Polarities may vary for some displays.

Fig 61. Vertical timing for TFT displays

23.9 LCD panel signal usage

Table 494. LCD panel connections for STN single panel mode

External pin	4-bit mono STN single panel		8-bit mono STN single panel		Color STN single panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCDVD23	-	-	-	-	-	-
LCDVD22	-	-	-	-	-	-
LCDVD21	-	-	-	-	-	-
LCDVD20	-	-	-	-	-	-
LCDVD19	-	-	-	-	-	-
LCDVD18	-	-	-	-	-	-
LCDVD17	-	-	-	-	-	-
LCDVD16	-	-	-	-	-	-
LCDVD15	-	-	-	-	-	-
LCDVD14	-	-	-	-	-	-
LCDVD13	-	-	-	-	-	-
LCDVD12	-	-	-	-	-	-
LCDVD11	-	-	-	-	-	-
LCDVD10	-	-	-	-	-	-
LCDVD9	-	-	-	-	-	-

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Table 494. LCD panel connections for STN single panel mode

External pin	4-bit mono STN single panel		8-bit mono STN single panel		Color STN single panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCDVD8	-	-	-	-	-	-
LCDVD7	-	-	P8_4	UD[7]	P8_4	UD[7]
LCDVD6	-	-	P8_5	UD[6]	P8_5	UD[6]
LCDVD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCDVD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCDVD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]
LCDVD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCDVD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCDVD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCDLP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCDFP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCDLE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCDPWR	P7_7	CDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 495. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCDVD23	-	-	-	-	-	-
LCDVD22	-	-	-	-	-	-
LCDVD21	-	-	-	-	-	-
LCDVD20	-	-	-	-	-	-
LCDVD19	-	-	-	-	-	-
LCDVD18	-	-	-	-	-	-
LCDVD17	-	-	-	-	-	-
LCDVD16	-	-	-	-	-	-
LCDVD15	-	-	PB_4	LD[7]	PB_4	LD[7]
LCDVD14	-	-	PB_5	LD[6]	PB_5	LD[6]
LCDVD13	-	-	PB_6	LD[5]	PB_6	LD[5]
LCDVD12	-	-	P8_3	LD[4]	P8_3	LD[4]
LCDVD11	P4_9	LD[3]	P4_9	LD[3]	P4_9	LD[3]
LCDVD10	P4_10	LD[2]	P4_10	LD[2]	P4_10	LD[2]
LCDVD9	P4_8	LD[1]	P4_8	LD[1]	P4_8	LD[1]
LCDVD8	P7_5	LD[0]	P7_5	LD[0]	P7_5	LD[0]
LCDVD7	-	-		UD[7]	P8_4	UD[7]
LCDVD6	-	-	P8_5	UD[6]	P8_5	UD[6]

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Table 495. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCDVD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCDVD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCDVD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]
LCDVD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCDVD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCDVD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCDLP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCDFP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCDLE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 496. LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCDVD23	PB_0	BLUE3	PB_0	BLUE4	PB_0	BLUE4		BLUE7
LCDVD22	PB_1	BLUE2	PB_1	BLUE3	PB_1	BLUE3		BLUE6
LCDVD21	PB_2	BLUE1	PB_2	BLUE2	PB_2	BLUE2		BLUE5
LCDVD20	PB_3	BLUE0	PB_3	BLUE1	PB_3	BLUE1		BLUE4
LCDVD19	-	-	P7_1	BLUE0	P7_1	BLUE0		BLUE3
LCDVD18	-	-	-	-	P7_2	intensity		BLUE2
LCDVD17	-	-	-	-	-	-	P7_3	BLUE1
LCDVD16	-	-	-	-	-	-	P7_4	BLUE0
LCDVD15	PB_4	GREEN3	PB_4	GREEN5	PB_4	GREEN4	PB_4	GREEN7
LCDVD14	PB_5	GREEN2	PB_5	GREEN4	PB_5	GREEN3	PB_5	GREEN6
LCDVD13	PB_6	GREEN1	PB_6	GREEN3	PB_6	GREEN2	PB_6	GREEN5
LCDVD12	P8_3	GREEN0	P8_3	GREEN2	P8_3	GREEN1	P8_3	GREEN4
LCDVD11	-	-	P4_9	GREEN1	P4_9	GREEN0	P4_9	GREEN3
LCDVD10	-	-	P4_10	GREEN0	P4_10	intensity	P4_10	GREEN2
LCDVD9	-	-	-	-	-	-	P4_8	GREEN1
LCDVD8	-	-	-	-	-	-	P7_5	GREEN0
LCDVD7	P8_4	RED3	P8_4	RED4	P8_4	RED4	P8_4	RED7
LCDVD6	P8_5	RED2	P8_5	RED3	P8_5	RED3	P8_5	RED6
LCDVD5	P8_6	RED1	P8_6	RED2	P8_6	RED2	P8_6	RED5
LCDVD4	P8_7	RED0	P8_7	RED1	P8_7	RED1	P8_7	RED4

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Table 496. LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCDVD3	-	-	P4_2	RED0	P4_2	RED0	P4_2	RED3
LCDVD2	-	-	-	-	P4_3	intensity	P4_3	RED2
LCDVD1	-	-	-	-	-	-	P4_4	RED1
LCDVD0	-	-	-	-	-	-	P4_1	RED0
LCDLP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/L CDM
LCDFP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCDLE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

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24.1 How to read this chapter

The SCT is available on all LPC18xx parts.

The following configuration options apply to parts LPC1850_30_20_10 Rev 'A' only:

- The SCT inputs and outputs are connected to event-driven peripherals through the GIMA (see Section 14.3).

24.2 Basic configuration

The SCT is configured as follows:

- See Table 497 for clocking and power control.
- The SCT is reset by the SCT_RST (reset #37).
- Connect inputs and outputs of the SCT through the GIMA (see Chapter 14).
- The SCT combined interrupt is connected to slot # 10 in the NVIC. SCT outputs 2, 6, 14 are ORed with timer match channels and connected to slots # 13, 14, 16 in the Event router (see Table 16).
- For connecting the SCT outputs 0 and 1 to the GPDMA, use the DMAMUX register in the CREG block (see Table 35) and enable the GPDMA channel in the DMA Channel Configuration registers Section 16.6.20.

Table 497. SCT clocking and power control

	Base clock	Branch clock	Maximum frequency
SCT	BASE_M3_CLK	CLK_M3_SCT	150 MHz

24.3 Features

- Two 16-bit counters or one 32-bit counter.
- Counter(s) clocked by bus clock or selected input.
- Up counter(s) or up-down counter(s).
- State variable allows sequencing across multiple counter cycles.
- Event can be defined by a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state.
- Events control outputs, interrupts, and DMA requests.
- Selected event(s) can limit, halt, start, or stop a counter.
- Supports:
  - 8 inputs
  - 16 outputs
  - 16 match/capture registers
  - 16 events

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– 32 states

24.4 General description

The State Configurable Timer (SCT) allows a wide variety of timing, counting, output modulation, and input capture operations.

The most basic user-programmable option is whether a SCT operates as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable
- Limit, halt, stop, and start conditions
- Values of Match/Capture registers, plus reload or capture control values

In the two-counter case, the following operational elements are global to the SCT, but events, outputs, interrupts, and DMA requests can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts
- DMA requests

Remark: This document uses the term “bus error” to indicate a SCT response that makes the processor take an exception.

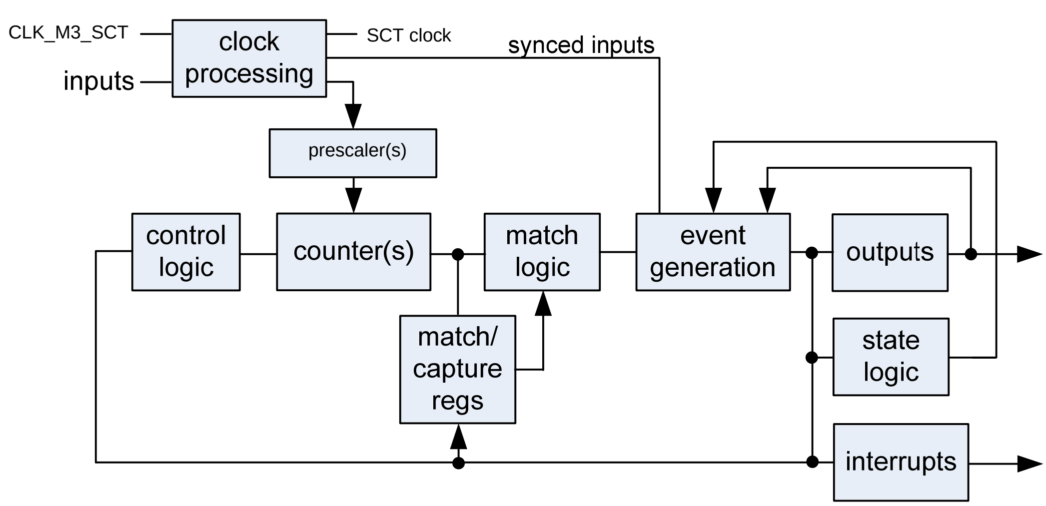


Fig 62. SCT block diagram

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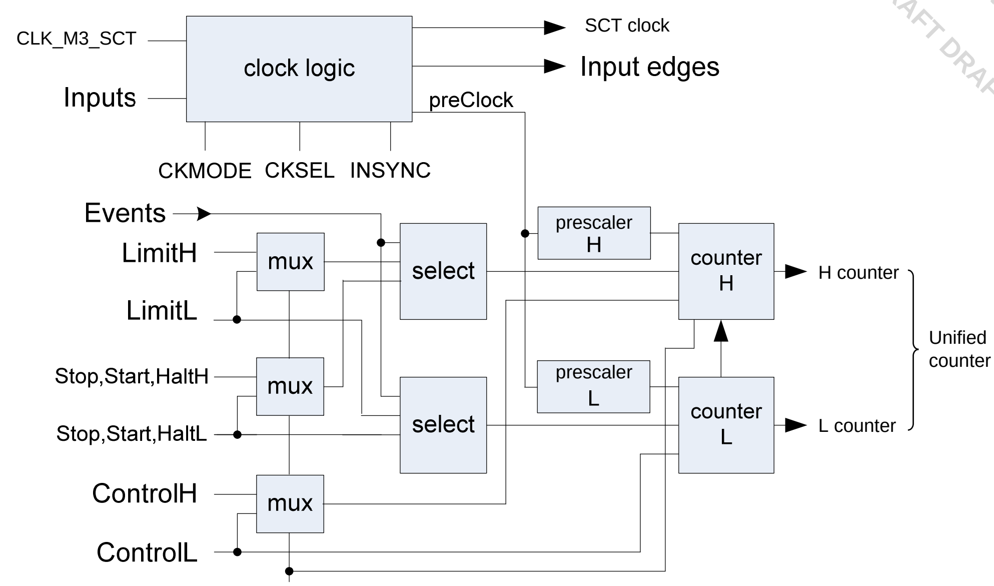


Fig 63. SCT counter and select logic

24.5 Pin description

Table 498. SCT pin description

Function name	Direction	Description
CTIN_[7:0]	I	State Configurable Timer (SCT) inputs.
CTOUT_[15:0]	O	State Configurable Timer (SCT) outputs.

24.6 Register description

The register addresses of the State Configurable Timer are shown in Table 499. For most of the SCT registers, the register function depends on the setting of certain other register bits:

1. The UNIFY bit in the CONFIG register determines whether the SCT is used as one 32-bit register (for operation as one 32-bit counter/timer) or as two 16-bit counter/timers named L and H. The setting of the UNIFY bit is reflected in the register map:
   – UNIFY = 1: Only one register is used (for operation as one 32-bit counter/timer).
   – UNIFY = 0: The L and H registers can be accessed by a 32-bit read or write operation or can be read or written to individually (for operation as two 16-bit counter/timers).

   Typically, the UNIFY bit is configured by writing to the CONFIG register before any other registers are accessed.
2. The REGMODEn bits in the REGMODE register determine whether each set of Match/Capture registers uses the match or capture functionality:
   – REGMODEn = 1: Registers operate as match and reload registers.

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– REGMODEn = 0: Registers operate as capture and capture control registers.

Table 499. Register overview: State Configurable Timer (base address 0x4000 0000)

Name	Access	Address offset	Description	Reset value
CONFIG	R/W	0x000	SCT configuration register	0x0000 7E00
CTRL	R/W	0x004	SCT control register	0x0004 0004
CTRL_L	R/W	0x004	SCT control register low counter 16-bit	0x0004 0004
CTRL_H	R/W	0x006	SCT control register high counter 16-bit	0x0004 0004
LIMIT	R/W	0x008	SCT limit register	0x0000 0000
LIMIT_L	R/W	0x008	SCT limit register low counter 16-bit	0x0000 0000
LIMIT_H	R/W	0x00A	SCT limit register high counter 16-bit	0x0000 0000
HALT	R/W	0x00C	SCT halt condition register	0x0000 0000
HALT_L	R/W	0x00C	SCT halt condition register low counter 16-bit	0x0000 0000
HALT_H	R/W	0x00E	SCT halt condition register high counter 16-bit	0x0000 0000
STOP	R/W	0x010	SCT stop condition register	0x0000 0000
STOP_L	R/W	0x010	SCT stop condition register low counter 16-bit	0x0000 0000
STOP_H	R/W	0x012	SCT stop condition register high counter 16-bit	0x0000 0000
START	R/W	0x014	SCT start condition register	0x0000 0000
START_L	R/W	0x014	SCT start condition register low counter 16-bit	0x0000 0000
START_H	R/W	0x016	SCT start condition register high counter 16-bit	0x0000 0000
-	-	0x018 - 0x03C	Reserved	
COUNT	R/W	0x040	SCT counter register	0x0000 0000
COUNT_L	R/W	0x040	SCT counter register low counter 16-bit	0x0000 0000
COUNT_H	R/W	0x042	SCT counter register high counter 16-bit	0x0000 0000
STATE	R/W	0x044	SCT state register	0x0000 0000
STATE_L	R/W	0x044	SCT state register low counter 16-bit	0x0000 0000
STATE_H	R/W	0x046	SCT state register high counter 16-bit	0x0000 0000
INPUT	RO	0x048	SCT input register	0x0000 0000
REGMODE	R/W	0x04C	SCT match/capture registers mode register	0x0000 0000
REGMODE_L	R/W	0x04C	SCT match/capture registers mode register low counter 16-bit	0x0000 0000
REGMODE_O	R/W	0x04E	SCT match/capture registers mode register high counter 16-bit	0x0000 0000
OUTPUT	R/W	0x050	SCT output register	0x0000 0000
OUTPUTDIRCTRL	R/W	0x054	SCT output counter direction control register	0x0000 0000
RES	R/W	0x058	SCT conflict resolution register	0x0000 0000
DMAREQ0	R/W	0x05C	SCT DMA request 0 register	0x0000 0000
DMAREQ1	R/W	0x060	SCT DMA request 1 register	0x0000 0000
-	-	0x064 - 0x0EC	Reserved	
EVEN	R/W	0x0F0	SCT event enable register	0x0000 0000
EVFLAG	R/W	0x0F4	SCT event flag register	0x0000 0000
CONEN	R/W	0x0F8	SCT conflict enable register	0x0000 0000
CONFLAG	R/W	0x0FC	SCT conflict flag register	0x0000 0000

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Table 499. Register overview: State Configurable Timer (base address 0x4000 0000) *…continued*

Name	Access	Address offset	Description	Reset value
MATCH0 to MATCH15	R/W	0x100 to 0x13C	SCT match value register of match channels 0 to 15; REGMOD0 to REGMODE15 = 0	0x0000 0000
MATCH0_L to MATCH15_L	R/W	0x100 to 0x13C	SCT match value register of match channels 0 to 15; low counter 16-bit; REGMOD0_L to REGMODE15_L = 0	0x0000 0000
MATCH0_H to MATCH15_H	R/W	0x102 to 0x13E	SCT match value register of match channels 0 to 15; high counter 16-bit; REGMOD0_H to REGMODE15_H = 0	0x0000 0000
CAP0 to CAP15		0x100 to 0x13C	SCT capture register of capture channel 0 to 15; REGMOD0 to REGMODE15 = 1	0x0000 0000
CAP0_L to CAP15_L		0x100 to 0x13C	SCT capture register of capture channel 0 to 15; low counter 16-bit; REGMOD0_L to REGMODE15_L = 1	0x0000 0000
CAP0_H to CAP15_H		0x102 to 0x13E	SCT capture register of capture channel 0 to 15; high counter 16-bit; REGMOD0_H to REGMODE15_H = 1	0x0000 0000
MATCHREL0 to MATCHREL15	R/W	0x200 to 0x23C	SCT match reload value register 0 to 15; REGMOD0 = 0 to REGMODE15 = 0	0x0000 0000
MATCHREL0_L to MATCHREL15_L	R/W	0x200 to 0x23C	SCT match reload value register 0 to 15; low counter 16-bit; REGMOD0_L = 0 to REGMODE15_L = 0	0x0000 0000
MATCHREL0_H to MATCHREL15_H	R/W	0x202 to 0x23E	SCT match reload value register 0 to 15; high counter 16-bit; REGMOD0_H = 0 to REGMODE15_H = 0	0x0000 0000
CAPCTRL0 to CAPCTRL15		0x200 to 0x23C	SCT capture control register 0 to 15; REGMOD0 = 1 to REGMODE15 = 1	0x0000 0000
CAPCTRL0_L to CAPCTRL15_L		0x200 to 0x23C	SCT capture control register 0 to 15; low counter 16-bit; REGMOD0_L = 1 to REGMODE15_L = 1	0x0000 0000
CAPCTRL0 to CAPCTRL15		0x202 to 0x23E	SCT capture control register 0 to 15; high counter 16-bit; REGMOD0 = 1 to REGMODE15 = 1	0x0000 0000
EVSTATEMSK0	R/W	0x300	SCT event state register 0	0x0000 0000
EVCTRL0	R/W	0x304	SCT event control register 0	0x0000 0000
EVSTATEMSK1	R/W	0x308	SCT event state register 1	0x0000 0000
EVCTRL1	R/W	0x30C	SCT event control register 1	0x0000 0000
EVSTATEMSK2	R/W	0x310	SCT event state register 2	0x0000 0000
EVCTRL2	R/W	0x314	SCT event control register 2	0x0000 0000
EVSTATEMSK3	R/W	0x318	SCT event state register 3	0x0000 0000
EVCTRL3	R/W	0x31C	SCT event control register 3	0x0000 0000
EVSTATEMSK4	R/W	0x320	SCT event state register 4	0x0000 0000
EVCTRL4	R/W	0x324	SCT event control register4	0x0000 0000
EVSTATEMSK5	R/W	0x328	SCT event state register 5	0x0000 0000
EVCTRL5	R/W	0x32C	SCT event control register 5	0x0000 0000
EVSTATEMSK6	R/W	0x330	SCT event state register 6	0x0000 0000
EVCTRL6	R/W	0x334	SCT event control register 6	0x0000 0000
EVSTATEMSK7	R/W	0x338	SCT event state register 7	0x0000 0000
EVCTRL7	R/W	0x33C	SCT event control register 7	0x0000 0000
EVSTATEMSK8	R/W	0x340	SCT event state register 8	0x0000 0000
EVCTRL8	R/W	0x344	SCT event control register 8	0x0000 0000
EVSTATEMSK9	R/W	0x348	SCT event state register 9	0x0000 0000

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Table 499. Register overview: State Configurable Timer (base address 0x4000 0000) *…continued*

Name	Access	Address offset	Description	Reset value
EVCTRL9	R/W	0x34C	SCT event control register 9	0x0000 0000
EVSTATEMSK10	R/W	0x350	SCT event state register 10	0x0000 0000
EVCTRL10	R/W	0x354	SCT event control register 10	0x0000 0000
EVSTATEMSK11	R/W	0x358	SCT event state register 11	0x0000 0000
EVCTRL11	R/W	0x35C	SCT event control register 11	0x0000 0000
EVSTATEMSK12	R/W	0x360	SCT event state register 12	0x0000 0000
EVCTRL12	R/W	0x364	SCT event control register 12	0x0000 0000
EVSTATEMSK13	R/W	0x368	SCT event state register 13	0x0000 0000
EVCTRL13	R/W	0x36C	SCT event control register 13	0x0000 0000
EVSTATEMSK14	R/W	0x370	SCT event state register 14	0x0000 0000
EVCTRL14	R/W	0x374	SCT event control register 14	0x0000 0000
EVSTATEMSK15	R/W	0x378	SCT event state register 15	0x0000 0000
EVCTRL15	R/W	0x37C	SCT event control register 15	0x0000 0000
OUTPUTSET0	R/W	0x500	SCT output 0 set register	0x0000 0000
OUTPUTCL0	R/W	0x504	SCT output 0 clear register	0x0000 0000
OUTPUTSET1	R/W	0x508	SCT output 1 set register	0x0000 0000
OUTPUTCL1	R/W	0x50C	SCT output 1 clear register	0x0000 0000
OUTPUTSET2	R/W	0x510	SCT output 2 set register	0x0000 0000
OUTPUTCL2	R/W	0x514	SCT output 2 clear register	0x0000 0000
OUTPUTSET3	R/W	0x518	SCT output 3 set register	0x0000 0000
OUTPUTCL3	R/W	0x51C	SCT output 3 clear register	0x0000 0000
OUTPUTSET4	R/W	0x520	SCT output 4 set register	0x0000 0000
OUTPUTCL4	R/W	0x524	SCT output 4 clear register	0x0000 0000
OUTPUTSET5	R/W	0x528	SCT output 5 set register	0x0000 0000
OUTPUTCL5	R/W	0x52C	SCT output 5 clear register	0x0000 0000
OUTPUTSET6	R/W	0x530	SCT output 6 set register	0x0000 0000
OUTPUTCL6	R/W	0x534	SCT output 6 clear register	0x0000 0000
OUTPUTSET7	R/W	0x538	SCT output 7 set register	0x0000 0000
OUTPUTCL7	R/W	0x53C	SCT output 7 clear register	0x0000 0000
OUTPUTSET8	R/W	0x540	SCT output 8 set register	0x0000 0000
OUTPUTCL8	R/W	0x544	SCT output 8 clear register	0x0000 0000
OUTPUTSET9	R/W	0x548	SCT output 9 set register	0x0000 0000
OUTPUTCL9	R/W	0x54C	SCT output 9 clear register	0x0000 0000
OUTPUTSET10	R/W	0x550	SCT output 10 set register	0x0000 0000
OUTPUTCL10	R/W	0x554	SCT output 10 clear register	0x0000 0000
OUTPUTSET11	R/W	0x558	SCT output 11 set register	0x0000 0000
OUTPUTCL11	R/W	0x55C	SCT output 11 clear register	0x0000 0000
OUTPUTSET12	R/W	0x560	SCT output 12 set register	0x0000 0000
OUTPUTCL12	R/W	0x564	SCT output 12 clear register	0x0000 0000
OUTPUTSET13	R/W	0x568	SCT output 13 set register	0x0000 0000

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Table 499. Register overview: State Configurable Timer (base address 0x4000 0000) *…continued*

Name	Access	Address offset	Description	Reset value
OUTPUTCL13	R/W	0x56C	SCT output 13 clear register	0x0000 0000
OUTPUTSET14	R/W	0x570	SCT output 14 set register	0x0000 0000
OUTPUTCL14	R/W	0x574	SCT output 14 clear register	0x0000 0000
OUTPUTSET15	R/W	0x578	SCT output 15 set register	0x0000 0000
OUTPUTCL15	R/W	0x57C	SCT output 15 clear register	0x0000 0000

24.6.1 SCT configuration register

This register configures the overall operation of the SCT and should be written before any other registers.

Table 500. SCT configuration register (CONFIG - address 0x4000 0000) bit description

Bit	Symbol	Value	Description	Reset value
0	UNIFY		SCT operation	0
		0	The SCT operates as two 16-bit counters named L and H.	
		1	The SCT operates as a unified 32-bit counter.	
2:1	CLKMODE		SCT clock mode	00
		0x0	The SCT and prescaler(s) are clocked by the bus clock.	
		0x1	The SCT clock is the bus clock, but the prescaler(s) is (are) enabled to count only when sampling of the input selected by the CKSEL field finds the selected edge. The minimum pulse width on the clock input is 1 bus clock period. This is the high-performance sampled-clock mode.	
		0x2	The SCT and prescaler(s) are clocked by the input selected by CKSEL, synchronized to the bus clock and possibly inverted. The minimum pulse width on the clock input is 1 bus clock period. This is the low-power sampled-clock mode.	
		0x3	The SCT and prescaler(s) are clocked by the input edge selected by the CKSEL field. In this mode the following is true: Most of the SCT is clocked by the (selected polarity of the) input. Outputs are switched synchronously to the input clock. The input clock rate must be at least half the bus clock rate and can be faster than the bus clock.	

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Table 500. SCT configuration register (CONFIG - address 0x4000 0000) bit description *…continued*

Bit	Symbol	Value	Description	Reset value
6:3	CLKSEL		SCT clock select	0000
		0x0	Rising edges on input 0.	
		0x1	Falling edges on input 0.	
		0x2	Rising edges on input 1.	
		0x3	Falling edges on input 1.	
		0x4	Rising edges on input 2.	
		0x5	Falling edges on input 2.	
		0x6	Rising edges on input 3.	
		0x7	Falling edges on input 3.	
		0x8	Rising edges on input 4.	
		0x9	Falling edges on input 4.	
		0xA	Rising edges on input 5.	
		0xB	Falling edges on input 5.	
		0xC	Rising edges on input 6.	
		0xD	Falling edges on input 6.	
		0xE	Rising edges on input 7.	
		0xF	Falling edges on input 7.	
7	NORELAODL_ NORELOADU	-	A 1 in this bit prevents the lower match registers from being reloaded from their respective reload registers. Software can write to set or clear this bit at any time. This bit applies to both the higher and lower registers when the UNIFY bit is set.	0
8	NORELOADH	-	A 1 in this bit prevents the higher match registers from being reloaded from their respective reload registers. Software can write to set or clear this bit at any time. This bit is not used when the UNIFY bit is set.	0
16:9	INSYNCn	-	Synchronization for input n (bit 9 = input 0, bit 10 = input 1,..., bit 16 = input 7). A 1 in one of these bits subjects the corresponding input to synchronization to the SCT clock, before it is used to create an event. If an input is synchronous to the SCT clock, keep its bit 0 for faster response. When the CKMODE field is 1x, the bit in this field, corresponding to the input selected by the CKSEL field, is not used.	1
31:17	-		Reserved	-

24.6.2 SCT control register

If UNIFY = 1 in the CONFIG register, only the _L bits are used.

If UNIFY = 0 in the CONFIG register, this register can be written to as two registers CTRL_L (address 0x4000 4004) and CTRL_H (address 0x4000 4006). Both the L and H registers can be read or written in a single 32-bit read or write operation, or they can be read or written individually.

All bits in this register can be written to when the counter is stopped or halted. When the counter is running, the only bits that can be written are STOP or HALT. (Other bits can be written in a subsequent write after HALT is set to 1.)

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Table 501. SCT control register (CTRL - address 0x4000 0004) bit description

Bit	Symbol	Value	Description	Reset value
0	DOWN_L	-	This bit is 1 when the L or unified counter is counting down. It is set by hardware when the counter's limit is reached and BIDIR is 1. It is cleared by hardware when the counter reaches 0.	0
1	STOP_L	-	When this bit is 1 and HALT is 0, the L or unified counter does not run but I/O events related to the counter can occur. If such an event matches the mask in the Start register, this bit is cleared and counting resumes.	0
2	HALT_L	-	When this bit is 1, the L or unified counter does not run and no events can occur. This bit is set by reset. **Remark:** Once set, this bit can only be cleared by software to restore counter operation.	1
3	CLRCTR_L	-	Writing a 1 to this bit clears the L or unified counter. This bit always reads as 0.	0
4	BIDIR_L		L or unified counter direction select	0
		0	The counter counts up to its limit condition, then is cleared to zero.	
		1	The counter counts up to its limit, then counts down to 0.	
12:5	PRE_L	-	Specifies the factor by which the SCT clock is prescaled to produce the L or unified counter clock. The counter clock will be clocked at the rate of the SCT clock divided by PRE_L+1. **Remark:** Clear the counter (by writing a 1 to the CLRCTR bit) whenever changing the PRE value.	0
15:13	-		Reserved	
16	DOWN_H	-	This bit is 1 when the H counter is counting down. It is set by hardware when the counter's limit is reached and BIDIR is 1. It is cleared by hardware when the counter reaches 0.	0
17	STOP_H	-	When this bit is 1 and HALT is 0, the H counter does not run but I/O events related to the counter can occur. If such an event matches the mask in the Start register, this bit is cleared and counting resumes.	0
18	HALT_H	-	When this bit is 1, the H counter does not run and no events can occur. This bit is set by reset. **Remark:** Once set, this bit can only be cleared by software to restore counter operation.	1
19	CLRCTR_H	-	Writing a 1 to this bit clears the H counter. This bit always reads as 0.	0
20	BIDIR_H		Direction select	0
		0	The H counter counts up to its limit condition, then is cleared to zero.	
		1	The H counter counts up to its limit, then counts down to 0.	
28:21	PRE_H	-	Specifies the factor by which the SCT clock is prescaled to produce the H counter clock. The counter clock will be clocked at the rate of the SCT clock divided by PRELH+1. **Remark:** Clear the counter (by writing a 1 to the CLRCTR bit) whenever changing the PRE value.	0
31:29	-		Reserved	

24.6.3 SCT limit register

If UNIFY = 1 in the CONFIG register, only the _L bits are used.

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If UNIFY = 0 in the CONFIG register, this register can be written to as two registers LIMIT_L (address 0x4000 4008) and LIMIT_H (address 0x4000 400A). Both the L and H registers can be read or written in a single 32-bit read or write operation, or they can be read or written individually.

The bits in this register set which events act as counter limits. When a limit event occurs, the counter is cleared to zero in unidirectional mode or begins counting down in bidirectional mode. When the counter reaches all ones, this state is always treated as a limit event, and the counter is cleared in unidirectional mode or, in bidirectional mode, begins counting down on the next clock edge - even if no limit event as defined by the SCT limit register has occurred.

Table 502. SCT limit register (LIMIT - address 0x4000 0008) bit description

Bit	Symbol	Description	Reset value
15:0	LIMMSK_L	If bit n is one, event n is used as a counter limit for the L or unified counter (event 0 = bit 0, event 1 = bit 1, event 15 = bit 15).	0
31:16	LIMMSK_H	If bit n is one, event n is used as a counter limit for the H counter (event 0 = bit 16, event 1 = bit 17, event 15 = bit 31).	0

24.6.4 SCT halt condition register

If UNIFY = 1 in the CONFIG register, only the _L bits are used.

If UNIFY = 0 in the CONFIG register, this register can be written to as two registers HALT_L (address 0x4000 400C) and HALT_H (address 0x4000 400E). Both the L and H registers can be read or written in a single 32-bit read or write operation, or they can be read or written individually.

Remark: Any event halting the counter disables its operation until software clears the HALT bit (or bits) in the CTRL register (Table 501).

Table 503. SCT halt condition register (HALT - address 0x4000 000C) bit description

Bit	Symbol	Description	Reset value
15:0	HALTMSK_L	If bit n is one, event n sets the HALT_L bit in the CTRL register (event 0 = bit 0, event 1 = bit 1, event 15 = bit 15).	0
31:16	HALTMSK_H	If bit n is one, event n sets the HALT_H bit in the CTRL register (event 0 = bit 16, event 1 = bit 17, event 15 = bit 31).	0

24.6.5 SCT stop condition register

If UNIFY = 1 in the CONFIG register, only the _L bits are used.

If UNIFY = 0 in the CONFIG register, this register can be written to as two registers STOPT_L (address 0x4000 4010) and STOP_H (address 0x4000 4012). Both the L and H registers can be read or written in a single 32-bit read or write operation, or they can be read or written individually.

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Table 504. SCT stop condition register (STOP - address 0x4000 0010) bit description

Bit	Symbol	Description	Reset value
15:0	STOPMSK_L	If bit n is one, event n sets the STOP_L bit in the CTRL register (event 0 = bit 0, event 1 = bit 1, event 15 = bit 15).	0
31:16	STOPMSK_H	If bit n is one, event n sets the STOP_H bit in the CTRL register (event 0 = bit 16, event 1 = bit 17, event 15 = bit 31).	0

24.6.6 SCT start condition register

If UNIFY = 1 in the CONFIG register, only the _L bits are used.

If UNIFY = 0 in the CONFIG register, this register can be written to as two registers START_L (address 0x4000 4014) and START_H (address 0x4000 4016). Both the L and H registers can be read or written in a single 32-bit read or write operation, or they can be read or written individually.

The bits in this register select which event(s), if any, clear the STOP bit in the Control register. (Since no events can occur when HALT is 1, HALT can only be cleared by software writing the Control register.)

Table 505. SCT start condition register (START - address 0x4000 0014) bit description

Bit	Symbol	Description	Reset value
15:0	STARTMSK_L	If bit n is one, event n clears the STOP_L bit in the CTRL register (event 0 = bit 0, event 1 = bit 1, event 15 = bit 15).	0
31:16	STARTMSK_H	If bit n is one, event n clears the STOP_H bit in the CTRL register (event 0 = bit 16, event 1 = bit 17, event 15 = bit 31).	0

24.6.7 SCT counter register

If UNIFY = 1 in the CONFIG register, the counter is a unified 32-bit register and both the _L and _H bits are used.

If UNIFY = 0 in the CONFIG register, this register can be written to as two registers COUNT_L (address 0x4000 4040) and COUNT_H (address 0x4000 4042). Both the L and H registers can be read or written in a single 32-bit read or write operation, or they can be read or written individually. In this case, the L and H registers count independently under the control of the other registers.

Attempting to write a counter while it is running will not affect the counter but will produce a bus error. Software can read the counter register(s) at any time.

Table 506. SCT counter register (COUNT - address 0x4000 0040) bit description

Bit	Symbol	Description	Reset value
15:0	CTR_L	When UNIFY = 0, read or write the 16-bit L counter value. When UNIFY = 1, read or write the lower 16 bits of the 32-bit unified counter.	0
31:16	CTR_H	When UNIFY = 0, read or write the 16-bit H counter value. When UNIFY = 1, read or write the upper 16 bits of the 32-bit unified counter.	0

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24.6.8 SCT state register

If UNIFY = 1 in the CONFIG register, only the _L bits are used.

If UNIFY = 0 in the CONFIG register, this register can be written to as two registers STATE_L (address 0x4000 4044) and STATE_H (address 0x4000 4046). Both the L and H registers can be read or written in a single 32-bit read or write operation, or they can be read or written individually.

Software can read the state associated with a counter at any time. Writing the state is only allowed when the counter's HALT bit is 1; when HALT is 0, a write attempt does not change the state and results in a bus error.

The state variable is the main feature that distinguishes the SCT from other counter/timer/ PWM blocks. Events can be made to occur only in certain states. Events, in turn, can perform the following actions:

- set and clear outputs
- limit, stop, and start the counter
- cause interrupts and DMA requests
- modify the state variable

The value of a state variable is completely under the control of the application. If an application does not use states, the value of the state variable remains zero, which is the default value.

A state variable can be used to track and control multiple cycles of the associated counter in any desired operational sequence, and it is logically associated with a state machine diagram which represents the SCT configuration. See Section 24.6.23 and 24.6.24 for more about the relationship between states and events.

All possible values for the state variable are set by the STATELD/STADEV fields in the event control registers of all defined events. The change of the state variable during multiple counter cycles reflects how the associated state machine moves from one state to the next.

Table 507. SCT state register (STATE - address 0x4000 0044) bit description

Bit	Symbol	Description	Reset value
4:0	STATE_L	State variable.	0
15:5	-	Reserved.	-
20:16	STATE_H	State variable.	0
31:21	-	Reserved.	

24.6.9 SCT input register

Software can read the state of the SCT's inputs in this read-only register in two slightly different forms. The only situation in which these will differ is if CLKMODE = 2 in the CONFIG register.

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Table 508. SCT input register (INPUT - address 0x4000 0048) bit description

Bit	Symbol	Description	Reset value
0	AIN0	Real-time status of input 0.	pin
1	AIN1	Real-time status of input 1.	pin
2	AIN2	Real-time status of input 2.	pin
3	AIN3	Real-time status of input 3.	pin
4	AIN4	Real-time status of input 4.	pin
5	AIN5	Real-time status of input 5.	pin
6	AIN6	Real-time status of input 6.	pin
7	AIN7	Real-time status of input 7.	pin
15:8	-	Reserved.	-
16	SIN0	Input 0 state synchronized to the SCT clock.	-
17	SIN1	Input 1 state synchronized to the SCT clock.	-
18	SIN2	Input 2 state synchronized to the SCT clock.	-
19	SIN3	Input 3 state synchronized to the SCT clock.	-
20	SIN4	Input 4 state synchronized to the SCT clock.	-
21	SIN5	Input 5 state synchronized to the SCT clock.	-
22	SIN6	Input 6 state synchronized to the SCT clock.	-
23	SIN7	Input 7 state synchronized to the SCT clock.	-
31:24	-	Reserved	-

24.6.10 SCT match/capture registers mode register

If UNIFY = 1 in the CONFIG register, only the _L bits of this register are used, and they control whether each set of match/capture registers operate as unified 32-bit capture/match registers.

If UNIFY = 0 in the CONFIG register, this register can be written to as two registers REGMODE_L (address 0x4000 404C) and REGMODE_H (address 0x4000 404E). Both the L and H registers can be read or written in a single 32-bit read or write operation, or they can be read or written individually. The _L bits/registers control the L match/capture registers, and the _H bits/registers control the H match/capture registers.

The SCT contains 16 Match/Capture register pairs. The Register Mode register selects whether each register pair acts as a Match register (see Section 24.6.19) or as a Capture register (see Section 24.6.20). Each Match/Capture register has an accompanying register which serves as a Reload register when the register is used as a Match register (Section 24.6.21) or as a Capture-Control register when the register is used as a capture register (Section 24.6.22). REGMODE_H is used only when the UNIFY bit is 0.

An alternate addressing mode is available for all of the Match/Capture and Reload/Capture-Control registers, for DMA access to halfword registers when UNIFY=0. It is described in Section 24.7.9.

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Table 509. SCT match/capture registers mode register (REGMODE - address 0x4000 004C) bit description

Bit	Symbol	Description	Reset value
15:0	REGMOD_L	Each bit controls one pair of match/capture registers (register 0 = bit 0, register 1 = bit 1,..., register 15 = bit 15). 0 = registers operate as match registers. 1 = registers operate as capture registers.	0
31:16	REGMOD_H	Each bit controls one pair of match/capture registers (register 0 = bit 16, register 1 = bit 17,..., register 15 = bit 31). 0 = registers operate as match registers. 1 = registers operate as capture registers.	0

24.6.11 SCT output register

The SCT supports 16 outputs, each of which has a corresponding bit in this register.

Software can write to any of the output registers when both counters are halted to control the outputs directly. Writing to this register when either counter is stopped or running does not affect the outputs and results in an bus error.

Software can read this register at any time to sense the state of the outputs.

Table 510. SCT output register (OUTPUT - address 0x4000 0050) bit description

Bit	Symbol	Description	Reset value
15:0	OUT	Writing a 1 to bit n makes the corresponding output HIGH. 0 makes the corresponding output LOW (output 0 = bit 0, output 1 = bit 1,..., output 15 = bit 15).	0
31:16	-	Reserved	

24.6.12 SCT bidirectional output control register

This register specifies (for each output) the impact of the counting direction on the meaning of set and clear operations on the output (see Section 24.6.25 and Section 24.6.26).

Table 511. SCT bidirectional output control register (OUTPUTDIRCTRL - address 0x4000 0054) bit description

Bit	Symbol	Value	Description	Reset value
1:0	SETCLR0		Set/clear operation on output 0. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	
3:2	SETCLR1		Set/clear operation on output 1. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	

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Table 511. SCT bidirectional output control register (OUTPUTDIRCTRL - address 0x4000 0054) bit description

Bit	Symbol	Value	Description	Reset value
5:4	SETCLR2		Set/clear operation on output 2. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	
7:6	SETCLR3		Set/clear operation on output 3. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	
9:8	SETCLR4		Set/clear operation on output 4. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	
11:10	SETCLR5		Set/clear operation on output 5. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	
13:12	SETCLR6		Set/clear operation on output 6. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	
15:14	SETCLR7		Set/clear operation on output 7. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	
17:16	SETCLR8		Set/clear operation on output 8. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	
19:18	SETCLR9		Set/clear operation on output 9. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	
21:20	SETCLR10		Set/clear operation on output 5. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	
23:22	SETCLR11		Set/clear operation on output 11. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	

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Table 511. SCT bidirectional output control register (OUTPUTDIRCTRL - address 0x4000 0054) bit description

Bit	Symbol	Value	Description	Reset value
25: 24	SETCLR12		Set/clear operation on output 12. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	
27: 26	SETCLR13		Set/clear operation on output 13. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	
29: 28	SETCLR14		Set/clear operation on output 14. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	
31: 30	SETCLR15		Set/clear operation on output 15. Value 0x3 is reserved. Do not program this value.	0
		0x0	Set and clear do not depend on any counter.	
		0x1	Set and clear are reversed when counter L or the unified counter is counting down.	
		0x2	Set and clear are reversed when counter H is counting down. Do not use if UNIFY = 1.	

24.6.13 SCT conflict resolution register

The registers OUTPUTSETn (Section 24.6.25) and OUTPUTCLn (Section 24.6.26) allow both setting and clearing to be indicated for an output in the same clock cycle, even for the same event. This SCT conflict resolution register controls what happens when this occurs.

To enable an event to toggle an output, set the OnRES value to 0x3 in this register, and set the event's bits in both the Set and Clear registers.

Table 512. SCT conflict resolution register (RES - address 0x4000 0058) bit description

Bit	Symbol	Value	Description	Reset value
1:0	O0RES		Effect of simultaneous set and clear on output 0.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR0 field).	
		0x2	Clear output (or set based on the SETCLR0 field).	
		0x3	Toggle output.	
3:2	O1RES		Effect of simultaneous set and clear on output 1.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR1 field).	
		0x2	Clear output (or set based on the SETCLR1 field).	
		0x3	Toggle output.	

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Table 512. SCT conflict resolution register (RES - address 0x4000 0058) bit description

Bit	Symbol	Value	Description	Reset value
5:4	O2RES		Effect of simultaneous set and clear on output 2.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR2 field).	
		0x2	Clear output n (or set based on the SETCLR2 field).	
		0x3	Toggle output.	
7:6	O3RES		Effect of simultaneous set and clear on output 3.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR3 field).	
		0x2	Clear output (or set based on the SETCLR3 field).	
		0x3	Toggle output.	
9:8	O4RES		Effect of simultaneous set and clear on output 4.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR4 field).	
		0x2	Clear output (or set based on the SETCLR4 field).	
		0x3	Toggle output.	
11:10	O5RES		Effect of simultaneous set and clear on output 5.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR5 field).	
		0x2	Clear output (or set based on the SETCLR5 field).	
		0x3	Toggle output.	
13:12	O6RES		Effect of simultaneous set and clear on output 6.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR6 field).	
		0x2	Clear output (or set based on the SETCLR6 field).	
		0x3	Toggle output.	
15:14	O7RES		Effect of simultaneous set and clear on output 7.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR7 field).	
		0x2	Clear output (or set based on the SETCLR7 field).	
		0x3	Toggle output.	
17:16	O8RES		Effect of simultaneous set and clear on output 8.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR8 field).	
		0x2	Clear output (or set based on the SETCLR8 field).	
		0x3	Toggle output.	
19:18	O9RES		Effect of simultaneous set and clear on output 9.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR9 field).	
		0x2	Clear output (or set based on the SETCLR9 field).	
		0x3	Toggle output.	

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Table 512. SCT conflict resolution register (RES - address 0x4000 0058) bit description

Bit	Symbol	Value	Description	Reset value
21: 20	O10RES		Effect of simultaneous set and clear on output 10.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR10 field).	
		0x2	Clear output (or set based on the SETCLR10 field).	
		0x3	Toggle output.	
23: 22	O11RES		Effect of simultaneous set and clear on output 11.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR11 field).	
		0x2	Clear output (or set based on the SETCLR11 field).	
		0x3	Toggle output.	
25: 24	O10RES		Effect of simultaneous set and clear on output 12.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR12 field).	
		0x2	Clear output (or set based on the SETCLR12 field).	
		0x3	Toggle output.	
27: 26	O13RES		Effect of simultaneous set and clear on output 13.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR13 field).	
		0x2	Clear output (or set based on the SETCLR13 field).	
		0x3	Toggle output.	
29: 28	O14RES		Effect of simultaneous set and clear on output 14.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR14 field).	
		0x2	Clear output (or set based on the SETCLR14 field).	
		0x3	Toggle output.	
31: 30	O15RES		Effect of simultaneous set and clear on output 15.	0
		0x0	No change.	
		0x1	Set output (or clear based on the SETCLR15 field).	
		0x2	Clear output (or set based on the SETCLR15 field).	
		0x3	Toggle output.	

24.6.14 SCT DMA request 0 and 1 registers

The SCT includes two DMA request outputs. These registers enable the DMA requests to be triggered when a particular event occurs or when a counter’s Match registers are loaded from its Reload registers.

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Table 513. SCT DMA 0 request register (DMAREQ0 - address 0x4000 005C) bit description

Bit	Symbol	Description	Reset value
15:0	DEV_0	If bit n is one, event n sets DMA request 0 (event 0 = bit 0, event 1 = bit 1,..., event 15 = bit 15).	0
29:16	-	Reserved	-
30	DRL0	A 1 in this bit makes the SCT set DMA request 0 when it loads the Match_L/Unified registers from the Reload_L/Unified registers.	
31	DRQ0	This read-only bit indicates the state of DMA Request 0	

Table 514. SCT DMA 1 request register (DMAREQ1 - address 0x4000 0060) bit description

Bit	Symbol	Description	Reset value
15:0	DEV_1	If bit n is one, event n sets DMA request 1 (event 0 = bit 0, event 1 = bit 1,..., event 15 = bit 15).	0
29:16	-	Reserved	-
30	DRL1	A 1 in this bit makes the SCT set DMA request 1 when it loads the Match L/Unified registers from the Reload L/Unified registers.	
31	DRQ1	This read-only bit indicates the state of DMA Request 1.	

24.6.15 SCT flag enable register

This register enables flags to request an interrupt if the FLAGn bit in the SCT event flag register (Section 24.6.16) is also set.

Table 515. SCT flag enable register (EVEN - address 0x4000 00F0) bit description

Bit	Symbol	Description	Reset value
15:0	IEN	The SCT requests interrupt when bit n of this register and the event flag register are both one (event 0 = bit 0, event 1 = bit 1,..., event 15 = bit 15).	0
31:16	-	Reserved	

24.6.16 SCT event flag register

This register records events. Writing ones to this register clears the corresponding flags and will negate the SCT interrupt request if all enabled Flag bits are zero.

Table 516. SCT event flag register (EVFLAG - address 0x4000 00F4) bit description

Bit	Symbol	Description	Reset value
15:0	FLAG	Bit n is one if event n has occurred since reset or a 1 was last written to this bit (event 0 = bit 0, event 1 = bit 1,..., event 15 = bit 15).	0
31:16	-	Reserved	-

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24.6.17 SCT conflict enable register

This register enables the “no change conflict” events specified in the SCT conflict resolution register to request an IRQ.

Table 517. SCT conflict enable register (CONEN - address 0x4000 00F8) bit description

Bit	Symbol	Description	Reset value
15:0	NCEN	The SCT requests interrupt when bit n of this register and the SCT conflict flag register are both one (output 0 = bit 0, output 1 = bit 1,..., output 15 = bit 15).	0
31:16	-	Reserved	

24.6.18 SCT conflict flag register

This register records interrupt-enabled no-change conflict events and provides details of a bus error. Writing ones to the NCFLAG bits clears the corresponding read bits and will negate the SCT’s interrupt request if all enabled Flag bits are then zero.

Table 518. SCT conflict flag register (CONFLAG - address 0x4000 00FC) bit description

Bit	Symbol	Description	Reset value
15:0	NCFLAG	Bit n is one if a no-change conflict event occurred on output n since reset or a 1 was last written to this bit (output 0 = bit 0, output 1 = bit 1,..., output 15 = bit 15).	0
29:16	-	Reserved.	-
30	BUSERRL	The most recent bus error from this SCT involved writing CTR L/Unified, STATE L/Unified, MATCH L/Unified, or the Output register when the L/U counter was not halted. Note that a word write to certain L and H registers can be half successful and half unsuccessful.	0
31	BUSERRH	The most recent bus error from this SCT involved writing CTR H, STATE H, MATCH H, or the Output register when the H counter was not halted.	0

24.6.19 SCT match registers 0 to 15 (REGMODEn bit = 0)

Match registers are compared to the counter(s) to help create events. When the UNIFY bit is 0, the L and H registers are independently compared to the L and H counters. When UNIFY is 1, the L and H registers hold a 32-bit value that is compared to the unified counter. A Match can only occur in a clock in which the counter is running (STOP and HALT are both 0).

Match registers can be read at any time. Writing to a Match register while the associated counter is running will not affect the Match register and will result in an bus error. Match events occur in the SCT clock in which the counter is (or would be) incremented to the next value. When a Match event limits its counter as described in Section 24.6.3, the value in the Match register is the last value of the counter before it is cleared to zero (or decremented if BIDIR is 1).

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There is no “write-through” from Reload registers to Match registers. Before starting a counter, software can write one value to the Match register that will be used in the first cycle of the counter, and a different value to the corresponding Match Reload register that will be used in the second cycle.

Table 519. SCT match registers 0 to 15 (MATCH - address 0x4000 0100 (MATCH0) to 0x4000 4013C (MATCH15)) bit description (REGMODEn bit = 0)

Bit	Symbol	Description	Reset value
15:0	MATCHn_L	When UNIFY = 0, read or write the 16-bit value to be compared to the L counter. When UNIFY = 1, read or write the lower 16 bits of the 32-bit value to be compared to the unified counter.	0
31:16	MATCHn_H	When UNIFY = 0, read or write the 16-bit value to be compared to the H counter. When UNIFY = 1, read or write the upper 16 bits of the 32-bit value to be compared to the unified counter.	0

24.6.20 SCT capture registers 0 to 15 (REGMODEn bit = 1)

These register(s) allow software to read the counter value(s) at which the event selected by the corresponding Capture Control register(s) occurred.

Table 520. SCT capture registers 0 to 15 (CAP - address 0x4000 0100 (CAP0) to 0x4000 013C (CAP15)) bit description (REGMODEn bit = 1)

Bit	Symbol	Description	Reset value
15:0	CAPn_L	When UNIFY = 0, read the 16-bit counter value at which this register was last captured. When UNIFY = 1, read the lower 16 bits of the 32-bit value at which this register was last captured.	0
31:16	CAPn_H	When UNIFY = 0, read the 16-bit counter value at which this register was last captured. When UNIFY = 1, read the upper 16 bits of the 32-bit value at which this register was last captured.	0

24.6.21 SCT match reload registers 0 to 15 (REGMODEn bit = 0)

A Match register (L, H, or unified 32-bit) is loaded from the corresponding Reload register when BIDIR is 0 and the counter reaches its limit condition, or when BIDIR is 1 and the counter reaches 0.

Table 521. SCT match reload registers 0 to 15 (MATCHREL- address 0x4000 0200 (MATCHRELOAD0) to 0x4000 023C (MATCHRELOAD15) bit description (REGMODEn bit = 0)

Bit	Symbol	Description	Reset value
15:0	RELOADn_L	When UNIFY = 0, read or write the 16-bit value to be loaded into the SCTMATCHn_L register. When UNIFY = 1, read or write the lower 16 bits of the 32-bit value to be loaded into the MATCHn register.	0
31:16	RELOADn_H	When UNIFY = 0, read or write the 16-bit to be loaded into the MATCHn_H register. When UNIFY = 1, read or write the upper 16 bits of the 32-bit value to be loaded into the MATCHn register.	0

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24.6.22 SCT capture control registers 0 to 15 (REGMODEn bit = 1)

If UNIFY = 1 in the CONFIG register, only the _L bits are used.

If UNIFY = 0 in the CONFIG register, this register can be written to as two registers CAPCTRLn_L (address 0x4000 4100 to 0x4000 413C) and CAPCTRLn_H (address 0x4000 4102 to 0x4000 413E). Both the L and H registers can be read or written in a single 32-bit read or write operation, or they can be read or written individually.

Each Capture Control register (L, H, or unified 32-bit) controls which events load the corresponding Capture register from the counter.

Table 522. SCT capture control registers 0 to 15 (CAPCTRL- address 0x4000 0200 (CAPCTRL0) to 0x4000 023C (CAPCTRL15)) bit description (REGMODEn bit = 1)

Bit	Symbol	Description	Reset value
15:0	CAPCONn_L	If bit m is one, event m causes the CAPn_L (UNIFY = 0) or the CAPn (UNIFY = 1) register to be loaded (event 0 = bit 0, event 1 = bit 1,..., event 15 = bit 15).	0
31:16	CAPCONn_H	If bit m is one, event m causes the CAPn_H (UNIFY = 0) register to be loaded (event 0 = bit 16, event 1 = bit 17,..., event 15 = bit 31).	0

24.6.23 SCT event state mask registers 0 to 15

Each event has one associated SCT event state mask register that allow this event to happen in one or more states of the counter selected by the HEVENT bit in the corresponding EVCTRLn register.

An event n is disabled when its EVSTATEMSKn register contains all zeros, since it is masked regardless of the current state.

In simple applications that don’t use states, write 0x01 to this register to enable an event. Since the state will always remain at its reset value of 0, this effectively permanently state-enables this event.

Table 523. SCT event state mask registers 0 to 15 (EVSTATEMSK - addresses 0x4000 0300 (EVSTATEMSK0) to 0x4000 0378 (EVSTATEMSK15)) bit description

Bit	Symbol	Description	Reset value
31:0	STATEMSKn	If bit m is one, event n (n= 0 to 15) happens in state m of the counter selected by the HEVENT bit (m = state number; state 0 = bit 0, state 1= bit 1,..., state 31 = bit 31).	0

24.6.24 SCT event control registers 0 to 15

This register defines the conditions for event n to occur, other than the state variable which is defined by the state mask register above. Most events are associated with a particular counter (high, low, or unified), in which case the event can depend on a match to that register. The other possible ingredient of an event is a selected input or output signal.

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When the UNIFY bit is 0, each event is associated with a particular counter by the HEVENT bit in its event control register. An event can not occur when its related counter is halted nor when the current state is not enabled to cause the event as specified in its event mask register. Note that an event is permanently disabled when its event state mask register contains all 0s.

An enabled event can be programmed to occur based on a selected input or output edge or level and/or based on its counter value matching a selected match register.

Each event can modify its counter's STATE value. If more than one event associated with the same counter occurs in a given clock cycle, only the state change specified for the highest-numbered event among them takes place. Other actions dictated by any simultaneously occurring events will all take place.

Table 524. SCT event control register 0 to 15 (EVCTRL - address 0x4000 0304 (EVCTRL0) to 0x4000 037C (EVCTRL15)) bit description

Bit	Symbol	Value	Description	Reset value
3:0	MATCHSEL	-	Selects the Match register associated with this event (if any). A match can occur only when the counter selected by the HEVENT bit is running.	0
4	HEVENT		Select L/H counter. Do not set this bit if UNIFY = 1.	0
		0	Selects the L state and the L match register selected by MATCHSEL.	
		1	Selects the H state and the H match register selected by MATCHSEL.	
5	OUTSEL		Input/output select	0
		0	Selects the output selected by IOSEL.	
		1	Selects the input selected by IOSEL.	
9:6	IOSEL	-	Selects the input or output signal associated with this event (if any). If CKMODE is 1x, the clock input is an implicit ingredient of every event, and should not be selected in this register.	0
11:10	IOCOND		Selects the I/O condition for event n. (Note that the detection of edges on outputs will lag the conditions that switch the outputs by one SCT clock). An input must have a minimum pulse width of at least one SCT clock period in order to guarantee proper edge/state detection.	0
		0x0	LOW	
		0x1	Rise	
		0x2	Fall	
		0x3	HIGH	
13:12	COMBMODE		Selects how the specified match and I/O condition are used and combined.	
		0x0	OR. The event occurs when either the specified match or I/O condition occurs.	
		0x1	MATCH. Uses the specified match only.	
		0x2	IO. Uses the specified I/O condition only.	
		0x3	AND. The event occurs when the specified match and I/O condition occur simultaneously.	

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Table 524. SCT event control register 0 to 15 (EVCTRL - address 0x4000 0304 (EVCTRL0) to 0x4000 037C (EVCTRL15)) bit description

Bit	Symbol	Value	Description	Reset value
14	STATELD		This bit controls how the STATEV value modifies the state selected by HEVENT when this event is the highest-numbered event occurring for that state.	
		0	STATEV value is added into STATE (the carry-out is ignored).	
		1	STATEV value is loaded into STATE.	
19:15	STATEV		This value is loaded into or added to the state selected by HEVENT, depending on STATELD, when this event is the highest-numbered event occurring for that state. If STATELD and STATEV are both zero, there is no change to the STATE value.	
31:20	-		Reserved	

24.6.25 SCT output set registers 0 to 15

Each output n has one set register that controls how events effect each output. Whether outputs are set or cleared depends on the setting of the SETCLRn field in the SCTOUTPUTDIRCTRL register.

Table 525. SCT output set register 0 to 15 (OUTPUTSET - address 0x4000 0500 (OUTPUTSET0) to 0x4000 0578 (OUTPUTSET15)) bit description

Bit	Symbol	Description	Reset value
15:0	SET	A 1 in bit m selects event m to set output n (or clear it if SETCLRn = 0x1 or 0x2) event 0 = bit 0, event 1 = bit 1,..., event 15 = bit 15.	0
31:16	-	Reserved	

24.6.26 SCT output clear registers 0 to 15

Each output n has one clear register that controls how events effect each output. Whether outputs are set or cleared depends on the setting of the SETCLRn field in the OUTPUTDIRCTRL register.

Table 526. SCT output set register 0 to 15 (OUTPUTCL - address 0x4000 0504 (OUTPUTCL0) to 0x4000 057C (OUTPUTCL15)) bit description

Bit	Symbol	Description	Reset value
15:0	CLR	A 1 in bit m selects event m to clear output n (or set it if SETCLRn = 0x1 or 0x2) event 0 = bit 0, event 1 = bit 1,..., event 15 = bit 15.	0
31:16	-	Reserved	

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24.7 Functional description

24.7.1 Match logic

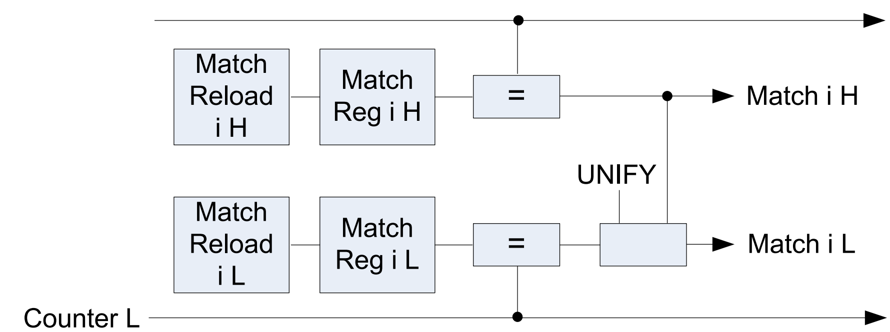


Fig 64. Match logic

24.7.2 Capture logic

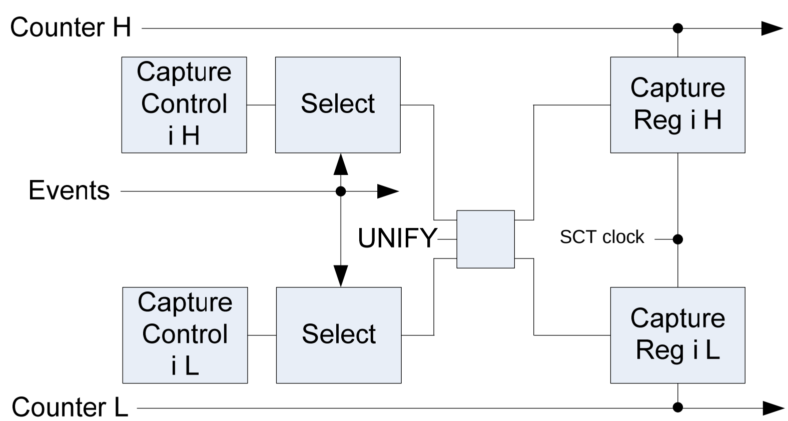


Fig 65. Capture logic

24.7.3 Event selection

State variable(s) allow control of the SCT across more than one cycle of the counter. Counter matches, input/output edges, and state values are combined into a set of general purpose events that can switch outputs, request interrupts, and change state values.

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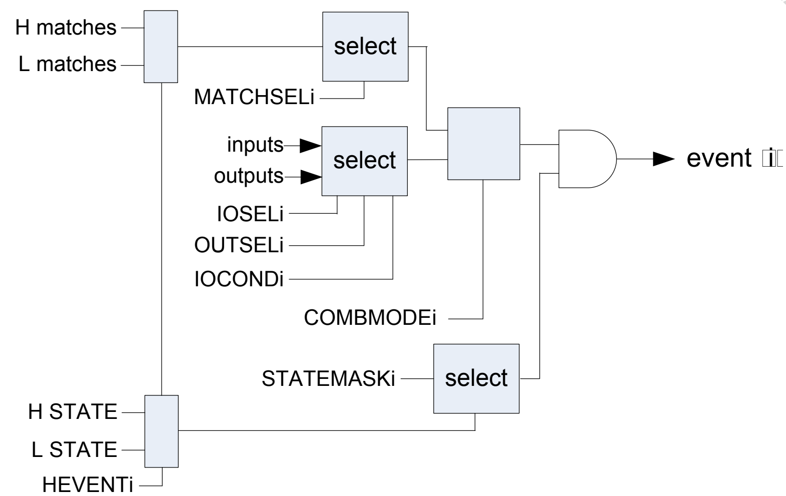


Fig 66. Event selection

24.7.4 Output generation

Figure 67 shows one output slice of the SCT.

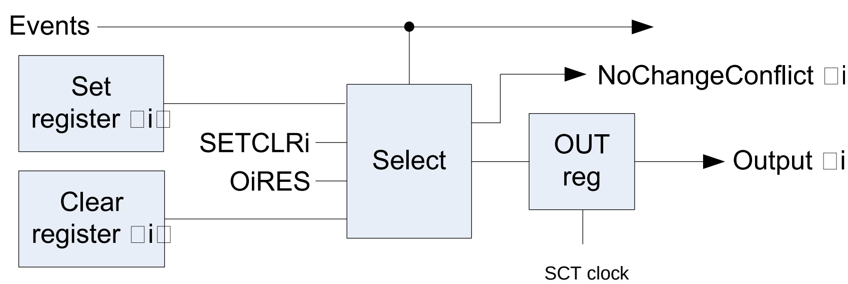


Fig 67. Output slice i

24.7.5 Interrupt generation

The SCT generates one interrupt to the NVIC.

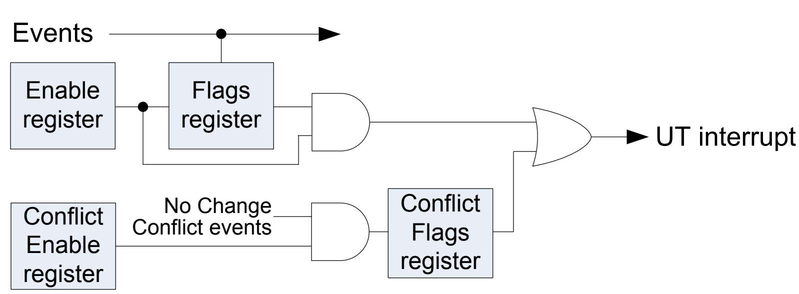


Fig 68. SCT interrupt generation

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24.7.6 Clearing the prescaler

When enabled by a non-zero PRE field in the Control register, the prescaler acts as a clock divider for the counter, like a fractional part of the counter value. The prescaler is cleared whenever the counter is cleared or loaded for any of the following reasons:

- Hardware reset
- Software writing to the counter register
- Software writing a 1 to the CLRCTR bit in the control register
- an event selected by a 1 in the counter's limit register when BIDIR = 0

When BIDIR is 0, a limit event caused by an I/O signal can clear a non-zero prescaler, but a limit event caused by a Match will only clear a non-zero prescaler in one special case as described Section 24.7.7.

A limit event when BIDIR is 1 does not clear the prescaler. Rather it clears the DOWN bit in the Control register, and decrements the counter on the same clock if the counter is enabled in that clock.

24.7.7 Match vs. I/O events

Counter operation is complicated by the prescaler, and by clock mode 01 in which the SCT clock is the bus clock, but the prescaler and counter are enabled to count only when a selected edge is detected on a clock input.

- The prescaler is enabled when the clock mode is not 01, or when the input edge selected by the CLKSEL field is detected.
- The counter is enabled when the prescaler is enabled, and (PRELIM=0 or the prescaler is equal to the value in PRELIM).

An I/O component of an event can occur in any SCT clock when its counter's HALT bit is 0. In general a Match component of an event can only occur in a UT clock when its counter's HALT and STOP bits are both 0 and the counter is enabled.

Table 527 shows when the various kinds of events can occur.

Table 527. Event conditions

COMBMODE	IOMODE	Event can occur on clock:
IO	Any	Event can occur whenever HALT = 0 (type A).
MATCH	Any	Event can occur when HALT = 0 and STOP = 0 and the counter is enabled (type C).
OR	Any	From the IO component: Event can occur whenever HALT = 0 (A). From the match component: Event can occur when HALT = 0 and STOP = 0 and the counter is enabled (C).
AND	LOW or HIGH	Event can occur when HALT = 0 and STOP = 0 and the counter is enabled (C).
AND	RISE or FALL	Event can occur whenever HALT = 0 (A).

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24.7.8 DMA operation

A DMA controller can be used to write one or more Reload registers, or read one or more Capture registers, typically at the start of a counter cycle. DMA access to more than one Reload or Capture register requires that they be consecutive registers. (Nothing else in the SCT constrains how these registers are assigned and used.)

A DMA request can be set by an event or when a counter's Match registers are loaded from its Reload registers, as described in Section 24.6.14. The SCT's two requests can be used to do the same kind of register access for both counters when UNIFY is 0, or one request can be used for writing Reload registers and the other for reading Capture registers.

The SCT does not know how many transfers should be done for each request, so it cannot control its DMA requests accordingly.

The two DMA requests are connected to DMABREQ7 and DMABREQ8. The number of registers to be transferred for each request should be written to the TransferSize field in the Channel Control Register of the DMA channel to which the request is connected. If the Linked List feature is used, there is a TransferSize value in each Linked List entry. The GPDMA asserts the DMACCLR signal when that number of transfers has been completed, which makes the SCT clear the request.

24.7.9 Alternate addressing for match/capture registers

The Match, Reload, Capture, and Capture Control registers are arranged as consecutive words, with the standard division of each word into two halfwords. When the UNIFY bit is zero, these two halfwords are related to the L and H counters. Software has the option of writing words initially to set up both halves of a SCT simultaneously, or writing halfwords to set up each half separately.
Applications can use a DMA controller to write Reload registers or to read Capture registers. However, when UNIFY is 0, the addressing of the halfword registers is not compatible with many DMA controllers' requirement to use consecutive addresses for sequential-address operation. Table 528 shows how the second half of the range occupied by each type of register contains an alternate address map for halfword accesses to the same registers, which is compatible with such DMA controllers. When UNIFY is 1, DMA word accesses should be done using standard offsets.

Table 528. Alternate address map for DMA halfword access

Match register	Capture register	Standard offset	DMA halfword offset
MATCH0_L	CAP0_L	0x100	0x180
MATCH0_H	CAP0_H	0x102	0x1C0
MATCH1_L	CAP1_L	0x104	0x182
MATCH1_H	CAP1_H	0x106	0x1C2
...	...	...	...
MATCHREL0_L	CAPCTRL0_L	0x200	0x280
MATCHREL0_H	CAPCTRL0_H	0x202	0x2C0
MATCHREL1_L	CAPCTRL1_L	0x204	0x282
MATCHREL1_H	CAPCTRL1_H	0x206	0x2C2
...	...	...	...

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24.7.10 SCT operation

In its simplest, single-state configuration, the SCT operates as an event controlled uni- or bidirectional counter. Events can be configured to be counter match events, an input or output level, transitions on an input or output pin, or a combination of match and input/output behavior. In response to an event, the SCT's output or outputs can transition or the SCT can perform other actions such as creating an interrupt or starting, stopping, or resetting the counter. Multiple simultaneous actions are allowed for each event. Furthermore, one specific action of the SCT can be triggered by any number of events.

An event is defined uniquely by an action or multiple actions of the SCT. A state is defined by which events are enabled to trigger an SCT action or actions in any stage of the counter. Events not selected for this state are ignored.

In a multi-state configuration, states change in response to events. A state change is an additional action that the SCT can perform when the event occurs. When an event is configured to change the state, the new state defines a new set of events resulting in different actions of the SCT. Through multiple cycles of the counter, events can change the state multiple times and thus create a large variety of event controlled transitions on the SCT's outputs and/or interrupts.

Once configured, the SCT can run continuously without software intervention and can generate multiple output patterns entirely under the control of events.

- To configure the SCT, see Section 24.7.10.1.
- To start, run, and stop the SCT, see Section 24.7.10.2.
- To configure the SCT without in using multiple states as simple event controlled counter/timer, see Section 24.7.10.3.

24.7.10.1 Configure the SCT

To set up the SCT for multiple events and states perform the following configuration steps:

24.7.10.1.1 Configure the counter

1. Configure the L and H counters in the CONFIG register by selecting two independent 16-bit counters (L counter and H counter) or one combined 32-bit counter in the UNIFY field.
2. Select the SCT clock source in the CONFIG register (fields CLKMODE and CLKSEL) from any of the inputs or an internal clock.

24.7.10.1.2 Configure the match and capture registers

1. Select how many match and capture registers are needed by the application (total of up to 16):
   – In the REGMODE register, select for each of the 16 match/capture register pairs whether the register is used as a match register or capture register.
2. Define match conditions for each match register selected:
   – Each match register MATCH allows to set one match value if a 32-bit counter is used or two match values if the L and H 16-bit counters are used.

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- Each match reload register MATCHRELOAD allows to set a reload value that is loaded into the match register when the counter reaches a limit condition or the value 0.

24.7.10.1.3 Configure events and event responses

1. Define when each event can occur in the following way in the EVCTRL registers (up to 16, one register per event):
   - Select whether the event occurs on an input or output changing, on an input or output level, a match condition of the counter, or a combination of match and input/output conditions in field COMBMODE.
   - For a match condition:

     Select the match register that contains the match condition for the event to occur. Enter the number of the selected match register in field MATCHSEL.

     If using L and H counters, define whether the event occurs on matching the L or the H counter in field HEVENT.
   - For an SCT input or output level or transition:

     Select the input number or the output number that is associated with this event in fields IOSEL and OUTSEL.

     Define how the selected input or output triggers the event (edge or level sensitive) in field IOCOND.
2. Define what the effect of each event is on the SCT's outputs in the OUTPUTSET or OUTPUTCLR registers (up to 16 outputs, one register per output):
   - For each SCT output, select which events set or clear this output. An output can be changed by more than one event, and each event can change multiple outputs.
3. Define how each event affects the counter:
   - Set the corresponding event bit in the LIMIT register for the event to set an upper limit for the counter.

     When a limit event occurs in unidirectional mode, the counter is cleared to zero and begins counting up on the next clock edge.

     When a limit event occurs in bidirectional mode, the counter begins to count down from the current value on the next clock edge.
   - Set the corresponding event bit in the HALT register for the event to halt the counter. If the counter is halted, it stops counting and no new events can occur. The counter operation can only be restored by clearing the HALT_L and/or the HALT_H bits in the CTRL register.
   - Set the corresponding event bit in the STOP register for the event to stop the counter. If the counter is stopped, it stops counting but can be restarted by an event that is configured as an transition on an input/output.
   - Set the corresponding event bit in the START register for the event to restart the counting. Only events that are defined by an input changing can be used to restart the counter.
4. Define which events contribute to the SCT interrupt:
   - Set the corresponding event bit in the EVEN and the EVFLAG registers to enable the event to contribute to the SCT interrupt.
5. Define whether an event triggers a DMA request.

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– Set the corresponding event bit in the DMAREQ0/1 registers for the event to trigger DMA requests 0 or 1.

24.7.10.1.4 Configure multiple states

1. In the EVSTATEMASK register for each event (up to 16 events, one register per event), select the state or states (up to 31) this event is allowed to occur in. Each state can be selected for more than one event.
2. Determine how the event affects the system's state:

   In the EVCTRL registers (up to 16 events, one register per event), set the new state value in the STATEV field for this event. If the event is the highest numbered in the current state, this value is either added to the existing state value or replaces the existing state value, depending on the field STATELD.

   Remark: If there are higher numbered events in the current state, the state cannot be changed by this event.

   If the STATEV and STATELD values are set to zero, the state does not change.

24.7.10.1.5 Miscellaneous options

- There are a certain (selectable) number of capture registers. Each capture register can be programmed to capture the counter contents when one or more events occur.
- If the counter is in bidirectional mode, the effect of set and clear of an output can be made to depend on whether the counter is counting up or down by writing to the OUTPUTDIRCTRL register.
-

24.7.10.2 Operate the SCT

1. Configure the SCT (see Section 24.7.10.1 "Configure the SCT").
   a. Configure the counter (see Section 24.7.10.1.1).
   b. Configure the match and capture registers (see Section 24.7.10.1.2).
   c. Configure the events and event responses (see Section 24.7.10.1.3).
   d. Configure multiple states (Section 24.7.10.1.4).
2. Write to the STATE register to define the initial state. By default this is state 0.
3. To start the SCT, write to the CTRL register:
   – Clear the counters.
   – Clear or set the STOP_L and/or STOP_H bits.

     Remark: The counter starts counting once the STOP bit is cleared as well. If the STOP bit is set, the SCT will wait instead for an event to occur that is configured to start the counter.
   – For each counter select unidirectional or bidirectional counting mode (field BIDIR_L and/or BIDIR_H).
   – Select the prescale factor for the counter clock (CTRL register).
   – Clear the HALT_L and/or HALT_H bit. By default, the counters are halted and no events can occur.
4. To stop the counters by software at any time, stop or halt the counter (write to STOP_L and/or STOP_H bits or HALT_L and/or HALT_H bits in the CTRL register).

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– When the counters are stopped, both an event configured to clear the STOP bit or software writing a zero to the STOP bit can start the counter again.
– When the counter are halted, only a software write to clear the HALT bit can start the counter again. No events can occur.
– When the counters are halted, software can set any SCT output HIGH or LOW directly by writing to the OUT register.

The current state can be read at any time by reading the STATE register.

To change the current state by software (that is independently of any event occurring), set the HALT bit and write to the STATE register to change the state value. Writing to the STATE register is only allowed when the counter is halted (the HALT_L and/or HALT_H bits are set) and no events can occur.

24.7.10.3 Configure the SCT without using states

The SCT can be used as standard counter/timer with external capture inputs and match outputs without using the state logic. To operate the SCT without states, configure the SCT as follows:

- Write zero to the STATE register (this is the default).
- Write zero to the STATELD and STATEV fields in the EVCTRL registers for each event.
- Write 0x1 to the EVSTATEMASK register of each event. This enables the event.

  In effect, the event is allowed to occur in a single state which never changes while the counter is running.

24.7.10.4 Example

Figure 69 shows a simple application of the SCT using two sets of match events (EV0/1 and EV3/4) to set/clear SCT output 0. A third match event (EV2) is used to reset the counter regardless of the current state.

In the initial state 0, match event EV0 causes the output 0 to be set to HIGH and match event EV1 causes output 0 to be cleared. The SCT input 0 is monitored: If the input transitions from HIGH to LOW (EV2), the state is changed to state 1, and EV3/4 are enabled, which create the same output but triggered by different match values. If input 0 transitions from LOW to HIGH, the associated event (EV5) causes the state to change back to state 0. In state 0, the events EV0 and EV1 are enabled.

The example uses the following SCT configuration:

- 1 input
- 1 output
- 5 match registers
- 7 events
- 2 states

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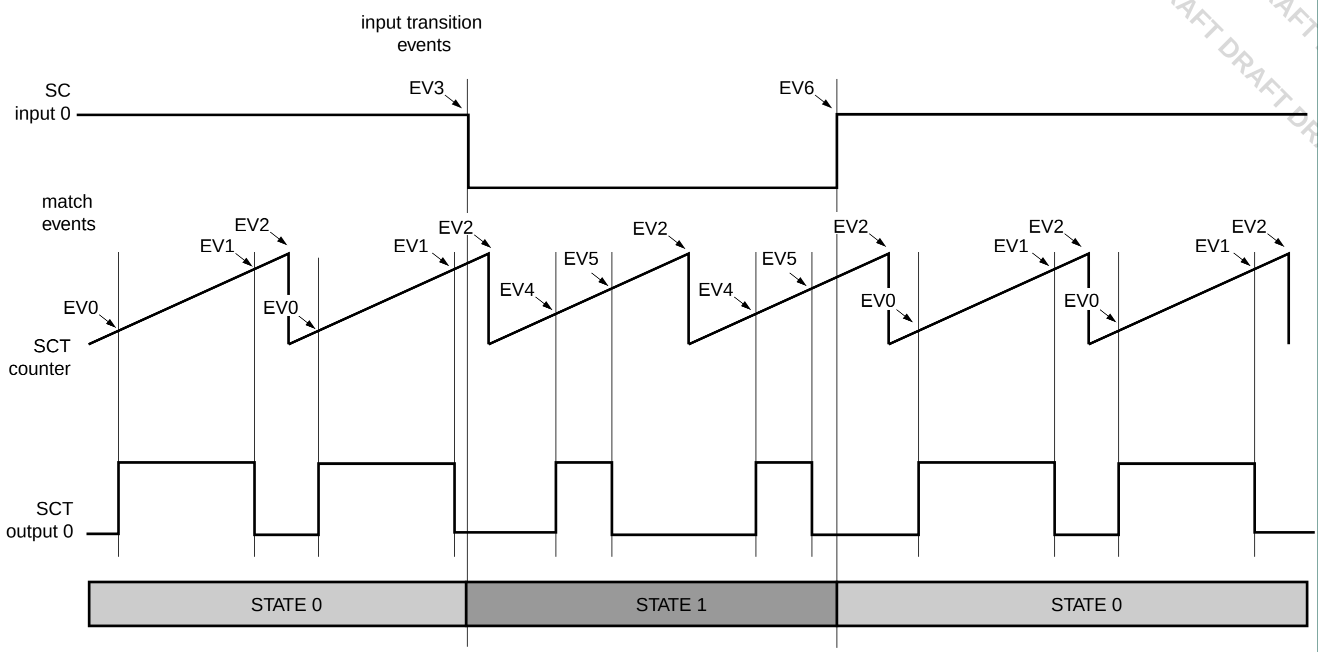


Fig 69. SCT configuration example

This application of the SCT uses the following configuration (all register values not listed in Table 529 are set to their default values):

Table 529. SCT configuration example

Configuration	Register(s)	Setting
Counter	CONFIG	Uses one counter (UNIFY = 1).
	CTRL	Uses unidirectional counter (BIDIR_L = 0).
Clock base	CONFIG	Uses default values for clock configuration.
Match/Capture registers	REGMODE	Configure one match register for each match event by setting REGMODE_L bits 0,1, 2, 4, 5 to 0. This is the default.
Define match values	MATCH0/1/2/4/5	Set a match value MATCH0/1/2/4/5_L in each register.
Define match reload values	MATCHREL0/1/2/4/5	Set a match reload value RELOAD0/1/2/4/5_L in each register (same as the match value in this example).
Define when event 0 occurs	EVCTRL0	• Set COMBMODE = 0x1. Event 0 uses match condition only. • Set MATCHSEL = 0. Select match value of match register 0.
Define when event 1 occurs	EVCTRL1	• Set COMBMODE = 0x1. Event 1 uses match condition only. • Set MATCHSEL = 1. Select match value of match register 1.
Define when event 2 occurs	EVCTRL2	• Set COMBMODE = 0x1. Event 2 uses match condition only. • Set MATCHSEL = 2. Select match value of match register 2.
Define when event 3 occurs	EVCTRL3	• Set COMBMODE = 0x2. Event 3 uses I/O condition only. • Set IOSEL = 0. Select input 0. • Set IOCOND = 0x2. Input 0 goes LOW.
Define how event 3 changes the state	EVCTRL3	Set STATEV bits to 1 and the STATED bit to 1. Event 3 changes the state to state 1.

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Table 529. SCT configuration example

Configuration	Register(s)	Setting
Define when event 4 occurs	EVCTRL4	• Set COMBMODE = 0x1. Event 4 uses match condition only. • Set MATCHSEL = 0x3. Select match value of match register 4.
Define when event 5 occurs	EVCTRL5	• Set COMBMODE = 0x1. Event 5 uses match condition only. • Set MATCHSEL = 0x3. Select match value of match register 5.
Define when event 6 occurs	EVCTRL6	• Set COMBMODE = 0x2. Event 6 uses I/O condition only. • Set IOSEL = 0. Select input 0. • Set IOCOND = 0x1. Input 0 goes HIGH.
Define how event 6 changes the state	EVCTRL6	Set STATEV bits to 0 and the STATED bit to 1. Event 6 changes the state to state 0.
Define by which events output 0 is set	OUTPUTSET0	Set SET0 bits 0 (for event 0) and 4 (for event 4) to one to set the output when these events 0 and 4 occur.
Define by which events output 0 is cleared	OUTPUTCLR0	Set CLR0 bits 1 (for events 1) and 5 (for event 5) to one to clear the output when events 1 and 5 occur.
Define which event resets the counter	LIMIT	Set LIMMASK_L bit 2 to 1 (for event 2 to limit the counter). Set all other bits to zero.
Configure states event 0 is enabled	EVSTATEMSK0	Set STATEMSK0 bit 0 to 1. Set all other bits to 0. Event 0 is enabled in state 0.
Configure states event 1 is enabled	EVSTATEMSK1	Set STATEMSK1 bit 0 to 1. Set all other bits to 0. Event 1 is enabled in state 0.
Configure states event 2 is enabled	EVSTATEMSK2	Set STATEMSK2 bit 0 to 1 and bit 1 to 1. Set all other bits to 0. Event 2 is enabled in state 0 and state 1.
Configure states event 3 is enabled	EVSTATEMSK3	Set STATEMSK3 bit 0 to 1. Set all other bits to 0. Event 3 is enabled in state 0.
Configure states event 4 is enabled	EVSTATEMSK4	Set STATEMSK4 bit 1 to 1. Set all other bits to 0. Event 4 is enabled in state 1.
Configure states event 5 is enabled	EVSTATEMSK5	Set STATEMSK5 bit 1 to 1. Set all other bits to 0. Event 5 is enabled in state 1.
Configure states event 6 is enabled	EVSTATEMSK6	Set STATEMSK6 bit 1 to 1. Set all other bits to 0. Event 6 is enabled in state 1.

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25.1 How to read this chapter

The timers are available on all LPC18xx parts.

The following configuration options apply to parts LPC1850_30_20_10 Rev 'A' only:

- The timer capture inputs and match outputs are configured through the GIMA (see Section 14.3).
- All timer capture inputs are also connected to dedicated external pins (see Section 14.3 and Section 13.3.6).

25.2 Basic configuration

The Timers are configured as follows:

- See Table 530 for clocking and power control.
- The Timer0/1/2/3 are reset by the TIMER0/1/2/3_RST (reset #32/33/34/35).
- The Timer0/1/2/3 interrupts are connected to slot # 12/13/14/15 in the NVIC. Match channels 2 of Timer0/1/3 are connected to slots # 13, 14, 16 in the Event router. (These outputs are ORed with SCT outputs 2, 6, 14.)
- For connecting the match channels 0 and 1 of Timer0/1/2/3 to the GPDMA, use the DMAMUX register in the CREG block (see Table 35) and enable the GPDMA channel in the DMA Channel Configuration registers (Section 16.6.20).
- Inputs to Timer1/2/3 capture inputs are controlled by the CREG6 register in the CREG block (see Table 37).
- The timer capture inputs and match outputs are configured through the GIMA (see Section 14.3).
- All timer capture inputs are also connected to dedicated external pins (see Section 14.3 and Section 13.3.6).

Table 530. Timer0/1/2/3 clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to the timer0 register interface and timer0 peripheral clock PCLK.	BASE_M3_CLK	CLK_M3_TIMER0	150 MHz
Clock to the timer1 register interface and timer1 peripheral clock PCLK.	BASE_M3_CLK	CLK_M3_TIMER1	150 MHz
Clock to the timer2 register interface and timer2 peripheral clock PCLK.	BASE_M3_CLK	CLK_M3_TIMER2	150 MHz
Clock to the timer3 register interface and timer3 peripheral clock PCLK.	BASE_M3_CLK	CLK_M3_TIMER3	150 MHz

25.3 Features

- A 32 bit Timer/Counter with a programmable 32 bit Prescaler.

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- Counter or Timer operation
- Up to four 32 bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32 bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set low on match.
  - Set high on match.
  - Toggle on match.
  - Do nothing on match.

25.4 General description

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally-supplied clock, and can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

25.5 Pin description

Remark: The capture inputs are shared between four SCT inputs and the timer inputs. The timer match outputs are ORed with the SCT outputs (see Figure 24).

Table 531. Timer0/1/2/3 pin description

Function name	Direction	Description
Timer0		
CTIN_[2:0]	I	CAP0_[2:0]; capture inputs 2 to 0 of timer 0.
CTOUT_[3:0]	O	MAT0_[3:0]; match outputs 3:0 of timer 0 are ORed with SCT outputs 3 to 0.
Timer1		
CTIN_0	I	CAP1_0; capture input 0 of timer 1.
CTIN_3	I	CAP1_1; capture input 1 of timer 1.
CTIN_4	I	CAP1_2; capture input 2 of timer 1.
CTOUT_[7:4]	O	MAT1_[3:0]; match outputs 3:0 of timer 1 are ORed with SCT outputs 7 to 4.
Timer2		
CTIN_0	I	CAP2_0; capture input 0 of timer 2.
CTIN_1	I	CAP2_1; capture input 1 of timer 2.
CTIN_5	I	CAP2_2; capture input 2 of timer 2.

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Table 531. Timer0/1/2/3 pin description

Function name	Direction	Description
CTOUT_[11:8]	O	MAT2_[3:0]; match outputs 3:0 of timer 2 are ORed with SCT outputs 11 to 8.
Timer3		
CTIN_0	I	CAP3_0; capture input 0 of timer 3.
CTIN_6	I	CAP3_1; capture input 1 of timer 3.
CTIN_7	I	CAP3_2; capture input 2 of timer 3.
CTOUT_[15:12]	O	MAT3_[3:0]; match outputs 3:0 of timer 3 are ORed with SCT outputs 15 to 12.

Table 532 gives a brief summary of each of the Timer/Counter related pins.

Table 532. Timer/Counter function description

Pin	Type	Description
CAP0_[3:0] CAP1_[3:0] CAP2_[3:0] CAP3_[3:0]	Input	Capture Signals- A transition on a capture pin can be configured to load one of the Capture Registers with the value in the Timer Counter and optionally generate an interrupt. Capture functionality can be selected from a number of pins. Timer/Counter block can select a capture signal as a clock source instead of the PCLK derived clock . For more details see Section 25.7.11.
MAT0_[3:0] MAT1_[3:0] MAT2_[3:0] MAT3_[3:0]	Output	External Match Output - When a match register (MR3:0) equals the timer counter (TC) this output can either toggle, go LOW, go HIGH, or do nothing. The External Match Register (EMR) controls the functionality of this output. Match Output functionality can be selected on a number of pins in parallel.

25.6 DMA connections

<tbd>

25.7 Register description

Each Timer/Counter contains the registers shown in Table 533.

Table 533. Register overview: Timer0/1/2/3 (register base addresses 0x4008 4000 (TIMER0), 0x4008 5000 (TIMER1), 0x400C 3000 (TIMER2), 0x400C 4000 (TIMER3))

Name	Access	Address offset	Description	Reset value[1]
IR	R/W	0x000	Interrupt Register. The IR can be written to clear interrupts. The IR can be read to identify which of eight possible interrupt sources are pending.	0
TCR	R/W	0x004	Timer Control Register. The TCR is used to control the Timer Counter functions. The Timer Counter can be disabled or reset through the TCR.	0
TC	R/W	0x008	Timer Counter. The 32 bit TC is incremented every PR+1 cycles of PCLK. The TC is controlled through the TCR.	0
PR	R/W	0x00C	Prescale Register. The Prescale Counter (below) is equal to this value, the next clock increments the TC and clears the PC.	0

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Table 533. Register overview: Timer0/1/2/3 (register base addresses 0x4008 4000 (TIMER0), 0x4008 5000 (TIMER1), 0x400C 3000 (TIMER2), 0x400C 4000 (TIMER3))

Name	Access	Address offset	Description	Reset value[1]
PC	R/W	0x010	Prescale Counter. The 32 bit PC is a counter which is incremented to the value stored in PR. When the value in PR is reached, the TC is incremented and the PC is cleared. The PC is observable and controllable through the bus interface.	0
MCR	R/W	0x014	Match Control Register. The MCR is used to control if an interrupt is generated and if the TC is reset when a Match occurs.	0
MR0	R/W	0x018	Match Register 0. MR0 can be enabled through the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt every time MR0 matches the TC.	0
MR1	R/W	0x01C	Match Register 1. See MR0 description.	0
MR2	R/W	0x020	Match Register 2. See MR0 description.	0
MR3	R/W	0x024	Match Register 3. See MR0 description.	0
CCR	R/W	0x028	Capture Control Register. The CCR controls which edges of the capture inputs are used to load the Capture Registers and whether or not an interrupt is generated when a capture takes place.	0
CR0	RO	0x02C	Capture Register 0. CR0 is loaded with the value of TC when there is an event on the CAPn.0(CAP0.0 or CAP1.0 respectively) input.	0
CR1	RO	0x030	Capture Register 1. See CR0 description.	0
CR2	RO	0x034	Capture Register 2. See CR0 description.	0
CR3	RO	0x038	Capture Register 3. See CR0 description.	0
EMR	R/W	0x03C	External Match Register. The EMR controls the external match pins MATn.0-3 (MAT0.0-3 and MAT1.0-3 respectively).	0
CTCR	R/W	0x070	Count Control Register. The CTCR selects between Timer and Counter mode, and in Counter mode selects the signal and edge(s) for counting.	0

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

25.7.1 Timer interrupt registers

The Interrupt Register consists of four bits for the match interrupts and four bits for the capture interrupts. If an interrupt is generated then the corresponding bit in the IR will be high. Otherwise, the bit will be low. Writing a logic one to the corresponding IR bit will reset the interrupt. Writing a zero has no effect. The act of clearing an interrupt for a timer match also clears any corresponding DMA request.

Table 534. Timer interrupt registers IR(IR - addresses 0x4008 4000 (TIMER0), 0x4008 5000 (TIMER1), 0x400C 3000 (TIMER3), 0x400C 4000 (TIMER4)) bit description

Bit	Symbol	Description	Reset value
0	MR0INT	Interrupt flag for match channel 0.	0
1	MR1INT	Interrupt flag for match channel 1.	0
2	MR2INT	Interrupt flag for match channel 2.	0
3	MR3INT	Interrupt flag for match channel 3.	0
4	CR0INT	Interrupt flag for capture channel 0 event.	0
5	CR1INT	Interrupt flag for capture channel 1 event.	0

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Table 534. Timer interrupt registers IR(IR - addresses 0x4008 4000 (TIMER0), 0x4008 5000 (TIMER1), 0x400C 3000 (TIMER3), 0x400C 4000 (TIMER4)) bit description

Bit	Symbol	Description	Reset value
6	CR2INT	Interrupt flag for capture channel 2 event.	0
7	CR3INT	Interrupt flag for capture channel 3 event.	0
31:8	-	Reserved.	-

25.7.2 Timer control registers

The Timer Control Register (TCR) is used to control the operation of the Timer/Counter.

Table 535. Timer control register TCR (TCR - addresses 0x4008 4004 (TIMER0), 0x4008 5004 (TIMER1), 0x400C 3003 (TIMER2), 0x400C 4004 (TIMER3)) bit description

Bit	Symbol	Description	Reset value
0	CEN	When one, the Timer Counter and Prescale Counter are enabled for counting. When zero, the counters are disabled.	0
1	CRST	When one, the Timer Counter and the Prescale Counter are synchronously reset on the next positive edge of PCLK. The counters remain reset until TCR[1] is returned to zero.	0
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

25.7.3 Timer counter registers

The 32-bit Timer Counter register is incremented when the prescale counter reaches its terminal count. Unless it is reset before reaching its upper limit, the Timer Counter will count up through the value 0xFFFF FFFF and then wrap back to the value 0x0000 0000. This event does not cause an interrupt, but a match register can be used to detect an overflow if needed.

Table 536. Timer counter registers TC (TC - addresses 0x4008 4008 (TIMER0), 0x4008 5008 (TIMER1), 0x400C 3008 (TIMER2), 0x400C 4008 (TIMER3)) bit description

Bit	Symbol	Description	Reset value
31:0	TC	Timer counter value.	0

25.7.4 Timer prescale registers

The 32-bit Timer prescale register specifies the maximum value for the Prescale Counter.

Table 537. Timer prescale registers PR (PR - addresses 0x4008 400C (TIMER0), 0x4008 500C (TIMER1), 0x400C 300C (TIMER2), 0x400C 400C (TIMER3)) bit description

Bit	Symbol	Description	Reset value
31:0	PM	Prescale counter maximum value.	0

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25.7.5 Timer prescale counter registers

The 32-bit Prescale Counter controls division of PCLK by some constant value before it is applied to the Timer Counter. This allows control of the relationship of the resolution of the timer versus the maximum time before the timer overflows. The Prescale Counter is incremented on every PCLK. When it reaches the value stored in the Prescale register, the Timer Counter is incremented and the Prescale Counter is reset on the next PCLK. This causes the Timer Counter to increment on every PCLK when PR = 0, every 2 PCLKs when PR = 1, etc.

Table 538. Timer prescale counter registers PC(PC - addresses 0x4008 4010 (TIMER0), 0x4008 5010 (TIMER1), 0x400C 3010 (TIMER2), 0x400C 4010 (TIMER3)) bit description

Bit	Symbol	Description	Reset value
31:0	PC	Prescale counter value.	0

25.7.6 Timer match control registers

The Match Control Register is used to control what operations are performed when one of the Match Registers matches the Timer Counter. The function of each of the bits is shown in Table 539.

Table 539. Timer match control registers MCR (MCR - addresses 0x4008 4014 (TIMER0), 0x4008 5014 (TIMER1), 0x400C 3014 (TIMER2), 0x400C 4014 (TIMER3)) bit description

Bit	Symbol	Value	Description	Reset value
0	MR0I		Interrupt on MR0	0
		1	Interrupt is generated when MR0 matches the value in the TC.	
		0	Interrupt is disabled	
1	MR0R		Reset on MR0	0
		1	TC will be reset if MR0 matches it.	
		0	Feature disabled.	
2	MR0S	1	Stop on MR0	0
		1	TC and PC will be stopped and TCR[0] will be set to 0 if MR0 matches the TC.	
		0	Feature disabled.	
3	MR1I		Interrupt on MR1	0
		1	Interrupt is generated when MR1 matches the value in the TC.	
		0	Interrupt is disabled.	
4	MR1R		Reset on MR1	0
		1	TC will be reset if MR1 matches it.	
		0	Feature disabled.	
5	MR1S		Stop on MR1	0
		1	TC and PC will be stopped and TCR[0] will be set to 0 if MR1 matches the TC.	
		0	Feature disabled.	

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Table 539. Timer match control registers MCR (MCR - addresses 0x4008 4014 (TIMER0), 0x4008 5014 (TIMER1), 0x400C 3014 (TIMER2), 0x400C 4014 (TIMER3)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value
6	MR2I		Interrupt on MR2	0
		1	Interrupt is generated when MR2 matches the value in the TC.	
		0	Interrupt is disabled	
7	MR2R		Reset on MR2	0
		1	TC will be reset if MR2 matches it.	
		0	Feature disabled.	
8	MR2S		Stop on MR2.	0
		1	TC and PC will be stopped and TCR[0] will be set to 0 if MR2 matches the TC	
		0	Feature disabled.	
9	MR3I		Interrupt on MR3	0
		1	Interrupt is generated when MR3 matches the value in the TC.	
		0	This interrupt is disabled	
10	MR3R		Reset on MR3	0
		1	TC will be reset if MR3 matches it.	
		0	Feature disabled.	
11	MR3S		Stop on MR3	0
		1	TC and PC will be stopped and TCR[0] will be set to 0 if MR3 matches the TC.	
		0	Feature disabled.	
31:12	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

25.7.7 Timer match registers (MR0 - MR3)

The Match register values are continuously compared to the Timer Counter value. When the two values are equal, actions can be triggered automatically. The action possibilities are to generate an interrupt, reset the Timer Counter, or stop the timer. Actions are controlled by the settings in the MCR register.

Table 540. Timer match registers MR0 to 3 (MR, addresses 0x4008 4018 (MR0) to 0x4008 4024 (M3) (TIMER0), 0x4008 5018 (MR0) to 0x4008 5024 (MR3)(TIMER1), 0x400C 3018 (MR0) to 0x400C 8024 (MR3) (TIMER2), 0x400C 4018 (MR0) to 0x400C 4024 (MR3)(TIMER3)) bit description

Bit	Symbol	Description	Reset value
31:0	MATCH	Timer counter match value.	0

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25.7.8 Timer capture control registers

The Capture Control Register is used to control whether one of the four Capture Registers is loaded with the value in the Timer Counter when the capture event occurs, and whether an interrupt is generated by the capture event. Setting both the rising and falling bits at the same time is a valid configuration, resulting in a capture event for both edges. In the description below, n represents the Timer number.

Remark: If Counter mode is selected for a particular CAP input in the CTCR, the 3 bits for that input in this register should be programmed as 000, but capture and/or interrupt can be selected for the other 3 CAP inputs.

Table 541. Timer capture control registers (CCR - addresses 0x4008 4028 (TIMER0), 0x4008 5020 (TIMER1), 0x400C 3028 (TIMER2), 0x400C 4028 (TIMER3)) bit description

Bit	Symbol	Value	Description	Reset value
0	CAP0RE		Capture on CAPn.0 rising edge	0
		1	A sequence of 0 then 1 on CAPn.0 will cause CR0 to be loaded with the contents of TC.	
		0	This feature is disabled.	
1	CAP0FE		Capture on CAPn.0 falling edge	0
		1	A sequence of 1 then 0 on CAPn.0 will cause CR0 to be loaded with the contents of TC.	
		0	This feature is disabled.	
2	CAP0I		Interrupt on CAPn.0 event	0
		1	A CR0 load due to a CAPn.0 event will generate an interrupt.	
		0	This feature is disabled.	
3	CAP1RE		Capture on CAPn.1 rising edge	0
		1	A sequence of 0 then 1 on CAPn.1 will cause CR1 to be loaded with the contents of TC.	
		0	This feature is disabled.	
4	CAP1FE		Capture on CAPn.1 falling edge	0
		1	A sequence of 1 then 0 on CAPn.1 will cause CR1 to be loaded with the contents of TC.	
		0	This feature is disabled.	
5	CAP1I		Interrupt on CAPn.1 event	0
		1	A CR1 load due to a CAPn.1 event will generate an interrupt.	
		0	This feature is disabled.	
6	CAP2RE		Capture on CAPn.2 rising edge	0
		1	A sequence of 0 then 1 on CAPn.2 will cause CR2 to be loaded with the contents of TC.	
		0	This feature is disabled.	
7	CAP2FE		Capture on CAPn.2 falling edge:	0
		1	A sequence of 1 then 0 on CAPn.2 will cause CR2 to be loaded with the contents of TC.	
		0	This feature is disabled.	

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Table 541. Timer capture control registers (CCR - addresses 0x4008 4028 (TIMER0), 0x4008 5020 (TIMER1), 0x400C 3028 (TIMER2), 0x400C 4028 (TIMER3)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value
8	CAP2I		Interrupt on CAPn.2 event	0
		1	A CR2 load due to a CAPn.2 event will generate an interrupt.	
		0	This feature is disabled.	
9	CAP3RE		Capture on CAPn.3 rising edge	0
		1	A sequence of 0 then 1 on CAPn.3 will cause CR3 to be loaded with the contents of TC.	
		0	This feature is disabled.	
10	CAP3FE		Capture on CAPn.3 falling edge	0
		1	A sequence of 1 then 0 on CAPn.3 will cause CR3 to be loaded with the contents of TC.	
		0	This feature is disabled.	
11	CAP3I		Interrupt on CAPn.3 event:	0
		1	A CR3 load due to a CAPn.3 event will generate an interrupt.	
		0	This feature is disabled.	
31:12	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

25.7.9 Timer capture registers (CR0 - CR3)

Each Capture register is associated with a device pin and may be loaded with the Timer Counter value when a specified event occurs on that pin. The settings in the Capture Control Register register determine whether the capture function is enabled, and whether a capture event happens on the rising edge of the associated pin, the falling edge, or on both edges.

Table 542. Timer capture registers CR0 to 3 (CR, address 0x4008 402C (CR0) to 0x4008 4038 (CR3) (TIMER0), 0x4008 502C (CR0) to 0x4008 5038 (CR3) (TIMER1), 0x400C 302C (CR0) to 0x400C 3038 (CR3) (TIMER2), 0x400C 402C (CR0) to 0x400C 4038 (CR3) (TIMER3)) bit description

Bit	Symbol	Description	Reset value
31:0	CAP	Timer counter capture value.	0

25.7.10 Timer external match registers

The External Match Register provides both control and status of the external match pins. In the descriptions below, “n” represents the Timer number, 0 or 1, and “m” represent a Match number, 0 through 3.

Match events for Match 0 and Match 1 in each timer can cause a DMA request, see Section 25.7.12.

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Table 543. Timer external match registers (EMR - addresses 0x4008 403C (TIMER0), 0x4008 503C (TIMER1), 0x400C 303C (TIMER2), 0x400C 403C (TIMER3)) bit description

Bit	Symbol	Value	Description	Reset value
0	EM0		External Match 0. When a match occurs between the TC and MR0, this bit can either toggle, go low, go high, or do nothing, depending on bits 5:4 of this register. This bit can be driven onto a MATn.0 pin, in a positive-logic manner (0 = low, 1 = high).	0
1	EM1		External Match 1. When a match occurs between the TC and MR1, this bit can either toggle, go low, go high, or do nothing, depending on bits 7:6 of this register. This bit can be driven onto a MATn.1 pin, in a positive-logic manner (0 = low, 1 = high).	0
2	EM2		External Match 2. When a match occurs between the TC and MR2, this bit can either toggle, go low, go high, or do nothing, depending on bits 9:8 of this register. This bit can be driven onto a MATn.0 pin, in a positive-logic manner (0 = low, 1 = high).	0
3	EM3		External Match 3. When a match occurs between the TC and MR3, this bit can either toggle, go low, go high, or do nothing, depending on bits 11:10 of this register. This bit can be driven onto a MATn.0 pin, in a positive-logic manner (0 = low, 1 = high).	0
5:4	EMC0		External Match Control 0. Determines the functionality of External Match 0.	00
		0x0	Do Nothing.	
		0x1	Clear the corresponding External Match bit/output to 0 (MATn.m pin is LOW if pinned out).	
		0x2	Set the corresponding External Match bit/output to 1 (MATn.m pin is HIGH if pinned out).	
		0x3	Toggle the corresponding External Match bit/output.	
7:6	EMC1		External Match Control 1. Determines the functionality of External Match 1.	00
		0x0	Do Nothing.	
		0x1	Clear the corresponding External Match bit/output to 0 (MATn.m pin is LOW if pinned out).	
		0x2	Set the corresponding External Match bit/output to 1 (MATn.m pin is HIGH if pinned out).	
		0x3	Toggle the corresponding External Match bit/output.	
9:8	EMC2		External Match Control 2. Determines the functionality of External Match 2.	00
		0x0	Do Nothing.	
		0x1	Clear the corresponding External Match bit/output to 0 (MATn.m pin is LOW if pinned out).	
		0x2	Set the corresponding External Match bit/output to 1 (MATn.m pin is HIGH if pinned out).	
		0x3	Toggle the corresponding External Match bit/output.	

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Table 543. Timer external match registers (EMR - addresses 0x4008 403C (TIMER0), 0x4008 503C (TIMER1), 0x400C 303C (TIMER2), 0x400C 403C (TIMER3)) bit description

Bit	Symbol	Value	Description	Reset value
11:10	EMC3		External Match Control 3. Determines the functionality of External Match 3.	00
		0x0	Do Nothing.	
		0x1	Clear the corresponding External Match bit/output to 0 (MATn.m pin is LOW if pinned out).	
		0x2	Set the corresponding External Match bit/output to 1 (MATn.m pin is HIGH if pinned out).	
		0x3	Toggle the corresponding External Match bit/output.	
15:12	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 544. External Match Control

EMR[11:10], EMR[9:8], EMR[7:6], or EMR[5:4]	Function
00	Do Nothing.
01	Clear the corresponding External Match bit/output to 0 (MATn.m pin is LOW if pinned out).
10	Set the corresponding External Match bit/output to 1 (MATn.m pin is HIGH if pinned out).
11	Toggle the corresponding External Match bit/output.

25.7.11 Timer count control registers

The Count Control Register (CTCR) is used to select between Timer and Counter mode, and in Counter mode to select the pin and edge(s) for counting.

When Counter Mode is chosen as a mode of operation, the CAP input (selected by the CTCR bits 3:2) is sampled on every rising edge of the PCLK clock. After comparing two consecutive samples of this CAP input, one of the following four events is recognized: rising edge, falling edge, either of edges or no changes in the level of the selected CAP input. Only if the identified event corresponds to the one selected by bits 1:0 in the CTCR register, the Timer Counter register will be incremented.

Effective processing of the externally supplied clock to the counter has some limitations. Since two successive rising edges of the PCLK clock are used to identify only one edge on the CAP selected input, the frequency of the CAP input can not exceed one quarter of the PCLK clock. Consequently, duration of the high/low levels on the same CAP input in this case can not be shorter than 1/(2 PCLK).

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Table 545. Timer count control register CTCR(CTCR - addresses 0x4008 4070 (TIMER0), 0x4008 5070 (TIMER1), 0x400C 3070 (TIMER2), 0x400C 4070 (TIMER3)) bit description

Bit	Symbol	Value	Description	Reset value
1:0	CTMODE		Counter/Timer Mode This field selects which rising PCLK edges can increment Timer's Prescale Counter (PC), or clear PC and increment Timer Counter (TC). Timer Mode: the TC is incremented when the Prescale Counter matches the Prescale Register.	00
		0x0	Timer Mode: every rising PCLK edge	
		0x1	Counter Mode: TC is incremented on rising edges on the CAP input selected by bits 3:2.	
		0x2	Counter Mode: TC is incremented on falling edges on the CAP input selected by bits 3:2.	
		0x3	Counter Mode: TC is incremented on both edges on the CAP input selected by bits 3:2.	
3:2	CINSEL		Count Input Select When bits 1:0 in this register are not 00, these bits select which CAP pin is sampled for clocking:	00
		0x0	CAPn.0 for TIMERn	
		0x1	CAPn.1 for TIMERn	
		0x2	CAPn.2 for TIMERn	
		0x3	CAPn.3 for TIMERn **Note:** If Counter mode is selected for a particular CAPn input in the TnCTCR, the 3 bits for that input in the Capture Control Register (TnCCR) must be programmed as 000. However, capture and/or interrupt can be selected for the other 3 CAPn inputs in the same timer.	
31:4	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

25.7.12 DMA operation

DMA requests are generated by 0 to 1 transitions of the External Match 0 and 1 bits of each timer. In order to have an effect, the GPDMA must be configured and the relevant timer DMA request selected as a DMA source via the CREG block, see Table 35.

When a timer is initially set up to generate a DMA request, the request may already be asserted before a match condition occurs. An initial DMA request may be avoided by having software by write a one to the interrupt flag location, as if clearing a timer interrupt. See Section 25.7.1. A DMA request will be cleared automatically when it is acted upon by the GPDMA controller.

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25.8 Example timer operation

Figure 70 shows a timer configured to reset the count and generate an interrupt on match. The prescaler is set to 2 and the match register set to 6. At the end of the timer cycle where the match occurs, the timer count is reset. This gives a full length cycle to the match value. The interrupt indicating that a match occurred is generated in the next clock after the timer reached the match value.

Figure 71 shows a timer configured to stop and generate an interrupt on match. The prescaler is again set to 2 and the match register set to 6. In the next clock after the timer reaches the match value, the timer enable bit in TCR is cleared, and the interrupt indicating that a match occurred is generated.

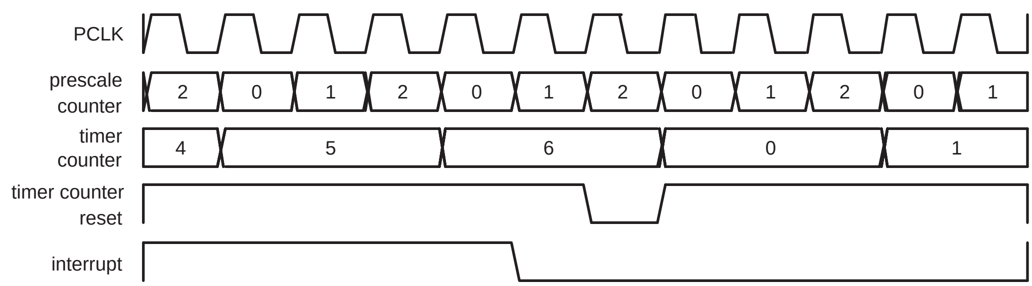


Fig 70. A timer cycle in which PR=2, MRx=6, and both interrupt and reset on match are enabled.

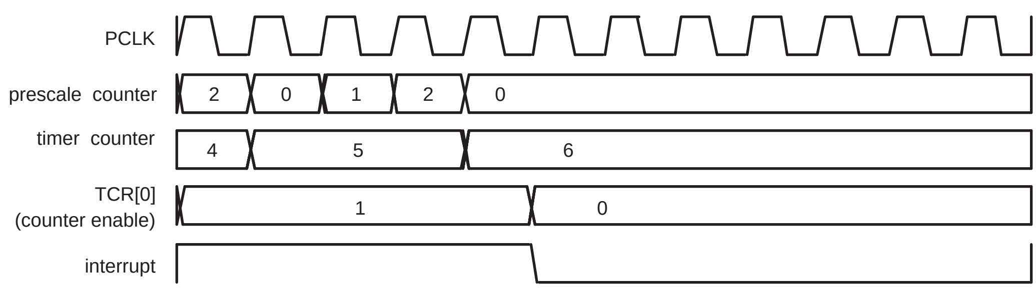


Fig 71. A timer Cycle in Which PR=2, MRx=6, and both interrupt and stop on match are enabled

25.9 Architecture

The block diagram for TIMER/COUNTER0 and TIMER/COUNTER1 is shown in Figure 72.

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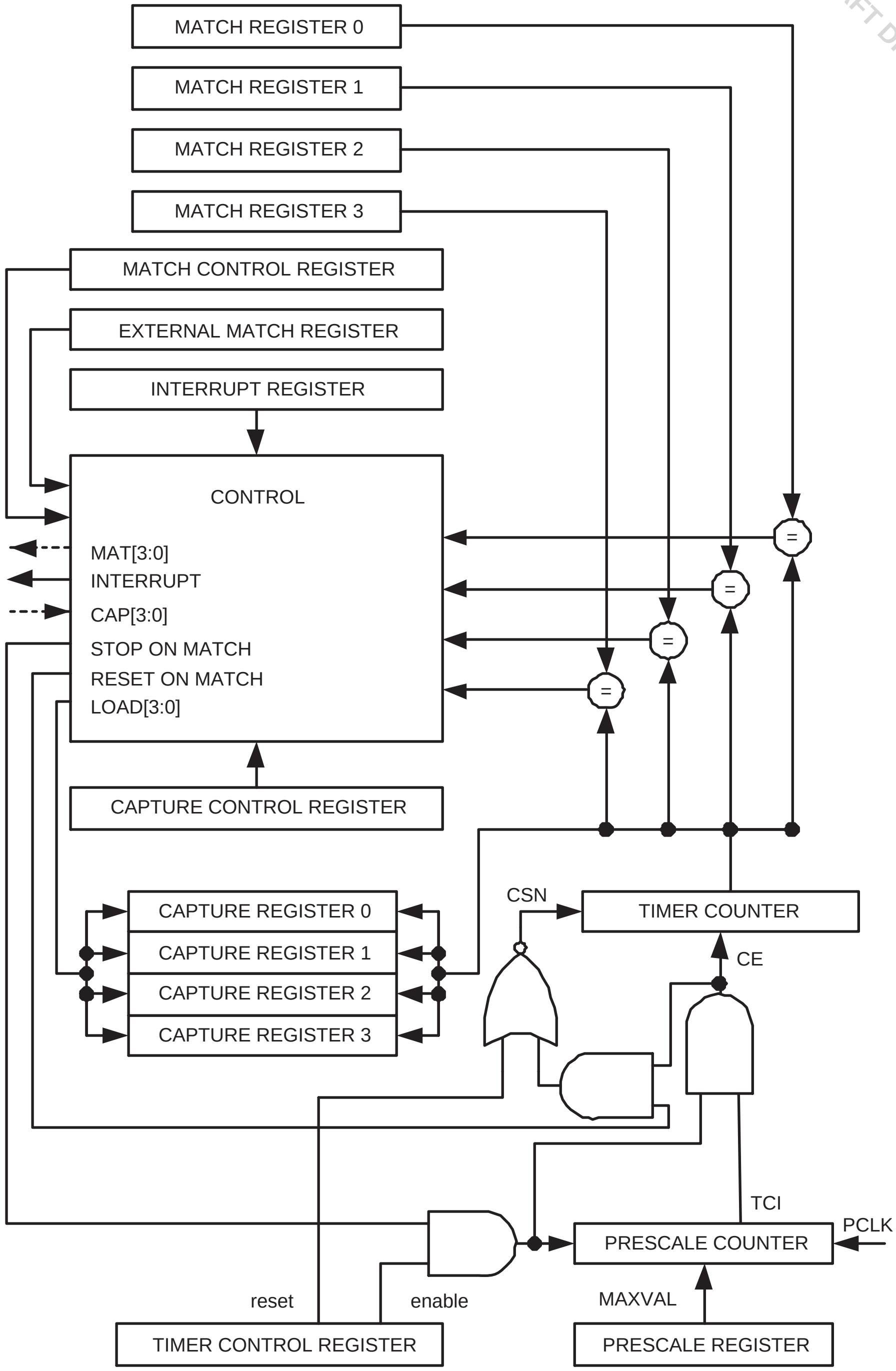


Fig 72. Timer block diagram

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26.1 How to read this chapter

The Motor control PWM is available on all LPC18xx parts.

26.2 Basic configuration

The PWM is configured as follows:

- See Table 546 for clocking and power control.
- The PWM is reset by the MOTOCONPWM_RST (reset #38).
- The PWM interrupt is connected to slot # 16 in the NVIC.

Table 546. PWM clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to the PWM Motor control block and PWM Motocon peripheral clock.	BASE_APB1_ CLK	CLK_APB1_ MOTOCON	150 MHz

26.3 Introduction

The Motor Control PWM (MCPWM) is optimized for three-phase AC and DC motor control applications, but can be used in many other applications that need timing, counting, capture, and comparison.

26.4 Features

The MCPWM contains three independent channels, each including:

- a 32-bit Timer/Counter (TC)
- a 32-bit Limit register (LIM)
- a 32-bit Match register (MAT)
- a 10-bit dead-time register (DT) and an associated 10-bit dead-time counter
- a 32-bit capture register (CAP)
- two modulated outputs (MCOA and MCOB) with opposite polarities
- a period interrupt, a pulse-width interrupt, and a capture interrupt

Input pins MCI0-2 can trigger TC capture or increment a channel’s TC. A global Abort input can force all of the channels into “A passive” state and cause an interrupt.

26.5 General description

Section 26.8 includes detailed descriptions of the various modes of MCPWM operation, but a quick preview here will provide background for the register descriptions below.

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The MCPWM includes 3 channels, each of which controls a pair of outputs that in turn can control something off-chip, like one set of coils in a motor. Each channel includes a Timer/Counter (TC) register that is incremented by a processor clock (timer mode) or by an input pin (counter mode).

Each channel has a Limit register that is compared to the TC value, and when a match occurs the TC is “recycled” in one of two ways. In “edge-aligned mode” the TC is reset to 0, while in “centered mode” a match switches the TC into a state in which it decrements on each processor clock or input pin transition until it reaches 0, at which time it starts counting up again.

Each channel also includes a Match register that holds a smaller value than the Limit register. In edge-aligned mode the channel’s outputs are switched whenever the TC matches either the Match or Limit register, while in center-aligned mode they are switched only when it matches the Match register.

So the Limit register controls the period of the outputs, while the Match register controls how much of each period the outputs spend in each state. Having a small value in the Limit register minimizes “ripple” if the output is integrated into a voltage, and allows the MCPWM to control devices that operate at high speed.

The “downside” of small values in the Limit register is that they reduce the resolution of the duty cycle controlled by the Match register. If you have 8 in the Limit register, the Match register can only select the duty cycle among 0%, 12.5%, 25%, …, 87.5%, or 100%. In general, the resolution of each step in the Match value is 1 divided by the Limit value.

This trade-off between resolution and period/frequency is inherent in the design of pulse width modulators.

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26.5.1 Block Diagram

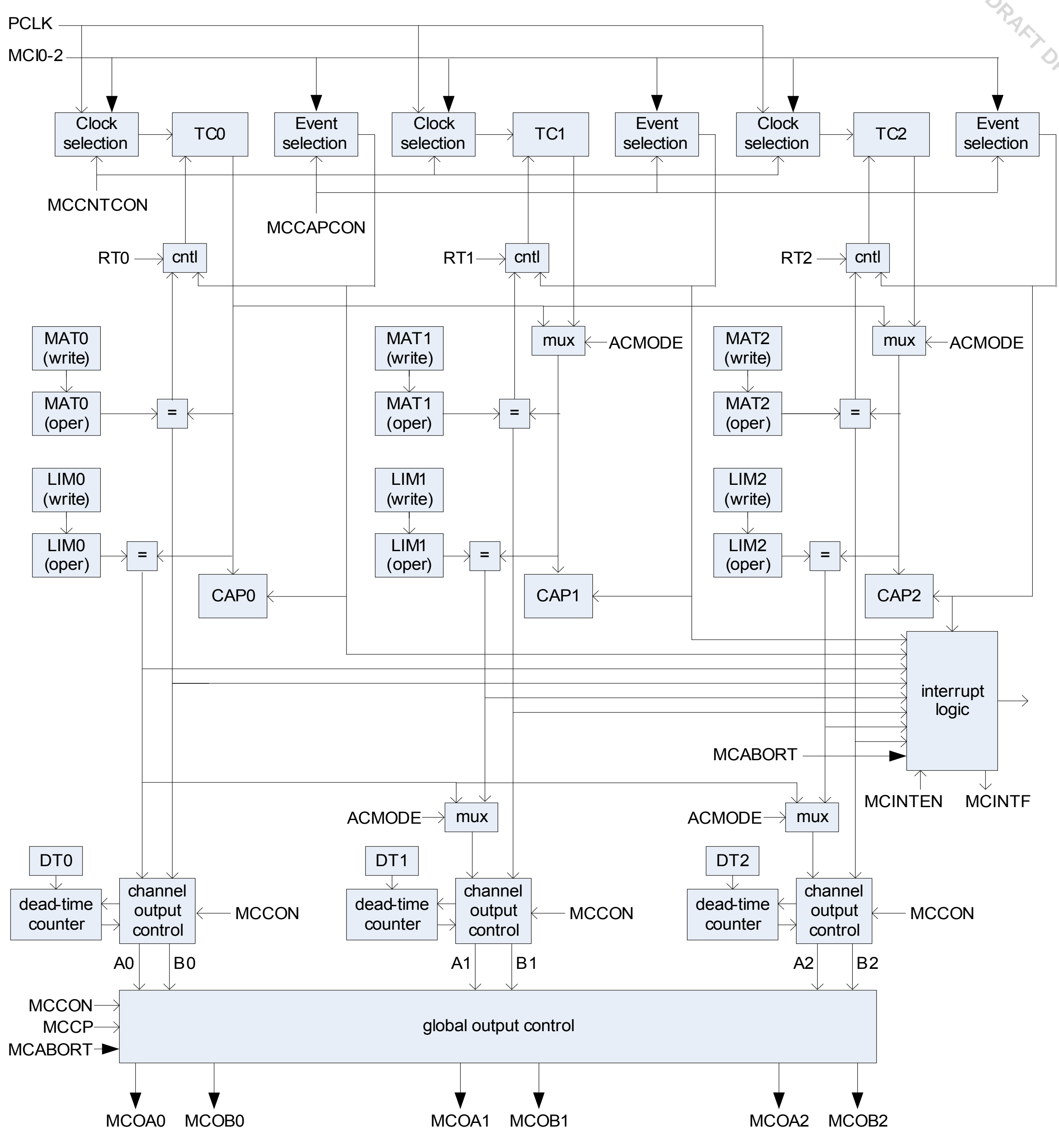


Fig 73. MCPWM Block Diagram

26.6 Pin description

Table 547 lists the MCPWM pins.

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Table 547. Pin summary

Pin	Type	Description
MCOA0/1/2	O	Output A for channels 0, 1, 2
MCOB0/1/2	O	Output B for channels 0, 1, 2
$\overline{\text{MCABORT}}$	I	Low-active Fast Abort
MCI0/1/2	I	Input for channels 0, 1, 2

26.7 Register description

“Control” registers and “interrupt” registers have separate read, set, and clear addresses. Reading such a register’s read address (e.g. MCCON) yields the state of the register bits. Writing ones to the set address (e.g. MCCON_SET) sets register bit(s), and writing ones to the clear address (e.g. MCCON_CLR) clears register bit(s).

The Capture registers (MCCAP) are read-only, and the write-only MCCAP_CLR address can be used to clear one or more of them. All the other MCPWM registers (MCTIM, MCPER, MCPW, MCDEADTIME, and MCCP) are normal read-write registers.

Table 548. Register overview: Motor Control Pulse Width Modulator (MCPWM) (base address 0x400A 0000)

Name	Access	Address offset	Description	Reset value
CON	RO	0x000	PWM Control read address	0
CON_SET	WO	0x004	PWM Control set address	-
CON_CLR	WO	0x008	PWM Control clear address	-
CAPCON	RO	0x00C	Capture Control read address	0
CAPCON_SET	WO	0x010	Capture Control set address	-
CAPCON_CLR	WO	0x014	Event Control clear address	-
TC0	R/W	0x018	Timer Counter register, channel 0	0
TC1	R/W	0x01C	Timer Counter register, channel 1	0
TC2	R/W	0x020	Timer Counter register, channel 2	0
LIM0	R/W	0x024	Limit register, channel 0	0xFFFF FFFF
LIM1	R/W	0x028	Limit register, channel 1	0xFFFF FFFF
LIM2	R/W	0x02C	Limit register, channel 2	0xFFFF FFFF
MAT0	R/W	0x030	Match register, channel 0	0xFFFF FFFF
MAT1	R/W	0x034	Match register, channel 1	0xFFFF FFFF
MAT2	R/W	0x038	Match register, channel 2	0xFFFF FFFF
DT	R/W	0x03C	Dead time register	0x3FFF FFFF
MCCP	R/W	0x040	Communication Pattern register	0
CAP0	RO	0x044	Capture register, channel 0	0
CAP1	RO	0x048	Capture register, channel 1	0
CAP2	RO	0x04C	Capture register, channel 2	0
INTEN	RO	0x050	Interrupt Enable read address	0
INTEN_SET	WO	0x054	Interrupt Enable set address	-
INTEN_CLR	WO	0x058	Interrupt Enable clear address	-
CNTCON	RO	0x05C	Count Control read address	0

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Table 548. Register overview: Motor Control Pulse Width Modulator (MCPWM) (base address 0x400A 0000)

Name	Access	Address offset	Description	Reset value
CNTCON_SET	WO	0x060	Count Control set address	-
CNTCON_CLR	WO	0x064	Count Control clear address	-
INTF	RO	0x068	Interrupt flags read address	0
INTF_SET	WO	0x06C	Interrupt flags set address	-
INTF_CLR	WO	0x070	Interrupt flags clear address	-
CAP_CLR	WO	0x074	Capture clear address	-

26.7.1 MCPWM Control register

26.7.1.1 MCPWM Control read address

The CON register controls the operation of all channels of the PWM. This address is read-only, but the underlying register can be modified by writing to addresses CON_SET and CON_CLR.

Table 549. MCPWM Control read address (CON - 0x400A 0000) bit description

Bit	Symbol	Value	Description	Reset value
0	RUN0		Stops/starts timer channel 0.	0
		0	Stop.	
		1	Run.	
1	CENTER0		Edge/center aligned operation for channel 0.	0
		0	Edge-aligned.	
		1	Center-aligned.	
2	POLA0		Selects polarity of the MCOA0 and MCOB0 pins.	0
		0	Passive state is LOW, active state is HIGH.	
		1	Passive state is HIGH, active state is LOW.	
3	DTE0		Controls the dead-time feature for channel 0.	0
		0	Dead-time disabled.	
		1	Dead-time enabled.	
4	DISUP0		Enable/disable updates of functional registers for channel 0 (see Section 26.8.2).	0
		0	Functional registers are updated from the write registers at the end of each PWM cycle.	
		1	Functional registers remain the same as long as the timer is running.	
7:5	-	-	Reserved.	
8	RUN1		Stops/starts timer channel 1.	0
		0	Stop.	
		1	Run.	
9	CENTER1		Edge/center aligned operation for channel 1.	0
		0	Edge-aligned.	
		1	Center-aligned.	

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Table 549. MCPWM Control read address (CON - 0x400A 0000) bit description

Bit	Symbol	Value	Description	Reset value
10	POLA1		Selects polarity of the MCOA1 and MCOB1 pins.	0
		0	Passive state is LOW, active state is HIGH.	
		1	Passive state is HIGH, active state is LOW.	
11	DTE1		Controls the dead-time feature for channel 1.	0
		0	Dead-time disabled.	
		1	Dead-time enabled.	
12	DISUP1		Enable/disable updates of functional registers for channel 1 (see Section 26.8.2).	0
		0	Functional registers are updated from the write registers at the end of each PWM cycle.	
		1	Functional registers remain the same as long as the timer is running.	
15:13	-	-	Reserved.	0
16	RUN2		Stops/starts timer channel 2.	0
		0	Stop.	
		1	Run.	
17	CENTER2		Edge/center aligned operation for channel 2.	0
		0	Edge-aligned.	
		1	Center-aligned.	
18	POLA2		Selects polarity of the MCOA2 and MCOB2 pins.	0
		0	Passive state is LOW, active state is HIGH.	
		1	Passive state is HIGH, active state is LOW.	
19	DTE2		Controls the dead-time feature for channel 1.	0
		0	Dead-time disabled.	
		1	Dead-time enabled.	
20	DISUP2		Enable/disable updates of functional registers for channel 2 (see Section 26.8.2).	0
		0	Functional registers are updated from the write registers at the end of each PWM cycle.	
		1	Functional registers remain the same as long as the timer is running.	
28:21	-	-	Reserved.	
29	INVBDC		Controls the polarity of the MCOB outputs for all 3 channels. This bit is typically set to 1 only in 3-phase DC mode.	
		0	The MCOB outputs have opposite polarity from the MCOA outputs (aside from dead time).	
		1	The MCOB outputs have the same basic polarity as the MCOA outputs. (see Section 26.8.6)	
30	ACMODE		3-phase AC mode select (see Section 26.8.7).	0
		0	3-phase AC-mode off: Each PWM channel uses its own timer-counter and period register.	
		1	3-phase AC-mode on: All PWM channels use the timer-counter and period register of channel 0.	

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Table 549. MCPWM Control read address (CON - 0x400A 0000) bit description

Bit	Symbol	Value	Description	Reset value
31	DCMODE		3-phase DC mode select (see Section 26.8.6).	0
		0	3-phase DC mode off: PWM channels are independent (unless bit ACMODE = 1)	
		1	3-phase DC mode on: The internal MCOA0 output is routed through the CP register (i.e. a mask) register to all six PWM outputs.	

26.7.1.2 MCPWM Control set address

Writing ones to this write-only address sets the corresponding bits in MCCON.

Table 550. MCPWM Control set address (CON_SET - 0x400A 0004) bit description

Bit	Symbol	Description	Reset value
0	RUN0_SET	Writing a one sets the corresponding bit in the CON register.	-
1	CENTER0_SET	Writing a one sets the corresponding bit in the CON register.	-
2	POLA0_SET	Writing a one sets the corresponding bit in the CON register.	-
3	DTE0_SET	Writing a one sets the corresponding bit in the CON register.	-
4	DISUP0_SET	Writing a one sets the corresponding bit in the CON register.	-
7:5	-	Writing a one sets the corresponding bit in the CON register.	-
8	RUN1_SET	Writing a one sets the corresponding bit in the CON register.	-
9	CENTER1_SET	Writing a one sets the corresponding bit in the CON register.	-
10	POLA1_SET	Writing a one sets the corresponding bit in the CON register.	-
11	DTE1_SET	Writing a one sets the corresponding bit in the CON register.	-
12	DISUP1_SET	Writing a one sets the corresponding bit in the CON register.	-
15:13	-	Writing a one sets the corresponding bit in the CON register.	-
16	RUN2_SET	Writing a one sets the corresponding bit in the CON register.	-
17	CENTER2_SET	Writing a one sets the corresponding bit in the CON register.	-
18	POLA2_SET	Writing a one sets the corresponding bit in the CON register.	-
19	DTE2_SET	Writing a one sets the corresponding bit in the CON register.	-
20	DISUP2_SET	Writing a one sets the corresponding bit in the CON register.	-
28:21	-	Writing a one sets the corresponding bit in the CON register.	-
29	INVBDC_SET	Writing a one sets the corresponding bit in the CON register.	-
30	ACMODE_SET	Writing a one sets the corresponding bit in the CON register.	-
31	DCMODE_SET	Writing a one sets the corresponding bit in the CON register.	-

26.7.1.3 MCPWM Control clear address

Writing ones to this write-only address clears the corresponding bits in CON.

Table 551. MCPWM Control clear address (CON_CLR - 0x400A 0008) bit description

Bit	Symbol	Description	Reset value
0	RUN0_CLR	Writing a one clears the corresponding bit in the CON register.	-
1	CENTER0_CLR	Writing a one clears the corresponding bit in the CON register.	-
2	POLA0_CLR	Writing a one clears the corresponding bit in the CON register.	-
3	DTE0_CLR	Writing a one clears the corresponding bit in the CON register.	-

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Table 551. MCPWM Control clear address (CON_CLR - 0x400A 0008) bit description

Bit	Symbol	Description	Reset value
4	DISUP0_CLR	Writing a one clears the corresponding bit in the CON register.	-
7:5	-	Writing a one clears the corresponding bit in the CON register.	-
8	RUN1_CLR	Writing a one clears the corresponding bit in the CON register.	-
9	CENTER1_CLR	Writing a one clears the corresponding bit in the CON register.	-
10	POLA1_CLR	Writing a one clears the corresponding bit in the CON register.	-
11	DTE1_CLR	Writing a one clears the corresponding bit in the CON register.	-
12	DISUP1_CLR	Writing a one clears the corresponding bit in the CON register.	-
15:13	-	Writing a one clears the corresponding bit in the CON register.	-
16	RUN2_CLR	Writing a one clears the corresponding bit in the CON register.	-
17	CENTER2_CLR	Writing a one clears the corresponding bit in the CON register.	-
18	POLA2_CLR	Writing a one clears the corresponding bit in the CON register.	-
19	DTE2_CLR	Writing a one clears the corresponding bit in the CON register.	-
20	DISUP2_CLR	Writing a one clears the corresponding bit in the CON register.	-
28:21	-	Writing a one clears the corresponding bit in the CON register.	-
29	INVBDC_CLR	Writing a one clears the corresponding bit in the CON register.	-
30	ACMOD_CLR	Writing a one clears the corresponding bit in the CON register.	-
31	DCMODE_CLR	Writing a one clears the corresponding bit in the CON register.	

26.7.2 PWM Capture Control register

26.7.2.1 MCPWM Capture Control read address

The MCCAPCON register controls detection of events on the MCI0-2 inputs for all MCPWM channels. Any of the three MCI inputs can be used to trigger a capture event on any or all of the three channels. This address is read-only, but the underlying register can be modified by writing to addresses CAPCON_SET and CAPCON_CLR.

Table 552. MCPWM Capture Control read address (CAPCON - 0x400A 000C) bit description

Bit	Symbol	Description	Reset value
0	CAP0MCI0_RE	A 1 in this bit enables a channel 0 capture event on a rising edge on MCI0.	0
1	CAP0MCI0_FE	A 1 in this bit enables a channel 0 capture event on a falling edge on MCI0.	0
2	CAP0MCI1_RE	A 1 in this bit enables a channel 0 capture event on a rising edge on MCI1.	0
3	CAP0MCI1_FE	A 1 in this bit enables a channel 0 capture event on a falling edge on MCI1.	0
4	CAP0MCI2_RE	A 1 in this bit enables a channel 0 capture event on a rising edge on MCI2.	0
5	CAP0MCI2_FE	A 1 in this bit enables a channel 0 capture event on a falling edge on MCI2.	0
6	CAP1MCI0_RE	A 1 in this bit enables a channel 1 capture event on a rising edge on MCI0.	0
7	CAP1MCI0_FE	A 1 in this bit enables a channel 1 capture event on a falling edge on MCI0.	0
8	CAP1MCI1_RE	A 1 in this bit enables a channel 1 capture event on a rising edge on MCI1.	0
9	CAP1MCI1_FE	A 1 in this bit enables a channel 1 capture event on a falling edge on MCI1.	0
10	CAP1MCI2_RE	A 1 in this bit enables a channel 1 capture event on a rising edge on MCI2.	0

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Table 552. MCPWM Capture Control read address (CAPCON - 0x400A 000C) bit description

Bit	Symbol	Description	Reset value
11	CAP1MCI2_FE	A 1 in this bit enables a channel 1 capture event on a falling edge on MCI2.	0
12	CAP2MCI0_RE	A 1 in this bit enables a channel 2 capture event on a rising edge on MCI0.	0
13	CAP2MCI0_FE	A 1 in this bit enables a channel 2 capture event on a falling edge on MCI0.	0
14	CAP2MCI1_RE	A 1 in this bit enables a channel 2 capture event on a rising edge on MCI1.	0
15	CAP2MCI1_FE	A 1 in this bit enables a channel 2 capture event on a falling edge on MCI1.	0
16	CAP2MCI2_RE	A 1 in this bit enables a channel 2 capture event on a rising edge on MCI2.	0
17	CAP2MCI2_FE	A 1 in this bit enables a channel 2 capture event on a falling edge on MCI2.	0
18	RT0	If this bit is 1, TC0 is reset by a channel 0 capture event.	0
19	RT1	If this bit is 1, TC1 is reset by a channel 1 capture event.	0
20	RT2	If this bit is 1, TC2 is reset by a channel 2 capture event.	0
21	HNFCAP0	Hardware noise filter: if this bit is 1, channel 0 capture events are delayed as described in Section 26.8.4.	0
22	HNFCAP1	Hardware noise filter: if this bit is 1, channel 1 capture events are delayed as described in Section 26.8.4.	0
23	HNFCAP2	Hardware noise filter: if this bit is 1, channel 2 capture events are delayed as described in Section 26.8.4.	0
31:24	-	Reserved.	-

26.7.2.2 MCPWM Capture Control set address

Writing ones to this write-only address sets the corresponding bits in CAPCON.

Table 553. MCPWM Capture Control set address (CAPCON_SET - 0x400A 0010) bit description

Bit	Symbol	Description	Reset value
0	CAP0MCI0_RE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
1	CAP0MCI0_FE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
2	CAP0MCI1_RE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
3	CAP0MCI1_FE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
4	CAP0MCI2_RE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
5	CAP0MCI2_FE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
6	CAP1MCI0_RE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
7	CAP1MCI0_FE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
8	CAP1MCI1_RE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
9	CAP1MCI1_FE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-

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Table 553. MCPWM Capture Control set address (CAPCON_SET - 0x400A 0010) bit description

Bit	Symbol	Description	Reset value
10	CAP1MCI2_RE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
11	CAP1MCI2_FE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
12	CAP2MCI0_RE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
13	CAP2MCI0_FE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
14	CAP2MCI1_RE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
15	CAP2MCI1_FE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
16	CAP2MCI2_RE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
17	CAP2MCI2_FE_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
18	RT0_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
19	RT1_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
20	RT2_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
21	HNFCAP0_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
22	HNFCAP1_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
23	HNFCAP2_SET	Writing a one sets the corresponding bits in the CAPCON register.	-
31:24	-	Reserved.	-

26.7.2.3 MCPWM Capture control clear address

Writing ones to this write-only address clears the corresponding bits in MCCAPCON.

Table 554. MCPWM Capture control clear register (CAPCON_CLR - address 0x400A 0014) bit description

Bit	Symbol	Description	Reset value
0	CAP0MCI0_RE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
1	CAP0MCI0_FE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
2	CAP0MCI1_RE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
3	CAP0MCI1_FE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-

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Table 554. MCPWM Capture control clear register (CAPCON_CLR - address 0x400A 0014) bit description

Bit	Symbol	Description	Reset value
4	CAP0MCI2_RE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
5	CAP0MCI2_FE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
6	CAP1MCI0_RE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
7	CAP1MCI0_FE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
8	CAP1MCI1_RE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
9	CAP1MCI1_FE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
10	CAP1MCI2_RE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
11	CAP1MCI2_FE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
12	CAP2MCI0_RE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
13	CAP2MCI0_FE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
14	CAP2MCI1_RE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
15	CAP2MCI1_FE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
16	CAP2MCI2_RE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
17	CAP2MCI2_FE_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
18	RT0_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
19	RT1_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
20	RT2_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
21	HNFCAP0_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
22	HNFCAP1_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
23	HNFCAP2_CLR	Writing a one clears the corresponding bits in the CAPCON register.	-
31:24	-	Reserved.	-

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26.7.3 MCPWM Timer/Counter 0-2 registers

These registers hold the current values of the 32-bit counter/timers for channels 0-2. Each value is incremented on every PCLK, or by edges on the MCI0-2 pins, as selected by CNTCON. The timer/counter counts up from 0 until it reaches the value in its corresponding PER register (or is stopped by writing to CON_CLR).

A TC register can be read at any time. In order to write to the TC register, its channel must be stopped. If not, the write will not take place, no exception is generated.

Table 555. MCPWM Timer/Counter 0 to 2 registers (TC - 0x400A 0018 (TC0), 0x400A 001C (TC1), 0x400A 0020) (TC2)bit description

Bit	Symbol	Description	Reset value
31:0	MCTC	Timer/Counter value.	0

26.7.4 MCPWM Limit 0-2 registers

These registers hold the limiting values for timer/counters 0-2. When a timer/counter reaches its corresponding limiting value: 1) in edge-aligned mode, it is reset and starts over at 0; 2) in center-aligned mode, it begins counting down until it reaches 0, at which time it begins counting up again.

If the channel's CENTER bit in CON is 0 selecting edge-aligned mode, the match between TC and LIM switches the channel's A output from "active" to "passive" state. If the channel's CENTER and DTE bits in CON are both 0, the match simultaneously switches the channel's B output from "passive" to "active" state.

If the channel's CENTER bit is 0 but the DTE bit is 1, the match triggers the channel's deadtime counter to begin counting -- when the deadtime counter expires, the channel's B output switches from "passive" to "active" state.

In center-aligned mode, matches between a channel's TC and LIM registers have no effect on its A and B outputs.

Writing to either a Limit or a Match (26.7.5) register loads a "write" register, and if the channel is stopped it also loads an "operating" register that is compared to the TC. If the channel is running and its "disable update" bit in CON is 0, the operating registers are loaded from the write registers: 1) in edge-aligned mode, when the TC matches the operating Limit register; 2) in center-aligned mode, when the TC counts back down to 0. If the channel is running and the "disable update" bit is 1, the operating registers are not loaded from the write registers until software stops the channel.

Reading an LIM address always returns the operating value.

Table 556. MCPWM Limit 0 to 2 registers (LIM - 0x400A 0024 (LIM0), 0x400A 0028 (LIM1), 0x400A 002C (LIM2)) bit description

Bit	Symbol	Description	Reset value
31:0	MCLIM	Limit value.	0xFFFF FFFF

Remark: In timer mode, the period of a channel's modulated MCO outputs is determined by its Limit register, and the pulse width at the start of the period is determined by its Match register. If it suits your way of thinking, consider the Limit register to be the "Period register" and the Match register to be the "Pulse Width register".

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26.7.5 MCPWM Match 0-2 registers

These registers also have “write” and “operating” versions as described above for the Limit registers, and the operating registers are also compared to the channels’ TCs. See 26.7.4 above for details of reading and writing both Limit and Match registers.

The Match and Limit registers control the MCO0-2 outputs. If a Match register is to have any effect on its channel’s operation, it must contain a smaller value than the corresponding Limit register.

Table 557. MCPWM Match 0 to 2 registers (MAT - addresses 0x400A 0030 (MAT0), 0x400A 0034 (MAT1), 0x400A 0038 (MAT2)) bit description

Bit	Symbol	Description	Reset value
31:0	MCMAT	Match value.	0xFFFF FFFF

26.7.5.1 Match register in Edge-Aligned mode

If the channel’s CENTER bit in CON is 0 selecting edge-aligned mode, a match between TC and MAT switches the channel’s B output from “active” to “passive” state. If the channel’s CENTER and DTE bits in CON are both 0, the match simultaneously switches the channel’s A output from “passive” to “active” state.

If the channel’s CENTER bit is 0 but the DTE bit is 1, the match triggers the channel’s deadtime counter to begin counting -- when the deadtime counter expires, the channel’s A output switches from “passive” to “active” state.

26.7.5.2 Match register in Center-Aligned mode

If the channel’s CENTER bit in CON is 1 selecting center-aligned mode, a match between TC and MAT while the TC is incrementing switches the channel’s B output from “active” to “passive” state, and a match while the TC is decrementing switches the A output from “active” to “passive”. If the channel’s CENTER bit in CON is 1 but the DTE bit is 0, a match simultaneously switches the channel’s other output in the opposite direction.

If the channel’s CENTER and DTE bits are both 1, a match between TC and MAT triggers the channel’s deadtime counter to begin counting -- when the deadtime counter expires, the channel’s B output switches from “passive” to “active” if the TC was counting up at the time of the match, and the channel’s A output switches from “passive” to “active” if the TC was counting down at the time of the match.

26.7.5.3 0 and 100% duty cycle

To lock a channel’s MCO outputs at the state “B active, A passive”, write its Match register with a higher value than you write to its Limit register. The match never occurs.

To lock a channel’s MCO outputs at the opposite state, “A active, B passive”, simply write 0 to its Match register.

26.7.6 MCPWM Dead-time register

This register holds the dead-time values for the three channels. If a channel’s DTE bit in CON is 1 to enable its dead-time counter, the counter counts down from this value whenever one its channel’s outputs changes from “active” to “passive” state. When the dead-time counter reaches 0, the channel changes its other output from “passive” to “active” state.

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The motivation for the dead-time feature is that power transistors, like those driven by the A and B outputs in a motor-control application, take longer to fully turn off than they take to start to turn on. If the A and B transistors are ever turned on at the same time, a wasteful and damaging current will flow between the power rails through the transistors. In such applications, the dead-time register should be programmed with the number of PCLK periods that is greater than or equal to the transistors' maximum turn-off time minus their minimum turn-on time.

Table 558. MCPWM Dead-time register (DT - address 0x400A 003C) bit description

Bit	Symbol	Description	Reset value
9:0	DT0	Dead time for channel 0.[1]	0x3FF
19:10	DT1	Dead time for channel 1.[2]	0x3FF
29:20	DT2	Dead time for channel 2.[2]	0x3FF
31:30	-	reserved	

[1] If ACMODE is 1 selecting AC-mode, this field controls the dead time for all three channels.

[2] If ACMODE is 0.

26.7.7 MCPWM Communication Pattern register

This register is used in DC mode only. The internal MCOA0 signal is routed to any or all of the six output pins under the control of the bits in this register. Like the Match and Limit registers, this register has "write" and "operational" versions. See 26.7.4 and 26.8.2 for more about this subject.

Table 559. MCPWM Communication Pattern register (CP - address 0x400A 0040) bit description

Bit	Symbol	Value	Description	Reset value
0	CCPA0		Communication pattern output A, channel 0.	0
		0	MCOA0 passive.	
		1	internal MCOA0.	
1	CCPB0		Communication pattern output B, channel 0.	0
		0	MCOB0 passive.	
		1	MCOB0 tracks internal MCOA0.	
2	CCPA1		Communication pattern output A, channel 1.	0
		0	MCOA1 passive.	
		1	MCOA1 tracks internal MCOA0.	
3	CCPB1		Communication pattern output B, channel 1.	0
		0	MCOB1 passive.	
		1	MCOB1 tracks internal MCOA0.	
4	CCPA2		Communication pattern output A, channel 2.	0
		0	MCOA2 passive.	
		1	MCOA2 tracks internal MCOA0.	
5	CCPB2		Communication pattern output B, channel 2.	0
		0	MCOB2 passive.	
		1	MCOB2 tracks internal MCOA0.	
31:6	-		Reserved.	

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26.7.8 MCPWM Capture read addresses

The CAPCON register (Table 552) allows software to select any edge(s) on any of the MCI0-2 inputs as a capture event for each channel. When a channel's capture event occurs, the current TC value for that channel is stored in its read-only Capture register. These addresses are read-only, but the underlying registers can be cleared by writing to the CAP_CLR address

Table 560. MCPWM Capture read addresses (CAP - 0x400A 0044 (CAP0), 0x400A 0048 (CAP1), 0x400A 004C 9CAP2)) bit description

Bit	Symbol	Description	Reset value
31:0	CAP	Current TC value at a capture event.	0x0000 00 00

26.7.9 MCPWM Interrupt registers

The Motor Control PWM module includes the following interrupt sources:

Table 561. Motor Control PWM interrupts

Symbol	Description
ILIM0/1/2	Limit interrupts for channels 0, 1, 2.
IMAT0/1/2	Match interrupts for channels 0, 1, 2.
ICAP0/1/2	Capture interrupts for channels 0, 1, 2.
ABORT	Fast abort interrupt

7.9.1 MCPWM Interrupt Enable read address

The INTEN register controls which of the MCPWM interrupts are enabled. This address is read-only, but the underlying register can be modified by writing to addresses INTEN_SET and INTEN_CLR.

Table 562. MCPWM Interrupt Enable read address (INTEN - 0x400A 0050) bit description

Bit	Symbol	Value	Description	Reset value
0	ILIM0		Limit interrupt for channel 0.	0
		0	Interrupt disabled.	
		1	Interrupt enabled.	
1	IMAT0		Match interrupt for channel 0.	0
		0	Interrupt disabled.	
		1	Interrupt enabled.	
2	ICAP0		Capture interrupt for channel 0.	0
		0	Interrupt disabled.	
		1	Interrupt enabled.	
3	-		Reserved.	-
4	ILIM1		Limit interrupt for channel 1.	0
		0	Interrupt disabled.	
		1	Interrupt enabled.	

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Table 562. MCPWM Interrupt Enable read address (INTEN - 0x400A 0050) bit description

Bit	Symbol	Value	Description	Reset value
5	IMAT1		Match interrupt for channel 1.	0
		0	Interrupt disabled.	
		1	Interrupt enabled.	
6	ICAP1		Capture interrupt for channel 1.	0
		0	Interrupt disabled.	
		1	Interrupt enabled.	
7	-		Reserved.	-
8	ILIM2		Limit interrupt for channel 2.	0
		0	Interrupt disabled.	
		1	Interrupt enabled.	
9	IMAT2		Match interrupt for channel 2.	0
		0	Interrupt disabled.	
		1	Interrupt enabled.	
10	ICAP2		Capture interrupt for channel 2.	0
		0	Interrupt disabled.	
		1	Interrupt enabled.	
14:11	-		Reserved.	-
15	ABORT		Fast abort interrupt.	0
		0	Interrupt disabled.	
		1	Interrupt enabled.	
31:16	-		Reserved.	-

26.7.9.2 MCPWM Interrupt Enable set address

Writing ones to this write-only address sets the corresponding bits in INTEN, thus enabling interrupts.

Table 563. MCPWM interrupt enable set register (INTEN_SET - address 0x400A 0054) bit description

Bit	Symbol	Description	Reset value
0	ILIM0_SET	Writing a one sets the corresponding bit in INTEN, thus enabling the interrupt.	-
1	IMAT0_SET	Writing a one sets the corresponding bit in INTEN, thus enabling the interrupt.	-
2	ICAP0_SET	Writing a one sets the corresponding bit in INTEN, thus enabling the interrupt.	-
3	-	Reserved.	-
4	ILIM1_SET	Writing a one sets the corresponding bit in INTEN, thus enabling the interrupt.	-
5	IMAT1_SET	Writing a one sets the corresponding bit in INTEN, thus enabling the interrupt.	-
6	ICAP1_SET	Writing a one sets the corresponding bit in INTEN, thus enabling the interrupt.	-

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Table 563. MCPWM interrupt enable set register (INTEN_SET - address 0x400A 0054) bit description

Bit	Symbol	Description	Reset value
7	-	Reserved.	-
9	ILIM2_SET	Writing a one sets the corresponding bit in INTEN, thus enabling the interrupt.	-
10	IMAT2_SET	Writing a one sets the corresponding bit in INTEN, thus enabling the interrupt.	-
11	ICAP2_SET	Writing a one sets the corresponding bit in INTEN, thus enabling the interrupt.	-
14:12	-	Reserved.	-
15	ABORT_SET	Writing a one sets the corresponding bit in INTEN, thus enabling the interrupt.	-
31:16	-	Reserved.	-

26.7.9.3 MCPWM Interrupt Enable clear address

Writing ones to this write-only address clears the corresponding bits in INTEN, thus disabling interrupts.

Table 564. PWM interrupt enable clear register (INTEN_CLR - address 0x400A 0058) bit description

Bit	Symbol	Description	Reset value
0	ILIM0_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
1	IMAT0_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
2	ICAP0_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
3	-	Reserved.	-
4	ILIM1_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
5	IMAT1_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
6	ICAP1_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
7	-	Reserved.	-
8	ILIM2_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
9	IMAT2_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
10	ICAP2_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
14:11	-	Reserved.	-
15	ABORT_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
31:16	-	Reserved.	-

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26.7.9.4 MCPWM Interrupt Flags read address

The INTF register includes all MCPWM interrupt flags, which are set when the corresponding hardware event occurs, or when ones are written to the INTF_SET address. When corresponding bits in this register and INTEN are both 1, the MCPWM asserts its interrupt request to the Interrupt Controller module. This address is read-only, but the bits in the underlying register can be modified by writing ones to addresses INTF_SET and INTF_CLR.

Table 565. MCPWM Interrupt flags read address (INTF - 0x400A 0068) bit description

Bit	Symbol	Value	Description	Reset value
0	ILIM0_F		Limit interrupt flag for channel 0.	0
		0	This interrupt source is not contributing to the MCPWM interrupt request.	
		1	If the corresponding bit in INTEN is 1, the MCPWM module is asserting its interrupt request to the Interrupt Controller.	
1	IMAT0_F		Match interrupt flag for channel 0.	0
		0	This interrupt source is not contributing to the MCPWM interrupt request.	
		1	If the corresponding bit in INTEN is 1, the MCPWM module is asserting its interrupt request to the Interrupt Controller.	
2	ICAP0_F		Capture interrupt flag for channel 0.	0
		0	This interrupt source is not contributing to the MCPWM interrupt request.	
		1	If the corresponding bit in INTEN is 1, the MCPWM module is asserting its interrupt request to the Interrupt Controller.	
3	-		Reserved.	-
4	ILIM1_F		Limit interrupt flag for channel 1.	0
		0	This interrupt source is not contributing to the MCPWM interrupt request.	
		1	If the corresponding bit in INTEN is 1, the MCPWM module is asserting its interrupt request to the Interrupt Controller.	
5	IMAT1_F		Match interrupt flag for channel 1.	0
		0	This interrupt source is not contributing to the MCPWM interrupt request.	
		1	If the corresponding bit in INTEN is 1, the MCPWM module is asserting its interrupt request to the Interrupt Controller.	
6	ICAP1_F		Capture interrupt flag for channel 1.	0
		0	This interrupt source is not contributing to the MCPWM interrupt request.	
		1	If the corresponding bit in INTEN is 1, the MCPWM module is asserting its interrupt request to the Interrupt Controller.	
7	-		Reserved.	-

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Table 565. MCPWM Interrupt flags read address (INTF - 0x400A 0068) bit description

Bit	Symbol	Value	Description	Reset value
8	ILIM2_F		Limit interrupt flag for channel 2.	0
		0	This interrupt source is not contributing to the MCPWM interrupt request.	
		1	If the corresponding bit in INTEN is 1, the MCPWM module is asserting its interrupt request to the Interrupt Controller.	
9	IMAT2_F		Match interrupt flag for channel 2.	0
		0	This interrupt source is not contributing to the MCPWM interrupt request.	
		1	If the corresponding bit in INTEN is 1, the MCPWM module is asserting its interrupt request to the Interrupt Controller.	
10	ICAP2_F		Capture interrupt flag for channel 2.	0
		0	This interrupt source is not contributing to the MCPWM interrupt request.	
		1	If the corresponding bit in INTEN is 1, the MCPWM module is asserting its interrupt request to the Interrupt Controller.	
14:11	-		Reserved.	-
15	ABORT_F		Fast abort interrupt flag.	0
		0	This interrupt source is not contributing to the MCPWM interrupt request.	
		1	If the corresponding bit in INTEN is 1, the MCPWM module is asserting its interrupt request to the Interrupt Controller.	
31:16	-		Reserved.	-

26.7.9.5 MCPWM Interrupt Flags set address

Writing one(s) to this write-only address sets the corresponding bit(s) in INTF, thus possibly simulating hardware interrupt(s).

Table 566. MCPWM Interrupt Flags set address (INTF_SET - 0x400A 006C) bit description

Bit	Symbol	Description	Reset value
0	ILIM0_F_SET	Writing a one sets the corresponding bit in the INTF register, thus possibly simulating hardware interrupt.	-
1	IMAT0_F_SET	Writing a one sets the corresponding bit in the INTF register, thus possibly simulating hardware interrupt.	-
2	ICAP0_F_SET	Writing a one sets the corresponding bit in the INTF register, thus possibly simulating hardware interrupt.	-
3	-	Reserved.	-
4	ILIM1_F_SET	Writing a one sets the corresponding bit in the INTF register, thus possibly simulating hardware interrupt.	-
5	IMAT1_F_SET	Writing a one sets the corresponding bit in the INTF register, thus possibly simulating hardware interrupt.	-
6	ICAP1_F_SET	Writing a one sets the corresponding bit in the INTF register, thus possibly simulating hardware interrupt.	-
7	-	Reserved.	-

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Table 566. MCPWM Interrupt Flags set address (INTF_SET - 0x400A 006C) bit description

Bit	Symbol	Description	Reset value
8	ILIM2_F_SET	Writing a one sets the corresponding bit in the INTF register, thus possibly simulating hardware interrupt.	-
9	IMAT2_F_SET	Writing a one sets the corresponding bit in the INTF register, thus possibly simulating hardware interrupt.	-
10	ICAP2_F_SET	Writing a one sets the corresponding bit in the INTF register, thus possibly simulating hardware interrupt.	-
14:11	-	Reserved.	-
15	ABORT_F_SET	Writing a one sets the corresponding bit in the INTF register, thus possibly simulating hardware interrupt.	-
31:16	-	Reserved.	-

26.7.9.6 MCPWM Interrupt Flags clear address

Writing one(s) to this write-only address sets the corresponding bit(s) in INTF, thus clearing the corresponding interrupt request(s). This is typically done in interrupt service routines.

Table 567. MCPWM Interrupt Flags clear address (INTF_CLR - 0x400A 0070) bit description

Bit	Symbol	Description	Reset value
0	ILIM0_F_CLR	Writing a one clears the corresponding bit in the INTF register, thus clearing the corresponding interrupt request.	-
1	IMAT0_F_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
2	ICAP0_F_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
3	-	Reserved.	-
4	ILIM1_F_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
5	IMAT1_F_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
6	ICAP1_F_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
7	-	Reserved.	-
8	ILIM2_F_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
9	IMAT2_F_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
10	ICAP2_F_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
14:11	-	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
15	ABORT_F_CLR	Writing a one clears the corresponding bit in INTEN, thus disabling the interrupt.	-
31:16	-	Reserved.	-

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26.7.10 MCPWM Count Control register

26.7.10.1 MCPWM Count Control read address

The CNTCON register controls whether the MCPWM channels are in timer or counter mode, and in counter mode whether the counter advances on rising and/or falling edges on any or all of the three MCI inputs. If timer mode is selected, the counter advances based on the PCLK clock.

This address is read-only. To set or clear the register bits, write ones to the CNTCON_SET or CNTCON_CLR address.

Table 568. MCPWM Count Control read address (CNTCON - 0x400A 005C) bit description

Bit	Symbol	Value	Description	Reset value
0	TC0MCI0_RE		Counter 0 rising edge mode, channel 0.	0
		0	A rising edge on MCI0 does not affect counter 0.	
		1	If MODE0 is 1, counter 0 advances on a rising edge on MCI0.	
1	TC0MCI0_FE		Counter 0 falling edge mode, channel 0.	0
		0	A falling edge on MCI0 does not affect counter 0.	
		1	If MODE0 is 1, counter 0 advances on a falling edge on MCI0.	
2	TC0MCI1_RE		Counter 0 rising edge mode, channel 1.	0
		0	A rising edge on MCI1 does not affect counter 0.	
		1	If MODE0 is 1, counter 0 advances on a rising edge on MCI1.	
3	TC0MCI1_FE		Counter 0 falling edge mode, channel 1.	0
		0	A falling edge on MCI1 does not affect counter 0.	
		1	If MODE0 is 1, counter 0 advances on a falling edge on MCI1.	
4	TC0MCI2_RE		Counter 0 rising edge mode, channel 2.	0
		0	A rising edge on MCI0 does not affect counter 0.	
		1	If MODE0 is 1, counter 0 advances on a rising edge on MCI2.	
5	TC0MCI2_FE		Counter 0 falling edge mode, channel 2.	0
		0	A falling edge on MCI0 does not affect counter 0.	
		1	If MODE0 is 1, counter 0 advances on a falling edge on MCI2.	
6	TC1MCI0_RE		Counter 1 rising edge mode, channel 0.	0
		0	A rising edge on MCI0 does not affect counter 1.	
		1	If MODE1 is 1, counter 1 advances on a rising edge on MCI0.	
7	TC1MCI0_FE		Counter 1 falling edge mode, channel 0.	0
		0	A falling edge on MCI0 does not affect counter 1.	
		1	If MODE1 is 1, counter 1 advances on a falling edge on MCI0.	
8	TC1MCI1_RE		Counter 1 rising edge mode, channel 1.	0
		0	A rising edge on MCI1 does not affect counter 1.	
		1	If MODE1 is 1, counter 1 advances on a rising edge on MCI1.	
9	TC1MCI1_FE		Counter 1 falling edge mode, channel 1.	0
		0	A falling edge on MCI0 does not affect counter 1.	
		1	If MODE1 is 1, counter 1 advances on a falling edge on MCI1.	

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Table 568. MCPWM Count Control read address (CNTCON - 0x400A 005C) bit description

Bit	Symbol	Value	Description	Reset value
10	TC1MCI2_RE		Counter 1 rising edge mode, channel 2.	0
		0	A rising edge on MCI2 does not affect counter 1.	
		1	If MODE1 is 1, counter 1 advances on a rising edge on MCI2.	
11	TC1MCI2_FE		Counter 1 falling edge mode, channel 2.	0
		0	A falling edge on MCI2 does not affect counter 1.	
		1	If MODE1 is 1, counter 1 advances on a falling edge on MCI2.	
12	TC2MCI0_RE		Counter 2 rising edge mode, channel 0.	0
		0	A rising edge on MCI0 does not affect counter 2.	
		1	If MODE2 is 1, counter 2 advances on a rising edge on MCI0.	
13	TC2MCI0_FE		Counter 2 falling edge mode, channel 0.	0
		0	A falling edge on MCI0 does not affect counter 2.	
		1	If MODE2 is 1, counter 2 advances on a falling edge on MCI0.	
14	TC2MCI1_RE		Counter 2 rising edge mode, channel 1.	0
		0	A rising edge on MCI1 does not affect counter 2.	
		1	If MODE2 is 1, counter 2 advances on a rising edge on MCI1.	
15	TC2MCI1_FE		Counter 2 falling edge mode, channel 1.	0
		0	A falling edge on MCI1 does not affect counter 2.	
		1	If MODE2 is 1, counter 2 advances on a falling edge on MCI1.	
16	TC2MCI2_RE		Counter 2 rising edge mode, channel 2.	0
		0	A rising edge on MCI2 does not affect counter 2.	
		1	If MODE2 is 1, counter 2 advances on a rising edge on MCI2.	
17	TC2MCI2_FE		Counter 2 falling edge mode, channel 2.	0
		0	A falling edge on MCI2 does not affect counter 2.	
		1	If MODE2 is 1, counter 2 advances on a falling edge on MCI2.	
28:18	-	-	Reserved.	-
29	CNTR0		Channel 0 counter/timer mode.	0
		0	Channel 0 is in timer mode.	
		1	Channel 0 is in counter mode.	
30	CNTR1		Channel 1 counter/timer mode.	0
		0	Channel 1 is in timer mode.	
		1	Channel 1 is in counter mode.	
31	CNTR2		Channel 2 counter/timer mode.	0
		0	Channel 2 is in timer mode.	
		1	Channel 2 is in counter mode.	

26.7.10.2 MCPWM Count Control set address

Writing one(s) to this write-only address sets the corresponding bit(s) in CNTCON.

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Table 569. MCPWM Count Control set address (CNTCON_SET - 0x400A 0060) bit description

Bit	Symbol	Description	Reset value
0	TC0MCI0_RE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
1	TC0MCI0_FE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
2	TC0MCI1_RE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
3	TC0MCI1_FE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
4	TC0MCI2_RE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
5	TC0MCI2_FE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
6	TC1MCI0_RE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
7	TC1MCI0_FE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
8	TC1MCI1_RE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
9	TC1MCI1_FE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
10	TC1MCI2_RE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
11	TC1MCI2_FE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
12	TC2MCI0_RE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
13	TC2MCI0_FE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
14	TC2MCI1_RE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
15	TC2MCI1_FE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
16	TC2MCI2_RE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
17	TC2MCI2_FE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
28:18	-	Reserved.	
29	CNTR0_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
30	CNTR1_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
31	CNTR2_SET	Writing a one sets the corresponding bit in the CNTCON register.	-

26.7.10.3 MCPWM Count Control clear address

Writing one(s) to this write-only address clears the corresponding bit(s) in CNTCON.

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Table 570. MCPWM Count Control clear address (CNTCON_CLR - 0x400A 0064) bit description

Bit	Symbol	Description	Reset value
0	TC0MCI0_RE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
1	TC0MCI0_FE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
2	TC0MCI1_RE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
3	TC0MCI1_FE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
4	TC0MCI2_RE	Writing a one clears the corresponding bit in the CNTCON register.	-
5	TC0MCI2_FE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
6	TC1MCI0_RE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
7	TC1MCI0_FE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
8	TC1MCI1_RE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
9	TC1MCI1_FE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
10	TC1MCI2_RE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
11	TC1MCI2_FE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
12	TC2MCI0_RE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
13	TC2MCI0_FE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
14	TC2MCI1_RE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
15	TC2MCI1_FE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
16	TC2MCI2_RE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
17	TC2MCI2_FE_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
28:18	-	Reserved.	
29	CNTR0_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
30	CNTR1_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-
31	CNTR2_CLR	Writing a one clears the corresponding bit in the CNTCON register.	-

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26.7.11 MCPWM Capture clear address

Writing ones to this write-only address clears the selected CAP register(s).

Table 571. MCPWM Capture clear address (CAP_CLR - 0x400A 0074) bit description

Bit	Symbol	Description
0	CAP_CLR0	Writing a 1 to this bit clears the CAP0 register.
1	CAP_CLR1	Writing a 1 to this bit clears the CAP1 register.
2	CAP_CLR2	Writing a 1 to this bit clears the CAP2 register.
31:3	-	Reserved

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26.8 Functional description

26.8.1 Pulse-width modulation

Each channel of the MCPWM has two outputs, A and B, that can drive a pair of transistors to switch a controlled point between two power rails. Most of the time the two outputs have opposite polarity, but a dead-time feature can be enabled (on a per-channel basis) to delay both signals' transitions from “passive” to “active” state so that the transistors are never both turned on simultaneously. In a more general view, the states of each output pair can be thought of “high”, “low”, and “floating” or “up”, “down”, and “center-off”.

Each channel's mapping from “active” and “passive” to “high” and “low” is programmable. After Reset, the three A outputs are passive/low, and the B outputs are active/high.

The MCPWM can perform edge-aligned and center-aligned pulse-width modulation.

Remark: In timer mode, the period of a channel's modulated MCO outputs is determined by its Limit register, and the pulse width at the start of the period is determined by its Match register. If it suits your way of thinking, consider the Limit register to be the “Period register” and the Match register to be the “Pulse Width register”.

Edge-aligned PWM without dead-time

In this mode the timer TC counts up from 0 to the value in the LIM register. As shown in Figure 74, the MCO state is “A passive” until the TC matches the Match register, at which point it changes to “A active”. When the TC matches the Limit register, the MCO state changes back to “A passive”, and the TC is reset and starts counting up again.

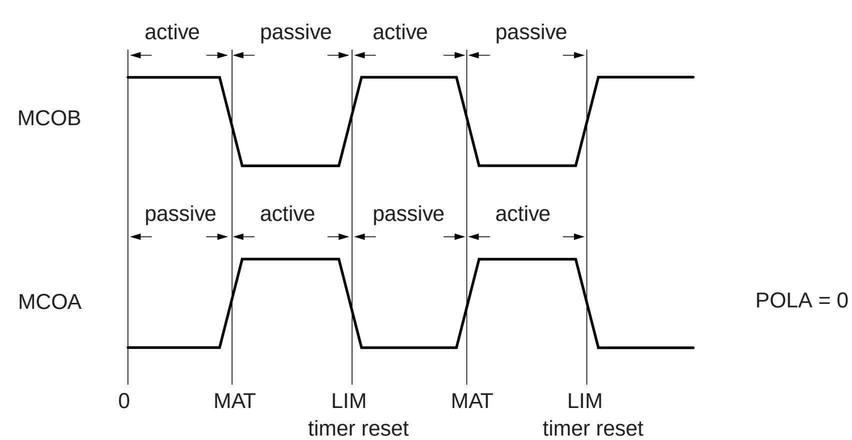


Fig 74. Edge-aligned PWM waveform without dead time, POLA = 0

Center-aligned PWM without dead-time

In this mode the timer TC counts up from 0 to the value in the LIM register, then counts back down to 0 and repeats. As shown in Figure 75, while the timer counts up, the MCO state is “A passive” until the TC matches the Match register, at which point it changes to “A active”. When the TC matches the Limit register it starts counting down. When the TC matches the Match register on the way down, the MCO state changes back to “A passive”.

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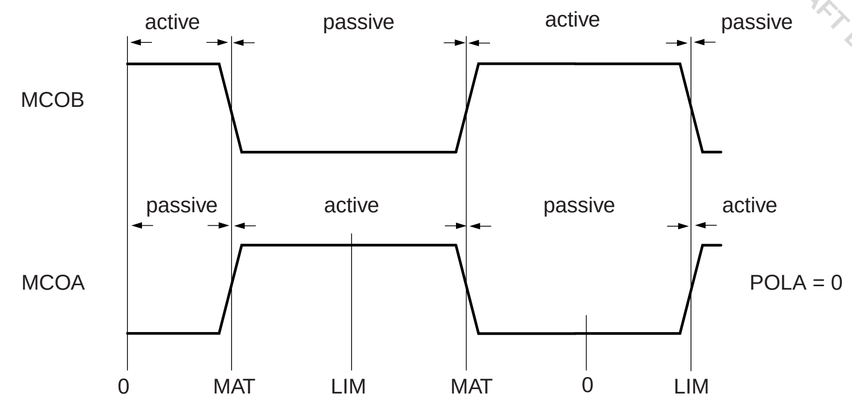


Fig 75. Center-aligned PWM waveform without dead time, POLA = 0

Dead-time counter

When the a channel's DTE bit is set in CON, the dead-time counter delays the passive-to-active transitions of both MCO outputs. The dead-time counter starts counting down, from the channel's DT value (in the DT register) to 0, whenever the channel's A or B output changes from active to passive. The transition of the other output from passive to active is delayed until the dead-time counter reaches 0. During the dead time, the MCOA and MCOB output levels are both passive. Figure 76 shows operation in edge aligned mode with dead time, and Figure 77 shows center-aligned operation with dead time.

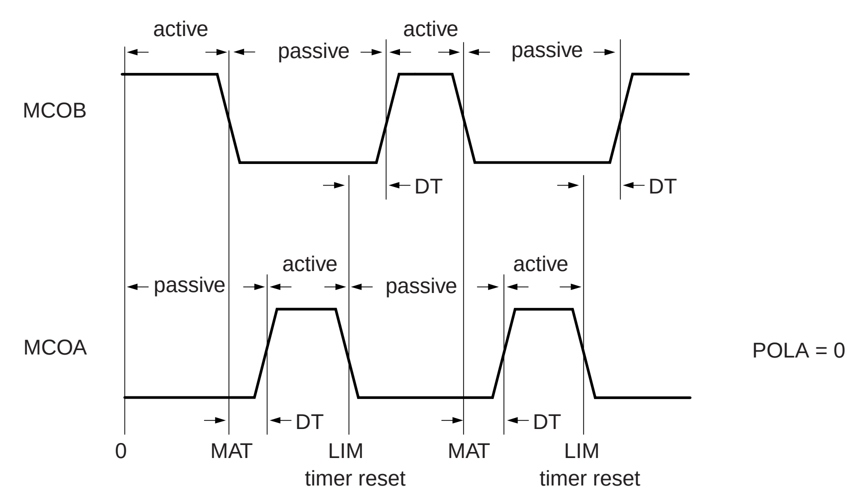


Fig 76. Edge-aligned PWM waveform with dead time, POLA = 0

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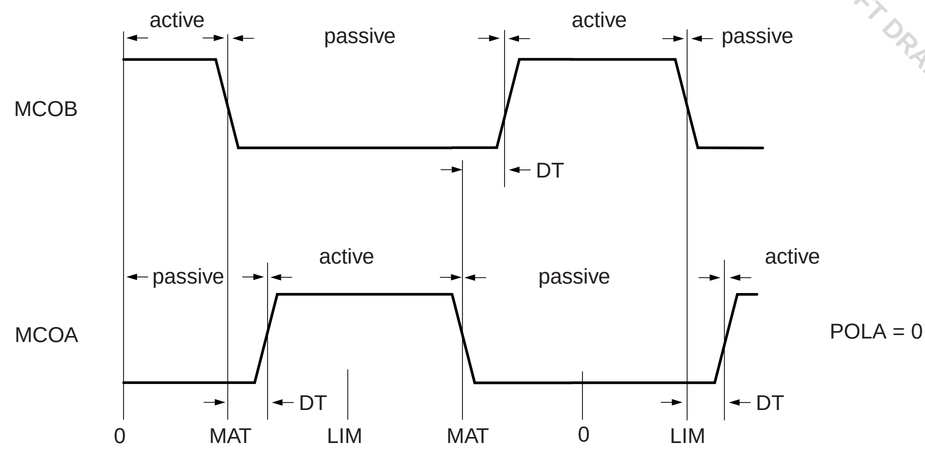


Fig 77. Center-aligned waveform with dead time, POLA = 0

26.8.2 Shadow registers and simultaneous updates

The Limit, Match, and Communication Pattern registers (LIM, MAT, and CP) are implemented as register pairs, each consisting of a write register and an operational register. Software writes into the write registers. The operational registers control the actual operation of each channel and are loaded with the current value in the write registers when the TC starts counting up from 0.

Updating of the functional registers can be disabled by setting a channel's DISUP bit in the CON register. If the DISUP bits are set, the functional registers are not updated until software stops the channel.

If a channel is not running when software writes to its LIM or MAT register, the functional register is updated immediately.

Software can write to a TC register only when its channel is stopped.

26.8.3 Fast Abort (ABORT)

The MCPWM has an external input $\overline{\text{MCABORT}}$. When this input goes low, all six MCO outputs assume their "A passive" states, and the Abort interrupt is generated if enabled. The outputs remain locked in "A passive" state until the ABORT interrupt flag is cleared or the Abort interrupt is disabled. The ABORT flag may not be cleared before the $\overline{\text{MCABORT}}$ input goes high.

In order to clear an ABORT flag, a 1 must be written to bit 15 of the INTF_CLR register. This will remove the interrupt request. The interrupt can also be disabled by writing a 1 to bit 15 of the INTEN_CLR register.

26.8.4 Capture events

Each PWM channel can take a snapshot of its TC when an input signal transitions. Any channel may use any combination of rising and/or falling edges on any or all of the MCI0-2 inputs as a capture event, under control of the CAPCON register. Rising or falling edges on the inputs are detected synchronously with respect to PCLK.

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If a channel's HNF bit in the CAPCON register is set to enable "noise filtering", a selected edge on an MCI pin starts the dead-time counter for that channel, and the capture event actions described below are delayed until the dead-time counter reaches 0. This function is targeted specifically for performing three-phase brushless DC motor control with Hall sensors.

A capture event on a channel (possibly delayed by HNF) causes the following:

- The current value of the TC is stored in the Capture register (CAP).
- If the channel's capture event interrupt is enabled (see Table 562), the capture event interrupt flag is set.
- If the channel's RT bit is set in the CAPCON register, enabling reset on a capture event, the input event has the same effect as matching the channel's TC to its LIM register. This includes resetting the TC and switching the MCO pin(s) in edge-aligned mode as described in 26.7.4 and 26.8.1.

26.8.5 External event counting (Counter mode)

If a channel's MODE bit is 1 in CNTCON, its TC is incremented by rising and/or falling edge(s) (synchronously detected) on the MCI0-2 input(s), rather than by PCLK. The PWM functions and capture functions are unaffected.

26.8.6 Three-phase DC mode

The three-phase DC mode is selected by setting the DCMODE bit in the CON register.

In this mode, the internal MCOA0 signal can be routed to any or all of the MCO outputs. Each MCO output is masked by a bit in the current commutation pattern register CP. If a bit in the CP register is 0, its output pin has the logic level for the passive state of output MCOA0. The polarity of the off state is determined by the POLA0 bit.

All MCO outputs that have 1 bits in the CP register are controlled by the internal MCOA0 signal.

The three MCOB output pins are inverted when the INVBDC bit is 1 in the CON register. This feature accommodates bridge-drivers that have active-low inputs for the low-side switches.

The CP register is implemented as a shadow register pair, so that changes to the active communication pattern occur at the beginning of a new PWM cycle. See 26.7.4 and 26.8.2 for more about writing and reading such registers.

Figure 78 shows sample waveforms of the MCO outputs in three-phase DC mode. Bits 1 and 3 in the CP register (corresponding to outputs MCOB1 and MCOB0) are set to 0 so that these outputs are masked and in the off state. Their logic level is determined by the POLA0 bit (here, POLA0 = 0 so the passive state is logic LOW). The INVBDC bit is set to 0 (logic level not inverted) so that the B output have the same polarity as the A outputs. Note that this mode differs from other modes in that the MCOB outputs are **not** the opposite of the MCOA outputs.

In the situation shown in Figure 78, bits 0, 2, 4, and 5 in the CP register are set to 1. That means that MCOA1 and both MCO outputs for channel 2 follow the MCOA0 signal.

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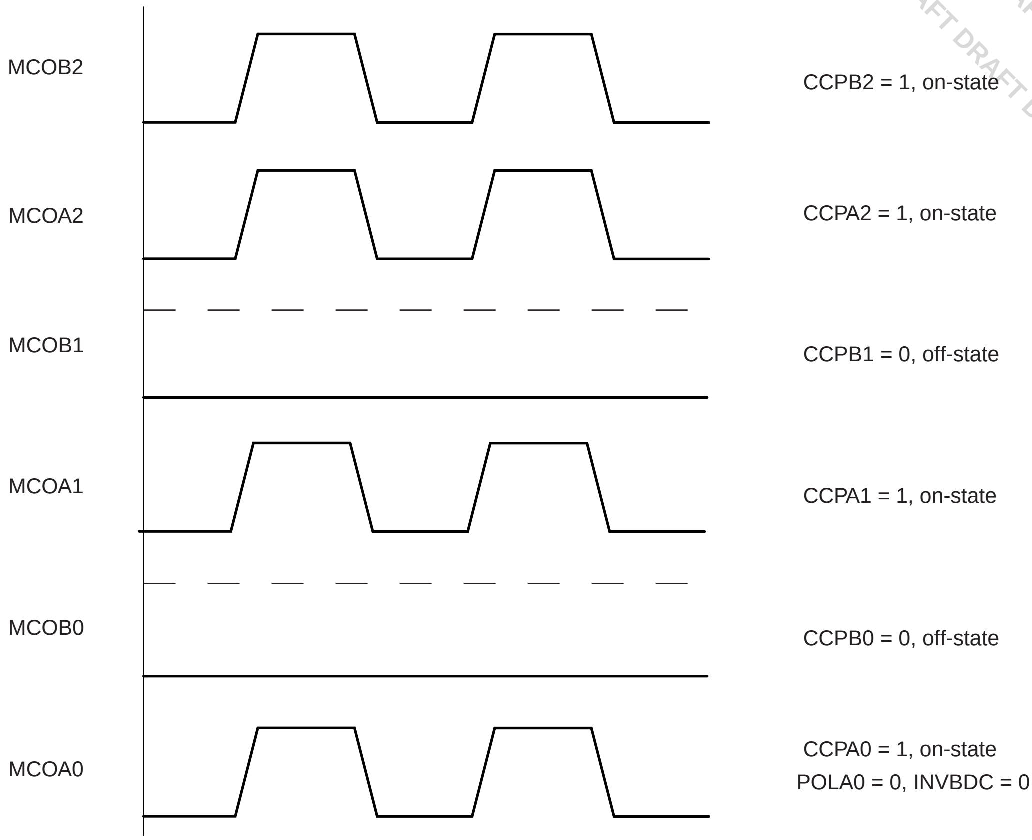


Fig 78. Three-phase DC mode sample waveforms

26.8.7 Three phase AC mode

The three-phase AC-mode is selected by setting the ACMODE bit in the CON register.

In this mode, the value of channel 0’s TC is routed to all channels for comparison with their MAT registers. (The LIM1-2 registers are not used.)

Each channel controls its MCO output by comparing its MAT value to TC0.

Figure 79 shows sample waveforms for the six MCO outputs in three-phase AC mode. The POLA bits are set to 0 for all three channels, so that for all MCO outputs the active levels are high and the passive levels are low. Each channel has a different MAT value which is compared to the TC0 value. In this mode the period value is identical for all three channels and is determined by LIM0. The dead-time mode is disabled.

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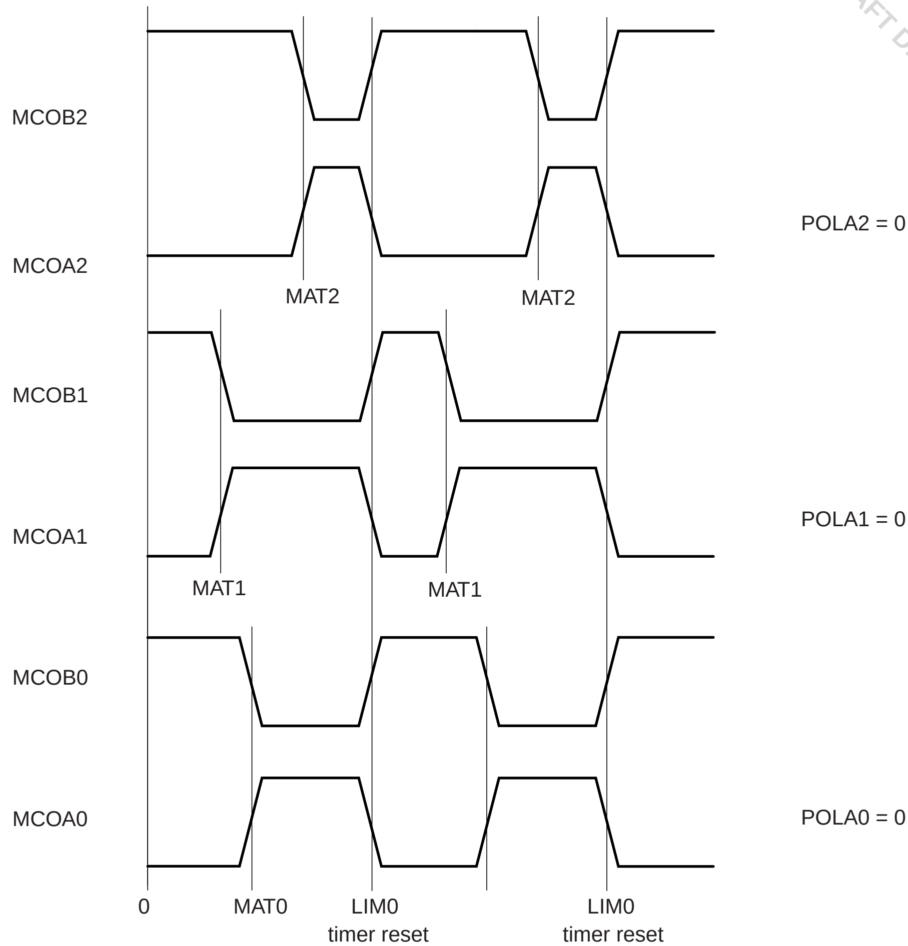


Fig 79. Three-phase AC mode sample waveforms, edge aligned PWM mode

26.8.8 Interrupts

The MCPWM includes 10 possible interrupt sources:

- When any channel's TC matches its Match register.
- When any channel's TC matches its Limit register.
- When any channel captures the value of its TC into its Capture register, because a selected edge occurs on any of MCI0-2.
- When all three channels' outputs are forced to "A passive" state because the $\overline{\text{MCABORT}}$ pin goes low.

Section 26.7.9 "MCPWM Interrupt registers" explains how to enable these interrupts, and Section 26.7.2 "PWM Capture Control register" describes how to map edges on the MCI0-2 inputs to "capture events" on the three channels.

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27.1 How to read this chapter

The QEI is available on all LPC18xx parts.

27.2 Basic configuration

The QEI is configured as follows:

- See Table 572 for clocking and power control.
- The QEI is reset by the QEI_RST (reset #39).
- The QEI interrupt is connected to slot # 15 in the Event router.

Table 572. QEI clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to the QEI register interface and QEI peripheral clock.	BASE_M3_CLK	CLK_M3_QEI	150 MHz

27.3 Features

This Quadrature Encoder Interface (QEI) has the following features:

- tracks encoder position.
- increments/ decrements depending on direction.
- programmable for 2X or 4X position counting.
- velocity capture using built-in timer.
- velocity compare function with less than interrupt.
- uses 32-bit registers for position and velocity.
- three position compare registers with interrupts.
- index counter for revolution counting.
- index compare register with interrupts.
- can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- digital filter with programmable delays for encoder input signals.
- can accept decoded signal inputs (clock and direction).

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27.4 Introduction

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, you can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. This quadrature encoder interface module decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, it can capture the velocity of the encoder wheel.

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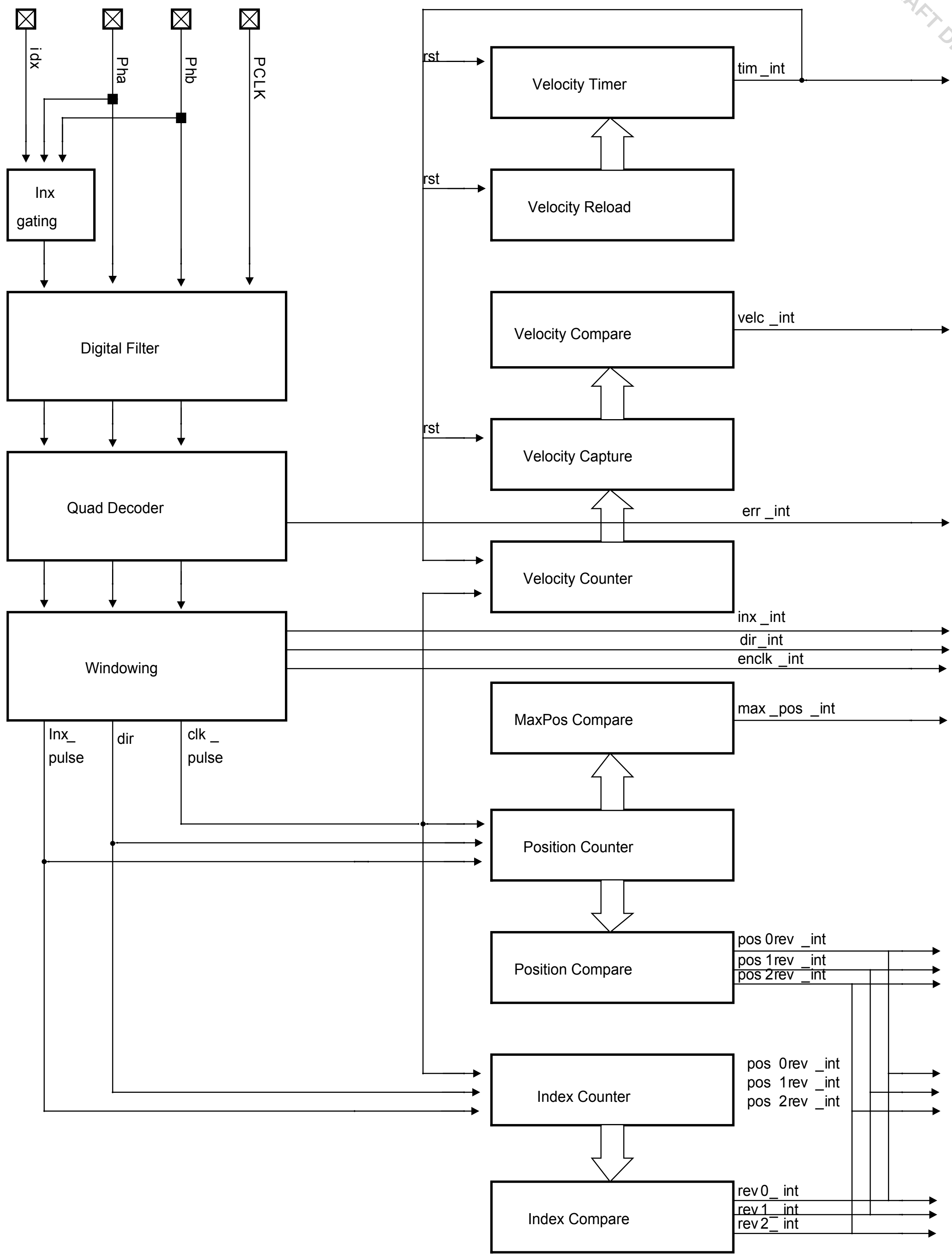


Fig 80. Encoder interface block diagram

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27.5 Pin description

Table 573. QEI pin description

Pin name	I/O	Description
QEI_A	I	Used as the Phase A (PhA) input to the Quadrature Encoder Interface.
QEI_B	I	Used as the Phase B (PhB) input to the Quadrature Encoder Interface.
QEI_IDX	I	Used as the Index (IDX) input to the Quadrature Encoder Interface.

27.6 Register description

Table 574. Register overview: QEI (base address 0x400C 6000)

Name	Access	Address offset	Description	Reset value
Control registers				
CON	WO	0x000	Control register	0
STAT	RO	0x004	Encoder status register	0
CONF	R/W	0x008	Configuration register	0x000F 0000
Position, index, and timer registers				
POS	RO	0x00C	Position register	0
MAXPOS	R/W	0x010	Maximum position register	0
CMPOS0	R/W	0x014	position compare register 0	0xFFFF FFFF
CMPOS1	R/W	0x018	position compare register 1	0xFFFF FFFF
CMPOS2	R/W	0x01C	position compare register 2	0xFFFF FFFF
INXCNT	RO	0x020	Index count register	0
INXCMP0	R/W	0x024	Index compare register 0	0xFFFF FFFF
LOAD	R/W	0x028	Velocity timer reload register	0xFFFF FFFF
TIME	RO	0x02C	Velocity timer register	0xFFFF FFFF
VEL	RO	0x030	Velocity counter register	0
CAP	RO	0x034	Velocity capture register	0xFFFF FFFF
VELCOMP	R/W	0x038	Velocity compare register	0
FILTERPHA	R/W	0x03C	Digital filter register on input phase A (QEI_A)	0
FILTERPHB	R/W	0x040	Digital filter register on input phase B (QEI_B)	0
FILTERINX	R/W	0x044	Digital filter register on input index (QEI_IDX)	0
WINDOW	R/W	0x048	Index acceptance window register	0x0000 0000
INXCMP1	R/W	0x04C	Index compare register 1	0xFFFF FFFF
INXCMP2	R/W	0x050	Index compare register 2	0xFFFF FFFF
Interrupt registers				
IEC	WO	0xFD8	Interrupt enable clear register	0
IES	WO	0xFDC	Interrupt enable set register	0
INTSTAT	RO	0xFE0	Interrupt status register	0

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Table 574. Register overview: QEI (base address 0x400C 6000)

Name	Access	Address offset	Description	Reset value
IE	RO	0xFE4	Interrupt enable register	0
CLR	WO	0xFE8	Interrupt status clear register	0
SET	WO	0xFEC	Interrupt status set register	0

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27.6.1 Control registers

27.6.1.1 QEI Control register

This register contains bits which control the operation of the position and velocity counters of the QEI module.

Table 575: QEI Control register (CON - address 0x400C 6000) bit description

Bit	Symbol	Description	Reset value
0	RESP	Reset position counter. When set = 1, resets the position counter to all zeros. Autoclears when the position counter is cleared.	0
1	RESPI	Reset position counter on index. When set = 1, resets the position counter to all zeros when an index pulse occurs. Autoclears when the position counter is cleared.	0
2	RESV	Reset velocity. When set = 1, resets the velocity counter to all zeros and reloads the velocity timer. Autoclears when the velocity counter is cleared.	0
3	RESI	Reset index counter. When set = 1, resets the index counter to all zeros. Autoclears when the index counter is cleared.	0
31:4	-	reserved	0

27.6.1.2 QEI Configuration register

This register contains the configuration of the QEI module.

Table 576: QEI Configuration register (CONF - address 0x400C 6008) bit description

Bit	Symbol	Description	Reset value
0	DIRINV	Direction invert. When = 1, complements the DIR bit.	0
1	SIGMODE	Signal Mode. When = 0, PhA and PhB function as quadrature encoder inputs. When = 1, PhA functions as the direction signal and PhB functions as the clock signal.	0
2	CAPMODE	Capture Mode. When = 0, only PhA edges are counted (2X). When = 1, BOTH PhA and PhB edges are counted (4X), increasing resolution but decreasing range.	0
3	INVINX	Invert Index. When set, inverts the sense of the index input.	0
4	CRESPI	Continuously reset position counter on index. When set = 1, resets the position counter to all zeros when an index pulse occurs at the next position increase (recalibration). Auto-clears when the position counter is cleared.	0
15:5	-	Reserved	0
19:16	INXGATE	Index gating configuration: when INXGATE(19)=1, pass the index when Pha=0 and Phb=0, else block. when INXGATE(18)=1, pass the index when Pha=0 and Phb=1, else block. when INXGATE(17)=1, pass the index when Pha=1 and Phb=1, else block. when INXGATE(16)=1, pass the index when Pha=1 and Phb=0, else block.	1111
31:20	-	reserved	0

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27.6.1.3 QEI Status register

This register provides the status of the encoder interface.

Table 577: QEI Interrupt Status register (STAT - address 0x400C 6004) bit description

Bit	Symbol	Description	Reset value
0	DIR	Direction bit. In combination with DIRINV bit indicates forward or reverse direction. See Table 604.	
31:1	-	reserved	0

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27.6.2 Position, index and timer registers

27.6.2.1 QEI Position register

This register contains the current value of the encoder position. Increments or decrements when encoder counts occur, depending on the direction of rotation.

Table 578. QEI Position register (POS - address 0x400C 600C) bit description

Bit	Symbol	Description	Reset value
31:0	POS	Current position value.	0

27.6.2.2 QEI Maximum Position register

This register contains the maximum value of the encoder position. In forward rotation the position register resets to zero when the position register exceeds this value. In reverse rotation the position register resets to this value when the position register decrements from zero.

Table 579. QEI Maximum Position register (MAXPOS - address 0x400C 6010) bit description

Bit	Symbol	Description	Reset value
31:0	MAXPOS	Maximum position value.	0

27.6.2.3 QEI Position Compare register 0

This register contains a position compare value. This value is compared against the current value of the position register. Interrupts can be enabled to interrupt when the compare value is less than, equal to, or greater than the current value of the position register.

Table 580. QEI Position Compare register 0 (CMPOS0 - address 0x400C 6014) bit description

Bit	Symbol	Description	Reset value
31:0	PCMP0	Position compare value 0.	0xFFFF FFFF

27.6.2.4 QEI Position Compare register 1

This register contains a position compare value. This value is compared against the current value of the position register. Interrupts can be enabled to interrupt when the compare value is less than, equal to, or greater than the current value of the position register.

Table 581. QEI Position Compare register 1 (CMPOS1 - address 0x400C 6018) bit description

Bit	Symbol	Description	Reset value
31:0	PCMP1	Position compare value 1.	0xFFFF FFFF

27.6.2.5 QEI Position Compare register 2

This register contains a position compare value. This value is compared against the current value of the position register. Interrupts can be enabled to interrupt when the compare value is less than, equal to, or greater than the current value of the position register.

Table 582. QEI Position Compare register 2 (CMPOS2 - address 0x400C 601C) bit description

Bit	Symbol	Description	Reset value
31:0	PCMP2	Position compare value 2.	0xFFFF FFFF

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27.6.2.6 QEI Index Count register

This register contains the current value of the encoder position. Increments or decrements when encoder counts occur, depending on the direction of rotation.

Table 583. QEI Index Count register (INXCNT- address 0x400C 6020) bit description

Bit	Symbol	Description	Reset value
31:0	ENCPOS	Current encoder position value.	0

27.6.2.7 QEI Index Compare register 0

This register contains an index compare value. This value is compared against the current value of the index count register. Interrupts can be enabled to interrupt when the compare value is less than, equal to, or greater than the current value of the index count register.

Table 584. QEI Index Compare register 0(INXCMP0 - address 0x400C 6024) bit description

Bit	Symbol	Description	Reset value
31:0	ICMP0	Index compare value.	0xFFFF FFFF

27.6.2.8 QEI Timer Reload register

This register contains the reload value of the velocity timer. When the timer (QEITIME) overflows or the RESV bit is asserted, this value is loaded into the timer (QEITIME).

Table 585. QEI Timer Load register (LOAD - address 0x400C 6028) bit description

Bit	Symbol	Description	Reset value
31:0	VELLOAD	Current velocity timer load value.	0xFFFF FFFF

27.6.2.9 QEI Timer register

This register contains the current value of the velocity timer. When this timer overflows the value of velocity counter (QEIVEL) is stored in the velocity capture register (QEICAP), the velocity counter is reset to zero, the timer is reloaded with the value stored in the velocity reload register (QEILOAD), and the velocity interrupt (TIM_Int) is asserted.

Table 586. QEI Timer register (TIME - address 0x400C 602C) bit description

Bit	Symbol	Description	Reset value
31:0	VELVAL	Current velocity timer value.	0xFFFF FFFF

27.6.2.10 QEI Velocity register

This register contains the running count of velocity pulses for the current time period. When the velocity timer (QEITIME) overflows the contents of this register is captured in the velocity capture register (QEICAP). After capture, this register is set to zero. This register is also reset when the velocity reset bit (RESV) is asserted.

Table 587. QEI Velocity register (VEL - address 0x400C 6030) bit description

Bit	Symbol	Description	Reset value
31:0	VELPC	Current velocity pulse count.	0x0

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27.6.2.11 QEI Velocity Capture register

This register contains the most recently measured velocity of the encoder. This corresponds to the number of velocity pulses counted in the previous velocity timer period.The current velocity count is latched into this register when the velocity timer overflows.

Table 588. QEI Velocity Capture register (CAP - address 0x400C 6034) bit description

Bit	Symbol	Description	Reset value
31:0	VELCAP	Velocity capture value.	0xFFFF FFFF

27.6.2.12 QEI Velocity Compare register

This register contains a velocity compare value. This value is compared against the captured velocity in the velocity capture register. If the capture velocity is less than the value in this compare register, a velocity compare interrupt (VELC_Int) will be asserted, if enabled.

Table 589. QEI Velocity Compare register (VELCOMP - address 0x400C 6038) bit description

Bit	Symbol	Description	Reset value
31:0	VELCMP	Velocity compare value.	0x0

27.6.2.13 QEI Digital filter on phase A input register

This register contains the sampling count for the digital filter. A sampling count of zero bypasses the filter.

Table 590. QEI Digital filter on phase A input register (FILTERPHA - 0x400C 603C) bit description

Bit	Symbol	Description	Reset value
31:0	FILTA	Digital filter sampling delay	0x0

27.6.2.14 QEI Digital filter on phase B input register

This register contains the sampling count for the digital filter. A sampling count of zero bypasses the filter.

Table 591. QEI Digital filter on phase B input register (FILTERPHB - 0x400C 6040) bit description

Bit	Symbol	Description	Reset value
31:0	FILTB	Digital filter sampling delay	0x0

27.6.2.15 QEI Digital filter on index input register

This register contains the sampling count for the digital filter. A sampling count of zero bypasses the filter.

Table 592. QEI Digital filter on index input register (FILTERINX - 0x400C 6044) bit description

Bit	Symbol	Description	Reset value
31:0	FITLINX	Digital filter sampling delay	0x0

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27.6.2.16 QEI Index acceptance window register

This register contains the width of the index acceptance window, when the index and the phase / clock edges fall nearly together. If the activating phase / clock edge falls before the Index, but within the window, the (re)calibration will be activated on that clock/phase edge.

Table 593. QEI Index acceptance window register (WINDOW - 0x400C 6048) bit description

Bit	Symbol	Description	Reset value
31:0	WINDOW	Index acceptance window width	0x0

27.6.2.17 QEI Index Compare register 1

This register contains an index compare value. This value is compared against the current value of the index count register. Interrupts can be enabled to interrupt when the compare value is less than, equal to, or greater than the current value of the index count register.

Table 594. QEI Index Compare register 1 (INXCMP1 - address 0x400C 604C) bit description

Bit	Symbol	Description	Reset value
31:0	ICMP1	Index compare value 1.	0xFFFF FFFF

27.6.2.18 QEI Index Compare register 2

This register contains an index compare value. This value is compared against the current value of the index count register. Interrupts can be enabled to interrupt when the compare value is less than, equal to, or greater than the current value of the index count register.

Table 595. QEI Index Compare register 0 (INXCMP2 - address 0x400C 6050) bit description

Bit	Symbol	Description	Reset value
31:0	ICMP2	Index compare value 2.	0xFFFF FFFF

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27.6.3 Interrupt registers

27.6.3.1 QEI Interrupt Enable Clear register

Writing a 1 to a bit in this register clears the corresponding bit in the QEI Interrupt Enable register (QEIIE).

Table 596: QEI Interrupt Enable Clear register (IEC - address 0x400C 6FD8) bit description

Bit	Symbol	Description	Reset value
0	INX_EN	Indicates that an index pulse was detected.	0
1	TIM_EN	Indicates that a velocity timer overflow occurred	0
2	VELC_EN	Indicates that captured velocity is less than compare velocity.	0
3	DIR_EN	Indicates that a change of direction was detected.	0
4	ERR_EN	Indicates that an encoder phase error was detected.	0
5	ENCLK_EN	Indicates that and encoder clock pulse was detected.	0
6	POS0_Int	Indicates that the position 0 compare value is equal to the current position.	0
7	POS1_Int	Indicates that the position 1compare value is equal to the current position.	0
8	POS2_Int	Indicates that the position 2 compare value is equal to the current position.	0
9	REV_Int	Indicates that the index compare value is equal to the current index count.	0
10	POS0REV_Int	Combined position 0 and revolution count interrupt. Set when both the POS0_Int bit is set and the REV_Int is set.	0
11	POS1REV_Int	Combined position 1 and revolution count interrupt. Set when both the POS1_Int bit is set and the REV_Int is set.	0
12	POS2REV_Int	Combined position 2 and revolution count interrupt. Set when both the POS2_Int bit is set and the REV_Int is set.	0
13	REV1_Int	Indicates that the index 1 compare value is equal to the current index count.	0
14	REV2_Int	Indicates that the index 2 compare value is equal to the current index count.	0
15	MAXPOS_Int	Indicates that the current position count goes through the MAXPOS value to zero in forward direction, or through zero to MAXPOS in backward direction.	0
31:16	-	Reserved	0

27.6.3.2 QEI Interrupt Enable Set register

Writing a 1 to a bit in this register sets the corresponding bit in the QEI Interrupt Enable register (QEIIE).

Table 597: QEI Interrupt Enable Set register (IES - address 0x400C 6FDC) bit description

Bit	Symbol	Description	Reset value
0	INX_EN	Indicates that an index pulse was detected.	0
1	TIM_EN	Indicates that a velocity timer overflow occurred	0
2	VELC_EN	Indicates that captured velocity is less than compare velocity.	0
3	DIR_EN	Indicates that a change of direction was detected.	0
4	ERR_EN	Indicates that an encoder phase error was detected.	0
5	ENCLK_EN	Indicates that and encoder clock pulse was detected.	0
6	POS0_Int	Indicates that the position 0 compare value is equal to the current position.	0
7	POS1_Int	Indicates that the position 1compare value is equal to the current position.	0

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Table 597: QEI Interrupt Enable Set register (IES - address 0x400C 6FDC) bit description

Bit	Symbol	Description	Reset value
8	POS2_Int	Indicates that the position 2 compare value is equal to the current position.	0
9	REV_Int	Indicates that the index compare value is equal to the current index count.	0
10	POS0REV_Int	Combined position 0 and revolution count interrupt. Set when both the POS0_Int bit is set and the REV_Int is set.	0
11	POS1REV_Int	Combined position 1 and revolution count interrupt. Set when both the POS1_Int bit is set and the REV_Int is set.	0
12	POS2REV_Int	Combined position 2 and revolution count interrupt. Set when both the POS2_Int bit is set and the REV_Int is set.	0
13	REV1_Int	Indicates that the index 1 compare value is equal to the current index count.	0
14	REV2_Int	Indicates that the index 2 compare value is equal to the current index count.	0
15	MAXPOS_Int	Indicates that the current position count goes through the MAXPOS value to zero in forward direction, or through zero to MAXPOS in backward direction.	0
31:16	-	Reserved	0

27.6.3.3 QEI Interrupt Status register

This register provides the status of the encoder interface and the current set of interrupt sources that are asserted to the controller. Bits set to 1 indicate the latched events that have occurred; a zero bit indicates that the event in question has not occurred. Writing a 0 to a bit position clears the corresponding interrupt.

Table 598: QEI Interrupt Status register (INTSTAT - address 0x400C 6FE0) bit description

Bit	Symbol	Description	Reset value
0	INX_Int	Indicates that an index pulse was detected.	0
1	TIM_Int	Indicates that a velocity timer overflow occurred	0
2	VELC_Int	Indicates that captured velocity is less than compare velocity.	0
3	DIR_Int	Indicates that a change of direction was detected.	0
4	ERR_Int	Indicates that an encoder phase error was detected.	0
5	ENCLK_Int	Indicates that and encoder clock pulse was detected.	0
6	POS0_Int	Indicates that the position 0 compare value is equal to the current position.	0
7	POS1_Int	Indicates that the position 1compare value is equal to the current position.	0
8	POS2_Int	Indicates that the position 2 compare value is equal to the current position.	0
9	REV_Int	Indicates that the index compare value is equal to the current index count.	0
10	POS0REV_Int	Combined position 0 and revolution count interrupt. Set when both the POS0_Int bit is set and the REV_Int is set.	0
11	POS1REV_Int	Combined position 1 and revolution count interrupt. Set when both the POS1_Int bit is set and the REV_Int is set.	0
12	POS2REV_Int	Combined position 2 and revolution count interrupt. Set when both the POS2_Int bit is set and the REV_Int is set.	0
13	REV1_Int	Indicates that the index 1 compare value is equal to the current index count.	0
14	REV2_Int	Indicates that the index 2 compare value is equal to the current index count.	0
15	MAXPOS_Int	Indicates that the current position count goes through the MAXPOS value to zero in forward direction, or through zero to MAXPOS in backward direction.	0
31:16	-	Reserved	0

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27.6.3.4 QEI Interrupt Enable register

This register enables interrupt sources. Bits set to 1 enable the corresponding interrupt; a 0 bit disables the corresponding interrupt.

Table 599: QEI Interrupt Enable register (IE - address 0x400C 6FE4) bit description

Bit	Symbol	Description	Reset value
0	INX_Int	Indicates that an index pulse was detected.	0
1	TIM_Int	Indicates that a velocity timer overflow occurred	0
2	VELC_Int	Indicates that captured velocity is less than compare velocity.	0
3	DIR_Int	Indicates that a change of direction was detected.	0
4	ERR_Int	Indicates that an encoder phase error was detected.	0
5	ENCLK_Int	Indicates that and encoder clock pulse was detected.	0
6	POS0_Int	Indicates that the position 0 compare value is equal to the current position.	0
7	POS1_Int	Indicates that the position 1compare value is equal to the current position.	0
8	POS2_Int	Indicates that the position 2 compare value is equal to the current position.	0
9	REV_Int	Indicates that the index compare value is equal to the current index count.	0
10	POS0REV_Int	Combined position 0 and revolution count interrupt. Set when both the POS0_Int bit is set and the REV_Int is set.	0
11	POS1REV_Int	Combined position 1 and revolution count interrupt. Set when both the POS1_Int bit is set and the REV_Int is set.	0
12	POS2REV_Int	Combined position 2 and revolution count interrupt. Set when both the POS2_Int bit is set and the REV_Int is set.	0
13	REV1_Int	Indicates that the index 1 compare value is equal to the current index count.	0
14	REV2_Int	Indicates that the index 2 compare value is equal to the current index count.	0
15	MAXPOS_Int	Indicates that the current position count goes through the MAXPOS value to zero in forward direction, or through zero to MAXPOS in backward direction.	0
31:16	-	Reserved	0

27.6.3.5 QEI Interrupt Clear register

Writing a 1 to a bit in this register clears the corresponding bit in the QEI Interrupt Status register (QEISTAT).

Table 600: QEI Interrupt Clear register (CLR - 0x400C 6FE8) bit description

Bit	Symbol	Description	Reset value
0	INX_Int	Indicates that an index pulse was detected.	0
1	TIM_Int	Indicates that a velocity timer overflow occurred	0
2	VELC_Int	Indicates that captured velocity is less than compare velocity.	0
3	DIR_Int	Indicates that a change of direction was detected.	0
4	ERR_Int	Indicates that an encoder phase error was detected.	0
5	ENCLK_Int	Indicates that and encoder clock pulse was detected.	0
6	POS0_Int	Indicates that the position 0 compare value is equal to the current position.	0
7	POS1_Int	Indicates that the position 1compare value is equal to the current position.	0
8	POS2_Int	Indicates that the position 2 compare value is equal to the current position.	0
9	REV_Int	Indicates that the index compare value is equal to the current index count.	0

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Table 600: QEI Interrupt Clear register (CLR - 0x400C 6FE8) bit description

Bit	Symbol	Description	Reset value
10	POS0REV_Int	Combined position 0 and revolution count interrupt. Set when both the POS0_Int bit is set and the REV_Int is set.	0
11	POS1REV_Int	Combined position 1 and revolution count interrupt. Set when both the POS1_Int bit is set and the REV_Int is set.	0
13	REV1_Int	Indicates that the index 1 compare value is equal to the current index count.	0
14	REV2_Int	Indicates that the index 2 compare value is equal to the current index count.	0
15	MAXPOS_Int	Indicates that the current position count goes through the MAXPOS value to zero in forward direction, or through zero to MAXPOS in backward direction.	0
31:16	-	Reserved	0

27.6.3.6 QEI Interrupt Set register

Writing a one to a bit in this register sets the corresponding bit in the QEI Interrupt Status register (STAT).

Table 601: QEI Interrupt Set register (SET - address 0x400C 6FEC) bit description

Bit	Symbol	Description	Reset value
0	INX_Int	Indicates that an index pulse was detected.	0
1	TIM_Int	Indicates that a velocity timer overflow occurred	0
2	VELC_Int	Indicates that captured velocity is less than compare velocity.	0
3	DIR_Int	Indicates that a change of direction was detected.	0
4	ERR_Int	Indicates that an encoder phase error was detected.	0
5	ENCLK_Int	Indicates that and encoder clock pulse was detected.	
6	POS0_Int	Indicates that the position 0 compare value is equal to the current position.	0
7	POS1_Int	Indicates that the position 1compare value is equal to the current position.	0
8	POS2_Int	Indicates that the position 2 compare value is equal to the current position.	0
9	REV_Int	Indicates that the index compare value is equal to the current index count.	0
10	POS0REV_Int	Combined position 0 and revolution count interrupt. Set when both the POS0_Int bit is set and the REV_Int is set.	0
11	POS1REV_Int	Combined position 1 and revolution count interrupt. Set when both the POS1_Int bit is set and the REV_Int is set.	0
12	POS2REV_Int	Combined position 2 and revolution count interrupt. Set when both the POS2_Int bit is set and the REV_Int is set.	0
13	REV1_Int	Indicates that the index 1 compare value is equal to the current index count.	0
14	REV2_Int	Indicates that the index 2 compare value is equal to the current index count.	0
15	MAXPOS_Int	Indicates that the current position count goes through the MAXPOS value to zero in forward direction, or through zero to MAXPOS in backward direction.	0
31:16	-	Reserved	0

27.7 Functional description

The QEI module interprets the two-bit gray code produced by a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, it can capture the velocity of the encoder wheel.

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27.7.1 Input signals

The QEI module supports two modes of signal operation: quadrature phase mode and clock/direction mode. In quadrature phase mode, the encoder produces two clocks that are 90 degrees out of phase; the edge relationship is used to determine the direction of rotation. In clock/direction mode, the encoder produces a clock signal to indicate steps and a direction signal to indicate the direction of rotation.).

This mode is determined by the SigMode bit of the QEI Control (CON) register (See Table 575). When the SigMode bit = 1, the quadrature decoder is bypassed and the PhA pin functions as the direction signal and PhB pin functions as the clock signal for the counters, etc. When the SigMode bit = 0, the PhA pin and PhB pins are decoded by the quadrature decoder. In this mode the quadrature decoder produces the direction and clock signals for the counters, etc. In both modes the direction signal is subject to the effects of the direction invert (DIRINV) bit.

27.7.1.1 Quadrature input signals

When edges on PhA lead edges on PhB, the position counter is incremented. When edges on PhB lead edges on PhA, the position counter is decremented. When a rising and falling edge pair is seen on one of the phases without any edges on the other, the direction of rotation has changed.

Table 602. Encoder states

Phase A	Phase B	state
1	0	1
1	1	2
0	1	3
0	0	4

Table 603. Encoder state transitions[1]

from state	to state	Direction
1	2	positive
2	3	
3	4	
4	1	
4	3	negative
3	2	
2	1	
1	4	

[1] All other state transitions are illegal and should set the ERR bit.

Interchanging of the PhA and PhB input signals are compensated by complementing the DIR bit. When set = 1, the direction inversion bit (DIRINV) complements the DIR bit.

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Table 604. Encoder direction

DIR bit	DIRINV bit	direction
0	0	forward
1	0	reverse
0	1	reverse
1	1	forward

Figure 81 shows how quadrature encoder signals equate to direction and count.

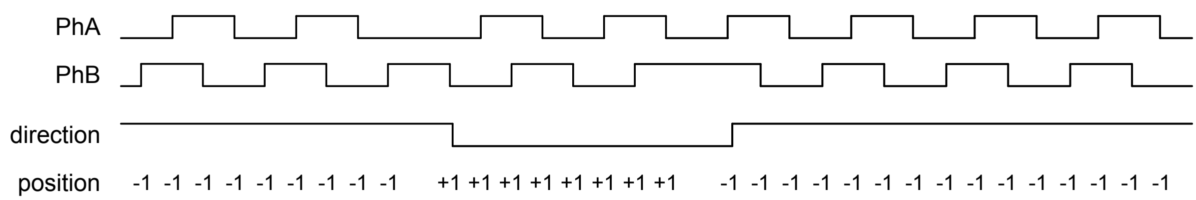


Fig 81. Quadrature Encoder Basic Operation

27.7.1.2 Digital input filtering

All three encoder inputs (PhA, PhB, and index) require digital filtering. The number of sample clocks is user programmable from 1 to 4,294,967,295 (0xFFFF FFFF). In order for a transition to be accepted, the input signal must remain in new state for the programmed number of sample clocks.

27.7.2 Position capture

The capture mode for the position integrator can be set to update the position counter on every edge of the PhA signal or to update on every edge of both PhA and PhB. Updating the position counter on every PhA and PhB provides more positional resolution at the cost of less range in the positional counter.

The position integrator and velocity capture can be independently enabled. Alternatively, the phase signals can be interpreted as a clock and direction signal as output by some encoders.

The position counter is automatically reset on one of three conditions. Incrementing past the maximum position value (MAXPOS) will reset the position counter to zero. If the reset on index bit (RESPI) is set, sensing the index pulse for the first time will once reset the position counter to zero after the next positional increase (calibrate). If the continuously reset on index bit (CRESPI) is set, sensing the index pulse will continuously reset the position counter to zero after the next positional increase (recalibrate).

27.7.3 Velocity capture

The velocity capture has a programmable timer and a capture register. It counts the number of phase edges (using the same configuration as for the position integrator) in a given time period. When the velocity timer (TIME) overflows the contents of the velocity counter (VEL) are transferred to the capture (CAP) register. The velocity counter is then

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cleared. The velocity timer is loaded with the contents of the velocity reload register (LOAD). Finally, the velocity interrupt (TIM_Int) is asserted. The number of edges counted in a given time period is directly proportional to the velocity of the encoder.

Setting the reset velocity bit (RESV) will clear the velocity counter, reset the velocity capture register to 0xFFFF FFFF, and load the velocity timer with the contents of the velocity reload register (LOAD).

The following equation converts the velocity counter value into an RPM value:

RPM = (PCLK × Speed × 60) / Load × PPR × Edges)

where:

- PCLK is the QEI controller clock.
- PPR is the number of pulses per revolution of the physical encoder.
- Edges is 2 or 4, based on the capture mode set in the CON register (2 for CapMode set to 0 and 4 for CapMode set to 1)

For example, consider a motor running at 600 rpm. A 2048 pulse per revolution quadrature encoder is attached to the motor, producing 8192 phase edges per revolution. With clocking on both PhA and PhB edges, this results in 81,920 pulses per second (the motor turns 10 times per second). If the timer were clocked at 10,000 Hz, and the load value was 2,500 (¼ of a second), it would count 20,480 pulses per update. Using the above equation:

RPM = (10000 × 20480 × 60) / (2500 × 2048 × 4) = 600 RPM

Now, consider that the motor is sped up to 3000 RPM. This results in 409,600 pulses per second, or 102,400 every ¼ of a second. Again, the above equation gives:

RPM = (10000 × 102400 × 60) / (2500 × 2048 × 4) = 3000 RPM

27.7.4 Velocity compare

In addition to velocity capture, the velocity measurement system includes a programmable velocity compare register. After every velocity capture event the contents of the velocity capture register (CAP) is compared with the contents of the velocity compare register (VELCOMP). If the captured velocity is less than the compare value an interrupt is asserted provided that the velocity compare interrupt enable bit is set. This can be used to determine if a motor shaft is either stalled or moving too slow.

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28.1 How to read this chapter

The RIT is available on all LPC18xx parts.

28.2 Basic configuration

The RIT is configured as follows:

- See Table 605 for clocking and power control.
- The RIT is reset by the RITIMER_RST (reset #36).
- The RIT interrupt is connected to slot # 11 in the NVIC.

Table 605. RIT clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to the RI timer register interface and RI timer peripheral clock.	BASE_M3_CLK	CLK_M3_RITIMER	150 MHz

28.3 Features

- 32-bit counter running from PCLK. Counter can be free-running, or be reset by a generated interrupt.
- 32-bit compare value.
- 32-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.

28.4 General description

The Repetitive Interrupt Timer provides a versatile means of generating interrupts at specified time intervals, without using a standard timer. It is intended for repeating interrupts that aren’t related to Operating System interrupts. However, it could be used as an alternative to the Cortex-M3 System Tick Timer if there are different system requirements.

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28.5 Register description

Table 606. Register overview: Repetitive Interrupt Timer (RIT) (base address 0x400C 0000)

Name	Access	Address	Description	Reset value[1]
COMPVAL	R/W	0x000	Compare register	0xFFFF FFFF
MASK	R/W	0x004	Mask register. This register holds the 32-bit mask value. A ‘1’ written to any bit will force a compare on the corresponding bit of the counter and compare register.	0
CTRL	R/W	0x008	Control register.	0xC
COUNTER	R/W	0x00C	32-bit counter	0

[1] Reset Value reflects the data stored in used bits only. It does not include content of reserved bits.

28.5.1 RI Compare Value register

Table 607. RI Compare Value register (COMPVAL - address 0x400C 0000) bit description

Bit	Symbol	Description	Reset value
31:0	RICOMP	Compare register. Holds the compare value which is compared to the counter.	0xFFFF FFFF

28.5.2 RI Mask register

Table 608. RI Mask register (MASK - address 0x400C 0004) bit description

Bit	Symbol	Description	Reset value
31:0	RIMASK	Mask register. This register holds the 32-bit mask value. A one written to any bit overrides the result of the comparison for the corresponding bit of the counter and compare register (causes the comparison of the register bits to be always true).	0

28.5.3 RI Control register

Table 609. RI Control register (CTRL - address 0x400C 0008) bit description

Bit	Symbol	Value	Description	Reset value
0	RITINT		Interrupt flag	0
		1	This bit is set to 1 by hardware whenever the counter value equals the masked compare value specified by the contents of RICOMPVAL and RIMASK registers. Writing a 1 to this bit will clear it to 0. Writing a 0 has no effect.	
		0	The counter value does not equal the masked compare value.	
1	RITENCLR		Timer enable clear	
		1	The timer will be cleared to 0 whenever the counter value equals the masked compare value specified by the contents of RICOMPVAL and RIMASK registers. This will occur on the same clock that sets the interrupt flag.	0
		0	The timer will not be cleared to 0.	

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Table 609. RI Control register (CTRL - address 0x400C 0008) bit description

Bit	Symbol	Value	Description	Reset value
2	RITENBR		Timer enable for debug	1
		1	The timer is halted when the processor is halted for debugging.	
		0	Debug has no effect on the timer operation.	
3	RITEN		Timer enable.	1
		1	Timer enabled. **Remark:** This can be overruled by a debug halt if enabled in bit 2.	
		0	Timer disabled.	
31:4	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

28.5.4 RI Counter register

Table 610. RI Counter register (COUNTER - address 0x400C 000C) bit description

Bit	Symbol	Description	Reset value
31:0	RICOUNTER	32-bit up counter. Counts continuously unless RITEN bit in RICTRL register is cleared or debug mode is entered (if enabled by the RITNEBR bit in RICTRL). Can be loaded to any value in software.	0

28.6 RI timer operation

Following reset, the counter begins counting up from 0x00000000. Whenever the counter value equals the value programmed into the RICOMPVAL register the interrupt flag will be set. Any bit or combination of bits can be removed from this comparison (i.e. forced to compare) by writing a ‘1’ to the corresponding bit(s) in the RIMASK register. If the enable_clr bit is low (default state), a valid comparison ONLY causes the interrupt flag to be set. It has no effect on the count sequence. Counting continues as usual. When the counter reaches 0xFFFFFFFF it rolls-over to 0x00000000 on the next clock and continues counting. If the enable_clr bit is set to ‘1’ a valid comparison will also cause the counter to be reset to zero. Counting will resume from there on the next clock edge.

Counting can be halted in software by writing a ‘0’ to the Enable_Timer bit - RICTRL(2). Counting will also be halted when the processor is halted for debugging provided the Enable_Break bit – RICTRL(1) is set. Both the Enable_Timer and Enable_Break bits are set on reset.

The interrupt flag can be cleared in software by writing a ‘1’ to the Interrupt bit – RICTRL(0).

Software can load the counter to any value at any time by writing to RICOUNTER.

The counter (RICOUNTER), RICOMPVAL register, RIMASK register and RICTRL register can all be read by software at any time.

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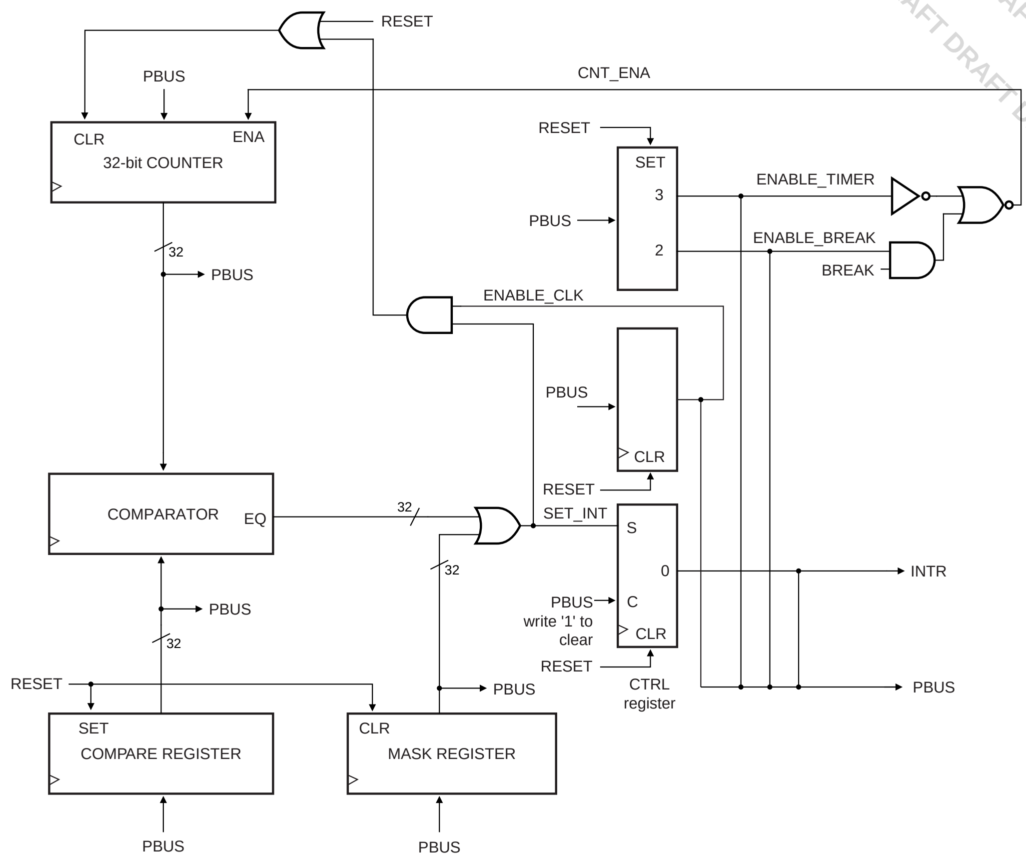


Fig 82. RI timer block diagram

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29.1 How to read this chapter

The Alarm timer is identical on all LPC18xx parts.

29.2 Basic configuration

The Alarm timer is configured as follows:

- See Table 611 for clocking and power control. The 32 kHz output of the 32 kHz oscillator must be enabled in the CREG0 register in the CREG block (see Table 31).
-
- The Alarm timer interrupt is connected to slot # 4 in the Event router.

Table 611. Alarm timer clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to alarm timer register interface	BASE_M3_CLK	CLK_M3_BUS	150 MHz
32 kHz crystal oscillator output for the counter/timer clock	-	-	1024 Hz (fixed frequency)

29.3 General description

The alarm timer is a 16-bit timer and counts down from a preset value. The counter triggers a status bit when it reaches 0x00 and asserts an interrupt if enabled.

The alarm timer operates in the RTC power domain. It consists of a 16-bit counter (DOWNCOUNTER) running at a 1024 Hz clock. The 1024 Hz clock is derived from the 32 kHz crystal clock. The alarm timer is inactive when this clock is not active.

The alarm timer counts down from an initial value PRESET. When it reaches 0x0 and the interrupt is enabled (via SET_EN), bit STATUS is triggered. The counter continues counting down starting from PRESET.

STATUS is propagated to the interrupt output. The interrupt is connected to the Event router and can be used to wake up the device from a low power mode.

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29.4 Register description

Table 612. Register overview: Alarm timer (base address 0x4004 0000)

Name	Access	Address offset	Description	Reset Value
DOWNCOUNTER	R/W	0x000	Downcounter register	0x000
PRESET	R/W	0x004	Preset value register	0x000
-	-	0x008 - 0xFD4	Reserved	-
CLR_EN	W	0xFD8	Interrupt clear enable register	0x0
SET_EN	W	0xFDC	Interrupt set enable register	0x0
STATUS	R	0xFE0	Status register	0x0
ENABLE	R	0xFE4	Enable register	0x0
CLR_STAT	W	0xFE8	Clear register	0x0
SET_STAT	W	0xFEC	Set register	0x0

29.4.1 Downcounter register

Table 613. Downcounter register (DOWNCOUNTER - 0x4004 0000) bit description

Bit	Symbol	Description	Reset value
15:0	CVAL	When equal to zero an interrupt is raised. When equal to zero PRESET is loaded and counting continues.	0x0
31:16	-	Reserved.	-

29.4.2 Preset value register

Table 614. Preset value register (PRESET - 0x4004 0004) bit description

Bit	Symbol	Description	Reset value
15:0	PRESETVAL	Value loaded in DOWNCOUNTER when DOWNCOUNTER equals zero	
31:16	-	Reserved.	-

29.4.3 Interrupt clear enable register

Table 615. Interrupt clear enable register (CLR_EN - 0x4004 0FD8) bit description

Bit	Symbol	Description	Reset value
0	CLR_EN	Writing a 1 to this bit clears the interrupt enable bit in the ENABLE register.	-
31:1	-	Reserved.	-

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29.4.4 Interrupt set enable register

Table 616. Interrupt set enable register (SET_EN - 0x4004 0FDC) bit description

Bit	Symbol	Description	Reset value
0	SET_EN	Writing a 1 to this bit sets the interrupt enable bit in the ENABLE register.	0
31:1	-	Reserved.	-

29.4.5 Interrupt status register

Table 617. Interrupt status register (STATUS - 0x4004 0FE0) bit description

Bit	Symbol	Description	Reset value
0	STAT	A 1 in this bit shows that the STATUS interrupt has been raised.	0
31:1	-	Reserved.	-

29.4.6 Interrupt enable register

Table 618. Interrupt enable register (ENABLE - 0x4004 0FE4) bit description

Bit	Symbol	Description	Reset value
0	EN	A 1 in this bit shows that the STATUS interrupt has been enabled and that the STATUS interrupt request signal is asserted when STAT = 1 in the STATUS register.	0
31:1	-	Reserved.	-

29.4.7 Clear status register

Table 619. Interrupt clear status register (CLR_STAT - 0x4004 0FE8) bit description

Bit	Symbol	Description	Reset value
0	CSTAT	Writing a 1 to this bit clears the STATUS interrupt bit in the STATUS register.	0
31:1	-	Reserved.	-

29.4.8 Set status register

Table 620. Interrupt set status register (SET_STAT - 0x4004 0FEC) bit description

Bit	Symbol	Description	Reset value
0	SSTAT	Writing a 1 to this bit sets the STATUS interrupt bit in the STATUS register.	0
31:1	-	Reserved.	-

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30.1 How to read this chapter

The WWDT is identical for all LPC18xx parts.

30.2 Basic configuration

The WWDT is configured as follows:

- See Table 621 for clocking and power control. The only clock source for the WWDT clock (WDCLK) is the IRC.
- The WWDT cannot be reset by software.
- The WWDT interrupt is connected to slot # 7 in the Event router.

Table 621. WWDT clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to WWDT register interface (PCLK)	BASE_M3_CLK	CLK_M3_WWDT	150 MHz
Watchdog clock (WDCLK)	BASE_SAFE_CLK	-	12 MHz (fixed frequency)

30.3 Features

- Internally resets chip if not reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time-out period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Programmable 24 bit timer with internal fixed pre-scaler.
- Selectable time period from 1,024 watchdog clocks ($T_{WDCLK} \times 256 \times 4$) to over 67 million watchdog clocks ($T_{WDCLK} \times 2^{24} \times 4$) in increments of 4 watchdog clocks.
- Safe watchdog operation. Once enabled, requires a hardware reset or a Watchdog reset to be disabled.
- Incorrect feed sequence causes immediate watchdog reset if enabled.
- The watchdog reload value can optionally be protected such that it can only be changed after the “warning interrupt” time is reached.
- Flag to indicate Watchdog reset.
- The WWDT uses the IRC as a fixed clock source.

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30.4 Applications

The purpose of the Watchdog Timer is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, a watchdog event will be generated if the user program fails to feed (or reload) the Watchdog within a predetermined amount of time. The Watchdog event will cause a chip reset if configured to do so.

When a watchdog window is programmed, an early watchdog feed is also treated as a watchdog event. This allows preventing situations where a system failure may still feed the watchdog. For example, application code could be stuck in an interrupt service that contains a watchdog feed. Setting the window such that this would result in an early feed will generate a watchdog event, allowing for system recovery.

30.5 Description

The Watchdog consists of a fixed divide by 4 pre-scaler and a 24-bit counter which decrements on every clock cycle. The minimum value from which the counter decrements is 0xFF. Setting a value lower than 0xFF causes 0xFF to be loaded in the counter. Hence the minimum Watchdog interval is ($T_{WDCLK} \times 256 \times 4$) and the maximum Watchdog interval is ($T_{WDCLK} \times 2^{24} \times 4$) in multiples of ($T_{WDCLK} \times 4$). The Watchdog should be used in the following manner:

- Set the Watchdog time-out value in TC register.
- Setup the Watchdog timer operating mode in MOD register.
- Set a value for the watchdog window time in WINDOW register if windowed operation is required.
- Set a compare value for the watchdog warning interrupt in the WARNINT register if a warning interrupt is required.
- Enable the Watchdog by writing 0xAA followed by 0x55 to the FEED register.
- The Watchdog must be fed again before the Watchdog counter reaches zero in order to prevent a watchdog event. If a window value is programmed, the feed must also occur after the watchdog counter passes that value.

When the Watchdog Timer is configured so that a watchdog event will cause a reset and the counter reaches zero, the CPU will be reset, loading the stack pointer and program counter from the vector table as in the case of external reset. The Watchdog time-out flag (WDTOF) can be examined to determine if the Watchdog has caused the reset condition. The WDTOF flag must be cleared by software.

When the Watchdog Timer is configured to generate a warning interrupt, the interrupt will occur when the counter matches the compare value defined by the WARNINT register.

30.5.1 WWDT behavior in debug mode

If code execution is halted in Debug mode, the WWDT stops counting until code execution resumes.

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30.6 Clocking

The watchdog timer block uses two clocks: PCLK and WDCLK. PCLK is used for the APB accesses to the watchdog registers and is derived from the BASE_M3_CLK. The WDCLK is used for the watchdog timer counting and is derived from the IRC. The clock source (the IRC) is fixed to ensure that the WDT always has a valid clock.

There is some synchronization logic between these two clock domains. When the MOD and TC registers are updated by APB operations, the new value will take effect in three WDCLK cycles on the logic in the WDCLK clock domain. When the watchdog timer is counting the WDCLK clock cycles, the synchronization logic will first lock the value of the counter on WDCLK and then synchronize it with the PCLK for reading as the TV register by the CPU.

30.7 Register description

The Watchdog contains six registers as shown in Table 622 below.

Table 622. Register overview: Watchdog timer (base address 0x4008 0000)

Name	Access	Address offset	Description	Reset value[1]
MOD	R/W	0x000	Watchdog mode register. This register contains the basic mode and status of the Watchdog Timer.	0
TC	R/W	0x004	Watchdog timer constant register. This register determines the time-out value.	0xFF
FEED	WO	0x008	Watchdog feed sequence register. Writing 0xAA followed by 0x55 to this register reloads the Watchdog timer with the value contained in WDTC.	NA
TV	RO	0x00C	Watchdog timer value register. This register reads out the current value of the Watchdog timer.	0xFF
-	-	0x010	Reserved	-
WARNINT	R/W	0x014	Watchdog warning interrupt register. This register contains the Watchdog warning interrupt compare value.	0
WINDOW	R/W	0x018	Watchdog timer window register. This register contains the Watchdog window value.	0xFF FFFF

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

30.7.1 Watchdog mode register

The WDMOD register controls the operation of the Watchdog as per the combination of WDEN and RESET bits. Note that a watchdog feed must be performed before any changes to the WDMOD register take effect.

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Table 623. Watchdog Mode register (MOD - 0x4008 0000) bit description

Bit	Symbol	Value	Description	Reset value
0	WDEN		Watchdog enable bit. This bit is Set Only.	0
		0	The watchdog timer is stopped.	
		1	The watchdog timer is running.	
1	WDRESET		Watchdog reset enable bit. This bit is Set Only.	0
		0	A watchdog time-out will not cause a chip reset.	
		1	A watchdog time-out will cause a chip reset.	
2	WDTOF		Watchdog time-out flag. Set when the watchdog timer times out, by a feed error, or by events associated with WDPROTECT, cleared by software. Causes a chip reset if WDRESET = 1. This flag is cleared by software writing a 0 to this bit.	0 (Only after external reset)
3	WDINT		Watchdog interrupt flag. Set when the timer reaches the value in the WARNINT register. Cleared by software by writing a 1 to this bit.	0
4	WDPROTECT		Watchdog update mode. This bit is Set Only.	0
		0	The watchdog time-out value (WDTC) can be changed at any time.	
		1	The watchdog time-out value (WDTC) can be changed only after the counter is below the value of WDWARNINT and WDWINDOW.	
7:5	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Once the **WDEN**, **WDPROTECT**, or **WDRESET** bits are set they can not be cleared by software. Both flags are cleared by an external reset or a Watchdog timer reset.

WDTOF The Watchdog time-out flag is set when the Watchdog times out, when a feed error occurs, or when WDPROTECT =1 and an attempt is made to write to the TC register. This flag is cleared by software writing a 0 to this bit.

WDINT The Watchdog interrupt flag is set when the Watchdog counter reaches the value specified by WDWARNINT. This flag is cleared when any reset occurs, and is cleared by software by writing a 1 to this bit.

Watchdog reset or interrupt will occur any time the watchdog is running and has an operating clock source. Any clock source works in Sleep mode, and the IRC works in Deep-sleep mode. If a watchdog interrupt occurs in Sleep or Deep-sleep mode, it will wake up the device.

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Table 624. Watchdog operating modes selection

WDEN	WDRESET	Mode of Operation
0	X (0 or 1)	Debug/Operate without the Watchdog running.
1	0	Watchdog interrupt mode: the watchdog warning interrupt will be generated but watchdog reset will not. When this mode is selected, the watchdog counter reaching the value specified by WDWARNINT will set the WDINT flag and the Watchdog interrupt request will be generated.
1	1	Watchdog reset mode: Both the watchdog interrupt and watchdog reset are enabled. When this mode is selected, the watchdog counter reaching the value specified by WDWARNINT will set the WDINT flag and the Watchdog interrupt request will be generated. The watchdog counter reaching zero will reset the microcontroller. **Remark:** Other causes for a watchdog reset are: A watchdog feed or changing the WDTC value (if the WDPROTECT bit is set in the MOD register) before reaching the value of WDWINDOW.

30.7.2 Watchdog timer constant register

The TC register determines the time-out value. Every time a feed sequence occurs, the TC register content is reloaded into the Watchdog timer. This is pre-loaded with the value 0x00 00FF upon reset. Writing values below 0xFF will cause 0x00 00FF to be loaded into the TC register. Thus the minimum time-out interval is $T_{WDCLK} \times 256 \times 4$.

If the WDPROTECT bit in MOD register is set to one, an attempt to change the value of TC before the watchdog counter is below the values of WDWARNINT and WDWINDOW will cause a watchdog reset and set the WDTOF flag.

Table 625. Watchdog Timer Constant register (TC - 0x4008 0004) bit description

Bit	Symbol	Description	Reset value
23:0	WDTC	Watchdog time-out value.	0x00 00FF
31:24	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

30.7.3 Watchdog feed register

Writing 0xAA followed by 0x55 to this register will reload the Watchdog timer with the time-out value in the TC register. This operation will also start the Watchdog if it is enabled via the MOD register. Setting the WDEN bit in the WDMOD register is not sufficient to enable the Watchdog. A valid feed sequence must be completed after setting WDEN before the Watchdog is capable of generating a reset. Until then, the Watchdog will ignore feed errors. After writing 0xAA to FEED register, access to any Watchdog register other than writing 0x55 to FEED register causes an immediate reset/interrupt when the Watchdog is enabled, and sets the WDTOF flag. The reset will be generated during the second PCLK following an incorrect access to a Watchdog register during a feed sequence.

Interrupts should be disabled during the feed sequence. An abort condition will occur if an interrupt happens during the feed sequence.

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Table 626. Watchdog Feed register (FEED - 0x4008 0008) bit description

Bit	Symbol	Description	Reset value
7:0	Feed	Feed value should be 0xAA followed by 0x55.	NA

30.7.4 Watchdog timer value register

The WDTV register is used to read the current value of Watchdog timer counter.

When reading the value of the 24 bit counter, the lock and synchronization procedure takes up to 6 WDCLK cycles plus 6 PCLK cycles, so the value of WDTV is older than the actual value of the timer when it's being read by the CPU.

Table 627. Watchdog Timer Value register (TV - 0x4008 000C) bit description

Bit	Symbol	Description	Reset value
23:0	Count	Counter timer value.	0x00 00FF
31:24	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

30.7.5 Watchdog timer warning interrupt register

The WDWARNINT register determines the watchdog timer counter value that will generate a watchdog interrupt. When the watchdog timer counter matches the value defined by WDWARNINT, an interrupt will be generated after the subsequent WDCLK.

A match of the watchdog timer counter to WDWARNINT occurs when the bottom 10 bits of the counter have the same value as the 10 bits of WARNINT, and the remaining upper bits of the counter are all 0. This gives a maximum time of 1,023 watchdog timer counts (4,096 watchdog clocks) for the interrupt to occur prior to a watchdog event. If WDWARNINT is set to 0, the interrupt will occur at the same time as the watchdog event.

Table 628. Watchdog Timer Warning Interrupt register (WARNINT - 0x4008 0014) bit description

Bit	Symbol	Description	Reset value
9:0	WDWARNINT	Watchdog warning interrupt compare value.	0
31:10	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

30.7.6 Watchdog timer window register

The WDWINDOW register determines the highest WDTV value allowed when a watchdog feed is performed. If a feed valid sequence completes prior to WDTV reaching the value in WDWINDOW, a watchdog event will occur.

WDWINDOW resets to the maximum possible WDTV value, so windowing is not in effect. Values of WDWINDOW below 0x100 will make it impossible to ever feed the watchdog successfully.

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Table 629. Watchdog Timer Window register (WINDOW - 0x4008 0018) bit description

Bit	Symbol	Description	Reset value
23:0	WDWINDOW	Watchdog window value.	0xFF FFFF
31:24	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

30.8 Block diagram

The block diagram of the Watchdog is shown below in the Figure 83. The synchronization logic (PCLK - WDCLK) is not shown in the block diagram.

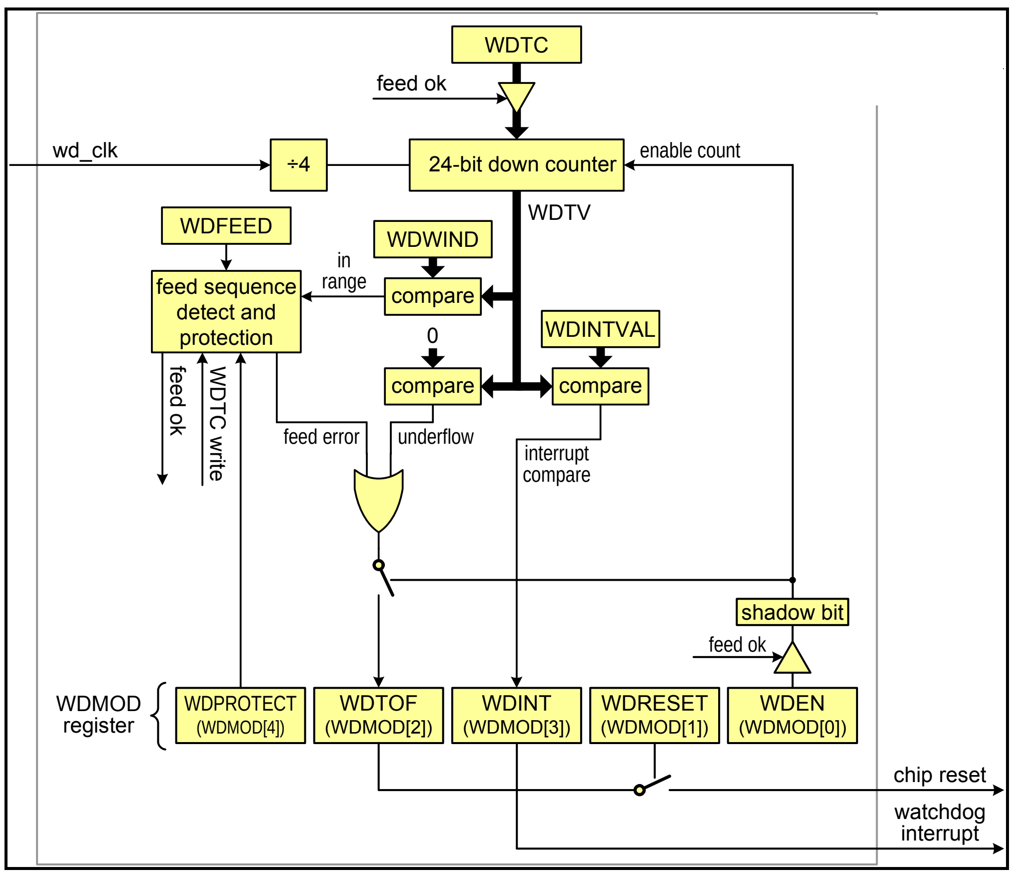


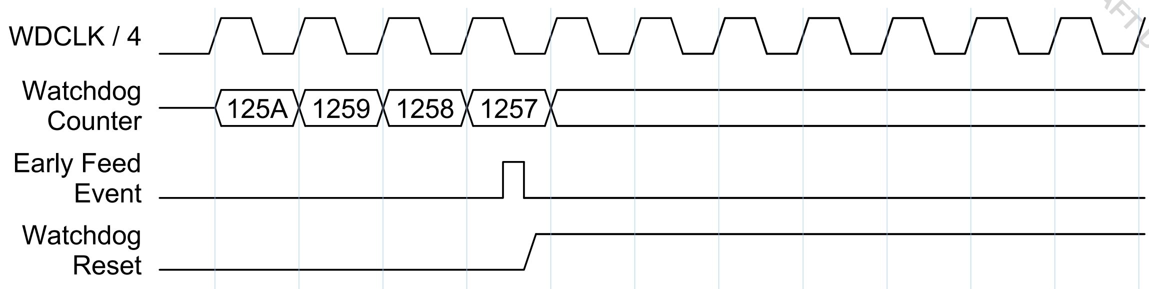
Fig 83. Watchdog block diagram

30.9 Watchdog timing examples

The following figures illustrate several aspects of Watchdog Timer operation is shown below in Figure 84.

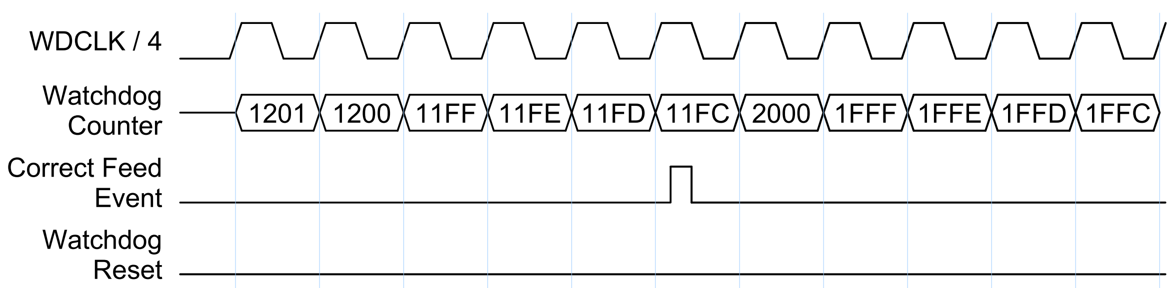
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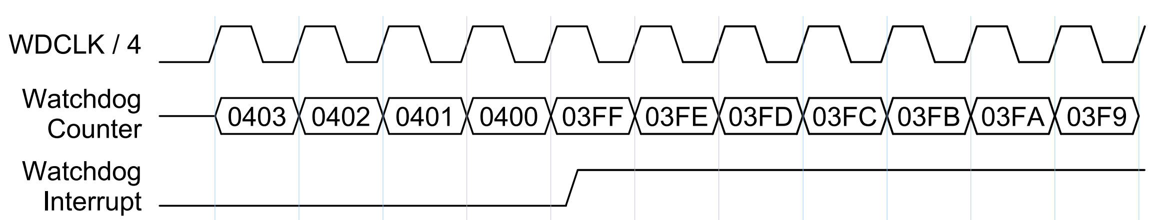
Conditions:
WDWINDOW = 0x1200
WDWARNINT = 0x3FF
WDTC = 0x2000

Fig 84. Early Watchdog Feed with Windowed Mode Enabled



Conditions:
WDWINDOW = 0x1200
WDWARNINT = 0x3FF
WDTC = 0x2000

Fig 85. Correct Watchdog Feed with Windowed Mode Enabled



Conditions:
WDWINDOW = 0x1200
WDWARNINT = 0x3FF
WDTC = 0x2000

Fig 86. Watchdog Warning Interrupt

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31.1 How to read this chapter

On parts LPC1850/30/20/10 Rev ‘A’, the function of the alarm pin RTC_ALARM must be configured in the CREG0 register (Table 31).

31.2 Basic configuration

The RTC is configured as follows:

- See Table 630 for clocking and power control. The 1 kHz output of the 32 kHz oscillator must be enabled in the CREG0 register in the CREG block (see Table 31).
- The RTC interrupt is connected to slot # 5 in the Event router.
-

Remark: After initializing the 32 kHZ oscillator, wait for 2 sec before writing to the RTC registers.

Table 630. RTC clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to alarm timer register interface	BASE_M3_CLK	CLK_M3_BUS	150 MHz
32 kHz crystal oscillator output for the counter/timer clock	-	-	1024 Hz (fixed frequency)

31.3 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.
- Ultra-low power design to support battery powered systems. Uses power from the CPU power supply when it is present.
- Dedicated battery power supply pin.
- RTC power supply is isolated from the rest of the chip.
- Calibration counter allows adjustment to better than ±1 sec/day with 1 sec resolution.
- Periodic interrupts can be generated from increments of any field of the time registers and selected fractional second values.
- Alarm interrupt can be generated for a specific date/time.

31.4 General description

The Real Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses very little power when its registers are not being accessed by the CPU, especially reduced power modes. On the LPC18xx, the RTC is clocked by a separate 32 kHz oscillator that produces a 1 Hz internal time reference. The RTC is powered by its own power supply pin, VBAT, .

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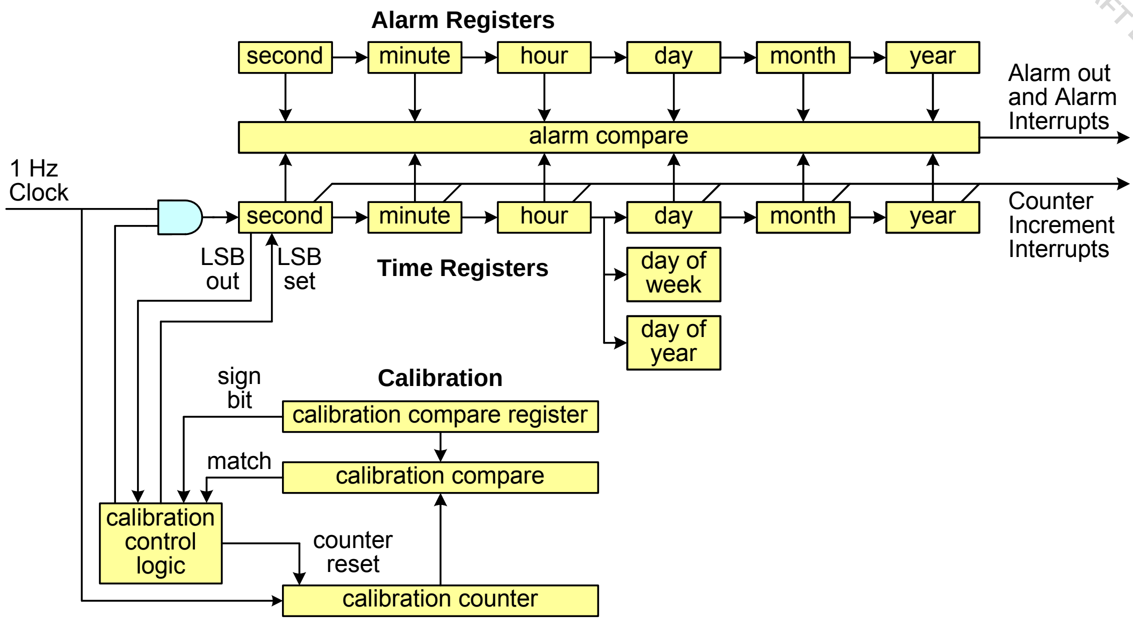


Fig 87. RTC functional block diagram

31.5 Pin description

Table 631. RTC pin description

Pin	Direction	Description
RTC_ALARM	O	RTC controlled output. This is a 1.8 V pin. It goes HIGH when a RTC alarm is generated.

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31.6 Register description

Table 632. Register overview: RTC (base address 0x4004 6000)

Name	Access	Address offset	Description	Reset Value
ILR	W	0x000	Interrupt Location Register	0x0
-	-	0x004	Reserved	0x00
CCR	R/W	0x008	Clock Control Register	0x00
CIIR	R/W	0x00C	Counter Increment Interrupt Register	0x00
AMR	R/W	0x010	Alarm Mask Register	-[1]
CTIME0	R	0x014	Consolidated Time Register 0	-[1]
CTIME1	R	0x018	Consolidated Time Register 1	-[1]
CTIME2	R	0x01C	Consolidated Time Register 2	-[1]
SEC	R/W	0x020	Seconds Register	-[1]
MIN	R/W	0x024	Minutes Register	-[1]
HRS	R/W	0x028	Hours Register	-[1]
DOM	R/W	0x02C	Day of Month Register	-[1]
DOW	R/W	0x030	Day of Week Register	-[1]
DOY	R/W	0x034	Day of Year Register	-[1]
MONTH	R/W	0x038	Months Register	-[1]
YEAR	R/W	0x03C	Years Register	-[1]
CALIBRATION	R/W	0x040	Calibration Value Register	-[1]
-	-	0x044 - 0x05C		-
ASEC	R/W	0x060	Alarm value for Seconds	-[1]
AMIN	R/W	0x064	Alarm value for Minutes	-[1]
AHRS	R/W	0x068	Alarm value for Hours	-[1]
ADOM	R/W	0x6C	Alarm value for Day of Month	-[1]
ADOW	R/W	0x070	Alarm value for Day of Week	-[1]
ADOY	R/W	0x074	Alarm value for Day of Year	-[1]
AMON	R/W	0x078	Alarm value for Months	-[1]
AYRS	R/W	0x07C	Alarm value for Year	-[1]

[1] This register value is not changed by reset.

In addition to the RTC registers, 64 general purpose registers are available to store data when the main power supply is switched off. The general purpose registers reside in the RTC power domain and can be battery powered.

Table 633. Register overview: REGFILE (base address 0x4004 1000)

Name	Access	Address offset	Description	Reset Value
REGFILE0	R/W	0x000	General purpose storage register	0x0
to				
REGFILE63	R/W	0x0FC	General purpose storage register	0x0

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31.6.1 Interrupt Location Register

The Interrupt Location Register is a 2-bit register that specifies which blocks are generating an interrupt (see Table 634). Writing a one to the appropriate bit clears the corresponding interrupt. Writing a zero has no effect. This allows the programmer to read this register and write back the same value to clear only the interrupt that is detected by the read.

Table 634. Interrupt Location Register (ILR - address 0x4004 6000) bit description

Bit	Symbol	Description	Reset value
0	RTCCIF	When one, the Counter Increment Interrupt block generated an interrupt. Writing a one to this bit location clears the counter increment interrupt.	0
1	RTCALF	When one, the alarm registers generated an interrupt. Writing a one to this bit location clears the alarm interrupt.	0
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

31.6.2 Clock Control Register

The clock register is a 4-bit register that controls the operation of the clock divide circuit. Each bit of the clock register is described in Table 635. Bits 0, 1, and 4 in this register should be initialized when the RTC is first turned on.

Table 635. Clock Control Register (CCR - address 0x4004 6008) bit description

Bit	Symbol	Value	Description	Reset value
0	CLKEN		Clock Enable.	-[1]
		0	The time counters are disabled so that they may be initialized.	
		1	The time counters are enabled.	
1	CTCRST		CTC Reset.	0
		0	No effect.	
		1	When one, the elements in the internal oscillator divider are reset, and remain reset until CCR[1] is changed to zero. This is the divider that generates the 1 Hz clock from the 32.768 kHz crystal. The state of the divider is not visible to software.	
3:2	-		Internal test mode controls. These bits must be 0 for normal RTC operation.	-[1]
4	CCALEN		Calibration counter enable.	-[1]
		0	The calibration counter is enabled and counting, using the 1 Hz clock. When the calibration counter is equal to the value of the CALIBRATION register, the counter resets and repeats counting up to the value of the CALIBRATION register. See Section 31.6.6.2 and Section 31.7.1.	
		1	The calibration counter is disabled and reset to zero.	
31:5	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

[1] This register value is not changed by reset.

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31.6.3 Counter Increment Interrupt Register

The Counter Increment Interrupt Register (CIIR) gives the ability to generate an interrupt every time a counter is incremented. This interrupt remains valid until cleared by writing a 1 to bit 0 of the Interrupt Location Register (ILR[0]).

Table 636. Counter Increment Interrupt Register (CIIR - address 0x4004 600C) bit description

Bit	Symbol	Description	Reset value
0	IMSEC	When 1, an increment of the Second value generates an interrupt.	0
1	IMMIN	When 1, an increment of the Minute value generates an interrupt.	0
2	IMHOUR	When 1, an increment of the Hour value generates an interrupt.	0
3	IMDOM	When 1, an increment of the Day of Month value generates an interrupt.	0
4	IMDOW	When 1, an increment of the Day of Week value generates an interrupt.	0
5	IMDOY	When 1, an increment of the Day of Year value generates an interrupt.	0
6	IMMON	When 1, an increment of the Month value generates an interrupt.	0
7	IMYEAR	When 1, an increment of the Year value generates an interrupt.	0
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

31.6.4 Alarm Mask Register

The Alarm Mask Register (AMR) allows the user to mask any of the alarm registers. Table 637 shows the relationship between the bits in the AMR and the alarms. For the alarm function, every non-masked alarm register must match the corresponding time counter for an interrupt to be generated. The interrupt is generated only when the counter comparison first changes from no match to match. The interrupt is removed when a one is written to the appropriate bit of the Interrupt Location Register (ILR). If all mask bits are set, then the alarm is disabled.

Table 637. Alarm Mask Register (AMR - address 0x4004 6010) bit description

Bit	Symbol	Description	Reset value
0	AMRSEC	When 1, the Second value is not compared for the alarm.	0
1	AMRMIN	When 1, the Minutes value is not compared for the alarm.	0
2	AMRHOUR	When 1, the Hour value is not compared for the alarm.	0
3	AMRDOM	When 1, the Day of Month value is not compared for the alarm.	0
4	AMRDOW	When 1, the Day of Week value is not compared for the alarm.	0
5	AMRDOY	When 1, the Day of Year value is not compared for the alarm.	0
6	AMRMON	When 1, the Month value is not compared for the alarm.	0
7	AMRYEAR	When 1, the Year value is not compared for the alarm.	0
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

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31.6.5 Consolidated time registers

The values of the Time Counters can optionally be read in a consolidated format which allows the programmer to read all time counters with only three read operations. The various registers are packed into 32-bit values as shown in Table 638, Table 639, and Table 640. The least significant bit of each register is read back at bit 0, 8, 16, or 24.

The Consolidated Time Registers are read-only. To write new values to the Time Counters, the Time Counter addresses should be used.

31.6.5.1 Consolidated Time Register 0

The Consolidated Time Register 0 contains the low order time values: Seconds, Minutes, Hours, and Day of Week.

Table 638. Consolidated Time register 0 (CTIME0 - address 0x4004 6014) bit description

Bit	Symbol	Description	Reset value
5:0	SECONDS	Seconds value in the range of 0 to 59	-[1]
7:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
13:8	MINUTES	Minutes value in the range of 0 to 59	-[1]
15:14	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
20:16	HOURS	Hours value in the range of 0 to 23	-[1]
23:21	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-[1]
26:24	DOW	Day of week value in the range of 0 to 6	-[1]
31:27	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

31.6.5.2 Consolidated Time Register 1

The Consolidate Time Register 1 contains the Day of Month, Month, and Year values.

Table 639. Consolidated Time register 1 (CTIME1 - address 0x4004 6018) bit description

Bit	Symbol	Description	Reset value
4:0	DOM	Day of month value in the range of 1 to 28, 29, 30, or 31 (depending on the month and whether it is a leap year).	-[1]
7:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
11:8	MONTH	Month value in the range of 1 to 12.	-[1]
15:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
27:16	YEAR	Year value in the range of 0 to 4095.	-[1]
31:28	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

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31.6.5.3 Consolidated Time Register 2

The Consolidate Time Register 2 contains just the Day of Year value.

Table 640. Consolidated Time register 2 (CTIME2 - address 0x4004 601C) bit description

Bit	Symbol	Description	Reset value
11:0	DOY	Day of year value in the range of 1 to 365 (366 for leap years).	-[1]
31:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

31.6.6 Time Counter Group

The time value consists of the eight counters shown in Table 641 and Table 642. These counters can be read or written at the locations shown in Table 642.

Table 641. Time Counter relationships and values

Counter	Size	Enabled by	Minimum value	Maximum value
Second	6	1 Hz Clock	0	59
Minute	6	Second	0	59
Hour	5	Minute	0	23
Day of Month	5	Hour	1	28, 29, 30 or 31
Day of Week	3	Hour	0	6
Day of Year	9	Hour	1	365 or 366 (for leap year)
Month	4	Day of Month	1	12
Year	12	Month or day of Year	0	4095

Table 642. Time Counter registers

Name	Size	Description	Access	Address
SEC	6	Seconds value in the range of 0 to 59	R/W	0x4004 6020
MIN	6	Minutes value in the range of 0 to 59	R/W	0x4004 6024
HRS	5	Hours value in the range of 0 to 23	R/W	0x4004 6028
DOM	5	Day of month value in the range of 1 to 28, 29, 30, or 31 (depending on the month and whether it is a leap year).[1]	R/W	0x4004 602C
DOW	3	Day of week value in the range of 0 to 6[1]	R/W	0x4004 6030
DOY	9	Day of year value in the range of 1 to 365 (366 for leap years)[1]	R/W	0x4004 6034
MONTH	4	Month value in the range of 1 to 12	R/W	0x4004 6038
YEAR	12	Year value in the range of 0 to 4095	R/W	0x4004 603C

[1] These values are simply incremented at the appropriate intervals and reset at the defined overflow point. They are not calculated and must be correctly initialized in order to be meaningful.

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Table 643. Second register (SEC - address 0x4004 6020) bit description

Bit	Symbol	Description	Reset value
5:0	SECONDS	Seconds value in the range of 0 to 59	-[1]
31:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

Table 644. Minute register (MIN - address 0x4004 6024) bit description

Bit	Symbol	Description	Reset value
5:0	MINUTES	Minutes value in the range of 0 to 59	-[1]
31:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

Table 645. Hour register (HRS - address 0x4004 6028) bit description

Bit	Symbol	Description	Reset value
4:0	HOURS	Hours value in the range of 0 to 23	-[1]
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

Table 646. Days of month register (DOM - address 0x4004 602C) bit description

Bit	Symbol	Description	Reset value
4:0	DOM	Day of month value in the range of 1 to 28, 29, 30, or 31 (depending on the month and whether it is a leap year).	-[1]
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

Table 647. Days of week register (DOW - address 0x4004 6030) bit description

Bit	Symbol	Description	Reset value
2:0	DOW	Day of week value in the range of 0 to 6.	-[1]
31:3	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

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Table 648. Days of year register (DOY - address 0x4004 6034) bit description

Bit	Symbol	Description	Reset value
8:0	DOY	Day of year value in the range of 1 to 365 (366 for leap years).	-[1]
31:9	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

Table 649. Month register (MONTH - address 0x4004 6038) bit description

Bit	Symbol	Description	Reset value
3:0	MONTH	Month value in the range of 1 to 12.	-[1]
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

Table 650. Year register (YEAR - address 0x4004 603C) bit description

Bit	Symbol	Description	Reset value
11:0	YEAR	Year value in the range of 0 to 4095.	-[1]
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

31.6.6.1 Leap year calculation

The RTC does a simple bit comparison to see if the two lowest order bits of the year counter are zero. If true, then the RTC considers that year a leap year. The RTC considers all years evenly divisible by 4 as leap years. This algorithm is accurate from the year 1901 through the year 2099, but fails for the year 2100, which is not a leap year. The only effect of leap year on the RTC is to alter the length of the month of February for the month, day of month, and year counters.

31.6.6.2 Calibration register

The following register is used to calibrate the time counter. The bits in this register are not changed by reset.

Table 651. Calibration register (CALIBRATION - address 0x4004 6040) bit description

Bit	Symbol	Value	Description	Reset value
16:0	CALVAL	-	If enabled, the calibration counter counts up to this value. The maximum value is 131072 corresponding to about 36.4 hours. Calibration is disabled if CALVAL = 0.	-[1]

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Table 651. Calibration register (CALIBRATION - address 0x4004 6040) bit description

Bit	Symbol	Value	Description	Reset value
17	CALDIR		Calibration direction	-[1]
		0	Forward calibration. When CALVAL is equal to the calibration counter, the RTC timers will jump by 2 seconds.	
		1	Backward calibration. When CALVAL is equal to the calibration counter, the RTC timers will stop incrementing for 1 second.	
31:12			Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

31.6.7 Alarm register group

The alarm registers are shown in Table 652. The values in these registers are compared with the time counters. If all the unmasked (See Section 31.6.4 "Alarm Mask Register" on page 703) alarm registers match their corresponding time counters then an interrupt is generated. The interrupt is cleared when a 1 is written to bit 1 of the Interrupt Location Register (ILR[1]).

Table 652. Alarm registers

Name	Size	Description	Access	Address
ALSEC	6	Alarm value for Seconds	R/W	0x4004 6060
ALMIN	6	Alarm value for Minutes	R/W	0x4004 6064
ALHRS	5	Alarm value for Hours	R/W	0x4004 6068
ALDOM	5	Alarm value for Day of Month	R/W	0x4004 606C
ALDOW	3	Alarm value for Day of Week	R/W	0x4004 6070
ALDOY	9	Alarm value for Day of Year	R/W	0x4004 6074
ALMON	4	Alarm value for Months	R/W	0x4004 6078
ALYEAR	12	Alarm value for Years	R/W	0x4004 607C

Table 653. Alarm Second register (ASEC - address 0x4004 6060) bit description

Bit	Symbol	Description	Reset value
5:0	SECONDS	Seconds value in the range of 0 to 59	-[1]
31:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

Table 654. Alarm Minute register (AMIN - address 0x4004 6064) bit description

Bit	Symbol	Description	Reset value
5:0	MINUTES	Minutes value in the range of 0 to 59	-[1]
31:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

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Table 655. Alarm Hour register (AHRS - address 0x4004 6068) bit description

Bit	Symbol	Description	Reset value
4:0	HOURS	Hours value in the range of 0 to 23	-[1]
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

Table 656. Alarm Days of month register (ADOM - address 0x4004 606C) bit description

Bit	Symbol	Description	Reset value
4:0	DOM	Day of month value in the range of 1 to 28, 29, 30, or 31 (depending on the month and whether it is a leap year).	-[1]
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

Table 657. Alarm Days of week register (ADOW - address 0x4004 6070) bit description

Bit	Symbol	Description	Reset value
2:0	DOW	Day of week value in the range of 0 to 6.	-[1]
31:3	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

Table 658. Alarm Days of year register (ADOY - address 0x4004 6074) bit description

Bit	Symbol	Description	Reset value
8:0	DOY	Day of year value in the range of 1 to 365 (366 for leap years).	-[1]
31:9	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

Table 659. Alarm Month register (AMON - address 0x4004 6078) bit description

Bit	Symbol	Description	Reset value
3:0	MONTH	Month value in the range of 1 to 12.	-[1]
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

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Table 660. Alarm Year register (AYRS - address 0x4004 607C) bit description

Bit	Symbol	Description	Reset value
11:0	YEAR	Year value in the range of 0 to 4095.	-[1]
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

[1] This register value is not changed by reset.

31.7 Functional description

31.7.1 Calibration procedure

The calibration logic can periodically adjust the time counter either by not incrementing the counter, or by incrementing the counter by 2 instead of 1. This allows calibrating the RTC oscillator under some typical voltage and temperature conditions without the need to externally trim the RTC oscillator.

A recommended method for determining the calibration value is to use the CLKOUT feature to unintrusively observe the RTC oscillator frequency under the conditions it is to be trimmed for, and calculating the number of clocks that will be seen before the time is off by one second. That value is used to determine CALVAL.

The exact method of calibration depends on whether CALVAL is even or odd. For even values, the hardware performs a two calibrations sequentially multiple times (one calibration at CALVAL+1 and one calibration at CALVAL - 1) and averages both calibration values. For odd values of CALVAL, the calibration time is accurate.

If the RTC oscillator is trimmed externally, the same method of unintrusively observing the RTC oscillator frequency may be helpful in that process.

Backward calibration

Enable the RTC timer and calibration in the CCR register (set bits CLKEN = 1 and CCALEN = 0). In the CALIBRATION register, set the calibration value CALVAL ≥ 1 and select CALDIR = 1.

- The SEC timer and the calibration counter count up for every 1 Hz clock cycle.
- When the calibration counter reaches CALVAL, a calibration match occurs and all RTC timers will be stopped for one clock cycle so that the timers will not increment in the next cycle.
- If an alarm match event occurs in the same cycle as the calibration match, the alarm interrupt will be delayed by one cycle to avoid a double alarm interrupt.

Forward calibration

Enable the RTC timer and calibration in the CCR register (set bits CLKEN = 1 and CCALEN = 0). In the CALIBRATION register, set the calibration value CALVAL ≥ 1 and select CALDIR = 0.

- The SEC timer and the calibration counter count up for every 1 Hz clock cycle.
- When the calibration counter reaches CALVAL, a calibration match occurs and the RTC timers are incremented by 2.

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- When the calibration event occurs, the LSB of the ALSEC register is forced to be one so that the alarm interrupt will not be missed when skipping a second.

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32.1 How to read this chapter

The USART0/2/3 controllers are available on all LPC18xx parts.

32.2 Basic configuration

The USART0/2/3 are configured as follows:

- See Table 661 for clocking and power control.
- The USART0/2/3 are reset by the UART0/2/3_RST (reset #44/46/47).
- The USART0/2/3 interrupts are connected to slots # 24/26/27 in the NVIC.
- For connecting the USART0/2/3 receive and transmit lines to the GPDMA, use the DMAMUX register in the CREG block (see Table 35) and enable the GPDMA channel in the DMA Channel Configuration registers (Section 16.6.20).

Table 661. USART0/2/3 clocking and power control

	Base clock	Branch clock	Maximum frequency
USART0 clock to register interface	BASE_M3_CLK	CLK_M3_UART0	150 MHz
USART0 peripheral clock (PCLK)	BASE_UART0_CLK	CLK_APB0_UART0	150 MHz
USART2 clock to register interface	BASE_M3_CLK	CLK_M3_UART2	150 MHz
USART2 peripheral clock (PCLK)	BASE_UART2_CLK	CLK_APB2_UART2	150 MHz
USART3 clock to register interface	BASE_M3_CLK	CLK_M3_UART3	150 MHz
USART3 peripheral clock (PCLK)	BASE_UART3_CLK	CLK_APB2_UART3	150 MHz

32.3 Features

- 16-byte receive and transmit FIFOs.
- Register locations conform to ‘550 industry standard.
- Receiver FIFO trigger points at 1, 4, 8, and 14 bytes.
- Built-in baud rate generator.
- UART allows for implementation of either software or hardware flow control.
- RS-485/EIA-485 9-bit mode support with output enable.
- Support for synchronous mode UART (USART).
- IrDA interface (USART3 only).
- DMA support.
- Smart Card interface.

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32.4 Pin description

Table 662. USART0/2/3 pin description

Function name	Direction	Description
USART0		
U0_RXD	I	**Serial Input.** Serial receive data.
U0_TXD	O	**Serial Output.** Serial transmit data.
U0_DIR	I/O	RS-485/EIA-485 output enable/direction control.
U0_UCLK	I/O	Serial clock input/output for USART0 in synchronous mode.
USART2		
U2_RXD	I	**Serial Input.** Serial receive data.
U2_TXD	O	**Serial Output.** Serial transmit data.
U2_DIR	I/O	RS-485/EIA-485 output enable/direction control.
U2_UCLK	I/O	Serial clock input/output for USART2 in synchronous mode.
USART3		
U3_RXD	I	**Serial Input.** Serial receive data.
U3_TXD	O	**Serial Output.** Serial transmit data.
U3_DIR	I/O	RS-485/EIA-485 output enable/direction control.
U3_UCLK	I/O	Serial clock input/output for USART3 in synchronous mode.
U3_BAUD		<tbd>

32.5 Register description

The UART contains registers organized as shown in Table 663. The Divisor Latch Access Bit (DLAB) is contained in LCR[7] and enables access to the Divisor Latches.

Reset value reflects the data stored in used bits only. It does not include the content of reserved bits.

Table 663. Register overview: UART0/2/3 (base address: 0x4008 1000, 0x400C 1000, 0x400C 2000)

Name	Access	Address offset	Description	Reset value
RBR	RO	0x000	Receiver Buffer Register. Contains the next received character to be read (DLAB = 0).	NA
THR	WO	0x000	Transmit Holding Register. The next character to be transmitted is written here (DLAB = 0).	NA
DLL	R/W	0x000	Divisor Latch LSB. Least significant byte of the baud rate divisor value. The full divisor is used to generate a baud rate from the fractional rate divider (DLAB = 1).	0x01
DLM	R/W	0x004	Divisor Latch MSB. Most significant byte of the baud rate divisor value. The full divisor is used to generate a baud rate from the fractional rate divider (DLAB = 1).	0x00
IER	R/W	0x004	Interrupt Enable Register. Contains individual interrupt enable bits for the 7 potential UART interrupts (DLAB = 0).	0x00

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Table 663. Register overview: UART0/2/3 (base address: 0x4008 1000, 0x400C 1000, 0x400C 2000)

Name	Access	Address offset	Description	Reset value
IIR	RO	0x008	Interrupt ID Register. Identifies which interrupt(s) are pending.	0x01
FCR	WO	0x008	FIFO Control Register. Controls UART FIFO usage and modes.	0x00
LCR	R/W	0x00C	Line Control Register. Contains controls for frame formatting and break generation.	0x00
-	-	0x010	Reserved	-
LSR	RO	0x014	Line Status Register. Contains flags for transmit and receive status, including line errors.	0x60
-	-	0x018	Reserved	-
SCR	R/W	0x01C	Scratch Pad Register. Eight-bit temporary storage for software.	0x00
ACR	R/W	0x020	Auto-baud Control Register. Contains controls for the auto-baud feature.	0x00
ICR	R/W	0x024	IrDA control register (UART3 only)	0x00
FDR	R/W	0x028	Fractional Divider Register. Generates a clock input for the baud rate divider.	0x10
-	-	0x02C - 0x03C	Reserved	-
HDEN	R/W	0x040	Half-duplex enable Register	
-	-	0x044	Reserved	-
SCICTRL	R/W	0x048	Smart card interface control register	
RS485CTRL	R/W	0x04C	RS-485/EIA-485 Control. Contains controls to configure various aspects of RS-485/EIA-485 modes.	0x00
RS485ADRMATCH	R/W	0x050	RS-485/EIA-485 address match. Contains the address match value for RS-485/EIA-485 mode.	0x00
RS485DLY	R/W	0x054	RS-485/EIA-485 direction control delay.	0x00
SYNCCTRL	R/W	0x058	Synchronous mode control register.	0x00
TER	R/W	0x05C	Transmit Enable Register. Turns off UART transmitter for use with software flow control.	0x01

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32.5.1 UART Receiver Buffer Register

The RBR is the top byte of the UART RX FIFO. The top byte of the RX FIFO contains the oldest character received and can be read via the bus interface. The LSB (bit 0) represents the “oldest” received data bit. If the character received is less than 8 bits, the unused MSBs are padded with zeroes.

The Divisor Latch Access Bit (DLAB) in LCR must be zero in order to access the RBR. The RBR is always Read Only.

Since PE, FE and BI bits (see Table 673) correspond to the byte sitting on the top of the RBR FIFO (i.e. the one that will be read in the next read from the RBR), the right approach for fetching the valid pair of received byte and its status bits is first to read the content of the LSR register, and then to read a byte from the RBR.

Table 664. UART Receiver Buffer Registers when DLAB = 0, Read Only (RBR - addresses 0x4008 1000 (UART0), 0x400C 1000 (UART2), 0x400C 2000 (UART3)) bit description

Bit	Symbol	Description	Reset value
7:0	RBR	Receiver buffer. The UART Receiver Buffer Register contains the oldest received byte in the UART RX FIFO.	undefined
31:8	-	Reserved	-

32.5.2 UART Transmitter Holding Register

The THR is the top byte of the UART TX FIFO. The top byte is the newest character in the TX FIFO and can be written via the bus interface. The LSB represents the first bit to transmit.

The Divisor Latch Access Bit (DLAB) in LCR must be zero in order to access the THR. The THR is always Write Only.

Table 665. UART Transmitter Holding Register when DLAB = 0, Write Only(THR - addresses 0x4008 1000 (UART0), 0x400C 1000 (UART2), 0x400C 2000 (UART3)) bit description

Bit	Symbol	Description	Reset value
7:0	THR	Transmit Holding Register. Writing to the UART Transmit Holding Register causes the data to be stored in the UART transmit FIFO. The byte will be sent when it reaches the bottom of the FIFO and the transmitter is available.	NA
31:8	-	Reserved	-

32.5.3 UART Divisor Latch LSB and MSB Registers

The UART Divisor Latch is part of the UART Baud Rate Generator and holds the value used, along with the Fractional Divider, to divide the UART_PCLK clock in order to produce the baud rate clock, which must be 16x the desired baud rate. The DLL and DLM registers together form a 16-bit divisor where DLL contains the lower 8 bits of the divisor and DLM contains the higher 8 bits of the divisor. A 0x0000 value is treated like a 0x0001 value as division by zero is not allowed.The Divisor Latch Access Bit (DLAB) in LCR must be one in order to access the UART Divisor Latches. Details on how to select the right value for DLL and DLM can be found in Section 32.5.12.

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Table 666. UART Divisor Latch LSB Register when DLAB = 1 (DLL - addresses 0x4008 1000 (UART0), 0x400C 1000 (UART2), 0x400C 2000 (UART3)) bit description

Bit	Symbol	Description	Reset value
7:0	DLLSB	Divisor latch LSB. The UART Divisor Latch LSB Register, along with the DLM register, determines the baud rate of the UART.	0x01
31:8	-	Reserved	-

Table 667. UART Divisor Latch MSB Register when DLAB = 1 (DLM - addresses 0x4008 1004 (UART0), 0x400C 1004 (UART2), 0x400C 2004 (UART3)) bit description

Bit	Symbol	Description	Reset value
7:0	DLMSB	Divisor latch MSB. The UART Divisor Latch MSB Register, along with the DLL register, determines the baud rate of the UART.	0x00
31:8	-	Reserved	-

32.5.4 UART Interrupt Enable Register

The IER is used to enable the four UART interrupt sources.

Table 668. UART Interrupt Enable Register when DLAB = 0 (IER - addresses 0x4008 1004 (UART0), 0x400C 1004 (UART2), 0x400C 2004 (UART3)) bit description

Bit	Symbol	Value	Description	Reset value
0	RBRIE		RBR Interrupt Enable. Enables the Receive Data Available interrupt for UART. It also controls the Character Receive Time-out interrupt.	0
		0	Disable the RDA interrupt.	
		1	Enable the RDA interrupt.	
1	THREIE		THRE Interrupt Enable. Enables the THRE interrupt for UART. The status of this interrupt can be read from LSR[5].	0
		0	Disable the THRE interrupt.	
		1	Enable the THRE interrupt.	
2	RXIE		RX Line Interrupt Enable. Enables the UART RX line status interrupts. The status of this interrupt can be read from LSR[4:1].	0
		0	Disable the RX line status interrupts.	
		1	Enable the RX line status interrupts.	
3	-	-	Reserved	-
6:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
7	-	-	Reserved	0
8	ABEOINTEN		Enables the end of auto-baud interrupt.	0
		0	Disable end of auto-baud Interrupt.	
		1	Enable end of auto-baud Interrupt.	

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Table 668. UART Interrupt Enable Register when DLAB = 0 (IER - addresses 0x4008 1004 (UART0), 0x400C 1004 (UART2), 0x400C 2004 (UART3)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value
9	ABTOINTEN		Enables the auto-baud time-out interrupt.	0
		0	Disable auto-baud time-out Interrupt.	
		1	Enable auto-baud time-out Interrupt.	
31:10	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

32.5.5 UART Interrupt Identification Register

IIR provides a status code that denotes the priority and source of a pending interrupt. The interrupts are frozen during a IIR access. If an interrupt occurs during a IIR access, the interrupt is recorded for the next IIR access.

Table 669. UART Interrupt Identification Register, read only (IIR - addresses 0x4008 1008 (UART0), 0x400C 1008 (UART2), 0x400C 2008 (UART3)) bit description

Bit	Symbol	Value	Description	Reset value
0	INTSTATUS		Interrupt status. Note that IIR[0] is active low. The pending interrupt can be determined by evaluating IIR[3:1].	1
		0	At least one interrupt is pending.	
		1	No interrupt is pending.	
3:1	INTID		Interrupt identification. IER[3:1] identifies an interrupt corresponding to the UART Rx FIFO. All other combinations of IER[3:1] not listed below are reserved (100,101,111).	0
		0x3	Priority 1 (highest) - Receive Line Status (RLS).	
		0x2	Priority 2 - Receive Data Available (RDA).	
		0x6	Priority 2 - Character Time-out Indicator (CTI).	
		0x1	Priority 3 - THRE Interrupt.	
		0x0	Priority 4 (lowest) - Reserved.	
5:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
7:6	FIFOENABLE		Copies of FCR[0].	0
8	ABEOINT		End of auto-baud interrupt. True if auto-baud has finished successfully and interrupt is enabled.	0
9	ABTOINT		Auto-baud time-out interrupt. True if auto-baud has timed out and interrupt is enabled.	0
31:10	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Bits IIR[9:8] are set by the auto-baud function and signal a time-out or end of auto-baud condition. The auto-baud interrupt conditions are cleared by setting the corresponding Clear bits in the Auto-baud Control Register.

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If the IntStatus bit is one and no interrupt is pending and the IntId bits will be zero. If the IntStatus is 0, a non auto-baud interrupt is pending in which case the IntId bits identify the type of interrupt and handling as described in Table 670. Given the status of IIR[3:0], an interrupt handler routine can determine the cause of the interrupt and how to clear the active interrupt. The IIR must be read in order to clear the interrupt prior to exiting the Interrupt Service Routine.

The UART RLS interrupt (IIR[3:1] = 011) is the highest priority interrupt and is set whenever any one of four error conditions occur on the UART RX input: overrun error (OE), parity error (PE), framing error (FE) and break interrupt (BI). The UART Rx error condition that set the interrupt can be observed via LSR[4:1]. The interrupt is cleared upon a LSR read.

The UART RDA interrupt (IIR[3:1] = 010) shares the second level priority with the CTI interrupt (IIR[3:1] = 110). The RDA is activated when the UART Rx FIFO reaches the trigger level defined in FCR7:6 and is reset when the UART Rx FIFO depth falls below the trigger level. When the RDA interrupt goes active, the CPU can read a block of data defined by the trigger level.

The CTI interrupt (IIR[3:1] = 110) is a second level interrupt and is set when the UART Rx FIFO contains at least one character and no UART Rx FIFO activity has occurred in 3.5 to 4.5 character times. Any UART Rx FIFO activity (read or write of UART RSR) will clear the interrupt. This interrupt is intended to flush the UART RBR after a message has been received that is not a multiple of the trigger level size. For example, if a peripheral wished to send a 105 character message and the trigger level was 10 characters, the CPU would receive 10 RDA interrupts resulting in the transfer of 100 characters and 1 to 5 CTI interrupts (depending on the service routine) resulting in the transfer of the remaining 5 characters.

Table 670. UART Interrupt Handling

IIR[3:0] value[1]	Priority	Interrupt type	Interrupt source	Interrupt reset
0001	-	None	None	-
0110	Highest	RX Line Status / Error	OE[2] or PE[2] or FE[2] or BI[2]	LSR Read[2]
0100	Second	RX Data Available	Rx data available or trigger level reached in FIFO (FCR0=1)	RBR Read[3] or UART FIFO drops below trigger level
1100	Second	Character Time-out indication	Minimum of one character in the RX FIFO and no character input or removed during a time period depending on how many characters are in FIFO and what the trigger level is set at (3.5 to 4.5 character times). The exact time will be: [(word length) $\times$ 7 - 2] $\times$ 8 + [(trigger level - number of characters) $\times$ 8 + 1] RCLKs	RBR Read[3]
0010	Third	THRE	THRE[2]	IIR Read[4] (if source of interrupt) or THR write

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[1] Values 0000, 0011, 010, 0111, 1000, 1001, 1010, 1011,1101, 1110,1111 are reserved.

[2] For details see Section 32.5.8 “UART Line Status Register”

[3] For details see Section 32.5.1 “UART Receiver Buffer Register”

[4] For details see Section 32.5.5 “UART Interrupt Identification Register” and Section 32.5.2 “UART Transmitter Holding Register”

The UART THRE interrupt (IIR[3:1] = 001) is a third level interrupt and is activated when the UART THR FIFO is empty provided certain initialization conditions have been met. These initialization conditions are intended to give the UART THR FIFO a chance to fill up with data to eliminate many THRE interrupts from occurring at system start-up. The initialization conditions implement a one character delay minus the stop bit whenever THRE = 1 and there have not been at least two characters in the THR at one time since the last THRE = 1 event. This delay is provided to give the CPU time to write data to THR without a THRE interrupt to decode and service. A THRE interrupt is set immediately if the UART THR FIFO has held two or more characters at one time and currently, the THR is empty. The THRE interrupt is reset when a THR write occurs or a read of the IIR occurs and the THRE is the highest interrupt (IIR[3:1] = 001).

32.5.6 UART FIFO Control Register

The FCR controls the operation of the UART RX and TX FIFOs.

Table 671. UART FIFO Control Register Write Only (FCR - addresses 0x4008 1008 (UART0), 0x400C 1008 (UART2), 0x400C 2008 (UART3)) bit description

Bit	Symbol	Value	Description	Reset value
0	FIFOEN		FIFO Enable.	0
		0	UART FIFOs are disabled. Must not be used in the application.	
		1	Active high enable for both UART Rx and TX FIFOs and FCR[7:1] access. This bit must be set for proper UART operation. Any transition on this bit will automatically clear the UART FIFOs.	
1	RXFIFO RES		RX FIFO Reset.	0
		0	No impact on either of UART FIFOs.	
		1	Writing a logic 1 to FCR[1] will clear all bytes in UART Rx FIFO, reset the pointer logic. This bit is self-clearing.	
2	TXFIFO RES		TX FIFO Reset.	0
		0	No impact on either of UART FIFOs.	
		1	Writing a logic 1 to FCR[2] will clear all bytes in UART TX FIFO, reset the pointer logic. This bit is self-clearing.	
3	DMAMO DE		DMA Mode Select. When the FIFO enable bit (bit 0 of this register) is set, this bit selects the DMA mode.	0
5:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

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Table 671. UART FIFO Control Register Write Only (FCR - addresses 0x4008 1008 (UART0), 0x400C 1008 (UART2), 0x400C 2008 (UART3)) bit description

Bit	Symbol	Value	Description	Reset value
7:6	RXTRIG LVL		RX Trigger Level. These two bits determine how many receiver UART FIFO characters must be written before an interrupt is activated.	0
		0x0	Trigger level 0 (1 character or 0x01).	
		0x1	Trigger level 1 (4 characters or 0x04).	
		0x2	Trigger level 2 (8 characters or 0x08).	
		0x3	Trigger level 3 (14 characters or 0x0E).	
31:8	-	-	Reserved	-

32.5.6.1 DMA Operation

The user can optionally operate the UART transmit and/or receive using DMA. The DMA mode is determined by the DMA Mode Select bit in the FCR register. Note that for DMA operation as for any operation of the UART, the FIFOs must be enabled via the FIFO Enable bit in the FCR register.

UART receiver DMA

In DMA mode, the receiver DMA request is asserted when the receiver FIFO level becomes equal to or greater than trigger level, or if a character time-out occurs. See the description of the RX Trigger Level above. The receiver DMA request is cleared by the DMA controller.

UART transmitter DMA

In DMA mode, the transmitter DMA request is asserted when the transmitter FIFO transitions to not full. The transmitter DMA request is cleared by the DMA controller.

32.5.7 UART Line Control Register

The LCR determines the format of the data character that is to be transmitted or received.

Table 672. UART Line Control Register (LCR - addresses 0x4008 100C (UART0), 0x400C 100C (UART2), 0x400C 200C (UART3)) bit description

Bit	Symbol	Value	Description	Reset Value
1:0	WLS		Word Length Select.	0
		0x0	5-bit character length.	
		0x1	6-bit character length.	
		0x2	7-bit character length.	
		0x3	8-bit character length.	
2	SBS		Stop Bit Select.	0
		0	1 stop bit.	
		1	2 stop bits (1.5 if LCR[1:0]=00).	

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Table 672. UART Line Control Register (LCR - addresses 0x4008 100C (UART0), 0x400C 100C (UART2), 0x400C 200C (UART3)) bit description *…continued*

Bit	Symbol	Value	Description	Reset Value
3	PE		Parity Enable	0
		0	Disable parity generation and checking.	
		1	Enable parity generation and checking.	
5:4	PS		Parity Select.	0
		0x0	Odd parity. Number of 1s in the transmitted character and the attached parity bit will be odd.	
		0x1	Even Parity. Number of 1s in the transmitted character and the attached parity bit will be even.	
		0x2	Forced "1" stick parity.	
		0x3	Forced "0" stick parity.	
6	BC		Break Control.	0
		0	Disable break transmission.	
		1	Enable break transmission. Output pin UART TXD is forced to logic 0 when LCR[6] is active high.	
7	DLAB		Divisor Latch Access Bit.	0
		0	Disable access to Divisor Latches.	
		1	Enable access to Divisor Latches.	
31:8	-	-	Reserved	-

32.5.8 UART Line Status Register

The LSR is a Read Only register that provides status information on the UART TX and RX blocks.

Table 673. UART Line Status Register Read Only (LSR - addresses 0x4008 1014 (UART0), 0x400C 1014 (UART2), 0x400C 2014 (UART3)) bit description

Bit	Symbol	Value	Description	Reset Value
0	RDR		Receiver Data Ready. LSR[0] is set when the RBR holds an unread character and is cleared when the UART RBR FIFO is empty.	0
		0	RBR is empty.	
		1	RBR contains valid data.	
1	OE		Overrun Error. The overrun error condition is set as soon as it occurs. A LSR read clears LSR[1]. LSR[1] is set when UART RSR has a new character assembled and the UART RBR FIFO is full. In this case, the UART RBR FIFO will not be overwritten and the character in the UART RSR will be lost.	0
		0	Overrun error status is inactive.	
		1	Overrun error status is active.	

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Table 673. UART Line Status Register Read Only (LSR - addresses 0x4008 1014 (UART0), 0x400C 1014 (UART2), 0x400C 2014 (UART3)) bit description *…continued*

Bit	Symbol	Value	Description	Reset Value
2	PE		Parity Error. When the parity bit of a received character is in the wrong state, a parity error occurs. A LSR read clears LSR[2]. Time of parity error detection is dependent on FCR[0]. **Note:** A parity error is associated with the character at the top of the UART RBR FIFO.	0
		0	Parity error status is inactive.	
		1	Parity error status is active.	
3	FE		Framing Error. When the stop bit of a received character is a logic 0, a framing error occurs. A LSR read clears LSR[3]. The time of the framing error detection is dependent on FCR0. Upon detection of a framing error, the RX will attempt to re-synchronize to the data and assume that the bad stop bit is actually an early start bit. However, it cannot be assumed that the next received byte will be correct even if there is no Framing Error. **Note:** A framing error is associated with the character at the top of the UART RBR FIFO.	0
		0	Framing error status is inactive.	
		1	Framing error status is active.	
4	BI		Break Interrupt. When RXD1 is held in the spacing state (all zeros) for one full character transmission (start, data, parity, stop), a break interrupt occurs. Once the break condition has been detected, the receiver goes idle until RXD1 goes to marking state (all ones). A LSR read clears this status bit. The time of break detection is dependent on FCR[0]. **Note:** The break interrupt is associated with the character at the top of the UART RBR FIFO.	0
		0	Break interrupt status is inactive.	
		1	Break interrupt status is active.	
5	THRE		Transmitter Holding Register Empty. THRE is set immediately upon detection of an empty UART THR and is cleared on a THR write.	1
		0	THR contains valid data.	
		1	THR is empty.	
6	TEMT		Transmitter Empty. TEMT is set when both THR and TSR are empty; TEMT is cleared when either the TSR or the THR contain valid data.	1
		0	THR and/or the TSR contains valid data.	
		1	THR and the TSR are empty.	

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Table 673. UART Line Status Register Read Only (LSR - addresses 0x4008 1014 (UART0), 0x400C 1014 (UART2), 0x400C 2014 (UART3)) bit description *…continued*

Bit	Symbol	Value	Description	Reset Value
7	RXFE		Error in RX FIFO. LSR[7] is set when a character with a RX error such as framing error, parity error or break interrupt, is loaded into the RBR. This bit is cleared when the LSR register is read and there are no subsequent errors in the UART FIFO.	0
		0	RBR contains no UART RX errors or FCR[0]=0.	
		1	UART RBR contains at least one UART RX error.	
8	TXERR		Error in transmitted character. A NACK response is given by the receiver in Smart card T=0 mode. This bit is cleared when the LSR register is read.	0
		0	No error (normal default condition).	
		1	A NACK response is received during Smart card T=0 operation.	
31:9	-	-	Reserved	-

32.5.9 UART Scratch Pad Register

The SCR has no effect on the UART operation. This register can be written and/or read at user’s discretion. There is no provision in the interrupt interface that would indicate to the host that a read or write of the SCR has occurred.

Table 674. UART Scratch Pad Register (SCR - addresses 0x4008 101C (UART0), 0x400C 101C (UART2), 0x400C 201C (UART3)) bit description

Bit	Symbol	Description	Reset Value
7:0	PAD	Scratch pad. A readable, writable byte.	0x00
31:8	-	Reserved	-

32.5.10 UART Auto-baud Control Register

The UART Auto-baud Control Register (ACR) controls the process of measuring the incoming clock/data rate for the baud rate generation and can be read and written at user’s discretion.

Table 675. Autobaud Control Register (ACR - addresses 0x4008 1020 (UART0), 0x400C 1020 (UART2), 0x400C 2020 (UART3)) bit description

Bit	Symbol	Value	Description	Reset value
0	START		Start bit. This bit is automatically cleared after auto-baud completion.	0
		0	Auto-baud stop (auto-baud is not running).	
		1	Auto-baud start (auto-baud is running). Auto-baud run bit. This bit is automatically cleared after auto-baud completion.	
1	MODE		Auto-baud mode select bit.	0
		0	Mode 0.	
		1	Mode 1.	

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Table 675. Autobaud Control Register (ACR - addresses 0x4008 1020 (UART0), 0x400C 1020 (UART2), 0x400C 2020 (UART3)) bit description

Bit	Symbol	Value	Description	Reset value
2	AUTORESTART		Restart bit.	0
		0	No restart	
		1	Restart in case of time-out (counter restarts at next UART Rx falling edge)	
7:3	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0
8	ABEOINTCLR		End of auto-baud interrupt clear bit (write-only).	0
		0	Writing a 0 has no impact.	
		1	Writing a 1 will clear the corresponding interrupt in the IIR.	
9	ABTOINTCLR		Auto-baud time-out interrupt clear bit (write-only).	0
		0	Writing a 0 has no impact.	
		1	Writing a 1 will clear the corresponding interrupt in the IIR.	
31:10	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0

32.5.10.1 Auto-baud

The UART auto-baud function can be used to measure the incoming baud rate based on the ”AT" protocol (Hayes command). If enabled the auto-baud feature will measure the bit time of the receive data stream and set the divisor latch registers DLM and DLL accordingly.

Auto-baud is started by setting the ACR Start bit. Auto-baud can be stopped by clearing the ACR Start bit. The Start bit will clear once auto-baud has finished and reading the bit will return the status of auto-baud (pending/finished).

Two auto-baud measuring modes are available which can be selected by the ACR Mode bit. In Mode 0 the baud rate is measured on two subsequent falling edges of the UART Rx pin (the falling edge of the start bit and the falling edge of the least significant bit). In Mode 1 the baud rate is measured between the falling edge and the subsequent rising edge of the UART Rx pin (the length of the start bit).

The ACR AutoRestart bit can be used to automatically restart baud rate measurement if a time-out occurs (the rate measurement counter overflows). If this bit is set, the rate measurement will restart at the next falling edge of the UART Rx pin.

The auto-baud function can generate two interrupts.

- The IIR ABTOInt interrupt will get set if the interrupt is enabled (IER ABToIntEn is set and the auto-baud rate measurement counter overflows).
- The IIR ABEOInt interrupt will get set if the interrupt is enabled (IER ABEOIntEn is set and the auto-baud has completed successfully).

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The auto-baud interrupts have to be cleared by setting the corresponding ACR ABTOIntClr and ABEOIntEn bits.

The fractional baud rate generator must be disabled (DIVADDVAL = 0) during auto-baud. Also, when auto-baud is used, any write to DLM and DLL registers should be done before ACR register write. The minimum and the maximum baud rates supported by UART are function of UART_PCLK, number of data bits, stop bits and parity bits.

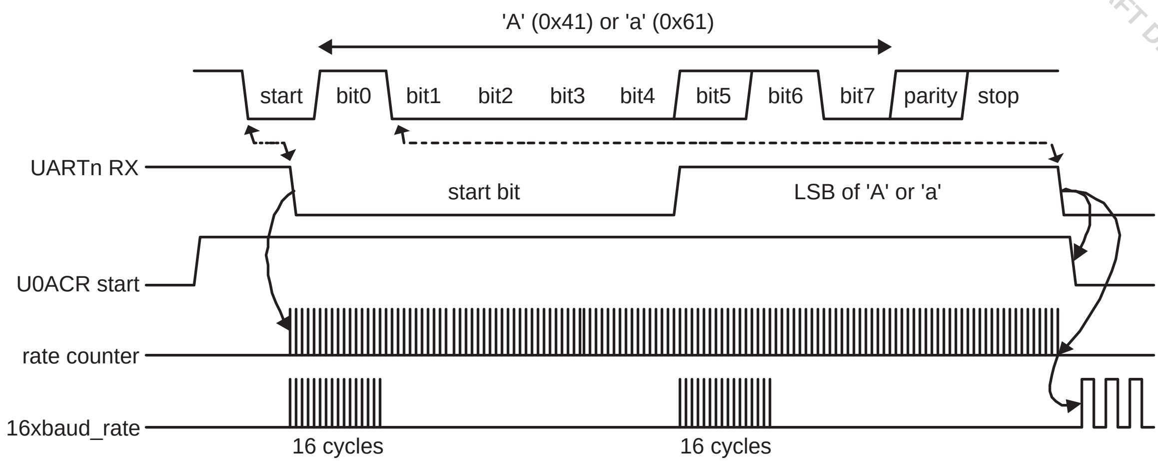
$$ratemin = \frac{2 \times PCLK}{16 \times 2^{15}} \le UART_{baudrate} \le \frac{PCLK}{16 \times (2 + databits + paritybits + stopbits)} = ratemax \quad (6)$$

32.5.10.2 Auto-baud modes

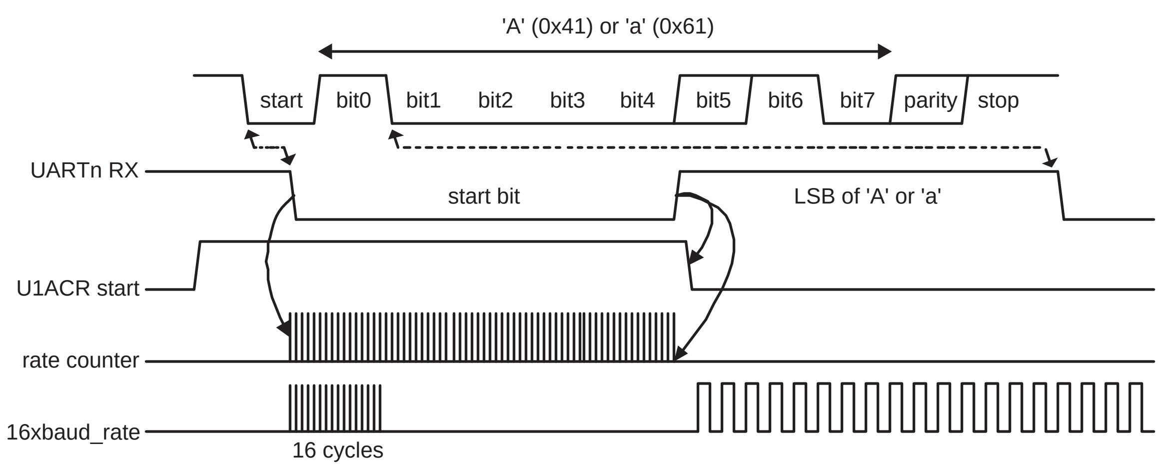
When the software is expecting an ”AT" command, it configures the UART with the expected character format and sets the ACR Start bit. The initial values in the divisor latches DLM and DLM don‘t care. Because of the ”A" or ”a" ASCII coding (”A" = 0x41, ”a" = 0x61), the UART Rx pin sensed start bit and the LSB of the expected character are delimited by two falling edges. When the ACR Start bit is set, the auto-baud protocol will execute the following phases:

1. On ACR Start bit setting, the baud rate measurement counter is reset and the UART RSR is reset. The RSR baud rate is switched to the highest rate.
2. A falling edge on UART Rx pin triggers the beginning of the start bit. The rate measuring counter will start counting UART_PCLK cycles.
3. During the receipt of the start bit, 16 pulses are generated on the RSR baud input with the frequency of the UART input clock, guaranteeing the start bit is stored in the RSR.
4. During the receipt of the start bit (and the character LSB for Mode = 0), the rate counter will continue incrementing with the pre-scaled UART input clock (UART_PCLK).
5. If Mode = 0, the rate counter will stop on next falling edge of the UART Rx pin. If Mode = 1, the rate counter will stop on the next rising edge of the UART Rx pin.
6. The rate counter is loaded into DLM/DLL and the baud rate will be switched to normal operation. After setting the DLM/DLL, the end of auto-baud interrupt IIR ABEOInt will be set, if enabled. The RSR will now continue receiving the remaining bits of the ”A/a" character.

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a. Mode 0 (start bit and LSB are used for auto-baud)



b. Mode 1 (only start bit is used for auto-baud)

Fig 88. Auto-baud a) mode 0 and b) mode 1 waveform

32.5.11 IrDA Control Register (UART3)

The IrDA Control Register enables and configures the IrDA mode for UART3 only. The value of U3ICR should not be changed while transmitting or receiving data, or data loss or corruption may occur.

Remark: IrDA is available on UART3 only.

Table 676. IrDA Control Register (ICR - address 0x4000 8024) bit description

Bit	Symbol	Value	Description	Reset value
0	IRDAEN		IrDA mode enable.	0
		0	IrDA mode on UART3 is disabled, UART3 acts as a standard UART.	
		1	IrDA mode on UART3 is enabled.	

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Table 676. IrDA Control Register (ICR - address 0x4000 8024) bit description

Bit	Symbol	Value	Description	Reset value
1	IRDAINV		Serial input direction.	0
		0	The serial input is not inverted.	
		1	The serial input is inverted. This has no effect on the serial output.	
2	FIXPULSEEN		IrDA fixed pulse width mode.	0
		0	IrDA fixed pulse width mode disabled.	
		1	IrDA fixed pulse width mode enabled.	
5:3	PULSEDIV		Configures the pulse when FixPulseEn = 1. See Table 677 for details.	0
31:6	-	NA	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0

The PulseDiv bits in U3ICR are used to select the pulse width when the fixed pulse width mode is used in IrDA mode (IrDAEn = 1 and FixPulseEn = 1). The value of these bits should be set so that the resulting pulse width is at least 1.63 μs. Table 677 shows the possible pulse widths.

Table 677. IrDA Pulse Width

FixPulseEn	PulseDiv	IrDA Transmitter Pulse width (μs)
0	x	$3 / (16 \times \text{baud rate})$
1	0	$2 \times T_{PCLK}$
1	1	$4 \times T_{PCLK}$
1	2	$8 \times T_{PCLK}$
1	3	$16 \times T_{PCLK}$
1	4	$32 \times T_{PCLK}$
1	5	$64 \times T_{PCLK}$
1	6	$128 \times T_{PCLK}$
1	7	$256 \times T_{PCLK}$

32.5.12 UART Fractional Divider Register (U0FDR - 0x4000 8028)

The UART Fractional Divider Register (FDR) controls the clock pre-scaler for the baud rate generation and can be read and written at the user’s discretion. This pre-scaler takes the APB clock and generates an output clock according to the specified fractional requirements.

Important: If the fractional divider is active (DIVADDVAL > 0) and DLM = 0, the value of the DLL register must be 3 or greater.

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Table 678. UART Fractional Divider Register (FDR - addresses 0x4008 1028 (UART0), 0x400C 1028 (UART2), 0x400C 2028 (UART3)) bit description

Bit	Function	Description	Reset value
3:0	DIVADDVAL	Baud rate generation pre-scaler divisor value. If this field is 0, fractional baud rate generator will not impact the UART baud rate.	0
7:4	MULVAL	Baud rate pre-scaler multiplier value. This field must be greater or equal 1 for UART to operate properly, regardless of whether the fractional baud rate generator is used or not.	1
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0

This register controls the clock pre-scaler for the baud rate generation. The reset value of the register keeps the fractional capabilities of UART disabled making sure that UART is fully software and hardware compatible with UARTs not equipped with this feature.

The UART baud rate can be calculated as:

$$UART_{baudrate} = \frac{PCLK}{16 \times (256 \times DLM + DLL) \times \left(1 + \frac{DivAddVal}{MulVal}\right)} \quad (7)$$

Where UART_PCLK is the peripheral clock, DLM and DLL are the standard UART baud rate divider registers, and DIVADDVAL and MULVAL are UART fractional baud rate generator specific parameters.

The value of MULVAL and DIVADDVAL should comply to the following conditions:

1. $1 \leq$ MULVAL ≤ 15
2. $0 \leq$ DIVADDVAL ≤ 14
3. DIVADDVAL< MULVAL

The value of the FDR should not be modified while transmitting/receiving data or data may be lost or corrupted.

If the FDR register value does not comply to these two requests, then the fractional divider output is undefined. If DIVADDVAL is zero then the fractional divider is disabled, and the clock will not be divided.

32.5.12.1 Baud rate calculation

UART can operate with or without using the Fractional Divider. In real-life applications it is likely that the desired baud rate can be achieved using several different Fractional Divider settings. The following algorithm illustrates one way of finding a set of DLM, DLL, MULVAL, and DIVADDVAL values. Such set of parameters yields a baud rate with a relative error of less than 1.1% from the desired one.

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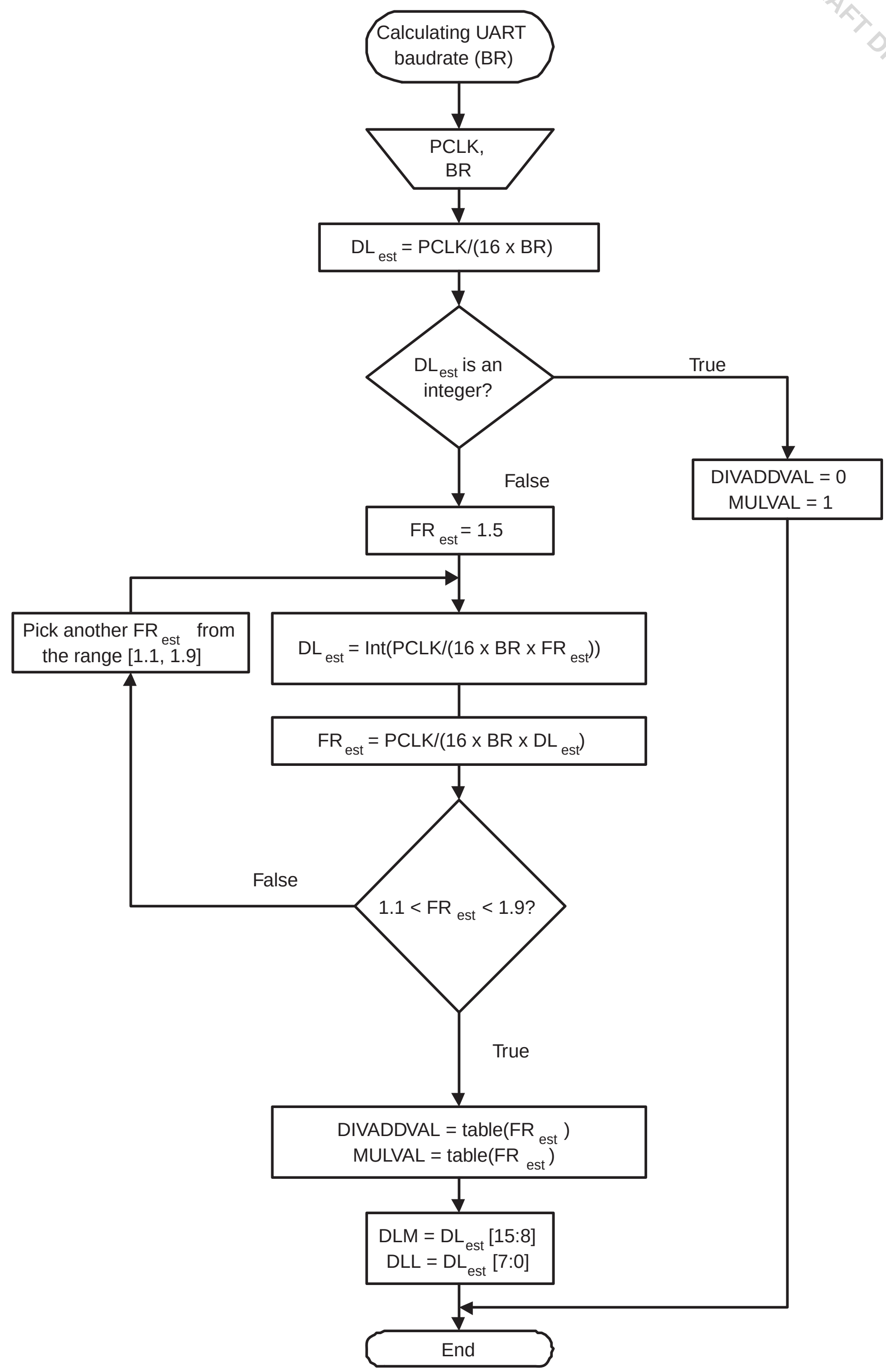


Fig 89. Algorithm for setting UART dividers

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Table 679. Fractional Divider setting look-up table

FR	DivAddVal/ MulVal	FR	DivAddVal/ MulVal	FR	DivAddVal/ MulVal	FR	DivAddVal/ MulVal
1.000	0/1	1.250	1/4	1.500	1/2	1.750	3/4
1.067	1/15	1.267	4/15	1.533	8/15	1.769	10/13
1.071	1/14	1.273	3/11	1.538	7/13	1.778	7/9
1.077	1/13	1.286	2/7	1.545	6/11	1.786	11/14
1.083	1/12	1.300	3/10	1.556	5/9	1.800	4/5
1.091	1/11	1.308	4/13	1.571	4/7	1.818	9/11
1.100	1/10	1.333	1/3	1.583	7/12	1.833	5/6
1.111	1/9	1.357	5/14	1.600	3/5	1.846	11/13
1.125	1/8	1.364	4/11	1.615	8/13	1.857	6/7
1.133	2/15	1.375	3/8	1.625	5/8	1.867	13/15
1.143	1/7	1.385	5/13	1.636	7/11	1.875	7/8
1.154	2/13	1.400	2/5	1.643	9/14	1.889	8/9
1.167	1/6	1.417	5/12	1.667	2/3	1.900	9/10
1.182	2/11	1.429	3/7	1.692	9/13	1.909	10/11
1.200	1/5	1.444	4/9	1.700	7/10	1.917	11/12
1.214	3/14	1.455	5/11	1.714	5/7	1.923	12/13
1.222	2/9	1.462	6/13	1.727	8/11	1.929	13/14
1.231	3/13	1.467	7/15	1.733	11/15	1.933	14/15

32.5.12.1.1 Example 1: UART_PCLK = 14.7456 MHz, BR = 9600

According to the provided algorithm DL_{est} = PCLK/(16 x BR) = 14.7456 MHz / (16 x 9600) = 96. Since this DL_{est} is an integer number, DIVADDVAL = 0, MULVAL = 1, DLM = 0, and DLL = 96.

32.5.12.1.2 Example 2: UART_PCLK = 12 MHz, BR = 115200

According to the provided algorithm DL_{est} = PCLK/(16 x BR) = 12 MHz / (16 x 115200) = 6.51. This DL_{est} is not an integer number and the next step is to estimate the FR parameter. Using an initial estimate of FR_{est} = 1.5 a new DL_{est} = 4 is calculated and FR_{est} is recalculated as FR_{est} = 1.628. Since FRest = 1.628 is within the specified range of 1.1 and 1.9, DIVADDVAL and MULVAL values can be obtained from the attached look-up table.

The closest value for FRest = 1.628 in the look-up Table 679 is FR = 1.625. It is equivalent to DIVADDVAL = 5 and MULVAL = 8.

Based on these findings, the suggested UART setup would be: DLM = 0, DLL = 4, DIVADDVAL = 5, and MULVAL = 8. According to Equation 7, the UART’s baud rate is 115384. This rate has a relative error of 0.16% from the originally specified 115200.

32.5.13 UART Half-duplex enable register

Remark: The HDEN register should be disabled when in smart card mode (smart card by default runs in half-duplex mode).

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After reset the USART will be in full-duplex mode, meaning that both TX and RX work independently. After setting the HDEN bit, the USART will be in half-duplex mode. In this mode, the USART ensures that the receiver is locked when idle, or will enter a locked state after having received a complete ongoing character reception. Line conflicts must be handled in software. The behavior of the USART is unpredictactable when data is presented for reception while data is being transmitted.

For this reason, the value of the HDEN register should not be modified while sending or receiving data, or data may be lost or corrupted.

Table 680. UART Half duplex enable register (HDEN - addresses 0x4008 1040 (UART0), 0x400C 1040 (UART2), 0x400C 2040 (UART3)) bit description

Bit	Symbol	Value	Description	Reset value
0	HDEN		Half-duplex mode enable	0
		0	Disable half-duplex mode.	
		1	Enable half-duplex mode.	
31:1	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

32.5.14 UART Smart card interface control register

Table 681. UART Smart card interface control register (SCICTRL - addresses 0x4008 1048 (UART0), 0x400C 1048 (UART2), 0x400C 2048 (UART3)) bit description

Bit	Symbol	Value	Description	Reset value
0	SCIEN		Smart Card Interface Enable.	0
		0	Smart card interface disabled.	
		1	Asynchronous half duplex smart card interface is enabled.	
1	NACKDIS		NACK response disable. Only applicable in T=0.	0
		0	A NACK response is enabled.	
		1	A NACK response is inhibited.	
2	PROTSEL		Protocol selection as defined in the ISO7816-3 standard.	0
		0	T = 0	
		1	T = 1	
7:5	TXRETRY		Maximum number of retransmissions in case of a negative acknowledge (protocol T=0). When the retry counter is exceeded, the USART will be locked until the FIFO is cleared. A TX error interrupt is generated when enabled.	-
15:8	GUARDTIME		Extra guard time. No extra guard time (0x0) results in a standard guard time as defined in ISO 7816-3, depending on the protocol type. A guard time of 0xFF indicates a minimal guard time as defined for the selected protocol.	
31:16	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

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After reset the USART smart card interface will be disabled. After setting the SCIEN bit the USART will be in ISO 7816-3 compliant asynchronous smart card mode T=0.

The NACKDIS bit is used to inhibit a nack response during T=0 (the I/O line is not pulled low during the guard time to indicate an erroneous reception). The received character will be stored in the RX FIFO but a parity error will be generated. It is up to the software to handle the incorrect received character.

The PROTSEL bit is used to selected between the two supported smart card protocols T=0 and T=1. More information on these protocols can be found in the ISO 7816-3 standard.

The retry bit field indicates the number of retransmission when receiving a NACK response, which can be up to 7 trails. When the number is exceeded, an interrupt is generated and the USART is locked until the FIFO is empty. This can be done by flushing the FIFO. When no FIFO is available, or the FIFO is already empty, the interrupt can be used by the software to determine the next action.

The guard time bit file is used to program the extra number of guard time cycles to allow the smart card to process the information before sending a response. The extra guard time can be programmed from 0 to 255, where 255 indicates the minimum possible character length. This value is depending on the selected protocol and can be either 11 etu for protocol T=1 or 12 etu for protocol T=0.

Waiting times as defined in the standard cannot be programmed directly, but are implemented using the CAP1 and CAP2 inputs of the timers. Use the CREG6 register in the CREG block (see Table 37) to set up the timers for polling the tx_active and rx_active polling signals.

Remark: The SCICTRL register should not be modified while sending or receiving data, or data may be lost or corrupted.

Remark: The SCICTRL register should not be enabled in combination with the SYNCCTRL register, as only asynchronous smart card is supported.

32.5.15 UART RS485 Control register

The RS485CTRL register controls the configuration of the UART in RS-485/EIA-485 mode.

Table 682. UART RS485 Control register (RS485CTRL - addresses 0x4008 104C (UART0), 0x400C 104C (UART2), 0x400C 204C (UART3)) bit description

Bit	Symbol	Value	Description	Reset value
0	NMMEN		NMM enable.	0
		0	RS-485/EIA-485 Normal Multidrop Mode (NMM) is disabled.	
		1	RS-485/EIA-485 Normal Multidrop Mode (NMM) is enabled. In this mode, an address is detected when a received byte causes the UART to set the parity error and generate an interrupt.	

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Table 682. UART RS485 Control register (RS485CTRL - addresses 0x4008 104C (UART0), 0x400C 104C (UART2), 0x400C 204C (UART3)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value
1	RXDIS		Receiver enable.	0
		0	The receiver is enabled.	
		1	The receiver is disabled.	
2	AADEN		AAD enable	0
		0	Auto Address Detect (AAD) is disabled.	
		1	Auto Address Detect (AAD) is enabled.	
3	-	-	Reserved.	-
4	DCTRL		Direction control for DIR pin.	0
		0	Disable Auto Direction Control.	
		1	Enable Auto Direction Control.	
5	OINV		Direction control pin polarity. This bit reverses the polarity of the direction control signal on the DIR pin.	0
		0	The direction control pin will be driven to logic ‘0’ when the transmitter has data to be sent. It will be driven to logic ‘1’ after the last bit of data has been transmitted.	
		1	The direction control pin will be driven to logic ‘1’ when the transmitter has data to be sent. It will be driven to logic ‘0’ after the last bit of data has been transmitted.	
31:6	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

After reset RS485 mode will be disabled. The RS485 feature allows the USART to be configured as one of multiple addressable slave receivers controlled by a single USART. In RS485 mode the USART differentiates between an address character and a data character by means of a ninth bit. The parity bit is used to implement this bit, and when set to ‘1’ indicates an address and when set to ‘0’ indicates data. RS485 mode is enabled by setting the NMMEN bit. The USART slave receiver can be assigned a unique address and, manually or automatically, reject or accept data based on a received address. See section Section 32.6.3 for details.

32.5.16 UART RS485 Address Match register

The RS485ADRMATCH register contains the address match value for RS-485/EIA-485 mode.

Table 683. UART RS485 Address Match register (RS485ADRMATCH - addresses 0x4008 1050 (UART0), 0x400C 1050 (UART2), 0x400C 2050 (UART3)) bit description

Bit	Symbol	Description	Reset value
7:0	ADRMATCH	Contains the address match value.	0x00
31:8	-	Reserved	-

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The ADRMATCH bit field contains the slave address match value that is used to compare a received address value to. During automatic address detection, this value is used to accept or reject serial input data.

32.5.17 UART1 RS485 Delay value register

The user may program the 8-bit RS485DLY register with a delay between the last stop bit leaving the TXFIFO and the de-assertion of the DIR pin. This delay time is in periods of the baud clock. Any delay time from 0 to 255 bit times may be programmed.

Table 684. UART RS485 Delay value register (RS485DLY - addresses 0x4008 1054 (UART0), 0x400C 1054 (UART2), 0x400C 2054 (UART3)) bit description

Bit	Symbol	Description	Reset value
7:0	DLY	Contains the direction control delay value. This register works in conjunction with an 8-bit counter.	0x00
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

32.5.18 UART Synchronous mode control register

SYNCCTRL register is a Read/write register that controls the synchronous mode. The synchronous mode control module generates or receives the synchronous clock with the serial input/ output data and distributes the edge detect samples to the transmit and receive shift registers.

Table 685. UART Synchronous mode control registers (SYNCCTRL - address addresses 0x4008 1058 (UART0), 0x400C 1058 (UART2), 0x400C 2058 (UART3)) bit description

Bit	Symbol	Value	Description	Reset value
0	SYNC		Enables synchronous mode.	0
		0	Disabled	
		1	Enabled	
1	CSRC		Clock source select.	0
		0	Synchronous slave mode (SCLK in)	
		1	Synchronous master mode (SCLK out)	
2	FES		Falling edge sampling.	0
		0	RxD is sampled on the rising edge of SCLK	
		1	RxD is sampled on the falling edge of SCLK	
3	TSBYPASS		Transmit synchronization register bypass.	0
		0	<tbd>	
		1	<tbd>	
4	CSCEN		Continuous master clock enable (used only when CSRC is 1)	0
		0	SCLK cycles only when characters are being sent on TxD	
		1	SCLK runs continuously (characters can be received on RxD independently from transmission on TxD)	

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Table 685. UART Synchronous mode control registers (SYNCCTRL - address addresses 0x4008 1058 (UART0), 0x400C 1058 (UART2), 0x400C 2058 (UART3)) bit description

Bit	Symbol	Value	Description	Reset value
5	SSSDIS		Start/stop bits	0
		0	Send start and stop bits as in other modes.	
		1	Do not send start/stop bits.	
6	CCCLR		Continuous clock clear	0
		0	CSCEN is under software control.	
		1	Hardware clears CSCEN after each character is received.	
31:7	-		Reserved. The value read from a reserved bit is not defined.	NA

After reset, synchronous mode is disabled. Synchronous mode allows the user to send (synchronous master mode) or receive (synchronous slave mode) a clock with the serial input and output data. Synchronous mode is enabled by setting the SYNC bit. The CSRC bit can be used to switch between synchronous slave mode (logic 0) and synchronous master mode (logic 1). The serial data can either be sampled on the rising edge (default) or the falling edge of the serial clock. When the STARTSTOPDISABLE bit is set, the FES bit is hardware overwritten to sample on the falling edge.

A master clock is only required to generate a clock when transmitting data. In this case, data can only be received when data is transmitted. When the CSCEN bit is set, the clock will always be running (during synchronous master mode only), allowing data to be received continuously.

Note that this option should not be used in combination with STARTSTOPDISABLE (during full-duplex communication). The continuous clock can be automatically stopped by hardware after having received a complete character. This can be done by asserting the CCCLR bit. This is useful in half-duplex mode, where the clock cannot be generated by sending a character. After the reception of one character, the CSCEN bit is automatically cleared by hardware. When another character needs to be received, the CSCEN should be enabled again.

By default data transmission and reception performs the same in asynchronous mode and synchronous mode. When the STARTSTOPDISABLE bit is set, no start and stop bits are transmitted (nor are they received). This means that all bits that are send or received (a clock is running) are data bits.

Remark: The value of the SYNCCTRL register should not be modified while transmitting/receiving, data or data might get lost or corrupted.

Remark: The SYNCCTRL register should not be enabled in combination with the SCICTRL register, as only asynchronous smart card is supported.

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32.5.19 UART Transmit Enable Register

In addition to being equipped with full hardware flow control (auto-cts and auto-rts mechanisms described above), TER enables implementation of software flow control. When TxEn = 1, UART transmitter will keep sending data as long as they are available. As soon as TxEn becomes 0, UART transmission will stop.

Table 686 describes how to use TXEn bit in order to achieve software flow control.

Table 686. UART Transmit Enable Register (TER - addresses 0x4008 1030 (UART0), 0x400C 1030 (UART2), 0x400C 205C (UART3)) bit description

Bit	Symbol	Description	Reset value
0	TXEN	Transmit enable. After reset transmission is enabled. When the txen bit is de-asserted, no data will be transmitted although data may be pending in the TSR or THR.	1
31:1	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

32.6 Functional description

32.6.1 Asynchronous mode

<tbd>

32.6.2 Synchronous mode

When the synchronous receiver/ transmitter feature is configured (USART), the serial interface is extended with a serial input and output clock and an output enable for controlling the clock pad.

Fig 90. USART serial interface protocol

By default transmission and reception in synchronous mode operates uses the same protocol as in asynchronous mode. Synchronous mode can be configured using the Synchronous Mode Control Register. This register allows to control:

- The direction of the serial clock, i.e. synchronous slave or master mode
- The sampling edge of the serial clock
- Two-stage or one stage synchronization of the input serial clock during transmission
- During synchronous master mode, the clock can be continuous or disabled when in idle or break mode
- The transmission of start and stop bits can be omitted. Valid data is identified by a running clock. Sampling is always done on the falling edge of the serial clock

Data is shifted in the receive shift register at the sampling edge of the serial clock.

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32.6.2.1 Synchronous slave mode

This mode is enabled by setting the CSRC bit of the control register to ‘0’. During synchronous slave mode, an external clock is required that clocks the serial input and output data. Note that internally, the serial clock is treated as a data signal. Edge detection on the serial clock is performed to synchronize the serial clock with the UART clock domain, hence no registers are clocked with the serial clock.

Reception

By default the received character is similar to the character in asynchronous mode. The serial data stream is kept HIGH when no data is available. During this time it is not required for the external serial clock to be running. The first bit that will be received is the start bit. During this time, the external serial clock must be running. The beginning of the start bit can either be aligned with the rising edge of the serial clock (sampling on the falling edge) or the falling edge (sampling on the rising edge), see the FES bit in Table 685. When sampling on the rising edge, it is not required that the beginning of the start bit is aligned with a clock edge (the clock may not have been running before). In this case, the edge on the serial input data due to the start bit (logic 1 to 0) is used to determine the start of the character (see figure 11).

Fig 91. Transmission of data in synchronous slave mode

The NOSTARTSTOPBITS bit of the Synchronous Mode Control register allows the user to disable the transmission/ reception of the start and stop bits, improving the efficiency of the USART. As a character is no longer identified by the start and stop bits, the serial clock is used to determine the data bits. When the serial clock is running, all data that is sampled is regarded as valid data.

In order to be able to identify the start of a character, the beginning of the character must be aligned with the rising edge of the serial clock. For this reason, the FES bit of the Synchronous Mode Control register is forced in hardware to ‘1’.

Directly after sampling the last bit, the character is stored in the receive FIFO.

Transmission

During synchronous slave mode, data can only be transmitted when the external serial clock is running. Hence, when no start and stop bits are sent, transmission can only take place when data is received from the master. When the start and stop bits are transmitted, the external clock may only be detected after the first half of the received start bit (sampling at the rising edge of the external serial clock). By using the edge created by the received start bit (logic 1 to 0), it is made sure that the start bit of the character that is to be transmitted by the slave is stable before this rising edge the external slave clock. In this way it is ensured, that the master receives as many bits as it has transmitted.

When the first sample edge of the incoming serial clock samples a ‘1’ on the serial input data (and start-stop bits are transmitted, thus the master has not initiated a transaction yet), it is assumed that the master is running a continuous clock (instead of only running the clock when sending data characters). The USART will not wait for a start bit from the master, but will immediately start transmitting data when available. Note that in this

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situation, the number of bits transmitted by the master and the number of bits transmitted by the slave (received by the master) may not be aligned. It is assumed that a higher level protocol ensures that complete characters are received when the master stops the clock.

Transmission of data during synchronous slave mode is most time-critical. First the external serial input clock must be detected using edge detection logic. Then, data needs to be shifted out and be stable before the sampling edge of the external serial clock.

Remark: In this mode the u_clk period is allowed to be 4x the serial clock period.

32.6.2.2 Synchronous master mode

Synchronous master mode is enabled by setting the CSRC register bit to ‘1’. In this mode, the external clock is generated internally by the baud-rate generation logic and is used to clock the input and output serial data. The functionality of the baud-rate generation is described in Section 32.5.12.1. Auto-baud is not supported during synchronous mode. The 1x baud rate clock is used to shift out the serial output data and to sample the serial input data.

Synchronous master mode behaves similar to the slave mode, except that the serial input data is not registered at the interface but is clocked in the UART clock domain at the sampling edge of the serial clock.

During synchronous master mode, when start and stop bits are transmitted, the user can enable the external clock continuously using cscen bit of the Synchronous Mode Control register. This allows the connected slave to transmit data even when no data is transmitted by the master itself.

32.6.3 RS-485/EIA-485 modes of operation

The RS-485/EIA-485 feature allows the UART to be configured as an addressable slave. The addressable slave is one of multiple slaves controlled by a single master.

The UART master transmitter will identify an address character by setting the parity (9th) bit to ‘1’. For data characters, the parity bit is set to ‘0’.

Each UART slave receiver can be assigned a unique address. The slave can be programmed to either manually or automatically reject data following an address which is not theirs.

RS-485/EIA-485 Normal Multidrop Mode (NMM)

Setting the RS485CTRL bit 0 enables this mode. In this mode, an address is detected when a received byte causes the UART to set the parity error and generate an interrupt.

If the receiver is disabled (RS485CTRL bit 1 = ‘1’), any received data bytes will be ignored and will not be stored in the RXFIFO. When an address byte is detected (parity bit = ‘1’) it will be placed into the RXFIFO and an Rx Data Ready Interrupt will be generated. The processor can then read the address byte and decide whether or not to enable the receiver to accept the following data.

While the receiver is enabled (RS485CTRL bit 1 =’0’), all received bytes will be accepted and stored in the RXFIFO regardless of whether they are data or address. When an address character is received a parity error interrupt will be generated and the processor can decide whether or not to disable the receiver.

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RS-485/EIA-485 Auto Address Detection (AAD) mode

When both RS485CTRL register bits 0 (9-bit mode enable) and 2 (AAD mode enable) are set, the UART is in auto address detect mode.

In this mode, the receiver will compare any address byte received (parity = ‘1’) to the 8-bit value programmed into the RS485ADRMATCH register.

If the receiver is disabled (RS485CTRL bit 1 = ‘1’), any received byte will be discarded if it is either a data byte OR an address byte which fails to match the RS485ADRMATCH value.

When a matching address character is detected it will be pushed onto the RXFIFO along with the parity bit, and the receiver will be automatically enabled (RS485CTRL bit 1 will be cleared by hardware). The receiver will also generate an Rx Data Ready Interrupt.

While the receiver is enabled (RS485CTRL bit 1 = ‘0’), all bytes received will be accepted and stored in the RXFIFO until an address byte which does not match the RS485ADRMATCH value is received. When this occurs, the receiver will be automatically disabled in hardware (RS485CTRL bit 1 will be set), The received non-matching address character will not be stored in the RXFIFO.

RS-485/EIA-485 Auto Direction Control

RS485/EIA-485 mode includes the option of allowing the transmitter to automatically control the state of the DIR pin as a direction control output signal.

Setting RS485CTRL bit 4 = ‘1’ enables this feature.

When Auto Direction Control is enabled, the selected pin will be asserted (driven LOW) when the CPU writes data into the TXFIFO. The pin will be de-asserted (driven HIGH) once the last bit of data has been transmitted. See bits 4 and 5 in the RS485CTRL register.

The RS485CTRL bit 4 takes precedence over all other mechanisms controlling the direction control pin.

RS485/EIA-485 driver delay time

The driver delay time is the delay between the last stop bit leaving the TXFIFO and the de-assertion of the DIR pin. This delay time can be programmed in the 8-bit RS485DLY register. The delay time is in periods of the baud clock. Any delay time from 0 to 255 bit times may be used.

RS485/EIA-485 output inversion

The polarity of the direction control signal on the DIR pin can be reversed by programming bit 5 in the RS485CTRL register. When this bit is set, the direction control pin will be driven to logic 1 when the transmitter has data waiting to be sent. The direction control pin will be driven to logic 0 after the last bit of data has been transmitted.

32.6.4 Smart card mode

Figure 92 shows a typical asynchronous smart card application.

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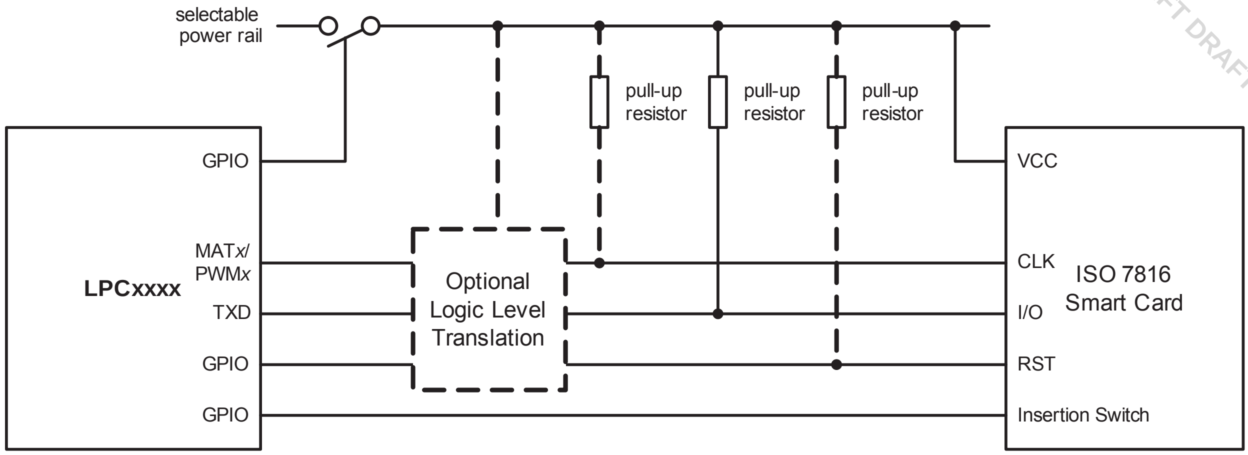


Fig 92. Typical smart card application

When the SCIEN bit in the SCICTRL register (Table 681) is set as described above, the UART provides bidirectional serial data on the open-drain TXD pin. No RXD pin is used when SCIEN is 1. If a clock source is needed as an oscillator source into the Smart Card, a timer match or PWM output can be used in cases when a higher frequency clock is needed that is not synchronous with the data bit rate. The UART SCLK pin will output synchronously with the data and at the data bit rate and may not be adequate for most asynchronous cards. Software must use timers to implement character and block waiting times (no hardware support via trigger signals is provided on the LPCxxxx). GPIO pins can be used to control the smart card reset and power pins. Any power supplied to the card must be externally switched as card power supply requirements often exceed source currents possible on the LPCxxxx. As the specific application may accommodate any of the available ISO 7816 class A, B, or C power requirements, be aware of the logic level tolerances and requirements when communicating or powering cards that use different power rails than the LPCxxxx.

32.6.4.1 Smart card set-up procedure

A T = 0 protocol transfer consists of 8-bits of data, an even parity bit, and two guard bits that allow for the receiver of the particular transfer to flag parity errors through the NACK response (see Figure 93). Extra guard bits may be added according to card requirements. If no NACK is sent (provided the interface accepts them in SCICTRL), the next byte may be transmitted immediately after the last guard bit. If the NACK is sent, the transmitter will retry sending the byte until successfully received or until the SCICTRL retry limit has been met.

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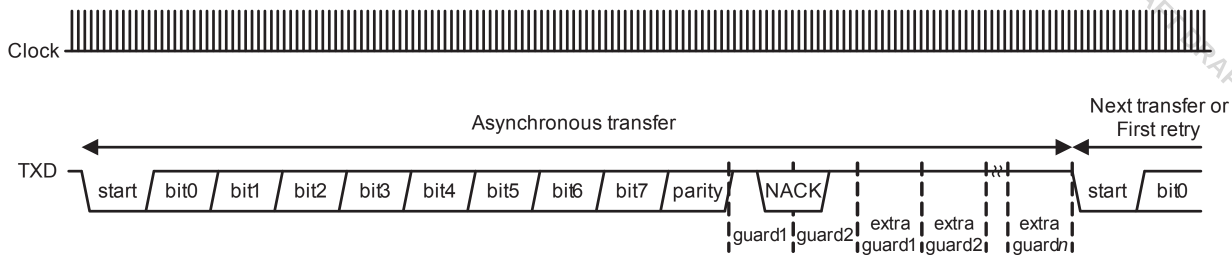


Fig 93. Smart card T = 0 waveform

The smart card must be set up with the following considerations:

1. If necessary, bring the UART out of reset and enable clocking to the peripheral.
2. Setup an available UART TXD pin for the bidirectional transfers.
3. Setup the match output or PWM clock source. The default clock requirement for most asynchronous cards is 372 times the bit rate.
4. Configure DLL and DLM for baud rate. It may not be necessary to target a specific standard baud rate but rather to maintain a fraction of the previously mentioned clock rate. For example if the clock rate is set to 4 MHz the baud rate would be 10753. A clock rate of 3.5712 MHz would need a baud rate of 9600. An ISO 7816 PPS exchange may require the baud rate to be changed later.
5. Configure LCR for character size and parity (typically 8-bit and even parity).
6. Configure SCICTRL with the desired NACK response, extra guard bits, and protocol type.
7. Place the GPIO output signals into an inactive state where card power is off, RST is low, and CLK is low and unchanging.

Thereafter, software should monitor card insertion, handle activation, wait for answer to reset as described in ISO7816-3.

32.7 Architecture

The architecture of the UART is shown below in the block diagram.

The APB interface provides a communications link between the CPU or host and the UART.

The UART receiver block, RX, monitors the serial input line, RXD, for valid input. The UART RX Shift Register (RSR) accepts valid characters via RXD. After a valid character is assembled in the RSR, it is passed to the UART RX Buffer Register FIFO to await access by the CPU or host via the generic host interface.

The UART transmitter block, TX, accepts data written by the CPU or host and buffers the data in the UART TX Holding Register FIFO (THR). The UART TX Shift Register (TSR) reads the data stored in the THR and assembles the data to transmit via the serial output pin, TXD1.

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The UART Baud Rate Generator block, BRG, generates the timing enables used by the UART TX block. The BRG clock input source is UART_PCLK. The main clock is divided down per the divisor specified in the DLL and DLM registers. This divided down clock is a 16x oversample clock, NBAUDOUT.

The interrupt interface contains registers IER and IIR. The interrupt interface receives several one clock wide enables from the TX and RX blocks.

Status information from the TX and RX is stored in the LSR. Control information for the TX and RX is stored in the LCR.

Fig 94. UART block diagram

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33.1 How to read this chapter

The UART1 controller is available on all LPC18xx parts.

33.2 Basic configuration

The UART1 is configured as follows:

- See Table 687 for clocking and power control.
- The UART1 is reset by the UART1_RST (reset #45).
- The UART1 interrupt is connected to slot # 25 in the NVIC.
- For connecting the UART1 receive and transmit lines to the GPDMA, use the DMAMUX register in the CREG block (see Table 35) and enable the GPDMA channel in the DMA Channel Configuration registers (Section 16.6.20).

Table 687. UART1 clocking and power control

	Base clock	Branch clock	Maximum frequency
UART1 clock to register interface	BASE_M3_CLK	CLK_M3_UART0	150 MHz
UART1 peripheral clock (PCLK)	BASE_UART1_CLK	CLK_APB0_UART1	150 MHz

33.3 Features

- Full modem control handshaking available.
- Data sizes of 5, 6, 7, and 8 bits.
- Parity generation and checking: odd, even mark, space or none.
- One or two stop bits.
- 16 byte Receive and Transmit FIFOs.
- Built-in baud rate generator, including a fractional rate divider for great versatility.
- Supports DMA for both transmit and receive.
- Auto-baud capability.
- Break generation and detection.
- Multiprocessor addressing mode.
- RS-485 support.

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33.4 Pin description

Table 688: UART1 Pin description

Pin	Direction	Description
RXD1	Input	**Serial Input.** Serial receive data.
TXD1	Output	**Serial Output.** Serial transmit data.
CTS1	Input	**Clear To Send.** Active low signal indicates if the external modem is ready to accept transmitted data via TXD1 from the UART1. In normal operation of the modem interface (U1MCR[4] = 0), the complement value of this signal is stored in U1MSR[4]. State change information is stored in U1MSR[0] and is a source for a priority level 4 interrupt, if enabled (U1IER[3] = 1). Clear to send. CTS1 is an asynchronous, active low modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the Modem Status Register (MSR) indicates that CTS1 has changed states since the last read from the MSR. If the modem status interrupt is enabled when CTS1 changes levels and the auto-cts mode is not enabled, an interrupt is generated. CTS1 is also used in the auto-cts mode to control the transmitter.
DCD1	Input	**Data Carrier Detect.** Active low signal indicates if the external modem has established a communication link with the UART1 and data may be exchanged. In normal operation of the modem interface (U1MCR[4]=0), the complement value of this signal is stored in U1MSR[7]. State change information is stored in U1MSR3 and is a source for a priority level 4 interrupt, if enabled (U1IER[3] = 1).
DSR1	Input	**Data Set Ready.** Active low signal indicates if the external modem is ready to establish a communications link with the UART1. In normal operation of the modem interface (U1MCR[4] = 0), the complement value of this signal is stored in U1MSR[5]. State change information is stored in U1MSR[1] and is a source for a priority level 4 interrupt, if enabled (U1IER[3] = 1).
DTR1	Output	Data Terminal Ready. Active low signal indicates that the UART1 is ready to establish connection with external modem. The complement value of this signal is stored in U1MCR[0]. The DTR pin can also be used as an RS-485/EIA-485 output enable signal.
RI1	Input	**Ring Indicator.** Active low signal indicates that a telephone ringing signal has been detected by the modem. In normal operation of the modem interface (U1MCR[4] = 0), the complement value of this signal is stored in U1MSR[6]. State change information is stored in U1MSR[2] and is a source for a priority level 4 interrupt, if enabled (U1IER[3] = 1).
RTS1	Output	**Request To Send.** Active low signal indicates that the UART1 would like to transmit data to the external modem. The complement value of this signal is stored in U1MCR[1]. In auto-rts mode, RTS1 is used to control the transmitter FIFO threshold logic. Request to send. RTS1 is an active low signal informing the modem or data set that the UART is ready to receive data. RTS1 is set to the active (low) level by setting the RTS modem control register bit and is set to the inactive (high) level either as a result of a system reset or during loop-back mode operations or by clearing bit 1 (RTS) of the MCR. In the auto-rts mode, RTS1 is controlled by the transmitter FIFO threshold logic. The RTS pin can also be used as an RS-485/EIA-485 output enable signal.

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33.5 Register description

UART1 contains registers organized as shown in Table 689. The Divisor Latch Access Bit (DLAB) is contained in U1LCR[7] and enables access to the Divisor Latches.

Reset value reflects the data stored in used bits only. It does not include the content of reserved bits.

Table 689: Register overview: UART1 (base address 0x4008 2000)

Name	Access	Address offset	Description	Reset value
RBR	RO	0x000	Receiver Buffer Register. Contains the next received character to be read. (DLAB=0)	NA
THR	WO	0x000	Transmit Holding Register. The next character to be transmitted is written here. (DLAB=0)	NA
DLL	R/W	0x000	Divisor Latch LSB. Least significant byte of the baud rate divisor value. The full divisor is used to generate a baud rate from the fractional rate divider. (DLAB=1)	0x01
DLM	R/W	0x004	Divisor Latch MSB. Most significant byte of the baud rate divisor value. The full divisor is used to generate a baud rate from the fractional rate divider.(DLAB=1)	0x00
IER	R/W	0x004	Interrupt Enable Register. Contains individual interrupt enable bits for the 7 potential UART1 interrupts. (DLAB=0)	0x00
IIR	RO	0x008	Interrupt ID Register. Identifies which interrupt(s) are pending.	0x01
FCR	WO	0x008	FIFO Control Register. Controls UART1 FIFO usage and modes.	0x00
LCR	R/W	0x00C	Line Control Register. Contains controls for frame formatting and break generation.	0x00
MCR	R/W	0x010	Modem Control Register. Contains controls for flow control handshaking and loopback mode.	0x00
LSR	RO	0x014	Line Status Register. Contains flags for transmit and receive status, including line errors.	0x60
MSR	RO	0x018	Modem Status Register. Contains handshake signal status flags.	0x00
SCR	R/W	0x01C	Scratch Pad Register. 8-bit temporary storage for software.	0x00
ACR	R/W	0x020	Auto-baud Control Register. Contains controls for the auto-baud feature.	0x00
FDR	R/W	0x028	Fractional Divider Register. Generates a clock input for the baud rate divider.	0x10
TER	R/W	0x030	Transmit Enable Register. Turns off UART transmitter for use with software flow control.	0x80
RS485CTRL	R/W	0x04C	RS-485/EIA-485 Control. Contains controls to configure various aspects of RS-485/EIA-485 modes.	0x00

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Table 689: Register overview: UART1 (base address 0x4008 2000) *…continued*

Name	Access	Address offset	Description	Reset value
RS485ADRMATCH	R/W	0x050	RS-485/EIA-485 address match. Contains the address match value for RS-485/EIA-485 mode.	0x00
RS485DLY	R/W	0x054	RS-485/EIA-485 direction control delay.	0x00
FIFOLVL	RO	0x058	FIFO Level register. Provides the current fill levels of the transmit and receive FIFOs.	0x00

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33.5.1 UART1 Receiver Buffer Register (when DLAB = 0)

The U1RBR is the top byte of the UART1 RX FIFO. The top byte of the RX FIFO contains the oldest character received and can be read via the bus interface. The LSB (bit 0) represents the “oldest” received data bit. If the character received is less than 8 bits, the unused MSBs are padded with zeroes.

The Divisor Latch Access Bit (DLAB) in U1LCR must be zero in order to access the U1RBR. The U1RBR is always read-only.

Since PE, FE and BI bits correspond to the byte sitting on the top of the RBR FIFO (i.e. the one that will be read in the next read from the RBR), the right approach for fetching the valid pair of received byte and its status bits is first to read the content of the U1LSR register, and then to read a byte from the U1RBR.

Table 690: UART1 Receiver Buffer Register when DLAB = 0 (RBR - address 0x4008 2000) bit description

Bit	Symbol	Description	Reset value
7:0	RBR	Receiver Buffer. Contains the oldest received byte in the UART1 RX FIFO.	undefined
31:8	-	Reserved, the value read from a reserved bit is not defined.	NA

33.5.2 UART1 Transmitter Holding Register (when DLAB = 0)

The write-only U1THR is the top byte of the UART1 TX FIFO. The top byte is the newest character in the TX FIFO and can be written via the bus interface. The LSB represents the first bit to transmit.

The Divisor Latch Access Bit (DLAB) in U1LCR must be zero in order to access the U1THR. The U1THR is write-only.

Table 691: UART1 Transmitter Holding Register when DLAB = 0 (THR - address 0x4008 2000) bit description

Bit	Symbol	Description	Reset value
7:0	THR	Transmit Holding Register. Writing to the UART1 Transmit Holding Register causes the data to be stored in the UART1 transmit FIFO. The byte will be sent when it reaches the bottom of the FIFO and the transmitter is available.	NA
31:8	-	Reserved, user software should not write ones to reserved bits.	NA

33.5.3 UART1 Divisor Latch LSB and MSB Registers (when DLAB = 1)

The UART1 Divisor Latch is part of the UART1 Baud Rate Generator and holds the value used, along with the Fractional Divider, to divide the APB clock (PCLK) in order to produce the baud rate clock, which must be 16x the desired baud rate. The U1DLL and U1DLM registers together form a 16-bit divisor where U1DLL contains the lower 8 bits of the divisor and U1DLM contains the higher 8 bits of the divisor. A 0x0000 value is treated like a 0x0001 value as division by zero is not allowed.The Divisor Latch Access Bit (DLAB) in U1LCR must be one in order to access the UART1 Divisor Latches. Details on how to select the right value for U1DLL and U1DLM can be found later in this chapter, see Section 33.5.16.

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Table 692: UART1 Divisor Latch LSB Register when DLAB = 1 (DLL - address 0x4008 2000) bit description

Bit	Symbol	Description	Reset value
7:0	DLLSB	Divisor Latch LSB. The UART1 Divisor Latch LSB Register, along with the U1DLM register, determines the baud rate of the UART1.	0x01
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 693: UART1 Divisor Latch MSB Register when DLAB = 1 (DLM - address 0x4008 2004) bit description

Bit	Symbol	Description	Reset value
7:0	DLMSB	Divisor Latch MSB. The UART1 Divisor Latch MSB Register, along with the U1DLL register, determines the baud rate of the UART1.	0x00
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

33.5.4 UART1 Interrupt Enable Register (when DLAB = 0)

The U1IER is used to enable the four UART1 interrupt sources.

Table 694: UART1 Interrupt Enable Register when DLAB = 0 (IER - address 0x4008 2004) bit description

Bit	Symbol	Value	Description	Reset value
0	RBRIE		RBR Interrupt Enable. Enables the Receive Data Available interrupt for UART1. It also controls the Character Receive Time-out interrupt.	0
		0	Disable the RDA interrupts.	
		1	Enable the RDA interrupts.	
1	THREIE		THRE Interrupt Enable. Enables the THRE interrupt for UART1. The status of this interrupt can be read from U1LSR[5].	0
		0	Disable the THRE interrupts.	
		1	Enable the THRE interrupts.	
2	RXIE		RX Line Interrupt Enable. Enables the UART1 RX line status interrupts. The status of this interrupt can be read from U1LSR[4:1].	0
		0	Disable the RX line status interrupts.	
		1	Enable the RX line status interrupts.	
3	MSIE		Modem Status Interrupt Enable. Enables the modem interrupt. The status of this interrupt can be read from U1MSR[3:0].	0
		0	Disable the modem interrupt.	
		1	Enable the modem interrupt.	
6:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

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Table 694: UART1 Interrupt Enable Register when DLAB = 0 (IER - address 0x4008 2004) bit description

Bit	Symbol	Value	Description	Reset value
7	CTSIE		CTS Interrupt Enable. If auto-cts mode is enabled this bit enables/disables the modem status interrupt generation on a CTS1 signal transition. If auto-cts mode is disabled a CTS1 transition will generate an interrupt if Modem Status Interrupt Enable (U1IER[3]) is set. In normal operation a CTS1 signal transition will generate a Modem Status Interrupt unless the interrupt has been disabled by clearing the U1IER[3] bit in the U1IER register. In auto-cts mode a transition on the CTS1 bit will trigger an interrupt only if both the U1IER[3] and U1IER[7] bits are set.	0
		0	Disable the CTS interrupt.	
		1	Enable the CTS interrupt.	
8	ABEOIE		Enables the end of auto-baud interrupt.	0
		0	Disable end of auto-baud Interrupt.	
		1	Enable end of auto-baud Interrupt.	
9	ABTOIE		Enables the auto-baud time-out interrupt.	0
		0	Disable auto-baud time-out Interrupt.	
		1	Enable auto-baud time-out Interrupt.	
31:10	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

33.5.5 UART1 Interrupt Identification Register

The U1IIR provides a status code that denotes the priority and source of a pending interrupt. The interrupts are frozen during an U1IIR access. If an interrupt occurs during an U1IIR access, the interrupt is recorded for the next U1IIR access.

Table 695: UART1 Interrupt Identification Register (IIR - address 0x4008 2008) bit description

Bit	Symbol	Value	Description	Reset value
0	INTSTATUS		Interrupt status. Note that U1IIR[0] is active low. The pending interrupt can be determined by evaluating U1IIR[3:1].	1
		0	At least one interrupt is pending.	
		1	No interrupt is pending.	
3:1	INTID		Interrupt identification. U1IER[3:1] identifies an interrupt corresponding to the UART1 Rx or TX FIFO. All other combinations of U1IER[3:1] not listed below are reserved (100,101,111).	0
		0x3	1 - Receive Line Status (RLS).	
		0x2	2a - Receive Data Available (RDA).	
		0x6	2b - Character Time-out Indicator (CTI).	
		0x1	3 - THRE Interrupt.	
		0x0	4 - Modem Interrupt.	
5:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
7:6	FIFOENABLE		Copies of U1FCR[0].	0

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Table 695: UART1 Interrupt Identification Register (IIR - address 0x4008 2008) bit description

Bit	Symbol	Value	Description	Reset value
8	ABEOINT		End of auto-baud interrupt. True if auto-baud has finished successfully and interrupt is enabled.	0
9	ABTOINT		Auto-baud time-out interrupt. True if auto-baud has timed out and interrupt is enabled.	0
31:10	-		Reserved, the value read from a reserved bit is not defined.	NA

Bit U1IIR[9:8] are set by the auto-baud function and signal a time-out or end of auto-baud condition. The auto-baud interrupt conditions are cleared by setting the corresponding Clear bits in the Auto-baud Control Register.

If the IntStatus bit is 1 no interrupt is pending and the IntId bits will be zero. If the IntStatus is 0, a non auto-baud interrupt is pending in which case the IntId bits identify the type of interrupt and handling as described in Table 696. Given the status of U1IIR[3:0], an interrupt handler routine can determine the cause of the interrupt and how to clear the active interrupt. The U1IIR must be read in order to clear the interrupt prior to exiting the Interrupt Service Routine.

The UART1 RLS interrupt (U1IIR[3:1] = 011) is the highest priority interrupt and is set whenever any one of four error conditions occur on the UART1RX input: overrun error (OE), parity error (PE), framing error (FE) and break interrupt (BI). The UART1 Rx error condition that set the interrupt can be observed via U1LSR[4:1]. The interrupt is cleared upon an U1LSR read.

The UART1 RDA interrupt (U1IIR[3:1] = 010) shares the second level priority with the CTI interrupt (U1IIR[3:1] = 110). The RDA is activated when the UART1 Rx FIFO reaches the trigger level defined in U1FCR7:6 and is reset when the UART1 Rx FIFO depth falls below the trigger level. When the RDA interrupt goes active, the CPU can read a block of data defined by the trigger level.

The CTI interrupt (U1IIR[3:1] = 110) is a second level interrupt and is set when the UART1 Rx FIFO contains at least one character and no UART1 Rx FIFO activity has occurred in 3.5 to 4.5 character times. Any UART1 Rx FIFO activity (read or write of UART1 RSR) will clear the interrupt. This interrupt is intended to flush the UART1 RBR after a message has been received that is not a multiple of the trigger level size. For example, if a peripheral wished to send a 105 character message and the trigger level was 10 characters, the CPU would receive 10 RDA interrupts resulting in the transfer of 100 characters and 1 to 5 CTI interrupts (depending on the service routine) resulting in the transfer of the remaining 5 characters.

Table 696: UART1 Interrupt Handling

U1IIR[3:0] value[1]	Priority	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	RX Line Status / Error	OE[2] or PE[2] or FE[2] or BI[2]	U1LSR Read[2]
0100	Second	RX Data Available	Rx data available or trigger level reached in FIFO (U1FCR0=1)	U1RBR Read[3] or UART1 FIFO drops below trigger level

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Table 696: UART1 Interrupt Handling

U1IIR[3:0] value[1]	Priority	Interrupt Type	Interrupt Source	Interrupt Reset
1100	Second	Character Time-out indication	Minimum of one character in the RX FIFO and no character input or removed during a time period depending on how many characters are in FIFO and what the trigger level is set at (3.5 to 4.5 character times). The exact time will be: [(word length) × 7 - 2] × 8 + [(trigger level - number of characters) × 8 + 1] RCLKs	U1RBR Read[3]
0010	Third	THRE	THRE[2]	U1IIR Read[4] (if source of interrupt) or THR write
0000	Fourth	Modem Status	CTS or DSR or RI or DCD	MSR Read

[1] Values "0000", “0011”, “0101”, “0111”, “1000”, “1001”, “1010”, “1011”,”1101”,”1110”,”1111” are reserved.

[2] For details see Section 33.5.10 “UART1 Line Status Register”

[3] For details see Section 33.5.1 “UART1 Receiver Buffer Register (when DLAB = 0)”

[4] For details see Section 33.5.5 “UART1 Interrupt Identification Register” and Section 33.5.2 “UART1 Transmitter Holding Register (when DLAB = 0)”

The UART1 THRE interrupt (U1IIR[3:1] = 001) is a third level interrupt and is activated when the UART1 THR FIFO is empty provided certain initialization conditions have been met. These initialization conditions are intended to give the UART1 THR FIFO a chance to fill up with data to eliminate many THRE interrupts from occurring at system start-up. The initialization conditions implement a one character delay minus the stop bit whenever THRE = 1 and there have not been at least two characters in the U1THR at one time since the last THRE = 1 event. This delay is provided to give the CPU time to write data to U1THR without a THRE interrupt to decode and service. A THRE interrupt is set immediately if the UART1 THR FIFO has held two or more characters at one time and currently, the U1THR is empty. The THRE interrupt is reset when a U1THR write occurs or a read of the U1IIR occurs and the THRE is the highest interrupt (U1IIR[3:1] = 001).

It is the lowest priority interrupt and is activated whenever there is any state change on modem inputs pins, DCD, DSR or CTS. In addition, a low to high transition on modem input RI will generate a modem interrupt. The source of the modem interrupt can be determined by examining U1MSR[3:0]. A U1MSR read will clear the modem interrupt.

33.5.6 UART1 FIFO Control Register

The write-only U1FCR controls the operation of the UART1 RX and TX FIFOs.

Table 697: UART1 FIFO Control Register (FCR - address 0x4008 2008) bit description

Bit	Symbol	Value	Description	Reset value
0	FIFOEN		FIFO enable.	0
		0	Must not be used in the application.	
		1	Active high enable for both UART1 Rx and TX FIFOs and U1FCR[7:1] access. This bit must be set for proper UART1 operation. Any transition on this bit will automatically clear the UART1 FIFOs.	

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Table 697: UART1 FIFO Control Register (FCR - address 0x4008 2008) bit description

Bit	Symbol	Value	Description	Reset value
1	RXFIFORES		RX FIFO Reset.	0
		0	No impact on either of UART1 FIFOs.	
		1	Writing a logic 1 to U1FCR[1] will clear all bytes in UART1 Rx FIFO, reset the pointer logic. This bit is self-clearing.	
2	TXFIFORES		TX FIFO Reset.	0
		0	No impact on either of UART1 FIFOs.	
		1	Writing a logic 1 to U1FCR[2] will clear all bytes in UART1 TX FIFO, reset the pointer logic. This bit is self-clearing.	
3	DMAMODE		DMA Mode Select. When the FIFO enable bit (bit 0 of this register) is set, this bit selects the DMA mode. See Section 33.5.6.1.	0
5:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
7:6	RXTRIGLVL		RX Trigger Level. These two bits determine how many receiver UART1 FIFO characters must be written before an interrupt is activated.	0
		0x0	Trigger level 0 (1 character or 0x01).	
		0x1	Trigger level 1 (4 characters or 0x04).	
		0x2	Trigger level 2 (8 characters or 0x08).	
		0x3	Trigger level 3 (14 characters or 0x0E).	
31:8	-		Reserved, user software should not write ones to reserved bits.	NA

33.5.6.1 DMA Operation

The user can optionally operate the UART transmit and/or receive using DMA. The DMA mode is determined by the DMA Mode Select bit in the FCR register. Note that for DMA operation as for any operation of the UART, the FIFOs must be enabled via the FIFO Enable bit in the FCR register.

UART receiver DMA

In DMA mode, the receiver DMA request is asserted on the event of the receiver FIFO level becoming equal to or greater than trigger level, or if a character time-out occurs. See the description of the RX Trigger Level above. The receiver DMA request is cleared by the DMA controller.

UART transmitter DMA

In DMA mode, the transmitter DMA request is asserted on the event of the transmitter FIFO transitioning to not full. The transmitter DMA request is cleared by the DMA controller.

33.5.7 UART1 Line Control Register

The U1LCR determines the format of the data character that is to be transmitted or received.

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Table 698: UART1 Line Control Register (LCR - address 0x4008 200C) bit description

Bit	Symbol	Value	Description	Reset value
1:0	WLS		Word Length Select.	0
		0x0	5-bit character length.	
		0x1	6-bit character length.	
		0x2	7-bit character length.	
		0x3	8-bit character length.	
2	SBS		Stop Bit Select.	0
		0	1 stop bit.	
		1	2 stop bits (1.5 if U1LCR[1:0]=00).	
3	PE		Parity Enable.	0
		0	Disable parity generation and checking.	
		1	Enable parity generation and checking.	
5:4	PS		Parity Select.	0
		00	Odd parity. Number of 1s in the transmitted character and the attached parity bit will be odd.	
		01	Even Parity. Number of 1s in the transmitted character and the attached parity bit will be even.	
		10	Forced "1" stick parity.	
		11	Forced "0" stick parity.	
6	BC		Break Control.	0
		0	Disable break transmission.	
		1	Enable break transmission. Output pin UART1 TXD is forced to logic 0 when U1LCR[6] is active high.	
7	DLAB		Divisor Latch Access Bit (DLAB)	0
		0	Disable access to Divisor Latches.	
		1	Enable access to Divisor Latches.	
31:8	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

33.5.8 UART1 Modem Control Register

The U1MCR enables the modem loopback mode and controls the modem output signals.

Table 699: UART1 Modem Control Register (MCR - address 0x4008 2010) bit description

Bit	Symbol	Value	Description	Reset value
0	DTRCTRL	-	DTR Control. Source for modem output pin, DTR. This bit reads as 0 when modem loopback mode is active.	0
1	RTSCTRL	-	RTSControl. Source for modem output pin RTS. This bit reads as 0 when modem loopback mode is active.	0
3:2	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0

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Table 699: UART1 Modem Control Register (MCR - address 0x4008 2010) bit description

Bit	Symbol	Value	Description	Reset value
4	LMS		Loopback Mode Select. The modem loopback mode provides a mechanism to perform diagnostic loopback testing. Serial data from the transmitter is connected internally to serial input of the receiver. Input pin, RXD1, has no effect on loopback and output pin, TXD1 is held in marking state. The 4 modem inputs (CTS, DSR, RI and DCD) are disconnected externally. Externally, the modem outputs (RTS, DTR) are set inactive. Internally, the 4 modem outputs are connected to the 4 modem inputs. As a result of these connections, the upper 4 bits of the U1MSR will be driven by the lower 4 bits of the U1MCR rather than the 4 modem inputs in normal mode. This permits modem status interrupts to be generated in loopback mode by writing the lower 4 bits of U1MCR.	0
		0	Disable modem loopback mode.	
		1	Enable modem loopback mode.	
5	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0
6	RTSEN		RTS enable.	0
		0	Disable auto-rts flow control.	
		1	Enable auto-rts flow control.	
7	CTSEN		CTS enable.	0
		0	Disable auto-cts flow control.	
		1	Enable auto-cts flow control.	
31:8	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

33.5.9 Auto-flow control

If auto-RTS mode is enabled the UART1‘s receiver FIFO hardware controls the RTS1 output of the UART1. If the auto-CTS mode is enabled the UART1‘s U1TSR hardware will only start transmitting if the CTS1 input signal is asserted.

33.5.9.1 Auto-RTS

The auto-RTS function is enabled by setting the RTSen bit. Auto-RTS data flow control originates in the U1RBR module and is linked to the programmed receiver FIFO trigger level. If auto-RTS is enabled, the data-flow is controlled as follows:

When the receiver FIFO level reaches the programmed trigger level, RTS1 is de-asserted (to a high value). It is possible that the sending UART sends an additional byte after the trigger level is reached (assuming the sending UART has another byte to send) because it might not recognize the de-assertion of RTS1 until after it has begun sending the additional byte. RTS1 is automatically reasserted (to a low value) once the receiver FIFO has reached the previous trigger level. The re-assertion of RTS1 signals to the sending UART to continue transmitting data.

If Auto-RTS mode is disabled, the RTSen bit controls the RTS1 output of the UART1. If Auto-RTS mode is enabled, hardware controls the RTS1 output, and the actual value of RTS1 will be copied in the RTS Control bit of the UART1. As long as Auto-RTS is enabled, the value of the RTS Control bit is read-only for software.

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Example: Suppose the UART1 operating in '550 mode has trigger level in U1FCR set to 0x2 then if Auto-RTS is enabled the UART1 will de-assert the RTS1 output as soon as the receive FIFO contains 8 bytes (Table 697 on page 751). The RTS1 output will be reasserted as soon as the receive FIFO hits the previous trigger level: 4 bytes.

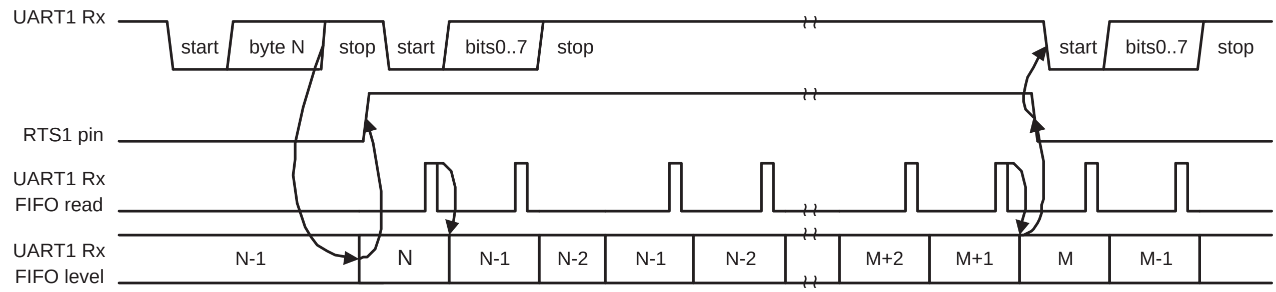


Fig 95. Auto-RTS Functional Timing

33.5.9.2 Auto-CTS

The Auto-CTS function is enabled by setting the CTSen bit. If Auto-CTS is enabled the transmitter circuitry in the U1TSR module checks CTS1 input before sending the next data byte. When CTS1 is active (low), the transmitter sends the next byte. To stop the transmitter from sending the following byte, CTS1 must be released before the middle of the last stop bit that is currently being sent. In Auto-CTS mode a change of the CTS1 signal does not trigger a modem status interrupt unless the CTS Interrupt Enable bit is set, Delta CTS bit in the U1MSR will be set though. Table 700 lists the conditions for generating a Modem Status interrupt.

Table 700: Modem status interrupt generation

Enable Modem Status Interrupt (U1ER[3])	CTSen (U1MCR[7])	CTS Interrupt Enable (U1IER[7])	Delta CTS (U1MSR[0])	Delta DCD or Trailing Edge RI or Delta DSR (U1MSR[3] or U1MSR[2] or U1MSR[1])	Modem Status Interrupt
0	x	x	x	x	No
1	0	x	0	0	No
1	0	x	1	x	Yes
1	0	x	x	1	Yes
1	1	0	x	0	No
1	1	0	x	1	Yes
1	1	1	0	0	No
1	1	1	1	x	Yes
1	1	1	x	1	Yes

The auto-CTS function reduces interrupts to the host system. When flow control is enabled, a CTS1 state change does not trigger host interrupts because the device automatically controls its own transmitter. Without Auto-CTS, the transmitter sends any data present in the transmit FIFO and a receiver overrun error can result. Figure 96 illustrates the Auto-CTS functional timing.

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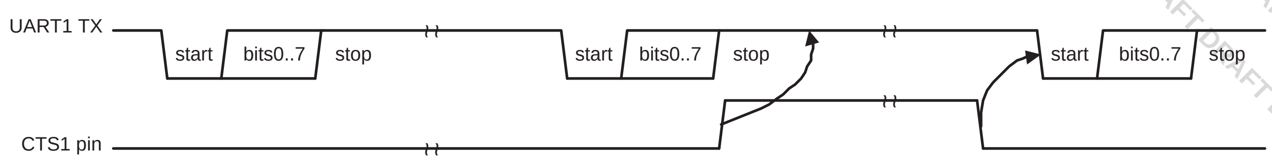


Fig 96. Auto-CTS Functional Timing

While starting transmission of the initial character the CTS1 signal is asserted. Transmission will stall as soon as the pending transmission has completed. The UART will continue transmitting a 1 bit as long as CTS1 is de-asserted (high). As soon as CTS1 gets de-asserted transmission resumes and a start bit is sent followed by the data bits of the next character.

33.5.10 UART1 Line Status Register

The U1LSR is a read-only register that provides status information on the UART1 TX and RX blocks.

Table 701: UART1 Line Status Register (LSR - address 0x4008 2014) bit description

Bit	Symbol	Value	Description	Reset value
0	RDR		Receiver Data Ready. U1LSR[0] is set when the U1RBR holds an unread character and is cleared when the UART1 RBR FIFO is empty.	0
		0	The UART1 receiver FIFO is empty.	
		1	The UART1 receiver FIFO is not empty.	
1	OE		Overrun Error. The overrun error condition is set as soon as it occurs. An U1LSR read clears U1LSR[1]. U1LSR[1] is set when UART1 RSR has a new character assembled and the UART1 RBR FIFO is full. In this case, the UART1 RBR FIFO will not be overwritten and the character in the UART1 RSR will be lost.	0
		0	Overrun error status is inactive.	
		1	Overrun error status is active.	
2	PE		Parity Error. When the parity bit of a received character is in the wrong state, a parity error occurs. An U1LSR read clears U1LSR[2]. Time of parity error detection is dependent on U1FCR[0]. **Note:** A parity error is associated with the character at the top of the UART1 RBR FIFO.	0
		0	Parity error status is inactive.	
		1	Parity error status is active.	

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Table 701: UART1 Line Status Register (LSR - address 0x4008 2014) bit description

Bit	Symbol	Value	Description	Reset value
3	FE		Framing Error. When the stop bit of a received character is a logic 0, a framing error occurs. An U1LSR read clears U1LSR[3]. The time of the framing error detection is dependent on U1FCR0. Upon detection of a framing error, the RX will attempt to resynchronize to the data and assume that the bad stop bit is actually an early start bit. However, it cannot be assumed that the next received byte will be correct even if there is no Framing Error. **Note:** A framing error is associated with the character at the top of the UART1 RBR FIFO.	0
		0	Framing error status is inactive.	
		1	Framing error status is active.	
4	BI		Break Interrupt. When RXD1 is held in the spacing state (all zeroes) for one full character transmission (start, data, parity, stop), a break interrupt occurs. Once the break condition has been detected, the receiver goes idle until RXD1 goes to marking state (all ones). An U1LSR read clears this status bit. The time of break detection is dependent on U1FCR[0]. **Note:** The break interrupt is associated with the character at the top of the UART1 RBR FIFO.	0
		0	Break interrupt status is inactive.	
		1	Break interrupt status is active.	
5	THRE		Transmitter Holding Register Empty. THRE is set immediately upon detection of an empty UART1 THR and is cleared on a U1THR write.	1
		0	U1THR contains valid data.	
		1	U1THR is empty.	
6	TEMT		Transmitter Empty. TEMT is set when both U1THR and U1TSR are empty; TEMT is cleared when either the U1TSR or the U1THR contain valid data.	1
		0	U1THR and/or the U1TSR contains valid data.	
		1	U1THR and the U1TSR are empty.	
7	RXFE		Error in RX FIFO. U1LSR[7] is set when a character with a RX error such as framing error, parity error or break interrupt, is loaded into the U1RBR. This bit is cleared when the U1LSR register is read and there are no subsequent errors in the UART1 FIFO.	0
		0	U1RBR contains no UART1 RX errors or U1FCR[0]=0.	
		1	UART1 RBR contains at least one UART1 RX error.	
31:8	-		Reserved, the value read from a reserved bit is not defined.	NA

33.5.11 UART1 Modem Status Register

The U1MSR is a read-only register that provides status information on the modem input signals. U1MSR[3:0] is cleared on U1MSR read. Note that modem signals have no direct effect on UART1 operation, they facilitate software implementation of modem signal operations.

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Table 702: UART1 Modem Status Register (MSR - address 0x4008 2018) bit description

Bit	Symbol	Value	Description	Reset value
0	DCTS		Delta CTS. Set upon state change of input CTS. Cleared on an U1MSR read.	0
		0	No change detected on modem input, CTS.	
		1	State change detected on modem input, CTS.	
1	DDSR		Delta DSR. Set upon state change of input DSR. Cleared on an U1MSR read.	0
		0	No change detected on modem input, DSR.	
		1	State change detected on modem input, DSR.	
2	TERI		Trailing Edge RI. Set upon low to high transition of input RI. Cleared on an U1MSR read.	0
		0	No change detected on modem input, RI.	
		1	Low-to-high transition detected on RI.	
3	DDCD		Delta DCD. Set upon state change of input DCD. Cleared on an U1MSR read.	0
		0	No change detected on modem input, DCD.	
		1	State change detected on modem input, DCD.	
4	CTS	-	Clear To Send State. Complement of input signal CTS. This bit is connected to U1MCR[1] in modem loopback mode.	0
5	DSR	-	Data Set Ready State. Complement of input signal DSR. This bit is connected to U1MCR[0] in modem loopback mode.	0
6	RI	-	Ring Indicator State. Complement of input RI. This bit is connected to U1MCR[2] in modem loopback mode.	0
7	DCD	-	Data Carrier Detect State. Complement of input DCD. This bit is connected to U1MCR[3] in modem loopback mode.	0
31:8	-	-	Reserved, the value read from a reserved bit is not defined.	NA

33.5.12 UART1 Scratch Pad Register

The U1SCR has no effect on the UART1 operation. This register can be written and/or read at user's discretion. There is no provision in the interrupt interface that would indicate to the host that a read or write of the U1SCR has occurred.

Table 703: UART1 Scratch Pad Register (SCR - address 0x4008 2014) bit description

Bit	Symbol	Description	Reset value
7:0	Pad	Scratch pad. A readable, writable byte.	0x00
31:8	-	Reserved, the value read from a reserved bit is not defined.	NA

33.5.13 UART1 Auto-baud Control Register

The UART1 Auto-baud Control Register (U1ACR) controls the process of measuring the incoming clock/data rate for the baud rate generation and can be read and written at user's discretion.

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Table 704: Autobaud Control Register (ACR - address 0x4008 2020) bit description

Bit	Symbol	Value	Description	Reset value
0	START		Auto-baud start bit. This bit is automatically cleared after auto-baud completion.	0
		0	Auto-baud stop (auto-baud is not running).	
		1	Auto-baud start (auto-baud is running). Auto-baud run bit. This bit is automatically cleared after auto-baud completion.	
1	MODE		Auto-baud mode select bit.	0
		0	Mode 0.	
		1	Mode 1.	
2	AUTORESTART		Auto-baud restart bit.	0
		0	No restart	
		1	Restart in case of time-out (counter restarts at next UART1 Rx falling edge)	
7:3	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0
8	ABEOINTCLR		End of auto-baud interrupt clear bit (write-only).	0
		0	Writing a 0 has no impact.	
		1	Writing a 1 will clear the corresponding interrupt in the U1IIR.	
9	ABTOINTCLR		Auto-baud time-out interrupt clear bit (write-only).	0
		0	Writing a 0 has no impact.	
		1	Writing a 1 will clear the corresponding interrupt in the U1IIR.	
31:10	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0

33.5.14 Auto-baud

The UART1 auto-baud function can be used to measure the incoming baud-rate based on the “AT” protocol (Hayes command). If enabled the auto-baud feature will measure the bit time of the receive data stream and set the divisor latch registers U1DLM and U1DLL accordingly.

Remark: the fractional rate divider is not connected during auto-baud operations, and therefore should not be used when the auto-baud feature is needed.

Auto-baud is started by setting the U1ACR Start bit. Auto-baud can be stopped by clearing the U1ACR Start bit. The Start bit will clear once auto-baud has finished and reading the bit will return the status of auto-baud (pending/finished).

Two auto-baud measuring modes are available which can be selected by the U1ACR Mode bit. In mode 0 the baud-rate is measured on two subsequent falling edges of the UART1 Rx pin (the falling edge of the start bit and the falling edge of the least significant bit). In mode 1 the baud-rate is measured between the falling edge and the subsequent rising edge of the UART1 Rx pin (the length of the start bit).

The U1ACR AutoRestart bit can be used to automatically restart baud-rate measurement if a time-out occurs (the rate measurement counter overflows). If this bit is set the rate measurement will restart at the next falling edge of the UART1 Rx pin.

The auto-baud function can generate two interrupts.

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- The U1IIR ABTOInt interrupt will get set if the interrupt is enabled (U1IER ABToIntEn is set and the auto-baud rate measurement counter overflows).
- The U1IIR ABEOInt interrupt will get set if the interrupt is enabled (U1IER ABEOIntEn is set and the auto-baud has completed successfully).

The auto-baud interrupts have to be cleared by setting the corresponding U1ACR ABTOIntClr and ABEOIntEn bits.

Typically the fractional baud-rate generator is disabled (DIVADDVAL = 0) during auto-baud. However, if the fractional baud-rate generator is enabled (DIVADDVAL > 0), it is going to impact the measuring of UART1 Rx pin baud-rate, but the value of the U1FDR register is not going to be modified after rate measurement. Also, when auto-baud is used, any write to U1DLM and U1DLL registers should be done before U1ACR register write. The minimum and the maximum baud rates supported by UART1 are function of pclk, number of data bits, stop bits and parity bits.

$$ratemin = \frac{2 \times PCLK}{16 \times 2^{15}} \leq UART1_{baudrate} \leq \frac{PCLK}{16 \times (2 + databits + paritybits + stopbits)} = ratemax \quad (8)$$

33.5.15 Auto-baud modes

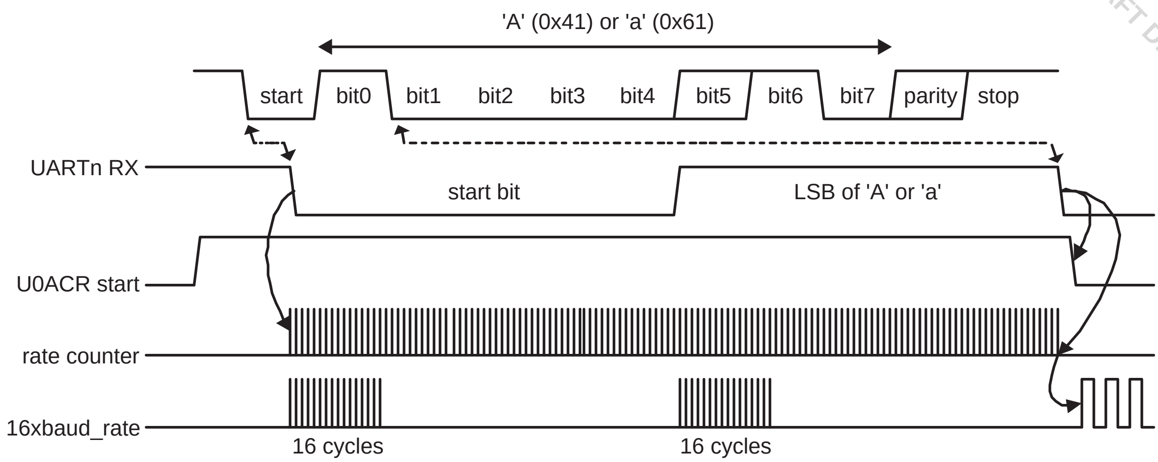
When the software is expecting an “AT” command, it configures the UART1 with the expected character format and sets the U1ACR Start bit. The initial values in the divisor latches U1DLM and U1DLM don‘t care. Because of the “A” or “a” ASCII coding (”A" = 0x41, “a” = 0x61), the UART1 Rx pin sensed start bit and the LSB of the expected character are delimited by two falling edges. When the U1ACR Start bit is set, the auto-baud protocol will execute the following phases:

1. On U1ACR Start bit setting, the baud-rate measurement counter is reset and the UART1 U1RSR is reset. The U1RSR baud rate is switch to the highest rate.
2. A falling edge on UART1 Rx pin triggers the beginning of the start bit. The rate measuring counter will start counting pclk cycles optionally pre-scaled by the fractional baud-rate generator.
3. During the receipt of the start bit, 16 pulses are generated on the RSR baud input with the frequency of the (fractional baud-rate pre-scaled) UART1 input clock, guaranteeing the start bit is stored in the U1RSR.
4. During the receipt of the start bit (and the character LSB for mode = 0) the rate counter will continue incrementing with the pre-scaled UART1 input clock (pclk).
5. If Mode = 0 then the rate counter will stop on next falling edge of the UART1 Rx pin. If Mode = 1 then the rate counter will stop on the next rising edge of the UART1 Rx pin.
6. The rate counter is loaded into U1DLM/U1DLL and the baud-rate will be switched to normal operation. After setting the U1DLM/U1DLL the end of auto-baud interrupt U1IIR ABEOInt will be set, if enabled. The U1RSR will now continue receiving the remaining bits of the “A/a” character.

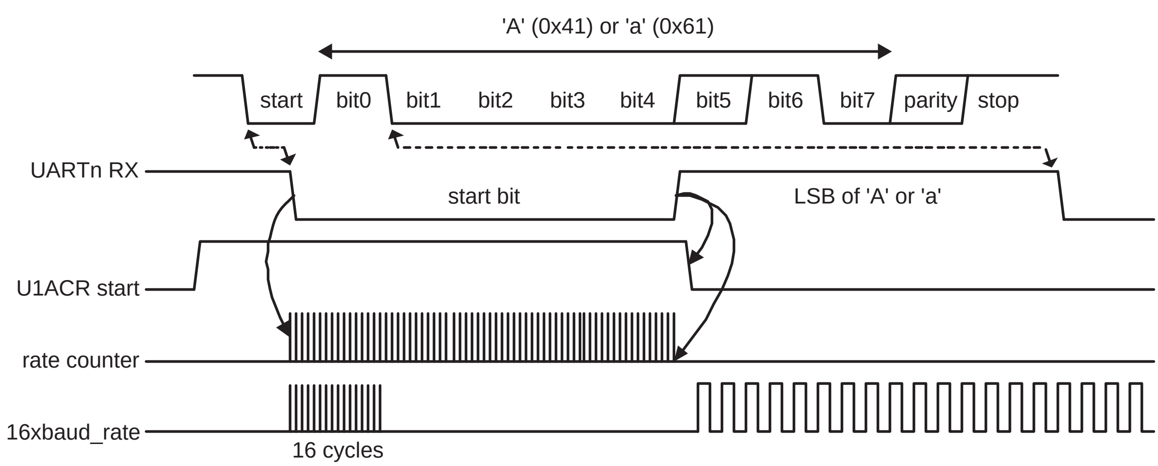
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a. Mode 0 (start bit and LSB are used for auto-baud)



b. Mode 1 (only start bit is used for auto-baud)

Fig 97. Auto-baud a) mode 0 and b) mode 1 waveform

33.5.16 UART1 Fractional Divider Register

The UART1 Fractional Divider Register (U1FDR) controls the clock pre-scaler for the baud rate generation and can be read and written at the user's discretion. This pre-scaler takes the APB clock and generates an output clock according to the specified fractional requirements.

Important: If the fractional divider is active (DIVADDVAL > 0) and DLM = 0, the value of the DLL register must be greater than 2.

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Table 705: UART1 Fractional Divider Register (FDR - address 0x4008 2028) bit description

Bit	Function	Description	Reset value
3:0	DIVADDVAL	Baud-rate generation pre-scaler divisor value. If this field is 0, fractional baud-rate generator will not impact the UARTn baudrate.	0
7:4	MULVAL	Baud-rate pre-scaler multiplier value. This field must be greater or equal 1 for UARTn to operate properly, regardless of whether the fractional baud-rate generator is used or not.	1
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0

This register controls the clock pre-scaler for the baud rate generation. The reset value of the register keeps the fractional capabilities of UART1 disabled making sure that UART1 is fully software and hardware compatible with UARTs not equipped with this feature.

UART1 baud rate can be calculated as (n = 1):

$$UART1_{baudrate} = \frac{PCLK}{16 \times (256 \times U1DLM + U1DLL) \times \left(1 + \frac{DivAddVal}{MulVal}\right)} \quad (9)$$

Where PCLK is the peripheral clock, U1DLM and U1DLL are the standard UART1 baud rate divider registers, and DIVADDVAL and MULVAL are UART1 fractional baud rate generator specific parameters.

The value of MULVAL and DIVADDVAL should comply to the following conditions:

1. 1 ≤ MULVAL ≤ 15
2. 0 ≤ DIVADDVAL ≤ 14
3. DIVADDVAL < MULVAL

The value of the U1FDR should not be modified while transmitting/receiving data or data may be lost or corrupted.

If the U1FDR register value does not comply to these two requests, then the fractional divider output is undefined. If DIVADDVAL is zero then the fractional divider is disabled, and the clock will not be divided.

33.5.16.1 Baud rate calculation

UART1 can operate with or without using the Fractional Divider. In real-life applications it is likely that the desired baud rate can be achieved using several different Fractional Divider settings. The following algorithm illustrates one way of finding a set of DLM, DLL, MULVAL, and DIVADDVAL values. Such set of parameters yields a baud rate with a relative error of less than 1.1% from the desired one.

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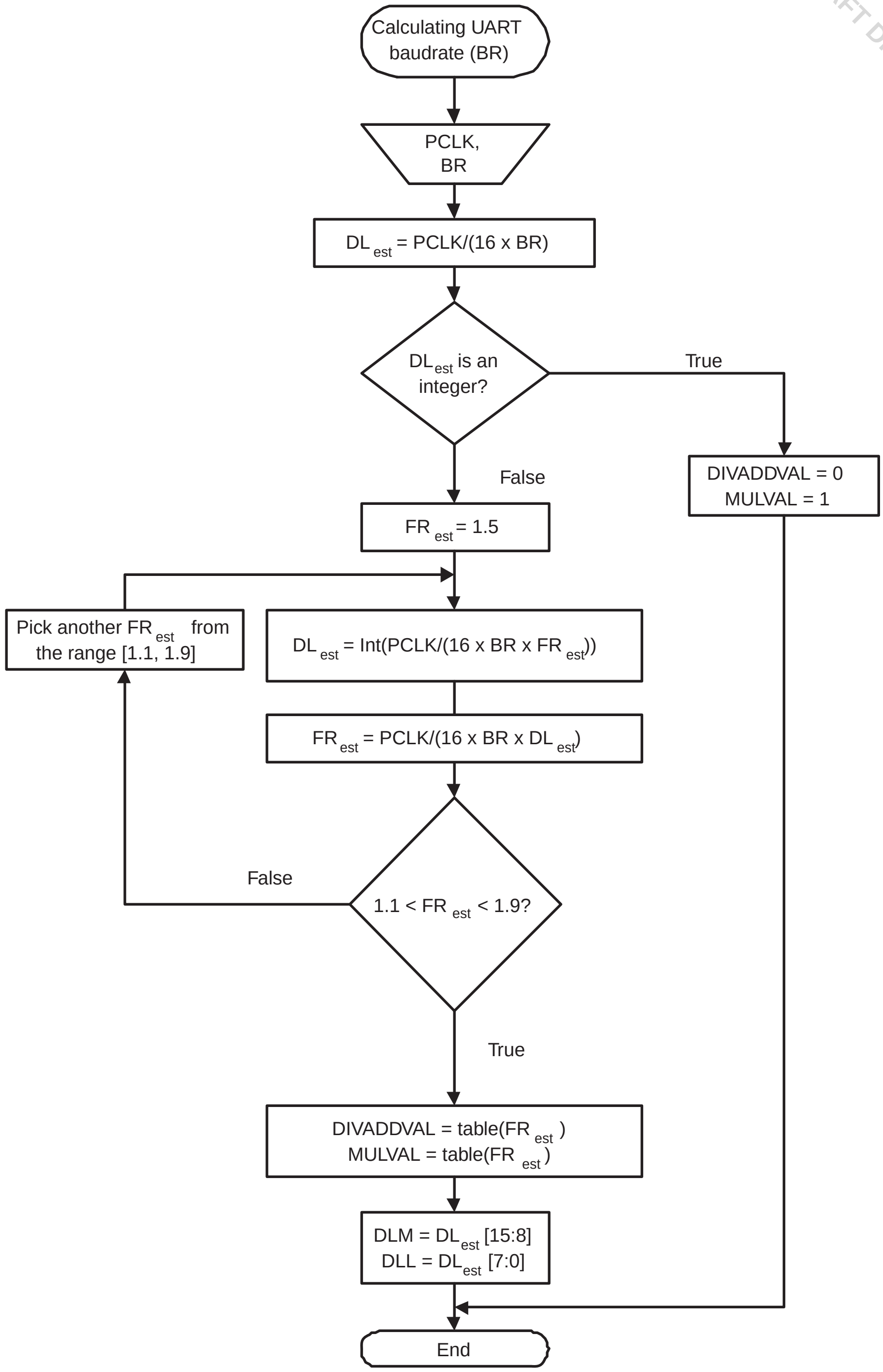


Fig 98. Algorithm for setting UART dividers

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Table 706. Fractional Divider setting look-up table

FR	DivAddVal/ MulVal	FR	DivAddVal/ MulVal	FR	DivAddVal/ MulVal	FR	DivAddVal/ MulVal
1.000	0/1	1.250	1/4	1.500	1/2	1.750	3/4
1.067	1/15	1.267	4/15	1.533	8/15	1.769	10/13
1.071	1/14	1.273	3/11	1.538	7/13	1.778	7/9
1.077	1/13	1.286	2/7	1.545	6/11	1.786	11/14
1.083	1/12	1.300	3/10	1.556	5/9	1.800	4/5
1.091	1/11	1.308	4/13	1.571	4/7	1.818	9/11
1.100	1/10	1.333	1/3	1.583	7/12	1.833	5/6
1.111	1/9	1.357	5/14	1.600	3/5	1.846	11/13
1.125	1/8	1.364	4/11	1.615	8/13	1.857	6/7
1.133	2/15	1.375	3/8	1.625	5/8	1.867	13/15
1.143	1/7	1.385	5/13	1.636	7/11	1.875	7/8
1.154	2/13	1.400	2/5	1.643	9/14	1.889	8/9
1.167	1/6	1.417	5/12	1.667	2/3	1.900	9/10
1.182	2/11	1.429	3/7	1.692	9/13	1.909	10/11
1.200	1/5	1.444	4/9	1.700	7/10	1.917	11/12
1.214	3/14	1.455	5/11	1.714	5/7	1.923	12/13
1.222	2/9	1.462	6/13	1.727	8/11	1.929	13/14
1.231	3/13	1.467	7/15	1.733	11/15	1.933	14/15

33.5.16.1.1 Example 1: PCLK = 14.7456 MHz, BR = 9600

According to the provided algorithm DL_{est} = PCLK/(16 x BR) = 14.7456 MHz / (16 x 9600) = 96. Since this DL_{est} is an integer number, DIVADDVAL = 0, MULVAL = 1, DLM = 0, and DLL = 96.

33.5.16.1.2 Example 2: PCLK = 12 MHz, BR = 115200

According to the provided algorithm DL_{est} = PCLK/(16 x BR) = 12 MHz / (16 x 115200) = 6.51. This DL_{est} is not an integer number and the next step is to estimate the FR parameter. Using an initial estimate of FR_{est} = 1.5 a new DL_{est} = 4 is calculated and FR_{est} is recalculated as FR_{est} = 1.628. Since FRest = 1.628 is within the specified range of 1.1 and 1.9, DIVADDVAL and MULVAL values can be obtained from the attached look-up table.

The closest value for FRest = 1.628 in the look-up Table 706 is FR = 1.625. It is equivalent to DIVADDVAL = 5 and MULVAL = 8.

Based on these findings, the suggested UART setup would be: DLM = 0, DLL = 4, DIVADDVAL = 5, and MULVAL = 8. According to Equation 9 the UART rate is 115384. This rate has a relative error of 0.16% from the originally specified 115200.

33.5.17 UART1 Transmit Enable Register

In addition to being equipped with full hardware flow control (auto-cts and auto-rts mechanisms described above), U1TER enables implementation of software flow control, too. When TxEn=1, UART1 transmitter will keep sending data as long as they are available. As soon as TxEn becomes 0, UART1 transmission will stop.

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Although Table 707 describes how to use TxEn bit in order to achieve hardware flow control, it is strongly suggested to let UART1 hardware implemented auto flow control features take care of this, and limit the scope of TxEn to software flow control.

U1TER enables implementation of software and hardware flow control. When TXEn=1, UART1 transmitter will keep sending data as long as they are available. As soon as TXEn becomes 0, UART1 transmission will stop.

Table 707 describes how to use TXEn bit in order to achieve software flow control.

Table 707: UART1 Transmit Enable Register (TER - address 0x4008 2030) bit description

Bit	Symbol	Description	Reset value
6:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
7	TXEN	Transmit enable bit. When this bit is 1, as it is after a Reset, data written to the THR is output on the TXD pin as soon as any preceding data has been sent. If this bit cleared to 0 while a character is being sent, the transmission of that character is completed, but no further characters are sent until this bit is set again. In other words, a 0 in this bit blocks the transfer of characters from the THR or TX FIFO into the transmit shift register. Software can clear this bit when it detects that the a hardware-handshaking TX-permit signal (CTS) has gone false, or with software handshaking, when it receives an XOFF character (DC3). Software can set this bit again when it detects that the TX-permit signal has gone true, or when it receives an XON (DC1) character.	1
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

33.5.18 UART1 RS485 Control register

The U1RS485CTRL register controls the configuration of the UART in RS-485/EIA-485 mode.

Table 708: UART1 RS485 Control register (RS485CTRL - address 0x4008 204C) bit description

Bit	Symbol	Value	Description	Reset value
0	NMMEN		Multidrop mode select.	0
		0	RS-485/EIA-485 Normal Multidrop Mode (NMM) is disabled.	
		1	RS-485/EIA-485 Normal Multidrop Mode (NMM) is enabled. In this mode, an address is detected when a received byte causes the UART to set the parity error and generate an interrupt.	
1	RXDIS		Receive enable.	0
		0	The receiver is enabled.	
		1	The receiver is disabled.	
2	AADEN		Auto Address Detect enable.	0
		0	Auto Address Detect (AAD) is disabled.	
		1	Auto Address Detect (AAD) is enabled.	
3	SEL		Direction control.	0
		0	If direction control is enabled (bit DCTRL = 1), pin $\overline{RTS}$ is used for direction control.	
		1	If direction control is enabled (bit DCTRL = 1), pin DTR is used for direction control.	

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Table 708: UART1 RS485 Control register (RS485CTRL - address 0x4008 204C) bit description

Bit	Symbol	Value	Description	Reset value
4	DCTRL		Direction control enable.	0
		0	Disable Auto Direction Control.	
		1	Enable Auto Direction Control.	
5	OINV		Polarity. This bit reverses the polarity of the direction control signal on the RTS (or DTR) pin.	0
		0	The direction control pin will be driven to logic ‘0’ when the transmitter has data to be sent. It will be driven to logic ‘1’ after the last bit of data has been transmitted.	
		1	The direction control pin will be driven to logic ‘1’ when the transmitter has data to be sent. It will be driven to logic ‘0’ after the last bit of data has been transmitted.	
31:6	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

33.5.19 UART1 RS-485 Address Match register

The U1RS485ADRMATCH register contains the address match value for RS-485/EIA-485 mode.

Table 709. UART1 RS485 Address Match register (RS485ADRMATCH - address 0x4008 2050) bit description

Bit	Symbol	Description	Reset value
7:0	ADRMATCH	Contains the address match value.	0x00
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

33.5.20 UART1 RS-485 Delay value register

The user may program the 8-bit RS485DLY register with a delay between the last stop bit leaving the TXFIFO and the de-assertion of $\overline{RTS}$ (or $\overline{DTR}$). This delay time is in periods of the baud clock. Any delay time from 0 to 255 bit times may be programmed.

Table 710. UART1 RS485 Delay value register (RS485DLY - address 0x4008 2054) bit description

Bit	Symbol	Description	Reset value
7:0	DLY	Contains the direction control (RTS or DTR) delay value. This register works in conjunction with an 8-bit counter.	0x00
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

33.5.21 RS-485/EIA-485 modes of operation

The RS-485/EIA-485 feature allows the UART to be configured as an addressable slave. The addressable slave is one of multiple slaves controlled by a single master.

The UART master transmitter will identify an address character by setting the parity (9th) bit to ‘1’. For data characters, the parity bit is set to ‘0’.

Each UART slave receiver can be assigned a unique address. The slave can be programmed to either manually or automatically reject data following an address which is not theirs.

RS-485/EIA-485 Normal Multidrop Mode (NMM)

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Setting the RS485CTRL bit 0 enables this mode. In this mode, an address is detected when a received byte causes the UART to set the parity error and generate an interrupt.

If the receiver is DISABLED (RS485CTRL bit 1 = ‘1’) any received data bytes will be ignored and will not be stored in the RXFIFO. When an address byte is detected (parity bit = ‘1’) it will be placed into the RXFIFO and an Rx Data Ready Interrupt will be generated. The processor can then read the address byte and decide whether or not to enable the receiver to accept the following data.

While the receiver is ENABLED (RS485CTRL bit 1 =’0’) all received bytes will be accepted and stored in the RXFIFO regardless of whether they are data or address. When an address character is received a parity error interrupt will be generated and the processor can decide whether or not to disable the receiver.

RS-485/EIA-485 Auto Address Detection (AAD) mode

When both RS485CTRL register bits 0 (9-bit mode enable) and 2 (AAD mode enable) are set, the UART is in auto address detect mode.

In this mode, the receiver will compare any address byte received (parity = ‘1’) to the 8-bit value programmed into the RS485ADRMATCH register.

If the receiver is DISABLED (RS485CTRL bit 1 = ‘1’) any received byte will be discarded if it is either a data byte OR an address byte which fails to match the RS485ADRMATCH value.

When a matching address character is detected it will be pushed onto the RXFIFO along with the parity bit, and the receiver will be automatically enabled (RS485CTRL bit 1 will be cleared by hardware). The receiver will also generate n Rx Data Ready Interrupt.

While the receiver is ENABLED (RS485CTRL bit 1 = ‘0’) all bytes received will be accepted and stored in the RXFIFO until an address byte which does not match the RS485ADRMATCH value is received. When this occurs, the receiver will be automatically disabled in hardware (RS485CTRL bit 1 will be set), The received non-matching address character will not be stored in the RXFIFO.

RS-485/EIA-485 Auto Direction Control

RS485/EIA-485 Mode includes the option of allowing the transmitter to automatically control the state of either the $\overline{\text{RTS}}$ pin or the $\overline{\text{DTR}}$ pin as a direction control output signal.

Setting RS485CTRL bit 4 = ‘1’ enables this feature.

Direction control, if enabled, will use the $\overline{\text{RTS}}$ pin when RS485CTRL bit 3 = ‘0’. It will use the $\overline{\text{DTR}}$ pin when RS485CTRL bit 3 = ‘1’.

When Auto Direction Control is enabled, the selected pin will be asserted (driven low) when the CPU writes data into the TXFIFO. The pin will be de-asserted (driven high) once the last bit of data has been transmitted. See bits 4 and 5 in the RS485CTRL register.

The RS485CTRL bit 4 takes precedence over all other mechanisms controlling $\overline{\text{RTS}}$ (or $\overline{\text{DTR}}$) with the exception of loopback mode.

RS485/EIA-485 driver delay time

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The driver delay time is the delay between the last stop bit leaving the TXFIFO and the de-assertion of RTS (or DTR). This delay time can be programmed in the 8-bit RS485DLY register. The delay time is in periods of the baud clock. Any delay time from 0 to 255 bit times may be programmed.

RS485/EIA-485 output inversion

The polarity of the direction control signal on the $\overline{RTS}$ (or $\overline{DTR}$) pins can be reversed by programming bit 5 in the U1RS485CTRL register. When this bit is set, the direction control pin will be driven to logic 1 when the transmitter has data waiting to be sent. The direction control pin will be driven to logic 0 after the last bit of data has been transmitted.

33.5.22 UART1 FIFO Level register

U1FIFOLVL register is a read-only register that allows software to read the current FIFO level status. Both the transmit and receive FIFO levels are present in this register.

Table 711. UART1 FIFO Level register (FIFOLVL - address 0x4008 2058) bit description

Bit	Symbol	Description	Reset value
3:0	RXFIFILVL	Reflects the current level of the UART1 receiver FIFO. 0 = empty, 0xF = FIFO full.	0x00
7:4	-	Reserved. The value read from a reserved bit is not defined.	NA
11:8	TXFIFOLVL	Reflects the current level of the UART1 transmitter FIFO. 0 = empty, 0xF = FIFO full.	0x00
31:12	-	Reserved, the value read from a reserved bit is not defined.	NA

33.6 Architecture

The architecture of the UART1 is shown below in the block diagram.

The APB interface provides a communications link between the CPU or host and the UART1.

The UART1 receiver block, U1RX, monitors the serial input line, RXD1, for valid input. The UART1 RX Shift Register (U1RSR) accepts valid characters via RXD1. After a valid character is assembled in the U1RSR, it is passed to the UART1 RX Buffer Register FIFO to await access by the CPU or host via the generic host interface.

The UART1 transmitter block, U1TX, accepts data written by the CPU or host and buffers the data in the UART1 TX Holding Register FIFO (U1THR). The UART1 TX Shift Register (U1TSR) reads the data stored in the U1THR and assembles the data to transmit via the serial output pin, TXD1.

The UART1 Baud Rate Generator block, U1BRG, generates the timing enables used by the UART1 TX block. The U1BRG clock input source is the APB clock (PCLK). The main clock is divided down per the divisor specified in the U1DLL and U1DLM registers. This divided down clock is a 16x oversample clock, NBAUDOUT.

The modem interface contains registers U1MCR and U1MSR. This interface is responsible for handshaking between a modem peripheral and the UART1.

The interrupt interface contains registers U1IER and U1IIR. The interrupt interface receives several one clock wide enables from the U1TX and U1RX blocks.

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Status information from the U1TX and U1RX is stored in the U1LSR. Control information for the U1TX and U1RX is stored in the U1LCR.

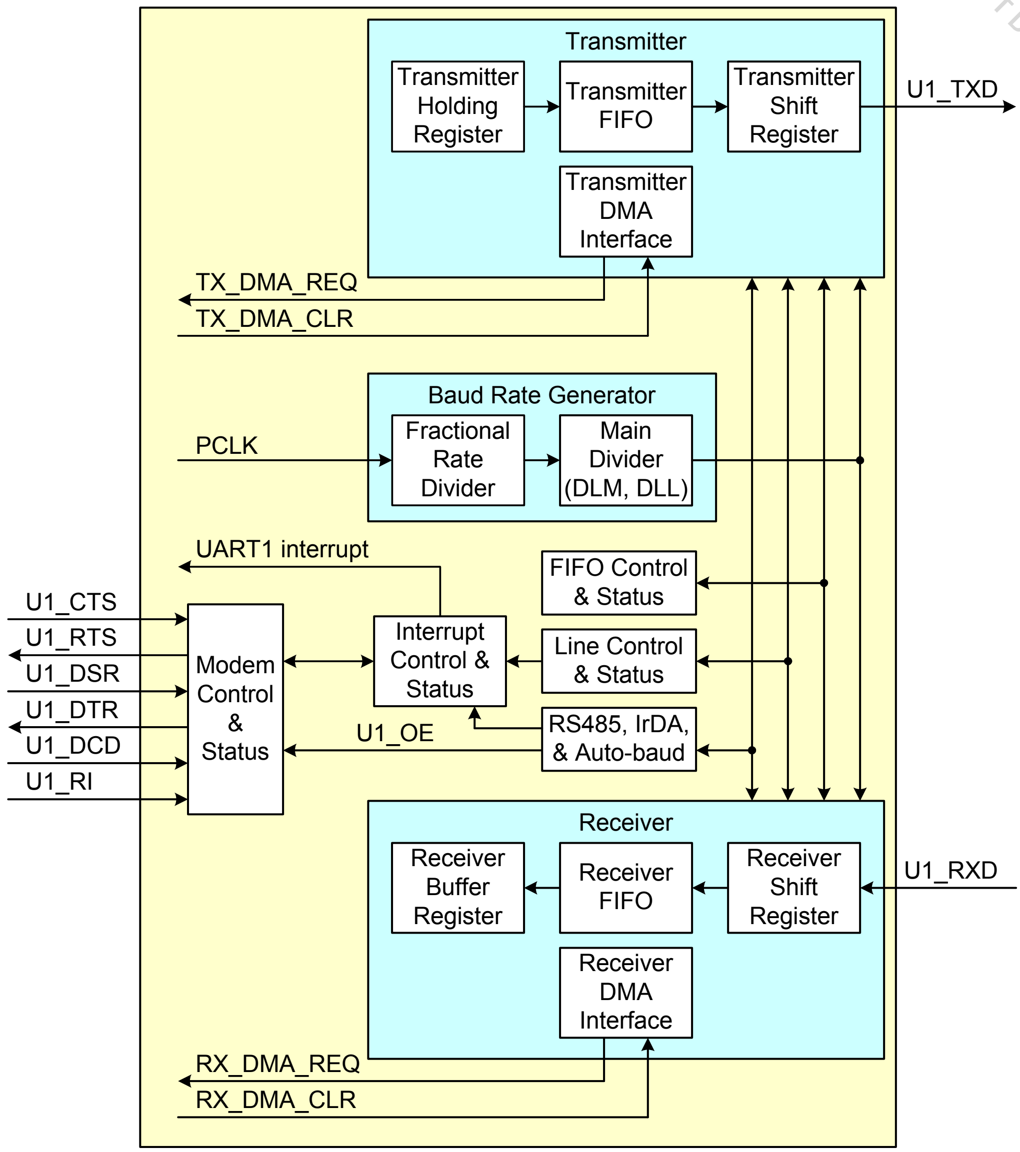


Fig 99. UART1 block diagram

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34.1 How to read this chapter

The SSP0/1 controllers are available on all LPC18xx parts.

34.2 Basic configuration

The SSP0/1 are configured as follows:

- See Table 712 for clocking and power control.
- The SSP0/1 are reset by the SSP0/1_RST (reset #50/51).
- The SSP0/1 interrupts are connected to slots # 22/23 in the NVIC.
- For connecting the SSP0/1 receive and transmit lines to the GPDMA, use the DMAMUX register in the CREG block (see Table 35) and enable the GPDMA channel in the DMA Channel Configuration registers (Section 16.6.20).

Table 712. SSP0/1 clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to SSP0 register interface	BASE_M3_CLK	CLK_M3_SSP0	150 MHz
SSP0 peripheral clock (PCLK)	BASE_SSP0_CLK	CLK_APB0_SSP0	150 MHz
Clock to SSP1 register interface	BASE_M3_CLK	CLK_M3_SSP1	150 MHz
SSP1 peripheral clock (PCLK)	BASE_SSP1_CLK	CLK_APB2_SSP1	150 MHz

34.3 Features

- Compatible with Motorola SPI, 4-wire TI SSI, and National Semiconductor Microwire buses.
- Synchronous Serial Communication.
- Supports master or slave operation.
- Eight-frame FIFOs for both transmit and receive.
- 4-bit to 16-bit frame.

34.4 General description

The SSP is a Synchronous Serial Port (SSP) controller capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of 4 to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice it is often the case that only one of these data flows carries meaningful data.

The LPC18xx has two Synchronous Serial Port controllers -- SSP0 and SSP1.

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34.5 Pin description

Table 713. SSP pin description

Pin Name	Direction	Interface pin name/function			Pin description
		SPI	SSI	Microwire	
SCK0/1	I/O	SCK	CLK	SK	**Serial Clock.** SCK/CLK/SK is a clock signal used to synchronize the transfer of data. It is driven by the master and received by the slave. When the SPI interface is used, the clock is programmable to be active-high or active-low, otherwise it is always active-high. SCK1 only switches during a data transfer. Any other time, the SSPn interface either holds it in its inactive state, or does not drive it (leaves it in high-impedance state).
SSEL0/1	I/O	SSEL	FS	CS	**Frame Sync/Slave Select.** When the SSPn interface is a bus master, it drives this signal to an active state before the start of serial data, and then releases it to an inactive state after the serial data has been sent. The active state of this signal can be high or low depending upon the selected bus and mode. When the SSPn is a bus slave, this signal qualifies the presence of data from the Master, according to the protocol in use. When there is just one bus master and one bus slave, the Frame Sync or Slave Select signal from the Master can be connected directly to the slave's corresponding input. When there is more than one slave on the bus, further qualification of their Frame Select/Slave Select inputs will typically be necessary to prevent more than one slave from responding to a transfer.
MISO0/1	I/O	MISO	DR(M) DX(S)	SI(M) SO(S)	**Master In Slave Out.** The MISO signal transfers serial data from the slave to the master. When the SSPn is a slave, serial data is output on this signal. When the SSPn is a master, it clocks in serial data from this signal. When the SSPn is a slave and is not selected by FS/SSEL, it does not drive this signal (leaves it in high-impedance state).
MOSI0/1	I/O	MOSI	DX(M) DR(S)	SO(M) SI(S)	**Master Out Slave In.** The MOSI signal transfers serial data from the master to the slave. When the SSPn is a master, it outputs serial data on this signal. When the SSPn is a slave, it clocks in serial data from this signal.

34.6 Register description

The register addresses of the SSP controllers are shown in Table 714 and Table 715.

Table 714. Register overview: SSP0 (base address 0x4008 3000)

Name	Access	Address offset	Description	Reset value[1]
CR0	R/W	0x000	Control Register 0. Selects the serial clock rate, bus type, and data size.	0
CR1	R/W	0x004	Control Register 1. Selects master/slave and other modes.	0
DR	R/W	0x008	Data Register. Writes fill the transmit FIFO, and reads empty the receive FIFO.	0
SR	RO	0x00C	Status Register	0x0000 0003
CPSR	R/W	0x010	Clock Prescale Register	0
IMSC	R/W	0x014	Interrupt Mask Set and Clear Register	0

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Table 714. Register overview: SSP0 (base address 0x4008 3000)

Name	Access	Address offset	Description	Reset value[1]
RIS	RO	0x018	Raw Interrupt Status Register	0x0000 0008
MIS	RO	0x01C	Masked Interrupt Status Register	0
ICR	WO	0x020	SSPICR Interrupt Clear Register	-
DMACR	R/W	0x024	SSP0 DMA control register	0

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

Table 715. Register overview: SSP1 (base address 0x400C 5000)

Name	Access	Address offset	Description	Reset value[1]
CR0	R/W	0x000	Control Register 0. Selects the serial clock rate, bus type, and data size.	0
CR1	R/W	0x004	Control Register 1. Selects master/slave and other modes.	0
DR	R/W	0x008	Data Register. Writes fill the transmit FIFO, and reads empty the receive FIFO.	0
SR	RO	0x00C	Status Register	0x0000 0003
CPSR	R/W	0x010	Clock Prescale Register	0
IMSC	R/W	0x014	Interrupt Mask Set and Clear Register	0
RIS	RO	0x018	Raw Interrupt Status Register	0x0000 0008
MIS	RO	0x01C	Masked Interrupt Status Register	0
ICR	R/W	0x020	SSPICR Interrupt Clear Register	-
DMACR	R/W	0x024	SSP1 DMA control register	0

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

34.6.1 SSPControl Register 0

This register controls the basic operation of the SSP controller.

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Table 716: SSP Control Register 0 (CR0 - address 0x4008 3000 (SSP0), 0x400C 5000 (SSP1)) bit description

Bit	Symbol	Value	Description	Reset value
3:0	DSS		Data Size Select. This field controls the number of bits transferred in each frame. Values 0000-0010 are not supported and should not be used.	0000
		0x3	4-bit transfer	
		0x4	5-bit transfer	
		0x5	6-bit transfer	
		0x6	7-bit transfer	
		0x7	8-bit transfer	
		0x8	9-bit transfer	
		0x9	10-bit transfer	
		0xA	11-bit transfer	
		0xB	12-bit transfer	
		0xC	13-bit transfer	
		0xD	14-bit transfer	
		0xE	15-bit transfer	
		0xF	16-bit transfer	
5:4	FRF		Frame Format.	00
		0x0	SPI	
		0x1	TI	
		0x2	Microwire	
		0x3	This combination is not supported and should not be used.	
6	CPOL		Clock Out Polarity. This bit is only used in SPI mode.	0
		0	SSP controller maintains the bus clock low between frames.	
		1	SSP controller maintains the bus clock high between frames.	
7	CPHA		Clock Out Phase. This bit is only used in SPI mode.	0
		0	SSP controller captures serial data on the first clock transition of the frame, that is, the transition **away from** the inter-frame state of the clock line.	
		1	SSP controller captures serial data on the second clock transition of the frame, that is, the transition **back to** the inter-frame state of the clock line.	
15:8	SCR		Serial Clock Rate. The number of prescaler-output clocks per bit on the bus, minus one. Given that CPSDVSR is the prescale divider, and the APB clock PCLK clocks the prescaler, the bit frequency is PCLK / (CPSDVSR × [SCR+1]).	0x00
31:16	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

34.6.2 SSP Control Register 1

This register controls certain aspects of the operation of the SSP controller.

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Table 717: SSP Control Register 1 (CR1 - address 0x4008 3004 (SSP0), 0x400C 5004 (SSP1)) bit description

Bit	Symbol	Value	Description	Reset value
0	LBM		Loop Back Mode.	0
		0	During normal operation.	
		1	Serial input is taken from the serial output (MOSI or MISO) rather than the serial input pin (MISO or MOSI respectively).	
1	SSE		SSP Enable.	0
		0	The SSP controller is disabled.	
		1	The SSP controller will interact with other devices on the serial bus. Software should write the appropriate control information to the other SSP registers and interrupt controller registers, before setting this bit.	
2	MS		Master/Slave Mode.This bit can only be written when the SSE bit is 0.	0
		0	The SSP controller acts as a master on the bus, driving the SCLK, MOSI, and SSEL lines and receiving the MISO line.	
		1	The SSP controller acts as a slave on the bus, driving MISO line and receiving SCLK, MOSI, and SSEL lines.	
3	SOD		Slave Output Disable. This bit is relevant only in slave mode (MS = 1). If it is 1, this blocks this SSP controller from driving the transmit data line (MISO).	0
31:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

34.6.3 SSP Data Register

Software can write data to be transmitted to this register, and read data that has been received.

Table 718: SSP Data Register (DR - address 0x4008 3008 (SSP0), 0x400C 5008 (SSP1)) bit description

Bit	Symbol	Description	Reset value
15:0	DATA	**Write:** software can write data to be sent in a future frame to this register whenever the TNF bit in the Status register is 1, indicating that the Tx FIFO is not full. If the Tx FIFO was previously empty and the SSP controller is not busy on the bus, transmission of the data will begin immediately. Otherwise the data written to this register will be sent as soon as all previous data has been sent (and received). If the data length is less than 16 bits, software must right-justify the data written to this register. **Read:** software can read data from this register whenever the RNE bit in the Status register is 1, indicating that the Rx FIFO is not empty. When software reads this register, the SSP controller returns data from the least recent frame in the Rx FIFO. If the data length is less than 16 bits, the data is right-justified in this field with higher order bits filled with 0s.	0x0000
31:16	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

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34.6.4 SSP Status Register

This read-only register reflects the current status of the SSP controller.

Table 719: SSP Status Register (SR - address 0x4008 300C (SSP0), 0x400C 500C (SSP1)) bit description

Bit	Symbol	Description	Reset value
0	TFE	Transmit FIFO Empty. This bit is 1 is the Transmit FIFO is empty, 0 if not.	1
1	TNF	Transmit FIFO Not Full. This bit is 0 if the Tx FIFO is full, 1 if not.	1
2	RNE	Receive FIFO Not Empty. This bit is 0 if the Receive FIFO is empty, 1 if not.	0
3	RFF	Receive FIFO Full. This bit is 1 if the Receive FIFO is full, 0 if not.	0
4	BSY	Busy. This bit is 0 if the SSPn controller is idle, or 1 if it is currently sending/receiving a frame and/or the Tx FIFO is not empty.	0
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

34.6.5 SSP Clock Prescale Register

This register controls the factor by which the Prescaler divides the SSP peripheral clock PCLK to yield the prescaler clock that is, in turn, divided by the SCR factor in SSPnCR0, to determine the bit clock.

Table 720: SSP Clock Prescale Register (CPSR - address 0x4008 3010 (SSP0), 0x400C 5010 (SSP1)) bit description

Bit	Symbol	Description	Reset value
7:0	CPSDVSR	This even value between 2 and 254, by which PCLK is divided to yield the prescaler output clock. Bit 0 always reads as 0.	0
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Important: the SSPnCPSR value must be properly initialized or the SSP controller will not be able to transmit data correctly.

In Slave mode, the SSP clock rate provided by the master must not exceed 1/12 of the SSP peripheral clock. The content of the SSPnCPSR register is not relevant.

In master mode, $CPSDVSR_{min}$ = 2 or larger (even numbers only).

34.6.6 SSP Interrupt Mask Set/Clear Register

This register controls whether each of the four possible interrupt conditions in the SSP controller are enabled. Note that ARM uses the word “masked” in the opposite sense from classic computer terminology, in which “masked” meant “disabled”. ARM uses the word “masked” to mean “enabled”. To avoid confusion we will not use the word “masked”.

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Table 721: SSP Interrupt Mask Set/Clear register (IMSC - address 0x4008 3014 (SSP0), 0x400C 5014 (SSP1)) bit description

Bit	Symbol	Description	Reset value
0	RORIM	Software should set this bit to enable interrupt when a Receive Overrun occurs, that is, when the Rx FIFO is full and another frame is completely received. The ARM spec implies that the preceding frame data is overwritten by the new frame data when this occurs.	0
1	RTIM	Software should set this bit to enable interrupt when a Receive Time-out condition occurs. A Receive Time-out occurs when the Rx FIFO is not empty, and no has not been read for a time-out period. The time-out period is the same for master and slave modes and is determined by the SSP bit rate: 32 bits at PCLK / (CPSDVSR × [SCR+1]).	0
2	RXIM	Software should set this bit to enable interrupt when the Rx FIFO is at least half full.	0
3	TXIM	Software should set this bit to enable interrupt when the Tx FIFO is at least half empty.	0
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

34.6.7 SSP Raw Interrupt Status Register

This read-only register contains a 1 for each interrupt condition that is asserted, regardless of whether or not the interrupt is enabled in the SSPnIMSC.

Table 722: SSP Raw Interrupt Status register (RIS - address 0x4008 3018 (SSP0), RIS - 0x400C 5018 (SSP1)) bit description

Bit	Symbol	Description	Reset value
0	RORRIS	This bit is 1 if another frame was completely received while the RxFIFO was full. The ARM spec implies that the preceding frame data is overwritten by the new frame data when this occurs.	0
1	RTRIS	This bit is 1 if the Rx FIFO is not empty, and has not been read for a time-out period. The time-out period is the same for master and slave modes and is determined by the SSP bit rate: 32 bits at PCLK / (CPSDVSR × [SCR+1]).	0
2	RXRIS	This bit is 1 if the Rx FIFO is at least half full.	0
3	TXRIS	This bit is 1 if the Tx FIFO is at least half empty.	1
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

34.6.8 SSP Masked Interrupt Status Register

This read-only register contains a 1 for each interrupt condition that is asserted and enabled in the SSPnIMSC. When an SSP interrupt occurs, the interrupt service routine should read this register to determine the cause(s) of the interrupt.

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Table 723: SSP Masked Interrupt Status register (MIS -address 0x4008 301C (SSP0), 0x400C 501C (SSP1)) bit description

Bit	Symbol	Description	Reset value
0	RORMIS	This bit is 1 if another frame was completely received while the RxFIFO was full, and this interrupt is enabled.	0
1	RTMIS	This bit is 1 if the Rx FIFO is not empty, has not been read for a time-out period, and this interrupt is enabled. The time-out period is the same for master and slave modes and is determined by the SSP bit rate: 32 bits at PCLK / (CPSDVSR $\times$ [SCR+1]).	0
2	RXMIS	This bit is 1 if the Rx FIFO is at least half full, and this interrupt is enabled.	0
3	TXMIS	This bit is 1 if the Tx FIFO is at least half empty, and this interrupt is enabled.	0
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

34.6.9 SSP Interrupt Clear Register

Software can write one or more one(s) to this write-only register, to clear the corresponding interrupt condition(s) in the SSP controller. Note that the other two interrupt conditions can be cleared by writing or reading the appropriate FIFO, or disabled by clearing the corresponding bit in SSPnIMSC.

Table 724: SSP interrupt Clear Register (ICR - address 0x4008 3020 (SSP0), ICR - 0x400C 5020 (SSP1)) bit description

Bit	Symbol	Description	Reset value
0	RORIC	Writing a 1 to this bit clears the “frame was received when RxFIFO was full” interrupt.	NA
1	RTIC	Writing a 1 to this bit clears the Rx FIFO was not empty and has not been read for a time-out period interrupt. The time-out period is the same for master and slave modes and is determined by the SSP bit rate: 32 bits at PCLK / (CPSDVSR $\times$ [SCR+1]).	NA
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

34.6.10 SSP DMA Control Register

The SSPnDMACR register is the DMA control register. It is a read/write register.

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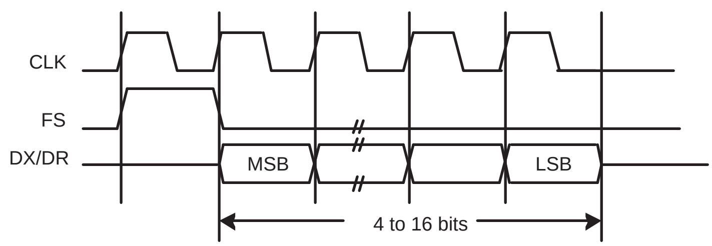
Table 725: SSP DMA Control Register (DMACR - address 0x4008 3024 (SSP0), 0x400C 5024 (SSP1)) bit description

Bit	Symbol	Description	Reset value
0	RXDMAE	Receive DMA Enable. When this bit is set to one 1, DMA for the receive FIFO is enabled, otherwise receive DMA is disabled.	0
1	TXDMAE	Transmit DMA Enable. When this bit is set to one 1, DMA for the transmit FIFO is enabled, otherwise transmit DMA is disabled	0
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

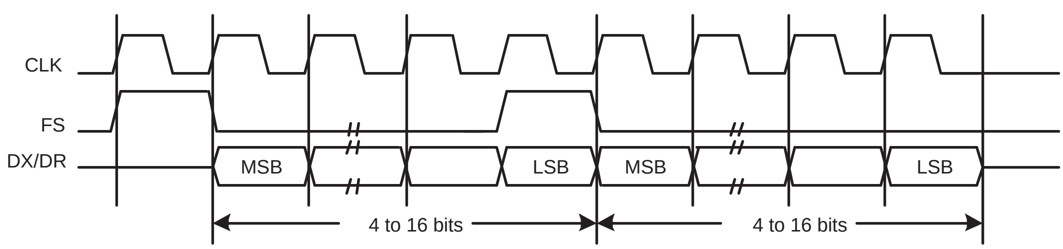
34.7 Functional description

34.7.1 Texas Instruments synchronous serial frame format

Figure 100 shows the 4-wire Texas Instruments synchronous serial frame format supported by the SSP module.



a. Single frame transfer



b. Continuous/back-to-back frames transfer

Fig 100. Texas Instruments Synchronous Serial Frame Format: a) Single and b) Continuous/back-to-back Two Frames Transfer

For device configured as a master in this mode, CLK and FS are forced LOW, and the transmit data line DX is tri-stated whenever the SSP is idle. Once the bottom entry of the transmit FIFO contains data, FS is pulsed HIGH for one CLK period. The value to be transmitted is also transferred from the transmit FIFO to the serial shift register of the transmit logic. On the next rising edge of CLK, the MSB of the 4-bit to 16-bit data frame is shifted out on the DX pin. Likewise, the MSB of the received data is shifted onto the DR pin by the off-chip serial slave device.

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Both the SSP and the off-chip serial slave device then clock each data bit into their serial shifter on the falling edge of each CLK. The received data is transferred from the serial shifter to the receive FIFO on the first rising edge of CLK after the LSB has been latched.

34.7.2 SPI frame format

The SPI interface is a four-wire interface where the SSEL signal behaves as a slave select. The main feature of the SPI format is that the inactive state and phase of the SCK signal are programmable through the CPOL and CPHA bits within the SSPCR0 control register.

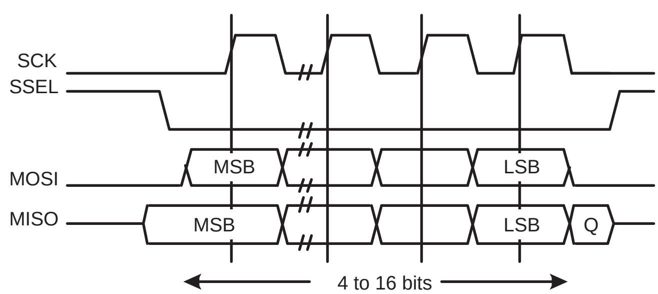
34.7.2.1 Clock Polarity (CPOL) and Phase (CPHA) control

When the CPOL clock polarity control bit is 0, it produces a steady state low value on the SCK pin. If the CPOL clock polarity control bit is 1, a steady state high value is placed on the CLK pin when data is not being transferred.

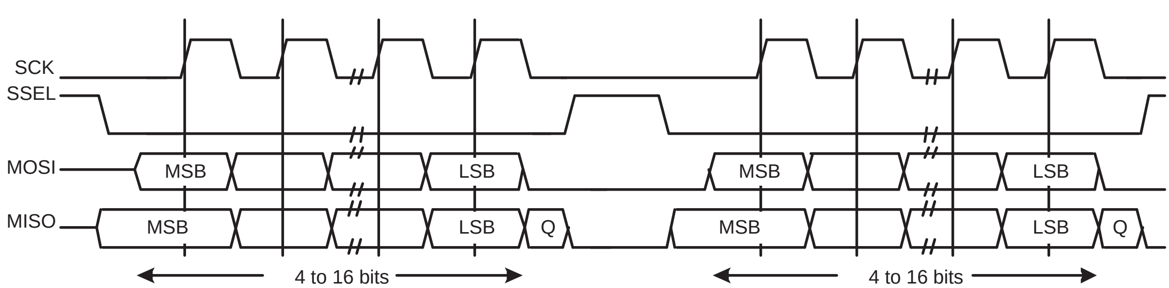
The CPHA control bit selects the clock edge that captures data and allows it to change state. It has the most impact on the first bit transmitted by either allowing or not allowing a clock transition before the first data capture edge. When the CPHA phase control bit is 0, data is captured on the first clock edge transition. If the CPHA clock phase control bit is 1, data is captured on the second clock edge transition.

34.7.2.2 SPI format with CPOL=0,CPHA=0

Single and continuous transmission signal sequences for SPI format with CPOL = 0, CPHA = 0 are shown in Figure 101.



a. Single transfer with CPOL=0 and CPHA=0



b. Continuous transfer with CPOL=0 and CPHA=0

Fig 101. SPI frame format with CPOL=0 and CPHA=0 (a) Single and b) Continuous Transfer)

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In this configuration, during idle periods:

- The CLK signal is forced LOW.
- SSEL is forced HIGH.
- The transmit MOSI/MISO pad is in high impedance.

If the SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSEL master signal being driven LOW. This causes slave data to be enabled onto the MISO input line of the master. Master's MOSI is enabled.

One half SCK period later, valid master data is transferred to the MOSI pin. Now that both the master and slave data have been set, the SCK master clock pin goes HIGH after one further half SCK period.

The data is now captured on the rising and propagated on the falling edges of the SCK signal.

In the case of a single word transmission, after all bits of the data word have been transferred, the SSEL line is returned to its idle HIGH state one SCK period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the SSEL signal must be pulsed HIGH between each data word transfer. This is because the slave select pin freezes the data in its serial peripheral register and does not allow it to be altered if the CPHA bit is logic zero. Therefore the master device must raise the SSEL pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the SSEL pin is returned to its idle state one SCK period after the last bit has been captured.

34.7.2.3 SPI format with CPOL=0,CPHA=1

The transfer signal sequence for SPI format with CPOL = 0, CPHA = 1 is shown in Figure 102, which covers both single and continuous transfers.

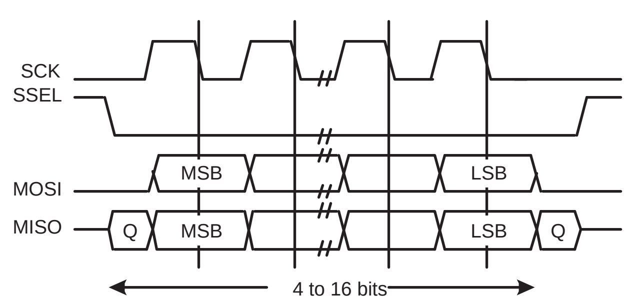


Fig 102. SPI frame format with CPOL=0 and CPHA=1

In this configuration, during idle periods:

- The CLK signal is forced LOW.
- SSEL is forced HIGH.
- The transmit MOSI/MISO pad is in high impedance.

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If the SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSEL master signal being driven LOW. Master's MOSI pin is enabled. After a further one half SCK period, both master and slave valid data is enabled onto their respective transmission lines. At the same time, the SCK is enabled with a rising edge transition.

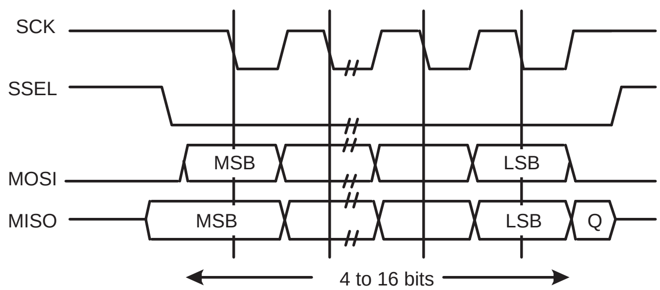
Data is then captured on the falling edges and propagated on the rising edges of the SCK signal.

In the case of a single word transfer, after all bits have been transferred, the SSEL line is returned to its idle HIGH state one SCK period after the last bit has been captured.

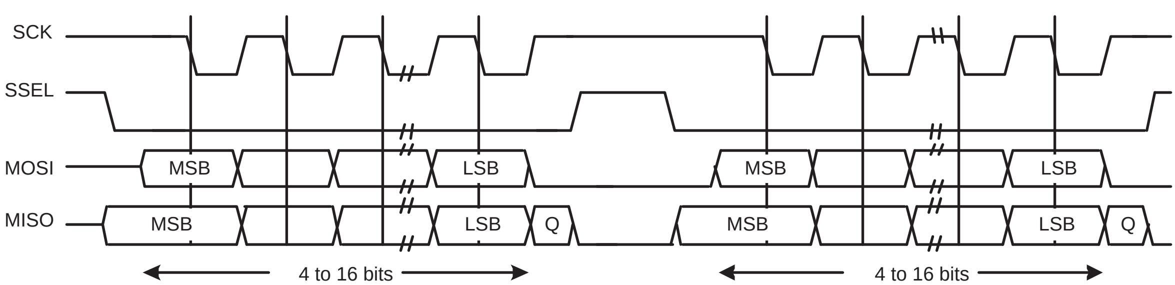
For continuous back-to-back transfers, the SSEL pin is held LOW between successive data words and termination is the same as that of the single word transfer.

34.7.2.4 SPI format with CPOL = 1,CPHA = 0

Single and continuous transmission signal sequences for SPI format with CPOL=1, CPHA=0 are shown in Figure 103.



a. Single transfer with CPOL=1 and CPHA=0



b. Continuous transfer with CPOL=1 and CPHA=0

Fig 103. SPI frame format with CPOL = 1 and CPHA = 0 (a) Single and b) Continuous Transfer)

In this configuration, during idle periods:

- The CLK signal is forced HIGH.
- SSEL is forced HIGH.
- The transmit MOSI/MISO pad is in high impedance.

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If the SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSEL master signal being driven LOW, which causes slave data to be immediately transferred onto the MISO line of the master. Master's MOSI pin is enabled.

One half period later, valid master data is transferred to the MOSI line. Now that both the master and slave data have been set, the SCK master clock pin becomes LOW after one further half SCK period. This means that data is captured on the falling edges and be propagated on the rising edges of the SCK signal.

In the case of a single word transmission, after all bits of the data word are transferred, the SSEL line is returned to its idle HIGH state one SCK period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the SSEL signal must be pulsed HIGH between each data word transfer. This is because the slave select pin freezes the data in its serial peripheral register and does not allow it to be altered if the CPHA bit is logic zero. Therefore the master device must raise the SSEL pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the SSEL pin is returned to its idle state one SCK period after the last bit has been captured.

34.7.2.5 SPI format with CPOL = 1,CPHA = 1

The transfer signal sequence for SPI format with CPOL = 1, CPHA = 1 is shown in Figure 104, which covers both single and continuous transfers.

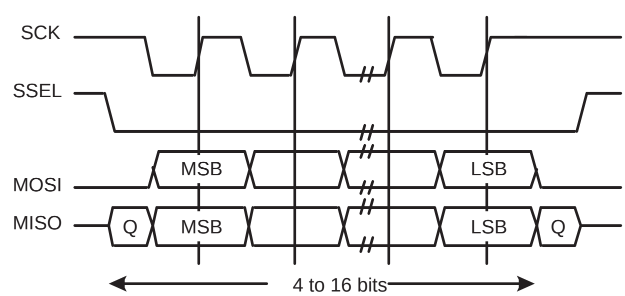


Fig 104. SPI Frame Format with CPOL = 1 and CPHA = 1

In this configuration, during idle periods:

- The CLK signal is forced HIGH.
- SSEL is forced HIGH.
- The transmit MOSI/MISO pad is in high impedance.

If the SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSEL master signal being driven LOW. Master's MOSI is enabled. After a further one half SCK period, both master and slave data are enabled onto their respective transmission lines. At the same time, the SCK is enabled with a falling edge transition. Data is then captured on the rising edges and propagated on the falling edges of the SCK signal.

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After all bits have been transferred, in the case of a single word transmission, the SSEL line is returned to its idle HIGH state one SCK period after the last bit has been captured. For continuous back-to-back transmissions, the SSEL pins remains in its active LOW state, until the final bit of the last word has been captured, and then returns to its idle state as described above. In general, for continuous back-to-back transfers the SSEL pin is held LOW between successive data words and termination is the same as that of the single word transfer.

34.7.3 National Semiconductor Microwire frame format

Figure 105 shows the Microwire frame format for a single frame. Figure 106 shows the same format when back-to-back frames are transmitted.

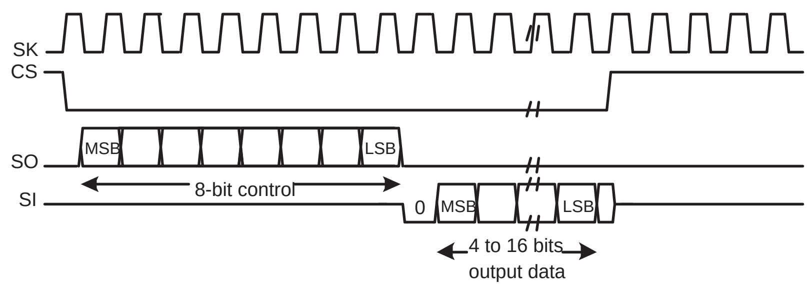


Fig 105. Microwire frame format (single transfer)

Microwire format is very similar to SPI format, except that transmission is half-duplex instead of full-duplex, using a master-slave message passing technique. Each serial transmission begins with an 8-bit control word that is transmitted from the SSP to the off-chip slave device. During this transmission, no incoming data is received by the SSP. After the message has been sent, the off-chip slave decodes it and, after waiting one serial clock after the last bit of the 8-bit control message has been sent, responds with the required data. The returned data is 4 to 16 bits in length, making the total frame length anywhere from 13 to 25 bits.

In this configuration, during idle periods:

- The SK signal is forced LOW.
- CS is forced HIGH.
- The transmit data line SO is arbitrarily forced LOW.

A transmission is triggered by writing a control byte to the transmit FIFO.The falling edge of CS causes the value contained in the bottom entry of the transmit FIFO to be transferred to the serial shift register of the transmit logic, and the MSB of the 8-bit control frame to be shifted out onto the SO pin. CS remains LOW for the duration of the frame transmission. The SI pin remains tristated during this transmission.

The off-chip serial slave device latches each control bit into its serial shifter on the rising edge of each SK. After the last bit is latched by the slave device, the control byte is decoded during a one clock wait-state, and the slave responds by transmitting data back to the SSP. Each bit is driven onto SI line on the falling edge of SK. The SSP in turn

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latches each bit on the rising edge of SK. At the end of the frame, for single transfers, the CS signal is pulled HIGH one clock period after the last bit has been latched in the receive serial shifter, that causes the data to be transferred to the receive FIFO.

Note: The off-chip slave device can tristate the receive line either on the falling edge of SK after the LSB has been latched by the receive shiftier, or when the CS pin goes HIGH.

For continuous transfers, data transmission begins and ends in the same manner as a single transfer. However, the CS line is continuously asserted (held LOW) and transmission of data occurs back to back. The control byte of the next frame follows directly after the LSB of the received data from the current frame. Each of the received values is transferred from the receive shifter on the falling edge SK, after the LSB of the frame has been latched into the SSP.

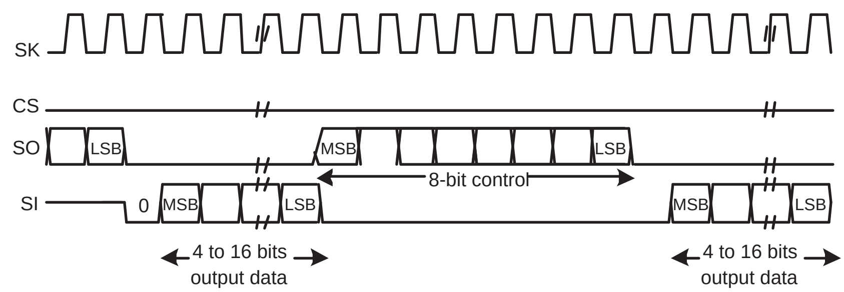


Fig 106. Microwire frame format (continuous transfers)

34.7.3.1 Setup and hold time requirements on CS with respect to SK in Microwire mode

In the Microwire mode, the SSP slave samples the first bit of receive data on the rising edge of SK after CS has gone LOW. Masters that drive a free-running SK must ensure that the CS signal has sufficient setup and hold margins with respect to the rising edge of SK.

Figure 107 illustrates these setup and hold time requirements. With respect to the SK rising edge on which the first bit of receive data is to be sampled by the SSP slave, CS must have a setup of at least two times the period of SK on which the SSP operates. With respect to the SK rising edge previous to this edge, CS must have a hold of at least one SK period.

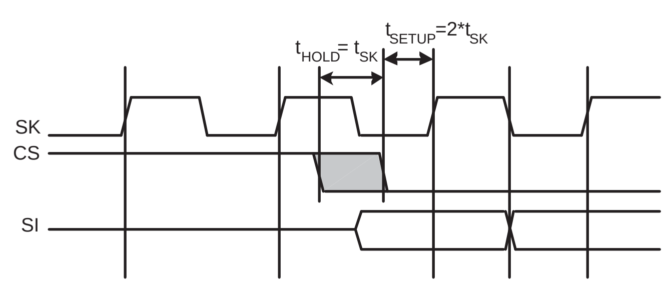


Fig 107. Microwire frame format setup and hold details

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35.1 How to read this chapter

This chapter applies to parts LPC1850/30/20/10 Rev 'A'.

The I^2S interface is available on all LPC18xx parts.

35.2 Basic configuration

The I^2S interface is configured as follows:

- See Table 726 for clocking and power control.
- The I2S0 is reset by the I2S0_RST (reset # 52).
- The I2S1 is reset by the I2S1_RST (reset # 53).
- The I2S0 interrupt is connected to slot # 28 in the NVIC.
- The I2S1 interrupt is connected to slot # 29 in the NVIC.
- For connecting the I2S receive and transmit lines to the GPDMA, use the DMAMUX register in the CREG block (see Table 35) and enable the GPDMA channel in the DMA Channel Configuration registers (Section 16.6.20).
- See Table 37 for interconnections between the I2S transmit/receive lines and the timer and SCT inputs.

Table 726. I2S clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to the I2S0 and I2S1 register interface and I2S0/1 peripheral clock.	BASE_APB1_CLK	CLK_APB1_I2S	150 MHz

35.3 Features

The I2S bus provides a standard communication interface for digital audio applications.

The I2S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select signal. The basic I2S connection has one master, which is always the master, and one slave. The I2S interface provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

- The I2S input can operate in both master and slave mode.

  The I2S output can operate in both master and slave mode, independent of the I2S input.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- Versatile clocking includes independent transmit and receive fractional rate generators, and an ability to use a single clock input or output for a 4-wire mode.

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- The sampling frequency (fs) can range (in practice) from 16 to 192 kHz (16, 22.05, 32, 44.1, 48, 96, or 192 kHz) for audio applications.
- Separate Master Clock outputs for both transmit and receive channels support a clock up to 512 times the I^2S sampling frequency.
- Word Select period in master mode is configurable (separately for I^2S input and I^2S output).
- Two 8 word (32 byte) FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the General Purpose DMA block.
- Controls include reset, stop and mute options separately for I2S input and I2S output.

35.4 General description

The I2S performs serial data out via the transmit channel and serial data in via the receive channel. These support the NXP Inter IC Audio format for 8-bit, 16-bit and 32-bit audio data, both for stereo and mono modes. Configuration, data access and control is performed by a APB register set. Data streams are buffered by FIFOs with a depth of 8 words.

The I2S receive and transmit stage can operate independently in either slave or master mode. Within the I2S module the difference between these modes lies in the word select (WS) signal which determines the timing of data transmissions. Data words start on the next falling edge of the transmitting clock after a WS change. In stereo mode when WS is low left data is transmitted and right data when WS is high. In mono mode the same data is transmitted twice, once when WS is low and again when WS is high.

- In master mode, word select is generated internally with a 9-bit counter. The half period count value of this counter can be set in the control register.
- In slave mode, word select is input from the relevant bus pin.
- When an I2S bus is active, the word select, receive clock and transmit clock signals are sent continuously by the bus master, while data is sent continuously by the transmitter.
- Disabling the I2S can be done with the stop or mute control bits separately for the transmit and receive.
- The stop bit will disable accesses by the transmit channel or the receive channel to the FIFOs and will place the transmit channel in mute mode.
- The mute control bit will place the transmit channel in mute mode. In mute mode, the transmit channel FIFO operates normally, but the output is discarded and replaced by zeroes. This bit does not affect the receive channel, data reception can occur normally.

35.4.1 I2S connection schemes

I2S1 is automatically a slave to I2S0 if no external pins are selected for the I2S1 clock and data lines.

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The MCLK can be provided by a master or used by the master to create the I2S CLK. MCLK can also be generated internally by the audio PLL through the CREG block (see Table 37).

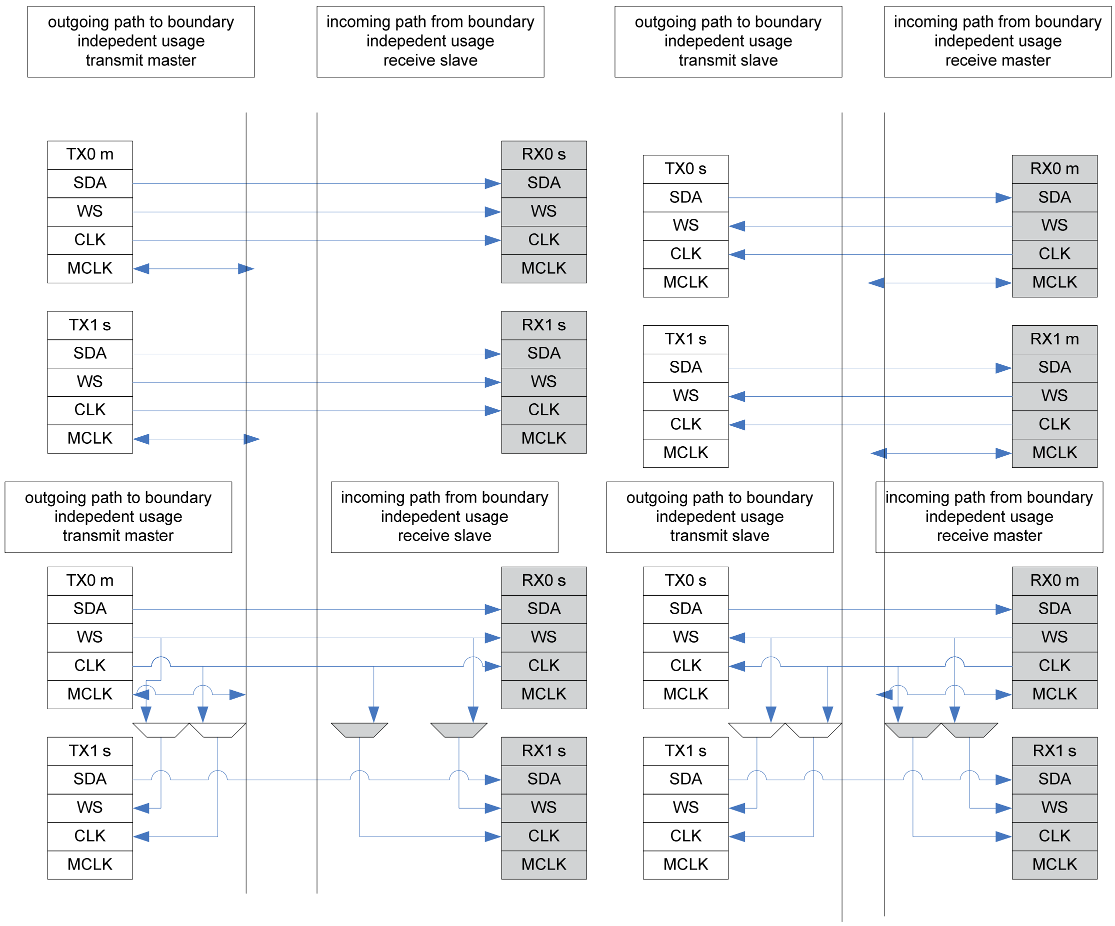


Fig 108. I2S connections

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35.5 Pin description

Table 727. Pin description

Pin name	Direction	Description
I2S0/1_RX_SCK	Input/ Output	Receive Clock. A clock signal used to synchronize the transfer of data on the receive channel. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I2S bus specification.
I2S0/1_RX_WS	Input/ Output	Receive Word Select. Selects the channel from which data is to be received. It is driven by the master and received by the slave. Corresponds to the signal WS in the I2S bus specification. WS = 0 indicates that data is being received by channel 1 (left channel). WS = 1 indicates that data is being received by channel 2 (right channel).
I2S0/1_RX_SDA	Input/ Output	Receive Data. Serial data, received MSB first. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the I2S bus specification.
I2S0/1_RX_MCLK	Output	Optional master clock output for the I2S receive function.
I2S0/1_TX_SCK	Input/ Output	Transmit Clock. A clock signal used to synchronize the transfer of data on the transmit channel. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I2S bus specification.
I2S0/1_TX_WS	Input/ Output	Transmit Word Select. Selects the channel to which data is being sent. It is driven by the master and received by the slave. Corresponds to the signal WS in the I2S bus specification. WS = 0 indicates that data is being sent to channel 1 (left channel). WS = 1 indicates that data is being sent to channel 2 (right channel).
I2S0/1_TX_SDA	Input/ Output	Transmit Data. Serial data, sent MSB first. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the I2S bus specification.
IS0/1_TX_MCLK	Output	Optional master clock output for the I2S transmit function.

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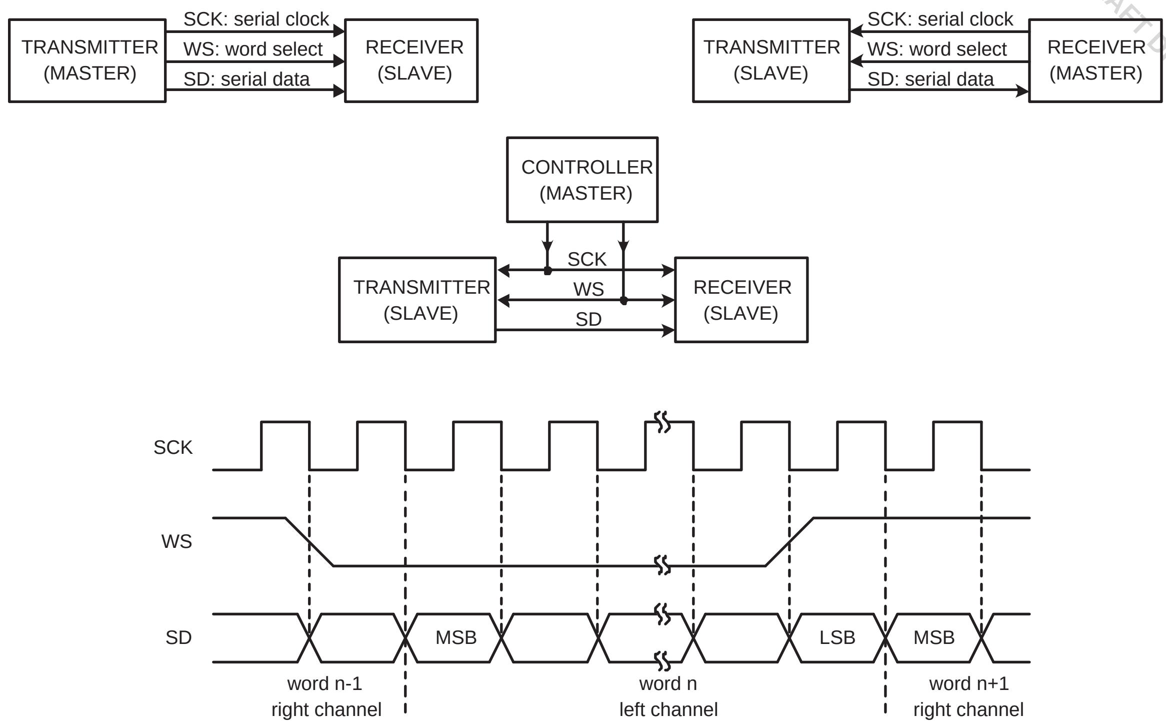


Fig 109. Simple I2S configurations and bus timing

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35.6 Register description

Table 728 shows the registers associated with the I2S interface and a summary of their functions. Following the table are details for each register.

Reset value reflects the data stored in used bits only. It does not include reserved bits content.

Table 728. Register overview: I2S0 (base address 0x400A 2000)

Name	Access	Address offset	Description	Reset value
DAO	R/W	0x000	I2S Digital Audio Output Register. Contains control bits for the I2S transmit channel.	0x87E1
DAI	R/W	0x004	I2S Digital Audio Input Register. Contains control bits for the I2S receive channel.	0x07E1
TXFIFO	WO	0x008	I2S Transmit FIFO. Access register for the 8 x 32-bit transmitter FIFO.	0
RXFIFO	RO	0x00C	I2S Receive FIFO. Access register for the 8 x 32-bit receiver FIFO.	0
STATE	RO	0x010	I2S Status Feedback Register. Contains status information about the I2S interface.	0x7
DMA1	R/W	0x014	I2S DMA Configuration Register 1. Contains control information for DMA request 1.	0
DMA2	R/W	0x018	I2S DMA Configuration Register 2. Contains control information for DMA request 2.	0
IRQ	R/W	0x01C	I2S Interrupt Request Control Register. Contains bits that control how the I2S interrupt request is generated.	0
TXRATE	R/W	0x020	I2S Transmit MCLK divider. This register determines the I2S TX MCLK rate by specifying the value to divide PCLK by in order to produce MCLK.	0
RXRATE	R/W	0x024	I2S Receive MCLK divider. This register determines the I2S RX MCLK rate by specifying the value to divide PCLK by in order to produce MCLK.	0
TXBITRATE	R/W	0x028	I2S Transmit bit rate divider. This register determines the I2S transmit bit rate by specifying the value to divide TX_MCLK by in order to produce the transmit bit clock.	0
RXBITRATE	R/W	0x02C	I2S Receive bit rate divider. This register determines the I2S receive bit rate by specifying the value to divide RX_MCLK by in order to produce the receive bit clock.	0
TXMODE	R/W	0x030	I2S Transmit mode control.	0
RXMODE	R/W	0x034	I2S Receive mode control.	0

Table 729. Register overview: I2S1 (base address 0x400A 3000)

Name	Access	Address offset	Description	Reset value
DAO	R/W	0x000	I2S Digital Audio Output Register. Contains control bits for the I2S transmit channel.	0x87E1
DAI	R/W	0x004	I2S Digital Audio Input Register. Contains control bits for the I2S receive channel.	0x07E1
TXFIFO	WO	0x008	I2S Transmit FIFO. Access register for the 8 x 32-bit transmitter FIFO.	0
RXFIFO	RO	0x00C	I2S Receive FIFO. Access register for the 8 x 32-bit receiver FIFO.	0

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Table 729. Register overview: I2S1 (base address 0x400A 3000)

Name	Access	Address offset	Description	Reset value
STATE	RO	0x010	I2S Status Feedback Register. Contains status information about the I2S interface.	0x7
DMA1	R/W	0x014	I2S DMA Configuration Register 1. Contains control information for DMA request 1.	0
DMA2	R/W	0x018	I2S DMA Configuration Register 2. Contains control information for DMA request 2.	0
IRQ	R/W	0x01C	I2S Interrupt Request Control Register. Contains bits that control how the I2S interrupt request is generated.	0
TXRATE	R/W	0x020	I2S Transmit MCLK divider. This register determines the I2S TX MCLK rate by specifying the value to divide PCLK by in order to produce MCLK.	0
RXRATE	R/W	0x024	I2S Receive MCLK divider. This register determines the I2S RX MCLK rate by specifying the value to divide PCLK by in order to produce MCLK.	0
TXBITRATE	R/W	0x028	I2S Transmit bit rate divider. This register determines the I2S transmit bit rate by specifying the value to divide TX_MCLK by in order to produce the transmit bit clock.	0
RXBITRATE	R/W	0x02C	I2S Receive bit rate divider. This register determines the I2S receive bit rate by specifying the value to divide RX_MCLK by in order to produce the receive bit clock.	0
TXMODE	R/W	0x030	I2S Transmit mode control.	0
RXMODE	R/W	0x034	I2S Receive mode control.	0

35.6.1 I2S Digital Audio Output register

The DAO register controls the operation of the I2S transmit channel. The function of bits in DAO are shown in Table 730.

Table 730. I2S Digital Audio Output register (DAO - address 0x400A 2000 (I2S0) and 0x400A 3000 (I2S1)) bit description

Bit	Symbol	Value	Description	Reset value
1:0	WORDWIDTH		Selects the number of bytes in data as follows:	01
		0x0	8-bit data	
		0x1	16-bit data	
		0x2	Reserved, do not use this setting	
		0x3	32-bit data	
2	MONO		When 1, data is of monaural format. When 0, the data is in stereo format.	0
3	STOP		When 1, disables accesses on FIFOs, places the transmit channel in mute mode.	0
4	RESET		When 1, asynchronously resets the transmit channel and FIFO.	0
5	WS_SEL		When 0, the interface is in master mode. When 1, the interface is in slave mode. See Section 35.7.2 for a summary of useful combinations for this bit with TXMODE.	1

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Table 730. I2S Digital Audio Output register (DAO - address 0x400A 2000 (I2S0) and 0x400A 3000 (I2S1)) bit description

Bit	Symbol	Value	Description	Reset value
14:6	WS_HALFPERIOD		Word select half period minus 1, i.e. WS 64clk period -> ws_halfperiod = 31.	0x1F
15	MUTE		When 1, the transmit channel sends only zeroes.	1
31:16	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

35.6.2 I2S Digital Audio Input register

The DAI register controls the operation of the I2S receive channel. The function of bits in DAI are shown in Table 731.

Table 731. I2S Digital Audio Input register (DAI - address 0x400A 2004 (I2S0) and 0x400A 3004 (I2S1)) bit description

Bit	Symbol	Value	Description	Reset value
1:0	WORDWIDTH		Selects the number of bytes in data as follows:	01
		0x0	8-bit data	
		0x1	16-bit data	
		0x2	Reserved, do not use this setting	
		0x3	32-bit data	
2	MONO		When 1, data is of monaural format. When 0, the data is in stereo format.	0
3	STOP		When 1, disables accesses on FIFOs, places the transmit channel in mute mode.	0
4	RESET		When 1, asynchronously reset the transmit channel and FIFO.	0
5	WS_SEL		When 0, the interface is in master mode. When 1, the interface is in slave mode. See Section 35.7.2 for a summary of useful combinations for this bit with RXMODE.	1
14:6	WS_HALFPERIOD		Word select half period minus 1, i.e. WS 64clk period -> ws_halfperiod = 31.	0x1F
31:15	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

35.6.3 I2S Transmit FIFO register

The TXFIFO register provides access to the transmit FIFO. The function of bits in TXFIFO are shown in Table 732.

Table 732. Transmit FIFO register (TXFIFO - address 0x400A 2008 (I2S0) and 0x400A 3008 (I2S1)) bit description

Bit	Symbol	Description	Reset value
31:0	I2STXFIFO	8 x 32-bit transmit FIFO.	0

35.6.4 Receive FIFO register

The I2SRXFIFO register provides access to the receive FIFO. The function of bits in I2SRXFIFO are shown in Table 733.

Table 733. I2S Receive FIFO register (RXFIFO - address 0x400A 200C (I2S0) and 0x400A 300C (I2S1)) bit description

Bit	Symbol	Description	Reset value
31:0	I2SRXFIFO	8 x 32-bit transmit FIFO.	0

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35.6.5 I2S Status Feedback register

The STATE register provides status information about the I2S interface. The meaning of bits in STATE are shown in Table 734.

Table 734. I2S Status Feedback register (STATE - address 0x400A 2010 (I2S0) and 0x400A 3010 (I2S1)) bit description

Bit	Symbol	Description	Reset value
0	IRQ	This bit reflects the presence of Receive Interrupt or Transmit Interrupt. This is determined by comparing the current FIFO levels to the rx_depth_irq and tx_depth_irq fields in the IRQ register.	1
1	DMAREQ1	This bit reflects the presence of Receive or Transmit DMA Request 1. This is determined by comparing the current FIFO levels to the rx_depth_dma1 and tx_depth_dma1 fields in the DMA1 register.	1
2	DMAREQ2	This bit reflects the presence of Receive or Transmit DMA Request 2. This is determined by comparing the current FIFO levels to the rx_depth_dma2 and tx_depth_dma2 fields in the DMA2 register.	1
7:3	-	Reserved.	0
11:8	RX_LEVEL	Reflects the current level of the Receive FIFO.	0
15:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
19:16	TX_LEVEL	Reflects the current level of the Transmit FIFO.	0
31:20	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

35.6.6 I2S DMA Configuration Register 1

The DMA1 register controls the operation of DMA request 1. The function of bits in DMA1 are shown in Table 735. Refer to Chapter 16 “LPC18xx General Purpose DMA (GPDMA) controller” for details of DMA operation.

This register enables the DMA for the I^2S receive and transmit channels and sets the FIFO level.

Remark: The FIFOs contain eight 16-bit words. Therefore, if the I^2S controller is configured for 32-bit mode (see Table 730 and Table 731), the maximum allowed FIFO level is 4.

Table 735. I2S DMA Configuration register 1 (DMA1 - address 0x400A 2014 (I2S0) and 0x400A 3014 (I2S1)) bit description

Bit	Symbol	Description	Reset value
0	RX_DMA1_ENABLE	When 1, enables DMA1 for I2S receive.	0
1	TX_DMA1_ENABLE	When 1, enables DMA1 for I2S transmit.	0
7:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0
11:8	RX_DEPTH_DMA1	Set the FIFO level that triggers a receive DMA request on DMA1.	0

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Table 735. I2S DMA Configuration register 1 (DMA1 - address 0x400A 2014 (I2S0) and 0x400A 3014 (I2S1)) bit description

Bit	Symbol	Description	Reset value
15:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
19:16	TX_DEPTH_DMA1	Set the FIFO level that triggers a transmit DMA request on DMA1.	0
31:20	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

35.6.7 I2S DMA Configuration Register 2

The DMA2 register controls the operation of DMA request 2. The function of bits in DMA2 are shown in Table 730.

This register enables the DMA for the I^{2}S receive and transmit channels and sets the FIFO level.

Remark: The FIFOs contain eight 16-bit words. Therefore, if the I^{2}S controller is configured for 32-bit mode (see Table 730 and Table 731), the maximum allowed FIFO level is 4.

Table 736. I2S DMA Configuration register 2 (DMA2 - address 0x400A 2018 (I2S0) and 0x400A 3018 (I2S1)) bit description

Bit	Symbol	Description	Reset value
0	RX_DMA2_ENABLE	When 1, enables DMA1 for I2S receive.	0
1	TX_DMA2_ENABLE	When 1, enables DMA1 for I2S transmit.	0
7:2	-	Reserved.	0
11:8	RX_DEPTH_DMA2	Set the FIFO level that triggers a receive DMA request on DMA2.	0
15:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
19:16	TX_DEPTH_DMA2	Set the FIFO level that triggers a transmit DMA request on DMA2.	0
31:20	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

35.6.8 I2S Interrupt Request Control register

The IRQ register controls the operation of the I2S interrupt request. The function of bits in IRQ are shown in Table 730.

Table 737. I2S Interrupt Request Control register (IRQ - address 0x400A 201C (I2S0) and 0x400A 301C (I2S1)) bit description

Bit	Symbol	Description	Reset value
0	RX_IRQ_ENABLE	When 1, enables I2S receive interrupt.	0
1	TX_IRQ_ENABLE	When 1, enables I2S transmit interrupt.	0
7:2	-	Reserved.	0
11:8	RX_DEPTH_IRQ	Set the FIFO level on which to create an irq request.	0

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Table 737. I2S Interrupt Request Control register (IRQ - address 0x400A 201C (I2S0) and 0x400A 301C (I2S1)) bit description

Bit	Symbol	Description	Reset value
15:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
19:16	TX_DEPTH_IRQ	Set the FIFO level on which to create an irq request.	0
31:20	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

35.6.9 I2S Transmit Clock Rate register

The MCLK rate for the I2S transmitter is determined by the values in the TXRATE register. The required TXRATE setting depends on the desired audio sample rate desired, the format (stereo/mono) used, and the data size.

The transmitter MCLK rate is generated using a fractional rate generator, dividing down the frequency of PCLK_I2S (= CLK_APB1_I2S). Values of the numerator (X) and the denominator (Y) must be chosen to produce a frequency twice that desired for the transmitter MCLK, which must be an integer multiple of the transmitter bit clock rate. Fractional rate generators have some aspects that the user should be aware of when choosing settings. These are discussed in Section 35.6.9.1. The equation for the fractional rate generator is:

I2STXMCLK = PCLK_I2S * (X/Y) /2

Note: If the value of X or Y is 0, then no clock is generated. Also, the value of Y must be greater than or equal to X.

Table 738. I2S Transmit Clock Rate register (TXRATE - address 0x400A 2020 (I2S0) and 0x400A 3020 (I2S1)) bit description

Bit	Symbol	Description	Reset value
7:0	Y_DIVIDER	I2S transmit MCLK rate denominator. This value is used to divide PCLK to produce the transmit MCLK. Eight bits of fractional divide supports a wide range of possibilities. A value of 0 stops the clock.	0
15:8	X_DIVIDER	I2S transmit MCLK rate numerator. This value is used to multiply PCLK by to produce the transmit MCLK. A value of 0 stops the clock. Eight bits of fractional divide supports a wide range of possibilities. Note: the resulting ratio X/Y is divided by 2.	0
31:16	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

35.6.9.1 Notes on fractional rate generators

The nature of a fractional rate generator is that there will be some output jitter with some divide settings. This is because the fractional rate generator is a fully digital function, so output clock transitions are synchronous with the source clock, whereas a theoretical perfect fractional rate may have edges that are not related to the source clock. So, output jitter will not be greater than plus or minus one source clock between consecutive clock edges.

For example, if X = 0x07 and Y = 0x11, the fractional rate generator will output 7 clocks for every 17 (11 hex) input clocks, distributed as evenly as it can. In this example, there is no way to distribute the output clocks in a perfectly even fashion, so some clocks will be

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longer than others. The output is divided by 2 in order to square it up, which also helps with the jitter. The frequency averages out to exactly (7/17) / 2, but some clocks will be a slightly different length than their neighbors. It is possible to avoid jitter entirely by choosing fractions such that X divides evenly into Y, such as 2/4, 2/6, 3/9, 1/N, etc.

35.6.10 I2S Receive Clock Rate register

The MCLK rate for the I2S receiver is determined by the values in the RXRATE register. The required RXRATE setting depends on the peripheral clock rate (PCLK_I2S = CLK_APB1_I2S) and the desired MCLK rate (such as 256 fs).

The receiver MCLK rate is generated using a fractional rate generator, dividing down the frequency of PCLK_I2S. Values of the numerator (X) and the denominator (Y) must be chosen to produce a frequency twice that desired for the receiver MCLK, which must be an integer multiple of the receiver bit clock rate. Fractional rate generators have some aspects that the user should be aware of when choosing settings. These are discussed in Section 35.6.9.1. The equation for the fractional rate generator is:

I2SRXMCLK = PCLK_I2S * (X/Y) /2

Note: If the value of X or Y is 0, then no clock is generated. Also, the value of Y must be greater than or equal to X.

Table 739. I2S Receive Clock Rate register (RXRATE - address 0x400A 2024 (I2S0) and 0x400A 3024 (I2S1)) bit description

Bit	Symbol	Description	Reset value
7:0	Y_DIVIDER	I2S receive MCLK rate denominator. This value is used to divide PCLK to produce the receive MCLK. Eight bits of fractional divide supports a wide range of possibilities. A value of 0 stops the clock.	0
15:8	X_DIVIDER	I2S receive MCLK rate numerator. This value is used to multiply PCLK by to produce the receive MCLK. A value of 0 stops the clock. Eight bits of fractional divide supports a wide range of possibilities. Note: the resulting ratio X/Y is divided by 2.	0
31:16	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

35.6.11 I2S Transmit Clock Bit Rate register

The bit rate for the I2S transmitter is determined by the value of the TXBITRATE register. The value depends on the audio sample rate desired, and the data size and format (stereo/mono) used. For example, a 48 kHz sample rate for 16-bit stereo data requires a bit rate of 48,000´16´2 = 1.536 MHz.

Table 740. I2S Transmit Clock Rate register (TXBITRATE - address 0x400A 2028 (I2S0) and 0x400A 3028 (I2S1)) bit description

Bit	Symbol	Description	Reset value
5:0	TX_BITRATE	I2S transmit bit rate. This value plus one is used to divide TX_MCLK to produce the transmit bit clock.	0
31:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

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35.6.12 I2S Receive Clock Bit Rate register

The bit rate for the I2S receiver is determined by the value of the RXBITRATE register. The value depends on the audio sample rate, as well as the data size and format used. The calculation is the same as for RXBITRATE.

Table 741. I2S Receive Clock Rate register (RXBITRATE - address 0x400A 202C (I2S0) and 0x400A 302C (I2S1)) bit description

Bit	Symbol	Description	Reset value
5:0	RX_BITRATE	I2S receive bit rate. This value plus one is used to divide RX_MCLK to produce the receive bit clock.	0
31:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

35.6.13 I2S Transmit Mode Control register

The Transmit Mode Control register contains additional controls for transmit clock source, enabling the 4-pin mode, and how MCLK is used. See Section 35.7.2 for a summary of useful mode combinations.

Table 742. I2S Transmit Mode Control register (TXMODE - address 0x400A 2030 (I2S0) and 0x400A 3030 (I2S1)) bit description

Bit	Symbol	Value	Description	Reset value
1:0	TXCLKSEL		Clock source selection for the transmit bit clock divider.	0
		0x0	Select the TX fractional rate divider clock output as the source	
		0x1	Reserved	
		0x2	Select the RX_MCLK signal as the TX_MCLK clock source	
		0x3	Reserved	
2	TX4PIN		Transmit 4-pin mode selection. When 1, enables 4-pin mode.	0
3	TXMCENA		Enable for the TX_MCLK output. When 0, output of TX_MCLK is not enabled. When 1, output of TX_MCLK is enabled.	0
31:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

35.6.14 I2S Receive Mode Control register

The Receive Mode Control register contains additional controls for receive clock source, enabling the 4-pin mode, and how MCLK is used. See Section 35.7.2 for a summary of useful mode combinations.

Table 743. I2S Receive Mode Control register (RXMODE - address 0x400A 2034 (I2S0) and 0x400A 3034 (I2S1)) bit description

Bit	Symbol	Value	Description	Reset value
1:0	RXCLKSEL		Clock source selection for the receive bit clock divider.	0
		0x0	Select the RX fractional rate divider clock output as the source	
		0x1	Reserved	
		0x2	Select the TX_MCLK signal as the RX_MCLK clock source	
		0x3	Reserved	

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Table 743. I2S Receive Mode Control register (RXMODE - address 0x400A 2034 (I2S0) and 0x400A 3034 (I2S1)) bit description

Bit	Symbol	Value	Description	Reset value
2	RX4PIN		Receive 4-pin mode selection. When 1, enables 4-pin mode.	0
3	RXMCENA		Enable for the RX_MCLK output. When 0, output of RX_MCLK is not enabled. When 1, output of RX_MCLK is enabled.	0
31:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

35.7 Functional description

35.7.1 I²S transmit and receive interfaces

The I2S interface can transmit and receive 8-bit, 16-bit or 32-bit stereo or mono audio information. Some details of I2S implementation are:

- When the FIFO is empty, the transmit channel will repeat transmitting the same data until new data is written to the FIFO.
- When mute is true, the data value 0 is transmitted.
- When mono is false, two successive data words are respectively left and right data.
- Data word length is determined by the wordwidth value in the configuration register. There is a separate wordwidth value for the receive channel and the transmit channel.
  - 0: word is considered to contain four 8-bit data words.
  - 1: word is considered to contain two 16-bit data words.
  - 3: word is considered to contain one 32-bit data word.
- When the transmit FIFO contains insufficient data the transmit channel will repeat transmitting the last data until new data is available. This can occur when the microprocessor or the DMA at some time is unable to provide new data fast enough. Because of this delay in new data there is a need to fill the gap, which is accomplished by continuing to transmit the last sample. The data is not muted as this would produce an noticeable and undesirable effect in the sound.
- The transmit channel and the receive channel only handle 32-bit aligned words, data chunks must be clipped or extended to a multiple of 32 bits.

When switching between data width or modes the I2S must be reset via the reset bit in the control register in order to ensure correct synchronization. It is advisable to set the stop bit also until sufficient data has been written in the transmit FIFO. Note that when stopped data output is muted.

All data accesses to FIFOs are 32 bits. Figure 122 shows the possible data sequences.

A data sample in the FIFO consists of:

- 1´32 bits in 8-bit or 16-bit stereo modes.
- 1´32 bits in mono modes.
- 2´32 bits, first left data, second right data, in 32-bit stereo modes.

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Data is read from the transmit FIFO after the falling edge of WS, it will be transferred to the transmit clock domain after the rising edge of WS. On the next falling edge of WS the left data will be loaded in the shift register and transmitted and on the following rising edge of WS the right data is loaded and transmitted.

The receive channel will start receiving data after a change of WS. When word select becomes low it expects this data to be left data, when WS is high received data is expected to be right data. Reception will stop when the bit counter has reached the limit set by wordwidth. On the next change of WS the received data will be stored in the appropriate hold register. When complete data is available it will be written into the receive FIFO.

35.7.2 I^{2}S operating modes

The clocking and WS usage of the I2S interface is configurable. In addition to master and slave modes, which are independently configurable for the transmitter and the receiver, several different clock sources are possible, including variations that share the clock and/or WS between the transmitter and receiver. This last option allows using I2S with fewer pins, typically four.

Many configurations are possible that are not considered useful, the following tables and figures give details of the configurations that are most likely to be useful.

Table 744. I2S transmit modes

DAO bit 5	TXMODE bits [3:0]	Description
0	0 0 0 0	Typical transmitter master mode. See Figure 110. The I2S transmit function operates as a master. The transmit clock source is the fractional rate divider. The WS used is the internally generated TX_WS. The TX_MCLK pin is not enabled for output.
0	0 0 1 0	Transmitter master mode sharing the receiver reference clock. See Figure 111. The I2S transmit function operates as a master. The transmit clock source is RX_REF. The WS used is the internally generated TX_WS. The TX_MCLK pin is not enabled for output.
0	0 1 0 0	4-wire transmitter master mode sharing the receiver bit clock and WS. See Figure 112. The I2S transmit function operates as a master. The transmit clock source is the RX bit clock. The WS used is the internally generated RX_WS. The TX_MCLK pin is not enabled for output.
0	1 0 0 0	Transmitter master mode with TX_MCLK output. See Figure 110. The I2S transmit function operates as a master. The transmit clock source is the fractional rate divider. The WS used is the internally generated TX_WS. The TX_MCLK pin is enabled for output.

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Table 744. I2S transmit modes

DAO bit 5	TXMODE bits [3:0]	Description
1	0 0 0 0	Typical transmitter slave mode. See Figure 113. The I2S transmit function operates as a slave. The transmit clock source is the TX_SCK pin. The WS used is the TX_WS pin.
1	0 0 1 0	Transmitter slave mode sharing the receiver reference clock. See Figure 114. The I2S transmit function operates as a slave. The transmit clock source is RX_REF. The WS used is the TX_WS pin.
1	0 1 0 0	4-wire transmitter slave mode sharing the receiver bit clock and WS. See Figure 115. The I2S transmit function operates as a slave. The transmit clock source is the RX bit clock. The WS used is RX_WS ref.

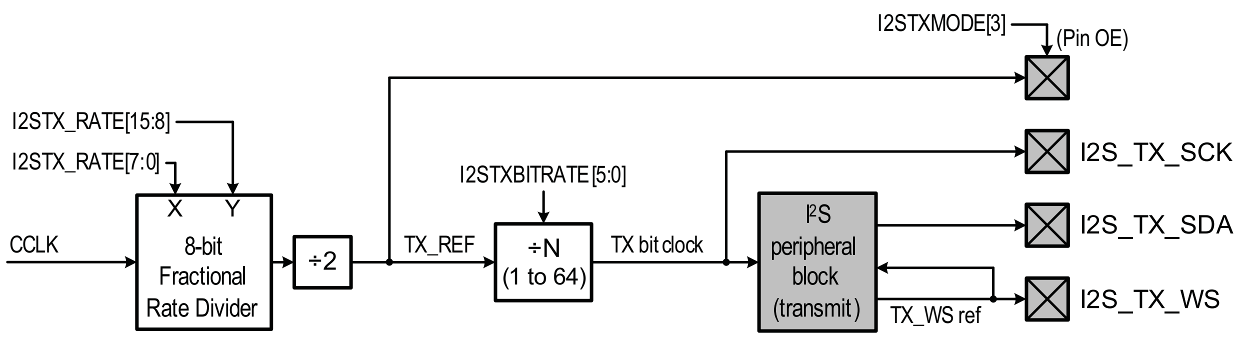


Fig 110. Typical transmitter master mode, with or without MCLK output

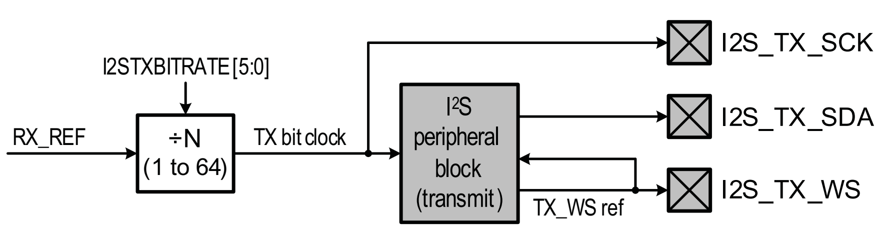


Fig 111. Transmitter master mode sharing the receiver reference clock

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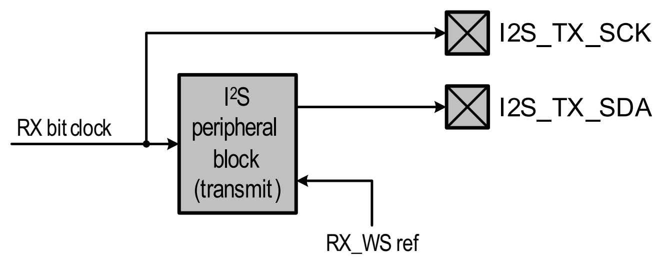


Fig 112. 4-wire transmitter master mode sharing the receiver bit clock and WS

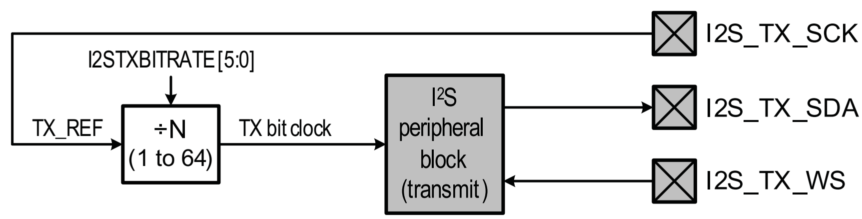


Fig 113. Typical transmitter slave mode

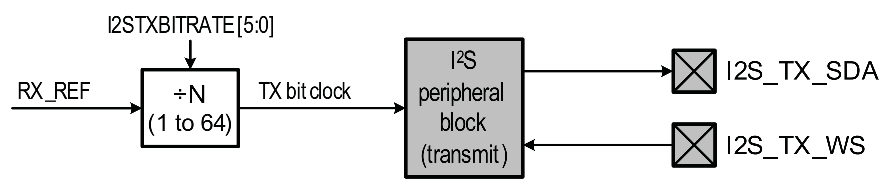


Fig 114. Transmitter slave mode sharing the receiver reference clock

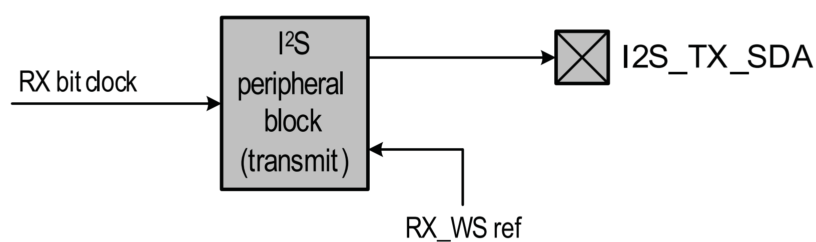


Fig 115. 4-wire transmitter slave mode sharing the receiver bit clock and WS

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Table 745. I2S receive modes

DAI bit 5	RXMODE bit [3:0]	Description
0	0 0 0 0	Typical receiver master mode. See Figure 116. The I2S receive function operates as a master. The receive clock source is the fractional rate divider. The WS used is the internally generated RX_WS. The RX_MCLK pin is not enabled for output.
0	0 0 1 0	Receiver master mode sharing the transmitter reference clock. See Figure 117. The I2S receive function operates as a master. The receive clock source is TX_REF. The WS used is the internally generated RX_WS. The RX_MCLK pin is not enabled for output.
0	0 1 0 0	4-wire receiver master mode sharing the transmitter bit clock and WS. See Figure 118. The I2S receive function operates as a master. The receive clock source is the TX bit clock. The WS used is the internally generated TX_WS. The RX_MCLK pin is not enabled for output.
0	1 0 0 0	Receiver master mode with RX_MCLK output. See Figure 116. The I2S receive function operates as a master. The receive clock source is the fractional rate divider. The WS used is the internally generated RX_WS. The RX_MCLK pin is enabled for output.
1	0 0 0 0	Typical receiver slave mode. See Figure 119. The I2S receive function operates as a slave. The receive clock source is the RX_SCK pin. The WS used is the RX_WS pin.
1	0 0 1 0	Receiver slave mode sharing the transmitter reference clock. See Figure 120. The I2S receive function operates as a slave. The receive clock source is TX_REF. The WS used is the RX_WS pin.
1	0 1 0 0	This is a 4-wire receiver slave mode sharing the transmitter bit clock and WS. See Figure 121. The I2S receive function operates as a slave. The receive clock source is the TX bit clock. The WS used is TX_WS ref.

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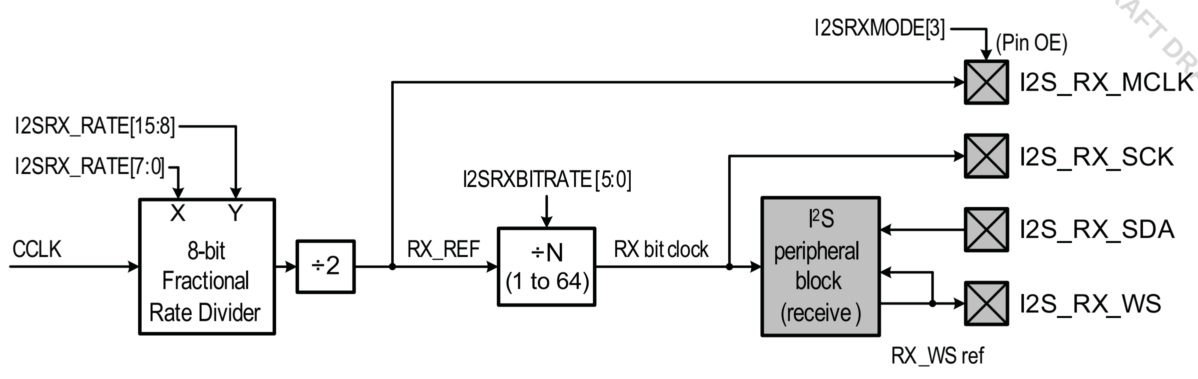


Fig 116. Typical receiver master mode, with or without MCLK output

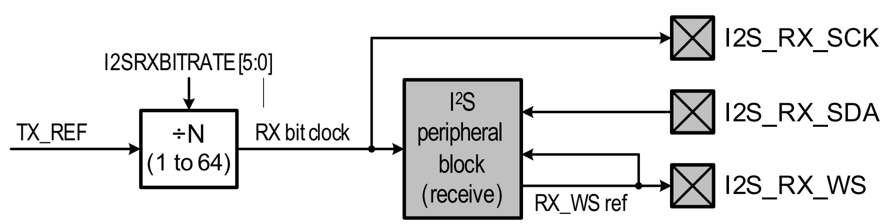


Fig 117. Receiver master mode sharing the transmitter reference clock

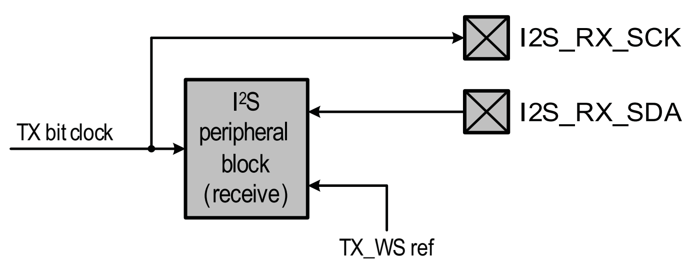


Fig 118. 4-wire receiver master mode sharing the transmitter bit clock and WS

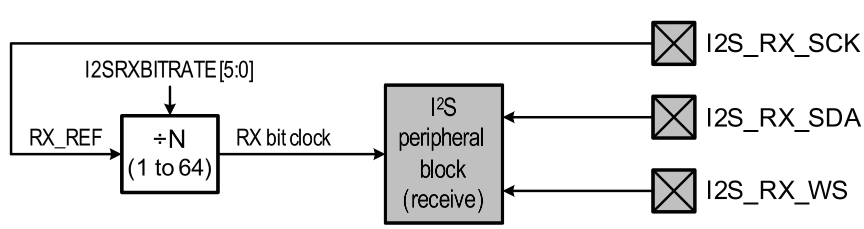


Fig 119. Typical receiver slave mode

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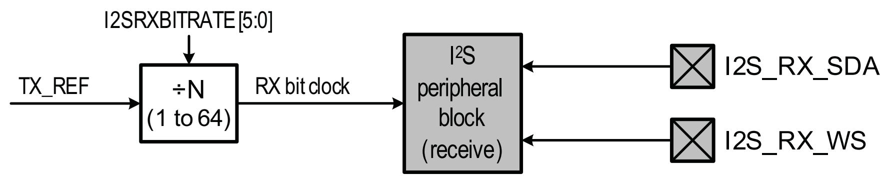


Fig 120. Receiver slave mode sharing the transmitter reference clock

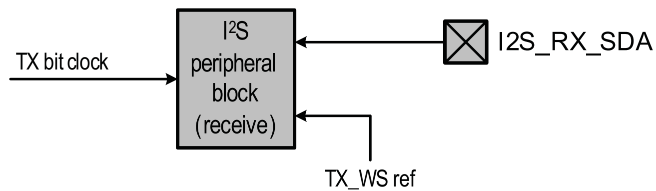


Fig 121. 4-wire receiver slave mode sharing the transmitter bit clock and WS

35.7.3 FIFO controller

Handling of data for transmission and reception is performed via the FIFO controller which can generate two DMA requests and an interrupt request. The controller consists of a set of comparators which compare FIFO levels with depth settings contained in registers. The current status of the level comparators can be seen in the APB status register.

Table 746. Conditions for FIFO level comparison

Level Comparison	Condition
dmareq_tx_1	tx_depth_dma1 >= tx_level
dmareq_rx_1	rx_depth_dma1 <= rx_level
dmareq_tx_2	tx_depth_dma2 >= tx_level
dmareq_rx_2	rx_depth_dma2 <= rx_level
irq_tx	tx_depth_irq >= tx_level
irq_rx	rx_depth_irq <= rx_level

System signaling occurs when a level detection is true and enabled.

Table 747. DMA and interrupt request generation

System Signaling	Condition
irq	(irq_rx & rx_irq_enable) | (irq_tx & tx_irq_enable)
dmareq[0]	(dmareq_tx_1 & tx_dma1_enable) | (dmareq_rx_1 & rx_dma1_enable)
dmareq[1]	(dmareq_tx_2 & tx_dma2_enable) | (dmareq_rx_2 & rx_dma2_enable)

Table 748. Status feedback in the STATE register

Status Feedback	Status
irq	irq_rx | irq_tx
dmareq1	(dmareq_tx_1 | dmareq_rx_1)
dmareq2	(dmareq_rx_2 | dmareq_tx_2)

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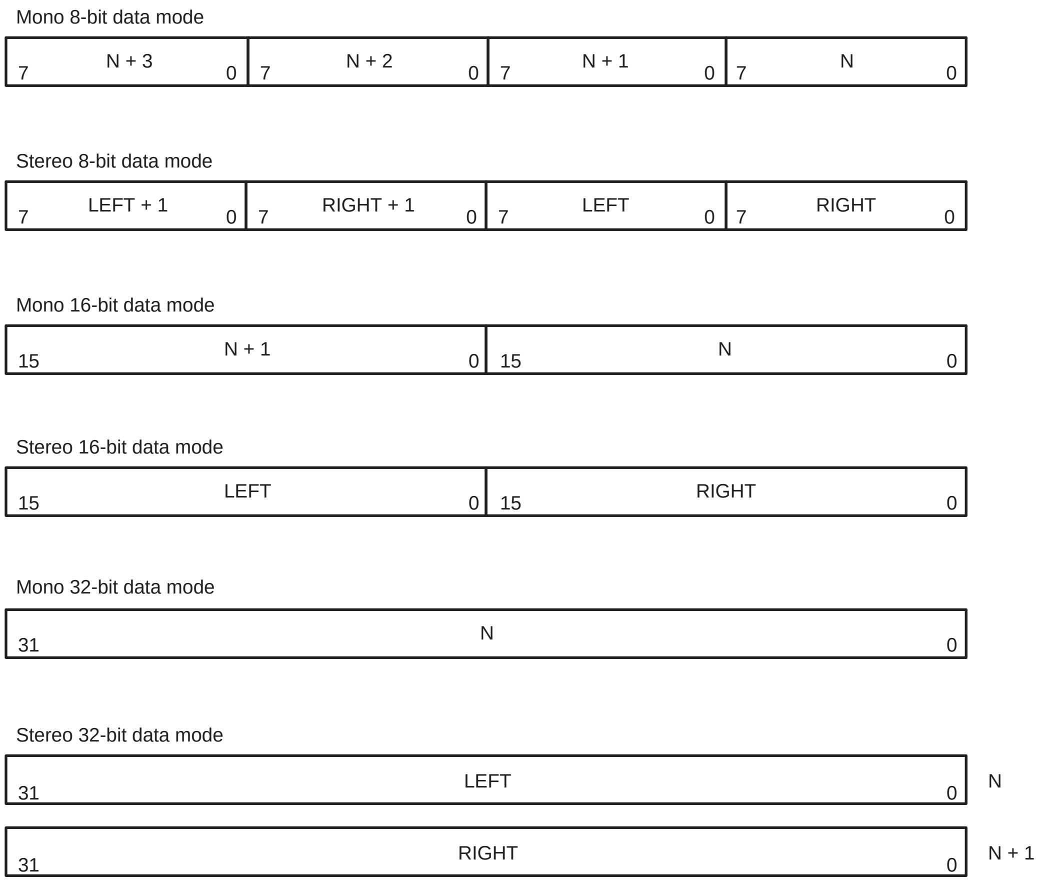


Fig 122. FIFO contents for various I²S modes

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36.1 How to read this chapter

The C_CAN0/1 controllers are available on all LPC18xx parts.

36.2 Basic configuration

The C_CAN is configured as follows:

- See Table 749 for clocking and power control.
- The C_CAN0 is reset by the CAN0_RST (reset # 55).
- The C_CAN1 is reset by the CAN1_RST (reset # 56).
- The ORed C_CAN0 and C_CAN1 interrupt is connected to slot # 12 in the Event router.
- The C_CAN0 interrupt is connected to interrupt #51 in the NVIC.
- The C_CAN1 interrupt is connected to interrupt #43 in the NVIC.

Table 749. C_CAN clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to the C_CAN0 register interface and C_CAN0 peripheral clock.	BASE_APB3_CLK	CLK_APB3_CAN0	150 MHz
Clock to the C_CAN1 register interface and C_CAN1 peripheral clock.	BASE_APB1_CLK	CLK_APB1_CAN1	150 MHz

36.3 Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.

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36.4 General description

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller allows to build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a very high level of security.

The CAN controller consists of a CAN core, message RAM, a message handler, control registers, and the APB interface.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM.

All functions concerning the handling of messages are implemented in the Message Handler. Those functions are the acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the CAN controller can be accessed directly by an external CPU via the APB bus. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

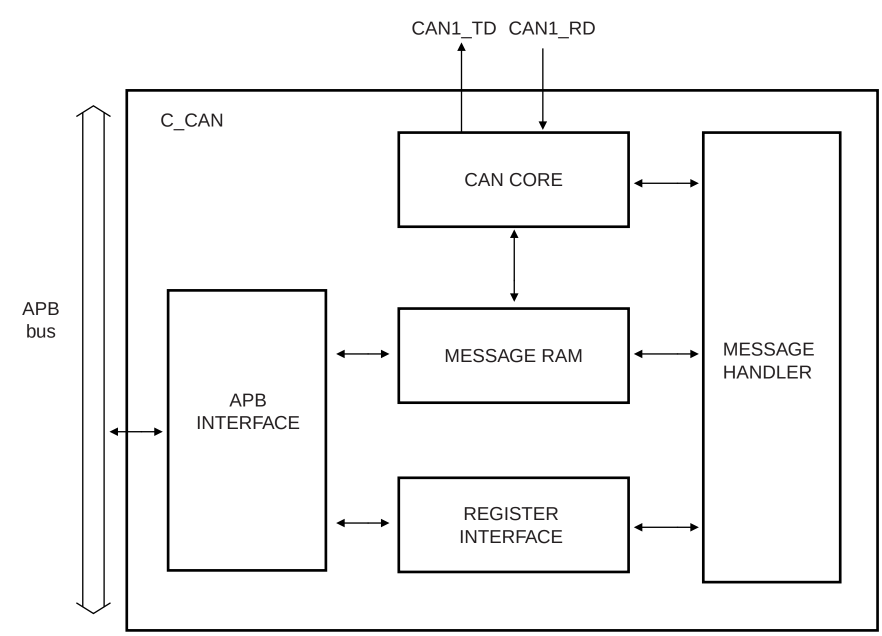


Fig 123. C_CAN block diagram

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36.5 Pin description

Table 750. C_CAN pin description

Function pinned out	Direction	Description
CAN0/1_RD	I	C_CAN receive input
CAN0/1_TD	O	C_CAN transmit output

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36.6 Register description

Register values at reset

After a hardware reset, the registers hold the values described in Table 751. Additionally, the busoff state is reset and the output TD0,1 is set to recessive (HIGH). The value 0x0001 (INIT = ‘1’) in the CAN Control Register enables the software initialization. The CAN controller does not communicate with the CAN bus until the CPU resets INIT to ‘0’.

The data stored in the message RAM is not affected by a hardware reset. After power-on, the contents of the message RAM is undefined.

Timing of read/write operations

Remark: Reading any of the CAN registers requires **two** consecutive read operations from the same location. Only the data from the **second** read operation are valid.

Successive read operations to the C_CAN registers must be separated by a minimum of (CLKDIVVAL × 2 + 2) × PCLK, where CLKDIVVAL is the can clock divider value and PCLK is the peripheral clock.

Successive write operations to the C_CAN registers must be separated by a minimum of (CLKDIVVAL × 2) × PCLK, where CLKDIVVAL is the can clock divider value and PCLK is the peripheral clock.

Table 751. Register overview: C_CAN0 (base address 0x400E 2000)

Name	Access	Address offset	Description	Reset value
CNTL		0x000	CAN control	0x0001
STAT		0x004	Status register	0x0000
EC	RO	0x008	Error counter	0x0000
BT		0x00C	Bit timing register	0x2301
INT	RO	0x010	Interrupt register	0x0000
TEST		0x014	Test register	-
BRPE		0x018	Baud rate prescaler extension register	0x0000
-	-	0x01C	Reserved	-
IF1_CMDREQ		0x020	Message interface 1 command request	0x0001
IF1_CMDMSK_W		0x024	Message interface 1 command mask (write direction)	0x0000
IF1_CMDMSK_R		0x024	Message interface 1 command mask (read direction)	0x0000
IF1_MSK1		0x028	Message interface 1 mask 1	0xFFFF
IF1_MSK2		0x02C	Message interface 1 mask 2	0xFFFF
IF1_ARB1		0x030	Message interface 1 arbitration 1	0x0000
IF1_ARB2		0x034	Message interface 1 arbitration 2	0x0000
IF1_MCTRL		0x038	Message interface 1 message control	0x0000
IF1_DA1		0x03C	Message interface 1 data A1	0x0000
IF1_DA2		0x040	Message interface 1 data A2	0x0000
IF1_DB1		0x044	Message interface 1 data B1	0x0000
IF1_DB2		0x048	Message interface 1 data B2	0x0000

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Table 751. Register overview: C_CAN0 (base address 0x400E 2000)

Name	Access	Address offset	Description	Reset value
-		0x04C - 0x07C	Reserved	-
IF2_CMDREQ		0x080	Message interface 2 command request	0x0001
IF2_CMDMSK		0x084	Message interface 2 command mask	0x0000
IF2_MSK1		0x088	Message interface 2 mask 1	0xFFFF
IF2_MSK2		0x08C	Message interface 2 mask 2	0xFFFF
IF2_ARB1		0x090	Message interface 2 arbitration 1	0x0000
IF2_ARB2		0x094	Message interface 2 arbitration 2	0x0000
IF2_MCTRL		0x098	Message interface 2 message control	0x0000
IF2_DA1		0x09C	Message interface 2 data A1	0x0000
IF2_DA2		0x0A0	Message interface 2 data A2	0x0000
IF2_DB1		0x0A4	Message interface 2 data B1	0x0000
IF2_DB2		0x0A8	Message interface 2 data B2	0x0000
-	-	0x0AC - 0x0FC		
TXREQ1	RO	0x100	Transmission request 1	0x0000
TXREQ2	RO	0x104	Transmission request 2	0x0000
-	-	0x108 - 0x11C	Reserved	-
ND1	RO	0x120	New data 1	0x0000
ND2	RO	0x124	New data 2	0x0000
-	-	0x128 - 0x13C	Reserved	-
IR1	RO	0x140	Interrupt pending 1	0x0000
IR2	RO	0x144	Interrupt pending 2	0x0000
-	-	0x148 - 0x15C	Reserved	-
MSGV1	RO	0x160	Message valid 1	0x0000
MSGV2	RO	0x164	Message valid 2	0x0000
-	-	0x168 - 0x17C	Reserved	-
CLKDIV	R/W	0x180	CAN clock divider register	0x0001

Table 752. Register overview: C_CAN1 (base address 0x400A 4000)

Name	Access	Address offset	Description	Reset value
CNTL		0x000	CAN control	0x0001
STAT		0x004	Status register	0x0000
EC	RO	0x008	Error counter	0x0000
BT		0x00C	Bit timing register	0x2301
INT	RO	0x010	Interrupt register	0x0000
TEST		0x014	Test register	-

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Table 752. Register overview: C_CAN1 (base address 0x400A 4000)

Name	Access	Address offset	Description	Reset value
BRPE		0x018	Baud rate prescaler extension register	0x0000
-	-	0x01C	Reserved	-
IF1_CMDREQ		0x020	Message interface 1 command request	0x0001
IF1_CMDMSK_W		0x024	Message interface 1 command mask (write direction)	0x0000
IF1_CMDMSK_R		0x024	Message interface 1 command mask (read direction)	0x0000
IF1_MSK1		0x028	Message interface 1 mask 1	0xFFFF
IF1_MSK2		0x02C	Message interface 1 mask 2	0xFFFF
IF1_ARB1		0x030	Message interface 1 arbitration 1	0x0000
IF1_ARB2		0x034	Message interface 1 arbitration 2	0x0000
IF1_MCTRL		0x038	Message interface 1 message control	0x0000
IF1_DA1		0x03C	Message interface 1 data A1	0x0000
IF1_DA2		0x040	Message interface 1 data A2	0x0000
IF1_DB1		0x044	Message interface 1 data B1	0x0000
IF1_DB2		0x048	Message interface 1 data B2	0x0000
-		0x04C - 0x07C	Reserved	-
IF2_CMDREQ		0x080	Message interface 2 command request	0x0001
IF2_CMDMSK		0x084	Message interface 2 command mask	0x0000
IF2_MSK1		0x088	Message interface 2 mask 1	0xFFFF
IF2_MSK2		0x08C	Message interface 2 mask 2	0xFFFF
IF2_ARB1		0x090	Message interface 2 arbitration 1	0x0000
IF2_ARB2		0x094	Message interface 2 arbitration 2	0x0000
IF2_MCTRL		0x098	Message interface 2 message control	0x0000
IF2_DA1		0x09C	Message interface 2 data A1	0x0000
IF2_DA2		0x0A0	Message interface 2 data A2	0x0000
IF2_DB1		0x0A4	Message interface 2 data B1	0x0000
IF2_DB2		0x0A8	Message interface 2 data B2	0x0000
-	-	0x0AC - 0x0FC		
TXREQ1	RO	0x100	Transmission request 1	0x0000
TXREQ2	RO	0x104	Transmission request 2	0x0000
-	-	0x108 - 0x11C	Reserved	-
ND1	RO	0x120	New data 1	0x0000
ND2	RO	0x124	New data 2	0x0000
-	-	0x128 - 0x13C	Reserved	-
IR1	RO	0x140	Interrupt pending 1	0x0000
IR2	RO	0x144	Interrupt pending 2	0x0000

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Table 752. Register overview: C_CAN1 (base address 0x400A 4000)

Name	Access	Address offset	Description	Reset value
-	-	0x148 - 0x15C	Reserved	-
MSGV1	RO	0x160	Message valid 1	0x0000
MSGV2	RO	0x164	Message valid 2	0x0000
-	-	0x168 - 0x17C	Reserved	-
CLKDIV	R/W	0x180	CAN clock divider register	0x0001

36.6.1 CAN protocol registers

36.6.1.1 CAN control register

After a hardware reset, the registers of the C_CAN controller hold the values described in Table 751. Additionally, the busoff state is set, and the TD0/1 outputs are set to HIGH. The reset value 0x0001 of the CANCTRL register enables initialization by software (INIT = 1). The C_CAN does not influence the CAN bus until the CPU resets the INIT bit to 0.

Table 753. CAN control registers (CNTL, address 0x400E 2000 (C_CAN0) and 0x400A 4000 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	INIT		Initialization	1	R/W
		0	Normal operation.		
		1	Initialization is started. On reset, software needs to initialize the CAN controller.		
1	IE		Module interrupt enable	0	R/W
		0	Disable CAN interrupts. The interrupt line is always HIGH.		
		1	Enable CAN interrupts. The interrupt line is set to LOW and remains LOW until all pending interrupts are cleared.		
2	SIE		Status change interrupt enable	0	R/W
		0	Disable status change interrupts. No status change interrupt will be generated.		
		1	Enable status change interrupts. A status change interrupt will be generated when a message transfer is successfully completed or a CAN bus error is detected.		
3	EIE		Error interrupt enable	0	R/W
		0	Disable error interrupt. No error status interrupt will be generated.		
		1	Enable error interrupt. A change in the bits BOFF or EWARN in the CANSTAT registers will generate an interrupt.		
4	-	-	Reserved	0	-

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Table 753. CAN control registers (CNTL, address 0x400E 2000 (C_CAN0) and 0x400A 4000 (C_CAN1)) bit description
…continued

Bit	Symbol	Value	Description	Reset value	Access
5	DAR		Disable automatic retransmission	0	R/W
		0	Automatic retransmission of disturbed messages enabled.		
		1	Automatic retransmission disabled.		
6	CCE		Configuration change enable	0	R/W
		0	The CPU has no write access to the bit timing register.		
		1	The CPU has write access to the CANBT register while the INIT bit is one.		
7	TEST		Test mode enable	0	R/W
		0	Normal operation.		
		1	Test mode.		
31:8	-		reserved	-	-

Remark: The busoff recovery sequence (see *CAN Specification Rev. 2.0*) cannot be shortened by setting or resetting the INIT bit. If the device goes into busoff state, it will set INIT, stopping all bus activities. Once INIT has been cleared by the CPU, the device will then wait for 129 occurrences of Bus Idle (129 × 11 consecutive HIGH/recessive bits) before resuming normal operations. At the end of the busoff recovery sequence, the Error Management Counters will be reset.

During the waiting time after the resetting of INIT, each time a sequence of 11 HIGH/recessive bits has been monitored, a Bit0Error code is written to the Status Register CANSTAT, enabling the CPU to monitor the proceeding of the busoff recovery sequence and to determine whether the CAN bus is stuck at LOW/dominant or continuously disturbed.

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36.6.1.2 CAN status register

Table 754. CAN status register (STAT, address 0x400E 2004 (C_CAN0) and 0x400A 4004 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
2:0	LEC		Last error code Type of the last error to occur on the CAN bus.The LEC field holds a code which indicates the type of the last error to occur on the CAN bus. This field will be cleared to ‘0’ when a message has been transferred (reception or transmission) without error. The unused code ‘111’ may be written by the CPU to check for updates.	000	R/W
		0x0	**No error**.		
		0x1	**Stuff error**: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.		
		0x2	**Form error**: A fixed format part of a received frame has the wrong format.		
		0x3	**AckError**: The message this CAN core transmitted was not acknowledged.		
		0x4	**Bit1Error**: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a HIGH/recessive level (bit of logical value ‘1’), but the monitored bus value was LOW/dominant.		
		0x5	**Bit0Error**: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a LOW/dominant level (data or identifier bit logical value ‘0’), but the monitored Bus value was HIGH/recessive. During busoff recovery this status is set each time a sequence of 11 HIGH/recessive bits has been monitored. This enables the CPU to monitor the proceeding of the busoff recovery sequence (indicating the bus is not stuck at LOW/dominant or continuously disturbed).		
		0x6	**CRCError**: The CRC checksum was incorrect in the message received.		
		0x7	**Unused:** No CAN bus event was detected (written by the CPU).		
3	TXOK		Transmitted a message successfully This bit is reset by the CPU. It is never reset by the CAN controller.	0	R/W
		0	Since this bit was reset by the CPU, no message has been successfully transmitted.		
		1	Since this bit was last reset by the CPU, a message has been successfully transmitted (error free and acknowledged by at least one other node).		
4	RXOK		Received a message successfully This bit is reset by the CPU. It is never reset by the CAN controller.	0	R/W
		0	Since this bit was last reset by the CPU, no message has been successfully transmitted.		
		1	Since this bit was last set to zero by the CPU, a message has been successfully received independent of the result of acceptance filtering.		

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Table 754. CAN status register (STAT, address 0x400E 2004 (C_CAN0) and 0x400A 4004 (C_CAN1)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
5	EPASS		Error passive	0	RO
		0	The CAN controller is in the error active state.		
		1	The CAN controller is in the error passive state as defined in the *CAN 2.0 specification*.		
6	EWARN		Warning status	0	RO
		0	Both error counters are below the error warning limit of 96.		
		1	At least one of the error counters in the EML has reached the error warning limit of 96.		
7	BOFF		Busoff status	0	RO
		0	The CAN module is not in busoff state.		
		1	The CAN controller is in busoff state.		
31:8	-	-	reserved		

A status interrupt is generated by bits BOFF, EWARN, RXOK, TXOK, or LEC. BOFF and EWARN generate an error interrupt, and RXOK, TXOK, and LEC generate a status change interrupt if EIE and SIE respectively are set to enabled in the CANCTRL register.

A change of bit EPASS and a write to RXOK, TXOK, or LEC will never create a status interrupt.

Reading the CANSTAT register will clear the Status Interrupt value in the CANIR register.

36.6.1.3 CAN error counter

Table 755. CAN error counter (EC, address 0x400E 2008 (C_CAN0) and 0x400A 4008 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
7:0	TEC_7_0		Transmit error counter Current value of the transmit error counter (maximum value 127)	0	RO
14:8	REC_6_0		Receive error counter Current value of the receive error counter (maximum value 255).	0	RO
15	RP		Receive error passive	0	RO
		0	The receive counter is below the error passive level.		
		1	The receive counter has reached the error passive level as defined in the *CAN2.0 specification*.		
31:16	-	-	Reserved	-	-

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36.6.1.4 CAN bit timing register

Table 756. CAN bit timing register (BT, address 0x400E 200C (C_CAN0) and 0x400A 400C (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
5:0	BRP	Baud rate prescaler The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 63[1]. Valid programmed values are 0x01 - 0x3F[1].	1	R/W
7:6	SJW	(Re)synchronization jump width Valid programmed values are 0 to 3[1].	0	R/w
11:8	TSEG1	Time segment after the sample point Valid values are 0 to 7[1].	0011	R/W
14:12	TSEG2	Time segment before the sample point Valid values are 1 to 15[1].	010	R/W
31:15	-	Reserved	-	-

[1] Hardware interprets the value programmed into these bits as the bit value + 1.

Remark: With a module clock CAN_CLK of 8 MHz, the reset value of 0x2301 configures the C_CAN for a bit rate of 500 kBit/s. The registers are only writable if a configuration change is enabled in CANCTRL and the controller is initialized by software (bits CCE and INIT in the CAN Control Register are set).

36.6.1.5 CAN interrupt register

Table 757. CAN interrupt register (INT, address 0x400E 2010 (C_CAN0) and 0x400A 4010 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	INTID15_0	0x0000 = No interrupt is pending 0x0001 to 0x0020 = Number of message object which caused the interrupt. 0x0021 to 0x7FFF = Unused 0x8000 = Status interrupt 0x8001 to 0xFFFF = Unused	0	R
31:16	-	Reserved	-	-

If several interrupts are pending, the CAN Interrupt Register will point to the pending interrupt with the highest priority, disregarding their chronological order. An interrupt remains pending until the CPU has cleared it. If INTID is different from 0x0000 and IE is set, the interrupt line to the CPU is active. The interrupt line remains active until INTID is back to value 0x0000 (the cause of the interrupt is reset) or until IE is reset.

The Status Interrupt has the highest priority. Among the message interrupts, the Message Object' s interrupt priority decreases with increasing message number.

A message interrupt is cleared by clearing the Message Object's INTPND bit. The StatusInterrupt is cleared by reading the Status Register.

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36.6.1.6 CAN test register

Write access to the Test Register is enabled by setting bit Test in the CAN Control Register.

The different test functions may be combined, but when TX[1:0] ≠ “00” is selected, the message transfer is disturbed.

Table 758. CAN test register (TEST, address 0x400E 2014 (C_CAN0) and 0x400A 4014 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
1:0	-	-			-
2	BASIC		Basic mode	0	R/W
		0	Basic mode disabled.		
		1	IF1 registers used as TX buffer, IF2 registers used as RX buffer.		
3	SILENT		Silent mode	0	R/W
		0	Normal operation.		
		1	The module is in silent mode.		
4	LBACK		Loop back mode	0	R/W
		0	Loop back mode is disabled.		
		1	Loop back mode is enabled.		
6:5	TX1_0		Control of TD pins	00	R/W
		0x0	Level at the TD pin is controlled by the CAN controller. This is the value at reset.		
		0x1	The sample point can be monitored at the TD pin.		
		0x2	TD pin is driven LOW/dominant.		
		0x3	TD pin is driven HIGH/recessive.		
7	RX		Monitors the actual value of the RD Pin	0	R
		0	The CAN bus is dominant (RD = 0).		
		1	The CAN bus is recessive (RD = 1).		
31:8	-		Reserved		-

36.6.1.7 CAN baud rate prescaler extension register

Table 759. CAN baud rate prescaler extension register (BRPE, address 0x400E 2018 (C_CAN0) and 0x400A 4018 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
3:0	BRPE	Baud rate prescaler extension By programming BRPE the Baud Rate Prescaler can be extended to values up to 1023. Hardware interprets the value as the value of BRPE (MSBs) and BRP (LSBs) plus one. Allowed values are 0x00 to 0x0F	0x0000	R/W
31:4	-	Reserved	-	-

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36.6.2 Message interface registers

There are two sets of interface registers which are used to control the CPU access to the Message RAM. The interface registers avoid conflicts between CPU access to the Message RAM and CAN message reception and transmission by buffering the data to be transferred. A complete Message Object (see Section 36.6.2.1) or parts of the Message Object may be transferred between the Message RAM and the IFx Message Buffer registers in one single transfer.

The function of the two interface register sets is identical (except for test mode Basic). One set of registers may be used for data transfer to the Message RAM while the other set of registers may be used for the data transfer from the Message RAM, allowing both processes to be interrupted by each other.

Each set of interface registers consists of message buffer registers controlled by their own command registers. The command mask register specifies the direction of the data transfer and which parts of a message object will be transferred. The command request register is used to select a message object in the message RAM as target or source for the transfer and to start the action specified in the command mask register.

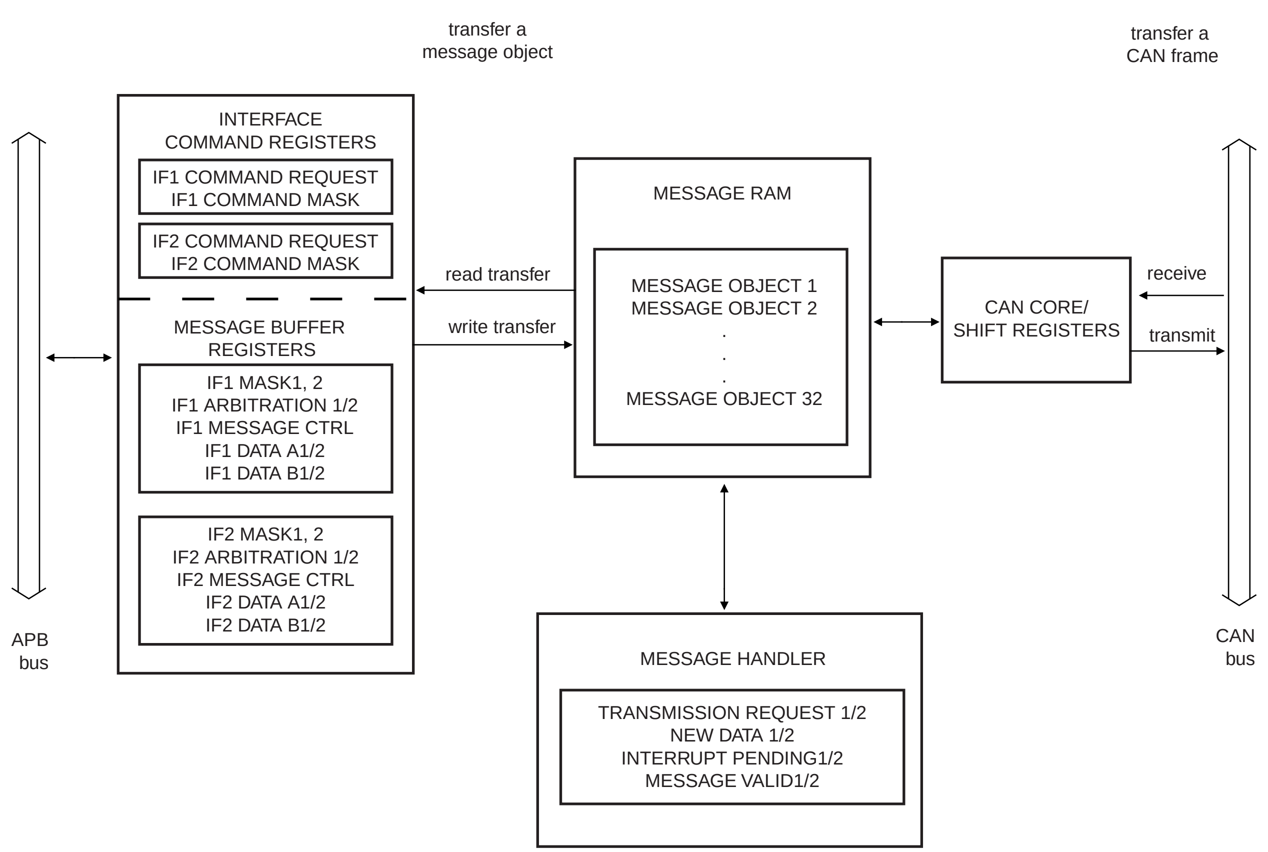


Fig 124. Block diagram of a message object transfer

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Table 760. Message interface registers

IF1 register names	IF1 register set	IF2 register names	IF2 register set
IF1_CMDREQ	IF1 command request	IF2_CMDREQ	IF2 command request
IF1_CMDMASK	IF1 command mask	IF2_CMDMASK	IF2 command mask
IF1_MASK1	IF1 mask 1	IF2_MSK1	IF2 mask 1
IF1_MASK2	IF1 mask 2	IF2_MSK2	IF2 mask 2
IF1_ARB1	IF1 arbitration 1	IF2_ARB1	IF2 arbitration 1
IF1_ARB2	IF1 arbitration 2	IF2_ARB2	IF2 arbitration 2
IF1_MCTRL	IF1 message control	IF2_MCTRL	IF2 message control
IF1_DA1	IF1 data A1	IF2_DA1	IF2 data A1
IF1_DA2	IF1 data A2	IF2_DA2	IF2 data A2
CIF1_DB1	IF1 data B1	IF2_DB1	IF2 data B1
IF1_DB2	IF1 data B2	IF2_DB2	IF2 data B2

There are 32 Message Objects in the Message RAM. To avoid conflicts between CPU access to the Message RAM and CAN message reception and transmission, the CPU cannot directly access the Message Objects. The message objects are accessed through the IFx Interface Registers.

36.6.2.1 Message objects

A message object contains the information from the various bits in the message interface registers. Table 761 below shows a schematic representation of the structure of the message object. The bits of a message object and the respective interface register where this bit is set or cleared are shown. For bit functions see the corresponding interface register.

Table 761. Structure of a message object in the message RAM

UMASK	MSK[28:0]	MXTD	MDIR	EOB	NEWDAT	MSGLST	RXIE	TXIE	INTPND
IF1/2_MCTRL	IF1/2_MSK1/2			IF1/2_MCTRL					

RMTEN	TXRQST	MSGVAL	ID[28:0]	XTD	DIR	DLC3	DLC2	DLC1	DLC0
IF1/2_MCTRL		IF1/2_ARB1/2				IF1/2_MCTRL			

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
IF1/2_DA1		IF1/2_DA2		IF1/2_DB1		IF1/2_DB2	

36.6.2.2 CAN message interface command request registers

A message transfer is started as soon as the CPU has written the message number to the Command Request Register. With this write operation the BUSY bit is automatically set to ‘1’ and the signal CAN_WAIT_B is pulled LOW) to notify the CPU that a transfer is in progress. After a wait time of 3 to 6 CAN_CLK periods, the transfer between the Interface Register and the Message RAM has completed. The BUSY bit is set back to zero and the signal CAN_WAIT_B is set back).

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Table 762. CAN message interface command request registers (IF1_CMDREQ, address 0x400E 2020 (C_CAN0) and 0x400A 4020 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
5:0	Message Number	Message number 0x01 to 0x20 = Valid message numbers The message object in the message RAM is selected for data transfer. 0x00 = Not a valid message number. This value is interpreted as 0x20.[1] 0x21 to 0x3F = Not a valid message number. This value is interpreted as 0x01 - 0x1F.[1]	0x01	R/W
14:6	-	Reserved		
15	BUSY	BUSY flag Set to one by hardware when writing to this Command request register. Set to zero by hardware when read/write action to this Command request register has finished.	0	R
31:16	-	Reserved	-	-

[1] When a message number that is not valid is written into the Command request registers, the message number will be transformed into a valid value and that message object will be transferred.

Table 763. CAN message interface command request registers (IF2_CMDREQ, address 0x400E 2080 (C_CAN0) and 0x400A 4080 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
5:0	Message Number	Message number 0x01 to 0x20 = Valid message numbers The message object in the message RAM is selected for data transfer. 0x00 = Not a valid message number. This value is interpreted as 0x20.[1] 0x21 to 0x3F = Not a valid message number. This value is interpreted as 0x01 - 0x1F.[1]	0x01	R/W
14:6	-	Reserved		
15	BUSY	BUSY flag Set to one by hardware when writing to this Command request register. Set to zero by hardware when read/write action to this Command request register has finished.	0	R
31:16	-	Reserved	-	-

[1] When a message number that is not valid is written into the Command request registers, the message number will be transformed into a valid value and that message object will be transferred.

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36.6.2.3 CAN message interface command mask registers

The control bits of the IFx Command Mask Register specify the transfer direction and select which of the IFx Message Buffer Registers are source or target of the data transfer.The functions of the register bits depend on the transfer direction (read or write) which is selected in the WR/RD bit (bit 7) of this Command mask register.

Select the WR/RD to

one for the Write transfer direction (write to message RAM)

zero for the Read transfer direction (read from message RAM)

Transfer direction Write

Table 764. CAN message interface command mask registers write direction (IF1_CMDMSK, address 0x400E 2024 (C_CAN0) and 0x400A 4024 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	DATA_B		Access data bytes 4-7	0	R/W
		0	Data bytes 4-7 unchanged.		
		1	Transfer data bytes 4-7 to message object.		
1	DATA_A		Access data bytes 0-3	0	R/W
		0	Data bytes 0-3 unchanged.		
		1	Transfer data bytes 0-3 to message object.		
2	TXRQST		Access transmission request bit	0	R/W
		0	No transmission request. TXRQSRT bit unchanged in IF1/2_MCTRL. **Remark:** If a transmission is requested by programming this bit, the TXRQST bit in the CANIFn_MCTRL register is ignored.		
		1	Request a transmission. Set the TXRQST bit IF1/2_MCTRL.		
3	CLRINTPND	-	This bit is ignored in the write direction.	0	R/W
4	CTRL		Access control bits	0	R/W
		0	Control bits unchanged.		
		1	Transfer control bits to message object		
5	ARB		Access arbitration bits	0	R/W
		0	Arbitration bits unchanged.		
		1	Transfer Identifier, DIR, XTD, and MSGVAL bits to message object.		

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Table 764. CAN message interface command mask registers write direction (IF1_CMDMSK, address 0x400E 2024 (C_CAN0) and 0x400A 4024 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
6	MASK		Access mask bits	0	R/W
		0	Mask bits unchanged.		
		1	Transfer Identifier MASK + MDIR + MXTD to message object.		
7	WR_RD	1	Write transfer Transfer data from the selected message buffer registers to the message object addressed by the command request register CANIFn_CMDREQ.	0	R/W
31:8	-	-	reserved	0	-

Table 765. CAN message interface command mask registers write direction (IF2_CMDMSK, address 0x400E 2084 (C_CAN0) and 0x400A 4080 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	DATA_B		Access data bytes 4-7	0	R/W
		0	Data bytes 4-7 unchanged.		
		1	Transfer data bytes 4-7 to message object.		
1	DATA_A		Access data bytes 0-3	0	R/W
		0	Data bytes 0-3 unchanged.		
		1	Transfer data bytes 0-3 to message object.		
2	TXRQST		Access transmission request bit	0	R/W
		0	No transmission request. TXRQSRT bit unchanged in IF1/2_MCTRL. **Remark:** If a transmission is requested by programming this bit, the TXRQST bit in the CANIFn_MCTRL register is ignored.		
		1	Request a transmission. Set the TXRQST bit IF1/2_MCTRL.		
3	CLRINTPND	-	This bit is ignored in the write direction.	0	R/W
4	CTRL		Access control bits	0	R/W
		0	Control bits unchanged.		
		1	Transfer control bits to message object		
5	ARB		Access arbitration bits	0	R/W
		0	Arbitration bits unchanged.		
		1	Transfer Identifier, DIR, XTD, and MSGVAL bits to message object.		

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Table 765. CAN message interface command mask registers write direction (IF2_CMDMSK, address 0x400E 2084 (C_CAN0) and 0x400A 4080 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
6	MASK		Access mask bits	0	R/W
		0	Mask bits unchanged.		
		1	Transfer Identifier MASK + MDIR + MXTD to message object.		
7	WR_RD	1	Write transfer Transfer data from the selected message buffer registers to the message object addressed by the command request register CANIFn_CMDREQ.	0	R/W
31:8	-	-	reserved	0	-

Transfer direction Read

Table 766. CAN message interface command mask registers read direction (IF1_CMDMSK, address 0x400E 2024 (C_CAN0) and 0x400A 4024 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	DATA_B		Access data bytes 4-7	0	R/W
		0	data bytes 4-7 unchanged.		
		1	Transfer data bytes 4-7 to IFx message buffer register.		
1	DATA_A		Access data bytes 0-3	0	R/W
		0	data bytes 0-3 unchanged.		
		1	Transfer data bytes 0-3 to IFx message buffer.		
2	NEWDAT		Access new data bit	0	R/W
		0	NEWDAT bit remains unchanged. **Remark:** A read access to a message object can be combined with the reset of the control bits INTPND and NEWDAT in IF1/2_MCTRL. The values of these bits transferred to the IFx Message Control Register always reflect the status before resetting these bits.		
		1	Clear NEWDAT bit in the message object.		
3	CLRINTPND		Clear interrupt pending bit.	0	R/W
		0	INTPND bit remains unchanged.		
		1	Clear INTPND bit in the message object.		
4	CTRL		Access control bits	0	R/W
		0	Control bits unchanged.		
		1	Transfer control bits to IFx message buffer.		
5	ARB		Access arbitration bits	0	R/W
		0	Arbitration bits unchanged.		
		1	Transfer Identifier, DIR, XTD, and MSGVAL bits to IFx message buffer register.		

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Table 766. CAN message interface command mask registers read direction (IF1_CMDMSK, address 0x400E 2024 (C_CAN0) and 0x400A 4024 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
6	MASK		Access mask bits	0	R/W
		0	Mask bits unchanged.		
		1	Transfer Identifier MASK + MDIR + MXTD to IFx message buffer register.		
7	WR_RD	0	Read transfer Transfer data from the message object addressed by the command request register to the selected message buffer registers CANIFn_CMDREQ.	0	R/W
31:8	-	-	reserved	0	-

Table 767. CAN message interface command mask registers read direction (IF2_CMDMSK, address 0x400E 2084 (C_CAN0) and 0x400A 4024 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	DATA_B		Access data bytes 4-7	0	R/W
		0	data bytes 4-7 unchanged.		
		1	Transfer data bytes 4-7 to IFx message buffer register.		
1	DATA_A		Access data bytes 0-3	0	R/W
		0	data bytes 0-3 unchanged.		
		1	Transfer data bytes 0-3 to IFx message buffer.		
2	NEWDAT		Access new data bit	0	R/W
		0	NEWDAT bit remains unchanged. **Remark:** A read access to a message object can be combined with the reset of the control bits INTPND and NEWDAT in IF1/2_MCTRL. The values of these bits transferred to the IFx Message Control Register always reflect the status before resetting these bits.		
		1	Clear NEWDAT bit in the message object.		
3	CLRINTPND		Clear interrupt pending bit.	0	R/W
		0	INTPND bit remains unchanged.		
		1	Clear INTPND bit in the message object.		
4	CTRL		Access control bits	0	R/W
		0	Control bits unchanged.		
		1	Transfer control bits to IFx message buffer.		
5	ARB		Access arbitration bits	0	R/W
		0	Arbitration bits unchanged.		
		1	Transfer Identifier, DIR, XTD, and MSGVAL bits to IFx message buffer register.		

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Table 767. CAN message interface command mask registers read direction (IF2_CMDMSK, address 0x400E 2084 (C_CAN0) and 0x400A 4024 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
6	MASK		Access mask bits	0	R/W
		0	Mask bits unchanged.		
		1	Transfer Identifier MASK + MDIR + MXTD to IFx message buffer register.		
7	WR_RD	0	Read transfer Transfer data from the message object addressed by the command request register to the selected message buffer registers CANIFn_CMDREQ.	0	R/W
31:8	-	-	reserved	0	-

36.6.2.4 IF1 and IF2 message buffer registers

The bits of the Message Buffer registers mirror the Message Objects in the Message RAM.

36.6.2.4.1 CAN message interface command mask 1 registers

Table 768. CAN message interface command mask 1 registers (IF1_MSK1, address 0x400E 2028 (C_CAN0) and 0x400A 4028 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	MSK15_0	Identifier mask 0 = The corresponding bit in the identifier of the message can not inhibit the match in the acceptance filtering. 1 = The corresponding identifier bit is used for acceptance filtering.	0xFFFF	R/W
31:16	-	reserved	0	-

Table 769. CAN message interface command mask 1 registers (IF2_MSK1, address 0x400E 2088 (C_CAN0) and 0x400A 4028 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	MSK15_0	Identifier mask 0 = The corresponding bit in the identifier of the message can not inhibit the match in the acceptance filtering. 1 = The corresponding identifier bit is used for acceptance filtering.	0xFFFF	R/W
31:16	-	reserved	0	-

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36.6.2.4.2 CAN message interface command mask 2 registers

Table 770. CAN message interface command mask 2 registers (IF1_MSK2, address 0x400E 202C (C_CAN0) and 0x400A 402C (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
12:0	MSK28_16		Identifier mask 0 = The corresponding bit in the identifier of the message can not inhibit the match in the acceptance filtering. 1 = The corresponding identifier bit is used for acceptance filtering.	0xFFF	R/W
13	-		Reserved	1	-
14	MDIR		Mask message direction	1	R/W
		0	The message direction bit (DIR) has no effect on acceptance filtering.		
		1	The message direction bit (DIR) is used for acceptance filtering.		
15	MXTD		Mask extend identifier	1	R/W
		0	The extended identifier bit (IDE) has no effect on acceptance filtering.		
		1	The extended identifier bit (IDE) is used for acceptance filtering.		
31:16	-	-	Reserved	0	-

Table 771. CAN message interface command mask 2 registers (IF2_MSK2, 0x400E 208C (C_CAN0) and 0x400A 402C (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
12:0	MSK28_16		Identifier mask 0 = The corresponding bit in the identifier of the message can not inhibit the match in the acceptance filtering. 1 = The corresponding identifier bit is used for acceptance filtering.	0xFFF	R/W
13	-		Reserved	1	-
14	MDIR		Mask message direction	1	R/W
		0	The message direction bit (DIR) has no effect on acceptance filtering.		
		1	The message direction bit (DIR) is used for acceptance filtering.		
15	MXTD		Mask extend identifier	1	R/W
		0	The extended identifier bit (IDE) has no effect on acceptance filtering.		
		1	The extended identifier bit (IDE) is used for acceptance filtering.		
31:16	-	-	Reserved	0	-

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36.6.2.4.3 CAN message interface command arbitration 1 registers

Table 772. CAN message interface command arbitration 1 registers (IF1_ARB1, address 0x400E 2030 (C_CAN0) and 0x400A 4030 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	ID15_0	Message identifier 29-bit identifier (“extended frame”) 11-bit identifier (“standard frame”)	0x00	R/W
31:16	-	Reserved	0	-

Table 773. CAN message interface command arbitration 1 registers (IF2_ARB1, address 0x400E 2090 (C_CAN0) and 0x400A 4090 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	ID15_0	Message identifier 29-bit identifier (“extended frame”) 11-bit identifier (“standard frame”)	0x00	R/W
31:16	-	Reserved	0	-

36.6.2.4.4 CAN message interface command arbitration 2 registers

Table 774. CAN message interface command arbitration 2 registers (IF1_ARB2, address 0x400E 2034 (C_CAN0) and 0x400A 4034 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
12:0	ID28_16		Message identifier 29-bit identifier (“extended frame”) 11-bit identifier (“standard frame”)	0x00	R/W
13	DIR		Message direction	0x00	R/W
		0	Direction = receive. On TXRQST, a Remote Frame with the identifier of this Message Object is transmitted. On reception of a Data Frame with matching identifier, that message is stored in this Message Object.		
		1	Direction = transmit. On TXRQST, the respective Message Object is transmitted as a Data Frame. On reception of a Remote Frame with matching identifier, the TXRQST bit of this Message Object is set (if RMTEN = one).		
14	XTD		Extend identifier	0x00	R/W
		0	The 11-bit standard identifier will be used for this message object.		
		1	The 29-bit extended identifier will be used for this message object.		

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Table 774. CAN message interface command arbitration 2 registers (IF1_ARB2, address 0x400E 2034 (C_CAN0) and 0x400A 4034 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
15	MSGVAL		Message valid **Remark:** The MSGVAL bit of all unused Messages Objects is reset during the initialization before bit INIT is reset in the CAN Control Register. This bit must be set to zero before the identifier ID28:0, the control bits XTD, DIR, or the Data Length Code DLC3:0 are modified, or if the Messages Object is no longer required.	0	R/W
		0	The message object is ignored by the message handler.		
		1	The message object is configured and should be considered by the message handler.		
31:16	-	-	Reserved	0	-

Table 775. CAN message interface command arbitration 2 registers (IF2_ARB2, address 0x400E 2094 (C_CAN0) and 0x400A 4094 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
12:0	ID28_16		Message identifier 29-bit identifier (“extended frame”) 11-bit identifier (“standard frame”)	0x00	R/W
13	DIR		Message direction	0x00	R/W
		0	Direction = receive. On TXRQST, a Remote Frame with the identifier of this Message Object is transmitted. On reception of a Data Frame with matching identifier, that message is stored in this Message Object.		
		1	Direction = transmit. On TXRQST, the respective Message Object is transmitted as a Data Frame. On reception of a Remote Frame with matching identifier, the TXRQST bit of this Message Object is set (if RMTEN = one).		
14	XTD		Extend identifier	0x00	R/W
		0	The 11-bit standard identifier will be used for this message object.		
		1	The 29-bit extended identifier will be used for this message object.		

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Table 775. CAN message interface command arbitration 2 registers (IF2_ARB2, address 0x400E 2094 (C_CAN0) and 0x400A 4094 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
15	MSGVAL		Message valid **Remark:** The MSGVAL bit of all unused Messages Objects is reset during the initialization before bit INIT is reset in the CAN Control Register. This bit must be set to zero before the identifier ID28:0, the control bits XTD, DIR, or the Data Length Code DLC3:0 are modified, or if the Messages Object is no longer required.	0	R/W
		0	The message object is ignored by the message handler.		
		1	The message object is configured and should be considered by the message handler.		
31:16	-	-	Reserved	0	-

36.6.2.4.5 CAN message interface message control registers

Table 776. CAN message interface message control registers (IF1_MCTRL, address 0x400E 2038 (C_CAN0) and 0x400A 4038 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
3:0	DLC3_0		Data length code **Remark:** The Data Length Code of a Message Object must be defined the same as in all the corresponding objects with the same identifier at other nodes. When the Message Handler stores a data frame, it will write the DLC to the value given by the received message. 0000 to 1000 = Data frame has 0 - 8 data bytes. 1001 to 1111 = Data frame has 8 data bytes.	0000	R/W
6:4	-		reserved	-	-
7	EOB		End of buffer	0	R/W
		0	Message object belongs to a FIFO buffer and is not the last message object of that FIFO buffer.		
		1	Single message object or last message object of a FIFO buffer.		
8	TXRQST		Transmit request	0	R/W
		0	This message object is not waiting for transmission.		
		1	The transmission of this message object is requested and is not yet done		
9	RMTEN		Remote enable	0	R/W
		0	At the reception of a remote frame, TXRQST is left unchanged.		
		1	At the reception of a remote frame, TXRQST is set.		

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Table 776. CAN message interface message control registers (IF1_MCTRL, address 0x400E 2038 (C_CAN0) and 0x400A 4038 (C_CAN1)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
10	RXIE		Receive interrupt enable	0	R/W
		0	INTPND will be left unchanged after successful reception of a frame.		
		1	INTPND will be set after successful reception of a frame.		
11	TXIE		Transmit interrupt enable	0	R/W
		0	The INTPND bit will be left unchanged after a successful reception of a frame.		
		1	INTPND will be set after a successful reception of a frame.		
12	UMASK		Use acceptance mask **Remark:** If UMASK is set to 1, the message object's mask bits have to be programmed during initialization of the message object before MAGVAL is set to 1.	0	R/W
		0	Mask ignored.		
		1	Use mask (MSK[28:0], MXTD, and MDIR) for acceptance filtering.		
13	INTPND		Interrupt pending	0	R/W
		0	This message object is not the source of an interrupt.		
		1	This message object is the source of an interrupt. The Interrupt Identifier in the Interrupt Register will point to this message object if there is no other interrupt source with higher priority.		
14	MSGLST		Message lost (only valid for message objects in the direction receive).	0	R/W
		0	No message lost since this bit was reset last by the CPU.		
		1	The Message Handler stored a new message into this object when NEWDAT was still set, the CPU has lost a message.		
15	NEWDAT		New data	0	R/W
		0	No new data has been written into the data portion of this message object by the message handler since this flag was cleared last by the CPU.		
		1	The message handler or the CPU has written new data into the data portion of this message object.		
31:16	-	-	Reserved	0	-

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Table 777. CAN message interface message control registers (IF2_MCTRL, address 0x400E 2098 (C_CAN0) and 0x400A 4098 (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
3:0	DLC3_0		Data length code **Remark:** The Data Length Code of a Message Object must be defined the same as in all the corresponding objects with the same identifier at other nodes. When the Message Handler stores a data frame, it will write the DLC to the value given by the received message. 0000 to 1000 = Data frame has 0 - 8 data bytes. 1001 to 1111 = Data frame has 8 data bytes.	0000	R/W
6:4	-		reserved	-	-
7	EOB		End of buffer	0	R/W
		0	Message object belongs to a FIFO buffer and is not the last message object of that FIFO buffer.		
		1	Single message object or last message object of a FIFO buffer.		
8	TXRQST		Transmit request	0	R/W
		0	This message object is not waiting for transmission.		
		1	The transmission of this message object is requested and is not yet done		
9	RMTEN		Remote enable	0	R/W
		0	At the reception of a remote frame, TXRQST is left unchanged.		
		1	At the reception of a remote frame, TXRQST is set.		
10	RXIE		Receive interrupt enable	0	R/W
		0	INTPND will be left unchanged after successful reception of a frame.		
		1	INTPND will be set after successful reception of a frame.		
11	TXIE		Transmit interrupt enable	0	R/W
		0	The INTPND bit will be left unchanged after a successful reception of a frame.		
		1	INTPND will be set after a successful reception of a frame.		
12	UMASK		Use acceptance mask **Remark:** If UMASK is set to 1, the message object's mask bits have to be programmed during initialization of the message object before MAGVAL is set to 1.	0	R/W
		0	Mask ignored.		
		1	Use mask (MSK[28:0], MXTD, and MDIR) for acceptance filtering.		

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Table 777. CAN message interface message control registers (IF2_MCTRL, address 0x400E 2098 (C_CAN0) and 0x400A 4098 (C_CAN1)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
13	INTPND		Interrupt pending	0	R/W
		0	This message object is not the source of an interrupt.		
		1	This message object is the source of an interrupt. The Interrupt Identifier in the Interrupt Register will point to this message object if there is no other interrupt source with higher priority.		
14	MSGLST		Message lost (only valid for message objects in the direction receive).	0	R/W
		0	No message lost since this bit was reset last by the CPU.		
		1	The Message Handler stored a new message into this object when NEWDAT was still set, the CPU has lost a message.		
15	NEWDAT		New data	0	R/W
		0	No new data has been written into the data portion of this message object by the message handler since this flag was cleared last by the CPU.		
		1	The message handler or the CPU has written new data into the data portion of this message object.		
31:16	-	-	Reserved	0	-

36.6.2.4.6 CAN message interface data A1 registers

In a CAN Data Frame, DATA0 is the first, DATA7 (in CAN_IF1B2 AND CAN_IF2B2) is the last byte to be transmitted or received. In CAN's serial bit stream, the MSB of each byte will be transmitted first.

Remark: Byte DATA0 is the first data byte shifted into the shift register of the CAN Core during a reception, byte DATA7 is the last. When the Message Handler stores a Data Frame, it will write all the eight data bytes into a Message Object. If the Data Length Code is less than 8, the remaining bytes of the Message Object will be overwritten by non specified values.

Table 778. CAN message interface data A1 registers (IF1_DA1, address 0x400E 203C (C_CAN0) and 0x400A 403C (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
7:0	DATA0	Data byte 0	0x00	R/W
15:8	DATA1	Data byte 1	0x00	R/W
31:16	-	Reserved	-	-

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Table 779. CAN message interface data A1 registers (IF2_DA1, address 0x400E 209C (C_CAN0) and 0x400A 409C (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
7:0	DATA0	Data byte 0	0x00	R/W
15:8	DATA1	Data byte 1	0x00	R/W
31:16	-	Reserved	-	-

36.6.2.4.7 CAN message interface data A2 registers

Table 780. CAN message interface data A2 registers (IF1_DA2, address 0x400E 2040 (C_CAN0) and 0x400A 4040 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
7:0	DATA2	Data byte 2	0x00	R/W
15:8	DATA3	Data byte 3	0x00	R/W
31:16	-	Reserved	-	-

Table 781. CAN message interface data A2 registers (IF2_DA2, address 0x400E 20A0 (C_CAN0) and 0x400A 40A0 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
7:0	DATA2	Data byte 2	0x00	R/W
15:8	DATA3	Data byte 3	0x00	R/W
31:16	-	Reserved	-	-

36.6.2.4.8 CAN message interface data B1 registers

Table 782. CAN message interface data B1 registers (IF1_DB1, address 0x400E 2044 (C_CAN0) and 0x400A 4044 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
7:0	DATA4	Data byte 4	0x00	R/W
15:8	DATA5	Data byte 5	0x00	R/W
31:16	-	Reserved	-	-

Table 783. CAN message interface data B1 registers (IF2_DB1, address 0x400E 20A4 (C_CAN0) and 0x400A 40A4 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
7:0	DATA4	Data byte 4	0x00	R/W
15:8	DATA5	Data byte 5	0x00	R/W
31:16	-	Reserved	-	-

36.6.2.4.9 CAN message interface data B2 registers

Table 784. CAN message interface data B2 registers (IF1_DB2, address 0x400E 2048 (C_CAN0) and 0x400A 4048 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
7:0	DATA6	Data byte 6	0x00	R/W
15:8	DATA7	Data byte 7	0x00	R/W
31:16	-	Reserved	-	-

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Table 785. CAN message interface data B2 registers (IF2_DB2, address 0x400E 20A8 (C_CAN0) and 0x400A 40A8 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
7:0	DATA6	Data byte 6	0x00	R/W
15:8	DATA7	Data byte 7	0x00	R/W
31:16	-	Reserved	-	-

36.6.3 Message handler registers

All Message Handler registers are read-only. Their contents (TXRQST, NEWDAT, INTPND, and MSGVAL bits of each Message Object and the Interrupt Identifier) is status information provided by the Message Handler FSM.

36.6.3.1 CAN transmission request 1 register

This register contains the TXRQST bits of message objects 1 to 16. By reading out the TXRQST bits, the CPU can check for which Message Object a Transmission Request is pending. The TXRQST bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers or by the Message Handler after reception of a Remote Frame or after a successful transmission.

Table 786. CAN transmission request 1 register (TXREQ1, address 0x400E 2100 (C_CAN0) and 0x400A 4100 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	TXRQST16_1	Transmission request bit of message objects 16 to 1. 0 = This message object is not waiting for transmission. 1 = The transmission of this message object is requested and not yet done.	0x00	R
31:16	-	Reserved	-	-

36.6.3.2 CAN transmission request 2 register

This register contains the TXRQST bits of message objects 32 to 17. By reading out the TXRQST bits, the CPU can check for which Message Object a Transmission Request is pending. The TXRQST bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers or by the Message Handler after reception of a Remote Frame or after a successful transmission.

Table 787. CAN transmission request 2 register (TXREQ2, address 0x400E 2104 (C_CAN0) and 0x400A 4104 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	TXRQST32_17	Transmission request bit of message objects 32 to 17. 0 = This message object is not waiting for transmission. 1 = The transmission of this message object is requested and not yet done.	0x00	R
31:16	-	Reserved	-	-

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36.6.3.3 CAN new data 1 register

This register contains the NEWDAT bits of message objects 16 to 1. By reading out the NEWDAT bits, the CPU can check for which Message Object the data portion was updated. The NEWDAT bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers or by the Message Handler after reception of a Data Frame or after a successful transmission.

Table 788. CAN new data 1 register (ND1, address 0x400E 2120 (C_CAN0) and 0x400A 4120 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	NEWDAT16_1	New data bits of message objects 16 to 1. 0 = No new data has been written into the data portion of this Message Object by the Message Handler since last time this flag was cleared by the CPU. 1 = The Message Handler or the CPU has written new data into the data portion of this Message Object.	0x00	R
31:16	-	Reserved	-	-

36.6.3.4 CAN new data 2 register

This register contains the NEWDAT bits of message objects 32 to 17. By reading out the NEWDAT bits, the CPU can check for which Message Object the data portion was updated. The NEWDAT bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers or by the Message Handler after reception of a Data Frame or after a successful transmission.

Table 789. CAN new data 2 register (ND2, address 0x400E 2124 (C_CAN0) and 0x400A 4124 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	NEWDAT32_17	New data bits of message objects 32 to 17. 0 = No new data has been written into the data portion of this Message Object by the Message Handler since last time this flag was cleared by the CPU. 1 = The Message Handler or the CPU has written new data into the data portion of this Message Object.	0x00	R
31:16	-	Reserved	-	-

36.6.3.5 CAN interrupt pending 1 register

This register contains the INTPND bits of message objects 16 to 1. By reading out the INTPND bits, the CPU can check for which Message Object an interrupt is pending. The INTPND bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers or by the Message Handler after reception or after a successful transmission of a frame. This will also affect the value of INTPND in the Interrupt Register.

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Table 790. CAN interrupt pending 1 register (IR1, address 0x400E 2140 (C_CAN0) and 0x400A 4140 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	INTPND16_1	Interrupt pending bits of message objects 16 to 1. 0 = This message object is ignored by the message handler. 1 = This message object is the source of an interrupt.	0x00	R
31:16	-	Reserved	-	-

36.6.3.6 CAN interrupt pending 2 register

This register contains the INTPND bits of message objects 32 to 17. By reading out the INTPND bits, the CPU can check for which Message Object an interrupt is pending. The INTPND bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers or by the Message Handler after reception or after a successful transmission of a frame. This will also affect the value of INTPND in the Interrupt Register.

Table 791. CAN interrupt pending 2 register (IR2, addresses 0x400E 2144 (C_CAN0) and 0x400A 4144 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	INTPND32_17	Interrupt pending bits of message objects 32 to 17. 0 = This message object is ignored by the message handler. 1 = This message object is the source of an interrupt.	0x00	R
31:16	-	Reserved	-	-

36.6.3.7 CAN message valid 1 register

This register contains the MSGVAL bits of message objects 16 to 1. By reading out the MSGVAL bits, the CPU can check which Message Object is valid. The MSGVAL bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers.

Table 792. CAN message valid 1 register (MSGV1, addresses 0x400E 2160 (C_CAN0) and 0x400A 4160 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	MSGVAL16_1	Message valid bits of message objects 16 to 1. 0 = This message object is ignored by the message handler. 1 = This message object is configured and should be considered by the message handler.	0x00	R
31:16	-	Reserved	-	-

36.6.3.8 CAN message valid 2 register

This register contains the MSGVAL bits of message objects 32 to 17. By reading out the MSGVAL bits, the CPU can check which Message Object is valid. The MSGVAL bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers.

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Table 793. CAN message valid 2 register (MSGV2, address 0x400E 2164 (C_CAN0) and 0x400A 4164 (C_CAN1)) bit description

Bit	Symbol	Description	Access	Reset value
15:0	MSGVAL32_17	Message valid bits of message objects 32 to 17. 0 = This message object is ignored by the message handler. 1 = This message object is configured and should be considered by the message handler.	R	0x00
31:16	-	Reserved	-	-

36.6.4 CAN timing register

36.6.4.1 CAN clock divider register

This register determines the CAN clock signal. The CAN_CLK is derived from the peripheral clock PCLK divided by the values in this register.

Table 794. CAN clock divider register (CLKDIV, address 0x400E 2180 (C_CAN0) and 0x400A 4180 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
3:0	CLKDIVVAL	Clock divider value CAN_CLK = PCLK/($2^{CLKDIVVAL\ -1}$+1) 0000: CAN_CLK = PCLK divided by 1. 0001: CAN_CLK = PCLK divided by 2. 0010: CAN_CLK = PCLK divided by 3. 0010: CAN_CLK = PCLK divided by 4. 0011: CAN_CLK = PCLK divided by 5. 0100: CAN_CLK = PCLK divided by 9. 0101: CAN_CLK = PCLK divided by 17. ... 1111: CAN_CLK = PCLK divided by 16385.	0000	R/W
31:4	-	reserved	-	-

36.7 Functional description

36.7.1 C_CAN controller state after reset

After a hardware reset, the registers hold the values described in Table 751. Additionally, the busoff state is reset and the output CAN_TXD is set to recessive (HIGH). The value 0x0001 (INIT = ‘1’) in the CAN Control Register enables the software initialization. The CAN controller does not communicate with the CAN bus until the CPU resets INIT to ‘0’.

The data stored in the message RAM is not affected by a hardware reset. After power-on, the contents of the message RAM is undefined.

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36.7.2 C_CAN operating modes

36.7.2.1 Software initialization

The software initialization is started by setting the bit INIT in the CAN Control Register, either by software or by a hardware reset, or by entering the busoff state.

During software initialization (INIT bit is set), the following conditions are present:

- All message transfer from and to the CAN bus is stopped.
- The status of the CAN output CAN_TXD is recessive (HIGH).
- The EML counters are unchanged.
- The configuration registers are unchanged.
- Access to the bit timing register and the BRP extension register is enabled if the CCE bit in the CAN control register is also set.

To initialize the CAN controller, software has to set up the bit timing register and each message object. If a message object is not needed, it is sufficient to set its MSGVAL bit to not valid. Otherwise, the whole message object has to be initialized.

Resetting the INIT bit finishes the software initialization. Afterwards the Bit Stream Processor BSP synchronizes itself to the data transfer on the CAN bus by waiting for the occurrence of a sequence of 11 consecutive recessive bits (Bus Idle) before it can take part in bus activities and starts the message transfer.

Remark: The initialization of the Message Objects is independent of INIT and also can be done on the fly, but the Message Objects should all be configured to particular identifiers or set to not valid during software initialization before the BSP starts the message transfer. To change the configuration of a Message Object during normal operation, the CPU has to start by setting the MSGVAL bit to not valid. When the configuration is completed, MSAGVALis set to valid again.

36.7.2.2 CAN message transfer

Once the CAN controller is initialized and INIT is reset to zero, the CAN core synchronizes itself to the CAN bus and starts the message transfer.

Received messages are stored into their appropriate Message Objects if they pass the Message Handler's acceptance filtering. The whole message including all arbitration bits, DLC and eight data bytes is stored into the Message Object. If the Identifier Mask is used, the arbitration bits which are masked to “don't care” may be overwritten in the Message Object.

The CPU may read or write each message any time via the Interface Registers. The Message Handler guarantees data consistency in case of concurrent accesses.

Messages to be transmitted are updated by the CPU. If a permanent Message Object (arbitration and control bits set up during configuration) exists for the message, only the data bytes are updated and then TXRQUT bit with NEWDAT bit are set to start the transmission. If several transmit messages are assigned to the same Message Object (when the number of Message Objects is not sufficient), the whole Message Object has to be configured before the transmission of this message is requested.

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The transmission of any number of Message Objects may be requested at the same time, and they are transmitted subsequently according to their internal priority. Messages may be updated or set to not valid any time, even when their requested transmission is still pending. The old data will be discarded when a message is updated before its pending transmission has started.

Depending on the configuration of the Message Object, the transmission of a message may be requested autonomously by the reception of a remote frame with a matching identifier.

36.7.2.3 Disabled Automatic Retransmission (DAR)

According to the *CAN Specification (ISO11898, 6.3.3 Recovery Management)*, the CAN controller provides means for automatic retransmission of frames that have lost arbitration or that have been disturbed by errors during transmission. The frame transmission service will not be confirmed to the user before the transmission is successfully completed. By default, the automatic retransmission on lost arbitration or error is enabled. It can be disabled to enable the CAN controller to work within a Time Triggered CAN (TTCAN, see ISO11898-1) environment.

The Disable Automatic Retransmission mode is enabled by programming bit DAR in the CAN Control Register to one. In this operation mode the programmer has to consider the different behavior of bits TXRQST and NEWDAT in the Control Registers of the Message Buffers:

- When a transmission starts, bit TXRQST of the respective Message Buffer is reset while bit NEWDAT remains set.
- When the transmission completed successfully, bit NEWDAT is reset.
- When a transmission failed (lost arbitration or error), bit NEWDAT remains set. To restart the transmission, the CPU has to set TXRQST back to one.

36.7.2.4 Test modes

The Test mode is entered by setting bit TEST in the CAN Control Register to one. In Test mode the bits TX1, TX0, LBACK, SILENT, and BASIC in the Test Register are writable. Bit RX monitors the state of pins RD0,1 and therefore is only readable. All Test register functions are disabled when bit TEST is reset to zero.

36.7.2.4.1 Silent mode

The CAN core can be set in Silent mode by programming the Test register bit SILENT to one.

In Silent Mode, the CAN controller is able to receive valid data frames and valid remote frames, but it sends only recessive bits on the CAN bus, and it cannot start a transmission. If the CAN Core is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is rerouted internally so that the CAN Core monitors this dominant bit, although the CAN bus may remain in recessive state. The Silent mode can be used to analyze the traffic on a CAN bus without affecting it by the transmission of dominant bits (Acknowledge Bits, Error Frames).

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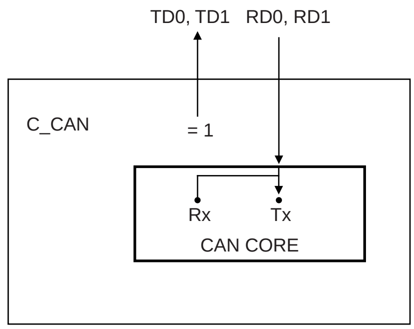


Fig 125. CAN core in Silent mode

36.7.2.4.2 Loop-back mode

The CAN Core can be set in Loop-back mode by programming the Test Register bit LBACK to one. In Loop-back Mode, the CAN Core treats its own transmitted messages as received messages and stores them (if they pass acceptance filtering) into a Receive Buffer.

This mode is provided for self-test functions. To be independent from external stimulation, the CAN Core ignores acknowledge errors (recessive bit sampled in the acknowledge slot of a data/remote frame) in Loop-back mode. In this mode the CAN core performs an internal feedback from its CAN_TXD output to its CAN_RXD input. The actual value of the CAN_RXD input pin is disregarded by the CAN Core. The transmitted messages can be monitored at the CAN_TXD pin.

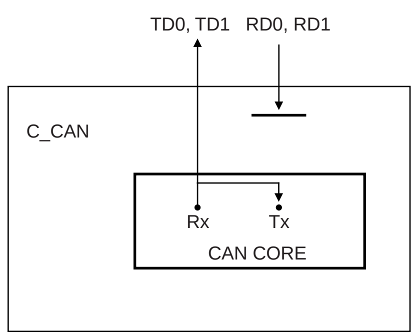


Fig 126. CAN core in Loop-back mode

36.7.2.4.3 Loop-back mode combined with Silent mode

It is also possible to combine Loop-back mode and Silent mode by programming bits LBACK and SILENT to one at the same time. This mode can be used for a “Hot Selftest”, meaning the C_CAN can be tested without affecting a running CAN system connected to the pins CAN_TXD and CAN_RXD. In this mode the CAN_RXD pin is disconnected from the CAN Core and the CAN_TXD pin is held recessive.

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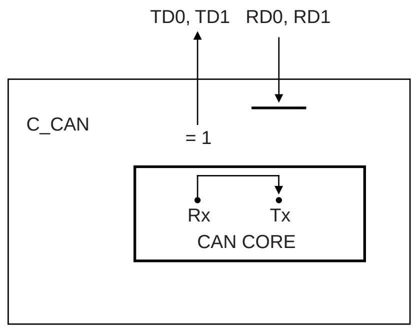


Fig 127. CAN core in Loop-back mode combined with Silent mode

36.7.2.4.4 Basic mode

The CAN Core can be set in Basic mode by programming the Test Register bit BASIC to one. In this mode the CAN controller runs without the Message RAM.

The IF1 Registers are used as Transmit Buffer. The transmission of the contents of the IF1 Registers is requested by writing the BUSY bit of the IF1 Command Request Register to ‘1’. The IF1 Registers are locked while the BUSY bit is set. The BUSY bit indicates that the transmission is pending.

As soon the CAN bus is idle, the IF1 Registers are loaded into the shift register of the CAN Core and the transmission is started. When the transmission has completed, the BUSY bit is reset and the locked IF1 Registers are released.

A pending transmission can be aborted at any time by resetting the BUSY bit in the IF1 Command Request Register while the IF1 Registers are locked. If the CPU has reset the BUSY bit, a possible retransmission in case of lost arbitration or in case of an error is disabled.

The IF2 Registers are used as Receive Buffer. After the reception of a message the contents of the shift register is stored into the IF2 Registers, without any acceptance filtering.

Additionally, the actual contents of the shift register can be monitored during the message transfer. Each time a read Message Object is initiated by writing the BUSY bit of the IF2 Command Request Register to ‘1’, the contents of the shift register is stored into the IF2 Registers.

In Basic mode the evaluation of all Message Object related control and status bits and of the control bits of the IFx Command Mask Registers is turned off. The message number of the Command request registers is not evaluated. The NEWDAT and MSGLST bits of the IF2 Message Control Register retain their function, DLC3-0 will show the received DLC, the other control bits will be read as ‘0’.

In Basic mode the ready output CAN_WAIT_B is disabled (always ‘1’)

36.7.2.4.5 Software control of pin CAN_TXD

Four output functions are available for the CAN transmit pin CAN_TXD:

1. serial data output (default).

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2. drives CAN sample point signal to monitor the CAN controller's timing.
3. drives recessive constant value.
4. drives dominant constant value.

The last two functions, combined with the readable CAN receive pin CAN_RXD, can be used to check the CAN bus' physical layer.

The output mode of pin CAN_TXD is selected by programming the Test Register bits TX1 and TX0 as described Section 36.6.1.6.

Remark: The three test functions for pin CAN_TXD interfere with all CAN protocol functions. The CAN_TXD pin must be left in its default function when CAN message transfer or any of the test modes Loo-back mode, Silent mode, or Basic mode are selected.

36.7.3 CAN message handler

The Message handler controls the data transfer between the Rx/Tx Shift Register of the CAN Core, the Message RAM and the IFx Registers, see Figure 124.

The message handler controls the following functions:

- Data Transfer between IFx Registers and the Message RAM
- Data Transfer from Shift Register to the Message RAM
- Data Transfer from Message RAM to Shift Register
- Data Transfer from Shift Register to the Acceptance Filtering unit
- Scanning of Message RAM for a matching Message Object
- Handling of TXRQST flags
- Handling of interrupts

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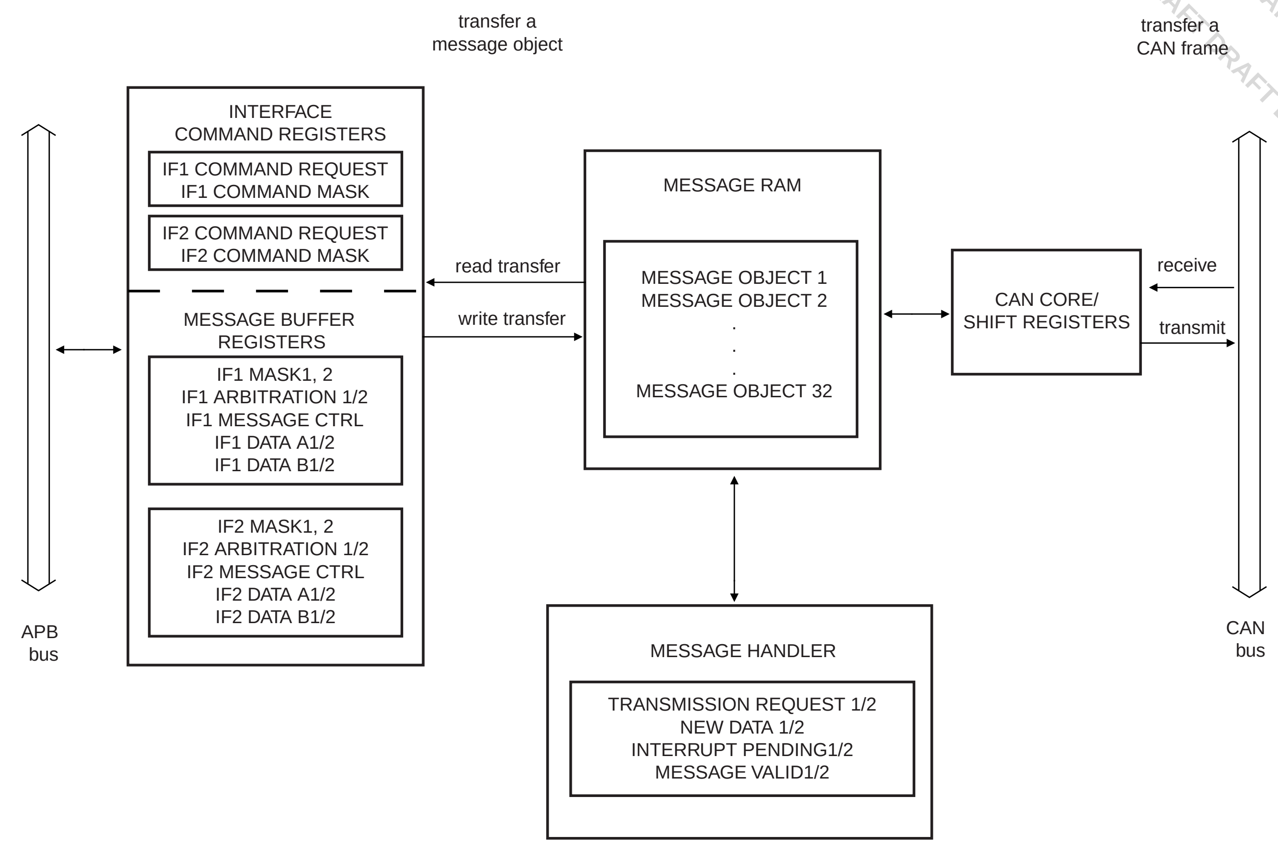


Fig 128. Block diagram of a message object transfer

36.7.3.1 Management of message objects

The configuration of the Message Objects in the Message RAM will (with the exception of the bits MSGVAL, NEWDAT, INTPND, and TXRQST) is not be affected by resetting the chip. All the Message Objects must be initialized by the CPU or they must be set to not valid (MSGVAL = ‘0’).The bit timing must be configured before the CPU clears the INIT bit in the CAN Control Register.

The configuration of a Message Object is done by programming Mask, Arbitration, Control and Data field of one of the two interface register sets to the desired values. By writing to the corresponding IFx Command Request Register, the IFx Message Buffer Registers are loaded into the addressed Message Object in the Message RAM.

When the INIT bit in the CAN Control Register is cleared, the CAN Protocol Controller state machine of the CAN core and the Message Handler State Machine control the CAN controller’s internal data flow. Received messages that pass the acceptance filtering are stored into the Message RAM, and messages with pending transmission request are loaded into the CAN core’s shift register and are transmitted via the CAN bus.

The CPU reads received messages and updates messages to be transmitted via the IFx Interface Registers. Depending on the configuration, the CPU is interrupted on certain CAN message and CAN error events.

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36.7.3.2 Data Transfer between IFx Registers and the Message RAM

When the CPU initiates a data transfer between the IFx Registers and Message RAM, the Message Handler sets the BUSY bit in the respective Command Register to ‘1’. After the transfer has completed, the BUSY bit is set back to ‘0’.

The Command Mask Register specifies whether a complete Message Object or only parts of it will be transferred. Due to the structure of the Message RAM it is not possible to write single bits/bytes of one Message Object. Software must always write a complete Message Object into the Message RAM. Therefore the data transfer from the IFx Registers to the Message RAM requires a read-modify-write cycle:

1. Read the parts of the message object that are not to be changed from the message RAM using the command mask register.
   – After the partial read of a Message Object, the Message Buffer Registers that are not selected in the Command Mask Register will be left unchanged.
2. Write the complete contents of the message buffer registers into the message object.
   – After the partial write of a Message Object, the Message Buffer Registers that are not selected in the Command Mask Register will set to the actual contents of the selected Message Object.

36.7.3.3 Transmission of messages between the shift registers in the CAN core and the Message buffer

If the shift register of the CAN Core cell is ready for loading and if there is no data transfer between the IFx Registers and Message RAM, the MSGVAL bits in the Message Valid Register TXRQST bits in the Transmission Request Register are evaluated. The valid Message Object with the highest priority pending transmission request is loaded into the shift register by the Message Handler and the transmission is started. The Message Object’s NEWDAT bit is reset.

After a successful transmission and if no new data was written to the Message Object (NEWDAT = ‘0’) since the start of the transmission, the TXRQST bit will be reset. If TXIE is set, INTPND will be set after a successful transmission. If the CAN controller has lost the arbitration or if an error occurred during the transmission, the message will be retransmitted as soon as the CAN bus is free again. If meanwhile the transmission of a message with higher priority has been requested, the messages will be transmitted in the order of their priority.

36.7.3.4 Acceptance filtering of received messages

When the arbitration and control field (Identifier + IDE + RTR + DLC) of an incoming message is completely shifted into the Rx/Tx Shift Register of the CAN Core, the Message Handler state machine starts the scanning of the Message RAM for a matching valid Message Object.

To scan the Message RAM for a matching Message Object, the Acceptance Filtering unit is loaded with the arbitration bits from the CAN Core shift register. Then the arbitration and mask fields (including MSGVAL, UMASK, NEWDAT, and EOB) of Message Object 1 are loaded into the Acceptance Filtering unit and compared with the arbitration field from the shift register. This is repeated with each following Message Object until a matching Message Object is found or until the end of the Message RAM is reached.

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If a match occurs, the scanning is stopped and the Message Handler state machine proceeds depending on the type of frame (Data Frame or Remote Frame) received.

36.7.3.4.1 Reception of a data frame

The Message Handler state machine stores the message from the CAN Core shift register into the respective Message Object in the Message RAM. The data bytes, all arbitration bits, and the Data Length Code are stored into the corresponding Message Object. This is implemented to keep the data bytes connected with the identifier even if arbitration mask registers are used.

The NEWDAT bit is set to indicate that new data (not yet seen by the CPU) has been received. The CPU/software should reset NEWDAT when it reads the Message Object. If at the time of the reception the NEWDAT bit was already set, MSGLST is set to indicate that the previous data (supposedly not seen by the CPU) is lost. If the RxIE bit is set, the INTPND bit is also set, causing the Interrupt Register to point to this Message Object.

The TXRQST bit of this Message Object is reset to prevent the transmission of a Remote Frame, while the requested Data Frame has just been received.

36.7.3.4.2 Reception of a remote frame

When a Remote Frame is received, three different configurations of the matching Message Object have to be considered:

1. DIR = ‘1’ (direction = transmit), RMTEN = ‘1’, UMASK = ‘1’ or ’0’

   On the reception of a matching Remote Frame, the TXRQST bit of this Message Object is set. The rest of the Message Object remains unchanged.
2. DIR = ‘1’ (direction = transmit), RMTEN = ‘0’, UMASK = ’0’

   On the reception of a matching Remote Frame, the TXRQST bit of this Message Object remains unchanged; the Remote Frame is ignored.
3. DIR = ‘1’ (direction = transmit), RMTEN = ‘0’, UMASK = ’1’

   On the reception of a matching Remote Frame, the TXRQST bit of this Message Object is reset. The arbitration and control field (Identifier + IDE + RTR + DLC) from the shift register is stored into the Message Object in the Message RAM, and the NEWDAT bit of this Message Object is set. The data field of the Message Object remains unchanged; the Remote Frame is treated similar to a received Data Frame.

36.7.3.5 Receive/transmit priority

The receive/transmit priority for the Message Objects is attached to the message number. Message Object 1 has the highest priority, while Message Object 32 has the lowest priority. If more than one transmission request is pending, they are serviced due to the priority of the corresponding Message Object.

36.7.3.6 Configuration of a transmit object

Table 795 shows how a transmit object should be initialized by software (see also Table 761):

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Table 795. Initialization of a transmit object

MSGVAL	Arbitration bits	Data bits	Mask bits	EOB	DIR	NEWDAT
1	application dependent	application dependent	application dependent	1	1	0
MSGLST	**RXIE**	**TXIE**	**INTPND**	**RMTEN**	**TXRQST**	
0	0	application dependent	0	application dependent	0	

The Arbitration Registers (ID28:0 and XTD bit) are given by the application. They define the identifier and the type of the outgoing message. If an 11-bit Identifier (“Standard Frame”) is used, it is programmed to ID28. In this case ID18, ID17 to ID0 can be disregarded.

If the TXIE bit is set, the INTPND bit will be set after a successful transmission of the Message Object.

If the RMTEN bit is set, a matching received Remote Frame will cause the TXRQST bit to be set, and the Remote Frame will autonomously be answered by a Data Frame.

The Data Registers (DLC3:0, Data0:7) are given by the application. TXRQST and RMTEN may not be set before the data is valid.

The Mask Registers (Msk28-0, UMASK, MXTD, and MDIR bits) may be used (UMASK=’1’) to allow groups of Remote Frames with similar identifiers to set the TXRQST bit. For details see Section 36.7.3.4.2. The DIR bit should not be masked.

36.7.3.7 Updating a transmit object

The CPU may update the data bytes of a Transmit Object any time via the IFx Interface registers. Neither MSGVAL nor TXRQST have to be reset before the update.

Even if only a part of the data bytes are to be updated, all four bytes of the corresponding IFx Data A Register or IFx Data B Register have to be valid before the content of that register is transferred to the Message Object. Either the CPU has to write all four bytes into the IFx Data Register or the Message Object is transferred to the IFx Data Register before the CPU writes the new data bytes.

When only the (eight) data bytes are updated, first 0x0087 is written to the Command Mask Register. Then the number of the Message Object is written to the Command Request Register, concurrently updating the data bytes and setting TXRQST.

To prevent the reset of TXRQST at the end of a transmission that may already be in progress while the data is updated, NEWDAT has to be set together with TXRQST. For details see Section 36.7.3.3.

When NEWDAT is set together with TXRQST, NEWDAT will be reset as soon as the new transmission has started.

36.7.3.8 Configuration of a receive object

Table 796 shows how a receive object should be initialized by software (see also Table 761)

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Table 796. Initialization of a receive object

MSGVAL	Arbitration bits	Data bits	Mask bits	EOB	DIR	NEWDAT
1	application dependent	application dependent	application dependent	1	0	0
MSGLST	**RXIE**	**TXIE**	**INTPND**	**RMTEN**	**TXRQST**	
0	application dependent	0	0	0	0	

The Arbitration Registers (ID28-0 and XTD bit) are given by the application. They define the identifier and type of accepted received messages. If an 11-bit Identifier ("Standard Frame") is used, it is programmed to ID28 to ID18. ID17 to ID0 can then be disregarded. When a Data Frame with an 11-bit Identifier is received, ID17 to ID0 will be set to '0'.

If the RxIE bit is set, the INTPND bit will be set when a received Data Frame is accepted and stored in the Message Object.

The Data Length Code (DLC[3:0] is given by the application. When the Message Handler stores a Data Frame in the Message Object, it will store the received Data Length Code and eight data bytes. If the Data Length Code is less than 8, the remaining bytes of the Message Object will be overwritten by non specified values.

The Mask Registers (Msk[28:0], UMASK, MXTD, and MDIR bits) may be used (UMASK='1') to allow groups of Data Frames with similar identifiers to be accepted. For details see section Section 36.7.3.4.1. The DIR bit should not be masked in typical applications.

36.7.3.9 Handling of received messages

The CPU may read a received message any time via the IFx Interface registers. The data consistency is guaranteed by the Message Handler state machine.

To transfer the entire received message from message RAM into the message buffer, software must write first 0x007F to the Command Mask Register and then the number of the Message Object to the Command Request Register. Additionally, the bits NEWDAT and INTPND are cleared in the Message RAM (not in the Message Buffer).

If the Message Object uses masks for acceptance filtering, the arbitration bits show which of the matching messages has been received.

The actual value of NEWDAT shows whether a new message has been received since last time this Message Object was read. The actual value of MSGLST shows whether more than one message has been received since last time this Message Object was read. MSGLST will not be automatically reset.

Using a Remote Frame, the CPU may request another CAN node to provide new data for a receive object. Setting the TXRQST bit of a receive object will cause the transmission of a Remote Frame with the receive object's identifier. This Remote Frame triggers the other CAN node to start the transmission of the matching Data Frame. If the matching Data Frame is received before the Remote Frame could be transmitted, the TXRQST bit is automatically reset.

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36.7.3.10 Configuration of a FIFO buffer

With the exception of the EOB bit, the configuration of Receive Objects belonging to a FIFO Buffer is the same as the configuration of a (single) Receive Object, see section Section 36.7.3.8.

To concatenate two or more Message Objects into a FIFO Buffer, the identifiers and masks (if used) of these Message Objects have to be programmed to matching values. Due to the implicit priority of the Message Objects, the Message Object with the lowest number will be the first Message Object of the FIFO Buffer. The EOB bit of all Message Objects of a FIFO Buffer except the last have to be programmed to zero. The EOB bits of the last Message Object of a FIFO Buffer is set to one, configuring it as the End of the Block.

36.7.3.10.1 Reception of messages with FIFO buffers

Received messages with identifiers matching to a FIFO Buffer are stored into a Message Object of this FIFO Buffer starting with the Message Object with the lowest message number.

When a message is stored into a Message Object of a FIFO Buffer the NEWDAT bit of this Message Object is set. By setting NEWDAT while EOB is zero the Message Object is locked for further write accesses by the Message Handler until the CPU has written the NEWDAT bit back to zero.

Messages are stored into a FIFO Buffer until the last Message Object of this FIFO Buffer is reached. If none of the preceding Message Objects is released by writing NEWDAT to zero, all further messages for this FIFO Buffer will be written into the last Message Object of the FIFO Buffer and therefore overwrite previous messages.

36.7.3.10.2 Reading from a FIFO buffer

When the CPU transfers the contents of Message Object to the IFx Message Buffer registers by writing its number to the IFx Command Request Register, bits NEWDAT and INTPND in the corresponding Command Mask Register should be reset to zero (TXRQST/NEWDAT = ‘1’ and ClrINTPND = ‘1’). The values of these bits in the Message Control Register always reflect the status before resetting the bits.

To assure the correct function of a FIFO Buffer, the CPU should read out the Message Objects starting at the FIFO Object with the lowest message number.

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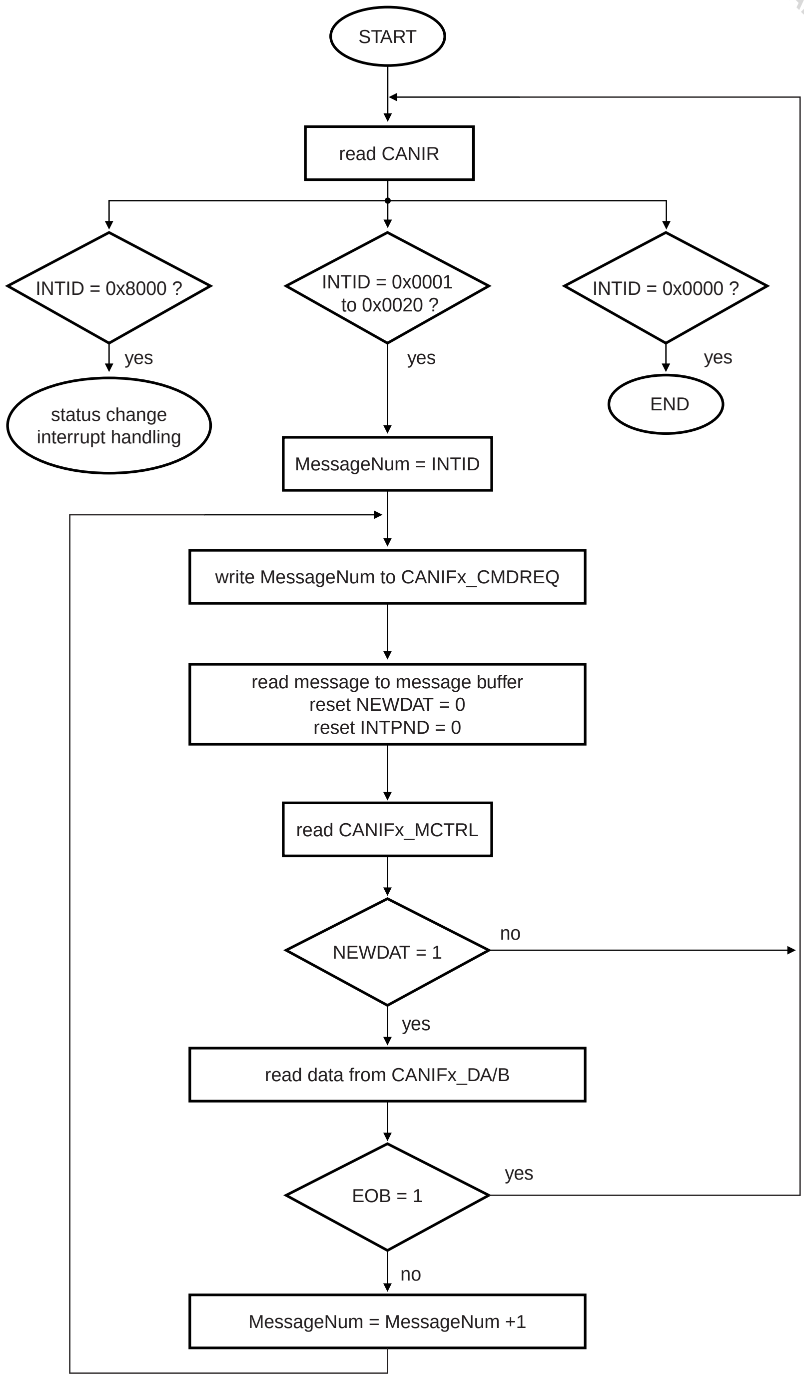


Fig 129. Reading a message from the FIFO buffer to the message buffer

36.7.4 Interrupt handling

If several interrupts are pending, the CAN Interrupt Register will point to the pending interrupt with the highest priority, disregarding their chronological order. An interrupt remains pending until the CPU has cleared it.

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The Status Interrupt has the highest priority. Among the message interrupts, the Message Object's interrupt priority decreases with increasing message number.

A message interrupt is cleared by clearing the Message Object's INTPND bit. The Status Interrupt is cleared by reading the Status Register.

The interrupt identifier INTID in the Interrupt Register indicates the cause of the interrupt. When no interrupt is pending, the register will hold the value zero. If the value of the Interrupt Register is different from zero, then there is an interrupt pending and, if IE is set, the interrupt line to the CPU, IRQ_B, is active. The interrupt line remains active until the Interrupt Register is back to value zero (the cause of the interrupt is reset) or until IE is reset.

The value 0x8000 indicates that an interrupt is pending because the CAN Core has updated (not necessarily changed) the Status Register (Error Interrupt or Status Interrupt). This interrupt has the highest priority. The CPU can update (reset) the status bits RXOK, TXOK and LEC, but a write access of the CPU to the Status Register can never generate or reset an interrupt.

All other values indicate that the source of the interrupt is one of the Message Objects where INTID points to the pending message interrupt with the highest interrupt priority.

The CPU controls whether a change of the Status Register may cause an interrupt (bits EIE and SIE in the CAN Control Register) and whether the interrupt line becomes active when the Interrupt Register is different from zero (bit IE in the CAN Control Register). The Interrupt Register will be updated even when IE is reset.

The CPU has two possibilities to follow the source of a message interrupt:

- Software can follow the INTID in the Interrupt Register.
- Software can poll the interrupt pending register.

An interrupt service routine reading the message that is the source of the interrupt may read the message and reset the Message Object's INTPND at the same time (bit ClrINTPND in the Command Mask Register). When INTPND is cleared, the Interrupt Register will point to the next Message Object with a pending interrupt.

36.7.5 Bit timing

Even if minor errors in the configuration of the CAN bit timing do not result in immediate failure, the performance of a CAN network can be reduced significantly. In many cases, the CAN bit synchronization will amend a faulty configuration of the CAN bit timing to such a degree that only occasionally an error frame is generated. In the case of arbitration however, when two or more CAN nodes simultaneously try to transmit a frame, a misplaced sample point may cause one of the transmitters to become error passive.

The analysis of such sporadic errors requires a detailed knowledge of the CAN bit synchronization inside a CAN node and of the CAN nodes' interaction on the CAN bus.

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36.7.5.1 Bit time and bit rate

CAN supports bit rates in the range of lower than 1 kBit/s up to 1000 kBit/s. Each member of the CAN network has its own clock generator, usually a quartz oscillator. The timing parameter of the bit time (i.e. the reciprocal of the bit rate) can be configured individually for each CAN node, creating a common bit rate even though the CAN nodes' oscillator periods (f_{osc}) may be different.

The frequencies of these oscillators are not absolutely stable, as small variations are caused by changes in temperature or voltage and by deteriorating components. As long as the variations remain inside a specific oscillator tolerance range (df), the CAN nodes are able to compensate for the different bit rates by re-synchronizing to the bit stream.

According to the CAN specification, the bit time is divided into four segments (Figure 130). The Synchronization Segment, the Propagation Time Segment, the Phase Buffer Segment 1, and the Phase Buffer Segment 2. Each segment consists of a specific, programmable number of time quanta (see Table 797). The length of the time quantum (t_q), which is the basic time unit of the bit time, is defined by the CAN controller's system clock f and the Baud Rate Prescaler (BRP): t_q = BRP / f_{sys}. The C_CAN's system clock f_{sys} is the frequency C_CAN peripheral clock.

The Synchronization Segment Sync_Seg is the part of the bit time where edges of the CAN bus level are expected to occur; the distance between an edge that occurs outside of Sync_Seg and the Sync_Seg is called the phase error of that edge. The Propagation Time Segment Prop_Seg is intended to compensate for the physical delay times within the CAN network. The Phase Buffer Segments Phase_Seg1 and Phase_Seg2 surround the Sample Point. The (Re-)Synchronization Jump Width (SJW) defines how far a re-synchronization may move the Sample Point inside the limits defined by the Phase Buffer Segments to compensate for edge phase errors.

Table 797 describes the minimum programmable ranges required by the CAN protocol. Bit time parameters are programmed through the BT register, Table 756. For details on bit timing and examples, see the *C_CAN user's manual, revision 1.2*.

Table 797. Parameters of the C_CAN bit time

Parameter	Range	Function
BRP	(1...32)	Defines the length of the time quantum t_q.
SYNC_SEG	1t_q	Synchronization segment. Fixed length. Synchronization of bus input to system clock.
PROP_SEG	(1...8) × t_q	Propagation time segment. Compensates for physical delay times. This parameter is determined by the system delay times in the C_CAN network.
TSEG1	(1...8) × t_q	Phase buffer segment 1. May be lengthened temporarily by synchronization.
TSEG2	(1...8) × t_q	Phase buffer segment 2. May be shortened temporarily by synchronization.
SJW	(1...4) × t_q	(Re-) synchronization jump width. May not be longer than either phase buffer segment.

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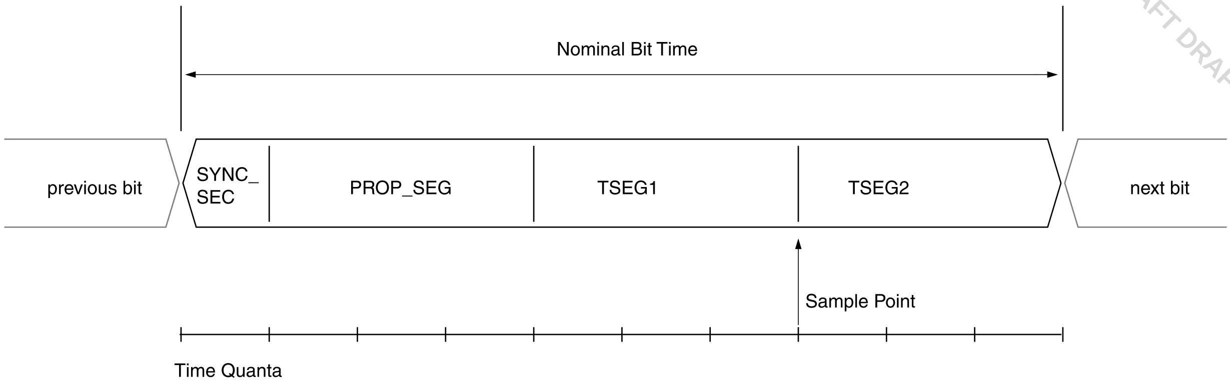


Fig 130. Bit timing

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37.1 How to read this chapter

The I2C-bus interfaces I2C0 and I2C1 are available on all LPC18xx parts.

37.2 Basic configuration

The I2C0/1 are configured as follows:

- See Table 798 for clocking and power control.
- The I2C0/1 are reset by the I2C0/1_RST (reset # 48/49).
- The I2C0/1 interrupts are connected to slots # 18/19 in the NVIC.
- Configure the I2C0 pins for Fast-mode Plus, Fast mode, or Standard mode through the SFSI2C0 register in the SYSCON block (see Table 205).

Table 798. I2C0/1 clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to the I2C0 register interface and I2C0 peripheral clock.	BASE_APB1_CLK	CLK_APB1_I2C0	150 MHz
Clock to the I2C1 register interface and I2C1 peripheral clock.	BASE_APB3_CLK	CLK_APB3_I2C1	150 MHz

37.3 Features

- Standard I^2C-compliant bus interfaces may be configured as Master, Slave, or Master/Slave.
- Arbitration is handled between simultaneously transmitting masters without corruption of serial data on the bus.
- Programmable clock allows adjustment of I^2C transfer rates.
- Data transfer is bidirectional between masters and slaves.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization is used as a handshake mechanism to suspend and resume serial transfer.
- Supports Fast-mode Plus.
- Optional recognition of up to four distinct slave addresses.
- Monitor mode allows observing all I^2C-bus traffic, regardless of slave address.
- I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus contains a standard I^2C-compliant bus interface with two pins.

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37.4 Applications

Interfaces to external I²C standard parts, such as serial RAMs, LCDs, tone generators, other microcontrollers, etc.

37.5 General description

A typical I²C-bus configuration is shown in Figure 131. Depending on the state of the direction bit (R/W), two types of data transfers are possible on the I²C-bus:

- Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
- Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows the data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a Repeated START condition. Since a Repeated START condition is also the beginning of the next serial transfer, the I²C bus will not be released.

The I²C interface is byte oriented and has four operating modes: master transmitter mode, master receiver mode, slave transmitter mode and slave receiver mode.

The I²C interface complies with the entire I²C specification, supporting the ability to turn power off to the processor without interfering with other devices on the same I²C-bus.

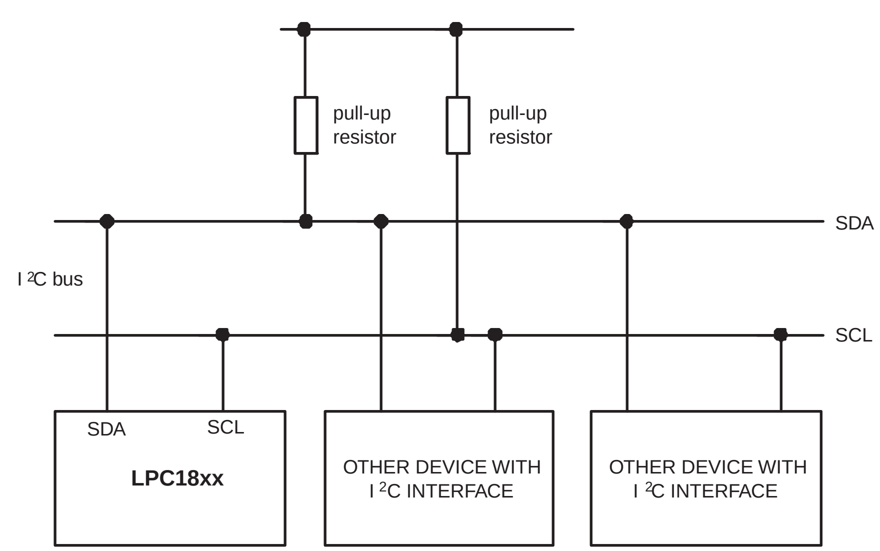


Fig 131. I²C-bus configuration

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37.5.1 I²C Fast-mode Plus

Fast-Mode Plus supports a 1 Mbit/sec transfer rate to communicate with the I²C-bus products which NXP Semiconductors is now providing.

In order to use Fast-Mode Plus, the I²C pins must be properly configured in the SFSI2C0 register in the SYSCON block (see Table 205).

37.6 Pin description

Table 799. I²C-bus pin description

Pin	Type	Description
SDA0	Input/Output	I²C data input/output. Open-drain output (for I²C-bus compliance).
SCL0	Input/Output	I²C clock input/output. Open-drain output (for I²C-bus compliance).
SDA1	Input/Output	I²C Serial Data. Uses standard I/O pins (Fast-mode only).
SCL1	Input/Output	I²C Serial Clock. Uses standard I/O pins (Fast-mode only).

The I²C-bus pins must be configured through SYSCON registers for Standard/ Fast-mode or Fast-mode Plus.

37.7 Register description

Table 800. Register overview: I²C0 (base address 0x400A 1000)

Name	Access	Address offset	Description	Reset value[1]
CONSET	R/W	0x000	**I2C Control Set Register.** When a one is written to a bit of this register, the corresponding bit in the I²C control register is set. Writing a zero has no effect on the corresponding bit in the I²C control register.	0x00
STAT	RO	0x004	**I2C Status Register.** During I²C operation, this register provides detailed status codes that allow software to determine the next action needed.	0xF8
DAT	R/W	0x008	**I2C Data Register.** During master or slave transmit mode, data to be transmitted is written to this register. During master or slave receive mode, data that has been received may be read from this register.	0x00
ADR0	R/W	0x00C	**I2C Slave Address Register 0.** Contains the 7-bit slave address for operation of the I²C interface in slave mode, and is not used in master mode. The least significant bit determines whether a slave responds to the General Call address.	0x00
SCLH	R/W	0x010	**SCH Duty Cycle Register High Half Word.** Determines the high time of the I²C clock.	0x04
SCLL	R/W	0x014	**SCL Duty Cycle Register Low Half Word.** Determines the low time of the I²C clock. SCLL and SCLH together determine the clock frequency generated by an I²C master and certain times used in slave mode.	0x04
CONCLR	WO	0x018	**I2C Control Clear Register.** When a one is written to a bit of this register, the corresponding bit in the I²C control register is cleared. Writing a zero has no effect on the corresponding bit in the I²C control register.	-

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Table 800. Register overview: I²C0 (base address 0x400A 1000) *…continued*

Name	Access	Address offset	Description	Reset value[1]
MMCTRL	R/W	0x01C	**Monitor mode control register.**	0x00
ADR1	R/W	0x020	**I2C Slave Address Register 1.** Contains the 7-bit slave address for operation of the I²C interface in slave mode, and is not used in master mode. The least significant bit determines whether a slave responds to the General Call address.	0x00
ADR2	R/W	0x024	**I2C Slave Address Register 2.** Contains the 7-bit slave address for operation of the I²C interface in slave mode, and is not used in master mode. The least significant bit determines whether a slave responds to the General Call address.	0x00
ADR3	R/W	0x028	**I2C Slave Address Register 3.** Contains the 7-bit slave address for operation of the I²C interface in slave mode, and is not used in master mode. The least significant bit determines whether a slave responds to the General Call address.	0x00
DATA_BUFFER	RO	0x02C	**Data buffer register.** The contents of the 8 MSBs of the DAT shift register will be transferred to the DATA_BUFFER automatically after every nine bits (8 bits of data plus ACK or NACK) has been received on the bus.	0x00
MASK0	R/W	0x030	**I2C Slave address mask register 0**. This mask register is associated with ADR0 to determine an address match. The mask register has no effect when comparing to the General Call address (‘0000000’).	0x00
MASK1	R/W	0x034	**I2C Slave address mask register 1**. This mask register is associated with ADR0 to determine an address match. The mask register has no effect when comparing to the General Call address (‘0000000’).	0x00
MASK2	R/W	0x038	**I2C Slave address mask register 2**. This mask register is associated with ADR0 to determine an address match. The mask register has no effect when comparing to the General Call address (‘0000000’).	0x00
MASK3	R/W	0x03C	**I2C Slave address mask register 3**. This mask register is associated with ADR0 to determine an address match. The mask register has no effect when comparing to the General Call address (‘0000000’).	0x00

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

Table 801. Register overview: I²C1 (base address 0x400E 0000)

Name	Access	Address offset	Description	Reset value[1]
CONSET	R/W	0x000	**I2C Control Set Register.** When a one is written to a bit of this register, the corresponding bit in the I²C control register is set. Writing a zero has no effect on the corresponding bit in the I²C control register.	0x00
STAT	RO	0x004	**I2C Status Register.** During I²C operation, this register provides detailed status codes that allow software to determine the next action needed.	0xF8
IDAT	R/W	0x008	**I2C Data Register.** During master or slave transmit mode, data to be transmitted is written to this register. During master or slave receive mode, data that has been received may be read from this register.	0x00
ADR0	R/W	0x00C	**I2C Slave Address Register 0.** Contains the 7-bit slave address for operation of the I²C interface in slave mode, and is not used in master mode. The least significant bit determines whether a slave responds to the General Call address.	0x00
SCLH	R/W	0x010	**SCH Duty Cycle Register High Half Word.** Determines the high time of the I²C clock.	0x04

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Table 801. Register overview: I²C1 (base address 0x400E 0000) *…continued*

Name	Access	Address offset	Description	Reset value[1]
SCLL	R/W	0x014	**SCL Duty Cycle Register Low Half Word.** Determines the low time of the I²C clock. I2nSCLL and nSCLH together determine the clock frequency generated by an I²C master and certain times used in slave mode.	0x04
CONCLR	WO	0x018	**I2C Control Clear Register.** When a one is written to a bit of this register, the corresponding bit in the I²C control register is cleared. Writing a zero has no effect on the corresponding bit in the I²C control register.	-
MMCTRL	R/W	0x01C	**Monitor mode control register.**	0x00
ADR1	R/W	0x020	**I2C Slave Address Register 1.** Contains the 7-bit slave address for operation of the I²C interface in slave mode, and is not used in master mode. The least significant bit determines whether a slave responds to the General Call address.	0x00
ADR2	R/W	0x024	**I2C Slave Address Register 2.** Contains the 7-bit slave address for operation of the I²C interface in slave mode, and is not used in master mode. The least significant bit determines whether a slave responds to the General Call address.	0x00
ADR3	R/W	0x028	**I2C Slave Address Register 3.** Contains the 7-bit slave address for operation of the I²C interface in slave mode, and is not used in master mode. The least significant bit determines whether a slave responds to the General Call address.	0x00
DATA_ BUFFER	RO	0x02C	**Data buffer register.** The contents of the 8 MSBs of the DAT shift register will be transferred to the DATA_BUFFER automatically after every nine bits (8 bits of data plus ACK or NACK) has been received on the bus.	0x00
MASK0	R/W	0x030	**I2C Slave address mask register 0**. This mask register is associated with ADR0 to determine an address match. The mask register has no effect when comparing to the General Call address (‘0000000’).	0x00
MASK1	R/W	0x034	**I2C Slave address mask register 1**. This mask register is associated with ADR0 to determine an address match. The mask register has no effect when comparing to the General Call address (‘0000000’).	0x00
MASK2	R/W	0x038	**I2C Slave address mask register 2**. This mask register is associated with ADR0 to determine an address match. The mask register has no effect when comparing to the General Call address (‘0000000’).	0x00
MASK3	R/W	0x03C	**I2C Slave address mask register 3**. This mask register is associated with ADR0 to determine an address match. The mask register has no effect when comparing to the General Call address (‘0000000’).	0x00

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

37.7.1 I²C Control Set register

The CONSET registers control setting of bits in the CON register that controls operation of the I²C interface. Writing a one to a bit of this register causes the corresponding bit in the I²C control register to be set. Writing a zero has no effect.

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Table 802. I2C Control Set register (CONSET - address 0x400A 1000 (I2C0) and 0x400E 0000 (I2C1)) bit description

Bit	Symbol	Description	Reset value
1:0	-	Reserved. User software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
2	AA	Assert acknowledge flag.	
3	SI	I2C interrupt flag.	0
4	STO	STOP flag.	0
5	STA	START flag.	0
6	I2EN	I2C interface enable.	0
31:7	-	Reserved. The value read from a reserved bit is not defined.	-

I2EN I2C Interface Enable. When I2EN is 1, the I2C interface is enabled. I2EN can be cleared by writing 1 to the I2ENC bit in the CONCLR register. When I2EN is 0, the I2C interface is disabled.

When I2EN is “0”, the SDA and SCL input signals are ignored, the I2C block is in the “not addressed” slave state, and the STO bit is forced to “0”.

I2EN should not be used to temporarily release the I2C-bus since, when I2EN is reset, the I2C-bus status is lost. The AA flag should be used instead.

STA is the START flag. Setting this bit causes the I2C interface to enter master mode and transmit a START condition or transmit a Repeated START condition if it is already in master mode.

When STA is 1 and the I2C interface is not already in master mode, it enters master mode, checks the bus and generates a START condition if the bus is free. If the bus is not free, it waits for a STOP condition (which will free the bus) and generates a START condition after a delay of a half clock period of the internal clock generator. If the I2C interface is already in master mode and data has been transmitted or received, it transmits a Repeated START condition. STA may be set at any time, including when the I2C interface is in an addressed slave mode.

STA can be cleared by writing 1 to the STAC bit in the CONCLR register. When STA is 0, no START condition or Repeated START condition will be generated.

If STA and STO are both set, then a STOP condition is transmitted on the I2C-bus if it the interface is in master mode, and transmits a START condition thereafter. If the I2C interface is in slave mode, an internal STOP condition is generated, but is not transmitted on the bus.

STO is the STOP flag. Setting this bit causes the I2C interface to transmit a STOP condition in master mode, or recover from an error condition in slave mode. When STO is 1 in master mode, a STOP condition is transmitted on the I2C-bus. When the bus detects the STOP condition, STO is cleared automatically.

In slave mode, setting this bit can recover from an error condition. In this case, no STOP condition is transmitted to the bus. The hardware behaves as if a STOP condition has been received and it switches to “not addressed” slave receiver mode. The STO flag is cleared by hardware automatically.

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SI is the I^{2}C Interrupt Flag. This bit is set when the I^{2}C state changes. However, entering state F8 does not set SI since there is nothing for an interrupt service routine to do in that case.

While SI is set, the low period of the serial clock on the SCL line is stretched, and the serial transfer is suspended. When SCL is HIGH, it is unaffected by the state of the SI flag. SI must be reset by software, by writing a 1 to the SIC bit in CONCLR register.

AA is the Assert Acknowledge Flag. When set to 1, an acknowledge (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line on the following situations:

1. The address in the Slave Address Register has been received.
2. The General Call address has been received while the General Call bit (GC) in ADR is set.
3. A data byte has been received while the I^{2}C is in the master receiver mode.
4. A data byte has been received while the I^{2}C is in the addressed slave receiver mode

The AA bit can be cleared by writing 1 to the AAC bit in the CONCLR register. When AA is 0, a not acknowledge (HIGH level to SDA) will be returned during the acknowledge clock pulse on the SCL line on the following situations:

1. A data byte has been received while the I^{2}C is in the master receiver mode.
2. A data byte has been received while the I^{2}C is in the addressed slave receiver mode.

37.7.2 I^{2}C Status register

Each I^{2}C Status register reflects the condition of the corresponding I^{2}C interface. The I^{2}C Status register is Read-Only.

Table 803. I^{2}C Status register (STAT - address 0x400A 1004 (I2C0) and 0x400E 0004 (I2C1)) bit description

Bit	Symbol	Description	Reset value
2:0	-	These bits are unused and are always 0.	0
7:3	Status	These bits give the actual status information about the I^{2}C interface.	0x1F
31:8	-	Reserved. The value read from a reserved bit is not defined.	-

The three least significant bits are always 0. Taken as a byte, the status register contents represent a status code. There are 26 possible status codes. When the status code is 0xF8, there is no relevant information available and the SI bit is not set. All other 25 status codes correspond to defined I^{2}C states. When any of these states entered, the SI bit will be set. For a complete list of status codes, refer to tables from Table 818 to Table 823.

37.7.3 I^{2}C Data register

This register contains the data to be transmitted or the data just received. The CPU can read and write to this register only while it is not in the process of shifting a byte, when the SI bit is set. Data in DAT remains stable as long as the SI bit is set. Data in DAT is always shifted from right to left: the first bit to be transmitted is the MSB (bit 7), and after a byte has been received, the first bit of received data is located at the MSB of DAT.

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Table 804. I²C Data register (DAT - 0x400A 1008 (I2C0) and 0x400E 0008 (I2C1)) bit description

Bit	Symbol	Description	Reset value
7:0	Data	This register holds data values that have been received or are to be transmitted.	0
31:8	-	Reserved. The value read from a reserved bit is not defined.	-

37.7.4 I²C Slave Address register 0

This register is readable and writable and are only used when an I²C interface is set to slave mode. In master mode, this register has no effect. The LSB of ADR is the General Call bit. When this bit is set, the General Call address (0x00) is recognized.

If this register contains 0x00, the I²C will not acknowledge any address on the bus. This register will be cleared to this disabled state on reset. See also Table 811.

Table 805. I²C Slave Address register 0 (ADR0 - address 0x400A 100C (I2C0) and 0x400E 000C (I2C1)) bit description

Bit	Symbol	Description	Reset value
0	GC	General Call enable bit.	0
7:1	Address	The I²C device address for slave mode.	0x00
31:8	-	Reserved. The value read from a reserved bit is not defined.	-

37.7.5 I²C SCL HIGH and LOW duty cycle registers

Table 806. I²C SCL HIGH Duty Cycle register (SCLH - address 0x400A 1010 (I2C0) and 0x400E 0010 (I2C1)) bit description

Bit	Symbol	Description	Reset value
15:0	SCLH	Count for SCL HIGH time period selection.	0x0004
31:16	-	Reserved. The value read from a reserved bit is not defined.	-

Table 807. I²C SCL Low duty cycle register (SCLL - address 0x400A 1014 (I2C0) and 0x400E 0014 (I2C1)) bit description

Bit	Symbol	Description	Reset value
15:0	SCLL	Count for SCL low time period selection.	0x0004
31:16	-	Reserved. The value read from a reserved bit is not defined.	-

37.7.5.1 Selecting the appropriate I²C data rate and duty cycle

Software must set values for the registers SCLH and SCLL to select the appropriate data rate and duty cycle. SCLH defines the number of C_PCLK cycles for the SCL HIGH time, SCLL defines the number of I2C_PCLK cycles for the SCL low time. The frequency is determined by the following formula (I2C_PCLK is the frequency of the peripheral I2C clock):

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$$I^2C_{bitfrequency} = \frac{I2CPCLK}{I2CSCLH + I2CSCLL} \tag{10}$$

The values for SCLL and SCLH must ensure that the data rate is in the appropriate I^2C data rate range. Each register value must be greater than or equal to 4. Table 808 gives some examples of I^2C-bus rates based on I2C_PCLK frequency and SCLL and SCLH values.

Table 808. SCLL + SCLH values for selected I^2C clock values

I^2C mode	I^2C bit frequency	I2C_PCLK (MHz)								
		6	8	10	12	16	20	30	40	50
		SCLH + SCLL								
Standard mode	100 kHz	60	80	100	120	160	200	300	400	500
Fast-mode	400 kHz	15	20	25	30	40	50	75	100	125
Fast-mode Plus	1 MHz	-	8	10	12	16	20	30	40	50

SCLL and SCLH values should not necessarily be the same. Software can set different duty cycles on SCL by setting these two registers. For example, the I^2C-bus specification defines the SCL low time and high time at different values for a Fast-mode and Fast-mode Plus I^2C.

37.7.6 I^2C Control Clear register

The CONCLR registers control clearing of bits in the CON register that controls operation of the I^2C interface. Writing a one to a bit of this register causes the corresponding bit in the I^2C control register to be cleared. Writing a zero has no effect.

Table 809. I^2C Control Clear register (CONCLR - address 0x400A 1018 and 0x400E 0018 (I2C1)) bit description

Bit	Symbol	Description	Reset value
1:0	-	Reserved. User software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
2	AAC	Assert acknowledge Clear bit.	
3	SIC	I^2C interrupt Clear bit.	0
4	-	Reserved. User software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
5	STAC	START flag Clear bit.	0
6	I2ENC	I^2C interface Disable bit.	0
7	-	Reserved. User software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
31:8	-	Reserved. The value read from a reserved bit is not defined.	-

AAC is the Assert Acknowledge Clear bit. Writing a 1 to this bit clears the AA bit in the CONSET register. Writing 0 has no effect.

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SIC is the I^{2}C Interrupt Clear bit. Writing a 1 to this bit clears the SI bit in the CONSET register. Writing 0 has no effect.

STAC is the START flag Clear bit. Writing a 1 to this bit clears the STA bit in the CONSET register. Writing 0 has no effect.

I2ENC is the I^{2}C Interface Disable bit. Writing a 1 to this bit clears the I2EN bit in the CONSET register. Writing 0 has no effect.

37.7.7 I^{2}C Monitor mode control register

This register controls the Monitor mode which allows the I^{2}C module to monitor traffic on the I^{2}C bus without actually participating in traffic or interfering with the I^{2}C bus.

Table 810. I^{2}C Monitor mode control register (MMCTRL - address 0x400A 101C (I2C0) and 0x400E 001C (I2C1)) bit description

Bit	Symbol	Value	Description	Reset value
0	MM_ENA		Monitor mode enable.	0
		0	Monitor mode disabled.	
		1	The I^{2}C module will enter monitor mode. In this mode the SDA output will be forced high. This will prevent the I^{2}C module from outputting data of any kind (including ACK) onto the I^{2}C data bus. Depending on the state of the ENA_SCL bit, the output may be also forced high, preventing the module from having control over the I^{2}C clock line.	
1	ENA_SCL		SCL output enable.	0
		0	When this bit is cleared to ‘0’, the SCL output will be forced high when the module is in monitor mode. As described above, this will prevent the module from having any control over the I^{2}C clock line.	
		1	When this bit is set, the I^{2}C module may exercise the same control over the clock line that it would in normal operation. This means that, acting as a slave peripheral, the I^{2}C module can “stretch” the clock line (hold it low) until it has had time to respond to an I^{2}C interrupt.[1]	
2	MATCH_ALL		Select interrupt register match.	0
		0	When this bit is cleared, an interrupt will only be generated when a match occurs to one of the (up-to) four address registers described above. That is, the module will respond as a normal slave as far as address-recognition is concerned.	
		1	When this bit is set to ‘1’ and the I2C is in monitor mode, an interrupt will be generated on ANY address received. This will enable the part to monitor all traffic on the bus.	
31:3	-	-	Reserved. The value read from reserved bits is not defined.	-

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[1] When the ENA_SCL bit is cleared and the I2C no longer has the ability to stall the bus, interrupt response time becomes important. To give the part more time to respond to an I2C interrupt under these conditions, a DATA _BUFFER register is used (Section 37.7.9) to hold received data for a full 9-bit word transmission time.

Remark: The ENA_SCL and MATCH_ALL bits have no effect if the MM_ENA is '0' (i.e. if the module is NOT in monitor mode).

37.7.7.1 Interrupt in Monitor mode

All interrupts will occur as normal when the module is in monitor mode. This means that the first interrupt will occur when an address-match is detected (any address received if the MATCH_ALL bit is set, otherwise an address matching one of the four address registers).

Subsequent to an address-match detection, interrupts will be generated after each data byte is received for a slave-write transfer, or after each byte that the module "thinks" it has transmitted for a slave-read transfer. In this second case, the data register will actually contain data transmitted by some other slave on the bus which was actually addressed by the master.

Following all of these interrupts, the processor may read the data register to see what was actually transmitted on the bus.

37.7.7.2 Loss of arbitration in Monitor mode

In monitor mode, the I2C module will not be able to respond to a request for information by the bus master or issue an ACK). Some other slave on the bus will respond instead. This will most probably result in a lost-arbitration state as far as our module is concerned.

Software should be aware of the fact that the module is in monitor mode and should not respond to any loss of arbitration state that is detected.

37.7.8 I2C Slave Address registers

These registers are readable and writable and are only used when an I2C interface is set to slave mode. In master mode, this register has no effect. The LSB of ADR is the General Call bit. When this bit is set, the General Call address (0x00) is recognized.

If these registers contain 0x00, the I2C will not acknowledge any address on the bus. All four registers (including ADR0, see Table 805) will be cleared to this disabled state on reset.

Table 811. I2C Slave Address registers (ADR - address 0x400A 1020 (ADR1) to 0x400A 1028 (ADR3) (I2C0) and 0x400E 0020 (ADR1) to 0x400E 0028 (ADR3) (I2C1)) bit description

Bit	Symbol	Description	Reset value
0	GC	General Call enable bit.	0
7:1	Address	The I2C device address for slave mode.	0x00
31:8	-	Reserved. The value read from a reserved bit is not defined.	-

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37.7.9 I²C Data buffer register

In monitor mode, the I²C module may lose the ability to stretch the clock (stall the bus) if the ENA_SCL bit is not set. This means that the processor will have a limited amount of time to read the contents of the data received on the bus. If the processor reads the DAT shift register, as it ordinarily would, it could have only one bit-time to respond to the interrupt before the received data is overwritten by new data.

To give the processor more time to respond, a new 8-bit, read-only DATA_BUFFER register will be added. The contents of the 8 MSBs of the DAT shift register will be transferred to the DATA_BUFFER automatically after every nine bits (8 bits of data plus ACK or NACK) has been received on the bus. This means that the processor will have nine bit transmission times to respond to the interrupt and read the data before it is overwritten.

The processor will still have the ability to read DAT directly, as usual, and the behavior of DAT will not be altered in any way.

Although the DATA_BUFFER register is primarily intended for use in monitor mode with the ENA_SCL bit = ‘0’, it will be available for reading at any time under any mode of operation.

Table 812. I²C Data buffer register (DATA_BUFFER - address 0x400A 102C (I2C0) and 0x400E 002C (I2C1)) bit description

Bit	Symbol	Description	Reset value
7:0	Data	This register holds contents of the 8 MSBs of the DAT shift register.	0
31:8	-	Reserved. The value read from a reserved bit is not defined.	-

37.7.10 I²C Mask registers

The four mask registers each contain seven active bits (7:1). Any bit in these registers which is set to ‘1’ will cause an automatic compare on the corresponding bit of the received address when it is compared to the ADRn register associated with that mask register. In other words, bits in an ADRn register which are masked are not taken into account in determining an address match.

On reset, all mask register bits are cleared to ‘0’.

The mask register has no effect on comparison to the General Call address (“0000000”).

Bits(31:8) and bit(0) of the mask registers are unused and should not be written to. These bits will always read back as zeros.

When an address-match interrupt occurs, the processor will have to read the data register (DAT) to determine what the received address was that actually caused the match.

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Table 813. I^{2}C Mask registers (MASK - address 0x400A 1030 (MASK0) to 0x400A 103C (MASK3) (I2C0) and 0x400E 0030 (MASK0) to 0x400E 003C (MASK3) (I2C1)) bit description

Bit	Symbol	Description	Reset value
0	-	Reserved. User software should not write ones to reserved bits. This bit reads always back as 0.	0
7:1	MASK	Mask bits.	0x00
31:8	-	Reserved. The value read from a reserved bit is not defined.	-

37.8 I^{2}C operating modes

In a given application, the I^{2}C block may operate as a master, a slave, or both. In the slave mode, the I^{2}C hardware looks for any one of its four slave addresses and the General Call address. If one of these addresses is detected, an interrupt is requested. If the processor wishes to become the bus master, the hardware waits until the bus is free before the master mode is entered so that a possible slave operation is not interrupted. If bus arbitration is lost in the master mode, the I^{2}C block switches to the slave mode immediately and can detect its own slave address in the same serial transfer.

37.8.1 Master Transmitter mode

In this mode data is transmitted from master to slave. Before the master transmitter mode can be entered, the CONSET register must be initialized as shown in Table 814. I2EN must be set to 1 to enable the I^{2}C function. If the AA bit is 0, the I^{2}C interface will not acknowledge any address when another device is master of the bus, so it can not enter slave mode. The STA, STO and SI bits must be 0. The SI Bit is cleared by writing 1 to the SIC bit in the CONCLR register. The STA bit should be cleared after writing the slave address.

Table 814. CONSET used to configure Master mode

Bit	7	6	5	4	3	2	1	0
Symbol	-	I2EN	STA	STO	SI	AA	-	-
Value	-	1	0	0	0	0	-	-

The first byte transmitted contains the slave address of the receiving device (7 bits) and the data direction bit. In this mode the data direction bit (R/W) should be 0 which means Write. The first byte transmitted contains the slave address and Write bit. Data is transmitted 8 bits at a time. After each byte is transmitted, an acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

The I^{2}C interface will enter master transmitter mode when software sets the STA bit. The I^{2}C logic will send the START condition as soon as the bus is free. After the START condition is transmitted, the SI bit is set, and the status code in the STAT register is 0x08. This status code is used to vector to a state service routine which will load the slave address and Write bit to the DAT register, and then clear the SI bit. SI is cleared by writing a 1 to the SIC bit in the CONCLR register.

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When the slave address and R/W bit have been transmitted and an acknowledgment bit has been received, the SI bit is set again, and the possible status codes now are 0x18, 0x20, or 0x38 for the master mode, or 0x68, 0x78, or 0xB0 if the slave mode was enabled (by setting AA to 1). The appropriate actions to be taken for each of these status codes are shown in Table 818 to Table 823.

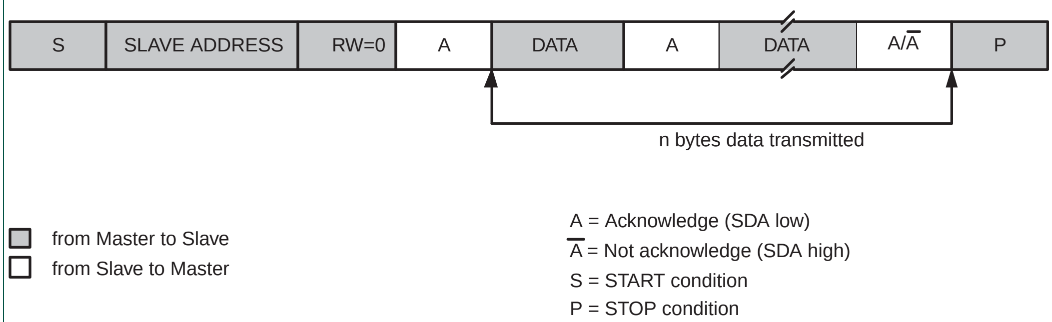


Fig 132. Format in the Master Transmitter mode

37.8.2 Master Receiver mode

In the master receiver mode, data is received from a slave transmitter. The transfer is initiated in the same way as in the master transmitter mode. When the START condition has been transmitted, the interrupt service routine must load the slave address and the data direction bit to the I²C Data register (DAT), and then clear the SI bit. In this case, the data direction bit (R/W) should be 1 to indicate a read.

When the slave address and data direction bit have been transmitted and an acknowledge bit has been received, the SI bit is set, and the Status Register will show the status code. For master mode, the possible status codes are 0x40, 0x48, or 0x38. For slave mode, the possible status codes are 0x68, 0x78, or 0xB0. For details, refer to Table 819.

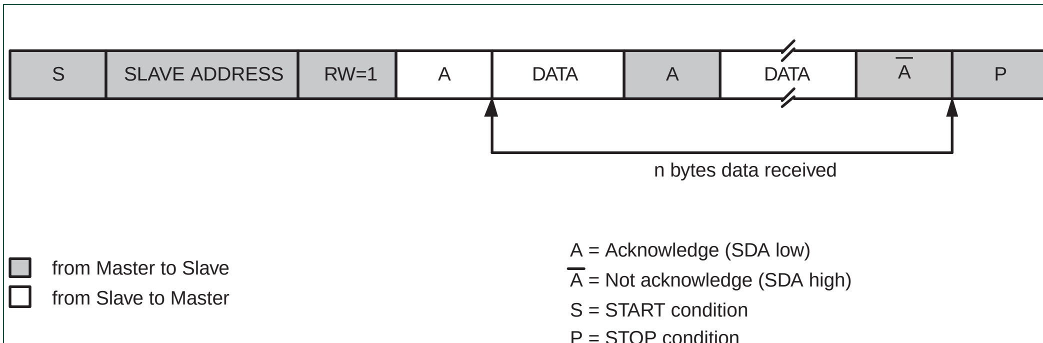


Fig 133. Format of Master Receiver mode

After a Repeated START condition, I²C may switch to the master transmitter mode.

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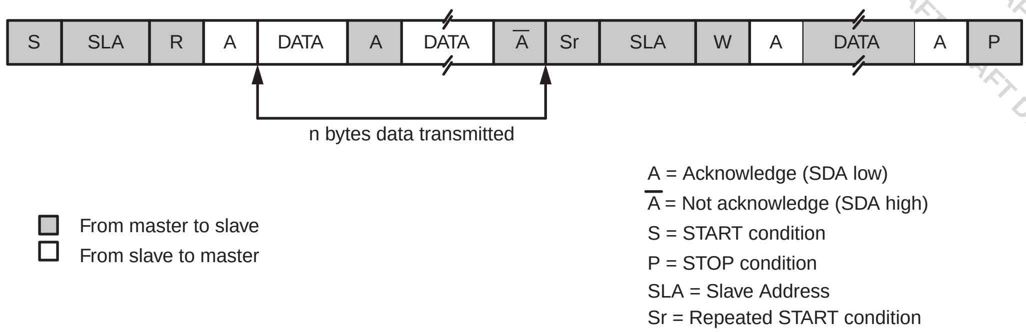


Fig 134. A Master Receiver switches to Master Transmitter after sending Repeated START

37.8.3 Slave Receiver mode

In the slave receiver mode, data bytes are received from a master transmitter. To initialize the slave receiver mode, write any of the Slave Address registers (ADR0-3) and write the I²C Control Set register (CONSET) as shown in Table 815.

Table 815. CONSET used to configure Slave mode

Bit	7	6	5	4	3	2	1	0
Symbol	-	I2EN	STA	STO	SI	AA	-	-
Value	-	1	0	0	0	1	-	-

I2EN must be set to 1 to enable the I²C function. AA bit must be set to 1 to acknowledge its own slave address or the General Call address. The STA, STO and SI bits are set to 0.

After ADR and CONSET are initialized, the I²C interface waits until it is addressed by its own address or general address followed by the data direction bit. If the direction bit is 0 (W), it enters slave receiver mode. If the direction bit is 1 (R), it enters slave transmitter mode. After the address and direction bit have been received, the SI bit is set and a valid status code can be read from the Status register (STAT). Refer to Table 822 for the status codes and actions.

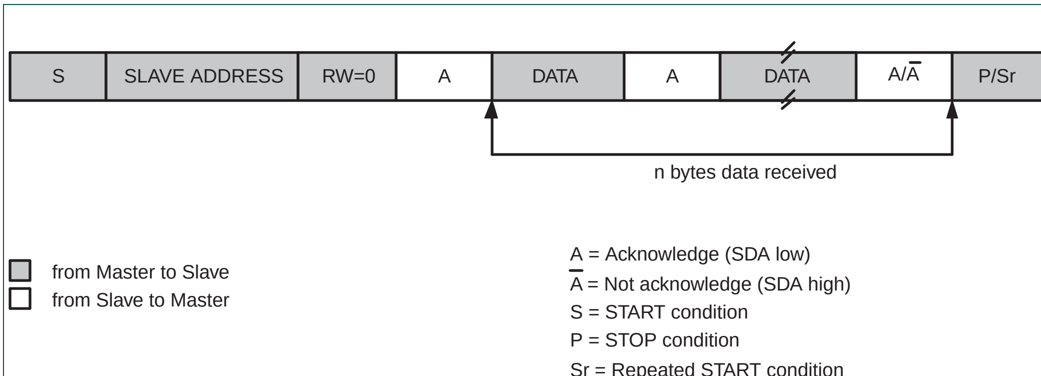


Fig 135. Format of Slave Receiver mode

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37.8.4 Slave Transmitter mode

The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will be 1, indicating a read operation. Serial data is transmitted via SDA while the serial clock is input through SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. In a given application, I^{2}C may operate as a master and as a slave. In the slave mode, the I^{2}C hardware looks for its own slave address and the General Call address. If one of these addresses is detected, an interrupt is requested. When the microcontrollers wishes to become the bus master, the hardware waits until the bus is free before the master mode is entered so that a possible slave action is not interrupted. If bus arbitration is lost in the master mode, the I^{2}C interface switches to the slave mode immediately and can detect its own slave address in the same serial transfer.

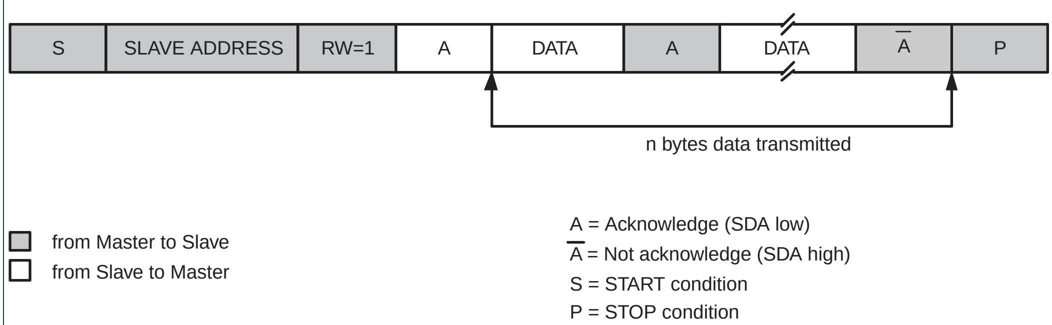


Fig 136. Format of Slave Transmitter mode

37.9 I^{2}C implementation and operation

Figure 137 shows how the on-chip I^{2}C-bus interface is implemented, and the following text describes the individual blocks.

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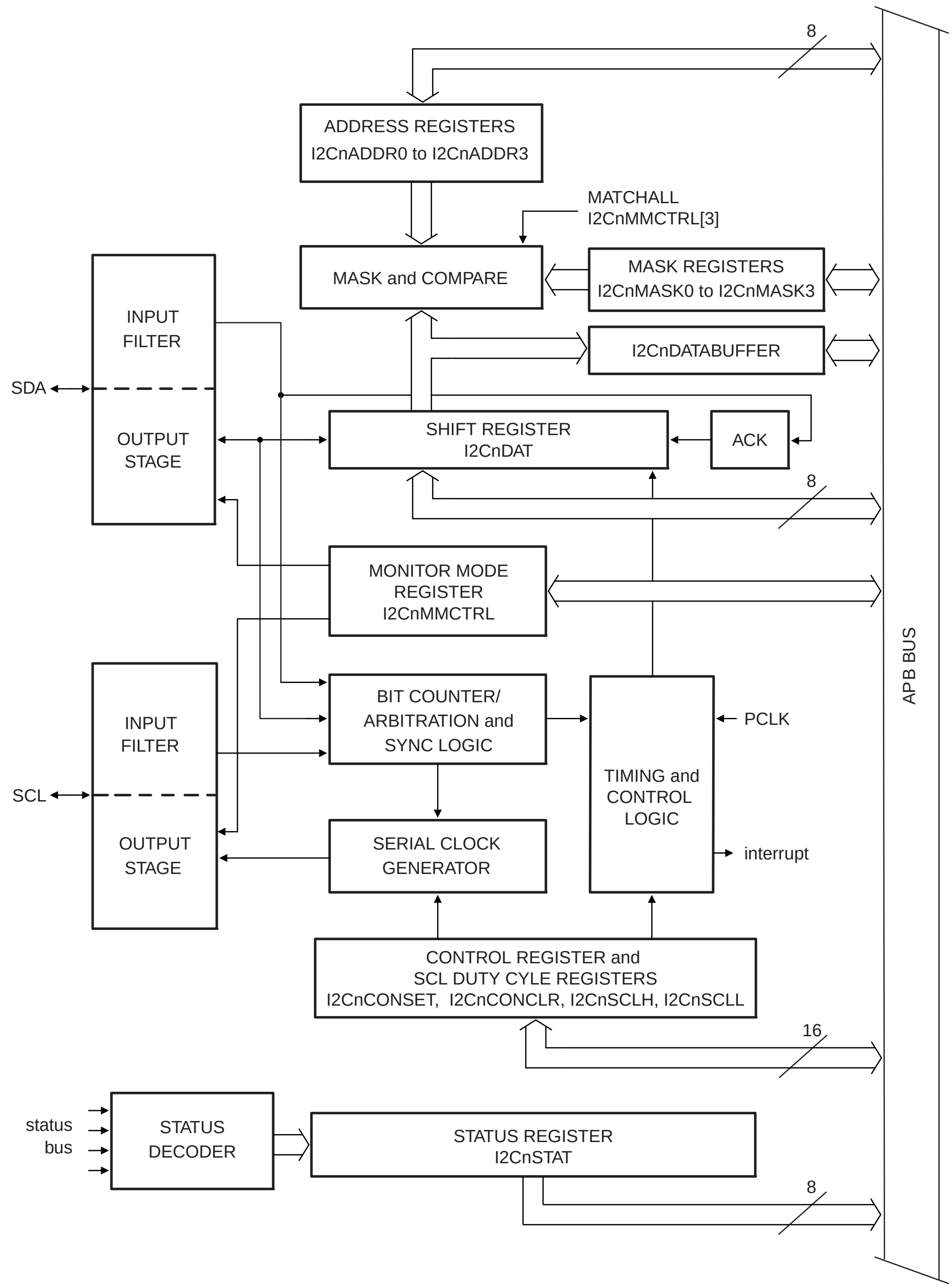


Fig 137. I^{2}C serial interface block diagram

37.9.1 Input filters and output stages

Input signals are synchronized with the internal clock, and spikes shorter than three clocks are filtered out.

The output for I^{2}C is a special pad designed to conform to the I^{2}C specification.

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37.9.2 Address Registers, ADR0 to ADR3

These registers may be loaded with the 7-bit slave address (7 most significant bits) to which the I^{2}C block will respond when programmed as a slave transmitter or receiver. The LSB (GC) is used to enable General Call address (0x00) recognition. When multiple slave addresses are enabled, the actual address received may be read from the DAT register at the state where the own slave address has been received.

37.9.3 Address mask registers, MASK0 to MASK3

The four mask registers each contain seven active bits (7:1). Any bit in these registers which is set to ‘1’ will cause an automatic compare on the corresponding bit of the received address when it is compared to the ADRn register associated with that mask register. In other words, bits in an ADRn register which are masked are not taken into account in determining an address match.

When an address-match interrupt occurs, the processor will have to read the data register (I2DAT) to determine which received address actually caused the match.

37.9.4 Comparator

The comparator compares the received 7-bit slave address with its own slave address (7 most significant bits in ADR). It also compares the first received 8-bit byte with the General Call address (0x00). If an equality is found, the appropriate status bits are set and an interrupt is requested.

37.9.5 Shift register, DAT

This 8-bit register contains a byte of serial data to be transmitted or a byte which has just been received. Data in DAT is always shifted from right to left; the first bit to be transmitted is the MSB (bit 7) and, after a byte has been received, the first bit of received data is located at the MSB of DAT. While data is being shifted out, data on the bus is simultaneously being shifted in; DAT always contains the last byte present on the bus. Thus, in the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data in DAT.

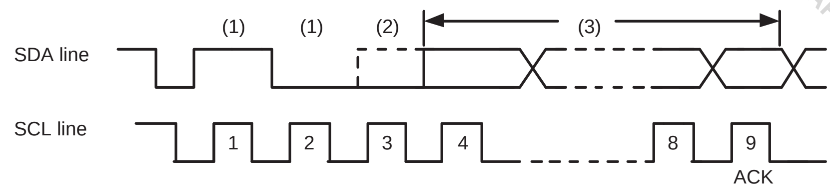
37.9.6 Arbitration and synchronization logic

In the master transmitter mode, the arbitration logic checks that every transmitted logic 1 actually appears as a logic 1 on the I^{2}C-bus. If another device on the bus overrules a logic 1 and pulls the SDA line low, arbitration is lost, and the I^{2}C block immediately changes from master transmitter to slave receiver. The I^{2}C block will continue to output clock pulses (on SCL) until transmission of the current serial byte is complete.

Arbitration may also be lost in the master receiver mode. Loss of arbitration in this mode can only occur while the I^{2}C block is returning a “not acknowledge”: (logic 1) to the bus. Arbitration is lost when another device on the bus pulls this signal low. Since this can occur only at the end of a serial byte, the I^{2}C block generates no further clock pulses. Figure 138 shows the arbitration procedure.

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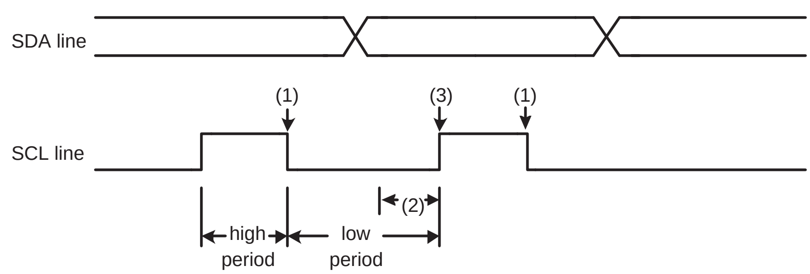
(1) Another device transmits serial data.

(2) Another device overrules a logic (dotted line) transmitted this I²C master by pulling the SDA line low. Arbitration is lost, and this I²C enters Slave Receiver mode.

(3) This I²C is in Slave Receiver mode but still generates clock pulses until the current byte has been transmitted. This I²C will not generate clock pulses for the next byte. Data on SDA originates from the new master once it has won arbitration.

Fig 138. Arbitration procedure

The synchronization logic will synchronize the serial clock generator with the clock pulses on the SCL line from another device. If two or more master devices generate clock pulses, the “mark” duration is determined by the device that generates the shortest “marks”, and the “space” duration is determined by the device that generates the longest “spaces”. Figure 139 shows the synchronization procedure.



(1) Another device pulls the SCL line low before this I²C has timed a complete high time. The other device effectively determines the (shorter) HIGH period.

(2) Another device continues to pull the SCL line low after this I²C has timed a complete low time and released SCL. The I²C clock generator is forced to wait until SCL goes HIGH. The other device effectively determines the (longer) LOW period.

(3) The SCL line is released , and the clock generator begins timing the HIGH time.

Fig 139. Serial clock synchronization

A slave may stretch the space duration to slow down the bus master. The space duration may also be stretched for handshaking purposes. This can be done after each bit or after a complete byte transfer. the I²C block will stretch the SCL space duration after a byte has been transmitted or received and the acknowledge bit has been transferred. The serial interrupt flag (SI) is set, and the stretching continues until the serial interrupt flag is cleared.

37.9.7 Serial clock generator

This programmable clock pulse generator provides the SCL clock pulses when the I²C block is in the master transmitter or master receiver mode. It is switched off when the I²C block is in slave mode. The I²C output clock frequency and duty cycle is programmable

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via the I^{2}C Clock Control Registers. See the description of the SCLL and SCLH registers for details. The output clock pulses have a duty cycle as programmed unless the bus is synchronizing with other SCL clock sources as described above.

37.9.8 Timing and control

The timing and control logic generates the timing and control signals for serial byte handling. This logic block provides the shift pulses for DAT, enables the comparator, generates and detects START and STOP conditions, receives and transmits acknowledge bits, controls the master and slave modes, contains interrupt request logic, and monitors the I^{2}C-bus status.

37.9.9 Control register, CONSET and CONCLR

The I^{2}C control register contains bits used to control the following I^{2}C block functions: start and restart of a serial transfer, termination of a serial transfer, bit rate, address recognition, and acknowledgment.

The contents of the I^{2}C control register may be read as CONSET. Writing to CONSET will set bits in the I^{2}C control register that correspond to ones in the value written. Conversely, writing to CONCLR will clear bits in the I^{2}C control register that correspond to ones in the value written.

37.9.10 Status decoder and status register

The status decoder takes all of the internal status bits and compresses them into a 5-bit code. This code is unique for each I^{2}C-bus status. The 5-bit code may be used to generate vector addresses for fast processing of the various service routines. Each service routine processes a particular bus status. There are 26 possible bus states if all four modes of the I^{2}C block are used. The 5-bit status code is latched into the five most significant bits of the status register when the serial interrupt flag is set (by hardware) and remains stable until the interrupt flag is cleared by software. The three least significant bits of the status register are always zero. If the status code is used as a vector to service routines, then the routines are displaced by eight address locations. Eight bytes of code is sufficient for most of the service routines (see the software example in this section).

37.10 Details of I^{2}C operating modes

The four operating modes are:

- Master Transmitter
- Master Receiver
- Slave Receiver
- Slave Transmitter

Data transfers in each mode of operation are shown in Figure 140, Figure 141, Figure 142, Figure 143, and Figure 144. Table 816 lists abbreviations used in these figures when describing the I^{2}C operating modes.

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Table 816. Abbreviations used to describe an I^{2}C operation

Abbreviation	Explanation
S	START Condition
SLA	7-bit slave address
R	Read bit (HIGH level at SDA)
W	Write bit (LOW level at SDA)
A	Acknowledge bit (LOW level at SDA)
$\overline{A}$	Not acknowledge bit (HIGH level at SDA)
Data	8-bit data byte
P	STOP condition

In Figure 140 to Figure 144, circles are used to indicate when the serial interrupt flag is set. The numbers in the circles show the status code held in the STAT register. At these points, a service routine must be executed to continue or complete the serial transfer. These service routines are not critical since the serial transfer is suspended until the serial interrupt flag is cleared by software.

When a serial interrupt routine is entered, the status code in STAT is used to branch to the appropriate service routine. For each status code, the required software action and details of the following serial transfer are given in tables from Table 818 to Table 824.

37.10.1 Master Transmitter mode

In the master transmitter mode, a number of data bytes are transmitted to a slave receiver (see Figure 140). Before the master transmitter mode can be entered, CON must be initialized as follows:

Table 817. CONSET used to initialize Master Transmitter mode

Bit	7	6	5	4	3	2	1	0
Symbol	-	I2EN	STA	STO	SI	AA	-	-
Value	-	1	0	0	0	x	-	-

The I^{2}C rate must also be configured in the SCLL and SCLH registers. I2EN must be set to logic 1 to enable the I^{2}C block. If the AA bit is reset, the I^{2}C block will not acknowledge its own slave address or the General Call address in the event of another device becoming master of the bus. In other words, if AA is reset, the I^{2}C interface cannot enter slave mode. STA, STO, and SI must be reset.

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The master transmitter mode may now be entered by setting the STA bit. The I^2C logic will now test the I^2C-bus and generate a START condition as soon as the bus becomes free. When a START condition is transmitted, the serial interrupt flag (SI) is set, and the status code in the status register (STAT) will be 0x08. This status code is used by the interrupt service routine to enter the appropriate state service routine that loads DAT with the slave address and the data direction bit (SLA+W). The SI bit in CON must then be reset before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgment bit has been received, the serial interrupt flag (SI) is set again, and a number of status codes in STAT are possible. There are 0x18, 0x20, or 0x38 for the master mode and also 0x68, 0x78, or 0xB0 if the slave mode was enabled (AA = logic 1). The appropriate action to be taken for each of these status codes is detailed in Table 818. After a Repeated START condition (state 0x10). The I^2C block may switch to the master receiver mode by loading DAT with SLA+R).

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Table 818. Master Transmitter mode

Status Code (STAT)	Status of the I²C-bus and hardware	Application software response					Next action taken by I²C hardware
		To/From DAT	To CON				
			STA	STO	SI	AA	
0x08	A START condition has been transmitted.	Load SLA+W; clear STA	X	0	0	X	SLA+W will be transmitted; ACK bit will be received.
0x10	A Repeated START condition has been transmitted.	Load SLA+W or	X	0	0	X	As above.
		Load SLA+R; Clear STA	X	0	0	X	SLA+R will be transmitted; the I²C block will be switched to MST/REC mode.
0x18	SLA+W has been transmitted; ACK has been received.	Load data byte or	0	0	0	X	Data byte will be transmitted; ACK bit will be received.
		No DAT action or	1	0	0	X	Repeated START will be transmitted.
		No DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		No DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
0x20	SLA+W has been transmitted; NOT ACK has been received.	Load data byte or	0	0	0	X	Data byte will be transmitted; ACK bit will be received.
		No DAT action or	1	0	0	X	Repeated START will be transmitted.
		No DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		No DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
0x28	Data byte in DAT has been transmitted; ACK has been received.	Load data byte or	0	0	0	X	Data byte will be transmitted; ACK bit will be received.
		No DAT action or	1	0	0	X	Repeated START will be transmitted.
		No DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		No DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
0x30	Data byte in DAT has been transmitted; NOT ACK has been received.	Load data byte or	0	0	0	X	Data byte will be transmitted; ACK bit will be received.
		No DAT action or	1	0	0	X	Repeated START will be transmitted.
		No DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		No DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
0x38	Arbitration lost in SLA+R/W or Data bytes.	No DAT action or	0	0	0	X	I²C-bus will be released; not addressed slave will be entered.
		No DAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free.

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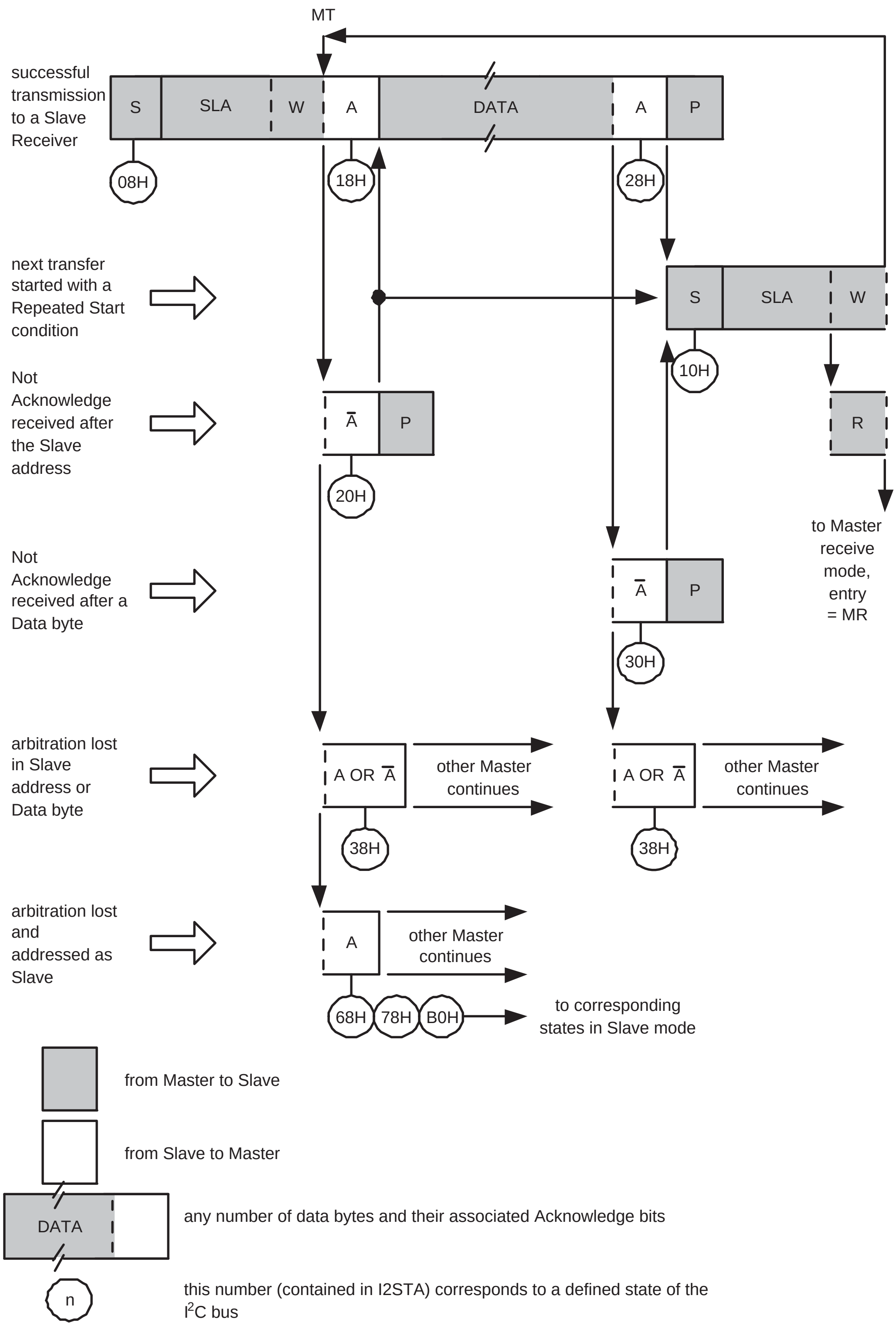


Fig 140. Format and states in the Master Transmitter mode

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37.10.2 Master Receiver mode

In the master receiver mode, a number of data bytes are received from a slave transmitter (see Figure 141). The transfer is initialized as in the master transmitter mode. When the START condition has been transmitted, the interrupt service routine must load DAT with the 7-bit slave address and the data direction bit (SLA+R). The SI bit in CON must then be cleared before the serial transfer can continue.

When the slave address and the data direction bit have been transmitted and an acknowledgment bit has been received, the serial interrupt flag (SI) is set again, and a number of status codes in STAT are possible. These are 0x40, 0x48, or 0x38 for the master mode and also 0x68, 0x78, or 0xB0 if the slave mode was enabled (AA = 1). The appropriate action to be taken for each of these status codes is detailed in Table 819. After a Repeated START condition (state 0x10), the I^2C block may switch to the master transmitter mode by loading DAT with SLA+W.

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Table 819. Master Receiver mode

Status Code (STAT)	Status of the I²C-bus and hardware	Application software response					Next action taken by I²C hardware
		To/From DAT	To CON				
			STA	STO	SI	AA	
0x08	A START condition has been transmitted.	Load SLA+R	X	0	0	X	SLA+R will be transmitted; ACK bit will be received.
0x10	A Repeated START condition has been transmitted.	Load SLA+R or	X	0	0	X	As above.
		Load SLA+W	X	0	0	X	SLA+W will be transmitted; the I²C block will be switched to MST/TRX mode.
0x38	Arbitration lost in NOT ACK bit.	No DAT action or	0	0	0	X	I²C-bus will be released; the I²C block will enter slave mode.
		No DAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free.
0x40	SLA+R has been transmitted; ACK has been received.	No DAT action or	0	0	0	0	Data byte will be received; NOT ACK bit will be returned.
		No DAT action	0	0	0	1	Data byte will be received; ACK bit will be returned.
0x48	SLA+R has been transmitted; NOT ACK has been received.	No DAT action or	1	0	0	X	Repeated START condition will be transmitted.
		No DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		No DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
0x50	Data byte has been received; ACK has been returned.	Read data byte or	0	0	0	0	Data byte will be received; NOT ACK bit will be returned.
		Read data byte	0	0	0	1	Data byte will be received; ACK bit will be returned.
0x58	Data byte has been received; NOT ACK has been returned.	Read data byte or	1	0	0	X	Repeated START condition will be transmitted.
		Read data byte or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		Read data byte	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.

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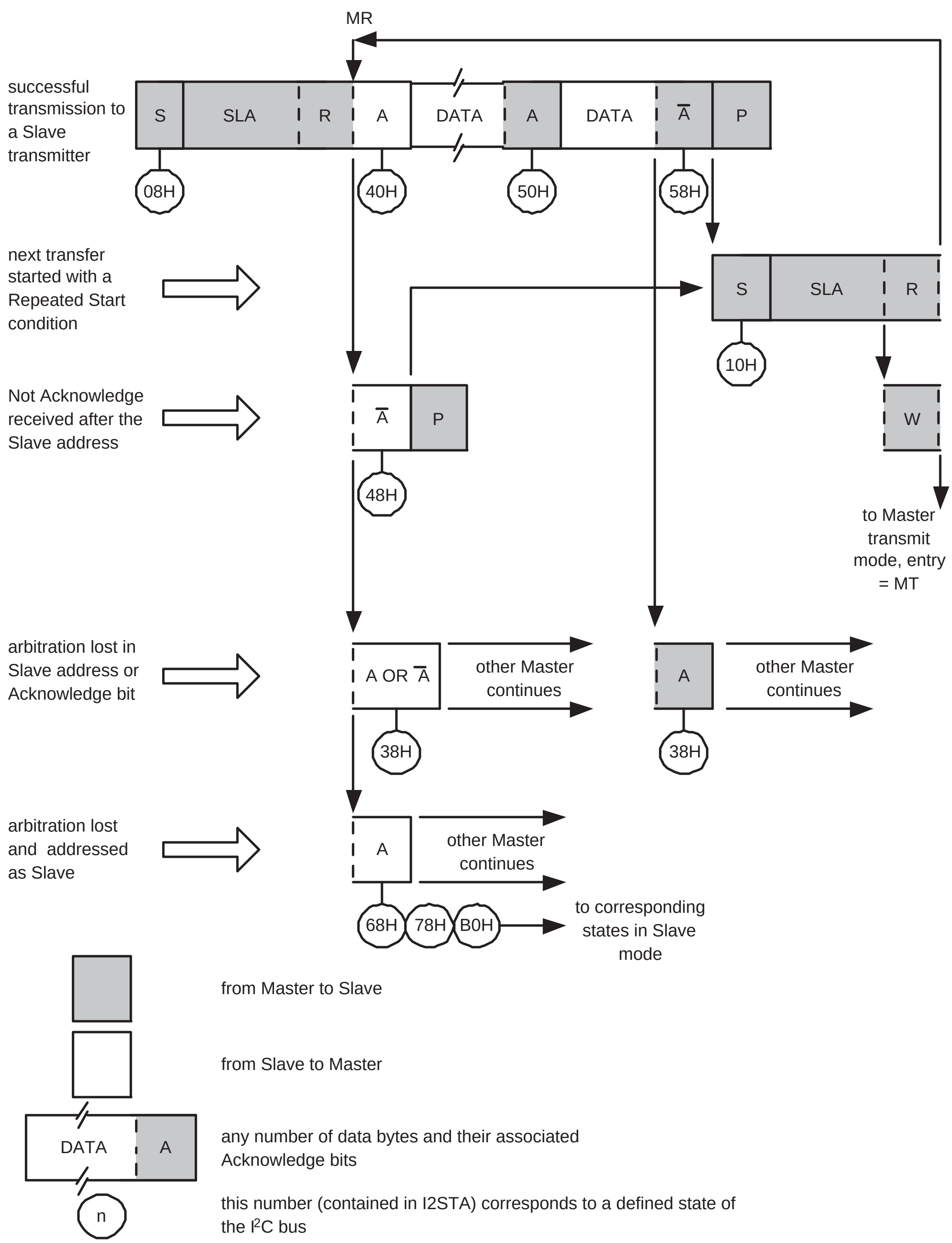


Fig 141. Format and states in the Master Receiver mode

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37.10.3 Slave Receiver mode

In the slave receiver mode, a number of data bytes are received from a master transmitter (see Figure 142). To initiate the slave receiver mode, ADR and CON must be loaded as follows:

Table 820. ADR usage in Slave Receiver mode

Bit	7	6	5	4	3	2	1	0
Symbol	own slave 7-bit address							GC

The upper 7 bits are the address to which the I²C block will respond when addressed by a master. If the LSB (GC) is set, the I²C block will respond to the General Call address (0x00); otherwise it ignores the General Call address.

Table 821. CONSET used to initialize Slave Receiver mode

Bit	7	6	5	4	3	2	1	0
Symbol	-	I2EN	STA	STO	SI	AA	-	-
Value	-	1	0	0	0	1	-	-

The I²C-bus rate settings do not affect the I²C block in the slave mode. I2EN must be set to logic 1 to enable the I²C block. The AA bit must be set to enable the I²C block to acknowledge its own slave address or the General Call address. STA, STO, and SI must be reset.

When ADR and CON have been initialized, the I²C block waits until it is addressed by its own slave address followed by the data direction bit which must be "0" (W) for the I²C block to operate in the slave receiver mode. After its own slave address and the W bit have been received, the serial interrupt flag (SI) is set and a valid status code can be read from STAT. This status code is used to vector to a state service routine. The appropriate action to be taken for each of these status codes is detailed in Table 822. The slave receiver mode may also be entered if arbitration is lost while the I²C block is in the master mode (see status 0x68 and 0x78).

If the AA bit is reset during a transfer, the I²C block will return a not acknowledge (logic 1) to SDA after the next received data byte. While AA is reset, the I²C block does not respond to its own slave address or a General Call address. However, the I²C-bus is still monitored and address recognition may be resumed at any time by setting AA. This means that the AA bit may be used to temporarily isolate the I²C block from the I²C-bus.

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Table 822. Slave Receiver mode

Status Code (STAT)	Status of the I²C-bus and hardware	Application software response					Next action taken by I²C hardware
		To/From DAT	To CON				
			STA	STO	SI	AA	
0x60	Own SLA+W has been received; ACK has been returned.	No DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No DAT action	X	0	0	1	Data byte will be received and ACK will be returned.
0x68	Arbitration lost in SLA+R/W as master; Own SLA+W has been received, ACK returned.	No DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No DAT action	X	0	0	1	Data byte will be received and ACK will be returned.
0x70	General call address (0x00) has been received; ACK has been returned.	No DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No DAT action	X	0	0	1	Data byte will be received and ACK will be returned.
0x78	Arbitration lost in SLA+R/W as master; General call address has been received, ACK has been returned.	No DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No DAT action	X	0	0	1	Data byte will be received and ACK will be returned.
0x80	Previously addressed with own SLV address; DATA has been received; ACK has been returned.	Read data byte or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.
0x88	Previously addressed with own SLA; DATA byte has been received; NOT ACK has been returned.	Read data byte or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address.
		Read data byte or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1.
		Read data byte or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free.
		Read data byte	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1. A START condition will be transmitted when the bus becomes free.
0x90	Previously addressed with General Call; DATA byte has been received; ACK has been returned.	Read data byte or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.

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Table 822. Slave Receiver mode *…continued*

Status Code (STAT)	Status of the I²C-bus and hardware	Application software response					Next action taken by I²C hardware
		To/From DAT	To CON				
			STA	STO	SI	AA	
0x98	Previously addressed with General Call; DATA byte has been received; NOT ACK has been returned.	Read data byte or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address.
		Read data byte or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1.
		Read data byte or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free.
		Read data byte	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1. A START condition will be transmitted when the bus becomes free.
0xA0	A STOP condition or Repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.	No STDAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address.
		No STDAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1.
		No STDAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free.
		No STDAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1. A START condition will be transmitted when the bus becomes free.

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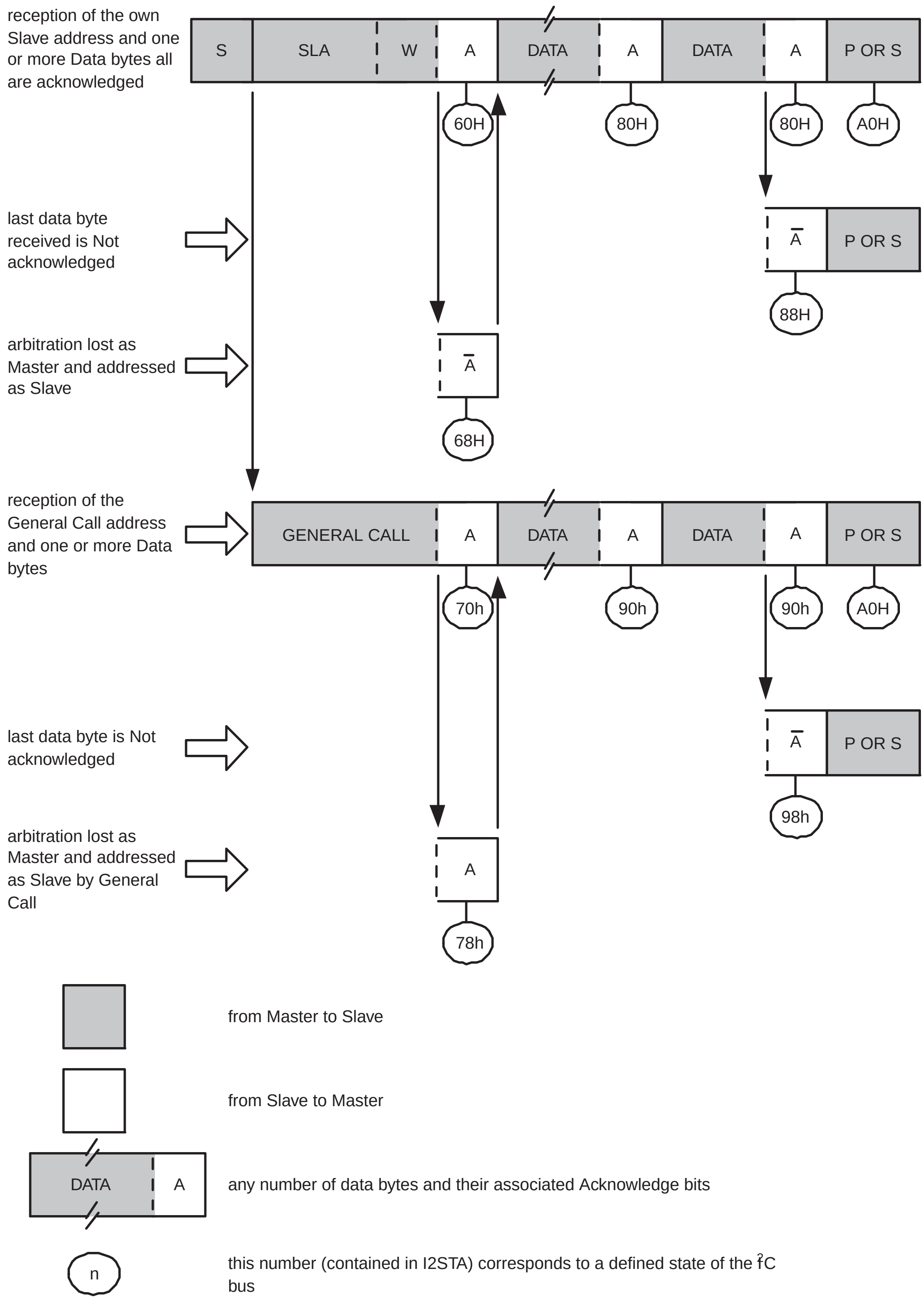


Fig 142. Format and states in the Slave Receiver mode

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37.10.4 Slave Transmitter mode

In the slave transmitter mode, a number of data bytes are transmitted to a master receiver (see Figure 143). Data transfer is initialized as in the slave receiver mode. When ADR and CON have been initialized, the I^2C block waits until it is addressed by its own slave address followed by the data direction bit which must be “1” (R) for the I^2C block to operate in the slave transmitter mode. After its own slave address and the R bit have been received, the serial interrupt flag (SI) is set and a valid status code can be read from STAT. This status code is used to vector to a state service routine, and the appropriate action to be taken for each of these status codes is detailed in Table 823. The slave transmitter mode may also be entered if arbitration is lost while the I^2C block is in the master mode (see state 0xB0).

If the AA bit is reset during a transfer, the I^2C block will transmit the last byte of the transfer and enter state 0xC0 or 0xC8. The I^2C block is switched to the not addressed slave mode and will ignore the master receiver if it continues the transfer. Thus the master receiver receives all 1s as serial data. While AA is reset, the I^2C block does not respond to its own slave address or a General Call address. However, the I^2C-bus is still monitored, and address recognition may be resumed at any time by setting AA. This means that the AA bit may be used to temporarily isolate the I^2C block from the I^2C-bus.

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Table 823. Slave Transmitter mode

Status Code (STAT)	Status of the I²C-bus and hardware	Application software response					Next action taken by I²C hardware
		To/From DAT	To CON				
			STA	STO	SI	AA	
0xA8	Own SLA+R has been received; ACK has been returned.	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received.
		Load data byte	X	0	0	1	Data byte will be transmitted; ACK will be received.
0xB0	Arbitration lost in SLA+R/W as master; Own SLA+R has been received, ACK has been returned.	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received.
		Load data byte	X	0	0	1	Data byte will be transmitted; ACK bit will be received.
0xB8	Data byte in DAT has been transmitted; ACK has been received.	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received.
		Load data byte	X	0	0	1	Data byte will be transmitted; ACK bit will be received.
0xC0	Data byte in DAT has been transmitted; NOT ACK has been received.	No DAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address.
		No DAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1.
		No DAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free.
		No DAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1. A START condition will be transmitted when the bus becomes free.
0xC8	Last data byte in DAT has been transmitted (AA = 0); ACK has been received.	No DAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address.
		No DAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1.
		No DAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free.
		No DAT action	1	0	0	01	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR.0 = logic 1. A START condition will be transmitted when the bus becomes free.

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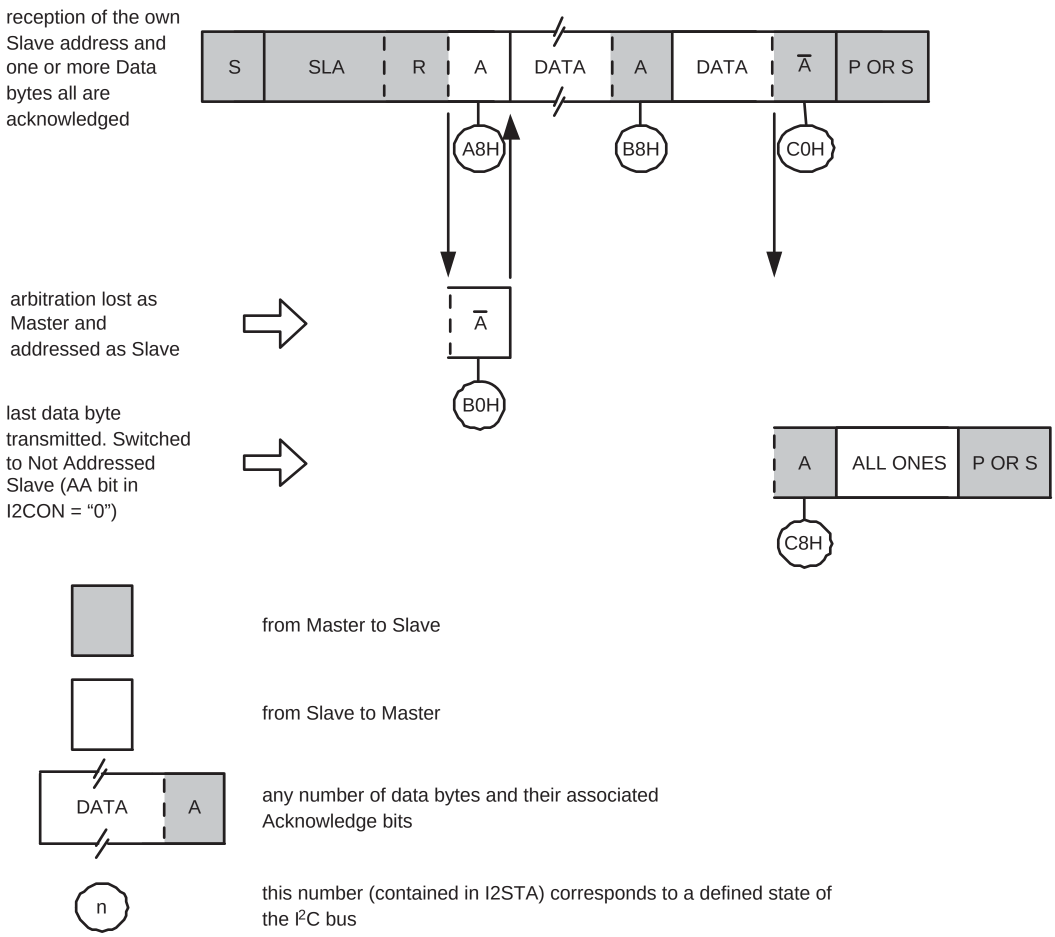


Fig 143. Format and states in the Slave Transmitter mode

37.10.5 Miscellaneous states

There are two STAT codes that do not correspond to a defined I²C hardware state (see Table 824). These are discussed below.

37.10.5.1 STAT = 0xF8

This status code indicates that no relevant information is available because the serial interrupt flag, SI, is not yet set. This occurs between other states and when the I²C block is not involved in a serial transfer.

37.10.5.2 STAT = 0x00

This status code indicates that a bus error has occurred during an I²C serial transfer. A bus error is caused when a START or STOP condition occurs at an illegal position in the format frame. Examples of such illegal positions are during the serial transfer of an address byte, a data byte, or an acknowledge bit. A bus error may also be caused when external interference disturbs the internal I²C block signals. When a bus error occurs, SI is set. To recover from a bus error, the STO flag must be set and SI must be cleared. This

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causes the I^{2}C block to enter the “not addressed” slave mode (a defined state) and to clear the STO flag (no other bits in CON are affected). The SDA and SCL lines are released (a STOP condition is not transmitted).

Table 824. Miscellaneous States

Status Code (STAT)	Status of the I^{2}C-bus and hardware	Application software response					Next action taken by I^{2}C hardware
		To/From DAT	To CON				
			STA	STO	SI	AA	
0xF8	No relevant state information available; SI = 0.	No DAT action	No CON action				Wait or proceed current transfer.
0x00	Bus error during MST or selected slave modes, due to an illegal START or STOP condition. State 0x00 can also occur when interference causes the I^{2}C block to enter an undefined state.	No DAT action	0	1	0	X	Only the internal hardware is affected in the MST or addressed SLV modes. In all cases, the bus is released and the I^{2}C block is switched to the not addressed SLV mode. STO is reset.

37.10.6 Some special cases

The I^{2}C hardware has facilities to handle the following special cases that may occur during a serial transfer:

- Simultaneous Repeated START conditions from two masters
- Data transfer after loss of arbitration
- Forced access to the I^{2}C-bus
- I^{2}C-bus obstructed by a LOW level on SCL or SDA
- Bus error

37.10.6.1 Simultaneous Repeated START conditions from two masters

A Repeated START condition may be generated in the master transmitter or master receiver modes. A special case occurs if another master simultaneously generates a Repeated START condition (see Figure 144). Until this occurs, arbitration is not lost by either master since they were both transmitting the same data.

If the I^{2}C hardware detects a Repeated START condition on the I^{2}C-bus before generating a Repeated START condition itself, it will release the bus, and no interrupt request is generated. If another master frees the bus by generating a STOP condition, the I^{2}C block will transmit a normal START condition (state 0x08), and a retry of the total serial data transfer can commence.

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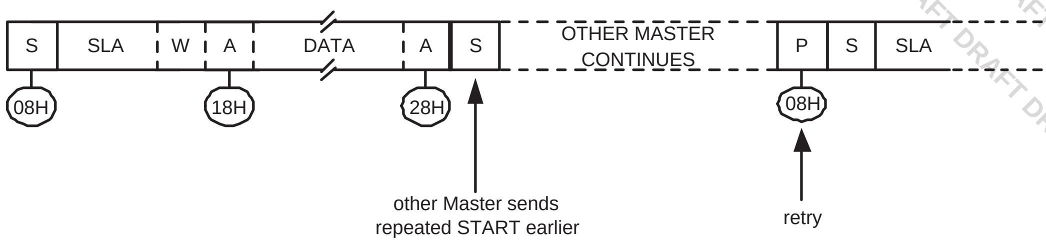


Fig 144. Simultaneous Repeated START conditions from two masters

37.10.6.2 Data transfer after loss of arbitration

Arbitration may be lost in the master transmitter and master receiver modes (see Figure 138). Loss of arbitration is indicated by the following states in STAT; 0x38, 0x68, 0x78, and 0xB0 (see Figure 140 and Figure 141).

If the STA flag in CON is set by the routines which service these states, then, if the bus is free again, a START condition (state 0x08) is transmitted without intervention by the CPU, and a retry of the total serial transfer can commence.

37.10.6.3 Forced access to the I^{2}C-bus

In some applications, it may be possible for an uncontrolled source to cause a bus hang-up. In such situations, the problem may be caused by interference, temporary interruption of the bus or a temporary short-circuit between SDA and SCL.

If an uncontrolled source generates a superfluous START or masks a STOP condition, then the I^{2}C-bus stays busy indefinitely. If the STA flag is set and bus access is not obtained within a reasonable amount of time, then a forced access to the I^{2}C-bus is possible. This is achieved by setting the STO flag while the STA flag is still set. No STOP condition is transmitted. The I^{2}C hardware behaves as if a STOP condition was received and is able to transmit a START condition. The STO flag is cleared by hardware (see Figure 145).

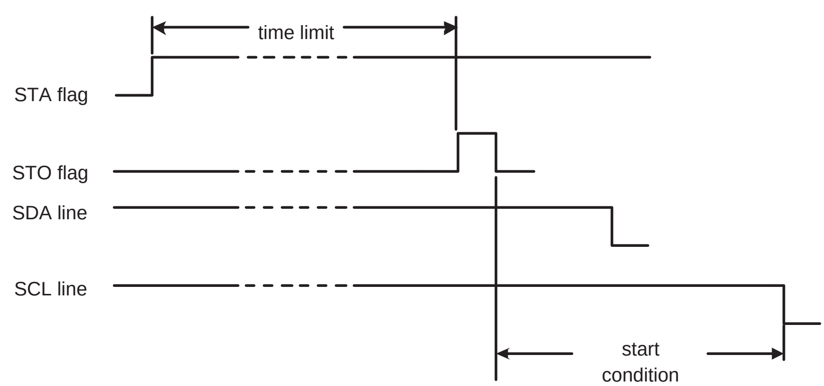


Fig 145. Forced access to a busy I^{2}C-bus

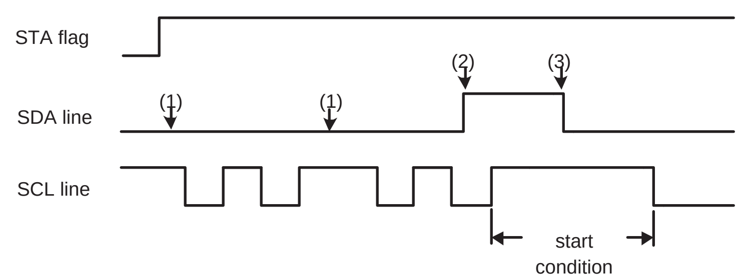
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37.10.6.4 I²C-bus obstructed by a LOW level on SCL or SDA

An I²C-bus hang-up can occur if either the SDA or SCL line is held LOW by any device on the bus. If the SCL line is obstructed (pulled LOW) by a device on the bus, no further serial transfer is possible, and the problem must be resolved by the device that is pulling the SCL bus line LOW.

Typically, the SDA line may be obstructed by another device on the bus that has become out of synchronization with the current bus master by either missing a clock, or by sensing a noise pulse as a clock. In this case, the problem can be solved by transmitting additional clock pulses on the SCL line (see Figure 146). The I²C interface does not include a dedicated time-out timer to detect an obstructed bus, but this can be implemented using another timer in the system. When detected, software can force clocks (up to 9 may be required) on SCL until SDA is released by the offending device. At that point, the slave may still be out of synchronization, so a START should be generated to insure that all I²C peripherals are synchronized.



(1) Unsuccessful attempt to send a START condition.

(2) SDA line is released.

(3) Successful attempt to send a START condition. State 08H is entered.

Fig 146. Recovering from a bus obstruction caused by a LOW level on SDA

37.10.6.5 Bus error

A bus error occurs when a START or STOP condition is detected at an illegal position in the format frame. Examples of illegal positions are during the serial transfer of an address byte, a data bit, or an acknowledge bit.

The I²C hardware only reacts to a bus error when it is involved in a serial transfer either as a master or an addressed slave. When a bus error is detected, the I²C block immediately switches to the not addressed slave mode, releases the SDA and SCL lines, sets the interrupt flag, and loads the status register with 0x00. This status code may be used to vector to a state service routine which either attempts the aborted serial transfer again or simply recovers from the error condition as shown in Table 824.

37.10.7 I²C state service routines

This section provides examples of operations that must be performed by various I²C state service routines. This includes:

- Initialization of the I²C block after a Reset.
- I²C Interrupt Service
- The 26 state service routines providing support for all four I²C operating modes.

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37.10.8 Initialization

In the initialization example, the I^{2}C block is enabled for both master and slave modes. For each mode, a buffer is used for transmission and reception. The initialization routine performs the following functions:

- I2ADR is loaded with the part's own slave address and the General Call bit (GC)
- The I^{2}C interrupt enable and interrupt priority bits are set
- The slave mode is enabled by simultaneously setting the I2EN and AA bits in CON and the serial clock frequency (for master modes) is defined by is defined by loading the SCLH and SCLL registers. The master routines must be started in the main program.

The I^{2}C hardware now begins checking the I^{2}C-bus for its own slave address and General Call. If the General Call or the own slave address is detected, an interrupt is requested and STAT is loaded with the appropriate state information.

37.10.9 I^{2}C interrupt service

When the I^{2}C interrupt is entered, STAT contains a status code which identifies one of the 26 state services to be executed.

37.10.10 The state service routines

Each state routine is part of the I^{2}C interrupt routine and handles one of the 26 states.

37.10.11 Adapting state services to an application

The state service examples show the typical actions that must be performed in response to the 26 I^{2}C state codes. If one or more of the four I^{2}C operating modes are not used, the associated state services can be omitted, as long as care is taken that the those states can never occur.

In an application, it may be desirable to implement some kind of time-out during I^{2}C operations, in order to trap an inoperative bus or a lost service routine.

37.11 Software example

37.11.1 Initialization routine

Example to initialize I^{2}C Interface as a Slave and/or Master.

1. Load ADR with own Slave Address, enable General Call recognition if needed.
2. Enable I^{2}C interrupt.
3. Write 0x44 to CONSET to set the I2EN and AA bits, enabling Slave functions. For Master only functions, write 0x40 to CONSET.

37.11.2 Start Master Transmit function

Begin a Master Transmit operation by setting up the buffer, pointer, and data count, then initiating a START.

1. Initialize Master data counter.

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2. Set up the Slave Address to which data will be transmitted, and add the Write bit.
3. Write 0x20 to CONSET to set the STA bit.
4. Set up data to be transmitted in Master Transmit buffer.
5. Initialize the Master data counter to match the length of the message being sent.
6. Exit

37.11.3 Start Master Receive function

Begin a Master Receive operation by setting up the buffer, pointer, and data count, then initiating a START.

1. Initialize Master data counter.
2. Set up the Slave Address to which data will be transmitted, and add the Read bit.
3. Write 0x20 to CONSET to set the STA bit.
4. Set up the Master Receive buffer.
5. Initialize the Master data counter to match the length of the message to be received.
6. Exit

37.11.4 I^{2}C interrupt routine

Determine the I^{2}C state and which state routine will be used to handle it.

1. Read the I^{2}C status from STA.
2. Use the status value to branch to one of 26 possible state routines.

37.11.5 Non mode specific states

37.11.5.1 State: 0x00

Bus Error. Enter not addressed Slave mode and release bus.

1. Write 0x14 to CONSET to set the STO and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit

37.11.5.2 Master States

State 08 and State 10 are for both Master Transmit and Master Receive modes. The R/W bit decides whether the next state is within Master Transmit mode or Master Receive mode.

37.11.5.3 State: 0x08

A START condition has been transmitted. The Slave Address + R/W bit will be transmitted, an ACK bit will be received.

1. Write Slave Address with R/W bit to DAT.
2. Write 0x04 to CONSET to set the AA bit.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Set up Master Transmit mode data buffer.

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5. Set up Master Receive mode data buffer.
6. Initialize Master data counter.
7. Exit

37.11.5.4 State: 0x10

A Repeated START condition has been transmitted. The Slave Address + R/W bit will be transmitted, an ACK bit will be received.

1. Write Slave Address with R/W bit to DAT.
2. Write 0x04 to CONSET to set the AA bit.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Set up Master Transmit mode data buffer.
5. Set up Master Receive mode data buffer.
6. Initialize Master data counter.
7. Exit

37.11.6 Master Transmitter states

37.11.6.1 State: 0x18

Previous state was State 8 or State 10, Slave Address + Write has been transmitted, ACK has been received. The first data byte will be transmitted, an ACK bit will be received.

1. Load DAT with first data byte from Master Transmit buffer.
2. Write 0x04 to CONSET to set the AA bit.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Increment Master Transmit buffer pointer.
5. Exit

37.11.6.2 State: 0x20

Slave Address + Write has been transmitted, NOT ACK has been received. A STOP condition will be transmitted.

1. Write 0x14 to CONSET to set the STO and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit

37.11.6.3 State: 0x28

Data has been transmitted, ACK has been received. If the transmitted data was the last data byte then transmit a STOP condition, otherwise transmit the next data byte.

1. Decrement the Master data counter, skip to step 5 if not the last data byte.
2. Write 0x14 to CONSET to set the STO and AA bits.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Exit
5. Load DAT with next data byte from Master Transmit buffer.

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6. Write 0x04 to CONSET to set the AA bit.
7. Write 0x08 to CONCLR to clear the SI flag.
8. Increment Master Transmit buffer pointer
9. Exit

37.11.6.4 State: 0x30

Data has been transmitted, NOT ACK received. A STOP condition will be transmitted.

1. Write 0x14 to CONSET to set the STO and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit

37.11.6.5 State: 0x38

Arbitration has been lost during Slave Address + Write or data. The bus has been released and not addressed Slave mode is entered. A new START condition will be transmitted when the bus is free again.

1. Write 0x24 to CONSET to set the STA and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit

37.11.7 Master Receive states

37.11.7.1 State: 0x40

Previous state was State 08 or State 10. Slave Address + Read has been transmitted, ACK has been received. Data will be received and ACK returned.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit

37.11.7.2 State: 0x48

Slave Address + Read has been transmitted, NOT ACK has been received. A STOP condition will be transmitted.

1. Write 0x14 to CONSET to set the STO and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit

37.11.7.3 State: 0x50

Data has been received, ACK has been returned. Data will be read from DAT. Additional data will be received. If this is the last data byte then NOT ACK will be returned, otherwise ACK will be returned.

1. Read data byte from DAT into Master Receive buffer.
2. Decrement the Master data counter, skip to step 5 if not the last data byte.
3. Write 0x0C to CONCLR to clear the SI flag and the AA bit.

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4. Exit
5. Write 0x04 to CONSET to set the AA bit.
6. Write 0x08 to CONCLR to clear the SI flag.
7. Increment Master Receive buffer pointer
8. Exit

37.11.7.4 State: 0x58

Data has been received, NOT ACK has been returned. Data will be read from DAT. A STOP condition will be transmitted.

1. Read data byte from DAT into Master Receive buffer.
2. Write 0x14 to CONSET to set the STO and AA bits.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Exit

37.11.8 Slave Receiver states

37.11.8.1 State: 0x60

Own Slave Address + Write has been received, ACK has been returned. Data will be received and ACK returned.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Set up Slave Receive mode data buffer.
4. Initialize Slave data counter.
5. Exit

37.11.8.2 State: 0x68

Arbitration has been lost in Slave Address and R/W bit as bus Master. Own Slave Address + Write has been received, ACK has been returned. Data will be received and ACK will be returned. STA is set to restart Master mode after the bus is free again.

1. Write 0x24 to CONSET to set the STA and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Set up Slave Receive mode data buffer.
4. Initialize Slave data counter.
5. Exit.

37.11.8.3 State: 0x70

General call has been received, ACK has been returned. Data will be received and ACK returned.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Set up Slave Receive mode data buffer.

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4. Initialize Slave data counter.
5. Exit

37.11.8.4 State: 0x78

Arbitration has been lost in Slave Address + R/W bit as bus Master. General call has been received and ACK has been returned. Data will be received and ACK returned. STA is set to restart Master mode after the bus is free again.

1. Write 0x24 to CONSET to set the STA and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Set up Slave Receive mode data buffer.
4. Initialize Slave data counter.
5. Exit

37.11.8.5 State: 0x80

Previously addressed with own Slave Address. Data has been received and ACK has been returned. Additional data will be read.

1. Read data byte from DAT into the Slave Receive buffer.
2. Decrement the Slave data counter, skip to step 5 if not the last data byte.
3. Write 0x0C to CONCLR to clear the SI flag and the AA bit.
4. Exit.
5. Write 0x04 to CONSET to set the AA bit.
6. Write 0x08 to CONCLR to clear the SI flag.
7. Increment Slave Receive buffer pointer.
8. Exit

37.11.8.6 State: 0x88

Previously addressed with own Slave Address. Data has been received and NOT ACK has been returned. Received data will not be saved. Not addressed Slave mode is entered.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit

37.11.8.7 State: 0x90

Previously addressed with General Call. Data has been received, ACK has been returned. Received data will be saved. Only the first data byte will be received with ACK. Additional data will be received with NOT ACK.

1. Read data byte from DAT into the Slave Receive buffer.
2. Write 0x0C to CONCLR to clear the SI flag and the AA bit.
3. Exit

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37.11.8.8 State: 0x98

Previously addressed with General Call. Data has been received, NOT ACK has been returned. Received data will not be saved. Not addressed Slave mode is entered.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit

37.11.8.9 State: 0xA0

A STOP condition or Repeated START has been received, while still addressed as a Slave. Data will not be saved. Not addressed Slave mode is entered.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit

37.11.9 Slave Transmitter states

37.11.9.1 State: 0xA8

Own Slave Address + Read has been received, ACK has been returned. Data will be transmitted, ACK bit will be received.

1. Load DAT from Slave Transmit buffer with first data byte.
2. Write 0x04 to CONSET to set the AA bit.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Set up Slave Transmit mode data buffer.
5. Increment Slave Transmit buffer pointer.
6. Exit

37.11.9.2 State: 0xB0

Arbitration lost in Slave Address and R/W bit as bus Master. Own Slave Address + Read has been received, ACK has been returned. Data will be transmitted, ACK bit will be received. STA is set to restart Master mode after the bus is free again.

1. Load DAT from Slave Transmit buffer with first data byte.
2. Write 0x24 to CONSET to set the STA and AA bits.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Set up Slave Transmit mode data buffer.
5. Increment Slave Transmit buffer pointer.
6. Exit

37.11.9.3 State: 0xB8

Data has been transmitted, ACK has been received. Data will be transmitted, ACK bit will be received.

1. Load DAT from Slave Transmit buffer with data byte.

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2. Write 0x04 to CONSET to set the AA bit.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Increment Slave Transmit buffer pointer.
5. Exit

37.11.9.4 State: 0xC0

Data has been transmitted, NOT ACK has been received. Not addressed Slave mode is entered.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit.

37.11.9.5 State: 0xC8

The last data byte has been transmitted, ACK has been received. Not addressed Slave mode is entered.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit

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38.1 How to read this chapter

The ADC0 and ADC1 are available on all LPC18xx parts.

The following configuration options apply to parts LPC1850_30_20_10 Rev 'A' only:

- The ADC start inputs are configured through the GIMA (see Section 14.3).
- The ADC0 and ADC1 functions are multiplexed with digital functions and need to be configured using the ENAIO0/1 registers (see Section 13.4.3 and Section 13.4.5.

38.2 Basic configuration

The ADC0 and ADC1 are configured as follows:

- See Table 825 for clocking and power control.
- The ADC0 is reset by the ADC0_RST (reset # 40).
- The ADC1 is reset by the ADC1_RST (reset # 41).
- The ADC0 interrupt is connected to interrupt slot # 17 in the NVIC.
- The ADC1 interrupt is connected to interrupt slot # 21 in the NVIC.
- For connecting to the GPDMA, use the DMAMUX register (Table 35) in the CREG block and enable the GPDMA channel in the DMA Channel Configuration registers Section 16.6.20.
- External pins (ADCTRIG0/1), the MOTOCON PWM MCOA2 output, and two SCT outputs can be selected as conversion triggers for ADC0/1 (see Figure 25).
- The ADC start inputs are configured through the GIMA (see Section 14.3).
- The ADC0 and ADC1 functions are multiplexed with digital functions and need to be configured using the ENAIO0/1 registers (see Section 13.4.3 and Section 13.4.5.

Table 825. ADC0/1 clocking and power control

	Base clock	Branch clock	Maximum frequency	Notes
ADC0 clock	BASE_APB3_CLK	CLK_APB3_ADC0	150 MHz	For register interface and ADC0 conversion rate.
ADC1 clock	BASE_APB3_CLK	CLK_APB3_ADC1	150 MHz	For register interface and ADC1 conversion rate.

38.3 Features

- 10 bit successive approximation analog to digital converter.

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- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 to 3.3 V.
- 10 bit conversion time ≥ 2.44 μs.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.
- Individual result registers for each A/D channel to reduce interrupt overhead.

38.4 General description

Basic clocking for the A/D converters is provided by the APB clocks (CLK_APB3_ADC0/1). A programmable divider is included in each converter to scale this clock to the 4.5 MHz (max) clock needed by the successive approximation process. A fully accurate conversion requires 11 of these clocks.

38.5 Pin description

Table 826 gives a brief summary of each of ADC related pins.

Table 826. ADC pin description

Pin	Type	Description
ADC[7:0]	Input	Analog Inputs. The A/D converter cell can measure the voltage on any of these input signals. The inputs are shared between ADC0 and ADC1. **Remark:** The ADC0 pin is shared with the DAC0 pin.
ADCTRIG0	Input	Trigger inputs to the ADC0/1.
ADCTRIG1	Input	Trigger inputs to the ADC0/1.
VDDA	Power	Analog Power. Also voltage reference VREF for both ADCs.
VSSA	Ground	Analog ground.

38.6 Register description

The register addresses for the ADC0 are shown in Table 827

Table 827. Register overview: ADC0 (base address 0x400E 3000)

Name	Access	Address offset	Description	Reset value[1]
CR	R/W	0x000	A/D Control Register. The AD0CR register must be written to select the operating mode before A/D conversion can occur.	0x0000 0000
GDR	R0	0x004	A/D Global Data Register. Contains the result of the most recent A/D conversion.	-
-	-	0x008	Reserved.	-

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Table 827. Register overview: ADC0 (base address 0x400E 3000)

Name	Access	Address offset	Description	Reset value[1]
INTEN	R/W	0x00C	A/D Interrupt Enable Register. This register contains enable bits that allow the DONE flag of each A/D channel to be included or excluded from contributing to the generation of an A/D interrupt.	0x0000 0100
DR0	RO	0x010	A/D Channel 0 Data Register. This register contains the result of the most recent conversion completed on channel 0	-
DR1	RO	0x014	A/D Channel 1 Data Register. This register contains the result of the most recent conversion completed on channel 1.	-
DR2	RO	0x018	A/D Channel 2 Data Register. This register contains the result of the most recent conversion completed on channel 2.	-
DR3	RO	0x01C	A/D Channel 3 Data Register. This register contains the result of the most recent conversion completed on channel 3.	-
DR4	RO	0x020	A/D Channel 4 Data Register. This register contains the result of the most recent conversion completed on channel 4.	-
DR5	RO	0x024	A/D Channel 5 Data Register. This register contains the result of the most recent conversion completed on channel 5.	-
DR6	RO	0x028	A/D Channel 6 Data Register. This register contains the result of the most recent conversion completed on channel 6.	-
DR7	RO	0x02C	A/D Channel 7 Data Register. This register contains the result of the most recent conversion completed on channel 7.	-
STAT	RO	0x030	A/D Status Register. This register contains DONE and OVERRUN flags for all of the A/D channels, as well as the A/D interrupt flag.	0

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

Table 828. Register overview: ADC1 (base address 0x400E 4000)

Name	Access	Address offset	Description	Reset value[1]
CR	R/W	0x000	A/D Control Register. The AD1CR register must be written to select the operating mode before A/D conversion can occur.	0x0000 0000
GDR	R0	0x004	A/D Global Data Register. Contains the result of the most recent A/D conversion.	-
-	-	0x008	Reserved.	-
INTEN	R/W	0x00C	A/D Interrupt Enable Register. This register contains enable bits that allow the DONE flag of each A/D channel to be included or excluded from contributing to the generation of an A/D interrupt.	0x0000 0100

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Table 828. Register overview: ADC1 (base address 0x400E 4000)

Name	Access	Address offset	Description	Reset value[1]
DR0	RO	0x010	A/D Channel 0 Data Register. This register contains the result of the most recent conversion completed on channel 0	-
DR1	RO	0x014	A/D Channel 1 Data Register. This register contains the result of the most recent conversion completed on channel 1.	-
DR2	RO	0x018	A/D Channel 2 Data Register. This register contains the result of the most recent conversion completed on channel 2.	-
DR3	RO	0x01C	A/D Channel 3 Data Register. This register contains the result of the most recent conversion completed on channel 3.	-
DR4	RO	0x020	A/D Channel 4 Data Register. This register contains the result of the most recent conversion completed on channel 4.	-
DR5	RO	0x024	A/D Channel 5 Data Register. This register contains the result of the most recent conversion completed on channel 5.	-
DR6	RO	0x028	A/D Channel 6 Data Register. This register contains the result of the most recent conversion completed on channel 6.	-
DR7	RO	0x02C	A/D Channel 7 Data Register. This register contains the result of the most recent conversion completed on channel 7.	-
STAT	RO	0x030	A/D Status Register. This register contains DONE and OVERRUN flags for all of the A/D channels, as well as the A/D interrupt flag.	0

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

38.6.1 A/D Control register

The A/D Control Register provides bits to select A/D channels to be converted, A/D timing, A/D modes, and the A/D start trigger.

Table 829. A/D Control register (CR - address 0x400E 3000 (ADC0) and 0x400E 4000 (ADC1)) bit description

Bit	Symbol	Value	Description	Reset value
7:0	SEL		Selects which of the ADC[7:0] pins are to be sampled and converted. Bit 0 selects Pin ADC0, bit 1 selects pin AD1,..., and bit 7 selects pin ADC7. In software-controlled mode, only one of these bits should be 1. In hardware scan mode, any value containing 1 to 8 ones. All zeroes is equivalent to 0x01.	0
15:8	CLKDIV		The ADC clock is divided by the CLKDIV value plus one to produce the clock for the A/D converter, which should be less than or equal to 4.5 MHz. Typically, software should program the smallest value in this field that yields a clock of 4.5 MHz or slightly less, but in certain cases (such as a high-impedance analog source) a slower clock may be desirable.	0

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Table 829. A/D Control register (CR - address 0x400E 3000 (ADC0) and 0x400E 4000 (ADC1)) bit description

Bit	Symbol	Value	Description	Reset value
16	BURST		Burst mode	0
		0	Conversions are software controlled and require 11 clocks.	
		1	The AD converter does repeated conversions at the rate selected by the CLKS field, scanning (if necessary) through the pins selected by 1s in the SEL field. The first conversion after the start corresponds to the least-significant 1 in the SEL field, then higher numbered 1 bits (pins) if applicable. Repeated conversions can be terminated by clearing this bit, but the conversion that's in progress when this bit is cleared will be completed. **Important:** START bits must be 000 when BURST = 1 or conversions will not start.	
19:17	CLKS		This field selects the number of clocks used for each conversion in Burst mode, and the number of bits of accuracy of the result in the LS bits of ADDR, between 11 clocks (10 bits) and 4 clocks (3 bits).	000
		0x0	11 clocks / 10 bits	
		0x1	10 clocks / 9 bits	
		0x2	9 clocks / 8 bits	
		0x3	8 clocks / 7 bits	
		0x4	7 clocks / 6 bits	
		0x5	6 clocks / 5 bits	
		0x6	5 clocks / 4 bits	
		0x7	4 clocks / 3 bits	
20	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
21	PDN		Power mode	0
		0	The A/D converter is in Power-down mode.	
		1	The A/D converter is operational.	
23:22	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
26:24	START		When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
		0x0	No start (this value should be used when clearing PDN to 0).	
		0x1	Start conversion now.	
		0x2	Start conversion when the edge selected by bit 27 occurs on CTOUT_15 (combined timer output 15, ADC start0).	
		0x3	Start conversion when the edge selected by bit 27 occurs on CTOUT_8 (combined timer output 8, ADC start1).	
		0x4	Start conversion when the edge selected by bit 27 occurs on ADCTRIG0 input (ADC start3).	
		0x5	Start conversion when the edge selected by bit 27 occurs on ADCTRIG1 input (ADC start4).	
		0x6	Start conversion when the edge selected by bit 27 occurs on Motocon PWM output MCOA2 (ADC start5).	
		0x7	Reserved.	

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Table 829. A/D Control register (CR - address 0x400E 3000 (ADC0) and 0x400E 4000 (ADC1)) bit description

Bit	Symbol	Value	Description	Reset value
27	EDGE		This bit is significant only when the START field contains 0x2 -0x6. In these cases:	0
		0	Start conversion on a rising edge on the selected signal.	
		1	Start conversion on a falling edge on the selected signal.	
31:28	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

38.6.2 A/D Global Data register

The A/D Global Data Register contains the result of the most recent A/D conversion. This includes the data, DONE, and Overrun flags, and the number of the A/D channel to which the data relates.

Table 830. A/D Global Data register (GDR - address 0x400E 3004 (ADC0) and 0x400E 4004 (ADC1)) bit description

Bit	Symbol	Description	Reset value
5:0	-	Reserved. These bits always read as zeroes.	0
15:6	V_VREF	When DONE is 1, this field contains a binary fraction representing the voltage on the ADCn pin selected by the SEL field, divided by the reference voltage on the VDDA pin. Zero in the field indicates that the voltage on the ADCn input pin was less than, equal to, or close to that on VSSA, while 0x3FF indicates that the voltage on ADCn input pin was close to, equal to, or greater than that on VDDA.	-
23:16	-	Reserved. These bits always read as zeroes.	0
26:24	CHN	These bits contain the channel from which the LS bits were converted.	-
29:27	-	Reserved. These bits always read as zeroes.	0
30	OVERRUN	This bit is 1 in burst mode if the results of one or more conversions was (were) lost and overwritten before the conversion that produced the result in the V_VREF bits.	0
31	DONE	This bit is set to 1 when an analog-to-digital conversion completes. It is cleared when this register is read and when the AD0/1CR register is written. If the AD0/1CR is written while a conversion is still in progress, this bit is set and a new conversion is started.	0

38.6.3 A/D Interrupt Enable register

This register allows control over which A/D channels generate an interrupt when a conversion is complete. For example, it may be desirable to use some A/D channels to monitor sensors by continuously performing conversions on them. The most recent results are read by the application program whenever they are needed. In this case, an interrupt is not desirable at the end of each conversion for some A/D channels.

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Table 831. A/D Interrupt Enable register (INTEN - address 0x400E 300C (ADC0) and 0x400E 400C (ADC1)) bit description

Bit	Symbol	Description	Reset value
7:0	ADINTEN	These bits allow control over which A/D channels generate interrupts for conversion completion. When bit 0 is one, completion of a conversion on A/D channel 0 will generate an interrupt, when bit 1 is one, completion of a conversion on A/D channel 1 will generate an interrupt, etc.	0x00
8	ADGINTEN	When 1, enables the global DONE flag in ADDR to generate an interrupt. When 0, only the individual A/D channels enabled by ADINTEN 7:0 will generate interrupts.	1
31:9	-	Reserved. Always 0.	0

38.6.4 A/D Data Registers

The A/D Data Register hold the result when an A/D conversion is complete, and also include the flags that indicate when a conversion has been completed and when a conversion overrun has occurred.

Table 832. A/D Data registers (DR - addresses 0x400E 3010 (DR0) to 0x400E 302C (DR7) (ADC0); 0x400E 4010 (DR0) to 0x400E 402C (DR7) (ADC1)) bit description

Bit	Symbol	Description	Reset value
5:0	-	Reserved. Always 0.	0
15:6	V_VREF	When DONE is 1, this field contains a binary fraction representing the voltage on the ADCn input pin selected in Table 829, divided by the voltage on the VDDA pin. Zero in the field indicates that the voltage on the ADCn input pin was less than, equal to, or close to that on VDDA, while 0x3FF indicates that the voltage on ADCn input pin was close to, equal to, or greater than that on VDDA.	-
29:16	-	Reserved. Always 0.	0
30	OVERRUN	This bit is 1 in burst mode if the results of one or more conversions was (were) lost and overwritten before the conversion that produced the result in the V_VREF bits in this register.This bit is cleared by reading this register.	0
31	DONE	This bit is set to 1 when an A/D conversion completes. It is cleared when this register is read.	0

38.6.5 A/D Status register

The A/D Status register allows checking the status of all A/D channels simultaneously. The DONE and OVERRUN flags appearing in the AD0/1DRn register for each A/D channel n are mirrored in ADSTAT. The interrupt flag (the logical OR of all DONE flags) is also found in ADSTAT.

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Table 833. A/D Status register (STAT - address 0x400E 3030 (ADC0) and 0x400E 4030 (ADC1)) bit description

Bit	Symbol	Description	Reset value
7:0	DONE	These bits mirror the DONE status flags that appear in the result register for each A/D channel.	0
15:8	OVERUN	These bits mirror the OVERRRUN status flags that appear in the result register for each A/D channel. Reading ADSTAT allows checking the status of all A/D channels simultaneously.	0
16	ADINT	This bit is the A/D interrupt flag. It is one when any of the individual A/D channel Done flags is asserted and enabled to contribute to the A/D interrupt via the ADINTEN register.	0
31:17	-	Reserved. Always 0.	0

38.7 Operation

38.7.1 Hardware-triggered conversion

If the BURST bit in the ADCR is 0 and the START field contains any value between 0x2 and 0x6, the A/D converter will start a conversion when a transition occurs on a selected pin or Timer signal. The choices include the two ADCTRIG external input pins, an output from the motocon PWM, and two combined timer outputs (see Section 38.6.1).

38.7.2 Interrupts

An interrupt is requested to the Vectored Interrupt Controller (VIC) when the ADINT bit in the ADSTAT register is 1. The ADINT bit is one when any of the DONE bits of A/D channels that are enabled for interrupts (via the ADINTEN register) are one. Software can use the Interrupt Enable bit in the VIC that corresponds to the ADC to control whether this results in an interrupt. The result register for an A/D channel that is generating an interrupt must be read in order to clear the corresponding DONE flag.

38.7.3 DMA control

A DMA transfer request is generated from the ADC interrupt request line. To generate a DMA transfer the same conditions must be met as the conditions for generating an interrupt. A pending DMA request is cleared after the DMA has read from the requesting channel’s A/D data register (DR[7:0]). Reading from the global data register (GDR) does not clear any pending DMA requests.

For DMA transfers, only burst requests are supported. The burst size can be set to one in the DMA channel control register (see Table 214). If the number of ADC channels is not equal to one of the other DMA-supported burst sizes (applicable DMA burst sizes are 1, 4, 8), set the burst size to one.

The DMA transfer size determines when a DMA interrupt is generated. The transfer size can be set to the number of ADC channels being converted (see Section 16.6.19). Non-contiguous channels can be transferred by the DMA using the scatter/gather linked lists (see Section 16.8.5).

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39.1 How to read this chapter

The DAC is available on all LPC18xx parts.

39.2 Basic configuration

The DAC is configured as follows:

- See Table 834 for clocking and power control.
- The DAC is reset by the DAC_RST (reset # 42).
- The DAC interrupt is connected to interrupt slot # 0 in the NVIC.
- For connecting to the GPDMA, use the DMAMUX register (Table 35) in the CREG block and enable the GPDMA channel in the DMA Channel Configuration registers Section 16.6.20.

Table 834. DAC clocking and power control

	Base clock	Branch clock	Maximum frequency	Notes
Clock to the DAC register interface and rate clock for the DMA counter.	BASE_APB3_CLK	CLK_APB3_DAC	150 MHz	-

39.3 Features

- 10-bit resolution
- Monotonic by design (resistor string architecture)
- Controllable conversion speed
- Low power consumption

39.4 Pin description

Table 835 gives a brief summary of each of DAC related pins.

Table 835. DAC pin description

Pin	Type	Description
ADC0	Output	Analog Output. After the selected settling time after the DACR is written with a new value, the voltage on this pin (with respect to V_{SSA}) is VALUE/1024 × VREF. The DACOUT pin is shared with the channel 0 input pin of ADC0 and ADC1.
VDDA	Power	Analog power and voltage reference. This pin provides a voltage reference level for the D/A converter.
VSSA	-	Ground.

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39.5 Register description

Table 836. Register overview: DAC (base address 0x400E 1000)

Name	Access	Address offset	Description	Reset value
CR	R/W	0x000	DAC register. Holds the conversion data.	0
CTRL	R/W	0x004	DAC control register.	0
CNTVAL	R/W	0x008	DAC counter value register.	0

39.5.1 D/A converter register

This read/write register includes the digital value to be converted to an analog output value and a bit that trades off performance vs. power.

Table 837: D/A Converter register (CR - address 0x400E 1000) bit description

Bit	Symbol	Value	Description	Reset value
5:0	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
15:6	VALUE		After the selected settling time after this field is written with a new VALUE, the voltage on the DACOUT pin (with respect to V_{SSA}) is VALUE/1024 $\times$ VDDA.	0
16	BIAS		Settling time	0
		0	The settling time of the DAC is 1 μs max, and the maximum current is 700 μA.	
		1	The settling time of the DAC is 2.5 μs and the maximum current is 350 μA.	
31:17	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

39.5.2 D/A Converter Control register

This read/write register enables the DMA operation and controls the DMA timer.

Table 838. D/A Control register (CTRL - address 0x400E 1004) bit description

Bit	Symbol	Value	Description	Reset value
0	INT_DMA_REQ		DMA request	0
		0	This bit is cleared on any write to the DACR register.	
		1	This bit is set by hardware when the timer times out.	
1	DBLBUF_ENA		DMA double-buffering	0
		0	DACR double-buffering is disabled.	
		1	When this bit and the CNT_ENA bit are both set, the double-buffering feature in the DACR register will be enabled. Writes to the DACR register are written to a pre-buffer and then transferred to the DACR on the next time-out of the counter.	

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Table 838. D/A Control register (CTRL - address 0x400E 1004) bit description

Bit	Symbol	Value	Description	Reset value
2	CNT_ENA		DMA time-out	0
		0	Time-out counter operation is disabled.	
		1	Time-out counter operation is enabled.	
3	DMA_ENA		DMA enable	0
		0	DMA access is disabled.	
		1	DMA Burst Request Input 15 is enabled for the DAC (see Table 195).	
31:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

39.5.3 D/A Converter Counter Value register

This read/write register contains the reload value for the Interrupt/DMA counter.

Table 839: D/A Converter counter value register (CNTVAL - address 0x400E 1008) bit description

Bit	Symbol	Description	Reset value
15:0	VALUE	16-bit reload value for the DAC interrupt/DMA timer.	0
31:16	-	Reserved.	-

39.6 Functional description

39.6.1 DMA counter

When the counter enable bit CNT_ENA in DACCTRL is set, a 16-bit counter will begin counting down, at the rate selected by CLK_APB3_DAC, from the value programmed into the DACCNTVAL register. The counter is decremented Each time the counter reaches zero, the counter will be reloaded by the value of DACCNTVAL and the DMA request bit INT_DMA_REQ will be set in hardware.

Note that the contents of the DACCTRL and DACCNTVAL registers are read and write accessible, but the timer itself is not accessible for either read or write.

If the DMA_ENA bit is set in the DACCTRL register, the DAC DMA request will be routed to the GPDMA. When the DMA_ENA bit is cleared, the default state after a reset, DAC DMA requests are blocked.

39.6.2 Double buffering

Double-buffering is enabled only if both, the CNT_ENA and the DBLBUF_ENA bits are set in DACCTRL. In this case, any write to the DACR register will only load the pre-buffer, which shares its register address with the DACR register. The DACR itself will be loaded from the pre-buffer whenever the counter reaches zero and the DMA request is set. At the same time the counter is reloaded with the COUNTVAL register value.

Reading the DACR register will only return the contents of the DACR register itself, not the contents of the pre-buffer register.

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If either the CNT_ENA or the DBLBUF_ENA bits are 0, any writes to the DACR address will go directly to the DACR register.

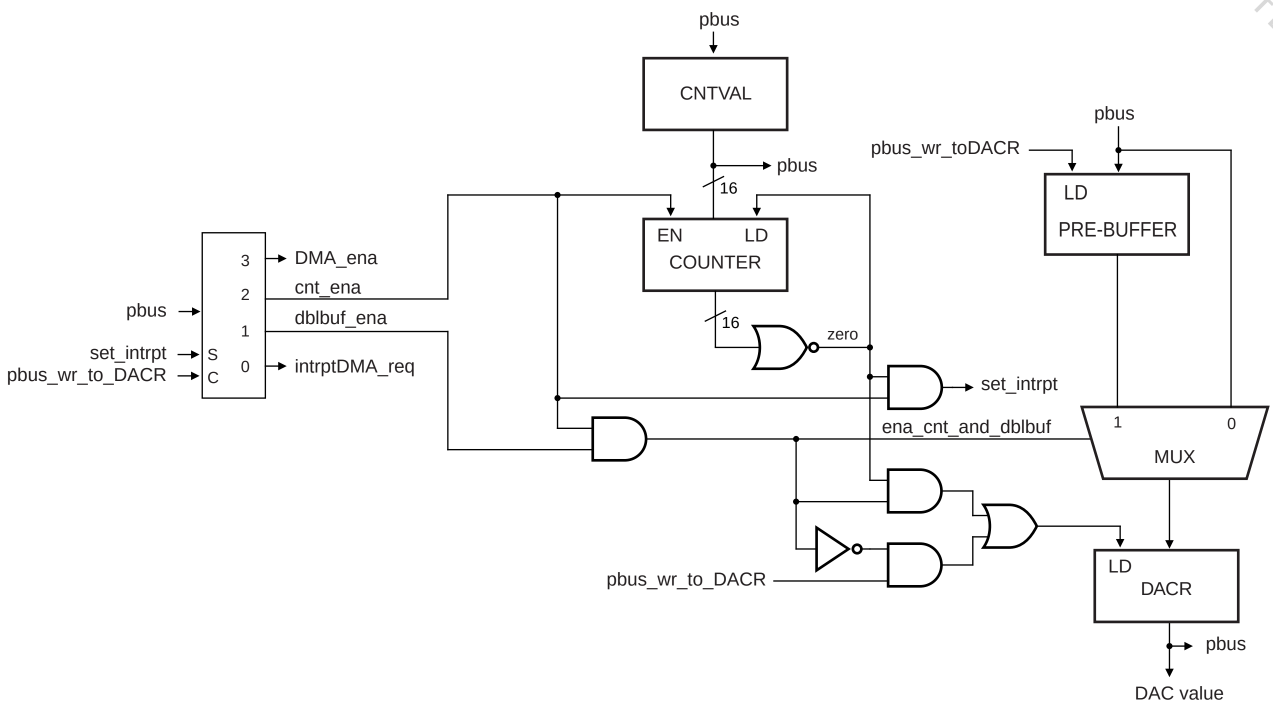


Fig 147. DAC control with DMA interrupt and timer

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UM10430

Chapter 40: LPC18xx flash programming interface

Rev. 00.13 — 20 July 2011 **User manual**

40.1 How to read this chapter

The flash programming interface is available for parts with on-chip flash. A reduced set of ISP commands is supported for flashless parts (see Table 843). See Chapter 3 for details of the boot process for flashless parts.

40.2 Introduction

The boot loader controls initial operation after reset and also provides the tools for programming the flash memory. This could be initial programming of a blank device, erasure and re-programming of a previously programmed device, or programming of the flash memory by the application program in a running system.

40.3 Features

- In-System Programming: In-System programming (ISP) is programming or reprogramming the on-chip flash memory, using the boot loader software and UART0 serial port. This can be done when the part resides in the end-user board.
- For parts without on-chip flash, ISP allows to load data to on-chip SRAM and to execute code from on-chip SRAM.
- In Application Programming: In-Application (IAP) programming is performing erase and write operation on the on-chip flash memory, as directed by the end-user application code.
- Flash signature generation: built-in hardware can generate a signature for a range of flash addresses or for the entire flash memory.

40.4 Description

The flash boot loader code is executed every time the part is powered on or reset. The loader can execute the ISP command handler or the user application code. A LOW level after reset at pin P2_7 is considered an external hardware request to start the ISP command handler. Assuming that power supply pins are on their nominal levels when the rising edge on $\overline{\text{RESET}}$ pin is generated, it may take up to 3 ms before P2_7 is sampled and the decision on whether to continue with user code or ISP handler is made. If P2_7 is sampled low and the watchdog overflow flag is set, the external hardware request to start the ISP command handler is ignored. If there is no request for the ISP command handler execution (P2_7 is sampled HIGH after reset), a search is made for a valid user program. If a valid user program is found then the execution control is transferred to it. If a valid user program is not found, the auto-baud routine is invoked.

Pin P2_7 is used as a hardware request signal for ISP and therefore requires special attention. Since P2_7 is in high impedance mode after reset, it is important that the user provides external hardware (a pull-up resistor or other device) to put the pin in a defined state. Otherwise unintended entry into ISP mode may occur.

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When ISP mode is entered after a power on reset, the IRC and PLL1 are used to generate the CCLK of 96 MHz. The UART0 pins are set to P2_0 and P2_1.

After determining the host's baud rate, the test string "Synchronized" is sent to a host. After a successful handshake, ISP enters the command interpret mode.

A hardware flash signature generation capability is built into the flash memory. This feature can be used to create a signature that can then be used to verify flash contents. Details of flash signature generation are shown in Section 40.11.

40.4.1 Memory map after any reset

When a user program begins execution after reset, the interrupt vectors are set to point to the beginning of flash memory (see Figure 7).

40.4.1.1 Criterion for Valid User Code

The reserved Cortex-M3 exception vector location 7 (offset 0x 001C in the vector table) should contain the 2's complement of the check-sum of table entries 0 through 6. This causes the checksum of the first 8 table entries to be 0. The boot loader code checksums the first 8 locations in sector 0 of the flash. If the result is 0, then execution control is transferred to the user code.

If the signature is not valid, the auto-baud routine synchronizes with the host via serial port 0. The host should send a "?" (0x3F) as a synchronization character and wait for a response. The host side serial port settings should be 8 data bits, 1 stop bit and no parity. The auto-baud routine measures the bit time of the received synchronization character in terms of its own frequency and programs the baud rate generator of the serial port. It also sends an ASCII string ("Synchronized<CR><LF>") to the host. In response to this the host should send the same string ("Synchronized<CR><LF>"). The auto-baud routine looks at the received characters to verify synchronization. If synchronization is verified then "OK<CR><LF>" string is sent to the host. The host should respond by sending the crystal frequency (in kHz) at which the part is running. For example, if the part is running at 10 MHz, the response from the host should be "10000<CR><LF>". "OK<CR><LF>" string is sent to the host after receiving the crystal frequency. If synchronization is not verified then the auto-baud routine waits again for a synchronization character. For auto-baud to work correctly in case of user invoked ISP, the CCLK frequency should be greater than or equal to 10 MHz.

Once the crystal frequency is received the part is initialized and the ISP command handler is invoked. For safety reasons an "Unlock" command is required before executing the commands resulting in flash erase/write operations and the "Go" command. The rest of the commands can be executed without the unlock command. The Unlock command is required to be executed once per ISP session. The Unlock command is explained in Section 40.8 "ISP commands" on page 917.

40.4.2 Communication protocol

All ISP commands should be sent as single ASCII strings. Strings should be terminated with Carriage Return (CR) and/or Line Feed (LF) control characters. Extra <CR> and <LF> characters are ignored. All ISP responses are sent as <CR><LF> terminated ASCII strings. Data is sent and received in UU-encoded format.

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40.4.2.1 ISP command format

"Command Parameter_0 Parameter_1 … Parameter_n<CR><LF>" "Data" (Data only for Write commands).

40.4.2.2 ISP response format

"Return_Code<CR><LF>Response_0<CR><LF>Response_1<CR><LF> … Response_n<CR><LF>" "Data" (Data only for Read commands).

40.4.2.3 ISP data format

The data stream is in UU-encoded format. The UU-encode algorithm converts 3 bytes of binary data in to 4 bytes of printable ASCII character set. It is more efficient than Hex format which converts 1 byte of binary data in to 2 bytes of ASCII hex. The sender should send the check-sum after transmitting 20 UU-encoded lines. The length of any UU-encoded line should not exceed 61 characters (bytes) i.e. it can hold 45 data bytes. The receiver should compare it with the check-sum of the received bytes. If the check-sum matches then the receiver should respond with "OK<CR><LF>" to continue further transmission. If the check-sum does not match the receiver should respond with "RESEND<CR><LF>". In response the sender should retransmit the bytes.

40.4.2.4 ISP flow control

A software XON/XOFF flow control scheme is used to prevent data loss due to buffer overrun. When the data arrives rapidly, the ASCII control character DC3 (0x13) is sent to stop the flow of data. Data flow is resumed by sending the ASCII control character DC1 (0x11). The host should also support the same flow control scheme.

40.4.2.5 ISP command abort

Commands can be aborted by sending the ASCII control character "ESC" (0x1B). This feature is not documented as a command under "ISP Commands" section. Once the escape code is received the ISP command handler waits for a new command.

40.4.2.6 Interrupts during IAP

The on-chip flash memory is not accessible during erase/write operations. When the user application code starts executing the interrupt vectors from the user flash area are active. The user should either disable interrupts, or ensure that user interrupt vectors are active in RAM and that the interrupt handlers reside in RAM, before making a flash erase/write IAP call. The IAP code does not use or disable interrupts.

40.4.2.7 RAM used by ISP command handler

ISP commands use on-chip RAM from 0x1000 0118 to 0x1000 01FF. The user could use this area, but the contents may be lost upon reset. Flash programming commands use the top 32 bytes of on-chip RAM. The stack is located at RAM top - 32. The maximum stack usage is 256 bytes and grows downwards.

40.4.2.8 RAM used by IAP command handler

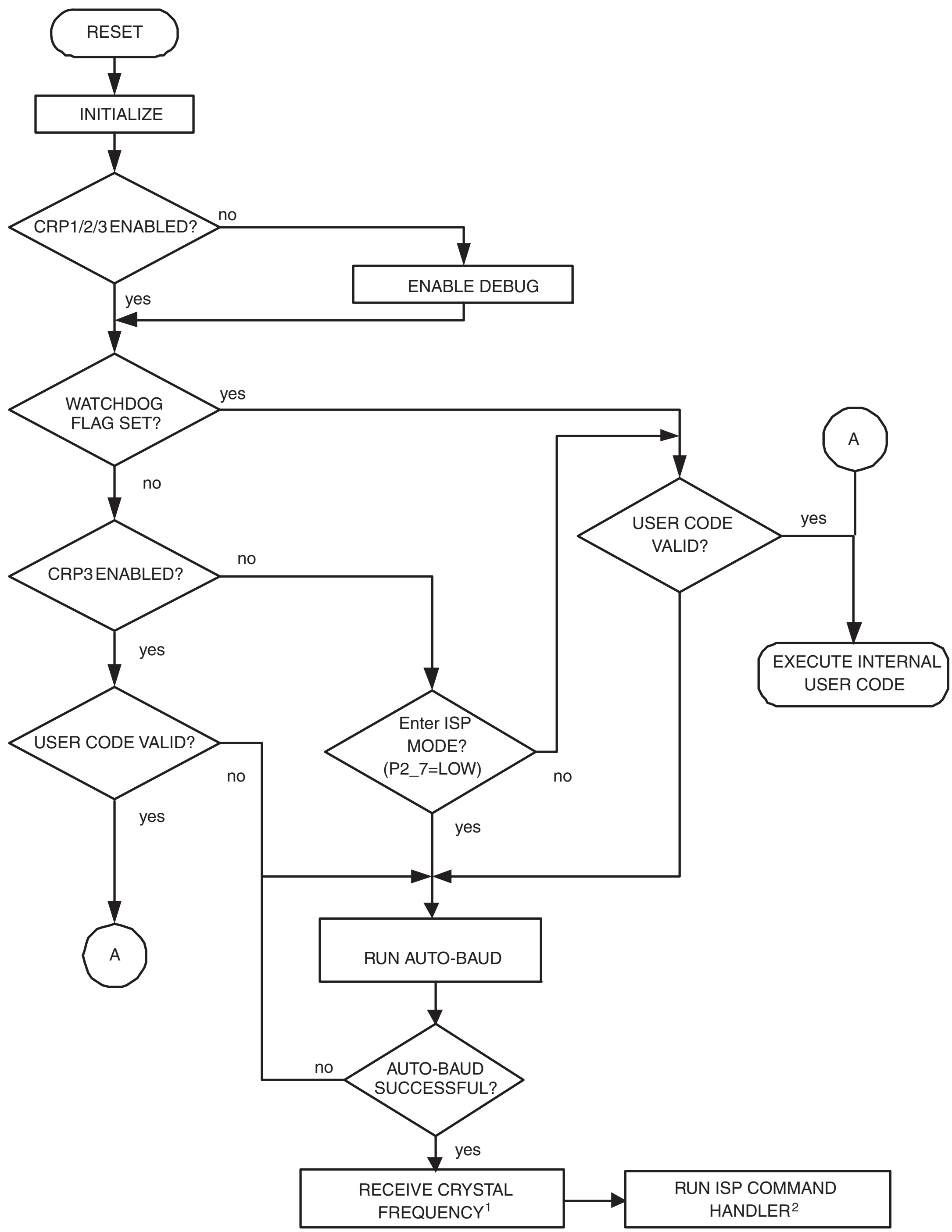
Flash programming commands use the top 32 bytes of on-chip RAM. The maximum stack usage in the user allocated stack space is 128 bytes and grows downwards.

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40.5 Boot process flowchart



(1) For details on handling the crystal frequency, see Section 40.9.9 “Re-invoke ISP” on page 930

(2) For details on available ISP commands based on the CRP settings see Section 40.7 “Code Read Protection (CRP)”

Fig 148. Boot process flowchart

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40.6 Sector numbers

Some IAP and ISP commands operate on "sectors" and specify sector numbers. The following table indicate the correspondence between sector numbers and memory addresses for LPC18xx device. IAP and ISP routines are located in the Boot ROM.

Table 840. Flash configuration

Flash bank	Sector number	Sector size [kB]	Start address	End address	LPC18x2	LPC18x3	LPC18x5	LPC18x7
A	0	8	0x1A00 0000	0x1A00 1FFF	x	x	x	x
A	1	8	0x1A00 2000	0x1A00 3FFF	x	x	x	x
A	2	8	0x1A00 4000	0x1A00 5FFF	x	x	x	x
A	3	8	0x1A00 6000	0x1A00 7FFF	x	x	x	x
A	4	8	0x1A00 8000	0x1A00 9FFF	x	x	x	x
A	5	8	0x1A00 A000	0x1A00 BFFF	x	x	x	x
A	6	8	0x1A00 C000	0x1A00 DFFF	x	x	x	x
A	7	8	0x1A00 E000	0x1A00 FFFF	x	x	x	x
A	8	64	0x1A01 0000	0x1A01 FFFF	x	x	x	x
A	9	64	0x1A02 0000	0x1A02 FFFF	x	x	x	x
A	10	64	0x1A03 0000	0x1A03 FFFF	x	x	x	x
A	11	64	0x1A04 0000	0x1A04 FFFF	x		x	x
A	12	64	0x1A05 0000	0x1A05 FFFF	x		x	x
A	13	64	0x1A06 0000	0x1A06 FFFF	x			x
A	14	64	0x1A07 0000	0x1A07 FFFF	x			x
B	0	8	0x1B00 0000	0x1B00 1FFF		x	x	x
B	1	8	0x1B00 2000	0x1B00 3FFF		x	x	x
B	2	8	0x1B00 4000	0x1B00 5FFF		x	x	x
B	3	8	0x1B00 6000	0x1B00 7FFF		x	x	x
B	4	8	0x1B00 8000	0x1B00 9FFF		x	x	x
B	5	8	0x1B00 A000	0x1B00 BFFF		x	x	x
B	6	8	0x1B00 C000	0x1B00 DFFF		x	x	x
B	7	8	0x1B00 E000	0x1B00 FFFF		x	x	x
B	8	64	0x1B01 0000	0x1B01 FFFF		x	x	x
B	9	64	0x1B02 0000	0x1B02 FFFF		x	x	x
B	10	64	0x1B03 0000	0x1B03 FFFF		x	x	x
B	11	64	0x1B04 0000	0x1B04 FFFF			x	x
B	12	64	0x1B05 0000	0x1B05 FFFF			x	x
B	13	64	0x1B06 0000	0x1B06 FFFF				x
B	14	64	0x1B07 0000	0x1B07 FFFF				x

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40.7 Code Read Protection (CRP)

Code Read Protection is a mechanism that allows user to enable different levels of security in the system so that access to the on-chip flash and use of the ISP can be restricted. When needed, CRP is invoked by programming a specific pattern in flash location at 0x000002FC. IAP commands are not affected by the code read protection.

Important: Any CRP change becomes effective only after the device has gone through a power cycle.

Table 841. Code Read Protection options

Name	Pattern programmed in 0x000002FC	Description
CRP1	0x12345678	Access to chip via the JTAG pins is disabled. This mode allows partial flash update using the following ISP commands and restrictions: • Because the ISP code uses SRAM, The Write to RAM command can not access SRAM below 0x1000 0200, see Section 40.4.2.7. • Read Memory command: disabled. • Copy RAM to Flash command: cannot write to Sector 0. • Go command: disabled. • Erase sector(s) command: can erase any individual sector except sector 0 only, or can erase all sectors at once. • Compare command: disabled This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased. The compare command is disabled, so in the case of partial flash updates the secondary loader should implement a checksum mechanism to verify the integrity of the flash.
CRP2	0x87654321	This is similar to CRP1 with the following additions: • Write to RAM command: disabled. • Copy RAM to Flash: disabled. • Erase command: only allows erase of all sectors.
CRP3	0x43218765	This is similar to CRP2, but ISP entry by pulling P2_7 LOW is disabled if a valid user code is present in flash sector 0. This mode effectively disables ISP override using the P2_7 pin. It is up to the user's application to provide for flash updates by using IAP calls or by invoking ISP with UART0. **Caution: If CRP3 is selected, no future factory testing can be performed on the device.**

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Table 842. Code Read Protection hardware/software interaction

CRP option	User Code Valid	P2_7 pin at reset	JTAG enabled	LPC18xx enters ISP mode	partial flash update in ISP mode
None	No	X	Yes	Yes	Yes
	Yes	High	Yes	No	NA
	Yes	Low	Yes	Yes	Yes
CRP1	No	x	No	Yes	Yes
	Yes	High	No	No	NA
	Yes	Low	No	Yes	Yes
CRP2	No	x	No	Yes	No
	Yes	High	No	No	NA
	Yes	Low	No	Yes	No
CRP3	No	x	No	Yes	No
	Yes	x	No	No	NA

If any CRP mode is enabled and access to the chip is allowed via the ISP, an unsupported or restricted ISP command will be terminated with return code CODE_READ_PROTECTION_ENABLED.

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40.8 ISP commands

The following commands are accepted by the ISP command handler. Detailed status codes are supported for each command. The command handler sends the return code INVALID_COMMAND when an undefined command is received. Commands and return codes are in ASCII format.

CMD_SUCCESS is sent by ISP command handler only when received ISP command has been completely executed and the new ISP command can be given by the host. Exceptions from this rule are "Set Baud Rate", "Write to RAM", "Read Memory", and "Go" commands.

Table 843. ISP command summary

ISP Command	Usage	Flashless parts	Parts with flash	Described in
Unlock	U <Unlock Code>	yes	yes	Table 844
Set Baud Rate	B <Baud Rate> <stop bit>	yes	yes	Table 845
Echo	A <setting>	yes	yes	Table 847
Write to RAM	W <start address> <number of bytes>	yes	yes	Table 848
Read Memory	R <address> <number of bytes>	yes	yes	Table 849
Prepare sector(s) for write operation	P <start sector number> <end sector number>	no	yes	Table 850
Copy RAM to Flash	C <flash address> <RAM address> <number of bytes>	no	yes	Table 851
Go	G <address> <Mode>	yes	yes	Table 852
Erase sector(s)	E <start sector number> <end sector number>	no	yes	Table 853
Blank check sector(s)	I <start sector number> <end sector number>	no	yes	Table 854
Read Part ID	J	yes	yes	Table 855
Read Boot Code version	K	yes	yes	Table 857
Read serial number	N	yes	yes	Table 858
Compare	M <address1> <address2> <number of bytes>	no	yes	Table 859

40.8.1 Unlock <Unlock code>

Table 844. ISP Unlock command

Command	U
Input	Unlock code: 23130_{10}
Return Code	CMD_SUCCESS | INVALID_CODE | PARAM_ERROR
Description	This command is used to unlock Flash Write, Erase, and Go commands.
Example	"U 23130<CR><LF>" unlocks the Flash Write/Erase & Go commands.

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40.8.2 Set Baud Rate <Baud Rate> <stop bit>

Table 845. ISP Set Baud Rate command

Command	B
Input	Baud Rate: 9600 | 19200 | 38400 | 57600 | 115200 | 230400 Stop bit: 1 | 2
Return Code	CMD_SUCCESS | INVALID_BAUD_RATE | INVALID_STOP_BIT | PARAM_ERROR
Description	This command is used to change the baud rate. The new baud rate is effective after the command handler sends the CMD_SUCCESS return code.
Example	"B 57600 1<CR><LF>" sets the serial port to baud rate 57600 bps and 1 stop bit.

Table 846. Correlation between possible ISP baudrates and CCLK frequency (in MHz)

ISP Baudrate .vs. CCLK Frequency	9600	19200	38400	57600	115200	230400
10.0000	+	+	+			
11.0592	+	+		+		
12.2880	+	+	+			
14.7456[1]	+	+	+	+	+	+
15.3600	+					
18.4320	+	+		+		
19.6608	+	+	+			
24.5760	+	+	+			
25.0000	+	+	+			

[1] ISP entry after reset uses the on chip IRC and PLL to run the device at CCLK = 14.748 MHz

40.8.3 Echo <setting>

Table 847. ISP Echo command

Command	A
Input	Setting: ON = 1 | OFF = 0
Return Code	CMD_SUCCESS | PARAM_ERROR
Description	The default setting for echo command is ON. When ON the ISP command handler sends the received serial data back to the host.
Example	"A 0<CR><LF>" turns echo off.

40.8.4 Write to RAM <start address> <number of bytes>

The host should send the data only after receiving the CMD_SUCCESS return code. The host should send the check-sum after transmitting 20 UU-encoded lines. The checksum is generated by adding raw data (before UU-encoding) bytes and is reset after transmitting 20 UU-encoded lines. The length of any UU-encoded line should not exceed 61 characters (bytes) i.e. it can hold 45 data bytes. When the data fits in less than 20 UU-encoded lines then the check-sum should be of the actual number of bytes sent.

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The ISP command handler compares it with the check-sum of the received bytes. If the check-sum matches, the ISP command handler responds with "OK<CR><LF>" to continue further transmission. If the check-sum does not match, the ISP command handler responds with "RESEND<CR><LF>". In response the host should retransmit the bytes.

Table 848. ISP Write to RAM command

Command	W
Input	**Start Address:** RAM address where data bytes are to be written. This address should be a word boundary. **Number of Bytes:** Number of bytes to be written. Count should be a multiple of 4
Return Code	CMD_SUCCESS | ADDR_ERROR (Address not on word boundary) | ADDR_NOT_MAPPED | COUNT_ERROR (Byte count is not multiple of 4) | PARAM_ERROR | CODE_READ_PROTECTION_ENABLED
Description	This command is used to download data to RAM. Data should be in UU-encoded format. This command is blocked when code read protection levels CRP2 or CRP3 are enabled.
Example	"W 268435968 4<CR><LF>" writes 4 bytes of data to address 0x1000 0200.

40.8.5 Read Memory <address> <no. of bytes>

The data stream is followed by the command success return code. The check-sum is sent after transmitting 20 UU-encoded lines. The checksum is generated by adding raw data (before UU-encoding) bytes and is reset after transmitting 20 UU-encoded lines. The length of any UU-encoded line should not exceed 61 characters (bytes) i.e. it can hold 45 data bytes. When the data fits in less than 20 UU-encoded lines then the check-sum is of actual number of bytes sent. The host should compare it with the checksum of the received bytes. If the check-sum matches then the host should respond with "OK<CR><LF>" to continue further transmission. If the check-sum does not match then the host should respond with "RESEND<CR><LF>". In response the ISP command handler sends the data again.

Table 849. ISP Read Memory command

Command	R
Input	**Start Address:** Address from where data bytes are to be read. This address should be a word boundary. **Number of Bytes:** Number of bytes to be read. Count should be a multiple of 4.
Return Code	CMD_SUCCESS followed by <actual data (UU-encoded)> | ADDR_ERROR (Address not on word boundary) | ADDR_NOT_MAPPED | COUNT_ERROR (Byte count is not a multiple of 4) | PARAM_ERROR | CODE_READ_PROTECTION_ENABLED
Description	This command is used to read data from RAM or flash memory. This command is blocked when any level of code read protection is enabled.
Example	"R 268435968 4<CR><LF>" reads 4 bytes of data from address 0x1000 0200.

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40.8.6 Prepare sector(s) for write operation <start sector number> <end sector number>

This command makes flash write/erase operation a two step process.

Table 850. ISP Prepare sector(s) for write operation command

Command	P
Input	**Start Sector Number** **End Sector Number:** Should be greater than or equal to start sector number.
Return Code	CMD_SUCCESS | BUSY | INVALID_SECTOR | PARAM_ERROR
Description	This command must be executed before executing "Copy RAM to Flash" or "Erase Sector(s)" command. Successful execution of the "Copy RAM to Flash" or "Erase Sector(s)" command causes relevant sectors to be protected again. To prepare a single sector use the same "Start" and "End" sector numbers.
Example	"P 0 0<CR><LF>" prepares the flash sector 0.

40.8.7 Copy RAM to Flash <flash address> <RAM address> <no of bytes>

Table 851. ISP Copy command

Command	C
Input	**Flash Address(DST):** Destination flash address where data bytes are to be written. The destination address should be a 256 byte boundary. **RAM Address(SRC):** Source RAM address from where data bytes are to be read. **Number of Bytes:** Number of bytes to be written. Should be 256 | 512 | 1024 | 4096.
Return Code	CMD_SUCCESS | SRC_ADDR_ERROR (Address not on word boundary) | DST_ADDR_ERROR (Address not on correct boundary) | SRC_ADDR_NOT_MAPPED | DST_ADDR_NOT_MAPPED | COUNT_ERROR (Byte count is not 256 | 512 | 1024 | 4096) | SECTOR_NOT_PREPARED_FOR WRITE_OPERATION | BUSY | CMD_LOCKED | PARAM_ERROR | CODE_READ_PROTECTION_ENABLED
Description	This command is used to program the flash memory. The "Prepare Sector(s) for Write Operation" command should precede this command. The affected sectors are automatically protected again once the copy command is successfully executed. This command is blocked when code read protection levels CRP2 or CRP3 are enabled. When code read protection level CRP1 is enabled, individual sectors other than sector 0 can be written.
Example	"C 0 268468224 512<CR><LF>" copies 512 bytes from the RAM address 0x1000 8000 to the flash address 0.

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40.8.8 Go <address> <mode>

Table 852. ISP Go command

Command	G
Input	**Address:** Flash or RAM address from which the code execution is to be started. This address should be on a word boundary. **Mode (retained for backward compatibility):** T (Execute program in Thumb Mode) | A (not allowed).
Return Code	CMD_SUCCESS | ADDR_ERROR | ADDR_NOT_MAPPED | CMD_LOCKED | PARAM_ERROR | CODE_READ_PROTECTION_ENABLED
Description	This command is used to execute a program residing in RAM or flash memory. It may not be possible to return to the ISP command handler once this command is successfully executed. This command is blocked when any level of code read protection is enabled.
Example	"G 0 T<CR><LF>" branches to address 0x0000 0000.

When the GO command is used, execution begins at the specified address (assuming it is an executable address) with the device left as it was configured for the ISP code. This means that some things are different than they would be for entering user code directly following a chip reset. Most importantly, the main PLL will be running and connected, configured to generate a CPU clock with a frequency of approximately 14.7456 MHz.

40.8.9 Erase sector(s) <start sector number> <end sector number>

Table 853. ISP Erase sector command

Command	E
Input	**Start Sector Number** **End Sector Number:** Should be greater than or equal to start sector number.
Return Code	CMD_SUCCESS | BUSY | INVALID_SECTOR | SECTOR_NOT_PREPARED_FOR_WRITE_OPERATION | CMD_LOCKED | PARAM_ERROR | CODE_READ_PROTECTION_ENABLED
Description	This command is used to erase one or more sector(s) of on-chip flash memory. This command is blocked when code read protection level CRP3 is enabled. When code read protection level CRP1 is enabled, individual sectors other than sector 0 can be erased. All sectors can be erased at once in CRP1 and CRP2.
Example	"E 2 3<CR><LF>" erases the flash sectors 2 and 3.

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40.8.10 Blank check sector(s) <sector number> <end sector number>

Table 854. ISP Blank check sector command

Command	I
Input	**Start Sector Number:** **End Sector Number:** Should be greater than or equal to start sector number.
Return Code	CMD_SUCCESS | SECTOR_NOT_BLANK (followed by <Offset of the first non blank word location> <Contents of non blank word location>) | INVALID_SECTOR | PARAM_ERROR |
Description	This command is used to blank check one or more sectors of on-chip flash memory.
Example	"I 2 3<CR><LF>" blank checks the flash sectors 2 and 3.

40.8.11 Read Part Identification number

Table 855. ISP Read Part Identification command

Command	J
Input	None.
Return Code	CMD_SUCCESS followed by part identification number in ASCII (see Table 856 “LPC18xx part identification numbers”).
Description	This command is used to read the part identification number. The part identification number maps to a feature subset within a device family. This number will not normally change as a result of technical revisions.

Table 856. LPC18xx part identification numbers

Device	ASCII/dec coding	Hex coding
<tbd>	<tbd>	<tbd>

40.8.12 Read Boot Code version number

Table 857. ISP Read Boot Code version number command

Command	K
Input	None
Return Code	CMD_SUCCESS followed by 2 bytes of boot code version number in ASCII format. It is to be interpreted as <byte1(Major)>.<byte0(Minor)>.
Description	This command is used to read the boot code version number.

40.8.13 Read device serial number

Table 858. ISP Read device serial number command

Command	N
Input	None.
Return Code	CMD_SUCCESS followed by the device serial number in 4 decimal ASCII groups, each representing a 32-bit value.
Description	This command is used to read the device serial number. The serial number may be used to uniquely identify a single unit among all LPC18xx devices.

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40.8.14 Compare <address1> <address2> <no of bytes>

Table 859. ISP Compare command

Command	M
Input	**Address1 (DST):** Starting flash or RAM address of data bytes to be compared. This address should be a word boundary. **Address2 (SRC):** Starting flash or RAM address of data bytes to be compared. This address should be a word boundary. **Number of Bytes:** Number of bytes to be compared; should be a multiple of 4.
Return Code	CMD_SUCCESS | (Source and destination data are equal) COMPARE_ERROR | (Followed by the offset of first mismatch) COUNT_ERROR (Byte count is not a multiple of 4) | ADDR_ERROR | ADDR_NOT_MAPPED | PARAM_ERROR |
Description	This command is used to compare the memory contents at two locations. This command is blocked when any level of code read protection is enabled.
Example	"M 8192 268435968 4<CR><LF>" compares 4 bytes from the RAM address 0x1000 0200 to the 4 bytes from the flash address 0x2000.

40.8.15 ISP Return Codes

Table 860. ISP Return Codes Summary

Return Code	Mnemonic	Description
0	CMD_SUCCESS	Command is executed successfully. Sent by ISP handler only when command given by the host has been completely and successfully executed.
1	INVALID_COMMAND	Invalid command.
2	SRC_ADDR_ERROR	Source address is not on word boundary.
3	DST_ADDR_ERROR	Destination address is not on a correct boundary.
4	SRC_ADDR_NOT_MAPPED	Source address is not mapped in the memory map. Count value is taken into consideration where applicable.
5	DST_ADDR_NOT_MAPPED	Destination address is not mapped in the memory map. Count value is taken into consideration where applicable.
6	COUNT_ERROR	Byte count is not multiple of 4 or is not a permitted value.
7	INVALID_SECTOR	Sector number is invalid or end sector number is greater than start sector number.
8	SECTOR_NOT_BLANK	Sector is not blank.
9	SECTOR_NOT_PREPARED_FOR_ WRITE_OPERATION	Command to prepare sector for write operation was not executed.
10	COMPARE_ERROR	Source and destination data not equal.
11	BUSY	Flash programming hardware interface is busy.
12	PARAM_ERROR	Insufficient number of parameters or invalid parameter.

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Table 860. ISP Return Codes Summary

Return Code	Mnemonic	Description
13	ADDR_ERROR	Address is not on word boundary.
14	ADDR_NOT_MAPPED	Address is not mapped in the memory map. Count value is taken in to consideration where applicable.
15	CMD_LOCKED	Command is locked.
16	INVALID_CODE	Unlock code is invalid.
17	INVALID_BAUD_RATE	Invalid baud rate setting.
18	INVALID_STOP_BIT	Invalid stop bit setting.
19	CODE_READ_PROTECTION_ ENABLED	Code read protection enabled.

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40.9 IAP commands

For in application programming the IAP routine should be called with a word pointer in register r0 pointing to memory (RAM) containing command code and parameters. Result of the IAP command is returned in the result table pointed to by register r1. The user can reuse the command table for result by passing the same pointer in registers r0 and r1. The parameter table should be big enough to hold all the results in case if number of results are more than number of parameters. Parameter passing is illustrated in the Figure 149. The number of parameters and results vary according to the IAP command. The maximum number of parameters is 5, passed to the "Copy RAM to Flash" command. The maximum number of results is 4, returned by the "Read device serial number" command. The command handler sends the status code INVALID_COMMAND when an undefined command is received. The IAP routine resides at location 0x1FFF 1FF0.

The IAP function could be called in the following way using C.

Define the IAP location entry point. Bit 0 of the IAP location is set since the Cortex-M3 uses only Thumb mode.

```
#define IAP_LOCATION 0x1FFF1FF1
```

Define data structure or pointers to pass IAP command table and result table to the IAP function:

```
unsigned long command[5];
unsigned long result[5];
```

or

```
unsigned long * command;
unsigned long * result;
command=(unsigned long *) 0x...
result= (unsigned long *) 0x...
```

Define pointer to function type, which takes two parameters and returns void. Note the IAP returns the result with the base address of the table residing in R1.

```
typedef void (*IAP)(unsigned int [],unsigned int[]);
IAP iap_entry;
```

Setting function pointer:

```
iap_entry=(IAP) IAP_LOCATION;
```

Whenever you wish to call IAP you could use the following statement.

```
iap_entry (command, result);
```

The IAP call could be simplified further by using the symbol definition file feature supported by ARM Linker in ADS (ARM Developer Suite). You could also call the IAP routine using assembly code.

As per the ARM specification (The ARM Thumb Procedure Call Standard SWS ESPC 0002 A-05) up to 4 parameters can be passed in the r0, r1, r2 and r3 registers respectively. Additional parameters are passed on the stack. Up to 4 parameters can be

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returned in the r0, r1, r2 and r3 registers respectively. Additional parameters are returned indirectly via memory. Some of the IAP calls require more than 4 parameters. If the ARM suggested scheme is used for the parameter passing/returning then it might create problems due to difference in the C compiler implementation from different vendors. The suggested parameter passing scheme reduces such risk.

The flash memory is not accessible during a write or erase operation. IAP commands, which results in a flash write/erase operation, use 32 bytes of space in the top portion of the on-chip RAM for execution. The user program should not be use this space if IAP flash programming is permitted in the application.

Table 861. IAP Command Summary

IAP Command	Command Code	Described in
Prepare sector(s) for write operation	50_{10}	Table 862
Copy RAM to Flash	51_{10}	Table 863
Erase sector(s)	52_{10}	Table 864
Blank check sector(s)	53_{10}	Table 865
Read part ID	54_{10}	Table 866
Read Boot Code version	55_{10}	Table 867
Read device serial number	58_{10}	Table 868
Compare	56_{10}	Table 869
Reinvoke ISP	57_{10}	Table 870

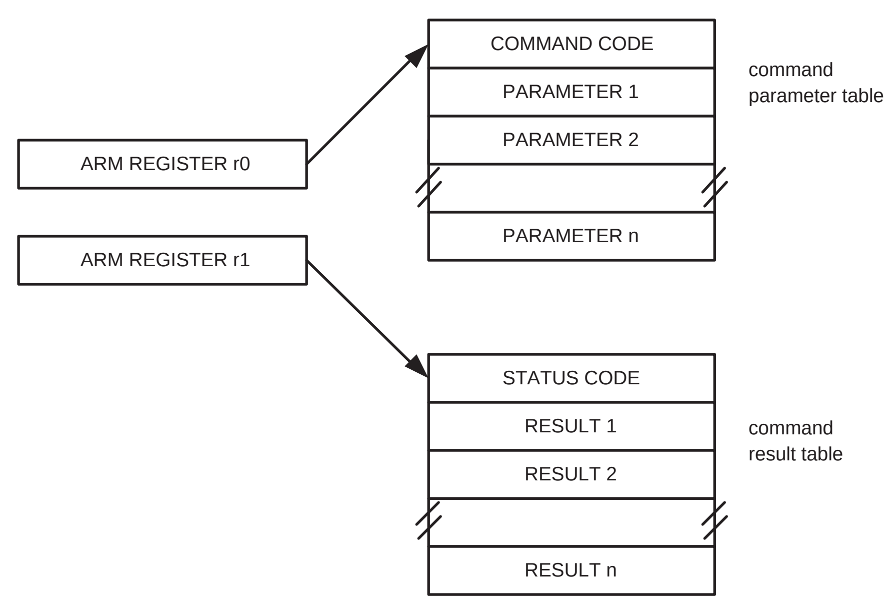


Fig 149. IAP parameter passing

40.9.1 Prepare sector(s) for write operation

This command makes flash write/erase operation a two step process.

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Table 862. IAP Prepare sector(s) for write operation command

Command	Prepare sector(s) for write operation
Input	**Command code: 50 (decimal)** **Param0:** Start Sector Number **Param1:** End Sector Number (should be greater than or equal to start sector number).
Return Code	CMD_SUCCESS | BUSY | INVALID_SECTOR
Result	None
Description	This command must be executed before executing "Copy RAM to Flash" or "Erase Sector(s)" command. Successful execution of the "Copy RAM to Flash" or "Erase Sector(s)" command causes relevant sectors to be protected again. To prepare a single sector use the same "Start" and "End" sector numbers.

40.9.2 Copy RAM to Flash

Table 863. IAP Copy RAM to Flash command

Command	Copy RAM to Flash
Input	**Command code: 51 (decimal)** **Param0(DST):** Destination flash address where data bytes are to be written. This address should be a 256 byte boundary. **Param1(SRC):** Source RAM address from which data bytes are to be read. This address should be a word boundary. **Param2:** Number of bytes to be written. Should be 256 | 512 | 1024 | 4096. **Param3:** CPU Clock Frequency (CCLK) in kHz.
Return Code	CMD_SUCCESS | SRC_ADDR_ERROR (Address not a word boundary) | DST_ADDR_ERROR (Address not on correct boundary) | SRC_ADDR_NOT_MAPPED | DST_ADDR_NOT_MAPPED | COUNT_ERROR (Byte count is not 256 | 512 | 1024 | 4096) | SECTOR_NOT_PREPARED_FOR_WRITE_OPERATION | BUSY |
Result	None
Description	This command is used to program the flash memory. The affected sectors should be prepared first by calling "Prepare Sector for Write Operation" command. The affected sectors are automatically protected again once the copy command is successfully executed.

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40.9.3 Erase Sector(s)

Table 864. IAP Erase Sector(s) command

Command	Erase Sector(s)
Input	**Command code: 52 (decimal)** **Param0:** Start Sector Number **Param1:** End Sector Number (should be greater than or equal to start sector number). **Param2:** CPU Clock Frequency (CCLK) in kHz.
Return Code	CMD_SUCCESS | BUSY | SECTOR_NOT_PREPARED_FOR_WRITE_OPERATION | INVALID_SECTOR
Result	None
Description	This command is used to erase a sector or multiple sectors of on-chip flash memory. To erase a single sector use the same "Start" and "End" sector numbers.

40.9.4 Blank check sector(s)

Table 865. IAP Blank check sector(s) command

Command	Blank check sector(s)
Input	**Command code: 53 (decimal)** **Param0:** Start Sector Number **Param1:** End Sector Number (should be greater than or equal to start sector number).
Return Code	CMD_SUCCESS | BUSY | SECTOR_NOT_BLANK | INVALID_SECTOR
Result	**Result0:** Offset of the first non blank word location if the Status Code is SECTOR_NOT_BLANK. **Result1:** Contents of non blank word location.
Description	This command is used to blank check a sector or multiple sectors of on-chip flash memory. To blank check a single sector use the same "Start" and "End" sector numbers.

40.9.5 Read part identification number

Table 866. IAP Read part identification number command

Command	Read part identification number
Input	**Command code: 54 (decimal)** **Parameters:** None
Return Code	CMD_SUCCESS |
Result	**Result0:** Part Identification Number.
Description	This command is used to read the part identification number. The value returned is the hexadecimal version of the part ID. See Table 856 “LPC18xx part identification numbers”.

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40.9.6 Read Boot Code version number

Table 867. IAP Read Boot Code version number command

Command	Read boot code version number
Input	**Command code: 55 (decimal)** **Parameters:** None
Return Code	CMD_SUCCESS |
Result	**Result0:** 2 bytes of boot code version number in ASCII format. It is to be interpreted as <byte1(Major)>.<byte0(Minor)>
Description	This command is used to read the boot code version number.

40.9.7 Read device serial number

Table 868. IAP Read device serial number command

Command	Read device serial number
Input	**Command code: 58 (decimal)** **Parameters:** None
Return Code	CMD_SUCCESS |
Result	**Result0:** First 32-bit word of Device Identification Number (at the lowest address) **Result1:** Second 32-bit word of Device Identification Number **Result2:** Third 32-bit word of Device Identification Number **Result3:** Fourth 32-bit word of Device Identification Number
Description	This command is used to read the device identification number. The serial number may be used to uniquely identify a single unit among all LPC18xx devices.

40.9.8 Compare <address1> <address2> <no of bytes>

Table 869. IAP Compare command

Command	Compare
Input	**Command code: 56 (decimal)** **Param0(DST):** Starting flash or RAM address of data bytes to be compared. This address should be a word boundary. **Param1(SRC):** Starting flash or RAM address of data bytes to be compared. This address should be a word boundary. **Param2:** Number of bytes to be compared; should be a multiple of 4.
Return Code	CMD_SUCCESS | COMPARE_ERROR | COUNT_ERROR (Byte count is not a multiple of 4) | ADDR_ERROR | ADDR_NOT_MAPPED
Result	**Result0:** Offset of the first mismatch if the Status Code is COMPARE_ERROR.
Description	This command is used to compare the memory contents at two locations. **The result may not be correct when the source or destination includes any of the first 64 bytes starting from address zero. The first 64 bytes can be re-mapped to RAM.**

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40.9.9 Re-invoke ISP

Table 870. Re-invoke ISP

Command	Compare
Input	**Command code: 57 (decimal)**
Return Code	None
Result	**None.**
Description	This command is used to invoke the boot loader in ISP mode. It maps boot vectors, sets the clock to 96 MHz, configures UART0 pins U0_RX and U0_TX, resets TIMER1 and resets the U0FDR (see Table 678). This command may be used when a valid user program is present in the internal flash memory and the P2_7 pin is not accessible to force the ISP mode. The command does not disable the PLL1 hence it is possible to invoke the boot loader when the part is running off the PLL1. In this case, the ISP utility must pass the PLL1 output frequency after the autobaud handshake. Another option is to disable the PLL1 and select the IRC as the clock source before making this IAP call. In this case,the frequency sent by ISP is ignored and IRC and PLL1 are used to generate a 14.748 MHz clock.

40.9.10 IAP Status Codes

Table 871. IAP Status Codes Summary

Status Code	Mnemonic	Description
0	CMD_SUCCESS	Command is executed successfully.
1	INVALID_COMMAND	Invalid command.
2	SRC_ADDR_ERROR	Source address is not on a word boundary.
3	DST_ADDR_ERROR	Destination address is not on a correct boundary.
4	SRC_ADDR_NOT_MAPPED	Source address is not mapped in the memory map. Count value is taken in to consideration where applicable.
5	DST_ADDR_NOT_MAPPED	Destination address is not mapped in the memory map. Count value is taken in to consideration where applicable.
6	COUNT_ERROR	Byte count is not multiple of 4 or is not a permitted value.
7	INVALID_SECTOR	Sector number is invalid.
8	SECTOR_NOT_BLANK	Sector is not blank.
9	SECTOR_NOT_PREPARED_ FOR_WRITE_OPERATION	Command to prepare sector for write operation was not executed.
10	COMPARE_ERROR	Source and destination data is not same.
11	BUSY	Flash programming hardware interface is busy.

40.10 JTAG flash programming interface

Debug tools can write parts of the flash image to the RAM and then execute the IAP call "Copy RAM to Flash" repeatedly with proper offset.

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40.11 Flash signature generation

The flash module contains a built-in signature generator. This generator can produce a 128-bit signature from a range of flash memory. A typical usage is to verify the flashed contents against a calculated signature (e.g. during programming).

The address range for generating a signature must be aligned on flash-word boundaries, i.e. 128-bit boundaries. Once started, signature generation completes independently. While signature generation is in progress, the flash memory cannot be accessed for other purposes, and an attempted read will cause a wait state to be asserted until signature generation is complete. Code outside of the flash (e.g. internal RAM) can be executed during signature generation. This can include interrupt services, if the interrupt vector table is re-mapped to memory other than the flash memory. The code that initiates signature generation should also be placed outside of the flash memory.

40.11.1 Register description for signature generation

Table 872. Register overview: FMC (base address 0x4008 4000)

Name	Description	Access	Reset Value	Address	Reference
FMSSTART	Signature start address register	R/W	0	0x4008 4020	Table 873
FMSSTOP	Signature stop-address register	R/W	0	0x4008 4024	Table 874
FMSW0	128-bit signature Word 0	R	-	0x4008 402C	Table 875
FMSW1	128-bit signature Word 1	R	-	0x4008 4030	Table 876
FMSW2	128-bit signature Word 2	R	-	0x4008 4034	Table 877
FMSW3	128-bit signature Word 3	R	-	0x4008 4038	Table 878
FMSTAT	Signature generation status register	R	0	0x4008 4FE0	Section 40.11.1.3
FMSTATCLR	Signature generation status clear register	W	-	0x4008 4FE8	Section 40.11.1.4

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40.11.1.1 Signature generation address and control registers

These registers control automatic signature generation. A signature can be generated for any part of the flash memory contents. The address range to be used for generation is defined by writing the start address to the signature start address register (FMSSTART) and the stop address to the signature stop address register (FMSSTOP. The start and stop addresses must be aligned to 128-bit boundaries and can be derived by dividing the byte address by 16.

Signature generation is started by setting the SIG_START bit in the FMSSTOP register. Setting the SIG_START bit is typically combined with the signature stop address in a single write.

Table 873 and Table 874 show the bit assignments in the FMSSTART and FMSSTOP registers respectively.

Table 873. Flash Module Signature Start register (FMSSTART - 0x4008 4020) bit description

Bit	Symbol	Description	Reset Value
31:17	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
16:0	START	Signature generation start address (corresponds to AHB byte address bits[20:4]).	0

Table 874. Flash Module Signature Stop register (FMSSTOP - 0x4008 4024) bit description

Bit	Symbol	Value	Description	Reset Value
31:18	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
17	SIG_START		Start control bit for signature generation.	0
		0	Signature generation is stopped	
		1	Initiate signature generation	
16:0	STOP		BIST stop address divided by 16 (corresponds to AHB byte address [20:4]).	0

40.11.1.2 Signature generation result registers

The signature generation result registers return the flash signature produced by the embedded signature generator. The 128-bit signature is reflected by the four registers FMSW0, FMSW1, FMSW2 and FMSW3.

The generated flash signature can be used to verify the flash memory contents. The generated signature can be compared with an expected signature and thus makes saves time and code space. The method for generating the signature is described in Section 40.11.2.

Table 878 show bit assignment of the FMSW0 and FMSW1, FMSW2, FMSW3 registers respectively.

Table 875. FMSW0 register bit description (FMSW0, address: 0x4008 402C)

Bit	Symbol	Description	Reset Value
31:0	SW0[31:0]	Word 0 of 128-bit signature (bits 31 to 0).	-

Table 876. FMSW1 register bit description (FMSW1, address: 0x4008 4030)

Bit	Symbol	Description	Reset Value
31:0	SW1[63:32]	Word 1 of 128-bit signature (bits 63 to 32).	-

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Table 877. FMSW2 register bit description (FMSW2, address: 0x4008 4034)

Bit	Symbol	Description	Reset Value
31:0	SW2[95:64]	Word 2 of 128-bit signature (bits 95 to 64).	-

Table 878. FMSW3 register bit description (FMSW3, address: 0x4008 4038)

Bit	Symbol	Description	Reset Value
31:0	SW3[127:96]	Word 3 of 128-bit signature (bits 127 to 96).	-

40.11.1.3 Flash Module Status register (FMSTAT - 0x0x4008 4FE0)

The read-only FMSTAT register provides a means of determining when signature generation has completed. Completion of signature generation can be checked by polling the SIG_DONE bit in FMSTAT. SIG_DONE should be cleared via the FMSTATCLR register before starting a signature generation operation, otherwise the status might indicate completion of a previous operation.

Table 879. Flash module Status register (FMSTAT - 0x4008 4FE0) bit description

Bit	Symbol	Description	Reset Value
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
2	SIG_DONE	When 1, a previously started signature generation has completed. See FMSTATCLR register description for clearing this flag.	0
1:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

40.11.1.4 Flash Module Status Clear register (FMSTATCLR - 0x0x4008 4FE8)

The FMSTATCLR register is used to clear the signature generation completion flag.

Table 880. Flash Module Status Clear register (FMSTATCLR - 0x0x4008 4FE8) bit description

Bit	Symbol	Description	Reset Value
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
2	SIG_DONE_CLR	Writing a 1 to this bits clears the signature generation completion flag (SIG_DONE) in the FMSTAT register.	0
1:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

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40.11.2 Algorithm and procedure for signature generation

Signature generation

A signature can be generated for any part of the flash contents. The address range to be used for signature generation is defined by writing the start address to the FMSSTART register, and the stop address to the FMSSTOP register.

The signature generation is started by writing a ‘1’ to FMSSTOP.MISR_START. Starting the signature generation is typically combined with defining the stop address, which is done in another field FMSSTOP.FMSSTOP of the same register.

The time that the signature generation takes is proportional to the address range for which the signature is generated. Reading of the flash memory for signature generation uses a self-timed read mechanism and does not depend on any configurable timing settings for the flash. A safe estimation for the duration of the signature generation is:

Duration = int((60 / tcy) + 3) x (FMSSTOP - FMSSTART + 1)

When signature generation is triggered via software, the duration is in AHB clock cycles, and tcy is the time in ns for one AHB clock. The SIG_DONE bit in FMSTAT can be polled by software to determine when signature generation is complete.

If signature generation is triggered via JTAG, the duration is in JTAG tck cycles, and tcy is the time in ns for one JTAG clock. Polling the SIG_DONE bit in FMSTAT is not possible in this case.

After signature generation, a 128-bit signature can be read from the FMSW0 to FMSW3 registers. The 128-bit signature reflects the corrected data read from the flash. The 128-bit signature reflects flash parity bits and check bit values.

Content verification

The signature as it is read from the FMSW0 to FMSW3 registers must be equal to the reference signature. The algorithms to derive the reference signature is given in Figure 150.

```
sign = 0
FOR address = FMSTART.FMSTART TO FMSTOP.FMSTOP
{
        FOR i = 0 TO 126
                nextSign[i] = f_Q[address][i] XOR sign[i+1]
                nextSign[127] = f_Q[address][127] XOR sign[0] XOR sign[2] XOR
                        sign[27] XOR sign[29]
        sign = nextSign
}
signature128 = sign
```

Fig 150. Algorithm for generating a 128 bit signature

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UM10430

Chapter 41: LPC18xx JTAG, Serial Wire Debug (SWD), and trace functions

Rev. 00.13 — 20 July 2011 **User manual**

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41.1 How to read this chapter

The power management controller is identical on all LPC18xx parts.

41.2 Features

- Supports both standard JTAG and ARM Serial Wire Debug modes.
- Direct debug access to all memories, registers, and peripherals.
- No target resources are required for the debugging session.
- Trace port provides CPU instruction trace capability. Output can be via a 4-bit trace data port, or Serial Wire Viewer.
- Eight Breakpoints. Six instruction breakpoints that can also be used to remap instruction addresses for code patches. Two data comparators that can be used to remap addresses for patches to literal values.
- Four data Watchpoints that can also be used as trace triggers.
- Instrumentation Trace Macrocell allows additional software controlled trace.

41.3 Introduction

Debug and trace functions are integrated into the ARM Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M3 is configured to support up to eight breakpoints and four watchpoints.

41.4 Description

Debugging with the LPC18xx defaults to JTAG. Once in the JTAG debug mode, the debug tool can switch to Serial Wire Debug mode.

Trace can be done using either a 4-bit parallel interface or the Serial Wire Output.

41.5 Pin Description

The tables below indicate the various pin functions related to debug and trace. Some of these functions share pins with other functions which therefore may not be used at the same time. Use of the JTAG port excludes use of Serial Wire Debug and Serial Wire Output. Use of the parallel trace requires 5 pins that may be part of the user application, limiting debug possibilities for those features. Trace using the Serial Wire Output does not have this limitation, but has a limited bandwidth.

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Table 881. JTAG pin description

Pin Name	Type	Description
TCK	Input	**JTAG Test Clock.** This pin is the clock for debug logic when in the JTAG debug mode.
TMS	Input	**JTAG Test Mode Select.** The TMS pin selects the next state in the TAP state machine.
TDI	Input	**JTAG Test Data In.** This is the serial data input for the shift register.
TDO	Output	**JTAG Test Data Output.** This is the serial data output from the shift register. Data is shifted out of the device on the negative edge of the TCK signal.
$\overline{\text{TRST}}$	Input	**JTAG Test Reset.** The $\overline{\text{TRST}}$ pin can be used to reset the test logic within the debug logic.

Table 882. Serial Wire Debug pin description

Pin Name	Type	Description
SWDCLK	Input	**Serial Wire Clock.** This pin is the clock for debug logic when in the Serial Wire Debug mode.
SWDIO	Input / Output	**Serial wire debug data input/output.** The SWDIO pin is used by an external debug tool to communicate with and control the Cortex-M3 CPU.
SWO	Output	**Serial Wire Output.** The SWO pin optionally provides data from the ITM and/or the ETM for an external debug tool to evaluate.

Table 883. Parallel Trace pin description

Pin Name	Type	Description
TRACECLK	Input	**Trace Clock.** This pin provides the sample clock for trace data on the TRACEDATA pins when tracing is enabled by an external debug tool.
TRACEDATA[3:0]	Output	**Trace Data bits 3 to 0.** These pins provide ETM trace data when tracing is enabled by an external debug tool. The debug tool can then interpret the compressed information and make it available to the user.

41.6 Debug Notes

Important: The user should be aware of certain limitations during debugging. The most important is that, due to limitations of the Cortex-M3 integration, the LPC18xx cannot wake up in the usual manner from Deep Sleep and Power-down modes. It is recommended not to use these modes during debug.

Another issue is that debug mode changes the way in which reduced power modes are handled by the Cortex-M3 CPU. This causes power modes at the device level to be different from normal modes operation. These differences mean that power measurements should not be made while debugging, the results will be higher than during normal operation in an application.

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During a debugging session, the System Tick Timer and the Repetitive Interrupt Timers are automatically stopped whenever the CPU is stopped. Other peripherals are not affected. If the Repetitive Interrupt Timer is configured such that its PCLK rate is lower than the CPU clock rate, the RIT may not increment predictably during some debug operations, such as single stepping.

Debugging is disabled if code read protection is enabled.

41.7 Debug memory re-mapping

Following chip reset, a portion of the Boot ROM is mapped to address 0 so that it will be automatically executed. The Boot ROM switches the map to point to <tbd>. In this way a user normally does not need to know that this re-mapping occurs.

However, when a debugger halts CPU execution immediately following reset, the Boot ROM is still mapped to address 0 and can cause confusion. Ideally, the debugger should correct the mapping automatically in this case, so that a user does not need to deal with it.

41.8 JTAG TAP Identification

The JTAG TAP controller contains device ID that can be used by debugging software to identify the general type of device. <tbd>

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42.1 LPC1850/30/20/10 Rev '-' NVIC

42.1.1 How to read this chapter

Remark: This chapter describes the NVIC connections of parts LPC1850/30/20/10 Rev "-".

The available NVIC interrupt sources vary for different parts.

- Ethernet interrupt: available on LPC1850/30.
- USB0 interrupt: available on LPC1850/30/20.
- USB1 interrupt: available on LPC1850/30.
- SDIO interrupt: not available.

42.1.2 Basic configuration

The NVIC is part of the ARM Cortex-M3 core.

42.1.3 Features

- Nested Vectored Interrupt Controller that is an integral part of the ARM Cortex-M3
- Tightly coupled interrupt controller provides low interrupt latency
- Controls system exceptions and peripheral interrupts
- On the LPC18xx, the NVIC supports 32 vectored interrupts
- 32 programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table
- Non-Maskable Interrupt
- Software interrupt generation

42.1.4 General description

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

Refer to the Cortex-M3 User Guide for details of NVIC operation.

42.1.5 Pin description

Table 884. NVIC pin description

Function	Direction	Description
NMI	I	External Non-Maskable Interrupt (NMI) input

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42.1.6 Interrupt sources

Table 885 lists the interrupt sources for each peripheral function. Each peripheral device may have one or more interrupt lines to the Vectored Interrupt Controller. Each line may represent more than one interrupt source, as noted.

Exception numbers relate to where entries are stored in the exception vector table. Interrupt numbers are used in some other contexts, such as software interrupts.

In addition, the NVIC handles the Non-Maskable Interrupt (NMI). In order for NMI to operate from an external signal, the NMI function must be connected to the related device pin (P4_0 or PE_4). When connected, a logic 1 on the pin will cause the NMI to be processed. For details, refer to the Cortex-M3 User Guide.

Table 885. Connection of interrupt sources to the NVIC

Interrupt ID	Exception Number	Vector Offset	Function	Flag(s)
0	16	0x40	DAC	
1	17	0x44	Event router	Combined interrupt from the event router sources
2	18	0x48	DMA	
3	19	0x4C	-	Reserved
4	20	0x50	-	Reserved
5	21	0x54	Ethernet	sbd_intr_o Ethernet interrupt
6	22	0x58	SDIO	
7	23	0x5C	LCD	
8	24	0x60	USB0	OTG interrupt
9	25	0x64	USB1	
10	26	0x68	SCT	SCT combined interrupt
11	27	0x6C	RI timer	
12	28	0x70	Timer0	
13	29	0x74	Timer1	
14	30	0x78	Timer2	
15	31	0x7C	Timer3	
16	32	0x80	Motor control PWM	
17	33	0x84	ADC0	
18	34	0x88	I2C0	
19	35	0x8C	I2C1	
20	36	0x90	-	Reserved.
21	37	0x94	ADC1	
22	38	0x98	SSP0	
23	39	0x9C	SSP1	
24	40	0xA0	UART0	
25	41	0xA4	UART1	also modem interrupt
26	42	0xA8	UART2	
27	43	0xAC	UART3	also irda interrupt
28	44	0xB0	I2S	

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Table 885. Connection of interrupt sources to the NVIC

Interrupt ID	Exception Number	Vector Offset	Function	Flag(s)
29	45	0xB4	AES	
30	46	0xB8	SPIFI	
31	47	0xBC	-	Reserved
32 - 40	48 - 56	0xC0 - 0Xe0	-	Reserved

42.1.7 Vector table remapping

The Cortex-M3 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register (VTOR) contained in the Cortex-M3.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M3 address space. The vector table should be located on a 256 word (1024 byte) boundary. Refer to the Cortex-M3 User Guide for details of the Vector Table Offset feature.

ARM describes bit 29 of the VTOR (TBLOFF) as selecting a memory region, either code or SRAM. For simplicity, this bit can be thought as simply part of the address offset since the split between the “code” space and the “SRAM” space occurs at the location corresponding to bit 29 in a memory address.

Examples:

To place the vector table at the beginning of the “local” static RAM, starting at address 0x1000 0000, place the value 0x1000 0000 in the VTOR register. This indicates address 0x1000 0000 in the code space, since bit 29 of the VTOR equals 0.

To place the vector table at the beginning of the AHB static RAM, starting at address 0x2007 C000, place the value 0x2007 C000 in the VTOR register. This indicates address 0x2007 C000 in the SRAM space, since bit 29 of the VTOR equals 1.

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42.1.8 Register description

The following table summarizes the registers in the NVIC as implemented in the LPC18xx. The Cortex-M3 User Guide provides a functional description of the NVIC.

Table 886. Register overview: NVIC (base address 0xE000 E000)

Name	Access	Address offset	Description	Reset value
ISER0	RW	0x100	Interrupt Set-Enable Register 0. This register allows enabling interrupts and reading back the interrupt enables for specific peripheral functions.	0
-	RW	0x104	Reserved.	0
ICER0	RW	0x180	Interrupt Clear-Enable Register 0. This register allows disabling interrupts and reading back the interrupt enables for specific peripheral functions.	0
-	RW	0x184	Reserved.	0
ISPR0	RW	0x200	Interrupt Set-Pending Register 0. This register allows changing the interrupt state to pending and reading back the interrupt pending state for specific peripheral functions.	0
-	RW	0x204	Reserved.	0
ICPR0	RW	0x280	Interrupt Clear-Pending Register 0. This register allows changing the interrupt state to not pending and reading back the interrupt pending state for specific peripheral functions.	0
-	RW	0x284	Reserved.	0
IABR0	RO	0x300	Interrupt Active Bit Register 0. This register allows reading the current interrupt active state for specific peripheral functions.	0
-	RO	0x304	Reserved.	0
IPR0	RW	0x400	Interrupt Priority Registers 0. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR1	RW	0x404	Interrupt Priority Registers 1 This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR2	RW	0x408	Interrupt Priority Registers 2. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR3	RW	0x40C	Interrupt Priority Registers 3. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR4	RW	0x410	Interrupt Priority Registers 4. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR5	RW	0x414	Interrupt Priority Registers 5. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR6	RW	0x418	Interrupt Priority Registers 6. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
IPR7	RW	0x41C	Interrupt Priority Registers 7. This register allows assigning a priority to each interrupt. Each register contains the 5-bit priority fields for 4 interrupts.	0
STIR	WO	0xF00	Software Trigger Interrupt Register. This register allows software to generate an interrupt.	0

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42.1.8.1 Interrupt Set-Enable Register 0 register

The ISER0 register allows enabling the first 32 peripheral interrupts or reading the enabled state of those interrupts. Disabling interrupts is done through the ICER0 register (Section 42.1.8.2).

Table 887. Interrupt Set-Enable Register 0 register (ISER0 - address 0xE000 E100) bit description

Bit	Symbol	Description	Reset value
0	ISE_DAC	DAC interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
1	ISE_ER	Event router interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
2	ISE_DMA	xxx interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
3	-	Reserved.	0
4	-	Reserved.	0
5	ISE_ETHERNET	Ethernet interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
6	ISE_SDIO	SDIO interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
7	ISE_LCD	LCD interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
8	ISE_USB0	USB0 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
9	ISE_USB1	USB1 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
10	ISE_SCT	SCT interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
11	ISE_RIT	RIT interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
12	ISE_TIMER0	Timer0 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0

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Table 887. Interrupt Set-Enable Register 0 register (ISER0 - address 0xE000 E100) bit description *…continued*

Bit	Symbol	Description	Reset value
13	ISE_TIMER1	Timer1 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
14	ISE_TIMER2	Timer2 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
15	ISE_TIMER3	Timer3 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
16	ISE_MOTOCON PWM	MOTOCONPWM interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
17	ISE_ADC0	ADC0 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
18	ISE_I2C0	I2C0 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
19	ISE_I2C1	I2C1 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
20	-	Reserved.	0
21	ISE_ADC1	ADC1 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
22	ISE_SSP0	SSP0 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
23	ISE_USART0	USART0 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
24	ISE_UART1	UART1 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
25	ISE_USART2	USART2 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
26	ISE_USART3	USART3 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0

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Table 887. Interrupt Set-Enable Register 0 register (ISER0 - address 0xE000 E100) bit description *…continued*

Bit	Symbol	Description	Reset value
27	ISE_I2S	IS2 interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
28	ISE_AES	AES interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
29	ISE_SPIFI	SPIFI interrupt enable. Write: writing 0 has no effect, writing 1 enables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
31:30	-	Reserved.	0

42.1.8.2 Interrupt Clear-Enable Register 0

The ICER0 register allows disabling the first 32 peripheral interrupts, or for reading the enabled state of those interrupts. Enabling interrupts is done through the ISER0 register (Section 42.1.8.1).

Table 888. Interrupt Clear-Enable Register 0 (ICER0 - address 0xE000 E180) bit description

Bit	Symbol	Description	Reset value
0	ICE_DAC	DAC interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
1	ICE_ER	Event router interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
2	ICE_DMA	DMA interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
4:3	-	Reserved	0
5	ICE_ETHERNET	Ethernet interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
6	ICE_SDIO	SDIO interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
7	ICE_LCD	LCD interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
8	ICE_USB0	USB0 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0

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Table 888. Interrupt Clear-Enable Register 0 (ICER0 - address 0xE000 E180) bit description *…continued*

Bit	Symbol	Description	Reset value
9	ICE_USB1	USB1 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
10	ICE_SCT	SCT interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
11	ICE_RIT	xxx interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
12	ICE_TIMER0	Timer0 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
13	ICE_TIMER1	Timer1 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
14	ICE_TIMER2	Timer2 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
15	ICE_TIMER3	Timer3 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
16	ICE_MOTOCONPWM	MOTOCONPWM interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
17	ICE_ADC0	ADC0 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
18	ICE_I2C0	I2C0 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
19	ICE_I2C1	I2C1 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
20	-	Reserved.	0
21	ICE_ADC1	ADC1 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
22	ICE_SSP0	SSP0 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0

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Table 888. Interrupt Clear-Enable Register 0 (ICER0 - address 0xE000 E180) bit description *…continued*

Bit	Symbol	Description	Reset value
23	ICE_SSP1	SSP1 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
24	ICE_USART0	USART0 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
25	ICE_UART1	UART1 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
26	ICE_USART2	USART2 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
27	ICE_USART3	USART3 interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
28	ICE_I2S	I2S interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
29	ICE_AES	AES interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
30	ICE_SPIFI	SPIFI interrupt disable. Write: writing 0 has no effect, writing 1 disables the interrupt. Read: 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.	0
31: 30	-	Reserved.	0

42.1.8.3 Interrupt Set-Pending Register 0 register

The ISPR0 register allows setting the pending state of the first 32 peripheral interrupts, or for reading the pending state of those interrupts. Clearing the pending state of interrupts is done through the ICPR0 register (Section 42.1.8.4).

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Table 889. Interrupt Set-Pending Register 0 register (ISPR0 - address 0xE000 E200) bit description

Bit	Symbol	Description	Reset value
0	ISP_DAC	DAC interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
1	ISP_ER	Event router interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
2	ISP_DMA	DMA interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
4:3	-	xxx interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
5	ISP_ETHERNET	ETHERNET interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
6	ISP_SDIO	SDIO interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
7	ISP_LCD	LCD interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
8	ISP_USB0	USB0 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
9	ISP_USB1	USB1 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
10	ISP_SCT	SCT interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
11	ISP_RIT	RIT interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
12	ISP_TIMER0	Timer0 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
13	ISP_TIMER1	Timer1 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
14	ISP_TIMER2	Timer2 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0

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Table 889. Interrupt Set-Pending Register 0 register (ISPR0 - address 0xE000 E200) bit description *…continued*

Bit	Symbol	Description	Reset value
15	ISP_TIMER3	Timer3 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
16	ISP_MOTOCON PWM	MOTOCONPWM interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
17	ISP_ADC0	ADC0 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
18	ISP_I2C0	I2C0 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
19	ISP_I2C1	I2C1 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
20	-	Reserved.	0
21	ISP_ADC1	ADC1 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
22	ISP_SSP0	SSP0 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
23	ISP_SSP1	SSP1 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
24	ISP_USART0	USART0 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
25	ISP_UART1	UART1 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
26	ISP_USART2	USART2 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
27	ISP_USART3	USART3 interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
28	ISP_I2S	I2S interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0

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Table 889. Interrupt Set-Pending Register 0 register (ISPR0 - address 0xE000 E200) bit description *…continued*

Bit	Symbol	Description	Reset value
29	ISP_AES	AES interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
30	ISP_SPIFI	SPIFI interrupt pending set. Write: writing 0 has no effect, writing 1 changes the interrupt state to pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
31: 30	-	Reserved	0

42.1.8.4 Interrupt Clear-Pending Register 0 register

The ICPR0 register allows clearing the pending state of the peripheral interrupts, or for reading the pending state of those interrupts. Setting the pending state of interrupts is done through the ISPR0 register (Section 42.1.8.3).

Table 890. Interrupt Clear-Pending Register 0 register (ICPR0 - address 0xE000 E280) bit description

Bit	Symbol	Description	Reset value
0	ICP_DAC	DAC interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
1	ICP_ER	Event router interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
2	ICP_DMA	DMA interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
4:3	-	Reserved.	0
5	ICP_ETHERNET	ETHERNET interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
6	ICP_SDIO	SDIO interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
7	ICP_LCD	LCD interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
8	ICP_USB0	USB0 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
9	ICP_USB1	USB1interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0

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Table 890. Interrupt Clear-Pending Register 0 register (ICPR0 - address 0xE000 E280) bit description ...continued

Bit	Symbol	Description	Reset value
10	ICP_SCT	SCT interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
11	ICP_RIT	RIT interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
12	ICP_TIMER0	Timer0 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
13	ICP_TIMER1	Timer1 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
14	ICP_TIMER2	Timer2 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
15	ICP_TIMER3	Timer3 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
16	ICP_MOTOCON PWM	MOTOCONPWM interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
17	ICP_ADC0	ADC0 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
18	ICP_I2C0	I2C0 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
19	ICP_I2C1	I2C1 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
20	-	Reserved.	0
21	ICP_ADC1	ADC1 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
22	ICP_SSP0	SSP0 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
23	ICP_SSP1	SSP1 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0

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Table 890. Interrupt Clear-Pending Register 0 register (ICPR0 - address 0xE000 E280) bit description *…continued*

Bit	Symbol	Description	Reset value
24	ICP_USART0	USART0 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
25	ICP_UART1	UART1 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
26	ICP_USART2	USART2 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
27	ICP_USART3	USART3 interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
28	ICP_I2S	I2S interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
29	ICP_AES	AES interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
30	ICP_SPIFI	SPIFI interrupt pending clear. Write: writing 0 has no effect, writing 1 changes the interrupt state to not pending. Read: 0 indicates that the interrupt is not pending, 1 indicates that the interrupt is pending.	0
31:30	-	Reserved.	0

42.1.8.5 Interrupt Active Bit Register 0

The IABR0 register is a read-only register that allows reading the active state of the first 32 peripheral interrupts. This allows determining which peripherals are asserting an interrupt to the NVIC. An interrupt may also be pending if enabled.

Table 891. Interrupt Active Bit Register 0 (IABR0 - address 0xE000 E300) bit description

Bit	Symbol	Description	Reset value
0	IAB_DAC	DAC interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
1	IAB_ER	Event router interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
2	IAB_DMA	DMA interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
4:3	-		0
5	IAB_ETHERNET	Ethernet interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
6	IAB_SDIO	SDIO interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0

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Table 891. Interrupt Active Bit Register 0 (IABR0 - address 0xE000 E300) bit description *…continued*

Bit	Symbol	Description	Reset value
7	IAB_LCD	LCD interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
8	IAB_USB0	USB0 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
9	IAB_USB1	USB1 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
10	IAB_SCT	SCT interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
11	IAB_RIT	RIT interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
12	IAB_TIMER0	Timer0 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
13	IAB_TIMER1	Timer1 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
14	IAB_TIMER2	Timer2 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
15	IAB_TIMER3	Timer3 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
16	IAB_MOTOCONPWM	MOTOCONPWM interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
17	IAB_ADC0	ADC0 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
18	IAB_I2C0	I2C0 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
19	IAB_I2C1	I2C1 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
20	-	Reserved.	0
21	IAB_ADC1	ADC1 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
22	IAB_SSP0	SSP0 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
23	IAB_SSP1	SSP1 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
24	IAB_USART0	USART0 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
25	IAB_UART1	UART1 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
26	IAB_USART2	USART2 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
27	IAB_USART3	USART3 interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0

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Table 891. Interrupt Active Bit Register 0 (IABR0 - address 0xE000 E300) bit description *…continued*

Bit	Symbol	Description	Reset value
28	IAB_I2S	I2S interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
29	IAB_AES	AES interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
30	IAB_SPIFI	SPIFI interrupt active. Read: 0 indicates that the interrupt is not active, 1 indicates that the interrupt is active.	0
31: 30	-	Reserved.	0

42.1.8.6 Interrupt Priority Register 0

The IPR0 register controls the priority of the first 4 peripheral interrupts. Each interrupt can have one of 32 priorities, where 0 is the highest priority.

Table 892. Interrupt Priority Register 0 (IPR0 - address 0xE000 E400) bit description

Bit	Symbol	Description	Reset value
2:0	-	Reserved. These bits ignore writes, and read as 0.	0
7:3	IP_DAC	DAC interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
10:8	-	Reserved.These bits ignore writes, and read as 0.	0
15:11	IP_ER	Event router interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
18:16	-	These bits ignore writes, and read as 0.	0
23:19	IP_DMA	DMA interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
26:24	-	Reserved.These bits ignore writes, and read as 0.	0
31:27	-	Reserved.	-

42.1.8.7 Interrupt Priority Register 1

The IPR1 register controls the priority of the second group of 4 peripheral interrupts. Each interrupt can have one of 32 priorities, where 0 is the highest priority.

Table 893. Interrupt Priority Register 1 (IPR1 - address 0xE000 E404) bit description

Bit	Symbol	Description	Reset value
2:0	-	Reserved.These bits ignore writes, and read as 0.	0
7:3	-	Reserved.	0
10:8	-	Reserved.These bits ignore writes, and read as 0.	0
15:11	IP_ETHERNET	ETHERNET interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
18:16	-	Reserved.These bits ignore writes, and read as 0.	0

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Table 893. Interrupt Priority Register 1 (IPR1 - address 0xE000 E404) bit description *…continued*

Bit	Symbol	Description	Reset value
23:19	IP_SDIO	SDIO interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
26:24	-	Reserved.These bits ignore writes, and read as 0.	0
31:27	IP_LCD	LCD interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0

42.1.8.8 Interrupt Priority Register 2

The IPR2 register controls the priority of the third group of 4 peripheral interrupts. Each interrupt can have one of 32 priorities, where 0 is the highest priority.

Table 894. Interrupt Priority Register 2 (IPR2 - address 0xE000 E408) bit description

Bit	Symbol	Description	Reset value
2:0	-	Reserved.These bits ignore writes, and read as 0.	0
7:3	IP_USB0	USB0 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
10:8	-	Reserved.These bits ignore writes, and read as 0.	0
15:11	IP_USB1	USB1 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
18:16	-	Reserved.These bits ignore writes, and read as 0.	0
23:19	IP_SCT	SCT interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
26:24	-	Reserved.These bits ignore writes, and read as 0.	0
31:27	IP_RIT	RIT interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0

42.1.8.9 Interrupt Priority Register 3

The IPR3 register controls the priority of the fourth group of 4 peripheral interrupts. Each interrupt can have one of 32 priorities, where 0 is the highest priority.

Table 895. Interrupt Priority Register 3 (IPR3 - address 0xE000 E40C) bit description

Bit	Symbol	Description	Reset value
2:0	-	Reserved.These bits ignore writes, and read as 0.	0
7:3	IP_TIMER0	TIMER0 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
10:8	-	Reserved.These bits ignore writes, and read as 0.	0
15:11	IP_TIMER1	TIMER1 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
18:16	-	Reserved.These bits ignore writes, and read as 0.	0
23:19	IP_TIMER2	TIMER2 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
26:24	-	Reserved.These bits ignore writes, and read as 0.	0
31:27	IP_TIMER3	TIMER3 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0

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42.1.8.10 Interrupt Priority Register 4

The IPR4 register controls the priority of the fifth group of 4 peripheral interrupts. Each interrupt can have one of 32 priorities, where 0 is the highest priority.

Table 896. Interrupt Priority Register 4 (IPR4 - address 0xE000 E410) bit description

Bit	Symbol	Description	Reset value
2:0	-	Reserved.These bits ignore writes, and read as 0.	0
7:3	IP_MOTOCONPWM	MOTOCONPWM interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
10:8	-	Reserved.These bits ignore writes, and read as 0.	0
15:11	IP_ADC0	ADC0 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
18:16	-	Reserved.These bits ignore writes, and read as 0.	0
23:19	IP_I2C0	I2C0 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
26:24	-	Reserved.These bits ignore writes, and read as 0.	0
31:27	IP_I2C1	I2C1 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0

42.1.8.11 Interrupt Priority Register 5

The IPR5 register controls the priority of the sixth group of 4 peripheral interrupts. Each interrupt can have one of 32 priorities, where 0 is the highest priority.

Table 897. Interrupt Priority Register 5 (IPR5 - address 0xE000 E414) bit description

Bit	Symbol	Description	Reset value
2:0	-	Reserved.These bits ignore writes, and read as 0.	0
7:3	-	Reserved.	0
10:8	-	Reserved.These bits ignore writes, and read as 0.	0
15:11	IP_ADC1	ADC1 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
18:16	-	Reserved.These bits ignore writes, and read as 0.	0
23:19	IP_SSP0	SSP0 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
26:24	-	Reserved.These bits ignore writes, and read as 0.	0
31:27	IP_SSP1	SSP1 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0

42.1.8.12 Interrupt Priority Register 6

The IPR6 register controls the priority of the seventh group of 4 peripheral interrupts. Each interrupt can have one of 32 priorities, where 0 is the highest priority.

Table 898. Interrupt Priority Register 6 (IPR6 - address 0xE000 E418) bit description

Bit	Symbol	Description	Reset value
2:0	-	Reserved.These bits ignore writes, and read as 0.	0
7:3	IP_USART0	USART0 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
10:8	-	Reserved.These bits ignore writes, and read as 0.	0

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Table 898. Interrupt Priority Register 6 (IPR6 - address 0xE000 E418) bit description

Bit	Symbol	Description	Reset value
15:11	IP_UART1	UART1 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
18:16	-	Reserved.These bits ignore writes, and read as 0.	0
23:19	IP_USART2	USART2 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
26:24	-	Reserved.These bits ignore writes, and read as 0.	0
31:27	IP_USART3	USART3 interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0

42.1.8.13 Interrupt Priority Register 7

The IPR7 register controls the priority of the eighth group of 4 peripheral interrupts. Each interrupt can have one of 32 priorities, where 0 is the highest priority.

Table 899. Interrupt Priority Register 7 (IPR7 - address 0xE000 E41C) bit description

Bit	Symbol	Description	Reset value
2:0	-	Reserved.These bits ignore writes, and read as 0.	0
7:3	IP_I2S	I2S interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
10:8	-	Reserved.These bits ignore writes, and read as 0.	0
15:11	IP_AES	AES interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
18:16	-	Reserved.These bits ignore writes, and read as 0.	0
23:19	IP_SPIFI	SPIFI interrupt priority. 0 = highest priority. 31 (0x1F) = lowest priority.	0
31:24	-	Reserved.These bits ignore writes, and read as 0.	0

42.1.8.14 Software Trigger Interrupt Register (STIR - 0xE000 EF00)

The STIR register provides an alternate way for software to generate an interrupt, in addition to using the ISPR registers. This mechanism can only be used to generate peripheral interrupts, not system exceptions.

By default, only privileged software can write to the STIR register. Unprivileged software can be given this ability if privileged software sets the USERSETMPEND bit in the CCR register.

Table 900. Software Trigger Interrupt Register (STIR - address 0xE000 EF00) bit description

Bit	Symbol	Description	Reset value
8:0	INTID	Writing a value to this field generates an interrupt for the specified Interrupt ID (see Table 885).	
31:9	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

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42.2 LPC1850/30/20/10 Rev '-' Event router

42.2.1 How to read this chapter

Remark: The event router controls various event inputs to the NVIC and the wake-up process.

The available event router sources vary for different parts.

- Ethernet: available on LPC1850/30.
- USB0: available on LPC1850/30/20.
- USB1: available on LPC1850/30.

42.2.2 Basic configuration

Table 901. Event router clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to event router	BASE_M3_CLK	CLK_M3_BUS	150 MHz

42.2.3 General description

The event router is used to process wake-up events such as certain interrupts and external or internal inputs for wake-up from any of the low power modes (Sleep, Deep-sleep, Power-down, and Deep power-down modes). The event router has multiple event inputs from various peripherals. When the proper edge detection is set in the EDGE configuration register, the event router can wake up the part or can raise an interrupt in the NVIC.

Each event input to the event router can be configured to trigger an output signal on rising or falling edges or on HIGH or LOW levels. The event router combines all events to an output signal which is used as follows:

- Create an interrupt if the event router interrupt is enabled in the NVIC.
- Send a wake-up signal to the power management unit to wake up from Deep-sleep, Power-down, and Deep power-down modes.
- Send a wake-up signal to CCU1 and CCU2 for waking up from Sleep mode (see Section 14.5.3).

Remark: The ATIMER, RTC, BOD, WDT, CAN and QEI events are routed through the event router and have no direct connection to the NVIC. When proper edge detection in the Event router is set for the peripheral events, the event router can generate an interrupt in the NVIC.

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42.2.4 Event router inputs

Table 902. Event router inputs

Event #	Source	Notes
0	WAKEUP0	WAKEUP0 pin
1	WAKEUP1	WAKEUP1 pin
2	WAKEUP2	WAKEUP2 pin
3	WAKEUP3	WAKEUP3 pin
4	Alarm timer	Alarm timer interrupt
5	RTC	RTC interrupt
6	BOD	BOD interrupt
7	WWDT	WWDT interrupt
8	Ethernet	Wake-up packet indicator
9	USB0	Wake-up request
10	USB1	ahb_needclk signal
11	-	Reserved
12	C_CAN	C_CAN interrupt
13	Combined timer output 2	Output 2 of the combined timer (ORed output of SCT output 2 and the match channel 2 of timer 0). See Figure 178.
14	Combined timer output 6	Output 6 of the combined timer (ORed output of SCT output 6 and the match channel 2 of timer 1). See Figure 178.
15	QEI	QEI interrupt
16	Combined timer output 14	Output 14 of the combined timer (ORed output of SCT output 14 and the match channel 2 of timer 3). See Figure 178.
17	-	Reserved
18	-	Reserved
19	Reset	<tbd>

42.2.5 Pin description

Table 903. Event router pin description

Pin	Direction	Description
WAKEUP0/1/2/3	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.

42.2.6 Register description

Table 904. Register overview: Event router (base address 0x4004 4000)

Name	Access	Address offset	Description	Reset Value
HILO	R/W	0x000	Level configuration register	0x000
EDGE	R/W	0x004	Edge configuration	0x000
-	-	0x008 - 0xFD4	Reserved	-

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Table 904. Register overview: Event router (base address 0x4004 4000)

Name	Access	Address offset	Description	Reset Value
CLR_EN	W	0xFD8	Event clear enable register	0x0
SET_EN	W	0xFDC	Event set enable register	0x0
STATUS	R	0xFE0	Status register	0x0
ENABLE	R	0xFE4	Enable register	0x0
CLR_STAT	W	0xFE8	Clear register	0x0
SET_STAT	W	0xFEC	Set register	0x0

42.2.6.1 Level configuration register

This register works in combination with the edge configuration register EDGE (see Table 907) to configure the level and edge detection for each input to the event router.

Table 905. Level configuration register (HILO - address 0x4004 4000) bit description

Bit	Symbol	Value	Description	Reset value
0	WAKEUP0_L		Level detect mode for WAKEUP0 event.	0
		0	Detect LOW level if bit 0 in the EDGE register is 0. Detect falling edge if bit 0 in the EDGE register is 1.	
		1	Detect HIGH level if bit 0 in the EDGE register is 0. Detect rising edge if bit 0 in the EDGE register is 1.	
1	WAKEUP1_L		Level detect mode for WAKEUP1 event. The corresponding bit in the EDGE register must be 0.	0
		0	Detect LOW level if bit 1 in the EDGE register is 0.	
		1	Detect HIGH level if bit 1 in the EDGE register is 0. Detect rising edge if bit 1 in the EDGE register is 1.	
2	WAKEUP2_L		Level detect mode for WAKEUP2 event.	0
		0	Detect LOW level if bit 2 in the EDGE register is 0. Detect falling edge if bit 2 in the EDGE register is 1.	
		1	Detect HIGH level if bit 2 in the EDGE register is 0. Detect rising edge if bit 2 in the EDGE register is 1.	
3	WAKEUP3_L		Level detect mode for WAKEUP3 event.	0
		0	Detect LOW level if bit 3 in the EDGE register is 0. Detect falling edge if bit 3 in the EDGE register is 1.	
		1	Detect HIGH level if bit 3 in the EDGE register is 0. Detect rising edge if bit 3 in the EDGE register is 1.	
4	ATIMER_L		Level detect mode for alarm timer event.	0
		0	Detect LOW level if bit 4 in the EDGE register is 0. Detect falling edge if bit 4 in the EDGE register is 1.	
		1	Detect HIGH level if bit 4 in the EDGE register is 0. Detect rising edge if bit 4 in the EDGE register is 1.	
5	RTC_L		Level detect mode for RTC event.	0
		0	Detect LOW level if bit 5 in the EDGE register is 0. Detect falling edge if bit 5 in the EDGE register is 1.	
		1	Detect HIGH level if bit 5 in the EDGE register is 0. Detect rising edge if bit 5 in the EDGE register is 1.	

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Table 905. Level configuration register (HILO - address 0x4004 4000) bit description

Bit	Symbol	Value	Description	Reset value
6	BOD_L		Level detect mode for BOD event.	0
		0	Detect LOW level if bit 6 in the EDGE register is 0. Detect falling edge if bit 6 in the EDGE register is 1.	
		1	Detect HIGH level if bit 6 in the EDGE register is 0. Detect rising edge if bit 6 in the EDGE register is 1.	
7	WWDT_L		Level detect mode for WWDTD event.	0
		0	Detect LOW level if bit 7 in the EDGE register is 0. Detect falling edge if bit 7 in the EDGE register is 1.	
		1	Detect HIGH level if bit 7 in the EDGE register is 0. Detect rising edge if bit 7 in the EDGE register is 1.	
8	ETH_L		Level detect mode for ethernet event.	0
		0	Detect LOW level if bit 8 in the EDGE register is 0. Detect falling edge if bit 8 in the EDGE register is 1.	
		1	Detect HIGH level if bit 8 in the EDGE register is 0. Detect rising edge if bit 8 in the EDGE register is 1.	
9	USB0_L		Level detect mode for USB0 event.	0
		0	Detect LOW level if bit 9 in the EDGE register is 0. Detect falling edge if bit 9 in the EDGE register is 1.	
		1	Detect HIGH level if bit 9 in the EDGE register is 0. Detect rising edge if bit 9 in the EDGE register is 1.	
10	USB1_L		Level detect mode for USB1 event.	0
		0	Detect LOW level if bit 10 in the EDGE register is 0. Detect falling edge if bit 10 in the EDGE register is 1.	
		1	Detect HIGH level if bit 10 in the EDGE register is 0. Detect rising edge if bit 10 in the EDGE register is 1.	
11	-	-	Reserved.	
12	CAN_L		Level detect mode for C_CAN event.	0
		0	Detect LOW level if bit 12 in the EDGE register is 0. Detect falling edge if bit 12 in the EDGE register is 1.	
		1	Detect HIGH level if bit 12 in the EDGE register is 0. Detect rising edge if bit 12 in the EDGE register is 1.	
13	TIM2_L		Level detect mode for combined timer output 2 event.	0
		0	Detect LOW level if bit 13 in the EDGE register is 0. Detect falling edge if bit 13 in the EDGE register is 1.	
		1	Detect HIGH level if bit 13 in the EDGE register is 0. Detect rising edge if bit 13 in the EDGE register is 1.	
14	TIM6_L		Level detect mode for combined timer output 6 event.	0
		0	Detect LOW level if bit 14 in the EDGE register is 0. Detect falling edge if bit 14 in the EDGE register is 1.	
		1	Detect HIGH level if bit 14 in the EDGE register is 0. Detect rising edge if bit 14 in the EDGE register is 1.	

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Table 905. Level configuration register (HILO - address 0x4004 4000) bit description

Bit	Symbol	Value	Description	Reset value
15	QEI_L		Level detect mode for QEI event.	0
		0	Detect LOW level if bit 15 in the EDGE register is 0. Detect falling edge if bit 15 in the EDGE register is 1.	
		1	Detect HIGH level if bit 15 in the EDGE register is 0. Detect rising edge if bit 15 in the EDGE register is 1.	
16	TIM14_L		Level detect mode for combined timer output 14 event.	0
		0	Detect LOW level if bit 16 in the EDGE register is 0. Detect falling edge if bit 16 in the EDGE register is 1.	
		1	Detect HIGH level if bit 16 in the EDGE register is 0. Detect rising edge if bit 16 in the EDGE register is 1.	
18:17	-	-	Reserved.	
19	RESET_L		Level detect mode for RESET event.	0
		0	Detect LOW level if bit 17 in the EDGE register is 0. Detect falling edge if bit 17 in the EDGE register is 1.	
		1	Detect HIGH level if bit 17 in the EDGE register is 0. Detect rising edge if bit 17 in the EDGE register is 1.	
31:20	-	-	Reserved.	

42.2.6.2 Edge configuration register

This register works in combination with the level configuration register HILO (see Table 905) to configure the level or edge detection for each input to the event router.

The EDGE configuration register determines whether the event router responds to a level change (EDGEn=1), or a constant level (EDGEn=0). The HILOn bit determines a response to a rising edge (HILOn=1) or a falling edge (HILOn=0).

Table 906. EDGE and HILO combined register settings

HILOn	EDGEn	Description
0	0	Detect LOW level
0	1	Detect falling edge
1	0	Detect HIGH level
1	1	Detect rising edge

When a HIGH level detect is active, the event router status bits cannot be cleared until the signal is LOW. When a rising edge detect is active, the event router status bit can be cleared right after the event has occurred.

Table 907. Edge configuration register (EDGE - address 0x4004 4004) bit description

Bit	Symbol	Value	Description	Reset value
0	WAKEUP0_E		Edge detect mode for WAKEUP0 event.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 0 in the HILO register is 0. Detect rising edge if bit 0 in the HILO register is 1.	

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Table 907. Edge configuration register (EDGE - address 0x4004 4004) bit description

Bit	Symbol	Value	Description	Reset value
1	WAKEUP1_E		Edge/level detect mode for WAKEUP1 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 1 in the HILO register is 0. Detect rising edge if bit 1 in the HILO register is 1.	
2	WAKEUP2_E		Edge/level detect mode for WAKEUP2 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 2 in the HILO register is 0. Detect rising edge if bit 2 in the HILO register is 1.	
3	WAKEUP3_E		Edge/level detect mode for WAKEUP3 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 30 in the HILO register is 0. Detect rising edge if bit 3 in the HILO register is 1.	
4	ATIMER_E		Edge/level detect mode for alarm timer event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 4 in the HILO register is 0. Detect rising edge if bit 4 in the HILO register is 1.	
5	RTC_E		Edge/level detect mode for RTC event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 5 in the HILO register is 0. Detect rising edge if bit 5 in the HILO register is 1.	
6	BOD_E		Edge/level detect mode for BOD event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 6 in the HILO register is 0. Detect rising edge if bit 6 in the HILO register is 1.	
7	WWDT_E		Edge/level detect mode for WWDTD event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 7 in the HILO register is 0. Detect rising edge if bit 7 in the HILO register is 1.	

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Table 907. Edge configuration register (EDGE - address 0x4004 4004) bit description

Bit	Symbol	Value	Description	Reset value
8	ETH_E		Edge/level detect mode for ethernet event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 8 in the HILO register is 0. Detect rising edge if bit 8 in the HILO register is 1.	
9	USB0_E		Edge/level detect mode for USB0 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 9 in the HILO register is 0. Detect rising edge if bit 9 in the HILO register is 1.	
10	USB1_E		Edge/level detect mode for USB1 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 10 in the HILO register is 0. Detect rising edge if bit 10 in the HILO register is 1.	
11	-	-	Reserved.	
12	CAN_E		Edge/level detect mode for C_CAN event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 12 in the HILO register is 0. Detect rising edge if bit 12 in the HILO register is 1.	
13	TIM2_E		Edge/level detect mode for combined timer output 2 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 13 in the HILO register is 0. Detect rising edge if bit 13 in the HILO register is 1.	
14	TIM6_E		Edge/level detect mode for combined timer output 6 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 14 in the HILO register is 0. Detect rising edge if bit 14 in the HILO register is 1.	
15	QEI_E		Edge/level detect mode for QEI interrupt signal. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 15 in the HILO register is 0. Detect rising edge if bit 15 in the HILO register is 1.	

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Table 907. Edge configuration register (EDGE - address 0x4004 4004) bit description

Bit	Symbol	Value	Description	Reset value
16	TIM14_E		Edge/level detect mode for combined timer output 14 event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 16 in the HILO register is 0. Detect rising edge if bit 16 in the HILO register is 1.	
18:17	-	-	Reserved.	
19	RESET_E		Edge/level detect mode for RESET event. The corresponding bit in the EDGE register must be 0.	0
		0	Level detect.	
		1	Edge detect. Detect falling edge if bit 19 in the HILO register is 0. Detect rising edge if bit 19 in the HILO register is 1.	
31:20	-	-	Reserved.	

42.2.6.3 Interrupt clear enable register

Table 908. Interrupt clear enable register (CLR_EN - address 0x4004 4FD8) bit description

Bit	Symbol	Description	Reset value
0	WAKEUP0_CLREN	Writing a 1 to this bit clears the event enable bit 0 in the ENABLE register.	-
1	WAKEUP1_CLREN	Writing a 1 to this bit clears the event enable bit 1 in the ENABLE register.	-
2	WAKEUP2_CLREN	Writing a 1 to this bit clears the event enable bit 2 in the ENABLE register.	-
3	WAKEUP3_CLREN	Writing a 1 to this bit clears the event enable bit 3 in the ENABLE register.	-
4	ATIMER_CLREN	Writing a 1 to this bit clears the event enable bit 4 in the ENABLE register.	-
5	RTC_CLREN	Writing a 1 to this bit clears the event enable bit 5 in the ENABLE register.	-
6	BOD_CLREN	Writing a 1 to this bit clears the event enable bit 6 in the ENABLE register.	-
7	WWDT_CLREN	Writing a 1 to this bit clears the event enable bit 7 in the ENABLE register.	-
8	ETH_CLREN	Writing a 1 to this bit clears the event enable bit 8 in the ENABLE register.	-
9	USB0_CLREN	Writing a 1 to this bit clears the event enable bit 9 in the ENABLE register.	-
10	USB1_CLREN	Writing a 1 to this bit clears the event enable bit 10 in the ENABLE register.	-
11	-	Reserved.	-
12	CAN_CLREN	Writing a 1 to this bit clears the event enable bit 12 in the ENABLE register.	-

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Table 908. Interrupt clear enable register (CLR_EN - address 0x4004 4FD8) bit description

Bit	Symbol	Description	Reset value
13	TIM2_CLREN	Writing a 1 to this bit clears the event enable bit 13 in the ENABLE register.	-
14	TIM6_CLREN	Writing a 1 to this bit clears the event enable bit 14 in the ENABLE register.	-
15	QEI_CLREN	Writing a 1 to this bit clears the event enable bit 15 in the ENABLE register.	-
16	TIM14_CLREN	Writing a 1 to this bit clears the event enable bit 16 in the ENABLE register.	-
18:17	-	Reserved.	-
19	RESET_CLREN	Writing a 1 to this bit clears the event enable bit 19 in the ENABLE register.	-
31:20	-	Reserved.	-

42.2.6.4 Event set enable register

Table 909. Event set enable register (SET_EN - address 0x4004 4FDC) bit description

Bit	Symbol	Description	Reset value
0	WAKEUP0_SETEN	Writing a 1 to this bit sets the event enable bit 0 in the ENABLE register.	-
1	WAKEUP1_SETEN	Writing a 1 to this bit sets the event enable bit 1 in the ENABLE register.	-
2	WAKEUP2_SETEN	Writing a 1 to this bit sets the event enable bit 2 in the ENABLE register.	-
3	WAKEUP3_SETEN	Writing a 1 to this bit sets the event enable bit 3 in the ENABLE register.	-
4	ATIMER_SETEN	Writing a 1 to this bit sets the event enable bit 4 in the ENABLE register.	-
5	RTC_SETEN	Writing a 1 to this bit sets the event enable bit 5 in the ENABLE register.	-
6	BOD_SETEN	Writing a 1 to this bit sets the event enable bit 6 in the ENABLE register.	-
7	WWDT_SETEN	Writing a 1 to this bit sets the event enable bit 7 in the ENABLE register.	-
8	ETH_SETEN	Writing a 1 to this bit sets the event enable bit 8 in the ENABLE register.	-
9	USB0_SETEN	Writing a 1 to this bit sets the event enable bit 9 in the ENABLE register.	-
10	USB1_SETEN	Writing a 1 to this bit sets the event enable bit 10 in the ENABLE register.	-
11	-	Reserved.	-
12	CAN_SETEN	Writing a 1 to this bit sets the event enable bit 12 in the ENABLE register.	-
13	TIM2_SETEN	Writing a 1 to this bit sets the event enable bit 13 in the ENABLE register.	-

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Table 909. Event set enable register (SET_EN - address 0x4004 4FDC) bit description

Bit	Symbol	Description	Reset value
14	TIM6_SETEN	Writing a 1 to this bit sets the event enable bit 14 in the ENABLE register.	-
15	QEI_SETEN	Writing a 1 to this bit sets the event enable bit 15 in the ENABLE register.	-
16	TIM14_SETEN	Writing a 1 to this bit sets the event enable bit 16 in the ENABLE register.	-
18:17	-	Reserved.	-
19	RESET_SETEN	Writing a 1 to this bit sets the event enable bit 19 in the ENABLE register.	-
31:20	-	Reserved.	-

42.2.6.5 Event status register

Table 910. Interrupt status register (STATUS - address 0x4004 4FE0) bit description

Bit	Symbol	Description	Reset value
0	WAKEUP0_ST	A 1 in this bit shows that the WAKEUP0 event has been raised.	-
1	WAKEUP1_ST	A 1 in this bit shows that the WAKEUP1 event has been raised.	-
2	WAKEUP2_ST	A 1 in this bit shows that the WAKEUP2 event has been raised.	-
3	WAKEUP3_ST	A 1 in this bit shows that the WAKEUP3 event has been raised.	-
4	ATIMER_ST	A 1 in this bit shows that the ATIMER event has been raised.	-
5	RTC_ST	A 1 in this bit shows that the RTC event has been raised.	-
6	BOD_ST	A 1 in this bit shows that the BOD event has been raised.	-
7	WWDT_ST	A 1 in this bit shows that the WWDT event has been raised.	-
8	ETH_ST	A 1 in this bit shows that the ETHERNET event has been raised.	-
9	USB0_ST	A 1 in this bit shows that the USB0 event has been raised.	-
10	USB1_ST	A 1 in this bit shows that the USB1 event has been raised.	-
11	-	Reserved.	-
12	CAN_ST	A 1 in this bit shows that the C_CAN event has been raised.	-
13	TIM2_ST	A 1 in this bit shows that the combined timer 2 output event has been raised.	-
14	TIM6_ST	A 1 in this bit shows that the combined timer 6 output event has been raised.	-
15	QEI_ST	A 1 in this bit shows that the QEI event has been raised.	-
16	TIM14_ST	A 1 in this bit shows that the combined timer 14 output event has been raised.	-
18:17	-	Reserved.	-
19	RESET_ST	A 1 in this bit shows that the <tbd> event has been raised.	-
31:20	-	Reserved.	-

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42.2.6.6 Event enable register

Table 911. Event enable register (ENABLE - address 0x4004 4FE4) bit description

Bit	Symbol	Description	Reset value
0	WAKEUP0_EN	A 1 in this bit shows that the WAKEUP0 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
1	WAKEUP1_EN	A 1 in this bit shows that the WAKEUP1 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
2	WAKEUP2_EN	A 1 in this bit shows that the WAKEUP2 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
3	WAKEUP3_EN	A 1 in this bit shows that the WAKEUP3 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
4	ATIMER_EN	A 1 in this bit shows that the ATIMER event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
5	RTC_EN	A 1 in this bit shows that the RTC event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
6	BOD_EN	A 1 in this bit shows that the BOD event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
7	WWDT_EN	A 1 in this bit shows that the WWDT event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
8	ETH_EN	A 1 in this bit shows that the ETHERNET event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
9	USB0_EN	A 1 in this bit shows that the USB0 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
10	USB1_EN	A 1 in this bit shows that the USB1 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
11	-	Reserved.	-
12	CAN_EN	A 1 in this bit shows that the CAN event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
13	TIM2_EN	A 1 in this bit shows that the TIM2 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
14	TIM6_EN	A 1 in this bit shows that the TIM6 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
15	QEI_EN	A 1 in this bit shows that the QEI event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0

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Table 911. Event enable register (ENABLE - address 0x4004 4FE4) bit description

Bit	Symbol	Description	Reset value
16	TIM14_EN	A 1 in this bit shows that the TIM14 event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
18:17	-		-
19	RESET_EN	A 1 in this bit shows that the RESET event has been enabled. This event wakes up the chip and contributes to the event router interrupt when bit 0 = 1 in the STATUS register.	0
31:20	-	Reserved.	-

42.2.6.7 Clear status register

Table 912. Interrupt clear status register (CLR_STAT - address 0x4004 4FE8) bit description

Bit	Symbol	Description	Reset value
0	WAKEUP0_CLRST	Writing a 1 to this bit clears the STATUS event bit 0 in the STATUS register.	
1	WAKEUP1_CLRST	Writing a 1 to this bit clears the STATUS event bit 1 in the STATUS register.	
2	WAKEUP2_CLRST	Writing a 1 to this bit clears the STATUS event bit 2 in the STATUS register.	
3	WAKEUP3_CLRST	Writing a 1 to this bit clears the STATUS event bit 3 in the STATUS register.	
4	ATIMER_CLRST	Writing a 1 to this bit clears the STATUS event bit 4 in the STATUS register.	
5	RTC_CLRST	Writing a 1 to this bit clears the STATUS event bit 5 in the STATUS register.	
6	BOD_CLRST	Writing a 1 to this bit clears the STATUS event bit 6 in the STATUS register.	
7	WWDT_CLRST	Writing a 1 to this bit clears the STATUS event bit 7 in the STATUS register.	
8	ETH_CLRST	Writing a 1 to this bit clears the STATUS event bit 8 in the STATUS register.	
9	USB0_CLRST	Writing a 1 to this bit clears the STATUS event bit 9 in the STATUS register.	
10	USB1_CLRST	Writing a 1 to this bit clears the STATUS event bit 10 in the STATUS register.	
11	-	Reserved.	
12	CAN_CLRST	Writing a 1 to this bit clears the STATUS event bit 12 in the STATUS register.	
13	TIM2_CLRST	Writing a 1 to this bit clears the STATUS event bit 13 in the STATUS register.	
14	TIM6_CLRST	Writing a 1 to this bit clears the STATUS event bit 14 in the STATUS register.	
15	QEI_CLRST	Writing a 1 to this bit clears the STATUS event bit 15 in the STATUS register.	
16	TIM14_CLRST	Writing a 1 to this bit clears the STATUS event bit 16 in the STATUS register.	

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Table 912. Interrupt clear status register (CLR_STAT - address 0x4004 4FE8) bit description

Bit	Symbol	Description	Reset value
18:17	-		
19	RESET_CLRST	Writing a 1 to this bit clears the STATUS event bit 19 in the STATUS register.	
31:20	-	Reserved.	-

42.2.6.8 Set status register

Table 913. Interrupt set status register (SET_STAT - address 0x4004 4FEC) bit description

Bit	Symbol	Description	Reset value
0	WAKEUP0_SETST	Writing a 1 to this bit sets the STATUS event bit 0 in the STATUS register.	
1	WAKEUP1_SETST	Writing a 1 to this bit sets the STATUS event bit 1 in the STATUS register.	
2	WAKEUP2_SETST	Writing a 1 to this bit sets the STATUS event bit 2 in the STATUS register.	
3	WAKEUP3_SETST	Writing a 1 to this bit sets the STATUS event bit 3 in the STATUS register.	
4	ATIMER_SETST	Writing a 1 to this bit sets the STATUS event bit 4 in the STATUS register.	
5	RTC_SETST	Writing a 1 to this bit sets the STATUS event bit 5 in the STATUS register.	
6	BOD_SETST	Writing a 1 to this bit sets the STATUS event bit 6 in the STATUS register.	
7	WWDT_SETST	Writing a 1 to this bit sets the STATUS event bit 7 in the STATUS register.	
8	ETH_SETST	Writing a 1 to this bit sets the STATUS event bit 8 in the STATUS register.	
9	USB0_SETST	Writing a 1 to this bit sets the STATUS event bit 9 in the STATUS register.	
10	USB1_SETST	Writing a 1 to this bit sets the STATUS event bit 10 in the STATUS register.	
11	-	Reserved.	
12	CAN_SETST	Writing a 1 to this bit sets the STATUS event bit 12 in the STATUS register.	
13	TIM2_SETST	Writing a 1 to this bit sets the STATUS event bit 13 in the STATUS register.	
14	TIM6_SETST	Writing a 1 to this bit sets the STATUS event bit 14 in the STATUS register.	
15	QEI_SETST	Writing a 1 to this bit sets the STATUS event bit 15 in the STATUS register.	
16	TIM14_SETST	Writing a 1 to this bit sets the STATUS event bit 16 in the STATUS register.	

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Table 913. Interrupt set status register (SET_STAT - address 0x4004 4FEC) bit description

Bit	Symbol	Description	Reset value
18:17	-	Reserved.	
19	RESET_SETST	Writing a 1 to this bit sets the STATUS event bit 19 in the STATUS register.	
31:20	-	Reserved.	-

42.3 LPC1850/30/20/10 Rev ‘-’ CREG

42.3.1 How to read this chapter

Remark: This chapter applies to LPC1850/30/20/10 Rev ‘-’ only.

The available peripherals vary for different parts.

- Ethernet: available on LPC1850/30.
- USB0: available on LPC1850/30/20.
- USB1: available on LPC1850/30.

If a peripheral is not available, the corresponding bits in the CREG registers are reserved.

42.3.2 Basic configuration

The CREG block is configured as follows:

- See Table 925 for clocking and power control.
- The CREG block can not be reset by software.

Table 914. CREG clocking and power control

	Base clock	Branch clock	Maximum frequency
CREG	BASE_M3_CLK	CLK_M3_CREG	150 MHz

42.3.3 Features

The following settings are controlled in the configuration register block:

- BOD trip settings
- Oscillator output
- DMA-to-peripheral muxing
- Ethernet mode
- Memory mapping
- Timer/UART inputs
- USB0 ATX

In addition, the Creg block contains the part id and the part configuration information.

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42.3.4 Register description

Table 915. Register overview: Configuration registers (base address 0x4004 3000)

Name	Access	Address offset	Description	Reset value
IRCTRM	RO	0x000	IRC trim register	0x000F F2BC
CREG0	R/W	0x004	Chip configuration register 32 kHz oscillator output and BOD control register.	
PMUCON		0x008	Power mode control register.	0x0000 0000
-	-	0x008 - 0x0FC	Reserved	-
M3MEMMAP	R/W	0x100	ARM Cortex-M3 memory mapping	
-	-	0x104	Reserved	-
CREG1	RO	0x108	Chip configuration register 1	
CREG2	RO	0x10C	Chip configuration register 2	
CREG3	RO	0x110	Chip configuration register 3	
CREG4	RO	0x114	Chip configuration register 4	
CREG5	R/W	0x118	Chip configuration register 5. Controls JTAG access.	
DMAMUX	R/W	0x11C	DMA muxing control	
-	-	0x120 - 0x124	Reserved	-
ETBCFG	R/W	0x128	ETB RAM configuration	0x0000 0000
CREG6	R/W	0x12C	Chip configuration register 6.	
-	-	0x130 - 0x1FC	Reserved	-
CHIPID	RO	0x200	Part ID	
-	-	0x204 - 0x2FC	Reserved	-
-	-	0x300	Reserved	
-	-	0x304	Reserved	
-	-	0x308	Reserved	
-	-	0x30C - 0xEFC	Reserved	-
LOCKREG		0xF00	Lock register; blocks write access to CREG registers	

42.3.4.1 IRC trim register

Table 916. IRC trim register (IRCTRM, address 0x4004 3000) bit description

Bit	Symbol	Description	Reset value	Access
11:0	TRM	IRC trim value	0x2BC	R
19:12	-	Reserved	0xFF	R
31:20	-	Reserved	-	-

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42.3.4.2 CREG0 control register

Table 917. CREG0 register (CREG0, address 0x4004 3004) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	EN1KHZ		Enable 1 kHz output	0	R/W
		0	1 kHz output disabled		
		1	1 kHz output enabled		
1	EN32KHZ		Enable 32 kHz output	0	R/W
		0	32 kHz output disabled		
		1	32 kHz output enabled		
2	RESET32KHZ		32 kHz oscillator reset	1	R/W
		0	<tbd>		
		1	<tbd>		
3	32KHZPD		32 kHz power control	1	R/W
		0	32 kHz oscillator powered		
		1	32 kHz oscillator powered-down		
7:4	-		Reserved	-	-
9:8	BODLVL1		BOD trip level to generate an interrupt:	11	R/W
		0x0	2.75 V		
		0x1	2.85 V		
		0x2	2.95 V		
		0x3	3.05 V		
11:10	BODLVL2		BOD trip level to generate a reset:	11	R/W
		0x0	1.70 V		
		0x1	1.80 V		
		0x2	1.90 V		
		0x3	2.00 V		
31:12	-		Reserved	-	-

42.3.4.3 Power mode control register

For details on power mode selection, see Section 8.2.

Table 918. Power mode control register (PMUCON, address 0x4004 3008) bit description

Bit	Symbol	Value	Description	Reset value	Access
1:0	PMUCON		Controls power mode:	0	R/W
		0x0	Normal		
		0x1	Low-power		
		0x2	Reserved		
		0x3	Normal		
31:2	-		Reserved	-	-

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42.3.4.4 ARM Cortex-M3 memory mapping register

Table 919. Memory mapping register (M3MEMMAP, address 0x4004 3100) bit description

Bit	Symbol	Description	Reset value	Access
11:0		Reserved	0x000	-
31:12	M3MAP	this is the 32 kB ROM address - this is the shadow address when accessing memory at address 0x0000 0000	0x1040 0000	R/W

42.3.4.5 CREG5 control register

Table 920. CREG5 control register (CREG5, address 0x4004 3118) bit description

Bit	Symbol	Description	Reset value	Access
4:0	-	Reserved.	-	-
5	-	Reserved.	0	-
6	M3TAPSEL	Selects tap access to M3	0	R/W
7	-	Reserved. This bit must always be set to 0.	0	-
8	OTPJTAG	JTAG access to OTP	0	R/W
31:9	-	Reserved.	-	-

42.3.4.6 DMA muxing register

This register controls which set of peripherals is connected to the DMA controller (see Table 195).

Table 921. DMA muxing register (DMAMUX, address 0x4004 311C) bit description

Bit	Symbol	Value	Description	Reset value	Access
1:0	DMAMUXCH0		selects DMA to peripheral connection for DMA peripheral 0:	0	R/W
		0x0	SPIFI		
		0x1	Reserved		
		0x2	Reserved		
		0x3	Reserved		
3:2	DMAMUXCH1		selects DMA to peripheral connection for DMA peripheral 1:	0	R/W
		0x0	Timer 0, match channel 0		
		0x1	USART0 transmit		
		0x2	Reserved		
		0x3	Reserved		
5:4	DMAMUXCH2		selects DMA to peripheral connection for DMA peripheral 2:	0	R/W
		0x0	Timer 0, match channel 1		
		0x1	USART0 receive		
		0x2	Reserved		
		0x3	Reserved		

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Table 921. DMA muxing register (DMAMUX, address 0x4004 311C) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
7:6	DMAMUXCH3		selects DMA to peripheral connection for DMA peripheral 3:	0	R/W
		0x0	Timer 1, match channel 0		
		0x1	UART1 transmit		
		0x2	Reserved		
		0x3	Reserved		
9:8	DMAMUXCH4		selects DMA to peripheral connection for DMA peripheral 4:	0	R/W
		0x0	Timer 1, match channel 1		
		0x1	UART1 receive		
		0x2	Reserved		
		0x3	Reserved		
11:10	DMAMUXCH5		selects DMA to peripheral connection for DMA peripheral 5:	0	R/W
		0x0	Timer 2, match channel 0		
		0x1	USART2 transmit		
		0x2	Reserved		
		0x3	Reserved		
13:12	DMAMUXCH6		selects DMA to peripheral connection for DMA peripheral 6:	0	R/W
		0x0	Timer 2, match channel 1		
		0x1	USART2 receive		
		0x2	Reserved		
		0x3	Reserved		
15:14	DMAMUXCH7		selects DMA to peripheral connection for DMA peripheral 7:	0	R/W
		0x0	Timer 3, match channel 0		
		0x1	USART3 transmit		
		0x2	SCT output 0		
		0x3	Reserved		
17:16	DMAMUXCH8		selects DMA to peripheral connection for DMA peripheral 8:	0	R/W
		0x0	Timer 3, match channel 1		
		0x1	USART3 receive		
		0x2	SCT output 1		
		0x3	Reserved		

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Table 921. DMA muxing register (DMAMUX, address 0x4004 311C) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
19:18	DMAMUXCH9		selects DMA to peripheral connection for DMA peripheral 9:	0	R/W
		0x0	SSP0 receive		
		0x1	I2S0 channel 0		
		0x2	Reserved		
		0x3	Reserved		
21:20	DMAMUXCH10		selects DMA to peripheral connection for DMA peripheral 10:	0	R/W
		0x0	SSP0 transmit		
		0x1	I2S0 channel 1		
		0x2	Reserved		
		0x3	Reserved		
23:22	DMAMUXCH11		selects DMA to peripheral connection for DMA peripheral 11:	0	R/W
		0x0	SSP1 receive		
		0x1	Reserved		
		0x2	Reserved		
		0x3	Reserved		
25:24	DMAMUXCH12		selects DMA to peripheral connection for DMA peripheral 12:	0	R/W
		0x0	SSP1 transmit		
		0x1	I2S1 channel 0		
		0x2	Reserved		
		0x3	Reserved		
27:26	DMAMUXCH13		selects DMA to peripheral connection for DMA peripheral 13:	0	R/W
		0x0	ADC0		
		0x1	AES input		
		0x2	Reserved		
		0x3	Reserved		
29:28	DMAMUXCH14		selects DMA to peripheral connection for DMA peripheral 14:	0	R/W
		0x0	ADC1		
		0x1	AES output		
		0x2	Reserved		
		0x3	Reserved		

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Table 921. DMA muxing register (DMAMUX, address 0x4004 311C) bit description …continued

Bit	Symbol	Value	Description	Reset value	Access
31:30	DMAMUXCH15		selects DMA to peripheral connection for DMA peripheral 15:	0	R/W
		0x0	DAC		
		0x1	I2S1 channel 1		
		0x2	Reserved		
		0x3	Reserved		

42.3.4.7 ETB SRAM configuration register

This register selects the interface that is used to the 16 kB block of RAM located at address 0x2000 C000. This RAM memory block can be accessed either by the ETB or be used as normal SRAM on the AHB bus.

Note that by default, this memory area will be accessed by the ETB.

Table 922. ETB SRAM configuration register (ETBCFG, address 0x4004 3128) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	ETB		Select SRAM interface	0	R/W
		0	ETB accesses SRAM at address 0x2000 C000.		
		1	AHB accesses SRAM at address 0x2000 C000.		
31:1	-		Reserved.	-	-

42.3.4.8 CREG6 control register

This register controls various aspects of the LPC18xx:

- Bits 2:0 control the Ethernet PHY interface. The ethernet block reads this register during set-up, and therefore the ethernet must be reset after changing the PHY interface.
- Bits 5:4 control the input channel 7 of the combined timer inputs (see Figure 178). Input channel 7 is connected to input 7 of the SCT and the CAP2 channel of timer 3.
- Bits 8:6 control the input mux to the timer capture channels CAP1 and CAP2 and the SCT (see Figure 178). These particular capture inputs can be either routed to the timer input pins or are connected to the USART receive/transmit wait signal in smart card mode.

Table 923. CREG6 control register (CREG6, address 0x4004 312C) bit description

Bit	Symbol	Value	Description	Reset value	Access
2:0	ETHMODE		Selects the Ethernet mode. Reset the ethernet after changing the PHY interface. All other settings are reserved.		R/W
		0x0	MII		
		0x4	RMII		
3	-		USB0 ATX override. Selects USB0 RPU usage. Reserved.		R/W

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Table 923. CREG6 control register (CREG6, address 0x4004 312C) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
5:4	TIMIN7CTRL		Controls the input to timer 3 (CAP2) and the SCT (input 7):		R/W
		0x0	I2S0 receive mws signal		
		0x1	I2S0 transmit mws signal		
		0x2	USB0 SOF signal		
		0x3	USB1 SOF signal		
6	TIM1INCTRL		Controls the muxing of the timer1 CAP inputs CAP1 and CAP2.		R/W
		0	Timer1 CAP1 connected to pin CTIN_3; timer 1 CAP2 connected to CTIN_4.		
		1	Timer1 CAP1 connected to USART0 transmit wait; timer 1 CAP2 connected to USART0 receive wait.		
7	TIM2INCTRL		Controls the muxing of the timer 2 CAP inputs CAP1 and CAP2.		R/W
		0	Timer2 CAP1 connected to pin CTIN_1; timer 2 CAP2 connected to CTIN_4.		
		1	Timer2 CAP1 connected to USART2 transmit wait; timer 2 CAP2 connected to USART2 receive wait.		
8	TIM3INCTRL		Controls the muxing of the timer 3 CAP inputs CAP1 and CAP2.		R/W
		0	Timer3 CAP1 connected to pin CTIN_6; timer 3 CAP2 connected to combined timer input 7 (see bits 5:4).		
		1	Timer2 CAP1 connected to USART3 transmit wait; timer 2 CAP2 connected to USART3 receive wait.		
31:9	-		Reserved.	-	-

42.3.4.9 Part ID register

Table 924. Part ID register (CHIPID, address 0x4004 3200) bit description

Bit	Symbol	Description	Reset value	Access
31:0	ID	<tbd>		

42.4 LPC1850/30/20/10 Rev ‘-’ CGU

42.4.1 How to read this chapter

Remark: This chapter refers to the LPC1850/30/20/10 Rev ‘-’ parts only. See Chapter 9 for a description of the CGU for Parts LPC1850/30/20/10 Rev ‘A’ and all LPC18xx parts with on-chip flash.

Ethernet, USB0, USB1, and LCD related clocks are not available on all packages. The SDIO interface is not available. The corresponding clock control registers are reserved.

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42.4.2 Basic configuration

The CGU is configured as follows:

- See Table 925 for clocking and power control.
- Do not reset the CGU during normal operation.

Table 925. CGU clocking and power control

	Base clock	Branch clock	Maximum frequency
CGU	BASE_M3_CLK	CLK_M3_BUS	150 MHz

42.4.3 Features

- PLL0/1 control
- Oscillator control
- Clock generation and clock source multiplexing
- Five integer dividers

42.4.4 General description

The CGU generates multiple independent clocks for the core and the peripheral blocks of the LPC18xx. Each independent clock is called a base clock and itself is one of the inputs to the two Clock Control Units (CCUs) which control the branch clocks to the individual peripherals (see Chapter 14).

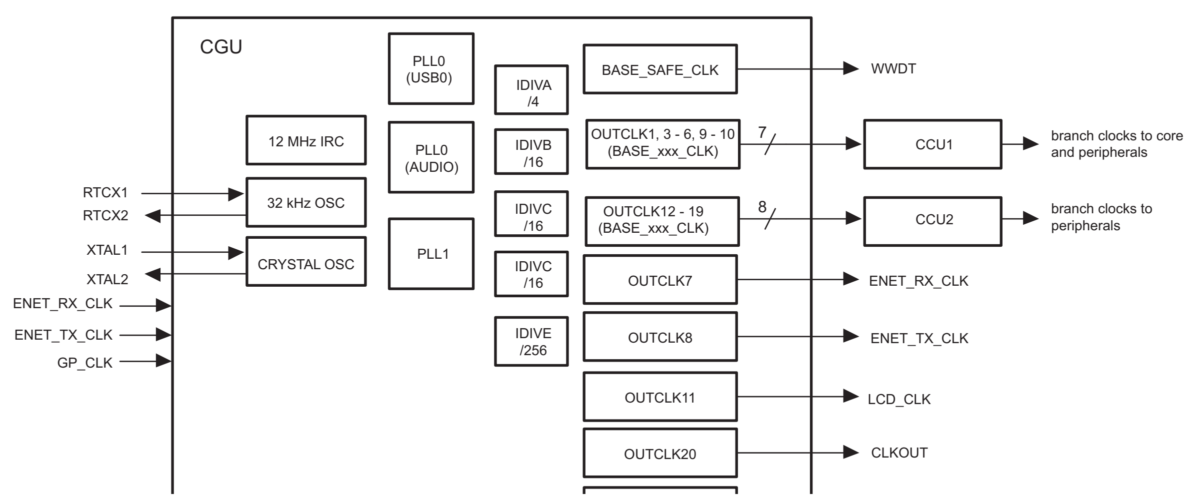


Fig 151. CGU and CCU0/1 block diagram

The CGU selects the inputs to the clock generators from multiple clock sources, controls the clock generation, and routes the outputs of the clock generators through the clock source bus to the output stages. Each output stage provides an independent clock source and corresponds to one of the base clocks for the LPC18xx. See Table 926 for a description of each base clock and Table 928 for the possible clock sources for each base clock.

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The CGU contains four types of clock generators:

1. External clock inputs and internal clocks: The external clock inputs are the Ethernet PHY clocks and the general purpose input clock GP_CLKIN. The clocks from the internal oscillators are the IRC and the 32 kHz oscillator output clocks. These clock generators have no selectable inputs from the clock source bus and provide one clock output each to the clock source bus.
2. Crystal oscillator: The crystal oscillator is controlled by the CGU. The input to the crystal oscillator are the XTAL pins. The crystal oscillator creates one output to the clock source bus.
3. PLLs: PLL0 and PLL1 are controlled by the CGU. Each PLL can select one input from the clock source bus and provides one output to the clock source bus. The input to the PLL can be selected from all external and internal clocks and oscillators, from the other PLL, and from the outputs of any of the integer dividers (see Table 927).
4. Integer dividers: Each of the five integer dividers can select one input from the clock source bus and creates one divided output clock to the clock source bus. The input to all integer dividers can be selected from all external and internal clocks and oscillators, and from both PLLs. In addition, the output of the first integer divider can be selected as an input to all other integer dividers (see Table 927). The integer dividers have different programmable division ratios:
   - Integer divider A: maximum division factor = 4 (see Table 939).
   - Integer dividers B, C, D: maximum division factor = 16 (see Table 940).
   - Integer divider E: maximum division factor = 256 (see Table 941).

The output stages select a clock source from the clock source bus for each base clock (see Table 928). Except for the base clocks to the WWDT (BASE_SAFE_CLK) and USB0 (BASE_USB0_CLK), the clock source for each output stage can be any of the external and internal clocks and oscillators directly or one of the PLL outputs or any of the outputs of the integer dividers.

Table 926. CGU0 base clocks

Number	Name	Frequency [1]	Description
0	BASE_SAFE_CLK	12 MHz	Base safe clock (always on) for WDT
1	BASE_USB0_CLK	480 MHz	Base clock for USB0
2	-	-	Reserved.
3	BASE_USB1_CLK	150 MHz	Base clock for USB1
4	BASE_M3_CLK	150 MHz	System base clock for ARM Cortex-M3 core and APB peripheral blocks #0 and #2
5	BASE_SPIFI_CLK	150 MHz	Base clock for SPIFI
6	-	-	Reserved.
7	BASE_PHY_RX_CLK	75 MHz	Base clock for Ethernet PHY Rx
8	BASE_PHY_TX_CLK	75 MHz	Base clock for Ethernet PHY Tx
9	BASE_APB1_CLK	150 MHz	Base clock for APB peripheral block # 1
10	BASE_APB3_CLK	150 MHz	Base clock for APB peripheral block # 3
11	BASE_LCD_CLK	150 MHz	Base clock for LCD
12	-	-	Reserved

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Table 926. CGU0 base clocks *…continued*

Number	Name	Frequency [1]	Description
13	BASE_SDIO_CLK	150 MHz	Base clock for SDIO card reader
14	BASE_SSP0_CLK	150 MHz	Base clock for SSP0
15	BASE_SSP1_CLK	150 MHz	Base clock for SSP1
16	BASE_UART0_CLK	150 MHz	Base clock for UART0
17	BASE_UART1_CLK	150 MHz	Base clock for UART1
18	BASE_UART2_CLK	150 MHz	Base clock for UART2
19	BASE_UART3_CLK	150 MHz	Base clock for UART3
20	BASE_OUT_CLK	150 MHz	Base clock for CLKOUT pin

[1] Maximum frequency that guarantees stable operation of the LPC18xx.

Table 927 shows all available input clock sources for each clock generator.

Table 927. Clock sources for clock generators with selectable inputs

Clock sources	Clock generators						
	PLL0 (USB0)	PLL1	IDIVA /4	IDIVB /16	IDIVC /16	IDIVD /16	IDIVE /256
32 kHz oscillator	yes	yes	yes	yes	yes	yes	yes
IRC 12 MHz	yes	yes	yes	yes	yes	yes	yes
ENET_RX_CLK	yes	yes	yes	yes	yes	yes	yes
ENET_TX_CLK	yes	yes	yes	yes	yes	yes	yes
GP_CLKIN	yes	yes	yes	yes	yes	yes	yes
Crystal oscillator	yes	yes	yes	yes	yes	yes	yes
PLL0 (USB0)	no	yes	yes	no	no	no	no
PLL1	yes	no	yes	yes	yes	yes	yes
IDIVA	yes	yes	no	yes	yes	yes	yes
IDIVB	yes	yes	no	no	no	no	no
IDIVC	yes	yes	no	no	no	no	no
IDIVD	yes	yes	no	no	no	no	no
IDIVE	yes	yes	no	no	no	no	no

Table 928. Clock sources for output stages

Clock sources	Output stages (d = default clock source)																				
	BASE_SAFE_CLK	BASE_USB0_CLK	Reserved	BASE_USB1_CLK	BASE_M3_CLK	BASE_SPIFI_CLK	Reserved	BASE_PHY_RX_CLK	BASE_PHY_TX_CLK	BASE_APB1_CLK	BASE_APB3_CLK	BASE_LCD_CLK	Reserved	BASE_SDIO_CLK	BASE_SSP0_CLK	BASE_SSP1_CLK	BASE_UART0_CLK	BASE_UART1_CLK	BASE_UART2_CLK	BASE_UART3_CLK	BASE_OUT_CLK
32 kHz oscillator	no	no	-	yes	yes	yes	-	yes	yes	yes	yes	yes	-	yes	yes	yes	yes	yes	yes	yes	yes
IRC 12 MHz	d	no	-	d	d	d	-	d	d	d	d	d	-	d	d	d	d	d	d	d	d
ENET_RX_CLK	no	no	-	yes	yes	yes	-	yes	yes	yes	yes	yes	-	yes	yes	yes	yes	yes	yes	yes	yes

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Table 928. Clock sources for output stages

Clock sources	Output stages (d = default clock source)																				
	BASE_SAFE_CLK	BASE_USB0_CLK	Reserved	BASE_USB1_CLK	BASE_M3_CLK	BASE_SPIFI_CLK	Reserved	BASE_PHY_RX_CLK	BASE_PHY_TX_CLK	BASE_APB1_CLK	BASE_APB3_CLK	BASE_LCD_CLK	Reserved	BASE_SDIO_CLK	BASE_SSP0_CLK	BASE_SSP1_CLK	BASE_UART0_CLK	BASE_UART1_CLK	BASE_UART2_CLK	BASE_UART3_CLK	BASE_OUT_CLK
ENET_TX_CLK	no	no	-	yes	yes	yes	-	yes	yes	yes	yes	yes	-	yes	yes	yes	yes	yes	yes	yes	yes
GP_CLKIN	no	no	-	yes	yes	yes	-	yes	yes	yes	yes	yes	-	yes	yes	yes	yes	yes	yes	yes	yes
Crystal oscillator	no	no	-	yes	yes	yes	-	yes	yes	yes	yes	yes	-	yes	yes	yes	yes	yes	yes	yes	yes
PLL0 (USB0)	no	d	-	no	no	no	-	no	no	no	no	no	-	no	no	no	no	no	no	no	yes
PLL1	no	no	-	yes	yes	yes	-	yes	yes	yes	yes	yes	-	yes	yes	yes	yes	yes	yes	yes	yes
IDIVA	no	no	-	yes	yes	yes	-	yes	yes	yes	yes	yes	-	yes	yes	yes	yes	yes	yes	yes	yes
IDIVB	no	no	-	yes	yes	yes	-	yes	yes	yes	yes	yes	-	yes	yes	yes	yes	yes	yes	yes	yes
IDIVC	no	no	-	yes	yes	yes	-	yes	yes	yes	yes	yes	-	yes	yes	yes	yes	yes	yes	yes	yes
IDIVD	no	no	-	yes	yes	yes	-	yes	yes	yes	yes	yes	-	yes	yes	yes	yes	yes	yes	yes	yes
IDIVE	no	no	-	yes	yes	yes	-	yes	yes	yes	yes	yes	-	yes	yes	yes	yes	yes	yes	yes	yes

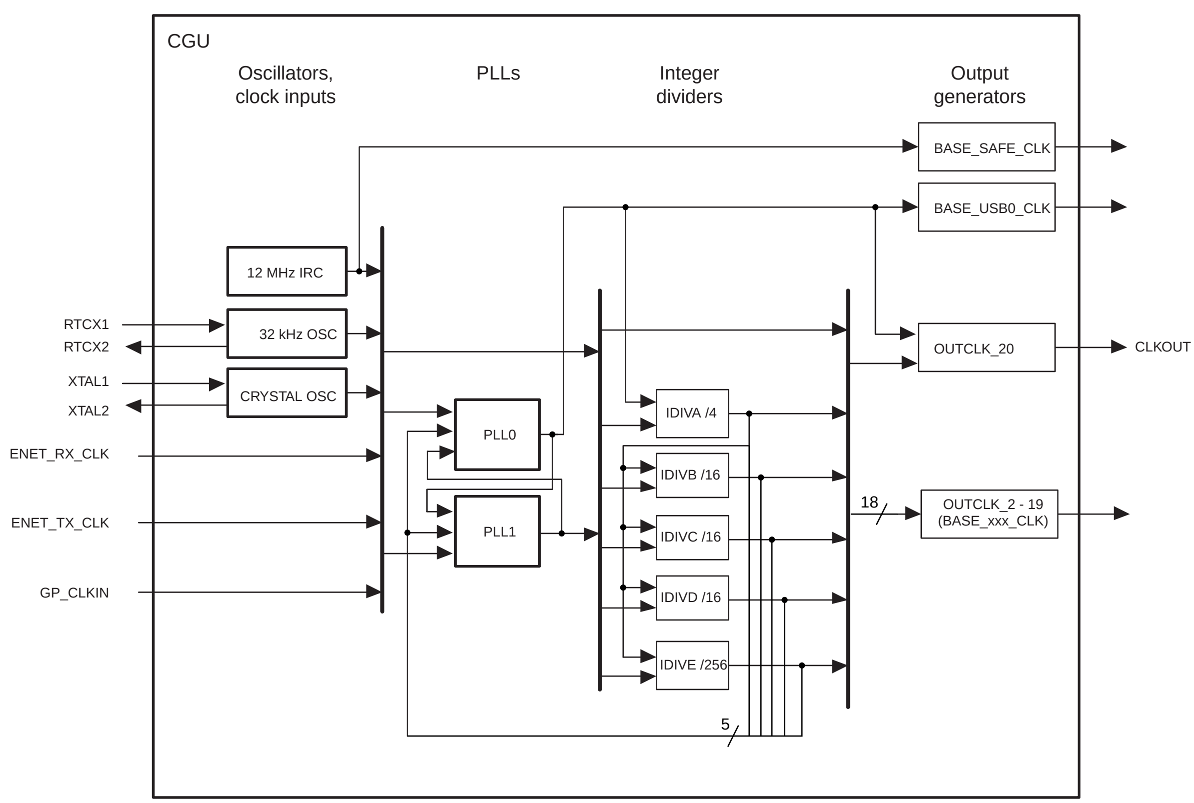


Fig 152. CGU block diagram

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42.4.5 Pin description

Table 929. CGU pin description

Pin name/ function name	Direction	Description
XTAL1	I	Crystal oscillator input
XTAL2	O	Crystal oscillator output
RTCX1	I	RTC 32 kHz oscillator input
RTCX2	O	RTC 32 kHz oscillator output
GP_CLKIN	I	General purpose input clock
ENET_TX_CLK	I	Ethernet PHY transmit clock
ENET_RX_CLK	I	Ethernet PHY receive clock
CLKOUT	O	Clock output pin

42.4.6 Register description

The register addresses of the CGU are shown in Table 930.

Remark: The CGU is configured by the boot loader at reset and when waking up from Deep power-down to produce a 72 MHz clock using PLL1. Note that this configuration is not reflected in the reset values given in Table 930.

Table 930. Register overview: CGU (base address 0x4005 0000)

Name	Access	Address offset	Description	Reset value
-	R	0x000	Reserved	0x0110 0106
-	R	0x004	Reserved	0x0000 0500
-	R	0x008	Reserved	0x1A00 0000
-	R	0x00C	Reserved	0x0000 0000
-	-	0x010	Reserved	-
FREQ_MON	R/W	0x014	Frequency monitor register	0x0000 0000
XTAL_OSC_CTRL	R/W	0x018	Crystal oscillator control register	0x0000 0005
PLL0_STAT	R	0x01C	PLL0 status register	0x0000 0000
PLL0_CTRL	R/W	0x020	PLL0 control register	0x0100 0003
PLL0_MDIV	R/W	0x024	PLL0 M-divider register	0x05F8 5B6A
PLL0_NP_DIV	R/W	0x028	PLL0 N/P-divider register	0x000B 1002
PLL1_STAT	R	0x02C	PLL1 status register	0x0000 0001
PLL1_CTRL	R/W	0x030	PLL1 control register	0x0100 0003
IDIVA_CTRL	R/W	0x034	Integer divider A control register	0x0100 0000
IDIVB_CTRL	R/W	0x038	Integer divider B control register	0x0100 0000
IDIVC_CTRL	R/W	0x03C	Integer divider C control register	0x0100 0000
IDIVD_CTRL	R/W	0x040	Integer divider D control register	0x0100 0000
IDIVE_CTRL	R/W	0x044	Integer divider E control register	0x0100 0000
OUTCLK_0_CTRL	R/W	0x048	Output stage 0 control register for base clock BASE_SAFE_CLK	0x0100 0800
OUTCLK_1_CTRL	R/W	0x04C	Output stage 1 control register for base clock BASE_USB0_CLK	0x0700 0000

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Table 930. Register overview: CGU (base address 0x4005 0000)

Name	Access	Address offset	Description	Reset value
-	-	0x050	Reserved	-
OUTCLK_3_CTRL	R/W	0x054	Output stage 3 control register for base clock BASE_USB1_CLK	0x0100 0000
OUTCLK_4_CTRL	R/W	0x058	Output stage 4 control register for base clock BASE_M3_CLK	0x0800 0800
OUTCLK_5_CTRL	R/W	0x05C	Output stage 5 control register for base clock BASE_SPIFI_CLK	0x0100 0000
-	-	0x060	Reserved	-
OUTCLK_7_CTRL	R/W	0x064	Output stage 7 control register for base clock BASE_PHY_RX_CLK	0x0100 0000
OUTCLK_8_CTRL	R/W	0x068	Output stage 8 control register for base clock BASE_PHY_TX_CLK	0x0100 0000
OUTCLK_9_CTRL	R/W	0x06C	Output stage 9 control register for base clock BASE_APB1_CLK	0x0100 0000
OUTCLK_10_CTRL	R/W	0x070	Output stage 10 control register for base clock BASE_APB3_CLK	0x0100 0000
OUTCLK_11_CTRL	R/W	0x074	Output stage 11 control register for base clock BASE_LCD_CLK	0x0100 0000
-	-	0x078	Reserved	-
OUTCLK_13_CTRL	R/W	0x07C	Output stage 13 control register for base clock BASE_SDIO_CLK	0x0100 0000
OUTCLK_14_CTRL	R/W	0x080	Output stage 14 control register for base clock BASE_SSP0_CLK	0x0100 0000
OUTCLK_15_CTRL	R/W	0x084	Output stage 15 control register for base clock BASE_SSP1_CLK	0x0100 0000
OUTCLK_16_CTRL	R/W	0x088	Output stage 16 control register for base clock BASE_UART0_CLK	0x0100 0000
OUTCLK_17_CTRL	R/W	0x08C	Output stage 17 control register for base clock BASE_UART1_CLK	0x0100 0000
OUTCLK_18_CTRL	R/W	0x090	Output stage 18 control register for base clock BASE_UART2_CLK	0x0100 0000
OUTCLK_19_CTRL	R/W	0x094	Output stage 19 control register for base clock BASE_UART3_CLK	0x0100 0000
OUTCLK_20_CTRL	R/W	0x098	Output stage 20 control register for base clock BASE_OUT_CLK	0x0100 0000
OUTCLK_21_CTRL to OUTCLK_25_CTRL	R/W	0x09C to 0x0AC	Reserved output stages	-

42.4.6.1 Frequency monitor register

The CGU can report the relative frequency of any operating clock. The clock to be measured must be selected by software, while the fixed-frequency IRC clock fref is used as the reference frequency. A 14-bit counter then counts the number of cycles of the measured clock that occur during a user-defined number of reference-clock cycles. When the MEAS bit is set, the measured-clock counter is reset to 0 and counts up, while the 9-bit reference-clock counter is loaded with the value in RCNT and then counts down

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towards 0. When either counter reaches its terminal value both counters are disabled and the MEAS bit is reset to 0. The current values of the counters can then be read out and the selected frequency obtained by the following equation:

$$fselected = \frac{Qselected}{(Qref[initial] - Qref[final])} \times fref$$

If RCNT is programmed to a value equal to the core clock frequency in kHz and reaches 0 before the FCNT counter saturates, the value stored in FCNT would then show the measured clock's frequency in kHz without the need for any further calculation.

Note that the accuracy of this measurement can be affected by several factors:

1. Quantization error is noticeable if the ratio between the two clocks is large (e.g. 100 kHz vs. 1 kHz), because one counter saturates while the other still has only a small count value.
2. Due to synchronization, the counters are not started and stopped at exactly the same time.
3. The measured frequency can only be to the same level of precision as the reference frequency.

Table 931. FREQ_MON register (FREQ_MON, address 0x4005 0014) bit description

Bit	Symbol	Value	Description	Reset value	Access
8:0	RCNT		9-bit reference clock-counter value	0	R/W
22:9	FCNT		14-bit selected clock-counter value	0	R
23	MEAS		Measure frequency	0	R/W
		0	RCNT and FCNT disabled		
		1	Frequency counters started		

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Table 931. FREQ_MON register (FREQ_MON, address 0x4005 0014) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
27:24	CLK_SEL		Clock-source selection for the clock to be measured.	0	R/W
		0x00	32 kHz oscillator (default)		
		0x01	IRC		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	Crystal oscillator		
		0x07	PLL0		
		0x08	PLL1		
		0x09	Reserved		
		0x0A	Reserved		
		0x0B	IDIVA		
		0x0C	IDIVB		
		0x0D	IDIVC		
		0x0E	IDIVD		
		0x0F	IDIVE		
31:28	-		Reserved	-	-

42.4.6.2 Crystal oscillator control register

The register XTAL_OSC_CONTROL contains the control bits for the crystal oscillator.

Table 932. XTAL_OSC_CTRL register (XTAL_OSC_CTRL, address 0x4005 0018) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	ENABLE		Oscillator pad enable[1]	1	R/W
		0	Enable		
		1	Power-down (default)		
1	BYPASS		Configure crystal operation or external-clock input pin XTAL1[1].	0	R/W
		0	Operation with crystal connected (default).		
		1	Bypass mode. Use this mode when an external clock source is used instead of a crystal.		
2	HF		Select frequency range. Between 15 MHz to 20 MHz, the value of this bit is don't care.	1	R/W
		0	Oscillator low-frequency mode (crystal or external clock source 1 to 20 MHz)		
		1	Oscillator high-frequency mode; crystal or external clock source 15 to 25 MHz (default)		
31:3	-		Reserved	-	R

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[1] Do not change the BYPASS and ENABLE bits in one write-action: this will result in unstable device operation!

42.4.6.3 PLL0 (for USB0) registers

The PLL0 provides a dedicated clock to the High-speed USB0 interface.

See Section 42.4.7.4.5 for instructions on how to set up the PLL0.

42.4.6.3.1 PLL0 status register

Table 933. PLL0_STAT register (PLL0_STAT, address 0x4005 001C) bit description

Bit	Symbol	Description	Reset value	Access
0	LOCK	PLL0 lock indicator	0	R
1	FR	PLL0 free running indicator	0	R
31:2	-	Reserved		-

42.4.6.3.2 PLL0 control register

Table 934. PLL0_CTRL register (PLL0_CTRL, address 0x4005 0020) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		PLL0 power down	1	R/W
		0	PLL0 enabled		
		1	PLL0 powered down		
1	BYPASS		Input clock bypass control	1	R/W
		0	CCO clock sent to post-dividers. Use this in normal operation.		
		1	PLL0 input clock sent to post-dividers (default).		
2	DIRECTI		PLL0 direct input	0	R/W
3	DIRECTO		PLL0 direct output	0	R/W
4	CLKEN		PLL0 clock enable	0	R/W
5	-		Reserved	-	-
6	FRM		Free running mode	0	R/W
7	-		Reserved	0	R/W
8	-		Reserved. Reads as zero. Do not write one to this register.	0	R/W
9	-		Reserved. Reads as zero. Do not write one to this register.	0	R/W
10	-		Reserved. Reads as zero. Do not write one to this register.	0	R/W
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-

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Table 934. PLL0_CTRL register (PLL0_CTRL, address 0x4005 0020) bit description
…continued

Bit	Symbol	Value	Description	Reset value	Access
27:24	CLK_SEL		Clock-source selection	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	Crystal oscillator		
		0x07	Reserved		
		0x08	PLL1		
		0x09	Reserved		
		0x0A	Reserved		
		0x0B	IDIVA		
		0x0C	IDIVB		
		0x0D	IDIVC		
		0x0E	IDIVD		
		0x0F	IDIVE		
31:28	-		Reserved	-	-

42.4.6.3.3 PLL0 M-divider register

Table 935. PLL0_MDIV register (PLL0_MDIV, address 0x4005 0024) bit description

Bit	Symbol	Description	Reset value	Access
16:0	MDEC	Decoded M-divider coefficient value. Select values for the M-divider between 1 and 131071.	0x5B6A	R/W
21:17	SELP	Bandwidth select P value	11100	R/W
27:22	SELI	Bandwidth select I value	010111	R/W
31:28	SELR	Bandwidth select R value	0000	R/W

42.4.6.3.4 PLL0 NP-divider register

Table 936. PLL0_NPDIV register (PLL0_NP_DIV, address 0x4005 0028) bit description

Bit	Symbol	Description	Reset value	Access
6:0	PDEC	Decoded P-divider coefficient value	000 0010	R/W
11:7	-	Reserved	-	-
21:12	NDEC	Decoded N-divider coefficient value	1011 0001	R/W
31:22	-	Reserved	-	-

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42.4.6.4 PLL1 registers

The PLL1 is used for the core and all peripheral blocks.

42.4.6.4.1 PLL1 status register

Table 937. PLL1_STAT register (PLL1_STAT, address 0x4005 002C) bit description

Bit	Symbol	Description	Reset value	Access
0	LOCK	PLL1 lock indicator	1	R
31:1	-	Reserved	-	-

42.4.6.4.2 PLL1 control register

Table 938. PLL1_CTRL register (PLL1_CTRL, address 0x4005 0030) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		PLL1 power down	1	R/W
		0	PLL1 enabled		
		1	PLL1 powered down		
1	BYPASS		Input clock bypass control	1	R/W
		0	CCO clock sent to post-dividers. Use for normal operation.		
		1	PLL1 input clock sent to post-dividers (default).		
2	-		Reserved. Do not write one to this bit.	0	R/W
5:3	-		Reserved. Do not write one to these bits.	-	-
6	FBSEL		PLL feedback select (see Figure 155 “PLL1 block diagram”).	0	R/W
		0	CCO output is used as feedback divider input clock.		
		1	PLL output clock (clkout) is used as feedback divider input clock. Use for normal operation.		
7	DIRECT		PLL direct CCO output	0	R/W
		0	Disabled		
		1	Enabled		
9:8	PSEL[1:0]		Post-divider division ratio. The value applied is 2xP.	01	R/W
		0x0	1		
		0x1	2 (default)		
		0x2	4		
		0x3	8		
10	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		

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Table 938. PLL1_CTRL register (PLL1_CTRL, address 0x4005 0030) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
13:12	NSEL[1:0]		Pre-divider division ratio	10	R/W
		0x0	1		
		0x1	2		
		0x2	3 (default)		
		0x3	4		
15:14	-		Reserved	-	-
23:16	MSEL[7:0]		Feedback-divider division ratio (M) 00000000 = 1 00000001 = 2 ... 11111111 = 256	11000	R/W
27:24	CLK_SEL		Clock-source selection.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	Crystal oscillator		
		0x07	PLL0		
		0x08	Reserved		
		0x09	Reserved		
		0x0A	Reserved		
		0x0B	IDIVA		
		0x0C	IDIVB		
		0x0D	IDIVC		
		0x0E	IDIVD		
		0x0F	IDIVE		
31:28	-		Reserved	-	-

42.4.6.5 Integer divider register A

Table 939. IDIVA control register (IDIVA_CTRL, address 0x4005 0034) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Integer divider A power down	0	R/W
		0	IDIVA enabled (default)		
		1	power-down		
1	-		Reserved	-	-

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Table 939. IDIVA control register (IDIVA_CTRL, address 0x4005 0034) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
3:2	IDIV[1:0]		Integer divider A divider values (1/(IDIV + 1))	00	R/W
		0x0	1 (default)		
		0x1	2		
		0x2	3		
		0x3	4		
10:4	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-
27:24	CLK_SEL		Clock-source selection.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	Crystal oscillator		
		0x07	PLL0		
		0x08	PLL1		
31:28	-		Reserved	-	-

42.4.6.6 Integer divider register B, C, D

Table 940. IDIVB/C/D control registers (IDIVB_CTRL, address 0x4005 0038; IDIVC_CTRL, address 0x4005 003C; IDIVC_CTRL, address 0x4005 0040) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Integer divider power down	0	R/W
		0	IDIV enabled (default)		
		1	power-down		
1	-		Reserved	-	-
5:2	IDIV[3:0]		Integer divider B, C, D divider values (1/(IDIV + 1)) 0000 = 1 (default) 0001 = 2 ... 1111 = 16	0000	R/W
10:6	-		Reserved	-	-

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Table 940. IDIVB/C/D control registers (IDIVB_CTRL, address 0x4005 0038; IDIVC_CTRL, address 0x4005 003C; IDIVC_CTRL, address 0x4005 0040) bit description

Bit	Symbol	Value	Description	Reset value	Access
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-
27:24	CLK_SEL		Clock-source selection.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	Crystal oscillator		
		0x07	Reserved		
		0x08	PLL1		
		0x09	Reserved		
		0x0A	Reserved		
		0x0B	IDIVA		
31:28	-		Reserved	-	-

42.4.6.7 Integer divider register E

Table 941. IDIVE control register (IDIVE_CTRL, address 0x4005 0044) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Integer divider power down	0	R/W
		0	IDIV enabled (default)		
		1	power-down		
1	-		Reserved	-	-
9:2	IDIV[7:0]		Integer divider E divider values (1/(IDIV + 1)) 00000000 = 1 (default) 00000001 = 2 ... 111111111 = 256	00000000	R/W
10	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-

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Table 941. IDIVE control register (IDIVE_CTRL, address 0x4005 0044) bit description

Bit	Symbol	Value	Description	Reset value	Access
27:24	CLK_SEL		Clock-source selection.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	Crystal oscillator		
		0x07	Reserved		
		0x08	PLL1		
		0x09	Reserved		
		0x0A	Reserved		
		0x0B	IDIVA		
31:28	-		Reserved	-	-

42.4.6.8 Output stage 0 control register

This register controls the BASE_SAFE_CLK to the watchdog oscillator. The only possible clock source for this base clock is the IRC.

Table 942. Output stage 0 control register (OUTCLK_0_CTRL, address 0x4005 0048) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Output stage power down	0	R/W
		0	Output stage enabled (default)		
		1	power-down		
10:1	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-
27:24	CLK_SEL		Clock-source selection.	0x01	R/W
		0x00	Reserved		
		0x01	IRC (default)		
31:28	-		Reserved	-	-

42.4.6.9 Output stage 1 control register

This register controls the BASE_USB0_CLK to the High-speed USB0. The only possible clock source for this base clock is the PLL0 output.

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Table 943. Output stage 1 control register (OUTCLK_1_CTRL, address 0x4005 004C) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Output stage power down	0	R/W
		0	Output stage enabled (default)		
		1	power-down		
10:1	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-
27:24	CLK_SEL		Clock-source selection.	0x07	R/W
		0x00	Reserved		
		0x07	PLL0 (default)		
31:28	-		Reserved	-	-

42.4.6.10 Output stage 3 to 19 control registers

These registers control base clocks 2 to 19.

Table 944. Output stage 3 to 19 control registers (OUTCLK_2_CTRL to OUTCLK_19_CTRL, address 0x4005 0050 to 0x4005 0094) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Output stage power down	0	R/W
		0	Output stage enabled (default)		
		1	power-down		
10:1	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-

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Table 944. Output stage 3 to 19 control registers (OUTCLK_2_CTRL to OUTCLK_19_CTRL, address 0x4005 0050 to 0x4005 0094) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
27:24	CLK_SEL		Clock-source selection.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	Crystal oscillator		
		0x07	Reserved		
		0x08	PLL1		
		0x09	Reserved		
		0x0A	Reserved		
		0x0B	IDIVA		
		0x0C	IDIVB		
		0x0D	IDIVC		
		0x0E	IDIVD		
		0x0F	IDIVE		
31:28	-		Reserved	-	-

42.4.6.11 Output stage 20 register

This register controls the clock output to the CLKOUT pin. All clock generator outputs can be monitored through this pin.

Table 945. Output stage 20 control register (OUTCLK_20_CTRL, addresses 0x4005 0098) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Output stage power down	0	R/W
		0	Output stage enabled (default)		
		1	power-down		
10:1	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-

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Table 945. Output stage 20 control register (OUTCLK_20_CTRL, addresses 0x4005 0098) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
27:24	CLK_SEL		Clock-source selection.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	Crystal oscillator		
		0x07	PLL0		
		0x08	PLL1		
		0x09	Reserved		
		0x0A	Reserved		
		0x0B	IDIVA		
		0x0C	IDIVB		
		0x0D	IDIVC		
		0x0E	IDIVD		
		0x0F	IDIVE		
31:28	-		Reserved	-	-

42.4.7 Functional description

42.4.7.1 32 kHz oscillator

The 32 kHz oscillator output is controlled by the CREG block (see Table 31). The RTC and the Alarm timer are connected directly to the 32 kHz oscillator.

42.4.7.2 IRC

The IRC is a trimmed 12 MHz internal oscillator. Although it's part of the CGU, the CGU has no control over this clock source. The IRC is put into power down depending on the power saving mode.

42.4.7.3 Crystal oscillator

The crystal oscillator is controlled by the XTAL_OSC_CTRL register in the CGU (see Table 932).

The crystal oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL.

The oscillator can operate in one of two modes: slave mode and oscillation mode.

- In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (C_C in Figure 153, drawing a), with an amplitude of at least 200 mVrms. The XTAL2 pin in this configuration can be left unconnected.

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- External components and models used in oscillation mode are shown in Figure 153, drawings b and c, and in Table 946 and Table 947. Since the feedback resistance is integrated on chip, only a crystal and the capacitances CX1 and CX2 need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, CL and RS). Capacitance C_P in Figure 153, drawing c, represents the parallel package capacitance and should not be larger than 7 pF. Parameters FC, CL, RS and CP are supplied by the crystal manufacturer.

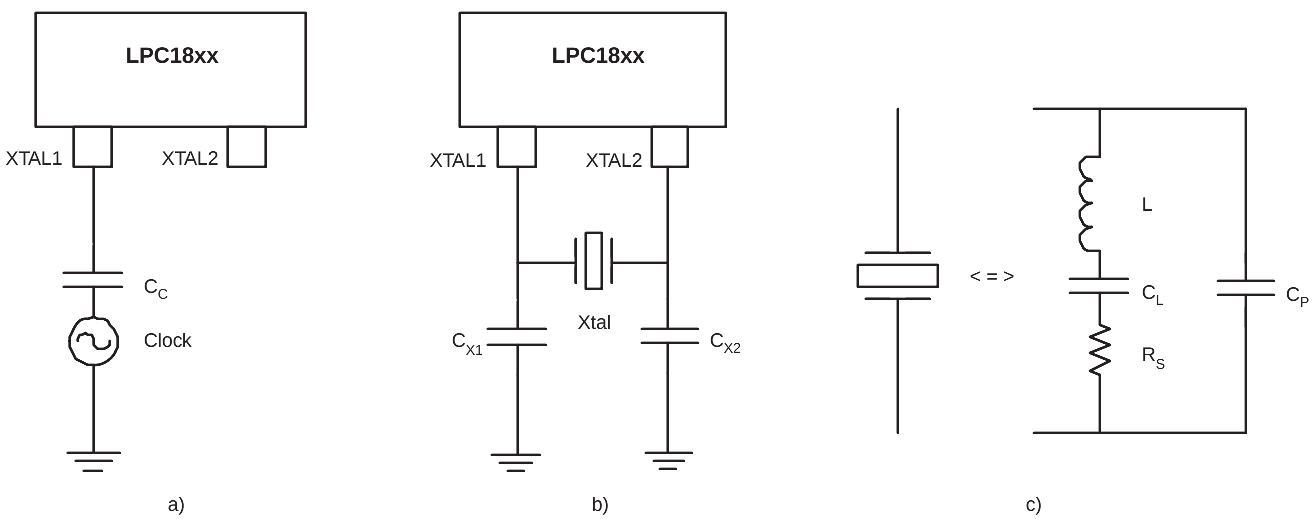


Fig 153. Oscillator modes and models: a) slave mode of operation, b) oscillation mode of operation, c) external crystal model used for $C_{X1}/_{X2}$ evaluation

Table 946. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
2 MHz	< 200 Ω	33 pF, 33 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
4 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
8 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF
12 MHz	< 160 Ω	18 pF, 18 pF
	< 160 Ω	39 pF, 39 pF
16 MHz	< 120 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF
20 MHz	<100 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF

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Table 947. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{x2}
15 MHz	< 80 Ω	18 pF, 18 pF
20 MHz	< 80 Ω	39 pF, 39 pF
	< 100 Ω	47 pF, 47 pF

42.4.7.4 PLL0 (for USB0)

42.4.7.4.1 Features

- Input frequency: 14 kHz to 150 MHz. The input from an external crystal is limited to 25 MHz.
- CCO frequency: 275 MHz to 550 MHz.
- Output clock range: 4.3 MHz to 550 MHz.
- Programmable dividers:
  - Pre-divider N (N, 1 to 2^8)
  - Feedback-divider 2 x M (M, 1 to 2^{15})
  - Post-divider P x 2 (P, 1 to 2^5).
- Programmable bandwidth (integrating action, proportional action, high frequency pole).
- On-the-fly adjustment of the clock possible (dividers with handshake control).
- Positive edge clocking.
- Frequency limiter to avoid hang-up of the PLL.
- Lock detector.
- Power-down mode.
- Free running mode

42.4.7.4.2 PLL0 description

The block diagram of the PLL is shown in Figure 154. The clock input has to be fed to pin clkin. Pin clkout is the PLL clock output. The analog part of the PLL consists of a Phase Frequency Detector (PFD), filter and a Current Controlled Oscillator (CCO). The PFD has two inputs, a reference input from the (divided) external clock and one input from the divided CCO output clock. The PFD compares the phase/frequency of these input signals and generates a control signal if they don’t match. This control signal is fed to a filter which drives the CCO.

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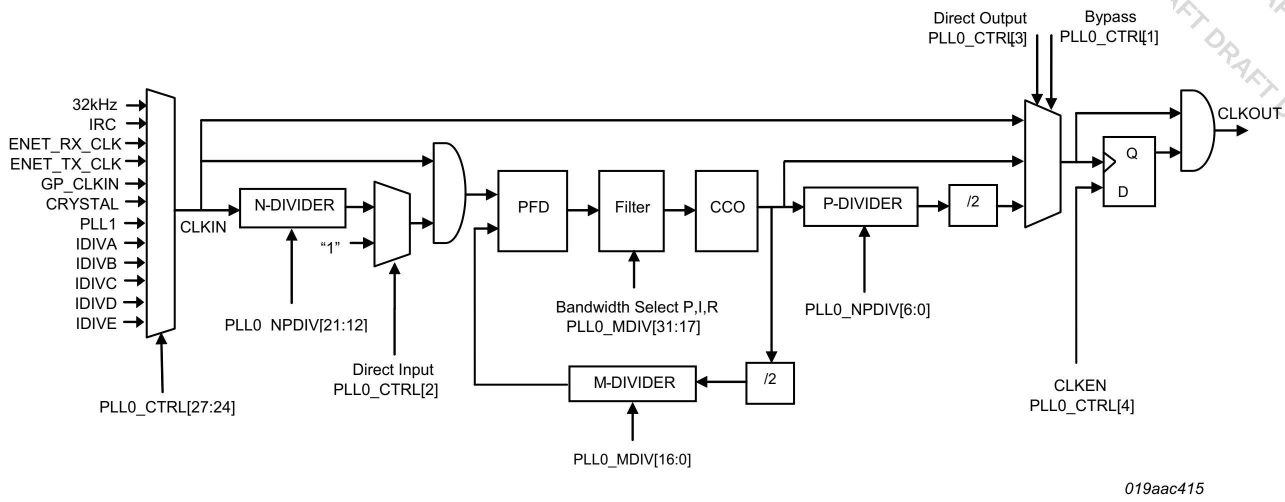


Fig 154. PLL0 block diagram

The PLL contains three programmable dividers: pre-divider (N), feedback-divider (M) and post-divider (P). The PLL contains a lock detector which measures the phase difference between the rising edges of the input and feedback clocks. Only when this difference is smaller than the so called "lock criterion" for more than seven consecutive input clock periods, the lock output switches from low to high. A single too large phase difference immediately resets the counter and causes the lock signal to drop (if it was high). Requiring seven phase measurements in a row to be below a certain figure ensures that the lock detector will not indicate lock until both the phase and frequency of the input and feedback clocks are very well aligned. This effectively prevents false lock indications, and thus ensures a glitch free lock signal.

To avoid frequency hang-up the PLL contains a frequency limiter. This feature is built in to prevent the CCO from running too fast, this can occur if e.g. a wrong feedback-divider (M) ratio is applied to the PLL.

42.4.7.4.3 Use of PLL0 operating modes

Table 948. PLL operating modes

	PLL0_Mode bit settings:					
Mode	**PD**	**CLKEN**	**BYPASS**	**DIRECTI**	**DIRECTO**	**FRM**
1: Normal	0	1	0	1/0	1/0	0
3: Power Down	1	x	x	x	x	x

Normal Mode: Mode 1 is the normal operating mode.

The pre- and post-divider can be selected to give:

- mode 1a: Normal operating mode without post-divider and without pre-divider
- mode 1b: Normal operating mode with post-divider and without pre-divider
- mode 1c: Normal operating mode without post-divider and with pre-divider
- mode 1d: Normal operating mode with post-divider and with pre-divider

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To get at the output of the PLL (clkout) the best phase-noise and jitter performance, the highest possible reference clock (clkref) at the PFD has to be used. Therefore mode 1a and 1b are recommended, when it is possible to make the right output frequency without pre-divider.

By using the post-divider the clock at the output of the PLL (clkout) the divider ratio is always even because the divide-by-2 divider after the post-divider.

Table 949. DIRECTL and DIRECTO bit settings in HP0/1_Mode register

Mode	DIRECTI	DIRECTO
1a	1	1
1b	1	0
1c	0	1
1d	0	0

Mode 1a: Normal operating mode without post-divider and without pre-divider: In normal operating mode 1a the post-divider and pre-divider are bypassed. The operating frequencies are:

Fout = Fcco = 2 x M x Fin Λ (275 MHz $\leq$Fcco $\leq$550 MHz, 4 kHz $\leq$ Fin $\leq$150 MHz)

The feedback divider ratio is programmable:

- Feedback-divider M (M, 1 to 2^{15})

Mode 1b: Normal operating mode with post-divider and without pre-divider: In normal operating mode 1b the pre-divider is bypassed. The operating frequencies are:

Fout = Fcco /(2 x P) = (M / P) x Fin Λ (275 MHz $\leq$Fcco $\leq$550 MHz, 4 kHz $\leq$Fin $\leq$ 150 MHz)

The divider ratios are programmable:

- Feedback-divider M (M, 1 to 2^{15})
- Post-divider P (P, 1 to 32)

Mode 1c: Normal operating mode without post-divider and with pre-divider: In normal operating mode 1c the post-divider with divide-by-2 divider is bypassed. The operating frequencies are:

Fout = Fcco = 2 x M x Fin / N Λ (275 MHz $\leq$Fcco $\leq$550 MHz, 4 kHz $\leq$Fin/N $\leq$150 MHz)

The divider ratios are programmable:

- Pre-divider N (N, 1 to 256)
- Feedback-divider M (M, 1 to 2^{15})

Mode 1d: Normal operating mode with post-divider and with pre-divider: In normal operating mode 1d none of the dividers are bypassed. The operating frequencies are:

Fout = Fcco /(2 x P) = M x Fin /(N x P) Λ (275 MHz $\leq$Fcco $\leq$550 MHz, 4 kHz $\leq$Fin/N $\leq$150 MHz)

The divider ratios are programmable:

- Pre-divider N (N, 1 to 256)

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- Feedback-divider M (M, 1 to 2^{15})
- Post-divider P (P, 1 to 32)

Mode 3: Power down mode (pd): In this mode (pd = '1'), the oscillator will be stopped, the lock output will be made low, and the internal current reference will be turned off. During pd it is also possible to load new divider ratios at the input buses (msel, psel, nsel). Power-down mode is ended by making pd low, causing the PLL to start up. The lock signal will be made high once the PLL has regained lock on the input clock.

42.4.7.4.4 Settings for USB0

Table 950 shows the divider settings used for configuring a certain output frequency F_{out} for USB0.

Table 950. System PLL divider ratio settings for 12 MHz

Fout (MHz)	FCCo (MHz)	Ndec	Mdec	Pdec	SELR	SELI	SELP
<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>

42.4.7.4.5 Usage notes

In order to set up the PLL0, follow these steps:

1. Power down the PLL0 by setting bit 1 in the PLL0_CTRL register to 1. This step is only needed if the PLL0 is currently enabled.
2. Configure the PLL0 m, n, and p divider values in the PLL0_M and PLL0_NP registers.
3. Power up the PLL0 by setting bit 1 in the PLL0_CTRL register to 0.
4. Wait for the PLL0 to lock by monitoring the LOCK bit in the PLL0_STAT register.
5. Enable the PLL0 clock output in the PLL0_CTRL register.

42.4.7.5 PLL1

42.4.7.5.1 Features

- 1 MHz to 50 MHz input frequency. The input from an external crystal is limited to 25 MHz.
- 9.75 MHz to 320 MHz selectable output frequency with 50% duty cycle.
- 156 MHz to 320 MHz Current Controlled Oscillator (CCO) frequency.
- Power-down mode.
- Lock detector.

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42.4.7.5.2 PLL1 description

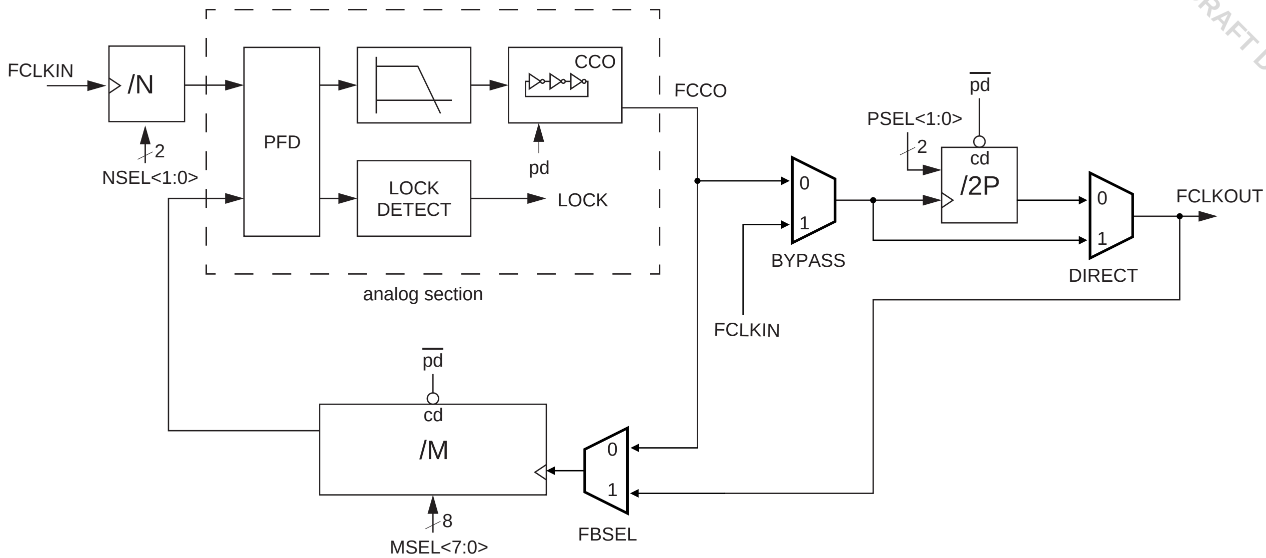


Fig 155. PLL1 block diagram

The block diagram of this PLL is shown in Figure 155. The input frequency range is 10 MHz to 25 MHz. The input clock is fed directly to the Phase-Frequency Detector (PFD). This block compares the phase and frequency of its inputs, and generates a control signal when phase and/ or frequency do not match. The loop filter filters these control signals and drives the current controlled oscillator (CCO), which generates the main clock. The CCO frequency range is 156 MHz to 320 MHz.These clocks are either divided by 2xP by the programmable post divider to create the output clock(s), or are sent directly to the output(s). The main output clock is then divided by M by the programmable feedback divider to generate the feedback clock. The output signal of the phase-frequency detector is also monitored by the lock detector, to signal when the PLL has locked on to the input clock.

Lock detector: The lock detector measures the phase difference between the rising edges of the input and feedback clocks. Only when this difference is smaller than the so called “lock criterion” for more than eight consecutive input clock periods, the lock output switches from low to high. A single too large phase difference immediately resets the counter and causes the lock signal to drop (if it was high). Requiring eight phase measurements in a row to be below a certain figure ensures that the lock detector will not indicate lock until both the phase and frequency of the input and feedback clocks are very well aligned. This effectively prevents false lock indications, and thus ensures a glitch free lock signal.

Power-down control: To reduce the power consumption when the PLL clock is not needed, a Power-down mode has been incorporated. In this mode, the internal current reference will be turned off, the oscillator and the phase-frequency detector will be stopped and the dividers will enter a reset state. While in Power-down mode, the lock output will be low to indicate that the PLL is not in lock. When the Power-down mode is terminated, the PLL will resume its normal operation and will make the lock signal high once it has regained lock on the input clock.

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Selectable feedback divider clock: To allow a trade-off to be made between functionality and power consumption, the feedback divider can be connected to either the CCO clock by setting FBSEL to 0 or to the output clock by setting FBSEL to 1. If the post-divider is used to divide down the CCO clock the current consumption of the feedback divider can be reduced by making it run on the lower output clock instead of the CCO clock, but doing so will limit the relation between output and phase detector clock frequencies to integer values.

Direct output mode: In normal operating mode (with DIRECT set to 0) the CCO clock is divided by 2, 4, 8 or 16 depending on the value of PSEL[1:0], automatically giving an output clock with a 50% duty cycle. If a higher output frequency is needed, the CCO clock can be sent directly to the output by setting DIRECT to 1. Since the CCO was designed to directly generate a clock with a 50% duty cycle, the output clock duty cycle will also be 50% in direct mode.

Divider ratio programming: Pre-divider

The pre-divider's division ratio is controlled by the NSEL[1:0] input. The division ratio between PLL's input clock and the phase detector clock is the decimal value on NSEL[1:0] plus one.

Post-divider

The division ratio of the post divider is controlled by the PSEL bits. The division ratio is two times the value of P selected by PSEL bits. This guarantees an output clock with a 50% duty cycle.

Feedback divider

The feedback divider's division ratio is controlled by the MSEL bits. The division ratio between the PLL's output clock and the input clock is the decimal value on MSEL bits plus one.

Changing the divider values

Changing the divider ratio while the PLL is running is not recommended. As there is no way to synchronize the change of the NSEL, MSEL, and PSEL values with the dividers, the risk exists that the counter will read in an undefined value, which could lead to unwanted spikes or drops in the frequency of the output clock. The recommended way of changing between divider settings is to power down the PLL, adjust the divider settings and then let the PLL start up again.

Frequency selection: The PLL frequency equations use the following parameters (also see Figure 155):

Integer mode

In this mode the post divider is enabled and the feedback divider is set to run on the PLL output clock, giving the following frequency relations:

(11)

$$FCLKOUT = M \times \frac{FCLKIN}{N}$$

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(12)

$$FCCO = 2 \times P \times FCLKOUT = 2 \times P \times M \times \frac{FCLKIN}{N}$$

Non-integer mode

In this mode the post-divider is enabled and the feedback divider is set to run directly on the CCO clock, which gives the following frequency dividers:

(13)

$$FCLKOUT = \frac{FCCO}{2 \times P} = \frac{M}{2 \times P} \times \frac{FCLKIN}{N}$$

(14)

$$FCCO = M \times \frac{FCLKIN}{N}$$

Direct mode

In this mode, the post-divider is disabled and the CCO clock is sent directly to the output, leading to the following frequency equation:

(15)

$$FCLKOUT = FCCO = M \times \frac{FCLKIN}{N}$$

Power-down mode

In this mode, the internal current reference will be turned off, the oscillator and the phase-frequency detector will be stopped and the dividers will enter a reset state. While in Power-down mode, the lock output will be low, to indicate that the PLL is not in lock. When the Power-down mode is terminated, the PLL will resume its normal operation and will make the lock signal high once it has regained lock on the input clock.

42.4.8 Example CGU configurations

42.4.8.1 Programming the CGU for Deep-sleep and Power-down modes

Before the LPC18xx enters Deep-sleep or Power-down mode, the IRC must be programmed as the clock source in the control registers for all output stages (OUTCLK_0 to OUTCLK_20). In addition, the PLLs must be in Power-down mode.

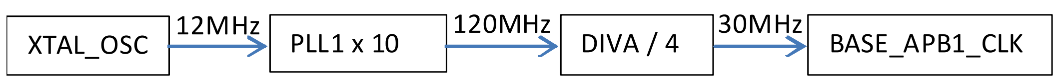
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When the LPC18xx wakes up from Deep-sleep or Power-down mode, the IRC is used as the clock soures for all output stages. Also see Section 8.2.3 and Section 8.2.4.

42.4.8.2 Programming the CGU for using I2S at peripheral clock rate of 30 MHz

In this example the peripheral clock of the I2S interface is set to 30 MHz. The peripheral I2S clock is a branch of the BASE_APB1_CLK. Using a crystal of 12 MHz as clock source, a PLL1 multiplier of 10, and an integer divider of 4 provide the desired clock rate.



For this example, program the CGU as follows:

1. Enable the crystal oscillator in the XTAL_OSC_CTRL register (Table 932).
2. Wait for the crystal to stabilize.
3. Select the crystal oscillator as input to the PLL1 and set up the divider in the PLL1_CTRL register (see Table 938):
   - Set bits CLK_SEL in the PLL1_CTRL register to 0x6.
   - Set MSEL = 9.
   - Set NSEL = 0.
   - Set PSEL = 1.
   - Set FBSEL = 1.
   - Set BYPASS = 0, DIRECT = 0.
4. Wait for the PLL1 to lock.
5. Select the PLL1 as clock source of the integer divider A (IDIVA) in the IDIVA register and set AUTOBLOCK = 1 (see Table 939).
6. Select IDIVA as clock source of the base clock BASE_APB1_CLK and set AUTOBLOCK = 1 (see Table 943).
7. Ensure that the I2S branch clock CLK_APB1_I2S is enabled in the CCU (see Table 152).

42.5 LPC1850/30/20/10 Rev '-' CCU

42.5.1 How to read this chapter

Remark: This chapter applies to parts LPC1850_30_20_10 Rev '-'.

Ethernet, USB0, USB1, and LCD related clocks are not available on all packages. The SDIO interface is not available. See <tbd>. The corresponding clock control registers and register bits are reserved.

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42.5.2 Basic configuration

The CCU1/2 are configured as follows:

- See Table 951 for clocking and power control.
- Do not reset the CCUs during normal operation.

Table 951. CCU clocking and power control

	Base clock	Branch clock	Maximum frequency
CCU1	BASE_M3_CLK	CLK_M3_BUS	150 MHz
CCU2	BASE_M3_CLK	CLK_M3_BUS	150 MHz

42.5.3 Features

The CCUs switch the clocks to individual peripherals on or off.

- Auto mode activates the AHB disable protocol before switching off the branch clock.
- Wake-up mode allows to select clocks to run automatically after a wake-up event.

42.5.4 General description

Each CGU base clock has several clock branches which can be turned on or off independently by the Clock Control Units CCU1 or CCU2. The branch clocks are distributed between CCU1 and CCU2.

Table 952. CCU1 branch clocks

Base clock	Branch clock	Description
BASE_APB3_CLK	CLK_APB3_BUS	
	CLK_APB3_I2C1	Clock to the I2C1 register interface and I2C1 peripheral clock.
	CLK_APB3_DAC	Clock to the DAC register interface.
	CLK_APB3_ADC0	Clock to the ADC0 register interface and ADC0 peripheral clock.
	CLK_APB3_ADC1	Clock to the ADC1 register interface and ADC1 peripheral clock.
	CLK_APB3_CAN	Clock to the C_CAN register interface and C_CAN peripheral clock.
BASE_APB1_CLK	CLK_APB1_BUS	
	CLK_APB1_MOTOCON	Clock to the PWM Motor control block and PWM Motocon peripheral clock.
	CLK_APB1_I2C0	Clock to the I2C0 register interface and I2C0 peripheral clock.
	CLK_APB1_I2S	Clock to the I2S register interface and I2S peripheral clock.
BASE_SPIFI_CLK	CLK_SPIFI	clock for the SPIFI SCKI clock input.

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Table 952. CCU1 branch clocks

Base clock	Branch clock	Description
BASE_M3_CLK	CLK_M3_BUS	
	CLK_M3_SPIFI	Clock to the SPIFI register interface.
	CLK_M3_GPIO	Clock to the GPIO register interface
	CLK_M3_LCD	Clock to the LCD register interface.
	CLK_M3_ETHERNET	Clock to the Ethernet register interface.
	CLK_M3_USB0	Clock to the USB0 register interface.
	CLK_M3_EMC	Clock to the External memory controller register interface.
	CLK_M3_SDIO	Clock to the SDIO register interface.
	CLK_M3_DMA	Clock to the DMA register interface.
	CLK_M3_M3CORE	Clock to the Cortex-M3 core
	CLK_M3_AES	Clock to the AES register interface.
	CLK_M3_SCT	Clock to the SCT register interface.
	CLK_M3_USB1	Clock to the USB1 register interface.
	CLK_M3_WWDT	Clock to the WWDT register interface.
	CLK_M3_UART0	Clock to the USART0 register interface.
	CLK_M3_UART1	Clock to the UART1 register interface.
	CLK_M3_SSP0	Clock to the SSP0 register interface.
	CLK_M3_TIMER0	Clock to the timer0 register interface and timer0 peripheral clock.
	CLK_M3_TIMER1	Clock to the timer1 register interface and timer1 peripheral clock.
	CLK_M3_SCU	Clock to the System control unit register interface.
	CLK_M3_CREG	Clock to the CREG register interface.
	CLK_M3_RITIMER	Clock to the RI timer register interface and RI timer peripheral clock.
	CLK_M3_UART2	Clock to the UART2 register interface.
	CLK_M3_UART3	Clock to the UART3 register interface.
	CLK_M3_TIMER2	Clock to the timer2 register interface and timer2 peripheral clock.
	CLK_M3_TIMER3	Clock to the timer3 register interface and timer3 peripheral clock.
BASE_M3_CLK	CLK_M3_SSP1	
	CLK_M3_QEI	Clock to the QEI register interface and QEI peripheral clock.
BASE_USB0_CLK	CLK_USB0	USB0 peripheral clock.
BASE_USB1_CLK	CLK_USB1	USB1 peripheral clock.
-	-	Reserved.

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Table 953. CCU2 branch clocks

Base clock	Branch clock	Description
BASE_UART3_CLK	CLK_APB2_UART3	USART3 peripheral clock.
BASE_UART2_CLK	CLK_APB2_UART2	USART2 peripheral clock.
BASE_UART1_CLK	CLK_APB0_UART1	UART1 peripheral clock.
BASE_UART0_CLK	CLK_APB0_UART0	USART0 peripheral clock.
BASE_SSP1_CLK	CLK_APB2_SSP1	SSP1 peripheral clock.
BASE_SSP0_CLK	CLK_APB0_SSP0	SSP0 peripheral clock.
BASE_SDIO_CLK	CLK_SDIO	Not used.

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42.5.5 Register description

Table 954. Register overview: CCU1 (base address 0x4005 1000)

Name	Access	Address offset	Description	Reset value
PM	R/W	0x000	CCU1 power mode register	0x0000 0000
BASE_STAT	R	0x004	CCU1 base clocks status register	0x0000 0FFF
-	-	0x008 to 0x0FC	Reserved	-
CLK_APB3_BUS_CFG	R/W	0x100	CLK_APB3_BUS clock configuration register	0x0000 0001
CLK_APB3_BUS_STAT	R	0x104	CLK_APB3_BUS clock status register	0x0000 0001
CLK_APB3_I2C1_CFG	R/W	0x108	CLK_APB3_I2C1 configuration register	0x0000 0001
CLK_APB3_I2C1_STAT	R	0x10C	CLK_APB3_I2C1v status register	0x0000 0001
CLK_APB3_DAC_CFG	R/W	0x110	CLK_APB3_DAC configuration register	0x0000 0001
CLK_APB3_DAC_STAT	R	0x114	CLK_APB3_DAC status register	0x0000 0001
CLK_APB3_ADC0_CFG	R/W	0x118	CLK_APB3_ADC0 configuration register	0x0000 0001
CLK_APB3_ADC0_STAT	R	0x11C	CLK_APB3_ADC0 status register	0x0000 0001
CLK_APB3_ADC1_CFG	R/W	0x120	CLK_APB3_ADC1 configuration register	0x0000 0001
CLK_APB3_ADC1_STAT	R	0x124	CLK_APB3_ADC1 status register	0x0000 0001
CLK_APB3_CAN_CFG	R/W	0x128	CLK_APB3_CAN configuration register	0x0000 0001
CLK_APB3_CAN_STAT	R	0x12C	CLK_APB3_CAN status register	0x0000 0001
-	-	0x130 to 0x1FC	Reserved	-
CLK_APB1_BUS_CFG	R/W	0x200	CLK_APB1_BUS configuration register	0x0000 0001
CLK_APB1_BUS_STAT	R	0x204	CLK_APB1_BUS status register	0x0000 0001
CLK_APB1_MOTOCONPWM_CFG	R/W	0x208	CLK_APB1_MOTOCON configuration register	0x0000 0001
CLK_APB1_MOTOCONPWM_STAT	R	0x20C	CLK_APB1_MOTOCON status register	0x0000 0001
CLK_APB1_I2C0_CFG	R/W	0x210	CLK_APB1_I2C0 configuration register	0x0000 0001
CLK_APB1_I2C0_STAT	R	0x214	CLK_APB1_I2C0 status register	0x0000 0001
CLK_APB1_I2S_CFG	R/W	0x218	CLK_APB1_I2S configuration register	0x0000 0001
CLK_APB1_I2S_STAT	R	0x21C	CLK_APB1_I2S status register	0x0000 0001
-	-	0x220 to 0x2FC	Reserved	-
CLK_SPIFI_CFG	R/W	0x300	CLK_SPIFI configuration register	0x0000 0001
CLK_SPIFI_STAT	R	0x304	CLK_SPIFI status register	0x0000 0001
-	-	0x308 to 0x3FC	Reserved	-
CLK_M3_BUS_CFG	R/W	0x400	CLK_M3_BUS configuration register	0x0000 0001
CLK_M3_BUS_STAT	R	0x404	CLK_M3_BUS status register	0x0000 0001
CLK_M3_SPIFI_CFG	R/W	0x408	CLK_M3_SPIFI configuration register	0x0000 0001
CLK_M3_SPIFI_STAT	R	0x40C	CLK_M3_SPIFI status register	0x0000 0001
CLK_M3_GPIO_CFG	R/W	0x410	CLK_M3_GPIO configuration register	0x0000 0001
CLK_M3_GPIO_STAT	R	0x414	CLK_M3_GPIO status register	0x0000 0001

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Table 954. Register overview: CCU1 (base address 0x4005 1000)

Name	Access	Address offset	Description	Reset value
CLK_M3_LCD_CFG	R/W	0x418	CLK_M3_LCD configuration register	0x0000 0001
CLK_M3_LCD_STAT	R	0x41C	CLK_M3_LCD status register	0x0000 0001
CLK_M3_ETHERNET_CFG	R/W	0x420	CLK_M3_ETHERNET configuration register	0x0000 0001
CLK_M3_ETHERNET_STAT	R	0x424	CLK_M3_ETHERNET status register	0x0000 0001
CLK_M3_USB0_CFG	R/W	0x428	CLK_M3_USB0 configuration register	0x0000 0001
CLK_M3_USB0_STAT	R	0x42C	CLK_M3_USB0 status register	0x0000 0001
CLK_M3_EMC_CFG	R/W	0x430	CLK_M3_EMC configuration register	0x0000 0001
CLK_M3_EMC_STAT	R	0x434	CLK_M3_EMC status register	0x0000 0001
CLK_M3_SDIO_CFG	R/W	0x438	CLK_M3_SDIO configuration register	0x0000 0001
CLK_M3_SDIO_STAT	R	0x43C	CLK_M3_SDIO status register	0x0000 0001
CLK_M3_DMA_CFG	R/W	0x440	CLK_M3_DMA configuration register	0x0000 0001
CLK_M3_DMA_STAT	R	0x444	CLK_M3_DMA status register	0x0000 0001
CLK_M3_M3CORE_CFG	R/W	0x448	CLK_M3_M3CORE configuration register	0x0000 0001
CLK_M3_M3CORE_STAT	R	0x44C	CLK_M3_M3CORE status register	0x0000 0001
-	-	0x450 to 0x45C	Reserved	-
CLK_M3_AES_CFG	R/W	0x460	CLK_M3_AES configuration register	0x0000 0001
CLK_M3_AES_STAT	R	0x464	CLK_M3_AES status register	0x0000 0001
CLK_M3_SCT_CFG	R/W	0x468	CLK_M3_SCT configuration register	0x0000 0001
CLK_M3_SCT_STAT	R	0x46C	CLK_M3_SCT status register	0x0000 0001
CLK_M3_USB1_CFG	R/W	0x470	CLK_M3_USB1 configuration register	0x0000 0001
CLK_M3_USB1_STAT	R	0x474	CLK_M3_USB1 status register	0x0000 0001
CLK_M3_EMCDIV_CFG	R/W	0x478	CLK_M3_EMCDIV configuration register	0x0000 0001
CLK_M3_EMCDIV_STAT	R	0x47C	CLK_M3_EMCDIV status register	0x0000 0001
-	-	0x480 to 0x4FC	Reserved	-
CLK_M3_WWDT_CFG	R/W	0x500	CLK_M3_WWDT configuration register	0x0000 0001
CLK_M3_WWDT_STAT	R	0x504	CLK_M3_WWDT status register	0x0000 0001
CLK_M3_USART0_CFG	R/W	0x508	CLK_M3_UART0 configuration register	0x0000 0001
CLK_M3_USART0_STAT	R	0x50C	CLK_M3_UART0 status register	0x0000 0001
CLK_M3_UART1_CFG	R/W	0x510	CLK_M3_UART1 configuration register	0x0000 0001
CLK_M3_UART1_STAT	R	0x514	CLK_M3_UART1 status register	0x0000 0001
CLK_M3_SSP0_CFG	R/W	0x518	CLK_M3_SSP0 configuration register	0x0000 0001
CLK_M3_SSP0_STAT	R	0x51C	CLK_M3_SSP0 status register	0x0000 0001
CLK_M3_TIMER0_CFG	R/W	0x520	CLK_M3_TIMER0 configuration register	0x0000 0001
CLK_M3_TIMER0_STAT	R	0x524	CLK_M3_TIMER0 status register	0x0000 0001
CLK_M3_TIMER1_CFG	R/W	0x528	CLK_M3_TIMER1 configuration register	0x0000 0001
CLK_M3_TIMER1_STAT	R	0x52C	CLK_M3_TIMER1 status register	0x0000 0001
CLK_M3_SCU_CFG	R/W	0x530	CLK_M3_SCU configuration register	0x0000 0001
CLK_M3_SCU_STAT	R	0x534	CLK_M3_SCU status register	0x0000 0001
CLK_M3_CREG_CFG	R/W	0x538	CLK_M3_CREG configuration register	0x0000 0001

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Table 954. Register overview: CCU1 (base address 0x4005 1000)

Name	Access	Address offset	Description	Reset value
CLK_M3_CREG_STAT	R	0x53C	CLK_M3_CREG status register	0x0000 0001
-	-	0x540 to 0x5FC	Reserved	-
CLK_M3_RITIMER_CFG	R/W	0x600	CLK_M3_RITIMER configuration register	0x0000 0001
CLK_M3_RITIMER_STAT	R	0x604	CLK_M3_RITIMER status register	0x0000 0001
CLK_M3_USART2_CFG	R/W	0x608	CLK_M3_UART2 configuration register	0x0000 0001
CLK_M3_USART2_STAT	R	0x60C	CLK_M3_UART2 status register	0x0000 0001
CLK_M3_USART3_CFG	R/W	0x610	CLK_M3_UART3 configuration register	0x0000 0001
CLK_M3_USART3_STAT	R	0x614	CLK_M3_UART3 status register	0x0000 0001
CLK_M3_TIMER2_CFG	R/W	0x618	CLK_M3_TIMER2 configuration register	0x0000 0001
CLK_M3_TIMER2_STAT	R	0x61C	CLK_M3_TIMER2 status register	0x0000 0001
CLK_M3_TIMER3_CFG	R/W	0x620	CLK_M3_TIMER3 configuration register	0x0000 0001
CLK_M3_TIMER3_STAT	R	0x624	CLK_M3_TIMER3 status register	0x0000 0001
CLK_M3_SSP1_CFG	R/W	0x628	CLK_M3_SSP1 configuration register	0x0000 0001
CLK_M3_SSP1_STAT	R	0x62C	CLK_M3_SSP1 status register	0x0000 0001
CLK_M3_QEI_CFG	R/W	0x630	CLK_M3_QEI configuration register	0x0000 0001
CLK_M3_QEI_STAT	R	0x634	CLK_M3_QEI status register	0x0000 0001
-	R/W	0x638 to 0x6FC	Reserved	-
-	R/W	0x700 to 0x7FC	Reserved	-
CLK_USB0_CFG	R/W	0x800	CLK_USB0configuration register	0x0000 0001
CLK_USB0_STAT	R	0x804	CLK_USB0 status register	0x0000 0001
-	-	0x808 to 0x8FC	Reserved	-
CLK_USB1_CFG	R/W	0x900	CLK_USB1 configuration register	0x0000 0001
CLK_USB1_STAT	R	0x904	CLK_USB1 status register	0x0000 0001
-	-	0x908 to 0x9FC	Reserved	-
-	-	0xA00	Reserved	-
-	-	0xA04	Reserved	-

Table 955. Register overview: CCU2 (base address 0x4005 2000)

Name	Access	Address offset	Description	Reset value
PM	R/W	0x000	CCU2 power mode register	0x0000 0000
BASE_STAT	R	0x004	CCU2 base clocks status register	0x0000 0FFF
-	-	0x008 to 0x0FC	Reserved	-
-	-	0x100 to 0x1FC	Reserved	-
CLK_APB2_USART3_CFG	R/W	0x200	CLK_APB2_UART3 configuration register	0x0000 0001

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Table 955. Register overview: CCU2 (base address 0x4005 2000)

Name	Access	Address offset	Description	Reset value
CLK_APB2_USART3_STAT	R	0x204	CLK_APB2_UART3 status register	0x0000 0001
-	-	0x208 to 0x2FC	Reserved	-
CLK_APB2_USART2_CFG	R/W	0x300	CLK_APB2_UART2 configuration register	0x0000 0001
CLK_APB2_USART2_STAT	R	0x304	CLK_APB2_UART2 status register	0x0000 0001
-	-	0x308 to 0x3FC	Reserved	-
CLK_APB0_UART1_CFG	R/W	0x400	CLK_APB0_UART1 configuration register	0x0000 0001
CLK_APB0_UART1_STAT	R	0x404	CLK_APB0_UART1 status register	0x0000 0001
-	-	0x408 to 0x4FC	Reserved	-
CLK_APB0_USART0_CFG	R/W	0x500	CLK_APB0_UART0 configuration register	0x0000 0001
CLK_APB0_USART0_STAT	R	0x504	CLK_APB0_UART0 status register	0x0000 0001
-	-	0x508 to 0x5FC	Reserved	-
CLK_APB2_SSP1_CFG	R/W	0x600	CLK_APB2_SSP1 configuration register	0x0000 0001
CLK_APB2_SSP1_STAT	R	0x604	CLK_APB2_SSP1 status register	0x0000 0001
-	-	0x608 to 0x6FC	Reserved	-
CLK_APB0_SSP0_CFG	R/W	0x700	CLK_APB0_SSP0 configuration register	0x0000 0001
CLK_APB0_SSP0_STAT	R	0x704	CLK_APB0_SSP0 status register	0x0000 0001
-	-	0x708 to 0x7FC	Reserved	-
CLK_SDIO_CFG	R/W	0x800	CLK_SDIO configuration register	0x0000 0001
CLK_SDIO_STAT	R	0x804	CLK_SDIO status register	0x0000 0001

42.5.5.1 Power mode register

This register contains a single bit, PD, that when set will disable all output clocks with Wake-up enabled (i.e. W = 1 in the CCU branch clock configuration registers, Section 42.5.5.3). Clocks disabled by writing to this register will be reactivated when a wake-up interrupt is detected or when a 0 is written into the PD bit.

Table 956. CCU1/2 power mode register (CCU1_PM, address 0x4005 1000 and CCU2_PM, address 0x4005 2000) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Initiate power-down mode	0	R/W
		0	Normal operation.		
		1	Clocks with wake-up mode enabled (W = 1) are disabled.		
31:1	-		Reserved.	-	-

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42.5.5.2 Base clock status register

Each bit in this register indicates if the specified base clock can be safely switched off. A logic zero indicates that all branch clocks generated from this base clock are disabled. Hence, the base clock can also be switched off. A logic one value indicates that there is still at least one branch clock running.

Remark: The base clock must be reactivated before writing to the configuration register of the branch clock.

Table 957. CCU1 base clock status register (CCU1_BASE_STAT, address 0x4005 1004) bit description

Bit	Symbol	Description	Reset value	Access
0	BASE_APB3_ CLK_IND	Base clock indicator for BASE_APB3_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
1	BASE_APB1_ CLK_IND	Base clock indicator for BASE_APB1_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
2	BASE_SPIFI_ CLK_IND	Base clock indicator for BASE_SPIFI_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
3	BASE_M3_ CLK_IND	Base clock indicator for BASE_M3_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
6:4	-	Reserved	-	-
7	BASE_USB0_ CLK_IND	Base clock indicator for BASE_USB0_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
8	BASE_USB1_ CLK_IND	Base clock indicator for BASE_USB1_CLK 0 = All branch clocks switched off. 1 = at least one branch clock running.	1	R
31:9	-	Reserved	-	-

Table 958. CCU2 base clock status register (CCU2_BASE_STAT, address 0x4005 2004) bit description

Bit	Symbol	Description	Reset value	Access
0	-	Reserved.	-	-
1	BASE_UART3_ CLK	Base clock indicator for BASE_UART3_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
2	BASE_UART2_ CLK	Base clock indicator for BASE_UART2_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R

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Table 958. CCU2 base clock status register (CCU2_BASE_STAT, address 0x4005 2004) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
3	BASE_UART1_ CLK	Base clock indicator for BASE_UART1_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
4	BASE_UART0_ CLK	Base clock indicator for BASE_UART0_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
5	BASE_SSP1_ CLK	Base clock indicator for BASE_SSP1_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
6	BASE_SSP0_ CLK	Base clock indicator for BASE_SSP0_CLK 0 = All branch clocks switched off. 1 = At least one branch clock running.	1	R
7	-	Reserved.	-	-
31:8	-	Reserved.	-	-

42.5.5.3 CCU1/2 branch clock configuration registers

Each generated output clock from the CCU has a configuration register. They all follow the format as described in Table 959 and Table 960.

On the LPC18xx, all branch clocks are in Run mode after reset. Auto and wake-up features are disabled.

The clock can be configured to run in the following modes described by the bits RUN, AUTO, and WAKEUP in the CLK_XXX_CFG registers:

RUN — The WAKEUP, PD, and AUTO control bits determine the activation of the branch clock. If register bit AUTO is set the AHB disable protocol must complete before the clock is switched off. The PD bit is set in Table 956.

AUTO — Enable auto (AHB disable mechanism). The PMU initiates the AHB disable protocol before switching the clock off. This protocol ensures that all AHB transactions have been completed before turning the clock off.

WAKEUP — The branch clock is wake-up enabled when the PD bit in the Power Mode register (seeTable 956) is set and clocks which are wake-up enabled are switched off. These clocks will be switched on if a wake-up event is detected or if the PD bit is cleared. If register bit AUTO is set, the AHB disable protocol must complete before the clock is switched off.

Remark: In order to safely disable any of the branch clocks, use two separate writes to the CLK_XXX_CFG register: first set the AUTO bit, and then on the next write, disable the clock by setting the RUN bit to zero.

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Table 959. CCU1 branch clock configuration register (CLK_XXX_CFG, addresses 0x4005 1100, 0x4005 1104,..., 0x4005 1A00) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	RUN		Run enable	1	R/W
		0	Clock is disabled.		
		1	Clock is enabled.		
1	AUTO		Auto (AHB disable mechanism) enable	0	R/W
		0	Auto is disabled.		
		1	Auto is enabled.		
2	WAKEUP		Wake-up mechanism enable	0	R/W
		0	Wake-up is disabled.		
		1	Wake-up is enabled.		
31:3	-		Reserved	-	-

Table 960. CCU2 branch clock configuration register (CLK_XXX_CFG, addresses 0x4005 2100, 0x4005 2200,..., 0x4005 2800) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	RUN		Run enable	1	R/W
		0	Clock is disabled.		
		1	Clock is enabled.		
1	AUTO		Auto (AHB disable mechanism) enable	0	R/W
		0	Auto is disabled.		
		1	Auto is enabled.		
2	WAKEUP		Wake-up mechanism enable	0	R/W
		0	Wake-up is disabled.		
		1	Wake-up is enabled.		
31:3	-		Reserved	-	-

42.5.5.4 CCU1/2 branch clock status registers

Like the Configuration Register, each generated output clock from the CCU has a status register. When the configuration register of an output clock is written into, the value of the actual hardware signals may not be updated immediately because of the Auto or Wake-up mechanism. The Status Register shows the current value of these signals. All output clock Status Registers follow the format as described in Table 961 and Table 962.

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Table 961. CCU1 branch clock status register (CLK_XXX_STAT, addresses 0x4005 1104, 0x4005 110C,..., 0x4005 1A04) bit description

Bit	Symbol	Description	Reset value	Access
0	RUN	Run enable status 0 = clock is disabled. 1 = clock is enabled.	1	R
1	AUTO	Auto (AHB disable mechanism) enable status 0 = Auto is disabled. 1 = Auto is enabled.	0	R
2	WAKEUP	Wake-up mechanism enable status 0 = Wake-up is disabled. 1 = Wake-up is enabled.	0	R
31:3	-	Reserved	-	-

Table 962. CCU2 branch clock status register (CLK_XXX_STAT, addresses 0x4005 2104, 0x4005 2204,..., 0x4005 2804) bit description

Bit	Symbol	Description	Reset value	Access
0	RUN	Run enable status 0 = clock is disabled 1 = clock is enabled	1	R
1	AUTO	Auto (AHB disable mechanism) enable status 0 = Auto is disabled 1 = Auto is enabled	0	R
2	WAKEUP	Wake-up mechanism enable status 0 = Wake-up is disabled 1 = Wake-up is enabled	0	R
31:3	-	Reserved	-	-

42.6 LPC1850/30/20/10 Rev ‘-’ Pin configuration

42.6.1 Pin description

On the LPC18xx, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin may support up to four different digital functions, including General Purpose I/O (GPIO), selectable through the SCU registers. Note that the pin name is not indicative of the GPIO port assigned to it.

Table 963. Pin description

Symbol	LBGA256	Reset state [1]	Type	Description
Multiplexed digital pins				

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
P0_0[2]	L3	I; PU	I/O	**GPIO0[0]** — General purpose digital input/output pin.
			I/O	**SSP1_MISO** — Master In Slave Out for SSP1.
			I	**ENET_RXD1** — Ethernet receive data 1 (RMII/MII interface).
			-	n.c.
P0_1[2]	M2	I; PU	I/O	**GPIO0[1]** — General purpose digital input/output pin.
			I/O	**SSP1_MOSI** — Master Out Slave in for SSP1.
			I	**ENET_COL** — Ethernet Collision detect (MII interface).
			-	n.c.
P1_0[2]	P2	I; PU	I/O	**GPIO0[4]** — General purpose digital input/output pin.
			I	**CTIN_3** — SCT input 3. Capture input 1 of timer 1.
			I/O	**EXTBUS_A5** — External memory address line 5.
			-	n.c.
P1_1[2]	R2	I; PU	I/O	**GPIO0[8]** — General purpose digital input/output pin.
			O	**CTOUT_7** — SCT output 7. Match output 3 of timer 1.
			I/O	**EXTBUS_A6** — External memory address line 6. Boot control pin 0 (see Table 8).
			-	n.c.
P1_2[2]	R3	I; PU	I/O	**GPIO0[9]** — General purpose digital input/output pin.
			O	**CTOUT_6** — SCT output 6. Match output 2 of timer 1.
			I/O	**EXTBUS_A7** — External memory address line 7. Boot control pin 1 (see Table 8).
			-	n.c.
P1_3[2]	P5	I; PU	I/O	**GPIO0[10]** — General purpose digital input/output pin.
			O	**CTOUT_8** — SCT output 8. Match output 0 of timer 2.
			-	n.c.
			O	**$\overline{\text{EXTBUS_OE}}$** — LOW active Output Enable signal.
P1_4[2]	T3	I; PU	I/O	**GPIO0[11]** — General purpose digital input/output pin.
			O	**CTOUT_9** — SCT output 9. Match output 1 of timer 2.
			-	n.c.
			O	**$\overline{\text{EXTBUS_BLS0}}$** — LOW active Byte Lane select signal 0.
P1_5[2]	R5	I; PU	I/O	**GPIO1[8]** — General purpose digital input/output pin.
			O	**CTOUT_10** — SCT output 10. Match output 2 of timer 2.
			-	n.c.
			O	**$\overline{\text{EXTBUS_CS0}}$** — LOW active Chip Select 0 signal.
P1_6[2]	T4	I; PU	I/O	**GPIO1[9]** — General purpose digital input/output pin.
			I	**CTIN_5** — SCT input 5. Capture input 2 of timer 2.
			-	n.c.
			O	**$\overline{\text{EXTBUS_WE}}$** — LOW active Write Enable signal.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
P1_7[2]	T5	I; PU	I/O	**GPIO1[0]** — General purpose digital input/output pin.
			I	**U1_DSR** — Data Set Ready input for UART1.
			O	**CTOUT_13** — SCT output 13. Match output 1 of timer 3.
			I/O	**EXTBUS_D0** — External memory data line 0.
P1_8[2]	R7	I; PU	I/O	**GPIO1[1]** — General purpose digital input/output pin.
			O	**U1_DTR** — Data Terminal Ready output for UART1.
			O	**CTOUT_12** — SCT output 12. Match output 0 of timer 3.
			I/O	**EXTBUS_D1** — External memory data line 1.
P1_9[2]	T7	I; PU	I/O	**GPIO1[2]** — General purpose digital input/output pin.
			O	**U1_RTS** — Request to Send output for UART1.
			O	**CTOUT_11** — SCT output 11. Match output 3 of timer 2.
			I/O	**EXTBUS_D2** — External memory data line 2.
P1_10[2]	R8	I; PU	I/O	**GPIO1[3]** — General purpose digital input/output pin.
			I	**U1_RI** — Ring Indicator input for UART1.
			O	**CTOUT_14** — SCT output 14. Match output 2 of timer 3.
			I/O	**EXTBUS_D3** — External memory data line 3.
P1_11[2]	T9	I; PU	I/O	**GPIO1[4]** — General purpose digital input/output pin.
			I	**U1_CTS** — Clear to Send input for UART1.
			O	**CTOUT_15** — SCT output 15. Match output 3 of timer 3.
			I/O	**EXTBUS_D4** — External memory data line 4.
P1_12[2]	R9	I; PU	I/O	**GPIO1[5]** — General purpose digital input/output pin.
			I	**U1_DCD** — Data Carrier Detect input for UART1.
			-	n.c.
			I/O	**EXTBUS_D5** — External memory data line 5.
P1_13[2]	R10	I; PU	I/O	**GPIO1[6]** — General purpose digital input/output pin.
			O	**U1_TXD** — Transmitter output for UART1.
			-	n.c.
			I/O	**EXTBUS_D6** — External memory data line 6.
P1_14[2]	R11	I; PU	I/O	**GPIO1[7]** — General purpose digital input/output pin.
			I	**U1_RXD** — Receiver input for UART1.
			-	n.c.
			I/O	**EXTBUS_D7** — External memory data line 7.
P1_15[2]	T12	I; PU	I/O	**GPIO0[2]** — General purpose digital input/output pin.
			O	**U2_TXD** — Transmitter output for UART2.
			-	n.c.
			I	**ENET_RXD0** — Ethernet receive data 0 (RMII/MII interface).

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
P1_16[2]	M7	I; PU	I/O	**GPIO0[3]** — General purpose digital input/output pin.
			I	**U2_RXD** — Receiver input for UART2.
			-	n.c.
			I	**ENET_CRS (ENET_CRS_DV)** — Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
P1_17[2]	M8	I; PU	I/O	**GPIO0[12]** — General purpose digital input/output pin.
			I/O	**U2_UCLK** — Serial clock input/output for UART2 in synchronous mode.
			-	n.c.
			I/O	**ENET_MDIO** — Ethernet MIIM data input and output.
P1_18[2]	N12	I; PU	I/O	**GPIO0[13]** — General purpose digital input/output pin.
			I/O	**U2_DIR** — RS-485/EIA-485 output enable/direction control for UART2.
			-	n.c.
			O	**ENET_TXD0** — Ethernet transmit data 0 (RMII/MII interface).
P1_19[2]	M11	I; PU	I	**ENET_TX_CLK (ENET_REF_CLK)** — Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
			I/O	**SSP1_SCK** — Serial clock for SSP1.
			-	n.c.
			-	n.c.
P1_20[2]	M10	I; PU	I/O	**GPIO0[15]** — General purpose digital input/output pin.
			I/O	**SSP1_SSEL** — Slave Select for SSP1.
			-	n.c.
			O	**ENET_TXD1** — Ethernet transmit data 1 (RMII/MII interface).
P2_0[2]	T16	I; PU	-	n.c.
			O	**U0_TXD** — Transmitter output for USART0.
			I/O	**EXTBUS_A13** — External memory address line 13.
			O	**USB0_PWR_EN** — VBUS drive signal (towards external charge pump or power management unit); indicates that Vbus must be driven (active high).
P2_1[2]	N15	I; PU	-	n.c.
			I	**U0_RXD** — Receiver input for USART0.
			I/O	**EXTBUS_A12** — External memory address line 12.
			O	**USB0_PWR_FAULT** — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
P2_2[2]	M15	I; PU	-	n.c.
			I/O	**U0_UCLK** — Serial clock input/output for USART0 in synchronous mode.
			I/O	**EXTBUS_A11** — External memory address line 11.
			O	**USB0_IND1** — USB0 port indicator LED control output 1.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
P2_3[2]	J12	I; PU	-	n.c.
			I/O	**I2C1_SDA** — I^{2}C1 data input/output (this pin does not use a specialized I2C pad).
			O	**U3_TXD** — Transmitter output for USART3.
			I	**CTIN_1** — SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
P2_4[2]	K11	I; PU	-	n.c.
			I/O	**I2C1_SCL** — I^{2}C1 clock input/output (this pin does not use a specialized I2C pad).
			I	**U3_RXD** — Receiver input for USART3.
			I	**CTIN_0** — SCT input 0. Capture input 0 of timer 0, 1, 2, 3.
P2_5[3]	K14	I; PU	-	n.c.
			I	**CTIN_2** — SCT input 2. Capture input 2 of timer 0.
			I	**USB1_VBUS** — Monitors the presence of USB1 bus power. **Note:** This signal must be HIGH for USB reset to occur.
			I	**ADCTRIG1** — ADC trigger input 1.
P2_6[2]	K16	I; PU	-	n.c.
			I/O	**U0_DIR** — RS-485/EIA-485 output enable/direction control for USART0.
			I/O	**EXTBUS_A10** — External memory address line 10.
			O	**USB0_IND0** — USB0 port indicator LED control output 0.
P2_7[2]	H14	I; PU	I/O	**GPIO0[7]** — General purpose digital input/output pin.
			O	**CTOUT_1** — SCT output 1. Match output 1 of timer 0.
			I/O	**U3_UCLK** — Serial clock input/output for USART3 in synchronous mode.
			I/O	**EXTBUS_A9** — External memory address line 9. Boot control pin 3 (see Table 8). This pin must be HIGH on reset.
P2_8[2]	J16	I; PU	-	n.c.
			O	**CTOUT_0** — SCT output 0. Match output 0 of timer 0.
			I/O	**U3_DIR** — RS-485/EIA-485 output enable/direction control for USART3.
			I/O	**EXTBUS_A8** — External memory address line 8. Boot control pin 2 (see Table 8).
P2_9[2]	H16	I; PU	I/O	**GPIO1[10]** — General purpose digital input/output pin.
			O	**CTOUT_3** — SCT output 3. Match output 3 of timer 0.
			I/O	**U3_BAUD3** — <tbd>for USART3.
			I/O	**EXTBUS_A0** — External memory address line 0.
P2_10[2]	G16	I; PU	I/O	**GPIO0[14]** — General purpose digital input/output pin.
			O	**CTOUT_2** — SCT output 2. Match output 2 of timer 0.
			O	**U2_TXD** — Transmitter output for USART2.
			I/O	**EXTBUS_A1** — External memory address line 1.

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Table 963. Pin description *...continued*

Symbol	LBGA256	Reset state [1]	Type	Description
P2_11[2]	F16	I; PU	I/O	**GPIO1[11]** — General purpose digital input/output pin.
			O	**CTOUT_5** — SCT output 5. Match output 1 of timer 1.
			I	**U2_RXD** — Receiver input for USART2.
			I/O	**EXTBUS_A2** — External memory address line 2.
P2_12[2]	E15	I; PU	I/O	**GPIO1[12]** — General purpose digital input/output pin.
			O	**CTOUT_4** — SCT output 4. Match output 0 of timer 1.
			-	n.c.
			I/O	**EXTBUS_A3** — External memory address line 3.
P2_13[2]	C16	I; PU	I/O	**GPIO1[13]** — General purpose digital input/output pin.
			I	**CTIN_4** — SCT input 4. Capture input 2 of timer 1.
			-	n.c.
			I/O	**EXTBUS_A4** — External memory address line 4.
P3_0[2]	F13	I; PU	I/O	**I2S_RX_SCK** — Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^{2}S-bus specification.
			O	**I2S_RX_MCLK** — I2S receive master clock.
			I/O	**I2S_TX_SCK** — I^{2}S transmit clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^{2}S-bus specification*.
			O	**I2S_TX_MCLK** — I2S transmit master clock.
P3_1[2]	G11	I; PU	I/O	**I2S_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^{2}S-bus specification*.
			I/O	**I2S_RX_WS** — Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^{2}S-bus specification*.
			I	**CAN1_RD** — CAN1 receiver input.
			O	**USB1_IND1** — USB1 port indicator LED control output 1.
P3_2[2]	F11	I; PU	I/O	**I2S_TX_SDA** — I^{2}S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^{2}S-bus specification*.
			I/O	**I2S_RX_SDA** — I^{2}S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^{2}S-bus specification*.
			O	**CAN1_TD** — CAN1 transmitter output.
			O	**USB1_IND0** — USB1 port indicator LED control output 0.
P3_3[2]	B14	I; PU	-	n.c.
			-	n.c.
			I/O	**SSP0_SCK** — Serial clock for SSP0.
			O	**SPIFI_SCK** — Serial clock for SPIFI.
P3_4[2]	A15	I; PU	I/O	**GPIO1[14]** — General purpose digital input/output pin.
			-	n.c.
			-	n.c.
			I/O	**SPIFI_SIO3** — I/O lane 3 for SPIFI.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
P3_5[2]	C12	I; PU	I/O	**GPIO1[15]** — General purpose digital input/output pin.
			-	n.c.
			-	n.c.
			I/O	**SPIFI_SIO2** — I/O lane 2 for SPIFI.
P3_6[2]	B13	I; PU	I/O	**GPIO0[6]** — General purpose digital input/output pin.
			-	n.c.
			I/O	**SSP0_SSEL** — Slave Select for SSP0.
			I/O	**SPIFI_MISO** — Input I1 in SPIFI quad mode; SPIFI output IO1.
P3_7[2]	C11	I; PU	-	n.c.
			-	n.c.
			I/O	**SSP0_MISO** — Master In Slave Out for SSP0.
			I/O	**SPIFI_MOSI** — Input I0 in SPIFI quad mode; SPIFI output IO0.
P3_8[2]	C10	I; PU	-	n.c.
			-	n.c.
			I/O	**SSP0_MOSI** — Master Out Slave in for SSP0.
			I/O	**SPIFI_CS** — SPIFI serial flash chip select.
P4_0[2]	D5	I; PU	I/O	**GPIO2[0]** — General purpose digital input/output pin.
			O	**MCOA0** — Motor control PWM channel 0, output A.
			I	**NMI** — External interrupt input to NMI.
			-	n.c.
P4_1[2]	A1	I; PU	I/O	**GPIO2[1]** — General purpose digital input/output pin.
			O	**CTOUT_1** — SCT output 1. Match output 1 of timer 0.
			O	**LCDVD0** — LCD data.
			-	n.c.
P4_2[2]	D3	I; PU	I/O	**GPIO2[2]** — General purpose digital input/output pin.
			O	**CTOUT_0** — SCT output 0. Match output 0 of timer 0.
			O	**LCDVD3** — LCD data.
			-	n.c.
P4_3[2]	C2	I; PU	I/O	**GPIO2[3]** — General purpose digital input/output pin.
			O	**CTOUT_3** — SCT output 0. Match output 3 of timer 0.
			O	**LCDVD2** — LCD data.
			-	n.c.
P4_4[2]	B1	I; PU	I/O	**GPIO2[4]** — General purpose digital input/output pin.
			O	**CTOUT_2** — SCT output 2. Match output 2 of timer 0.
			O	**LCDVD1** — LCD data.
			-	n.c.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
P4_5[2]	D2	I; PU	I/O	**GPIO2[5]** — General purpose digital input/output pin.
			O	**CTOUT_5** — SCT output 5. Match output 1 of timer 1.
			O	**LCDFP** — Frame pulse (STN). Vertical synchronization pulse (TFT).
			-	n.c.
P4_6[2]	C1	I; PU	I/O	**GPIO2[6]** — General purpose digital input/output pin.
			O	**CTOUT_4** — SCT output 4. Match output 0 of timer 1.
			O	**LCDENAB/LCDM** — STN AC bias drive or TFT data enable input.
			-	n.c.
P4_7[2]	H4	O;PU	O	**LCDDCLK** — LCD panel clock.
			I	**GP_CLKIN** — General purpose clock input to the CGU.
			-	n.c.
			-	n.c.
P4_8[2]	E2	I; PU	-	n.c.
			I	**CTIN_5** — SCT input 5. Capture input 2 of timer 2.
			O	**LCDVD9** — LCD data.
			-	n.c.
P4_9[2]	L2	I; PU	-	n.c.
			I	**CTIN_6** — SCT input 6. Capture input 1 of timer 3.
			O	**LCDVD11** — LCD data.
			-	n.c.
P4_10[2]	M3	I; PU	-	n.c.
			I	**CTIN_2** — SCT input 2. Capture input 2 of timer 0.
			O	**LCDVD10** — LCD data.
			-	n.c.
P5_0[2]	N3	I; PU	I/O	**GPIO2[9]** — General purpose digital input/output pin.
			O	**MCOB2** — Motor control PWM channel 2, output B.
			I/O	**EXTBUS_D12** — External memory data line 12.
			-	n.c.
P5_1[2]	P3	I; PU	I/O	**GPIO2[10]** — General purpose digital input/output pin.
			I	**MCI2** — Motor control PWM channel 2, input.
			I/O	**EXTBUS_D13** — External memory data line 13.
			-	n.c.
P5_2[2]	R4	I; PU	I/O	**GPIO2[11]** — General purpose digital input/output pin.
			I	**MCI1** — Motor control PWM channel 1, input.
			I/O	**EXTBUS_D14** — External memory data line 14.
			-	n.c.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
P5_3[2]	T8	I; PU	I/O	**GPIO2[12]** — General purpose digital input/output pin.
			I	**MCI0** — Motor control PWM channel 0, input.
			I/O	**EXTBUS_D15** — External memory data line 15.
			-	n.c.
P5_4[2]	P9	I; PU	I/O	**GPIO2[13]** — General purpose digital input/output pin.
			O	**MCOB0** — Motor control PWM channel 0, output B.
			I/O	**EXTBUS_D8** — External memory data line 8.
			-	n.c.
P5_5[2]	P10	I; PU	I/O	**GPIO2[14]** — General purpose digital input/output pin.
			O	**MCOA1** — Motor control PWM channel 1, output A.
			I/O	**EXTBUS_D9** — External memory data line 9.
			-	n.c.
P5_6[2]	T13	I; PU	I/O	**GPIO2[15]** — General purpose digital input/output pin.
			O	**MCOB1** — Motor control PWM channel 1, output B.
			I/O	**EXTBUS_D10** — External memory data line 10.
			-	n.c.
P5_7[2]	R12	I; PU	I/O	**GPIO2[7]** — General purpose digital input/output pin.
			O	**MCOA2** — Motor control PWM channel 2, output A.
			I/O	**EXTBUS_D11** — External memory data line 11.
			-	n.c.
P6_0	M12	I; PU	I/O	**I2S_RX_SCK** — Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
			O	**I2S_RX_MCLK** — I2S receive master clock.
			-	n.c.
			-	n.c.
P6_1[2]	R15	I; PU	I/O	**GPIO3[0]** — General purpose digital input/output pin.
			O	**EXTBUS_DYCS1** — SDRAM chip select 1.
			I/O	**U0_UCLK** — Serial clock input/output for USART0 in synchronous mode.
			I/O	**I2S_RX_WS** — Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
P6_2[2]	L13	I; PU	I/O	**GPIO3[1]** — General purpose digital input/output pin.
			O	**EXTBUS_CKEOUT1** — SDRAM clock enable 1.
			I/O	**U0_DIR** — RS-485/EIA-485 output enable/direction control for USART0.
			I/O	**I2S_RX_SDA** — I²S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
P6_3[2]	P15	I; PU	I/O	**GPIO3[2]** — General purpose digital input/output pin.
			O	**USB0_PWR_EN** — VBUS drive signal (towards external charge pump or power management unit); indicates that Vbus must be driven (active high).
			-	n.c.
			O	**EXTBUS_CS1** — LOW active Chip Select 1 signal.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
P6_4[2]	R16	I; PU	I/O	**GPIO3[3]** — General purpose digital input/output pin.
			I	**CTIN_6** — SCT input 6. Capture input 1 of timer 3.
			O	**U0_TXD** — Transmitter output for USART0.
			O	**EXTBUS_CAS** — LOW active SDRAM Column Address Strobe.
P6_5[2]	P16	I; PU	I/O	**GPIO3[4]** — General purpose digital input/output pin.
			O	**CTOUT_6** — SCT output 6. Match output 2 of timer 1.
			I	**U0_RXD** — Receiver input for USART0.
			O	**EXTBUS_RAS** — LOW active SDRAM Row Address Strobe.
P6_6[2]	L14	I; PU	I/O	**GPIO0[5]** — General purpose digital input/output pin.
			O	**EXTBUS_BLS1** — LOW active Byte Lane select signal 1.
			-	n.c.
			O	**USB0_PWR_FAULT** — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
P6_7[2]	J13	I; PU	-	n.c.
			I/O	**EXTBUS_A15** — External memory address line 15.
			-	n.c.
			O	**USB0_IND1** — USB0 port indicator LED control output 1.
P6_8[2]	H13	I; PU	-	n.c.
			I/O	**EXTBUS_A14** — External memory address line 14.
			-	n.c.
			O	**USB0_IND0** — USB0 port indicator LED control output 0.
P6_9[2]	J15	I; PU	I/O	**GPIO3[5]** — General purpose digital input/output pin.
			-	n.c.
			-	n.c.
			O	**EXTBUS_DYCS0** — SDRAM chip select 0.
P6_10[2]	H15	I; PU	I/O	**GPIO3[6]** — General purpose digital input/output pin.
			O	**MCABORT** — Motor control PWM, LOW-active fast abort.
			-	n.c.
			O	**EXTBUS_DQMOUT1** — Data mask 1 used with SDRAM and static devices.
P6_11[2]	H12	I; PU	I/O	**GPIO3[7]** — General purpose digital input/output pin.
			-	n.c.
			-	n.c.
			O	**EXTBUS_CKEOUT0** — SDRAM clock enable 0.
P6_12[2]	G15	I; PU	I/O	**GPIO2[8]** — General purpose digital input/output pin.
			O	**CTOUT_7** — SCT output 7. Match output 3 of timer 1.
			-	n.c.
			O	**EXTBUS_DQMOUT0** — Data mask 0 used with SDRAM and static devices.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
P7_0[2]	B16	I; PU	I/O	**GPIO3[8]** — General purpose digital input/output pin.
			O	**CTOUT_14** — SCT output 14. Match output 2 of timer 3.
			-	n.c.
			O	**LCDLE** — Line end signal.
P7_1[2]	C14	I; PU	I/O	**GPIO3[9]** — General purpose digital input/output pin.
			O	**CTOUT_15** — SCT output 15. Match output 3 of timer 3.
			I/O	**I2S_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
			O	**LCDVD19** — LCD data.
P7_2[2]	A16	I; PU	I/O	**GPIO3[10]** — General purpose digital input/output pin.
			I	**CTIN_4** — SCT input 4. Capture input 2 of timer 1.
			I/O	**I2S_TX_SDA** — I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
			O	**LCDVD18** — LCD data.
P7_3[2]	C13	I; PU	I/O	**GPIO3[11]** — General purpose digital input/output pin.
			I	**CTIN_3** — SCT input 3. Capture input 1 of timer 1.
			-	n.c.
			O	**LCDVD17** — LCD data.
P7_4[2]	C8	I; PU	I/O	**GPIO3[12]** — General purpose digital input/output pin.
			O	**CTOUT_13** — SCT output 13. Match output 1 of timer 3.
			-	n.c.
			O	**LCDVD16** — LCD data.
P7_5[2]	A7	I; PU	I/O	**GPIO3[13]** — General purpose digital input/output pin.
			O	**CTOUT_12** — SCT output 12. Match output 0 of timer 3.
			-	n.c.
			O	**LCDVD8** — LCD data.
P7_6[2]	C7	I; PU	I/O	**GPIO3[14]** — General purpose digital input/output pin.
			O	**CTOUT_11** — SCT output 1. Match output 3 of timer 2.
			-	n.c.
			O	**LCDLP** — Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
P7_7[2]	B6	I; PU	I/O	**GPIO3[15]** — General purpose digital input/output pin.
			O	**CTOUT_8** — SCT output 8. Match output 0 of timer 2.
			-	n.c.
			O	**LCDPWR** — LCD panel power enable.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
P8_0[2]	E5	I; PU	I/O	**GPIO4[0]** — General purpose digital input/output pin.
			O	**USB0_PWR_FAULT** — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
			-	n.c.
			I	**MCI2** — Motor control PWM channel 2, input.
P8_1[2]	H5	I; PU	I/O	**GPIO4[1]** — General purpose digital input/output pin.
			O	**USB0_IND1** — USB0 port indicator LED control output 1.
			-	n.c.
			I	**MCI1** — Motor control PWM channel 1, input.
P8_2[2]	K4	I; PU	I/O	**GPIO4[2]** — General purpose digital input/output pin.
			O	**USB0_IND0** — USB0 port indicator LED control output 0.
			-	n.c.
			I	**MCI0** — Motor control PWM channel 0, input.
P8_3[2]	J3	I; PU	I/O	**GPIO4[3]** — General purpose digital input/output pin.
			I/O	**USB1_ULPI_D2** — ULPI link bidirectional data line 2.
			-	n.c.
			O	**LCDVD12** — LCD data.
P8_4[2]	J2	I; PU	I/O	**GPIO4[4]** — General purpose digital input/output pin.
			I/O	**USB1_ULPI_D1** — ULPI link bidirectional data line 1.
			-	n.c.
			O	**LCDVD7** — LCD data.
P8_5[2]	J1	I; PU	I/O	**GPIO4[5]** — General purpose digital input/output pin.
			I/O	**USB1_ULPI_D0** — ULPI link bidirectional data line 0.
			-	n.c.
			O	**LCDVD6** — LCD data.
P8_6[2]	K3	I; PU	I/O	**GPIO4[6]** — General purpose digital input/output pin.
			I	**USB1_ULPI_NXT** — ULPI link NXT signal. Data flow control signal from the PHY.
			-	n.c.
			O	**LCDVD5** — LCD data.
P8_7[2]	K1	I; PU	I/O	**GPIO4[7]** — General purpose digital input/output pin.
			O	**USB1_ULPI_STP** — ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
			-	n.c.
			O	**LCDVD4** — LCD data.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
P8_8[2]	L1	I; PU	-	n.c.
			I	**USB1_ULPI_CLK** — ULPI link CLK signal. 60 MHz clock generated by the PHY.
			-	n.c.
			-	n.c.
P9_0[2]	T1	I; PU	I/O	**GPIO4[12]** — General purpose digital input/output pin.
			O	**MCABORT** — Motor control PWM, LOW-active fast abort.
			-	n.c.
			-	n.c.
P9_1[2]	N6	I; PU	I/O	**GPIO4[13]** — General purpose digital input/output pin.
			O	**MCOA2** — Motor control PWM channel 2, output A.
			-	n.c.
			-	n.c.
P9_2[2]	N8	I; PU	I/O	**GPIO4[14]** — General purpose digital input/output pin.
			O	**MCOB2** — Motor control PWM channel 2, output B.
			-	n.c.
			-	n.c.
P9_3[2]	M6	I; PU	I/O	**GPIO4[15]** — General purpose digital input/output pin.
			O	**MCOA0** — Motor control PWM channel 0, output A.
			O	**USB1_IND1** — USB1 Port indicator LED control output 1.
			-	n.c.
P9_4[2]	N10	I; PU	-	n.c.
			O	**MCOB0** — Motor control PWM channel 0, output B.
			O	**USB1_IND0** — USB1 Port indicator LED control output 0.
			-	n.c.
P9_5[2]	M9	I; PU	-	n.c.
			O	**MCOA1** — Motor control PWM channel 1, output A.
			O	**USB1_VBUS_EN** — USB1 VBUS power enable.
			-	n.c.
P9_6[2]	L11	I; PU	I/O	**GPIO4[11]** — General purpose digital input/output pin.
			O	**MCOB1** — Motor control PWM channel 1, output B.
			O	**USB1_PWR_FAULT** — USB1 Port power fault signal indicating over-current condition; this signal monitors over-current on the USB1 bus (external circuitry required to detect over-current condition).
			-	n.c.
PA_0[2]	L12	I; PU	-	n.c.
			-	n.c.
			-	n.c.
			-	n.c.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
PA_1[2]	J14	I; PU	I/O	**GPIO4[8]** — General purpose digital input/output pin.
			I	**QEI_IDX** — Quadrature Encoder Interface INDEX input.
			-	n.c.
			-	n.c.
PA_2[2]	K15	I; PU	I/O	**GPIO4[9]** — General purpose digital input/output pin.
			I	**QEI_PHB** — Quadrature Encoder Interface PHB input.
			-	n.c.
			-	n.c.
PA_3[2]	H11	I; PU	I/O	**GPIO4[10]** — General purpose digital input/output pin.
			I	**QEI_PHA** — Quadrature Encoder Interface PHA input.
			-	n.c.
			-	n.c.
PA_4[2]	G13	I; PU	-	n.c.
			O	**CTOUT_9** — SCT output 9. Match output 1 of timer 2.
			-	n.c.
			I/O	**EXTBUS_A23** — External memory address line 23.
PB_0[2]	B15	I; PU	-	n.c.
			O	**CTOUT_10** — SCT output 10. Match output 2 of timer 2.
			O	**LCDVD23** — LCD data.
			-	n.c.
PB_1[2]	A14	I; PU	-	n.c.
			I	**USB1_ULPI_DIR** — ULPI link DIR signal. Controls the ULP data line direction.
			O	**LCDVD22** — LCD data.
			-	n.c.
PB_2[2]	B12	I; PU	-	n.c.
			I/O	**USB1_ULPI_D7** — ULPI link bidirectional data line 7.
			O	**LCDVD21** — LCD data.
			-	n.c.
PB_3[2]	A13	I; PU	-	n.c.
			I/O	**USB1_ULPI_D6** — ULPI link bidirectional data line 6.
			O	**LCDVD20** — LCD data.
			-	n.c.
PB_4[2]	B11	I; PU	-	n.c.
			I/O	**USB1_ULPI_D5** — ULPI link bidirectional data line 5.
			O	**LCDVD15** — LCD data.
			-	n.c.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
PB_5[2]	A12	I; PU	-	n.c.
			I/O	**USB1_ULPI_D4** — ULPI link bidirectional data line 4.
			O	**LCDVD14** — LCD data.
			-	n.c.
PB_6[2]	A6	I; PU	-	n.c.
			I/O	**USB1_ULPI_D3** — ULPI link bidirectional data line 3.
			O	**LCDVD13** — LCD data.
			-	n.c.
PC_0[2]	D4	I; PU	I/O	**SDIO_CLK** — SD/MMC card clock.
			I	**USB1_ULPI_CLK** — ULPI link CLK signal. 60 MHz clock generated by the PHY.
			I/O	**SDIO_CLK** — SD/MMC card clock.
			I/O	**ENET_RX_CLK** — Ethernet Receive Clock (MII interface).
PC_1[2]	E4	I; PU	I/O	**USB1_ULPI_D7** — ULPI link bidirectional data line 7.
			O	**SDIO_VOLT0** — SD/MMC bus voltage select output 0.
			I	**U1_RI** — Ring Indicator input for UART 1.
			O	**ENET_MDC** — Ethernet MIIM clock.
PC_2[2]	F6	I; PU	I/O	**USB1_ULPI_D6** — ULPI link bidirectional data line 6.
			O	**SDIO_RST** — SD/MMC reset signal for MMC4.4 card.
			I	**U1_CTS** — Clear to Send input for UART 1.
			O	**ENET_TXD2** — Ethernet transmit data 2 (MII interface).
PC_3[2]	F5	I; PU	I/O	**USB1_ULPI_D5** — ULPI link bidirectional data line 5.
			O	**SDIO_VOLT1** — SD/MMC bus voltage select output 1.
			O	**U1_RTS** — Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
			O	**ENET_TXD3** — Ethernet transmit data 3 (MII interface).
PC_4[2]	F4	I; PU	I/O	**SDIO_D0** — SD/MMC data bus line 0.
			I/O	**USB1_ULPI_D4** — ULPI link bidirectional data line 4.
			-	n.c.
			O	**ENET_TX_EN** — Ethernet transmit data enable (RMII/MII interface).
PC_5[2]	G4	I; PU	I/O	**SDIO_D1** — SD/MMC data bus line 1.
			I/O	**USB1_ULPI_D3** — ULPI link bidirectional data line 3.
			-	n.c.
			O	**ENET_TX_ER** — Ethernet Transmit Error (MII interface).
PC_6[2]	H6	I; PU	I/O	**SDIO_D2** — SD/MMC data bus line 2.
			I/O	**USB1_ULPI_D2** — ULPI link bidirectional data line 2.
			-	n.c.
			I	**ENET_RXD2** — Ethernet receive data 2 (MII interface).

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
PC_7[2]	G5	I; PU	I/O	**SDIO_D3** — SD/MMC data bus line 3.
			I/O	**USB1_ULPI_D1** — ULPI link bidirectional data line 1.
			-	n.c.
			I	**ENET_RXD3** — Ethernet receive data 3 (MII interface).
PC_8[2]	N4	I; PU	I	**SDIO_CD** — SD/MMC card detect input.
			I/O	**USB1_ULPI_D0** — ULPI link bidirectional data line 0.
			-	n.c.
			I	**ENET_RX_DV** — Ethernet Receive Data Valid (MII interface).
PC_9[2]	K2	I; PU	O	**SDIO_POW** — <tbd>.
			I	**USB1_ULPI_NXT** — ULPI link NXT signal. Data flow control signal from the PHY.
			-	n.c.
			I	**ENET_RX_ER** — Ethernet receive error (MII interface).
PC_10[2]	M5	I; PU	I/O	**SDIO_CMD** — SD/MMC command signal.
			O	**USB1_ULPI_STP** — ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
			I	**U1_DSR** — Data Set Ready input for UART 1.
			-	n.c.
PC_11[2]	L5	I; PU	I/O	**SDIO_D4** — SD/MMC data bus line 4.
			I	**USB1_ULPI_DIR** — ULPI link DIR signal. Controls the ULP data line direction.
			I	**U1_DCD** — Data Carrier Detect input for UART 1.
			-	n.c.
PC_12[2]	L6	I; PU	I/O	**SDIO_D5** — SD/MMC data bus line 5.
			-	n.c.
			O	**U1_DTR** — Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
			-	n.c.
PC_13[2]	M1	I; PU	I/O	**SDIO_D6** — SD/MMC data bus line 6.
			-	n.c.
			O	**U1_TXD** — Transmitter output for UART 1.
			-	n.c.
PC_14[2]	N1	I; PU	I/O	**SDIO_D7** — SD/MMC data bus line 7.
			-	n.c.
			I	**U1_RXD** — Receiver input for UART 1.
			-	n.c.
PD_0[2]	N2	I; PU	-	n.c.
			O	**CTOUT_15** — SCT output 15. Match output 3 of timer 3.
			O	**EXTBUS_DQMOUT2** — Data mask 2 used with SDRAM and static devices.
			-	n.c.

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Table 963. Pin description *...continued*

Symbol	LBGA256	Reset state [1]	Type	Description
PD_1[2]	P1	I; PU	-	n.c.
			-	n.c.
			O	**EXTBUS_CKEOUT2** — SDRAM clock enable 2.
			-	n.c.
PD_2[2]	R1	I; PU	-	n.c.
			O	**CTOUT_7** — SCT output 7. Match output 3 of timer 1.
			I/O	**EXTBUS_D16** — External memory data line 16.
			-	n.c.
PD_3[2]	P4	I; PU	-	n.c.
			O	**CTOUT_6** — SCT output 7. Match output 2 of timer 1.
			I/O	**EXTBUS_D17** — External memory data line 17.
			-	n.c.
PD_4[2]	T2	I; PU	-	n.c.
			O	**CTOUT_8** — SCT output 8. Match output 0 of timer 2.
			I/O	**EXTBUS_D18** — External memory data line 18.
			-	n.c.
PD_5[2]	P6	I; PU	-	n.c.
			O	**CTOUT_9** — SCT output 9. Match output 1 of timer 2.
			I/O	**EXTBUS_D19** — External memory data line 19.
			-	n.c.
PD_6[2]	R6	I; PU	-	n.c.
			O	**CTOUT_10** — SCT output 10. Match output 2 of timer 2.
			I/O	**EXTBUS_D20** — External memory data line 20.
			-	n.c.
PD_7[2]	T6	I; PU	-	n.c.
			I	**CTIN_5** — SCT input 5. Capture input 2 of timer 2.
			I/O	**EXTBUS_D21** — External memory data line 21.
			-	n.c.
PD_8[2]	P8	I; PU	-	n.c.
			I	**CTIN_6** — SCT input 6. Capture input 1 of timer 3.
			I/O	**EXTBUS_D22** — External memory data line 22.
			-	n.c.
PD_9[2]	T11	I; PU	-	n.c.
			O	**CTOUT_13** — SCT output 13. Match output 1 of timer 3.
			I/O	**EXTBUS_D23** — External memory data line 23.
			-	n.c.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
PD_10[2]	P11	I; PU	-	n.c.
			I	**CTIN_1** — SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
			O	**EXTBUS_BLS3** — LOW active Byte Lane select signal 3.
			-	n.c.
PD_11[2]	N9	I; PU	-	n.c.
			-	n.c.
			O	**EXTBUS_CS3** — LOW active Chip Select 3 signal.
			-	n.c.
PD_12[2]	N11	I; PU	-	n.c.
			-	n.c.
			O	**EXTBUS_CS2** — LOW active Chip Select 2 signal.
			-	n.c.
PD_13[2]	T14	I; PU	-	n.c.
			I	**CTIN_0** — SCT input 0. Capture input 0 of timer 0, 1, 2, 3.
			O	**EXTBUS_BLS2** — LOW active Byte Lane select signal 2.
			-	n.c.
PD_14[2]	R13	I; PU	-	n.c.
			-	n.c.
			O	**EXTBUS_DYCS2** — SDRAM chip select 2.
			-	n.c.
PD_15[2]	T15	I; PU	-	n.c.
			-	n.c.
			I/O	**EXTBUS_A17** — External memory address line 17.
			-	n.c.
PD_16[2]	R14	I; PU	-	n.c.
			-	n.c.
			I/O	**EXTBUS_A16** — External memory address line 16.
			-	n.c.
PE_0[2]	P14	I; PU	-	n.c.
			-	n.c.
			-	n.c.
			I/O	**EXTBUS_A18** — External memory address line 18.
PE_1[2]	N14	I; PU	-	n.c.
			-	n.c.
			-	n.c.
			I/O	**EXTBUS_A19** — External memory address line 19.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
PE_2[2]	M14	I; PU	I	**ADCTRIG0** — ADC trigger input 0.
			I	**CAN1_RD** — CAN1 receiver input.
			-	n.c.
			I/O	**EXTBUS_A20** — External memory address line 20.
PE_3[2]	K12	I; PU	-	n.c.
			O	**CAN1_TD** — CAN1 transmitter output.
			I	**ADCTRIG1** — ADC trigger input 1.
			I/O	**EXTBUS_A21** — External memory address line 21.
PE_4[2]	K13	I; PU	-	n.c.
			I	**NMI** — External interrupt input to NMI.
			-	n.c.
			I/O	**EXTBUS_A22** — External memory address line 22.
PE_5[2]	N16	I; PU	-	n.c.
			O	**CTOUT_3** — SCT output 3. Match output 3 of timer 0.
			O	**U1_RTS** — Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
			I/O	**EXTBUS_D24** — External memory data line 24.
PE_6[2]	M16	I; PU	-	n.c.
			O	**CTOUT_2** — SCT output 2. Match output 2 of timer 0.
			I	**U1_RI** — Ring Indicator input for UART 1.
			I/O	**EXTBUS_D25** — External memory data line 25.
PE_7[2]	F15	I; PU	-	n.c.
			O	**CTOUT_5** — SCT output 5. Match output 1 of timer 1.
			I	**U1_CTS** — Clear to Send input for UART1.
			I/O	**EXTBUS_D26** — External memory data line 26.
PE_8[2]	F14	I; PU	-	n.c.
			O	**CTOUT_4** — SCT output 4. Match output 0 of timer 0.
			I	**U1_DSR** — Data Set Ready input for UART 1.
			I/O	**EXTBUS_D27** — External memory data line 27.
PE_9[2]	E16	I; PU	-	n.c.
			I	**CTIN_4** — SCT input 4. Capture input 2 of timer 1.
			I	**U1_DCD** — Data Carrier Detect input for UART 1.
			I/O	**EXTBUS_D28** — External memory data line 28.
PE_10[2]	E14	I; PU	-	n.c.
			I	**CTIN_3** — SCT input 3. Capture input 1 of timer 1.
			O	**U1_DTR** — Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
			I/O	**EXTBUS_D29** — External memory data line 29.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
PE_11[2]	D16	I; PU	-	n.c.
			O	**CTOUT_12** — SCT output 12. Match output 0 of timer 3.
			O	**U1_TXD** — Transmitter output for UART 1.
			I/O	**EXTBUS_D30** — External memory data line 30.
PE_12[2]	D15	I; PU	-	n.c.
			O	**CTOUT_11** — SCT output 11. Match output 3 of timer 2.
			I	**U1_RXD** — Receiver input for UART 1.
			I/O	**EXTBUS_D31** — External memory data line 31.
PE_13[2]	G14	I; PU	-	n.c.
			O	**CTOUT_14** — SCT output 14. Match output 2 of timer 3.
			I/O	**I2C1_SDA** — I^2C1 data input/output (this pin does not use a specialized I2C pad).
			O	**EXTBUS_DQMOUT3** — Data mask 3 used with SDRAM and static devices.
PE_14[2]	C15	I; PU	-	n.c.
			-	n.c.
			-	n.c.
			O	**EXTBUS_DYCS3** — SDRAM chip select 3.
PE_15[2]	E13	I; PU	-	n.c.
			O	**CTOUT_0** — SCT output 0. Match output 0 of timer 0.
			I/O	**I2C1_SCL** — I^2C1 clock input/output (this pin does not use a specialized I2C pad).
			O	**EXTBUS_CKEOUT3** — SDRAM clock enable 3.
PF_0[2]	D12	I;IA	I/O	**SSP0_SCK** — Serial clock for SSP0.
			-	n.c.
			-	n.c.
			-	n.c.
PF_1[2]	E11	I; PU	-	n.c.
			-	n.c.
			I/O	**SSP0_SSEL** — Slave Select for SSP0.
			-	n.c.
PF_2[2]	D11	I; PU	-	n.c.
			O	**U3_TXD** — Transmitter output for USART3.
			I/O	**SSP0_MISO** — Master In Slave Out for SSP0.
			-	n.c.
PF_3[2]	E10	I; PU	-	n.c.
			I	**U3_RXD** — Receiver input for USART3.
			I/O	**SSP0_MOSI** — Master Out Slave in for SSP0.
			-	n.c.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
PF_4[2]	D10	I;IA	I/O	**SSP1_SCK** — Serial clock for SSP1.
			I	**GP_CLKIN** — General purpose clock input to the CGU.
			O	**TRACECLK** — Trace clock.
			-	n.c.
PF_5[2]	E9	I; PU	-	n.c.
			I/O	**U3_UCLK** — Serial clock input/output for USART3 in synchronous mode.
			I/O	**SSP1_SSEL** — Slave Select for SSP1.
			O	**TRACEDATA[0]** — Trace data, bit 0.
PF_6[2]	E7	I; PU	-	n.c.
			I/O	**U3_DIR** — RS-485/EIA-485 output enable/direction control for USART3.
			I/O	**SSP1_MISO** — Master In Slave Out for SSP1.
			O	**TRACEDATA[1]** — Trace data, bit 1.
PF_7[2]	B7	I; PU	-	n.c.
			I/O	**U3_BAUD** — <tbd> for USART3.
			I/O	**SSP1_MOSI** — Master Out Slave in for SSP1.
			O	**TRACEDATA[2]** — Trace data, bit 2.
PF_8[2]	E6	I; PU	-	n.c.
			I/O	**U0_UCLK** — Serial clock input/output for USART0 in synchronous mode.
			I	**CTIN_2** — SCT input 2. Capture input 2 of timer 0.
			O	**TRACEDATA[3]** — Trace data, bit 3.
PF_9[2]	D6	I; PU	-	n.c.
			I/O	**U0_DIR** — RS-485/EIA-485 output enable/direction control for USART0.
			O	**CTOUT_1** — SCT output 1. Match output 1 of timer 0.
			-	n.c.
PF_10[2]	A3	I; PU	-	n.c.
			O	**U0_TXD** — Transmitter output for USART0.
			I	**SDIO_WP** — SD/MMC card write protect input.
			-	n.c.
PF_11[2]	A2	I; PU	-	n.c.
			I	**U0_RXD** — Receiver input for USART0.
			O	**SDIO_VOLT2** — SD/MMC bus voltage select output 2.
			-	n.c.
Clock pins				
CLK0[4]	N5	O; PU	O	**EXTBUS_CLK0** — SDRAM clock 0.
			O	**CLKOUT** — Clock output pin.
			-	n.c.
			-	n.c.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
CLK1[2]	T10	O; PU	O	**EXTBUS_CLK1** — SDRAM clock 1.
			O	**CLKOUT** — Clock output pin.
			-	n.c.
			-	n.c.
CLK2[2]	D14	O; PU	O	**EXTBUS_CLK3** — SDRAM clock 3.
			O	**CLKOUT** — Clock output pin.
			-	n.c.
			-	n.c.
CLK3[2]	P12	O; PU	O	**EXTBUS_CLK2** — SDRAM clock 2.
			O	**CLKOUT** — Clock output pin.
			-	n.c.
			-	n.c.
Debug pins				**-**
DBGEN[2]	L4	I; PD	I	JTAG interface control signal. Also used for boundary scan.
TCK/SWDCLK[2]	J5	I; F	I	Test Clock for JTAG interface (default) or Serial Wire (SW) clock.
$\overline{\text{TRST}}$[2]	M4	I; PU	I	Test Reset for JTAG interface.
TMS/SWDIO[2]	K6	I; PU	I	Test Mode Select for JTAG interface (default) or SW debug data input/output.
TDO/SWO[2]	K5	O; PU	O	Test Data Out for JTAG interface (default) or SW trace output.
TDI[2]	J4	I; PU	I	Test Data In for JTAG interface.
I^{2}C-bus pins				
I2C0_SCL[8]	L15	I; F	I/O	I^{2}C clock input/output. Open-drain output (for I^{2}C-bus compliance).
I2C0_SDA[8]	L16	I; F	I/O	I^{2}C data input/output. Open-drain output (for I^{2}C-bus compliance).
USB0 pins				
USB0_DP[5]	F2	-	I/O	USB0 bidirectional D+ line.
USB0_DM[5]	G2	-	I/O	USB0 bidirectional D– line.
USB0_VBUS[5]	F1	-	I/O	VBUS pin (power on USB cable).
USB0_ID[6]	H2	-	I	Indicates to the transceiver whether connected a A-device (ID LOW) or B-device (ID HIGH).
USB0_RREF[6]	H1	-	-	USB connection for external reference resistor (12.0 kΩ $\pm$ 1 %) to analog ground supply.
USB1 pins				
USB1_DP[7]	F12	-	I/O	USB1 bidirectional D+ line.
USB1_DM[7]	G12	-	I/O	USB1 bidirectional D– line.
Reset and wake-up pins				
$\overline{\text{RESET}}$[9]	D9	I; IA	I	External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
WAKEUP0	A9	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
WAKEUP1	A10	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.
WAKEUP2	C9	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.
WAKEUP3	D8	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.
ADC pins				
ADC0[6]	E3	I; IA	-	ADC0/1 input channel 0. Shared between ADC0, ADC1, and DAC.
ADC1[6]	C3	I; IA	-	ADC0/1 input channel 1.
ADC2[6]	A4	I; IA	-	ADC0/1 input channel 2.
ADC3[6]	B5	I; IA	-	ADC0/1 input channel 3.
ADC4[6]	C6	I; IA	-	ADC0/1 input channel 4.
ADC5[6]	B3	I; IA	-	ADC0/1 input channel 5.
ADC6[6]	A5	I; IA	-	ADC0/1 input channel 6.
ADC7[6]	C5	I; IA	-	ADC0/1 input channel 7.
RTC				
RTC_ALARM	A11	-	-	RTC controlled output.
RTCX1	A8	-	-	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	B8	-	-	Output from the RTC 32 kHz ultra-low power oscillator circuit.

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
Crystal oscillator pins				
XTAL1[6]	D1	-	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2[6]	E1	-	O	Output from the oscillator amplifier.
Power and ground pins				
USB0_VDDA3V3_ DRIVER	F3	-	-	Separate analog 3.3 V power supply for driver.
USB0_VDDA3V3	G3	-	-	USB 3.3 V separate power supply voltage
USB0_VSSA_TERM	H3	-	-	Dedicated analog ground for clean reference for termination resistors.
USB0_VSSA_REF	G1	-	-	Dedicated clean analog ground for generation of reference currents and voltages.
VDDA	B4	-	-	Analog power supply.
VBAT	B10	-	-	RTC power supply: 3.3 V on this pin supplies power to the RTC.
VDDREG	F10; F9; L8; L7;	-	-	Main regulator power supply
VPP	E8	-	-	OTP programming voltage
VDDIO	F7; J7; N7; L10; E12; N13; L9; H10; G10; D7; J6; F8; K7	-	-	I/O power supply
VSSA	B2	-	-	Ground
VSS	H7; K8; G9; J11; J10	-	-	Ground

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Table 963. Pin description *…continued*

Symbol	LBGA256	Reset state [1]	Type	Description
VSSIO	G6; J8; J9; K9; K10; P7; M13; P13; D13; G8; H8; G7; C4; H9	-	-	Ground
Pins not connected				
-	B9	-	-	n.c.

[1] I = input; O = output; IA = inactive; PU = pull-up enabled; PD = pull-down enabled; F = floating.

[2] Digital I/O pin. Not 5 V tolerant.

[3] Digital I/O pin. 5 V tolerant.

[4] Digital high-speed I/O pin.

[5] 5 V tolerant analog I/O pin.

[6] 3.3 V tolerant analog I/O pin.

[7] 5 V tolerant USB I/O pin.

[8] I^{2}C-bus 5 V tolerant open-drain pin.

[9] Reset input pin; <tbd>.

42.7 LPC1850/30/20/10 Rev ‘-’ SCU

42.7.1 How to read this chapter

The following peripherals are not available on all parts:

- Ethernet: available on LPC1850/30.
- USB0: available on LPC1850/30/20.
- USB1: available on LPC1850/30.

For peripherals not available, the corresponding functions are reserved in the SFSP registers.

42.7.2 Basic configuration

The SCU is configured as follows:

- See Table 901 for clocking and power control.
- The SCU is reset by the SCU_RST (reset # 9).

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Table 964. SCU clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to SCU register interface	BASE_M3_CLK	CLK_M3_SCU	150 MHz

42.7.3 General description

The system control unit determines the function and electrical mode of the digital pins. By default function 0 is selected for all pins with pull-up enabled.

Remark: Analog I/Os for the ADCs and the DAC as well as several USB functions reside on separate pins and are not controlled through the SCU.

42.7.3.1 Digital pin function

The FUNC bits in the SFSX_Y registers control the function of each pin. If the function is GPIO, the GPIOnDIR registers determine whether the pin is configured as an input or output (see Table 280). For any peripheral function, the pin direction is controlled automatically depending on the pin's functionality. The GPIOnDIR registers have no effect for peripheral functions.

42.7.3.2 Digital pin mode

The MODE bits in the SFSX_Y registers allow the selection of on-chip pull-up or pull-down resistors for each pin or select the repeater mode.

The possible on-chip resistor configurations are pull-up enabled, pull-down enabled, or no pull-up/pull-down. The default value is pull-up enabled.

The repeater mode enables the pull-up resistor if the pin is at a logic HIGH and enables the pull-down resistor if the pin is at a logic LOW. This causes the pin to retain its last known state if it is configured as an input and is not driven externally. Repeater mode may typically be used to prevent a pin from floating (and potentially using significant power if it floats to an indeterminate state) if it is temporarily not driven.

42.7.3.3 I^{2}C0-bus pins

The EHS bits of the SFSI2C0 register (Table 968) configure different I^{2}C-modes:

- Standard mode/Fast-mode I^{2}C (this includes an open-drain output according to the I^{2}C-bus specification).
- Fast-mode Plus and High-speed mode with input glitch filter (this includes an open-drain output according to the I^{2}C-bus specification).

42.7.3.4 USB1 DP1/DM1 pins

<tbd>

42.7.3.5 EMC signal delay control

The SCU contains a programmable delay control for all EMC input and output data, address, and control signals. For detail on use of the EMC delay modes, see Table 271.

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42.7.4 Register description

Table 965. Register overview: System Control Unit (SCU) (base address 0x4008 6000)

Name	Access	Address offset	Description	Reset value
Pins P0_n				
SFSP0_0	R/W	0x000	Pin configuration register for pin P0_0	0x00
SFSP0_1	R/W	0x004	Pin configuration register for pin P0_1	0x00
-	-	0x008 - 0x07C	Reserved	-
Pins P1_n				
SFSP1_0	R/W	0x080	Pin configuration register for pin P1_0	0x00
SFSP1_1	R/W	0x084	Pin configuration register for pin P1_1	0x00
SFSP1_2	R/W	0x088	Pin configuration register for pin P1_2	0x00
SFSP1_3	R/W	0x08C	Pin configuration register for pin P1_3	0x00
SFSP1_4	R/W	0x090	Pin configuration register for pin P1_4	0x00
SFSP1_5	R/W	0x094	Pin configuration register for pin P1_5	0x00
SFSP1_6	R/W	0x098	Pin configuration register for pin P1_6	0x00
SFSP1_7	R/W	0x09C	Pin configuration register for pin P1_7	0x00
SFSP1_8	R/W	0x0A0	Pin configuration register for pin P1_8	0x00
SFSP1_9	R/W	0x0A4	Pin configuration register for pin P1_9	0x00
SFSP1_10	R/W	0x0A8	Pin configuration register for pin P1_10	0x00
SFSP1_11	R/W	0x0AC	Pin configuration register for pin P1_11	0x00
SFSP1_12	R/W	0x0B0	Pin configuration register for pin P1_12	0x00
SFSP1_13	R/W	0x0B4	Pin configuration register for pin P1_13	0x00
SFSP1_14	R/W	0x0B8	Pin configuration register for pin P1_14	0x00
SFSP1_15	R/W	0x0BC	Pin configuration register for pin P1_15	0x00
SFSP1_16	R/W	0x0C0	Pin configuration register for pin P1_16	0x00
SFSP1_17	R/W	0x0C4	Pin configuration register for pin P1_17	0x00
SFSP1_18	R/W	0x0C8	Pin configuration register for pin P1_18	0x00
SFSP1_19	R/W	0x0CC	Pin configuration register for pin P1_19	0x00
SFSP1_20	R/W	0x0D0	Pin configuration register for pin P1_20	0x00
-	-	0x0D4 - 0x0FC	Reserved	-
Pins P2_n				
SFSP2_0	R/W	0x100	Pin configuration register for pin P2_0	0x00
SFSP2_1	R/W	0x104	Pin configuration register for pin P2_1	0x00
SFSP2_2	R/W	0x108	Pin configuration register for pin P2_2	0x00
SFSP2_3	R/W	0x10C	Pin configuration register for pin P2_3	0x00
SFSP2_4	R/W	0x110	Pin configuration register for pin P2_4	0x00
SFSP2_5	R/W	0x114	Pin configuration register for pin P2_5	0x00
SFSP2_6	R/W	0x118	Pin configuration register for pin P2_6	0x00
SFSP2_7	R/W	0x11C	Pin configuration register for pin P2_7	0x00

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Table 965. Register overview: System Control Unit (SCU) (base address 0x4008 6000) *…continued*

Name	Access	Address offset	Description	Reset value
SFSP2_8	R/W	0x120	Pin configuration register for pin P2_8	0x00
SFSP2_9	R/W	0x124	Pin configuration register for pin P2_9	0x00
SFSP2_10	R/W	0x128	Pin configuration register for pin P2_10	0x00
SFSP2_11	R/W	0x12C	Pin configuration register for pin P2_11	0x00
SFSP2_12	R/W	0x130	Pin configuration register for pin P2_12	0x00
SFSP2_13	R/W	0x134	Pin configuration register for pin P2_13	0x00
-	-	0x138 - 0x17C	Reserved	-
Pins P3_n				
SFSP3_0	R/W	0x180	Pin configuration register for pin P3_0	0x00
SFSP3_1	R/W	0x184	Pin configuration register for pin P3_1	0x00
SFSP3_2	R/W	0x188	Pin configuration register for pin P3_2	0x00
SFSP3_3	R/W	0x18C	Pin configuration register for pin P3_3	0x00
SFSP3_4	R/W	0x190	Pin configuration register for pin P3_4	0x00
SFSP3_5	R/W	0x194	Pin configuration register for pin P3_5	0x00
SFSP3_6	R/W	0x198	Pin configuration register for pin P3_6	0x00
SFSP3_7	R/W	0x19C	Pin configuration register for pin P3_7	0x00
SFSP3_8	R/W	0x1A0	Pin configuration register for pin P3_8	0x00
-	-	0x1A4 - 0x1FC	Reserved	-
Pins P4_n				
SFSP4_0	R/W	0x200	Pin configuration register for pin P4_0	0x00
SFSP4_1	R/W	0x204	Pin configuration register for pin P4_1	0x00
SFSP4_2	R/W	0x208	Pin configuration register for pin P4_2	0x00
SFSP4_3	R/W	0x20C	Pin configuration register for pin P4_3	0x00
SFSP4_4	R/W	0x210	Pin configuration register for pin P4_4	0x00
SFSP4_5	R/W	0x214	Pin configuration register for pin P4_5	0x00
SFSP4_6	R/W	0x218	Pin configuration register for pin P4_6	0x00
SFSP4_7	R/W	0x21C	Pin configuration register for pin P4_7	0x00
SFSP4_8	R/W	0x220	Pin configuration register for pin P4_8	0x00
SFSP4_9	R/W	0x224	Pin configuration register for pin P4_9	0x00
SFSP4_10	R/W	0x228	Pin configuration register for pin P4_10	0x00
-	-	0x22C - 0x27C	Reserved	-
Pins P5_n				
SFSP5_0	R/W	0x280	Pin configuration register for pin P5_0	0x00
SFSP5_1	R/W	0x284	Pin configuration register for pin P5_1	0x00
SFSP5_2	R/W	0x288	Pin configuration register for pin P5_2	0x00
SFSP5_3	R/W	0x28C	Pin configuration register for pin P5_3	0x00
SFSP5_4	R/W	0x290	Pin configuration register for pin P5_4	0x00

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Table 965. Register overview: System Control Unit (SCU) (base address 0x4008 6000) *…continued*

Name	Access	Address offset	Description	Reset value
SFSP5_5	R/W	0x294	Pin configuration register for pin P5_5	0x00
SFSP5_6	R/W	0x298	Pin configuration register for pin P5_6	0x00
SFSP5_7	R/W	0x29C	Pin configuration register for pin P5_7	0x00
-	-	0x2A0 - 0x2FC	Reserved	-
Pins P6_n				
SFSP6_0	R/W	0x300	Pin configuration register for pin P6_0	0x00
SFSP6_1	R/W	0x304	Pin configuration register for pin P6_1	0x00
SFSP6_2	R/W	0x308	Pin configuration register for pin P6_2	0x00
SFSP6_3	R/W	0x30C	Pin configuration register for pin P6_3	0x00
SFSP6_4	R/W	0x310	Pin configuration register for pin P6_4	0x00
SFSP6_5	R/W	0x314	Pin configuration register for pin P6_5	0x00
SFSP6_6	R/W	0x318	Pin configuration register for pin P6_6	0x00
SFSP6_7	R/W	0x31C	Pin configuration register for pin P6_7	0x00
SFSP6_8	R/W	0x320	Pin configuration register for pin P6_8	0x00
SFSP6_9	R/W	0x324	Pin configuration register for pin P6_9	0x00
SFSP6_10	R/W	0x328	Pin configuration register for pin P6_10	0x00
SFSP6_11	R/W	0x32C	Pin configuration register for pin P6_11	0x00
SFSP6_12	R/W	0x330	Pin configuration register for pin P6_12	0x00
-	-	0x334 - 0x37C	Reserved	-
Pins P7_n				
SFSP7_0	R/W	0x380	Pin configuration register for pin P7_0	0x00
SFSP7_1	R/W	0x384	Pin configuration register for pin P7_1	0x00
SFSP7_2	R/W	0x388	Pin configuration register for pin P7_2	0x00
SFSP7_3	R/W	0x38C	Pin configuration register for pin P7_3	0x00
SFSP7_4	R/W	0x390	Pin configuration register for pin P7_4	0x00
SFSP7_5	R/W	0x394	Pin configuration register for pin P7_5	0x00
SFSP7_6	R/W	0x398	Pin configuration register for pin P7_6	0x00
SFSP7_7	R/W	0x39C	Pin configuration register for pin P7_7	0x00
-	-	0x3A0 - 0x3FC	Reserved	-
Pins P8_n				
SFSP8_0	R/W	0x400	Pin configuration register for pin P8_0	0x00
SFSP8_1	R/W	0x404	Pin configuration register for pin P8_1	0x00
SFSP8_2	R/W	0x408	Pin configuration register for pin P8_2	0x00
SFSP8_3	R/W	0x40C	Pin configuration register for pin P8_3	0x00
SFSP8_4	R/W	0x410	Pin configuration register for pin P8_4	0x00
SFSP8_5	R/W	0x414	Pin configuration register for pin P8_5	0x00
SFSP8_6	R/W	0x418	Pin configuration register for pin P8_6	0x00

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Table 965. Register overview: System Control Unit (SCU) (base address 0x4008 6000) *…continued*

Name	Access	Address offset	Description	Reset value
SFSP8_7	R/W	0x41C	Pin configuration register for pin P8_7	0x00
SFSP8_8	R/W	0x420	Pin configuration register for pin P8_8	0x00
-	-	0x424 - 0x47C	Reserved	-
Pins P9_n				
SFSP9_0	R/W	0x480	Pin configuration register for pin P9_0	0x00
SFSP9_1	R/W	0x484	Pin configuration register for pin P9_1	0x00
SFSP9_2	R/W	0x488	Pin configuration register for pin P9_2	0x00
SFSP9_3	R/W	0x49C	Pin configuration register for pin P9_3	0x00
SFSP9_4	R/W	0x490	Pin configuration register for pin P9_4	0x00
SFSP9_5	R/W	0x494	Pin configuration register for pin P9_5	0x00
SFSP9_6	R/W	0x498	Pin configuration register for pin P9_6	0x00
-	-	0x49C - 0x4FC	Reserved	-
Pins PA_n				
-	R/W	0x500	Reserved	-
SFSPA_1	R/W	0x504	Pin configuration register for pin PA_1	0x00
SFSPA_2	R/W	0x508	Pin configuration register for pin PA_2	0x00
SFSPA_3	R/W	0x50C	Pin configuration register for pin PA_3	0x00
SFSPA_4	R/W	0x510	Pin configuration register for pin PA_4	0x00
-	-	0x514 - 0x57C	Reserved	-
Pins PB_n				
SFSPB_0	R/W	0x580	Pin configuration register for pin PB_0	0x00
SFSPB_1	R/W	0x584	Pin configuration register for pin PB_1	0x00
SFSPB_2	R/W	0x588	Pin configuration register for pin PB_2	0x00
SFSPB_3	R/W	0x58C	Pin configuration register for pin PB_3	0x00
SFSPB_4	R/W	0x590	Pin configuration register for pin PB_4	0x00
SFSPB_5	R/W	0x594	Pin configuration register for pin PB_5	0x00
SFSPB_6	R/W	0x598	Pin configuration register for pin PB_6	0x00
-	-	0x59C - 0x5FC	Reserved	-
Pins PC_n				
SFSPC_0	R/W	0x600	Pin configuration register for pin PC_0	0x00
SFSPC_1	R/W	0x604	Pin configuration register for pin PC_1	0x00
SFSPC_2	R/W	0x608	Pin configuration register for pin PC_2	0x00
SFSPC_3	R/W	0x60C	Pin configuration register for pin PC_3	0x00
SFSPC_4	R/W	0x610	Pin configuration register for pin PC_4	0x00
SFSPC_5	R/W	0x614	Pin configuration register for pin PC_5	0x00
SFSPC_6	R/W	0x618	Pin configuration register for pin PC_6	0x00

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Table 965. Register overview: System Control Unit (SCU) (base address 0x4008 6000) *…continued*

Name	Access	Address offset	Description	Reset value
SFSPC_7	R/W	0x61C	Pin configuration register for pin PC_7	0x00
SFSPC_8	R/W	0x620	Pin configuration register for pin PC_8	0x00
SFSPC_9	R/W	0x624	Pin configuration register for pin PC_9	0x00
SFSPC_10	R/W	0x628	Pin configuration register for pin PC_10	0x00
SFSPC_11	R/W	0x62C	Pin configuration register for pin PC_11	0x00
SFSPC_12	R/W	0x630	Pin configuration register for pin PC_12	0x00
SFSPC_13	R/W	0x634	Pin configuration register for pin PC_13	0x00
SFSPC_14	R/W	0x638	Pin configuration register for pin PC_14	0x00
-	-	0x63C - 0x67C	Reserved	-
Pins PD_n				
SFSPD_0	R/W	0x680	Pin configuration register for pin PD_0	0x00
SFSPD_1	R/W	0x684	Pin configuration register for pin PD_1	0x00
SFSPD_2	R/W	0x688	Pin configuration register for pin PD_2	0x00
SFSPD_3	R/W	0x68C	Pin configuration register for pin PD_3	0x00
SFSPD_4	R/W	0x690	Pin configuration register for pin PD_4	0x00
SFSPD_5	R/W	0x694	Pin configuration register for pin PD_5	0x00
SFSPD_6	R/W	0x698	Pin configuration register for pin PD_6	0x00
SFSPD_7	R/W	0x69C	Pin configuration register for pin PD_7	0x00
SFSPD_8	R/W	0x6A0	Pin configuration register for pin PD_8	0x00
SFSPD_9	R/W	0x6A4	Pin configuration register for pin PD_9	0x00
SFSPD_10	R/W	0x6A8	Pin configuration register for pin PD_10	0x00
SFSPD_11	R/W	0x6AC	Pin configuration register for pin PD_11	0x00
SFSPD_12	R/W	0x6B0	Pin configuration register for pin PD_12	0x00
SFSPD_13	R/W	0x6B4	Pin configuration register for pin PD_13	0x00
SFSPD_14	R/W	0x6B8	Pin configuration register for pin PD_14	0x00
SFSPD_15	R/W	0x6BC	Pin configuration register for pin PD_15	0x00
SFSPD_16	R/W	0x6C0	Pin configuration register for pin PD_16	0x00
-	-	0x6C4 - 0x6FC	Reserved	-
Pins PE_n				
SFSPE_0	R/W	0x700	Pin configuration register for pin PE_0	0x00
SFSPE_1	R/W	0x704	Pin configuration register for pin PE_1	0x00
SFSPE_2	R/W	0x708	Pin configuration register for pin PE_2	0x00
SFSPE_3	R/W	0x70C	Pin configuration register for pin PE_3	0x00
SFSPE_4	R/W	0x710	Pin configuration register for pin PE_4	0x00
SFSPE_5	R/W	0x714	Pin configuration register for pin PE_5	0x00
SFSPE_6	R/W	0x718	Pin configuration register for pin PE_6	0x00
SFSPE_7	R/W	0x71C	Pin configuration register for pin PE_7	0x00
SFSPE_8	R/W	0x720	Pin configuration register for pin PE_8	0x00

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Table 965. Register overview: System Control Unit (SCU) (base address 0x4008 6000) *…continued*

Name	Access	Address offset	Description	Reset value
SFSPE_9	R/W	0x724	Pin configuration register for pin PE_9	0x00
SFSPE_10	R/W	0x728	Pin configuration register for pin PE_10	0x00
SFSPE_11	R/W	0x72C	Pin configuration register for pin PE_11	0x00
SFSPE_12	R/W	0x730	Pin configuration register for pin PE_12	0x00
SFSPE_13	R/W	0x734	Pin configuration register for pin PE_13	0x00
SFSPE_14	R/W	0x738	Pin configuration register for pin PE_14	0x00
SFSPE_15	R/W	0x73C	Pin configuration register for pin PE_15	0x00
-	-	0x740 - 0x77C	Reserved	-
Pins PF_n				
SFSPF_0	R/W	0x780	Pin configuration register for pin PF_0	0x00
SFSPF_1	R/W	0x784	Pin configuration register for pin PF_1	0x00
SFSPF_2	R/W	0x788	Pin configuration register for pin PF_2	0x00
SFSPF_3	R/W	0x78C	Pin configuration register for pin PF_3	0x00
SFSPF_4	R/W	0x790	Pin configuration register for pin PF_4	0x00
SFSPF_5	R/W	0x794	Pin configuration register for pin PF_5	0x00
SFSPF_6	R/W	0x798	Pin configuration register for pin PF_6	0x00
SFSPF_7	R/W	0x79C	Pin configuration register for pin PF_7	0x00
SFSPF_8	R/W	0x7A0	Pin configuration register for pin PF_8	0x00
SFSPF_9	R/W	0x7A4	Pin configuration register for pin PF_9	0x00
SFSPF_10	R/W	0x7A8	Pin configuration register for pin PF_10	0x00
SFSPF_11	R/W	0x7AC	Pin configuration register for pin PF_11	0x00
-	-	0x7B0 - 0xBFC	Reserved	-
CLKn pins				
SFSCLK0	R/W	0xC00	Pin configuration register for pin CLK0	0x00
SFSCLK1	R/W	0xC04	Pin configuration register for pin CLK1	0x00
SFSCLK2	R/W	0xC08	Pin configuration register for pin CLK2	0x00
SFSCLK3	R/W	0xC0C	Pin configuration register for pin CLK3	0x00
-	-	0xC10 - 0xC7C	Reserved	-
USB DP1/DPM pins and I^{2}C-bus open-drain pins				
SFSUSB	R/W	0xC80	Pin configuration register for	0x00
SFSI2C0	R/W	0xC84	Pin configuration register for I^{2}C0-bus pins	0x00
EMC delay registers				
EMCCLKDELAY	R/W	0xD00	EMC clock delay register	
EMCCTRLDELAY	R/W	0xD04	EMC control delay register	
EMCCSLDELAY	R/W	0xD08	EMC chip select delay register	
EMCDOUTDELAY	R/W	0xD0C	EMC data out delay register	

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Table 965. Register overview: System Control Unit (SCU) (base address 0x4008 6000) *…continued*

Name	Access	Address offset	Description	Reset value
EMCFBCLKDELAY	R/W	0xD10	EMC FBCLK delay register	
EMCADDRDELAY0	R/W	0xD14	EMC address line delay register 0	
EMCADDRDELAY1	R/W	0xD18	EMC address line delay register 1	
EMCADDRDELAY2	R/W	0xD1C	EMC address line delay register 2	
-	-	0xD20	Reserved	
EMCDINDELAY	R/W	0xD24	EMC data delay register	

42.7.4.1 Pin configuration registers for pins P0_n to PF_n and CLK0 to CLK3

Each digital pin and each clock pin on the LPC18xx have an associated pin configuration register which determines the pin’s function and input mode. The allowed functions for each pin are listed in Table 963.

Table 966. Pin configuration for pins P0_n to PF_n and CLK0 to CLK3 registers (SFSPY_X, address 0x4008 6000 to 0x4008 6C0C) bit description

Bit	Symbol	Value	Description	Reset value	Access
1:0	SFSP_FUNC		Select pin function	00	R/W
		0x0	Function 0 (default)		
		0x1	Function 1		
		0x2	Function 2		
		0x3	Function 3		
3:2	SFSP_MODE		Input mode	00	R/W
		0x0	Pull-up enabled		
		0x1	Repeater mode		
		0x2	Plain input (pull-up/pull-down disabled)		
		0x3	Pull-down enabled		
31:4	-		Reserved	-	-

42.7.4.2 Pin configuration register for USB1 pins DP1/DM1

Remark: The USB_ESEA bit must be set to 1 if USB1 is used.

Table 967. Pin configuration for pins DP1/DM1 register (SFSUSB, address 0x4008 6C80) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	USB_AIM		Differential data input AIP/AIM 0 = Going LOW with full speed edge rate 1 = Going HIGH with full speed edge rate	0	R/W
		0	Going LOW with full speed edge rate		
		1	Going HIGH with full speed edge rate		

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Table 967. Pin configuration for pins DP1/DM1 register (SFSUSB, address 0x4008 6C80) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
1	USB_ESEA		Control signal for differential input or single input	0	R/W
		0	Reserved. Do not use.		
		1	Single input AIP. Enables USB1.		
31:2	-		Reserved	-	-

42.7.4.3 Pin configuration register for open-drain I²C-bus pins

Table 968. Pin configuration for open-drain I²C-bus pins register (SFSI2C0, address 0x4008 6C84) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	SDA_EHS		Configures I²C0-bus speed for SDA0 pin	0	R/W
		0	Standard/Fast mode (400 kbit/s)		
		1	High-speed mode (3.4 Mbit/s)		
1	SCL_EHS		Configures I²C0-bus speed for SCL0 pin	0	R/W
		0	Standard/Fast mode (400 kbit/s)		
		1	High-speed mode (3.4 Mbit/s)		
2	SCL_ECS		Direction (only applies if SCL_EHS = 1)	0	R/W
		0	Receive		
		1	Transmit		
31:3	-		Reserved	-	-

42.7.4.4 EMC clock delay register

This register provides a programmable delay for the EMC clock outputs. The delay for each clock output is approximately 0.5 ns × CLKn_DELAY or 0.5 ns × CKEn_DELAY. (CLKn_DELAY/CKEn_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

Table 969. EMC clock delay register (EMCCLKDELAY, address 0x4008 6D00) bit description

Bit	Symbol	Description	Reset value	Access
2:0	CLK0_DELAY	Delay of the EXTBUS_CLK0 clock output.	0	R/W
3	-	Reserved.	-	-
6:4	CLK1_DELAY	Delay of the EXTBUS_CLK0 clock output.	0	R/W
7	-	Reserved.	-	-
10:8	CLK2_DELAY	Delay of the EXTBUS_CLK2 clock output.	0	R/W
11	-	Reserved.	-	-
14:12	CLK3_DELAY	Delay of the EXTBUS_CLK3 clock output.	0	R/W
15	-	Reserved.	-	-
18:16	CKE0_DELAY	Delay of the EXTBUS_CKEOUT0 clock enable output.	0	R/W
19	-	Reserved.	-	-
22:20	CKE1_DELAY	Delay of the EXTBUS_CKEOUT1 clock enable output.	0	R/W

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Table 969. EMC clock delay register (EMCCLKDELAY, address 0x4008 6D00) bit description

Bit	Symbol	Description	Reset value	Access
23	-	Reserved.	-	-
26:24	CKE2_DELAY	Delay of the EXTBUS_CKEOUT2 clock enable output.	0	R/W
27	-	Reserved.	-	-
30:28	CKE3_DELAY	Delay of the EXTBUS_CKEOUT3 clock enable output.	0	R/W
31	-	Reserved.	-	-

42.7.4.5 EMC control delay register

This register provides a programmable delay for the EMC control outputs. The delay for each control output is approximately 0.5 ns × XXX_DELAY. (XXX_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

Table 970. EMC control delay register (EMCCTRLDELAY, address 0x4008 6D04) bit description

Bit	Symbol	Description	Reset value	Access
2:0	RAS_DELAY	Delay of the EXTBUS_RAS output.	0	R/W
3	-	Reserved.	-	-
6:4	CAS_DELAY	Delay of the EXTBUS_CAS output.	0	R/W
7	-	Reserved.	-	-
10:8	OE_DELAY	Delay of the EXTBUS_OE output.	0	R/W
11	-	Reserved.	-	-
14:12	WE_DELAY	Delay of the EXTBUS_WE output.	0	R/W
15	-	Reserved.	-	-
18:16	BLS0_DELAY	Delay of the EXTBUS_BLS0 output.	0	R/W
19	-	Reserved.	-	-
22:20	BLS1_DELAY	Delay of the EXTBUS_BLS1 output.	0	R/W
23	-	Reserved.	-	-
26:24	BLS2_DELAY	Delay of the EXTBUS_BLS2 clock enable output.	0	R/W
27	-	Reserved.	-	-
30:28	BLS3_DELAY	Delay of the EXTBUS_BLS3 clock enable output.	0	R/W
31	-	Reserved.	-	-

42.7.4.6 EMC chip select delay register

This register provides a programmable delay for the EMC chip select outputs. The delay for each control output is approximately 0.5 ns × XXX_DELAY. (XXX_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

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Table 971. EMC chip select delay register (EMCCSDELAY, address 0x4008 6D08) bit description

Bit	Symbol	Description	Reset value	Access
2:0	DYCS0_DELAY	Delay of the EXTBUS_DYCS0 output.	0	R/W
3	-	Reserved.	-	-
6:4	DYCS1_DELAY	Delay of the EXTBUS_DYCS1 output.	0	R/W
7	-	Reserved.	-	-
10:8	DYCS2_DELAY	Delay of the EXTBUS_DYCS2 output.	0	R/W
11	-	Reserved.	-	-
14:12	DYCS3_DELAY	Delay of the EXTBUS_DYCS3 output.	0	R/W
15	-	Reserved.	-	-
18:16	CS0_DELAY	Delay of the EXTBUS_CS0 output.	0	R/W
19	-	Reserved.	-	-
22:20	CS1_DELAY	Delay of the EXTBUS_CS1 output.	0	R/W
23	-	Reserved.	-	-
26:24	CS2_DELAY	Delay of the EXTBUS_CS2 clock enable output.	0	R/W
27	-	Reserved.	-	-
30:28	CS3_DELAY	Delay of the EXTBUS_CS3 clock enable output.	0	R/W
31	-	Reserved.	-	-

42.7.4.7 EMC data out delay register

This register provides a programmable delay for the EMC DQM and EMC data outputs (8 data lanes per delay control). The delay for each control output is approximately 0.5 ns × XXX_DELAY. (XXX_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

Table 972. EMC data out delay register (EMCDOUTDELAY, address 0x4008 6D0C) bit description

Bit	Symbol	Description	Reset value	Access
2:0	DQM0_DELAY	Delay of the EXTBUS_DQM0 output.	0	R/W
3	-	Reserved.	-	-
6:4	DQM1_DELAY	Delay of the EXTBUS_DQM1 output.	0	R/W
7	-	Reserved.	-	-
10:8	DQM2_DELAY	Delay of the EXTBUS_DQM2 output.	0	R/W
11	-	Reserved.	-	-
14:12	DQM3_DELAY	Delay of the EXTBUS_DQM3 output.	0	R/W
15	-	Reserved.	-	-
18:16	D0_DELAY	Delay of the EXTBUS_D0 to EXTBUS_D7 outputs.	0	R/W
19	-	Reserved.	-	-
22:20	D1_DELAY	Delay of the EXTBUS_D8 to EXTBUS_D15 outputs.	0	R/W
23	-	Reserved.	-	-
26:24	D2_DELAY	Delay of the EXTBUS_D16 to EXTBUS_D23 outputs.	0	R/W

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Table 972. EMC data out delay register (EMCDOUTDELAY, address 0x4008 6D0C) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
27	-	Reserved.	-	-
30:28	D3_DELAY	Delay of the EXTBUS_D24 to EXTBUS_D31 outputs.	0	R/W
31	-	Reserved.	-	-

42.7.4.8 EMC feedback clock delay register

This register provides a programmable delay for the EMC feedback clocks (8 data lanes per feedback clock). The delay for each control output is approximately 0.5 ns × XXX_DELAY. (XXX_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

Table 973. EMC DQM delay register (EMCFBCLKDELAY, address 0x4008 6D10) bit description

Bit	Symbol	Description	Reset value	Access
2:0	FBCLK0_DELAY	Delay of the EMC feedback clock 0 (for byte lane 0).	0	R/W
3	-	Reserved.	-	-
6:4	FBCLK1_DELAY	Delay of the EMC feedback clock 1 (for byte lane 1).	0	R/W
7	-	Reserved.	-	-
10:8	FBCLK2_DELAY	Delay of the EMC feedback clock 2 (for byte lane 2).	0	R/W
11	-	Reserved.	-	-
14:12	FBCLK3_DELAY	Delay of the EMC feedback clock 3 (for byte lane 3).	0	R/W
15	-	Reserved.	-	-
18:16	CCLK_DELAY	Delay of the EMC CCLKDELAY clock.	0	R/W
31: 19	-	Reserved.	-	-

42.7.4.9 EMC address delay register 0

This register provides a programmable delay for the EMC address outputs. The delay for each control output is approximately 0.5 ns × ADDRn_DELAY. (ADDRn_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

Table 974. EMC address delay register 0 (EMCADDRDELAY0, address 0x4008 6D14) bit description

Bit	Symbol	Description	Reset value	Access
2:0	ADDR0_DELAY	Delay of the EXTBUS_A0 output.	0	R/W
3	-	Reserved.	-	-
6:4	ADDR1_DELAY	Delay of the EXTBUS_A1 output.	0	R/W
7	-	Reserved.	-	-
10:8	ADDR2_DELAY	Delay of the EXTBUS_A2 output.	0	R/W
11	-	Reserved.	-	-
14:12	ADDR3_DELAY	Delay of the EXTBUS_A3 output.	0	R/W
15	-	Reserved.	-	-
18:16	ADDR4_DELAY	Delay of the EXTBUS_A4 output.	0	R/W

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Table 974. EMC address delay register 0 (EMCADDRDELAY0, address 0x4008 6D14) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
19	-	Reserved.	-	-
22:20	ADDR5_DELAY	Delay of the EXTBUS_A5 output.	0	R/W
23	-	Reserved.	-	-
26:24	ADDR6_DELAY	Delay of the EXTBUS_A6 output.	0	R/W
27	-	Reserved.	-	-
30:28	ADDR7_DELAY	Delay of the EXTBUS_A7 output.	0	R/W
31	-	Reserved.	-	-

42.7.4.10 EMC address delay register 1

This register provides a programmable delay for the EMC address outputs. The delay for each control output is approximately 0.5 ns × ADDRn_DELAY. (ADDRn_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

Table 975. EMC address delay register 1 (EMCADDRDELAY1, address 0x4008 6D18) bit description

Bit	Symbol	Description	Reset value	Access
2:0	ADDR8_DELAY	Delay of the EXTBUS_A8 output.	0	R/W
3	-	Reserved.	-	-
6:4	ADDR9_DELAY	Delay of the EXTBUS_A9 output.	0	R/W
7	-	Reserved.	-	-
10:8	ADDR10_DELAY	Delay of the EXTBUS_A10 output.	0	R/W
11	-	Reserved.	-	-
14:12	ADDR11_DELAY	Delay of the EXTBUS_A11 output.	0	R/W
15	-	Reserved.	-	-
18:16	ADDR12_DELAY	Delay of the EXTBUS_A12 output.	0	R/W
19	-	Reserved.	-	-
22:20	ADDR13_DELAY	Delay of the EXTBUS_A13 output.	0	R/W
23	-	Reserved.	-	-
26:24	ADDR14_DELAY	Delay of the EXTBUS_A14 output.	0	R/W
27	-	Reserved.	-	-
30:28	ADDR15_DELAY	Delay of the EXTBUS_A15 output.	0	R/W
31	-	Reserved.	-	-

42.7.4.11 EMC address delay register 2

This register provides a programmable delay for the EMC address outputs. The delay for each control output is approximately 0.5 ns × ADDRn_DELAY. (ADDRn_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

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Table 976. EMC address delay register 2 (EMCADDRDELAY2, address 0x4008 6D1C) bit description

Bit	Symbol	Description	Reset value	Access
2:0	ADDR16_DELAY	Delay of the EXTBUS_A16 output.	0	R/W
3	-	Reserved.	-	-
6:4	ADDR17_DELAY	Delay of the EXTBUS_A17 output.	0	R/W
7	-	Reserved.	-	-
10:8	ADDR18_DELAY	Delay of the EXTBUS_A18 output.	0	R/W
11	-	Reserved.	-	-
14:12	ADDR19_DELAY	Delay of the EXTBUS_A19 output.	0	R/W
15	-	Reserved.	-	-
18:16	ADDR20_DELAY	Delay of the EXTBUS_A20 output.	0	R/W
19	-	Reserved.	-	-
22:20	ADDR21_DELAY	Delay of the EXTBUS_A21 output.	0	R/W
23	-	Reserved.	-	-
26:24	ADDR22_DELAY	Delay of the EXTBUS_A22 output.	0	R/W
27	-	Reserved.	-	-
30:28	ADDR23_DELAY	Delay of the EXTBUS_A23 output.	0	R/W
31	-	Reserved.	-	-

42.7.4.12 EMC data in delay register

This register provides a programmable delay for the EMC data inputs (8 data lanes per delay control). The delay for each control output is approximately 0.5 ns × ADDRn_DELAY. (ADDRn_DELAY = 0x0: delay ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ..., 0x7: delay ≈ 3.5 ns.)

Table 977. EMC data in delay register 3 (EMCDINDELAY, address 0x4008 6D24) bit description

Bit	Symbol	Description	Reset value	Access
2:0	DIN0_DELAY	Delay of the EXTBUS_D0 to EXTBUS_D7 inputs.	0	R/W
3	-	Reserved.	-	-
6:4	DIN1_DELAY	Delay of the EXTBUS_D8 to EXTBUS_D15 inputs.	0	R/W
7	-	Reserved.	-	-
10:8	DIN2_DELAY	Delay of the EXTBUS_D23 to EXTBUS_D16 inputs.	0	R/W
11	-	Reserved.	-	-
14:12	DIN3_DELAY	Delay of the EXTBUS_D31 to EXTBUS_D24 inputs.	0	R/W
15	-	Reserved.	-	-
18:16	DEN0_DELAY	Delay of the data enable lines 0 to 7.	0	R/W
19	-	Reserved.	-	-
22:20	DEN1_DELAY	Delay of the data enable lines 8 to 15.	0	R/W
23	-	Reserved.	-	-
26:24	DEN2_DELAY	Delay of the data enable lines 16 to 23.	0	R/W
31:27	-	Reserved.	-	-

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42.8 LPC1850/30/20/10 Rev '-' GPIO

42.8.1 Basic configuration

The GPIO is configured as follows:

- See Table 978 for clocking and power control.
- The GPIO is reset by a GPIO_RST (reset #28).
- All GPIO pins are set to input by default.

Table 978. GPIO clocking and power control

	Base clock	Branch clock	Maximum frequency
GPIO	BASE_M3_CLK	CLK_M3_GPIO	150 MHz

42.8.2 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.

42.8.3 Pin description

Table 979. GPIO pin description

Pin name	Type	Description
GPIO0_[15:0]	I/O	GPIO port 0, I/Os 15 to 0.
GPIO1_[15:0]	I/O	GPIO port 1, I/Os 15 to 0.
GPIO2_[15:0]	I/O	GPIO port 2, I/Os 15 to 0.
GPIO3_[15:0]	I/O	GPIO port 3, I/Os 15 to 0.
GPIO4_[15:0]	I/O	GPIO port 4, I/Os 15 to 0. GPIO4_11 is not used out.

Remark: The GPIO pins are typically shared with functions of other peripherals.

42.8.4 Register description

The LPC18xx has up to four 32-bit General Purpose I/O ports. For each GPIO port, the first 16 pins are available with the exception of port 4 which does not use GPIO4_11.

The registers are located on the AHB for the fastest possible read and write timing. They can also be accessed as byte or half-word long data. A mask register allows access to a group of bits in a single GPIO port independently from other bits in the same port.

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Table 980. Register overview: GPIO (register base address: 0x400F 0000)

Name	Access	Address offset	Description	Reset value[1]
DIR0	R/W	0x000	GPIO port 0 direction control register.	0x0
-	-	0x004 to 0x00C	Reserved.	-
MASK0	R/W	0x010	GPIO port 0 mask register for port access.	0x0
PIN0	R/W	0x014	GPIO port 0 pin value register using MASK0.	0x0
SET0	R/W	0x018	GPIO port 0 output set register using MASK0. This register controls the state of output pins. Only bits enabled by 0 in MASK0 can be altered.	0x0
CLR0	W	0x01C	GPIO port 0 output clear register using MASK0. This register controls the state of output pins. Only bits enabled by 0 in MASK0 can be altered.	0x0
DIR1	R/W	0x020	GPIO port 1 direction control register.	0x0
-	-	0x024 to 0x02C	Reserved.	-
MASK1	R/W	0x030	GPIO port 1 mask register for port access.	0x0
PIN1	R/W	0x034	GPIO port 1 pin value register using MASK1.	0x0
SET1	R/W	0x038	GPIO port 1 output set register using MASK1. This register controls the state of output pins. Only bits enabled by 0 in MASK1 can be altered.	0x0
CLR1	W	0x03C	GPIO port 1 output clear register using MASK1. This register controls the state of output pins. Only bits enabled by 0 in MASK1 can be altered.	0x0
DIR2	R/W	0x040	GPIO port 2 direction control register.	0x0
-	-	0x044 to 0x04C	Reserved.	-
MASK2	R/W	0x050	GPIO port 2 mask register for port access.	0x0
PIN2	R/W	0x054	GPIO port 2 pin value register using MASK2.	0x0
SET2	R/W	0x058	GPIO port 2 output set register using MASK2. This register controls the state of output pins. Only bits enabled by 0 in MASK2 can be altered.	0x0
CLR2	W	0x05C	GPIO port 2 output clear register using MASK2. This register controls the state of output pins. Only bits enabled by 0 in MASK2 can be altered.	0x0
DIR3	R/W	0x060	GPIO port 3 direction control register.	0x0
-	-	0x064 to 0x06C	Reserved.	-
MASK3	R/W	0x070	GPIO port 3 mask register for port access.	0x0
PIN3	R/W	0x074	GPIO port 3 pin value register using MASK3.	0x0
SET3	R/W	0x078	GPIO port 3 output set register using MASK3. This register controls the state of output pins. Only bits enabled by 0 in MASK3 can be altered.	0x0
CLR3	W	0x07C	GPIO port 3 output clear register using FIO3MASK. This register controls the state of output pins. Only bits enabled by 0 in MASK3 can be altered.	0x0
DIR4	R/W	0x080	GPIO port 4 direction control register.	0x0

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Table 980. Register overview: GPIO (register base address: 0x400F 0000) *…continued*

Name	Access	Address offset	Description	Reset value[1]
-	-	0x084 to 0x08C	Reserved.	-
MASK4	R/W	0x090	GPIO port 4 mask register for port access.	0x0
PIN4	R/W	0x094	GPIO port 4 pin value register using MASK.	0x0
SET4	R/W	0x098	GPIO port 4 output set register using MASK4. This register controls the state of output pins. Only bits enabled by 0 in MASK4 can be altered.	0x0
CLR4	W	0x09C	GPIO port 4 output clear register using MASK4. This register controls the state of output pins. Only bits enabled by 0 in MASK4 can be altered.	0x0

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

42.8.4.1 GPIO port direction register (DIR)

This word accessible register is used to control the direction of the pins when they are configured as GPIO port pins. The direction bit for any pin must be set according to the pin functionality.

Reading returns the status of the DIR register.

Table 981. GPIO port direction register (DIR0 to DIR4 - addresses 0x400F 0000 to 0x400F 0080) bit description

Bit	Symbol	Description	Reset value
15:0	DIRPIN	GPIO direction port x (x = 0 to 4) control bits. Bit 0 controls pin GPIOx_0, bit 15 controls pin GPIOx_15. 0 = Controlled pin is input. 1 = Controlled pin is output.	0x0
31:16	-	Reserved.	-

Aside from the 32-bit long and word only accessible DIR register, every GPIO port can also be controlled via two byte and one half-word accessible register listed in Table 982. Next to providing the same functions as the DIR register, these additional registers allow easier and faster access to the physical port pins.

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Table 982. GPIO port direction control byte and halfword accessible register view

Generic register name	Description	Register length in bits /access	Reset value	Port x register name - address
DIRn_0	GPIO port x (x = 0 to 4) direction control register 0. Bit 0 corresponds to pin GPIOx_0... bit 7 to pin GPIOx_7.	8 (byte)/ R/W	0x00	DIR0_0 - 0x400F 0000 DIR1_0 - 0x400F 0020 DIR2_0 - 0x400F 0040 DIR3_0 - 0x400F 0060 DIR4_0 - 0x00FF 0080
DIRn_1	GPIO port x direction control register 1. Bit 0 corresponds to pin GPIOx_8... bit 7 to pin GPIOx_15.	8 (byte)/ R/W	0x00	DIR0_1 - 0x400F 0001 DIR1_1 - 0x400F 0021 DIR2_1 - 0x400F 0041 DIR3_1 - 0x400F 0061 DIR4_1 - 0x400F 0081
DIRn_L	GPIO port x direction control Lower half-word register. Bit 0 corresponds to pin GPIOx_0... bit 15 to pin GPIOx_15.	16 (half-word)/ R/W	0x0000	DIR0_L - 0x400F 0000 DIR1_L - 0x400F 0020 DIR2_L - 0x400F 0040 DIR3_L - 0x400F 0060 DIR4_L - 0x400F 0080

42.8.4.2 GPIO port mask register (MASK)

This register is used to select port pins that will and will not be affected by write accesses to the SET, CLR, and PIN register. The mask register also filters out the port’s content when the PIN register is read and masks the contents of the SET register for read operations.

A zero in this register’s bit enables an access to the corresponding physical pin via a read or write access. If a bit in this register is one, the corresponding pin will not be changed with write access and if read, will not be reflected in the updated PIN register.

Reading returns the status of the MASK register.

Table 983. GPIO port mask register (MASK0 to MASK4 - addresses 0x400F 0010 to 0x400F 0090) bit description

Bit	Symbol	Description	Reset value
15:0	MASKPIN	GPIO physical pin access control. Bit 0 controls pin GPIOx_0, bit 15 controls pin GPIOx_15. 0 = Controlled pin is affected by writes to the port’s SETn, CLRn, and PINn register(s). Current state of the pin can be read from the PINn register. 1 = Controlled pin is not affected by writes into the port’s SETn, CLRn and PINn register(s). When the PIN register is read, this bit will not be updated with the state of the physical pin.	0x0
31:16	-	Reserved.	-

Aside from the 32-bit long and word only accessible MASKn register, every GPIO port can also be controlled via two byte and one half-word accessible register listed in Table 984. Next to providing the same functions as the MASKn register, these additional registers allow easier and faster access to the physical port pins.

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Table 984. GPIO port mask byte and half-word accessible register description

Generic register name	Description	Register length in bits /access	Reset value	Port x register name - address
MASKn_0	GPIO port x (x = 0 to 4) mask register 0. Bit 0 in corresponds to pin GPIOx_0... bit 7 to pin GPIOx_7.	8 (byte)/ R/W	0x0	MASK0_0 - 0x400F 0010 MASK1_0 - 0x400F 0030 MASK2_0 - 0x400F 0050 MASK3_0 - 0x400F 0070 MASK4_0 - 0x400F 0090
MASKn_1	GPIO port x mask register 1. Bit 0 corresponds to pin GPIOx_8... bit 7 to pin GPIOx_15.	8 (byte)/ R/W	0x0	MASK0_1 - 0x400F 0011 MASK1_1 - 0x400F 0031 MASK2_1 - 0x400F 0051 MASK3_1 - 0400F 0071 MASK4_1 - 0x400F 0091
MASKn_L	GPIO port x mask Lower half-word register. Bit 0 corresponds to pin GPIOx_0... bit 15 to pin GPIOx_15.	16 (half-word)/ R/W	0x0	MASK0_L - 0x400F 0010 MASK1_L - 0x400F 0030 MASK2_L - 0x400F 0050 MASK3_L - 0x400F 0070 MASK4_L - 0x400F 0090

42.8.4.3 GPIO port pin value register (PIN)

Writing to the PIN register stores the value in the port output register, bypassing the need to use both the SET and CLR registers to obtain the entire written value. This feature should be used carefully in an application since it affects the entire port.

This register provides the value of port pins that are configured to perform digital functions. A read of this register yields the logic value of the pin regardless of whether the pin is configured for input or output, as GPIO, or as an alternate digital function. For example, a particular port pin may have GPIO input, GPIO output, UART receive, and PWM output as selectable functions. Any configuration of that pin will allow its current logic state to be read from the corresponding PIN register.

Access to a port pin via the PIN register is masked by the corresponding bit of the MASK register (see Section 42.8.4.2).

Only pins masked with zeros in the Mask register (see Section 42.8.4.2) will be correlated to the current content of the GPIO port pin value register.

Remark: If the PINn register is read, its bit(s) masked with 1 in the MASK register will be set to 0 regardless of the physical pin state.

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Table 985. GPIO port pin value register (PIN0 to PIN0 - addresses 0x400F 0014 to 0x400F 0094) bit description

Bit	Symbol	Description	Reset value
15:0	VALPIN	GPIO output value bits. Bit 0 corresponds to pin GPIOx_0, bit 15 corresponds to pin GPIOx_15. Only bits also set to 0 in the MASKn register are affected by a write or show the pin's actual logic state. 0 = Reading a 0 indicates that the port pin's current state is LOW. Writing 0 sets the output register value to LOW. 1 = Reading a 1 indicates that the port pin's current state is HIGH. Writing a 1 sets the output register value to HIGH.	0x0
31:16	-	Reserved.	-

Aside from the 32-bit long and word only accessible PIN register, every GPIO port can also be controlled via two byte and one half-word accessible register listed in Table 986. Next to providing the same functions as the PIN register, these additional registers allow easier and faster access to the physical port pins.

Table 986. GPIO port pin value byte and half-word accessible register description

Generic register name	Description	Register length in bits /access	Reset value	Port x register name - address
PINn_0	GPIO port x pin value register 0. Bit 0 corresponds to pin GPIOx_0... bit 7 to pin GPIOx_7.	8 (byte)/ R/W	0x00	PIN0_0 - 0x400F 0014 PIN1_0 - 0x400F 0034 PIN2_0 - 0x400F 0054 PIN3_0 - 0x400F 0074 PIN4_0 - 0x400F 0094
PINn_1	GPIO port x pin value register 1. Bit 0 corresponds to pin GPIOx_8... bit 7 to pin GPIOx_15.	8 (byte)/ R/W	0x00	PIN0_1 - 0x400F 0015 PIN1_1 - 0x400F 0035 PIN2_1 - 0x400F 0055 PIN3_1 - 0x400F 0075 PIN4_1 - 0x400F 0095
PINn_L	GPIO port x pin value Lower half-word register. Bit 0 register corresponds to pin GPIOx_0... bit 15 to pin GPIOx_15.	16 (half-word)/ R/W	0x0000	PIN0_L - 0x400F 0014 PIN1_L - 0x400F 0034 PIN2_L - 0x400F 0054 PIN3_L - 0x400F 0074 PIN4_L - 0x400F 0094

42.8.4.4 GPIO port output set register (SET)

SET is used to produce a HIGH level output at the port pins configured as GPIO in output mode. Writing 1 produces a HIGH level at the corresponding port pins. Writing 0 has no effect. If any pin is configured as an input or a secondary function, writing 1 to the corresponding bit in the SET has no effect.

Reading SET returns the value of this register as determined by previous writes to SET and CLR (or PIN as noted above). This value does not reflect the effect of any outside world influence on the I/O pins.

Access to a port pin via the SET register is masked by the corresponding bit of the MASK register (see Section 42.8.4.2).

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Table 987. GPIO port output set register (SET0 to SET4 - addresses 0x400F 0018 to 0x400F 0098) bit description

Bit	Symbol	Description	Reset value
15:0	SETPIN	GPIO output value set bits. Bit 0 controls pin GPIOx_0, bit 15 controls pin GPIOx_15. 0 = Controlled pin output is unchanged. 1 = Controlled pin output is set to HIGH.	0x0
31:16	-	Reserved.	-

Aside from the 32-bit long and word only accessible FIOSET register, every GPIO port can also be controlled via two byte and one half-word accessible register listed in Table 988. Next to providing the same functions as the FIOSET register, these additional registers allow easier and faster access to the physical port pins.

Table 988. GPIO port output set byte and half-word accessible register description

Generic register name	Description	Register length in bits /access	Reset value	Port x register name - address
SETn_0	GPIO port x output set register 0. Bit 0 corresponds to pinGPIOx_0... bit 7 to pin GPIOx_7.	8 (byte)/ R/W	0x00	SET0_0 - 0x400F 0018 SET1_0 - 0x400F 0038 SET2_0 - 0x400F 0058 SET3_0 - 0x400F 0078 SET4_0 - 0x400F 0098
SETn_1	GPIO port x output set register 1. Bit 0 corresponds to pin Px.8... bit 7 to pin Px.15.	8 (byte)/ R/W	0x00	SET0_1 - 0x400F 0019 SET1_1 - 0x400F 0039 SET2_1 - 0x400F 0059 SET3_1 - 0x400F 0079 SET4_1 - 0x400F 0099
SETn_L	GPIO port x output set Lower half-word register. Bit 0 in corresponds to pin GPIOx_0... bit 15 to pin GPIOx_15.	16 (half-word)/ R/W	0x0000	SET0_L - 0x400F 0018 SET1_L - 0x400F 0038 SET2_L - 0x400F 0058 SET3_L - 0x400F 0078 SET4_L - 0x400F 0098

42.8.4.5 GPIO port output clear register (CLR)

FIOCLR is used to produce a LOW level output at port pins configured as GPIO in output mode. Writing 1 produces a LOW level at the corresponding port pin and clears the corresponding bit in the SET register. Writing 0 has no effect. If any pin is configured as an input or a secondary function, writing to CLR has no effect.

The CLR is a write-only register.

Access to a port pin via the FIOCLR register is masked by the corresponding bit of the MASK register (see Section 42.8.4.2).

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Table 989. GPIO port output clear register (CLR0 to CLR4 - 0x400F 001C to 0x400F 009C) bit description

Bit	Symbol	Description	Reset value
15:0	CLRPIN	GPIO output value clear bits. Bit 0 controls pin GPIOx_0, bit 15 controls pin GPIOx_15. 0 = Controlled pin output is unchanged. 1 = Controlled pin output is set to LOW.	0x0
31:16	-	Reserved.	-

Aside from the 32-bit long and word only accessible CLR register, every GPIO port can also be controlled via two byte and one half-word accessible register listed in Table 990. Next to providing the same functions as the CLR register, these additional registers allow easier and faster access to the physical port pins.

Table 990. GPIO port output clear byte and half-word accessible register description

Generic register name	Description	Register length in bits/ access	Reset value	Port x register name - address
CLRn_0	GPIO port x output clear register 0. Bit 0 corresponds to pin GPIOx_0... bit 7 to pin GPIOx_7.	8 (byte)/ W	0x00	CLR0_0 - 0x400F 001C CLR1_0 - 0x400F 003C CLR2_0 - 0x400F 005C CLR3_0 - 0x400F 007C CLR4_0 - 0x400F 009C
CLRn_1	GPIO port x output clear register 1. Bit 0 corresponds to pin GPIOx_8... bit 7 to pin GPIOx_15.	8 (byte)/ W	0x00	CLR0_1 - 0x400F 001D CLR1_1 - 0x400F 003D CLR2_1 - 0x400F 005D CLR3_1 - 0x400F 007D CLR4_1 - 0x400F 009D
CLRn_L	GPIO port x output clear Lower half-word register. Bit 0 corresponds to pin GPIOx_0... bit 15 to pin GPIOx_15.	16 (half-word)/ W	0x0000	CLR0_L - 0x400F 001C CLR1_L - 0x400F 003C CLR2_L - 0x400F 005C CLR3_L - 0x400F 007C CLR4_L - 0x400F 009C

42.9 LPC1850/30/20/10 Rev ‘-’ I2S

42.9.1 How to read this chapter

Remark: This chapter applies to parts LPC1850/30/20/10 Rev ‘-’.

The I^{2}S interface is available on all LPC18xx parts.

42.9.2 Basic configuration

The I^{2}S interface is configured as follows:

- See Table 901 for clocking and power control.
- The I2S is reset by the I2S_RST (reset # 52).
- The I2S interrupt is connected to slot # 28 in the NVIC.

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- For connecting the I2S receive and transmit lines to the GPDMA, use the DMAMUX register in the CREG block (see Table 35) and enable the GPDMA channel in the DMA Channel Configuration registers (Section 16.6.20).
- See Table 37 for interconnections between the I2S transmit/receive lines and the timer and SCT inputs.

Table 991. I2S clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to the I2S register interface and I2S peripheral clock.	BASE_APB1_CLK	CLK_APB1_I2S	150 MHz

42.9.3 Features

The I2S bus provides a standard communication interface for digital audio applications.

The I2S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select signal. The basic I2S connection has one master, which is always the master, and one slave. The I2S interface provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

- The I2S input can operate in both master and slave mode.

  The I2S output can operate in both master and slave mode, independent of the I2S input.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- Versatile clocking includes independent transmit and receive fractional rate generators, and an ability to use a single clock input or output for a 4-wire mode.
- The sampling frequency (fs) can range (in practice) from 16 to 192 kHz. (16, 22.05, 32, 44.1, 48, 96, or 192 kHz) for audio applications.
- Separate Master Clock outputs for both transmit and receive channels support a clock up to 512 times the I^2S sampling frequency.
- Word Select period in master mode is configurable (separately for I^2S input and I^2S output).
- Two 8 word (32 byte) FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the General Purpose DMA block.
- Controls include reset, stop and mute options separately for I2S input and I2S output.

42.9.4 General description

The I2S performs serial data out via the transmit channel and serial data in via the receive channel. These support the NXP Inter IC Audio format for 8-bit, 16-bit and 32-bit audio data, both for stereo and mono modes. Configuration, data access and control is performed by a APB register set. Data streams are buffered by FIFOs with a depth of 8 words.

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The I2S receive and transmit stage can operate independently in either slave or master mode. Within the I2S module the difference between these modes lies in the word select (WS) signal which determines the timing of data transmissions. Data words start on the next falling edge of the transmitting clock after a WS change. In stereo mode when WS is low left data is transmitted and right data when WS is high. In mono mode the same data is transmitted twice, once when WS is low and again when WS is high.

- In master mode, word select is generated internally with a 9-bit counter. The half period count value of this counter can be set in the control register.
- In slave mode, word select is input from the relevant bus pin.
- When an I2S bus is active, the word select, receive clock and transmit clock signals are sent continuously by the bus master, while data is sent continuously by the transmitter.
- Disabling the I2S can be done with the stop or mute control bits separately for the transmit and receive.
- The stop bit will disable accesses by the transmit channel or the receive channel to the FIFOs and will place the transmit channel in mute mode.
- The mute control bit will place the transmit channel in mute mode. In mute mode, the transmit channel FIFO operates normally, but the output is discarded and replaced by zeroes. This bit does not affect the receive channel, data reception can occur normally.

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42.9.5 Pin description

Table 992. Pin description

Pin name	Direction	Description
I2S_RX_SCK	Input/ Output	Receive Clock. A clock signal used to synchronize the transfer of data on the receive channel. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I2S bus specification.
I2S_RX_WS	Input/ Output	Receive Word Select. Selects the channel from which data is to be received. It is driven by the master and received by the slave. Corresponds to the signal WS in the I2S bus specification. WS = 0 indicates that data is being received by channel 1 (left channel). WS = 1 indicates that data is being received by channel 2 (right channel).
I2S_RX_SDA	Input/ Output	Receive Data. Serial data, received MSB first. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the I2S bus specification.
I2S_RX_MCLK	Output	Optional master clock output for the I2S receive function.
I2S_TX_SCK	Input/ Output	Transmit Clock. A clock signal used to synchronize the transfer of data on the transmit channel. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I2S bus specification.
I2S_TX_WS	Input/ Output	Transmit Word Select. Selects the channel to which data is being sent. It is driven by the master and received by the slave. Corresponds to the signal WS in the I2S bus specification. WS = 0 indicates that data is being sent to channel 1 (left channel). WS = 1 indicates that data is being sent to channel 2 (right channel).
I2S_TX_SDA	Input/ Output	Transmit Data. Serial data, sent MSB first. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the I2S bus specification.
IS_TX_MCLK	Output	Optional master clock output for the I2S transmit function.

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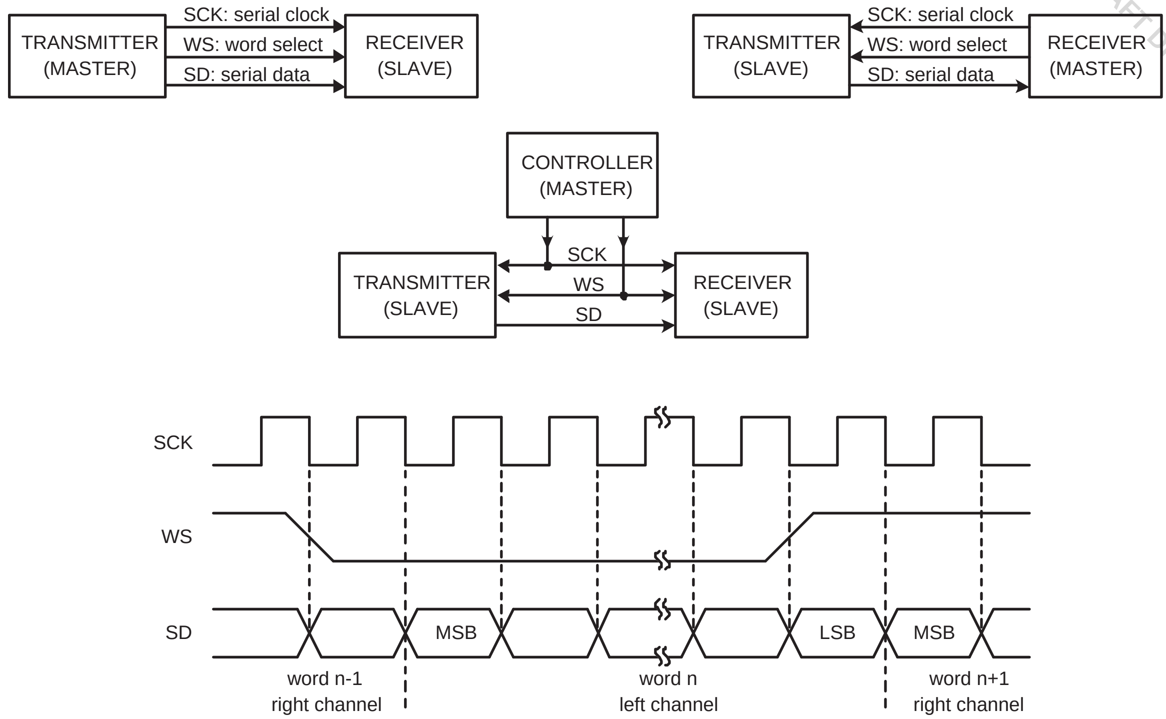


Fig 156. Simple I2S configurations and bus timing

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42.9.6 Register description

Table 993 shows the registers associated with the I2S interface and a summary of their functions. Following the table are details for each register.

Reset value reflects the data stored in used bits only. It does not include reserved bits content.

Table 993. Register overview: I2S (base address 0x400A 2000)

Name	Access	Address offset	Description	Reset value
DAO	R/W	0x000	I2S Digital Audio Output Register. Contains control bits for the I2S transmit channel.	0x87E1
DAI	R/W	0x004	I2S Digital Audio Input Register. Contains control bits for the I2S receive channel.	0x07E1
TXFIFO	WO	0x008	I2S Transmit FIFO. Access register for the 8 x 32-bit transmitter FIFO.	0
RXFIFO	RO	0x00C	I2S Receive FIFO. Access register for the 8 x 32-bit receiver FIFO.	0
STATE	RO	0x010	I2S Status Feedback Register. Contains status information about the I2S interface.	0x7
DMA1	R/W	0x014	I2S DMA Configuration Register 1. Contains control information for DMA request 1.	0
DMA2	R/W	0x018	I2S DMA Configuration Register 2. Contains control information for DMA request 2.	0
IRQ	R/W	0x01C	I2S Interrupt Request Control Register. Contains bits that control how the I2S interrupt request is generated.	0
TXRATE	R/W	0x020	I2S Transmit MCLK divider. This register determines the I2S TX MCLK rate by specifying the value to divide PCLK by in order to produce MCLK.	0
RXRATE	R/W	0x024	I2S Receive MCLK divider. This register determines the I2S RX MCLK rate by specifying the value to divide PCLK by in order to produce MCLK.	0
TXBITRATE	R/W	0x028	I2S Transmit bit rate divider. This register determines the I2S transmit bit rate by specifying the value to divide TX_MCLK by in order to produce the transmit bit clock.	0
RXBITRATE	R/W	0x02C	I2S Receive bit rate divider. This register determines the I2S receive bit rate by specifying the value to divide RX_MCLK by in order to produce the receive bit clock.	0
TXMODE	R/W	0x030	I2S Transmit mode control.	0
RXMODE	R/W	0x034	I2S Receive mode control.	0

42.9.6.1 I2S Digital Audio Output register

The DAO register controls the operation of the I2S transmit channel. The function of bits in DAO are shown in Table 994.

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Table 994. I2S Digital Audio Output register (DAO - address 0x400A 2000) bit description

Bit	Symbol	Value	Description	Reset value
1:0	WORDWIDTH		Selects the number of bytes in data as follows:	01
		0x0	8-bit data	
		0x1	16-bit data	
		0x2	Reserved, do not use this setting	
		0x3	32-bit data	
2	MONO		When 1, data is of monaural format. When 0, the data is in stereo format.	0
3	STOP		When 1, disables accesses on FIFOs, places the transmit channel in mute mode.	0
4	RESET		When 1, asynchronously resets the transmit channel and FIFO.	0
5	WS_SEL		When 0, the interface is in master mode. When 1, the interface is in slave mode. See Section 42.9.7.2 for a summary of useful combinations for this bit with TXMODE.	1
14:6	WS_HALFPERIOD		Word select half period minus 1, i.e. WS 64clk period -> ws_halfperiod = 31.	0x1F
15	MUTE		When 1, the transmit channel sends only zeroes.	1
31:16	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

42.9.6.2 I2S Digital Audio Input register

The DAI register controls the operation of the I2S receive channel. The function of bits in DAI are shown in Table 995.

Table 995. I2S Digital Audio Input register (DAI - address 0x400A 2004) bit description

Bit	Symbol	Value	Description	Reset value
1:0	WORDWIDTH		Selects the number of bytes in data as follows:	01
		0x0	8-bit data	
		0x1	16-bit data	
		0x2	Reserved, do not use this setting	
		0x3	32-bit data	
2	MONO		When 1, data is of monaural format. When 0, the data is in stereo format.	0
3	STOP		When 1, disables accesses on FIFOs, places the transmit channel in mute mode.	0
4	RESET		When 1, asynchronously reset the transmit channel and FIFO.	0
5	WS_SEL		When 0, the interface is in master mode. When 1, the interface is in slave mode. See Section 42.9.7.2 for a summary of useful combinations for this bit with RXMODE.	1
14:6	WS_HALFPERIOD		Word select half period minus 1, i.e. WS 64clk period -> ws_halfperiod = 31.	0x1F
31:15	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

42.9.6.3 I2S Transmit FIFO register

The TXFIFO register provides access to the transmit FIFO. The function of bits in TXFIFO are shown in Table 996.

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Table 996. Transmit FIFO register (TXFIFO - address 0x400A 2008) bit description

Bit	Symbol	Description	Reset value
31:0	I2STXFIFO	8 x 32-bit transmit FIFO.	0

42.9.6.4 Receive FIFO register

The I2SRXFIFO register provides access to the receive FIFO. The function of bits in I2SRXFIFO are shown in Table 997.

Table 997. I2S Receive FIFO register (RXFIFO - address 0x400A 200C) bit description

Bit	Symbol	Description	Reset value
31:0	I2SRXFIFO	8 x 32-bit transmit FIFO.	0

42.9.6.5 I2S Status Feedback register

The STATE register provides status information about the I2S interface. The meaning of bits in STATE are shown in Table 998.

Table 998. I2S Status Feedback register (STATE - address 0x400A 2010) bit description

Bit	Symbol	Description	Reset value
0	IRQ	This bit reflects the presence of Receive Interrupt or Transmit Interrupt. This is determined by comparing the current FIFO levels to the rx_depth_irq and tx_depth_irq fields in the IRQ register.	1
1	DMAREQ1	This bit reflects the presence of Receive or Transmit DMA Request 1. This is determined by comparing the current FIFO levels to the rx_depth_dma1 and tx_depth_dma1 fields in the DMA1 register.	1
2	DMAREQ2	This bit reflects the presence of Receive or Transmit DMA Request 2. This is determined by comparing the current FIFO levels to the rx_depth_dma2 and tx_depth_dma2 fields in the DMA2 register.	1
7:3	-	Reserved.	0
11:8	RX_LEVEL	Reflects the current level of the Receive FIFO.	0
15:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
19:16	TX_LEVEL	Reflects the current level of the Transmit FIFO.	0
31:20	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

42.9.6.6 I2S DMA Configuration Register 1

The DMA1 register controls the operation of DMA request 1. The function of bits in DMA1 are shown in Table 999. Refer to Chapter 16 “LPC18xx General Purpose DMA (GPDMA) controller” for details of DMA operation.

This register enables the DMA for the I^2S receive and transmit channels and sets the FIFO level.

Remark: The FIFOs contain eight 16-bit words. Therefore, if the I^2S controller is configured for 32-bit mode (see Table 994 and Table 995), the maximum allowed FIFO level is 4.

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Table 999. I2S DMA Configuration register 1 (DMA1 - address 0x400A 2014) bit description

Bit	Symbol	Description	Reset value
0	RX_DMA1_ENABLE	When 1, enables DMA1 for I2S receive.	0
1	TX_DMA1_ENABLE	When 1, enables DMA1 for I2S transmit.	0
7:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0
11:8	RX_DEPTH_DMA1	Set the FIFO level that triggers a receive DMA request on DMA1.	0
15:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
19:16	TX_DEPTH_DMA1	Set the FIFO level that triggers a transmit DMA request on DMA1.	0
31:20	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

42.9.6.7 I2S DMA Configuration Register 2

The DMA2 register controls the operation of DMA request 2. The function of bits in DMA2 are shown in Table 994.

This register enables the DMA for the I^{2}S receive and transmit channels and sets the FIFO level.

Remark: The FIFOs contain eight 16-bit words. Therefore, if the I^{2}S controller is configured for 32-bit mode (see Table 994 and Table 995), the maximum allowed FIFO level is 4.

Table 1000. I2S DMA Configuration register 2 (DMA2 - address 0x400A 2018) bit description

Bit	Symbol	Description	Reset value
0	RX_DMA2_ENABLE	When 1, enables DMA1 for I2S receive.	0
1	TX_DMA2_ENABLE	When 1, enables DMA1 for I2S transmit.	0
7:2	-	Reserved.	0
11:8	RX_DEPTH_DMA2	Set the FIFO level that triggers a receive DMA request on DMA2.	0
15:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
19:16	TX_DEPTH_DMA2	Set the FIFO level that triggers a transmit DMA request on DMA2.	0
31:20	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

42.9.6.8 I2S Interrupt Request Control register

The IRQ register controls the operation of the I2S interrupt request. The function of bits in IRQ are shown in Table 994.

Table 1001. I2S Interrupt Request Control register (IRQ - address 0x400A 201C) bit description

Bit	Symbol	Description	Reset value
0	RX_IRQ_ENABLE	When 1, enables I2S receive interrupt.	0
1	TX_IRQ_ENABLE	When 1, enables I2S transmit interrupt.	0
7:2	-	Reserved.	0
11:8	RX_DEPTH_IRQ	Set the FIFO level on which to create an irq request.	0

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Table 1001.I2S Interrupt Request Control register (IRQ - address 0x400A 201C) bit description

Bit	Symbol	Description	Reset value
15:12	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-
19:16	TX_DEPTH_IRQ	Set the FIFO level on which to create an irq request.	0
31:20	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

42.9.6.9 I2S Transmit Clock Rate register

The MCLK rate for the I2S transmitter is determined by the values in the TXRATE register. The required TXRATE setting depends on the desired audio sample rate desired, the format (stereo/mono) used, and the data size.

The transmitter MCLK rate is generated using a fractional rate generator, dividing down the frequency of PCLK_I2S (= CLK_APB1_I2S). Values of the numerator (X) and the denominator (Y) must be chosen to produce a frequency twice that desired for the transmitter MCLK, which must be an integer multiple of the transmitter bit clock rate. Fractional rate generators have some aspects that the user should be aware of when choosing settings. These are discussed in Section 42.9.6.9.1. The equation for the fractional rate generator is:

I2STXMCLK = PCLK_I2S * (X/Y) /2

Note: If the value of X or Y is 0, then no clock is generated. Also, the value of Y must be greater than or equal to X.

Table 1002.I2S Transmit Clock Rate register (TXRATE - address 0x400A 2020) bit description

Bit	Symbol	Description	Reset value
7:0	Y_DIVIDER	I2S transmit MCLK rate denominator. This value is used to divide PCLK to produce the transmit MCLK. Eight bits of fractional divide supports a wide range of possibilities. A value of 0 stops the clock.	0
15:8	X_DIVIDER	I2S transmit MCLK rate numerator. This value is used to multiply PCLK by to produce the transmit MCLK. A value of 0 stops the clock. Eight bits of fractional divide supports a wide range of possibilities. Note: the resulting ratio X/Y is divided by 2.	0
31:16	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

42.9.6.9.1 Notes on fractional rate generators

The nature of a fractional rate generator is that there will be some output jitter with some divide settings. This is because the fractional rate generator is a fully digital function, so output clock transitions are synchronous with the source clock, whereas a theoretical perfect fractional rate may have edges that are not related to the source clock. So, output jitter will not be greater than plus or minus one source clock between consecutive clock edges.

For example, if X = 0x07 and Y = 0x11, the fractional rate generator will output 7 clocks for every 17 (11 hex) input clocks, distributed as evenly as it can. In this example, there is no way to distribute the output clocks in a perfectly even fashion, so some clocks will be longer than others. The output is divided by 2 in order to square it up, which also helps

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with the jitter. The frequency averages out to exactly (7/17) / 2, but some clocks will be a slightly different length than their neighbors. It is possible to avoid jitter entirely by choosing fractions such that X divides evenly into Y, such as 2/4, 2/6, 3/9, 1/N, etc.

42.9.6.10 I2S Receive Clock Rate register

The MCLK rate for the I2S receiver is determined by the values in the RXRATE register. The required RXRATE setting depends on the peripheral clock rate (PCLK_I2S = CLK_APB1_I2S) and the desired MCLK rate (such as 256 fs).

The receiver MCLK rate is generated using a fractional rate generator, dividing down the frequency of PCLK_I2S. Values of the numerator (X) and the denominator (Y) must be chosen to produce a frequency twice that desired for the receiver MCLK, which must be an integer multiple of the receiver bit clock rate. Fractional rate generators have some aspects that the user should be aware of when choosing settings. These are discussed in Section 42.9.6.9.1. The equation for the fractional rate generator is:

I2SRXMCLK = PCLK_I2S * (X/Y) /2

Note: If the value of X or Y is 0, then no clock is generated. Also, the value of Y must be greater than or equal to X.

Table 1003.I2S Receive Clock Rate register (RXRATE - address 0x400A 2024) bit description

Bit	Symbol	Description	Reset value
7:0	Y_DIVIDER	I2S receive MCLK rate denominator. This value is used to divide PCLK to produce the receive MCLK. Eight bits of fractional divide supports a wide range of possibilities. A value of 0 stops the clock.	0
15:8	X_DIVIDER	I2S receive MCLK rate numerator. This value is used to multiply PCLK by to produce the receive MCLK. A value of 0 stops the clock. Eight bits of fractional divide supports a wide range of possibilities. Note: the resulting ratio X/Y is divided by 2.	0
31:16	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

42.9.6.11 I2S Transmit Clock Bit Rate register

The bit rate for the I2S transmitter is determined by the value of the TXBITRATE register. The value depends on the audio sample rate desired, and the data size and format (stereo/mono) used. For example, a 48 kHz sample rate for 16-bit stereo data requires a bit rate of 48,000´16´2 = 1.536 MHz.

Table 1004.I2S Transmit Clock Rate register (TXBITRATE - address 0x400A 2028) bit description

Bit	Symbol	Description	Reset value
5:0	TX_BITRATE	I2S transmit bit rate. This value plus one is used to divide TX_MCLK to produce the transmit bit clock.	0
31:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

42.9.6.12 I2S Receive Clock Bit Rate register

The bit rate for the I2S receiver is determined by the value of the RXBITRATE register. The value depends on the audio sample rate, as well as the data size and format used. The calculation is the same as for RXBITRATE.

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Table 1005.I2S Receive Clock Rate register (RXBITRATE - address 0x400A 202C) bit description

Bit	Symbol	Description	Reset value
5:0	RX_BITRATE	I2S receive bit rate. This value plus one is used to divide RX_MCLK to produce the receive bit clock.	0
31:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

42.9.6.13 I2S Transmit Mode Control register

The Transmit Mode Control register contains additional controls for transmit clock source, enabling the 4-pin mode, and how MCLK is used. See Section 42.9.7.2 for a summary of useful mode combinations.

Table 1006.I2S Transmit Mode Control register (TXMODE - address 0x400A 2030) bit description

Bit	Symbol	Value	Description	Reset value
1:0	TXCLKSEL		Clock source selection for the transmit bit clock divider.	0
		0x0	Select the TX fractional rate divider clock output as the source	
		0x1	Reserved	
		0x2	Select the RX_MCLK signal as the TX_MCLK clock source	
		0x3	Reserved	
2	TX4PIN		Transmit 4-pin mode selection. When 1, enables 4-pin mode.	0
3	TXMCENA		Enable for the TX_MCLK output. When 0, output of TX_MCLK is not enabled. When 1, output of TX_MCLK is enabled.	0
31:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

42.9.6.14 I2S Receive Mode Control register

The Receive Mode Control register contains additional controls for receive clock source, enabling the 4-pin mode, and how MCLK is used. See Section 42.9.7.2 for a summary of useful mode combinations.

Table 1007.I2S Receive Mode Control register (RXMODE - address 0x400A 2034) bit description

Bit	Symbol	Value	Description	Reset value
1:0	RXCLKSEL		Clock source selection for the receive bit clock divider.	0
		0x0	Select the RX fractional rate divider clock output as the source	
		0x1	Reserved	
		0x2	Select the TX_MCLK signal as the RX_MCLK clock source	
		0x3	Reserved	
2	RX4PIN		Receive 4-pin mode selection. When 1, enables 4-pin mode.	0
3	RXMCENA		Enable for the RX_MCLK output. When 0, output of RX_MCLK is not enabled. When 1, output of RX_MCLK is enabled.	0
31:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

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42.9.7 Functional description

42.9.7.1 I²S transmit and receive interfaces

The I2S interface can transmit and receive 8-bit, 16-bit or 32-bit stereo or mono audio information. Some details of I2S implementation are:

- When the FIFO is empty, the transmit channel will repeat transmitting the same data until new data is written to the FIFO.
- When mute is true, the data value 0 is transmitted.
- When mono is false, two successive data words are respectively left and right data.
- Data word length is determined by the wordwidth value in the configuration register. There is a separate wordwidth value for the receive channel and the transmit channel.
  - 0: word is considered to contain four 8-bit data words.
  - 1: word is considered to contain two 16-bit data words.
  - 3: word is considered to contain one 32-bit data word.
- When the transmit FIFO contains insufficient data the transmit channel will repeat transmitting the last data until new data is available. This can occur when the microprocessor or the DMA at some time is unable to provide new data fast enough. Because of this delay in new data there is a need to fill the gap, which is accomplished by continuing to transmit the last sample. The data is not muted as this would produce an noticeable and undesirable effect in the sound.
- The transmit channel and the receive channel only handle 32-bit aligned words, data chunks must be clipped or extended to a multiple of 32 bits.

When switching between data width or modes the I2S must be reset via the reset bit in the control register in order to ensure correct synchronization. It is advisable to set the stop bit also until sufficient data has been written in the transmit FIFO. Note that when stopped data output is muted.

All data accesses to FIFOs are 32 bits. Figure 169 shows the possible data sequences.

A data sample in the FIFO consists of:

- 1´32 bits in 8-bit or 16-bit stereo modes.
- 1´32 bits in mono modes.
- 2´32 bits, first left data, second right data, in 32-bit stereo modes.

Data is read from the transmit FIFO after the falling edge of WS, it will be transferred to the transmit clock domain after the rising edge of WS. On the next falling edge of WS the left data will be loaded in the shift register and transmitted and on the following rising edge of WS the right data is loaded and transmitted.

The receive channel will start receiving data after a change of WS. When word select becomes low it expects this data to be left data, when WS is high received data is expected to be right data. Reception will stop when the bit counter has reached the limit set by wordwidth. On the next change of WS the received data will be stored in the appropriate hold register. When complete data is available it will be written into the receive FIFO.

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42.9.7.2 I²S operating modes

The clocking and WS usage of the I2S interface is configurable. In addition to master and slave modes, which are independently configurable for the transmitter and the receiver, several different clock sources are possible, including variations that share the clock and/or WS between the transmitter and receiver. This last option allows using I2S with fewer pins, typically four.

Many configurations are possible that are not considered useful, the following tables and figures give details of the configurations that are most likely to be useful.

Table 1008. I2S transmit modes

DAO bit 5	TXMODE bits [3:0]	Description
0	0 0 0 0	Typical transmitter master mode. See Figure 157. The I2S transmit function operates as a master. The transmit clock source is the fractional rate divider. The WS used is the internally generated TX_WS. The TX_MCLK pin is not enabled for output.
0	0 0 1 0	Transmitter master mode sharing the receiver reference clock. See Figure 158. The I2S transmit function operates as a master. The transmit clock source is RX_REF. The WS used is the internally generated TX_WS. The TX_MCLK pin is not enabled for output.
0	0 1 0 0	4-wire transmitter master mode sharing the receiver bit clock and WS. See Figure 159. The I2S transmit function operates as a master. The transmit clock source is the RX bit clock. The WS used is the internally generated RX_WS. The TX_MCLK pin is not enabled for output.
0	1 0 0 0	Transmitter master mode with TX_MCLK output. See Figure 157. The I2S transmit function operates as a master. The transmit clock source is the fractional rate divider. The WS used is the internally generated TX_WS. The TX_MCLK pin is enabled for output.
1	0 0 0 0	Typical transmitter slave mode. See Figure 160. The I2S transmit function operates as a slave. The transmit clock source is the TX_SCK pin. The WS used is the TX_WS pin.
1	0 0 1 0	Transmitter slave mode sharing the receiver reference clock. See Figure 161. The I2S transmit function operates as a slave. The transmit clock source is RX_REF. The WS used is the TX_WS pin.
1	0 1 0 0	4-wire transmitter slave mode sharing the receiver bit clock and WS. See Figure 162. The I2S transmit function operates as a slave. The transmit clock source is the RX bit clock. The WS used is RX_WS ref.

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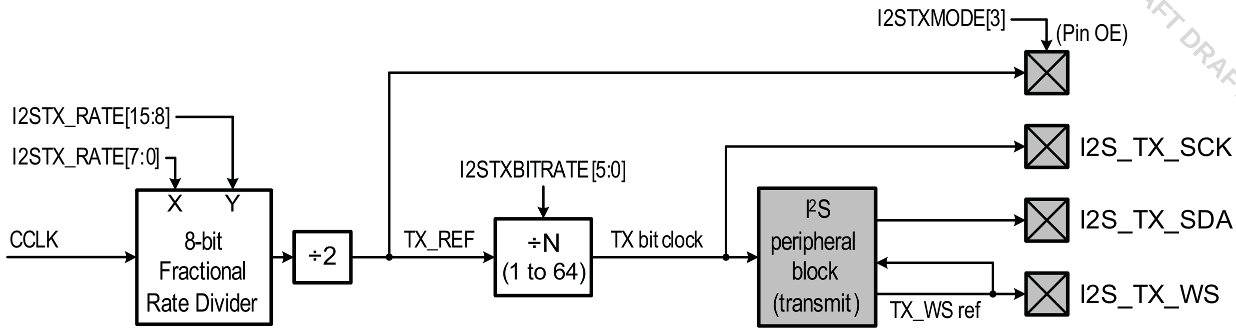


Fig 157. Typical transmitter master mode, with or without MCLK output

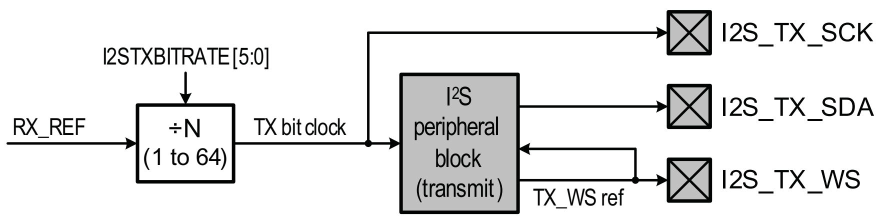


Fig 158. Transmitter master mode sharing the receiver reference clock

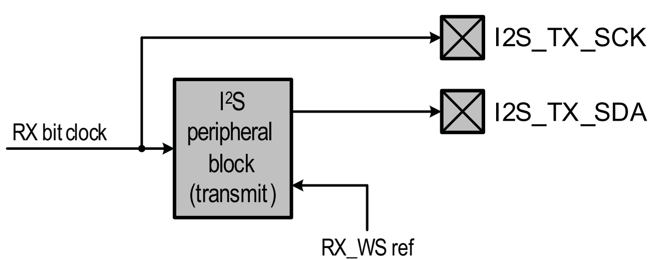


Fig 159. 4-wire transmitter master mode sharing the receiver bit clock and WS

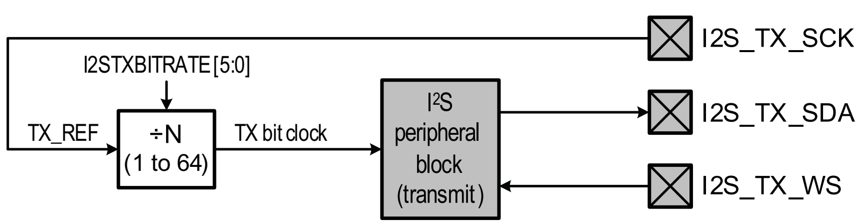


Fig 160. Typical transmitter slave mode

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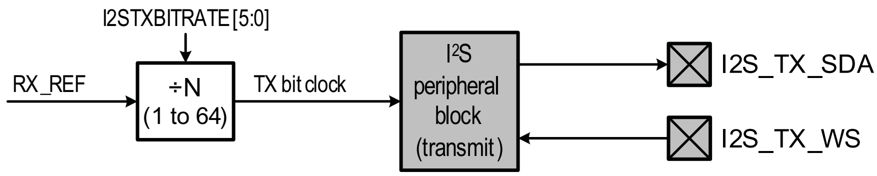


Fig 161. Transmitter slave mode sharing the receiver reference clock

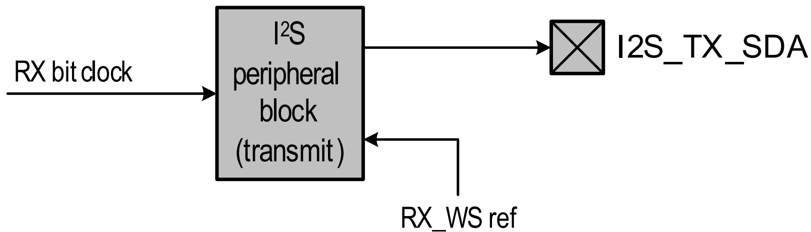


Fig 162. 4-wire transmitter slave mode sharing the receiver bit clock and WS

Table 1009.I2S receive modes

DAI bit 5	RXMODE bit [3:0]	Description
0	0 0 0 0	Typical receiver master mode. See Figure 163. The I2S receive function operates as a master. The receive clock source is the fractional rate divider. The WS used is the internally generated RX_WS. The RX_MCLK pin is not enabled for output.
0	0 0 1 0	Receiver master mode sharing the transmitter reference clock. See Figure 164. The I2S receive function operates as a master. The receive clock source is TX_REF. The WS used is the internally generated RX_WS. The RX_MCLK pin is not enabled for output.
0	0 1 0 0	4-wire receiver master mode sharing the transmitter bit clock and WS. See Figure 165. The I2S receive function operates as a master. The receive clock source is the TX bit clock. The WS used is the internally generated TX_WS. The RX_MCLK pin is not enabled for output.
0	1 0 0 0	Receiver master mode with RX_MCLK output. See Figure 163. The I2S receive function operates as a master. The receive clock source is the fractional rate divider. The WS used is the internally generated RX_WS. The RX_MCLK pin is enabled for output.

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Table 1009.I2S receive modes

DAI bit 5	RXMODE bit [3:0]	Description
1	0 0 0 0	Typical receiver slave mode. See Figure 166. The I2S receive function operates as a slave. The receive clock source is the RX_SCK pin. The WS used is the RX_WS pin.
1	0 0 1 0	Receiver slave mode sharing the transmitter reference clock. See Figure 167. The I2S receive function operates as a slave. The receive clock source is TX_REF. The WS used is the RX_WS pin.
1	0 1 0 0	This is a 4-wire receiver slave mode sharing the transmitter bit clock and WS. See Figure 168. The I2S receive function operates as a slave. The receive clock source is the TX bit clock. The WS used is TX_WS ref.

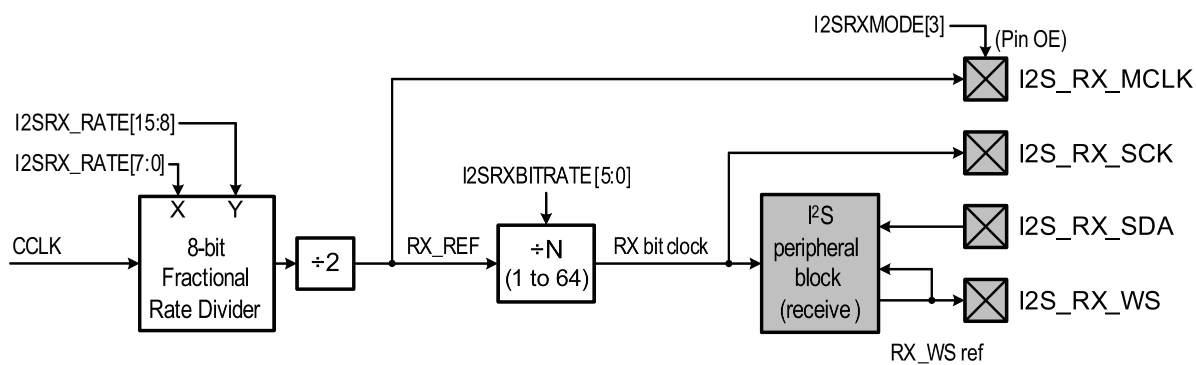


Fig 163. Typical receiver master mode, with or without MCLK output

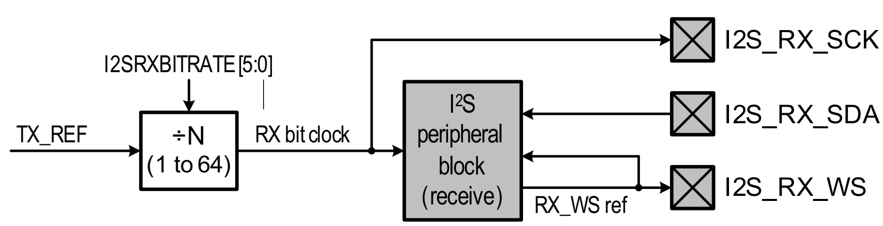


Fig 164. Receiver master mode sharing the transmitter reference clock

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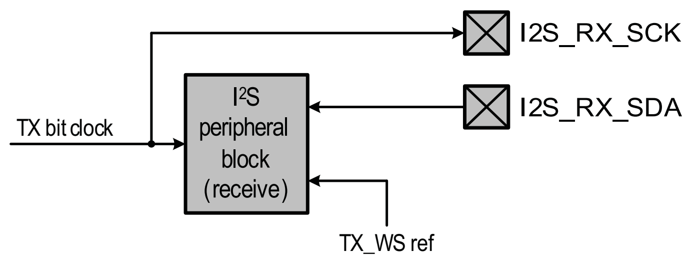


Fig 165. 4-wire receiver master mode sharing the transmitter bit clock and WS

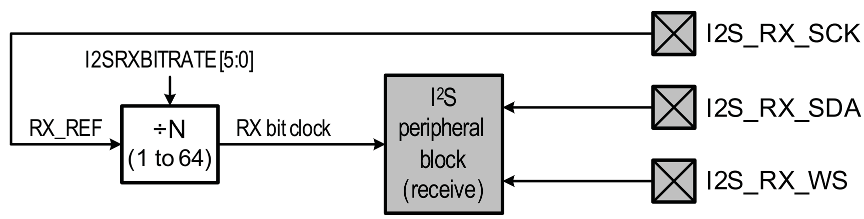


Fig 166. Typical receiver slave mode

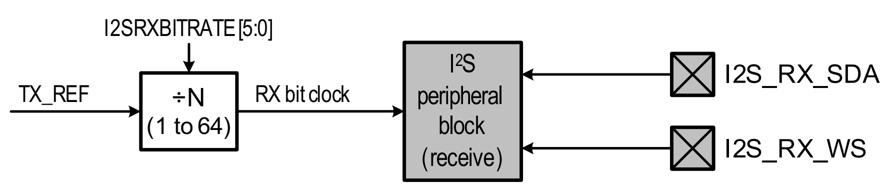


Fig 167. Receiver slave mode sharing the transmitter reference clock

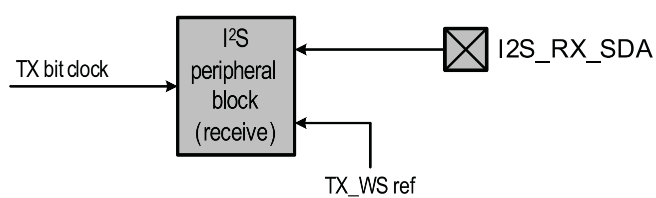


Fig 168. 4-wire receiver slave mode sharing the transmitter bit clock and WS

42.9.7.3 FIFO controller

Handling of data for transmission and reception is performed via the FIFO controller which can generate two DMA requests and an interrupt request. The controller consists of a set of comparators which compare FIFO levels with depth settings contained in registers. The current status of the level comparators can be seen in the APB status register.

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Table 1010. Conditions for FIFO level comparison

Level Comparison	Condition
dmareq_tx_1	tx_depth_dma1 >= tx_level
dmareq_rx_1	rx_depth_dma1 <= rx_level
dmareq_tx_2	tx_depth_dma2 >= tx_level
dmareq_rx_2	rx_depth_dma2 <= rx_level
irq_tx	tx_depth_irq >= tx_level
irq_rx	rx_depth_irq <= rx_level

System signaling occurs when a level detection is true and enabled.

Table 1011. DMA and interrupt request generation

System Signaling	Condition
irq	(irq_rx & rx_irq_enable) | (irq_tx & tx_irq_enable)
dmareq[0]	(dmareq_tx_1 & tx_dma1_enable) | (dmareq_rx_1 & rx_dma1_enable)
dmareq[1]	(dmareq_tx_2 & tx_dma2_enable) | (dmareq_rx_2 & rx_dma2_enable)

Table 1012. Status feedback in the STATE register

Status Feedback	Status
irq	irq_rx | irq_tx
dmareq1	(dmareq_tx_1 | dmareq_rx_1)
dmareq2	(dmareq_rx_2 | dmareq_tx_2)

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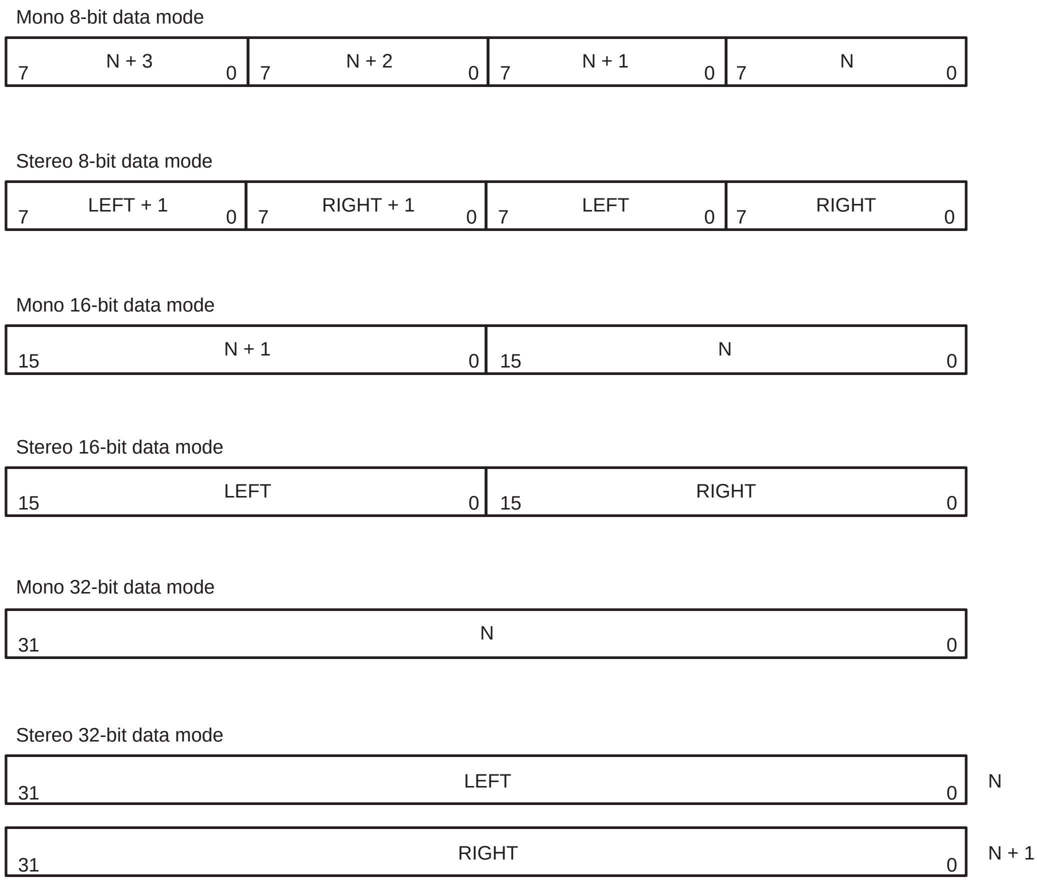


Fig 169. FIFO contents for various I²S modes

42.10 LPC1850/30/20/10 Rev '-' C_CAN

42.10.1 How to read this chapter

The C_CAN controller is available on all LPC18xx parts.

42.10.2 Basic configuration

The C_CAN is configured as follows:

- See Table 901 for clocking and power control.
- The C_CAN is reset by the CAN_RST (reset # 55).
- The C_CAN interrupt is connected to slot # 12 in the Event router.

Table 1013.C_CAN clocking and power control

	Base clock	Branch clock	Maximum frequency
Clock to the C_CAN register interface and C_CAN peripheral clock.	BASE_APB3_CLK	CLK_APB3_CAN	150 MHz

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42.10.3 Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.

42.10.4 General description

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller allows to build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a very high level of security.

The CAN controller consists of a CAN core, message RAM, a message handler, control registers, and the APB interface.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM.

All functions concerning the handling of messages are implemented in the Message Handler. Those functions are the acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the CAN controller can be accessed directly by an external CPU via the APB bus. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

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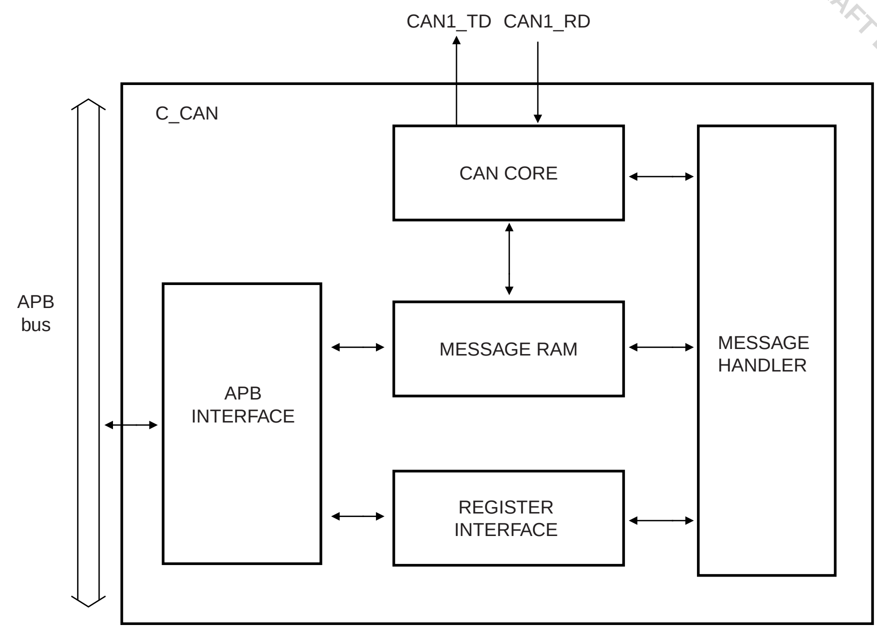


Fig 170. C_CAN block diagram

42.10.5 Pin description

Table 1014. C_CAN pin description

Function pinned out	Direction	Description
CAN_RD	I	C_CAN receive input
CAN_TD	O	C_CAN transmit output

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42.10.6 Register description

Register values at reset

After a hardware reset, the registers hold the values described in Table 904. Additionally, the busoff state is reset and the output TD0,1 is set to recessive (HIGH). The value 0x0001 (INIT = ‘1’) in the CAN Control Register enables the software initialization. The CAN controller does not communicate with the CAN bus until the CPU resets INIT to ‘0’.

The data stored in the message RAM is not affected by a hardware reset. After power-on, the contents of the message RAM is undefined.

Timing of read/write operations

Remark: Reading any of the CAN registers requires **two** consecutive read operations from the same location. Only the data from the **second** read operation are valid.

Successive read operations to the C_CAN registers must be separated by a minimum of (CLKDIVVAL × 2 + 2) × PCLK, where CLKDIVVAL is the can clock divider value and PCLK is the peripheral clock.

Successive write operations to the C_CAN registers must be separated by a minimum of (CLKDIVVAL × 2) × PCLK, where CLKDIVVAL is the can clock divider value and PCLK is the peripheral clock.

Table 1015. Register overview: C_CAN0 (base address 0x400E 2000)

Name	Access	Address offset	Description	Reset value
CNTL		0x000	CAN control	0x0001
STAT		0x004	Status register	0x0000
EC	RO	0x008	Error counter	0x0000
BT		0x00C	Bit timing register	0x2301
INT	RO	0x010	Interrupt register	0x0000
TEST		0x014	Test register	-
BRPE		0x018	Baud rate prescaler extension register	0x0000
-	-	0x01C	Reserved	-
IF1_CMDREQ		0x020	Message interface 1 command request	0x0001
IF1_CMDMSK_W		0x024	Message interface 1 command mask (write direction)	0x0000
IF1_CMDMSK_R		0x024	Message interface 1 command mask (read direction)	0x0000
IF1_MSK1		0x028	Message interface 1 mask 1	0xFFFF
IF1_MSK2		0x02C	Message interface 1 mask 2	0xFFFF
IF1_ARB1		0x030	Message interface 1 arbitration 1	0x0000
IF1_ARB2		0x034	Message interface 1 arbitration 2	0x0000
IF1_MCTRL		0x038	Message interface 1 message control	0x0000
IF1_DA1		0x03C	Message interface 1 data A1	0x0000
IF1_DA2		0x040	Message interface 1 data A2	0x0000
IF1_DB1		0x044	Message interface 1 data B1	0x0000
IF1_DB2		0x048	Message interface 1 data B2	0x0000

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Table 1015.Register overview: C_CAN0 (base address 0x400E 2000)

Name	Access	Address offset	Description	Reset value
-		0x04C - 0x07C	Reserved	-
IF2_CMDREQ		0x080	Message interface 2 command request	0x0001
IF2_CMDMSK		0x084	Message interface 2 command mask	0x0000
IF2_MSK1		0x088	Message interface 2 mask 1	0xFFFF
IF2_MSK2		0x08C	Message interface 2 mask 2	0xFFFF
IF2_ARB1		0x090	Message interface 2 arbitration 1	0x0000
IF2_ARB2		0x094	Message interface 2 arbitration 2	0x0000
IF2_MCTRL		0x098	Message interface 2 message control	0x0000
IF2_DA1		0x09C	Message interface 2 data A1	0x0000
IF2_DA2		0x0A0	Message interface 2 data A2	0x0000
IF2_DB1		0x0A4	Message interface 2 data B1	0x0000
IF2_DB2		0x0A8	Message interface 2 data B2	0x0000
-	-	0x0AC - 0x0FC		
TXREQ1	RO	0x100	Transmission request 1	0x0000
TXREQ2	RO	0x104	Transmission request 2	0x0000
-	-	0x108 - 0x11C	Reserved	-
ND1	RO	0x120	New data 1	0x0000
ND2	RO	0x124	New data 2	0x0000
-	-	0x128 - 0x13C	Reserved	-
IR1	RO	0x140	Interrupt pending 1	0x0000
IR2	RO	0x144	Interrupt pending 2	0x0000
-	-	0x148 - 0x15C	Reserved	-
MSGV1	RO	0x160	Message valid 1	0x0000
MSGV2	RO	0x164	Message valid 2	0x0000
-	-	0x168 - 0x17C	Reserved	-
CLKDIV	R/W	0x180	CAN clock divider register	0x0001

42.10.6.1 CAN protocol registers

42.10.6.1.1 CAN control register

After a hardware reset, the registers of the C_CAN controller hold the values described in Table 904. Additionally, the busoff state is set, and the TD0/1 outputs are set to HIGH. The reset value 0x0001 of the CANCTRL register enables initialization by software (INIT = 1). The C_CAN does not influence the CAN bus until the CPU resets the INIT bit to 0.

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Table 1016. CAN control registers (CNTL, address 0x400E 2000) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	INIT		Initialization	1	R/W
		1	Initialization is started. On reset, software needs to initialize the CAN controller.		
		0	Normal operation.		
1	IE		Module interrupt enable	0	R/W
		1	Enable CAN interrupts. The interrupt line is set to LOW and remains LOW until all pending interrupts are cleared.		
		0	Disable CAN interrupts. The interrupt line is always HIGH.		
2	SIE		Status change interrupt enable	0	R/W
		1	Enable status change interrupts. A status change interrupt will be generated when a message transfer is successfully completed or a CAN bus error is detected.		
		0	Disable status change interrupts. No status change interrupt will be generated.		
3	EIE		Error interrupt enable	0	R/W
		1	Enable error interrupt. A change in the bits BOFF or EWARN in the CANSTAT registers will generate an interrupt.		
		0	Disable error interrupt. No error status interrupt will be generated.		
4	-	-	reserved	0	-
5	DAR		Disable automatic retransmission	0	R/W
		1	Automatic retransmission disabled.		
		0	Automatic retransmission of disturbed messages enabled.		
6	CCE		Configuration change enable	0	R/W
		1	The CPU has write access to the CANBT register while the INIT bit is one.		
		0	The CPU has no write access to the bit timing register.		
7	TEST		Test mode enable	0	R/W
		1	Test mode.		
		0	Normal operation.		
31:8	-		reserved	-	-

Remark: The busoff recovery sequence (see *CAN Specification Rev. 2.0*) cannot be shortened by setting or resetting the INIT bit. If the device goes into busoff state, it will set INIT, stopping all bus activities. Once INIT has been cleared by the CPU, the device will then wait for 129 occurrences of Bus Idle (129 × 11 consecutive HIGH/recessive bits) before resuming normal operations. At the end of the busoff recovery sequence, the Error Management Counters will be reset.

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During the waiting time after the resetting of INIT, each time a sequence of 11 HIGH/recessive bits has been monitored, a Bit0Error code is written to the Status Register CANSTAT, enabling the CPU to monitor the proceeding of the busoff recovery sequence and to determine whether the CAN bus is stuck at LOW/dominant or continuously disturbed.

42.10.6.1.2 CAN status register

Table 1017.CAN status register (STAT, address 0x400E 2004) bit description

Bit	Symbol	Value	Description	Reset value	Access
2:0	LEC		Last error code Type of the last error to occur on the CAN bus.The LEC field holds a code which indicates the type of the last error to occur on the CAN bus. This field will be cleared to ‘0’ when a message has been transferred (reception or transmission) without error. The unused code ‘111’ may be written by the CPU to check for updates.	000	R/W
		0x0	**No error**.		
		0x1	**Stuff error**: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.		
		0x2	**Form error**: A fixed format part of a received frame has the wrong format.		
		0x3	**AckError**: The message this CAN core transmitted was not acknowledged.		
		0x4	**Bit1Error**: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a HIGH/recessive level (bit of logical value ‘1’), but the monitored bus value was LOW/dominant.		
		0x5	**Bit0Error**: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a LOW/dominant level (data or identifier bit logical value ‘0’), but the monitored Bus value was HIGH/recessive. During busoff recovery this status is set each time a sequence of 11 HIGH/recessive bits has been monitored. This enables the CPU to monitor the proceeding of the busoff recovery sequence (indicating the bus is not stuck at LOW/dominant or continuously disturbed).		
		0x6	**CRCError**: The CRC checksum was incorrect in the message received.		
		0x7	**Unused:** No CAN bus event was detected (written by the CPU).		
3	TXOK		Transmitted a message successfully This bit is reset by the CPU. It is never reset by the CAN controller.	0	R/W
		1	Since this bit was last reset by the CPU, a message has been successfully transmitted (error free and acknowledged by at least one other node).		
		0	Since this bit was reset by the CPU, no message has been successfully transmitted.		

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Table 1017.CAN status register (STAT, address 0x400E 2004) bit description
…continued

Bit	Symbol	Value	Description	Reset value	Access
4	RXOK		Received a message successfully This bit is reset by the CPU. It is never reset by the CAN controller.	0	R/W
		1	Since this bit was last set to zero by the CPU, a message has been successfully received independent of the result of acceptance filtering.		
		0	Since this bit was last reset by the CPU, no message has been successfully transmitted.		
5	EPASS		Error passive	0	RO
		1	The CAN controller is in the error passive state as defined in the *CAN 2.0 specification*.		
		0	The CAN controller is in the error active state.		
6	EWARN		Warning status	0	RO
		1	At least one of the error counters in the EML has reached the error warning limit of 96.		
		0	Both error counters are below the error warning limit of 96.		
7	BOFF		Busoff status	0	RO
		1	The CAN controller is in busoff state.		
		0	The CAN module is not in busoff.		
31:8	-	-	reserved		

A status interrupt is generated by bits BOFF, EWARN, RXOK, TXOK, or LEC. BOFF and EWARN generate an error interrupt, and RXOK, TXOK, and LEC generate a status change interrupt if EIE and SIE respectively are set to enabled in the CANCTRL register.

A change of bit EPASS and a write to RXOK, TXOK, or LEC will never create a status interrupt.

Reading the CANSTAT register will clear the Status Interrupt value in the CANIR register.

42.10.6.1.3 CAN error counter

Table 1018.CAN error counter (EC, address 0x400E 2008) bit description

Bit	Symbol	Value	Description	Reset value	Access
7:0	TEC_7_0		Transmit error counter Current value of the transmit error counter (maximum value 127)	0	RO
14:8	REC_6_0		Receive error counter Current value of the receive error counter (maximum value 255).	0	RO
15	RP		Receive error passive	0	RO
		1	The receive counter has reached the error passive level as defined in the *CAN2.0 specification*.		
		0	The receive counter is below the error passive level.		
31:16	-	-	Reserved	-	-

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42.10.6.1.4 CAN bit timing register

Table 1019.CAN bit timing register (BT, address 0x400E 200C) bit description

Bit	Symbol	Description	Reset value	Access
5:0	BRP	Baud rate prescaler The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 63[1]. Valid programmed values are 0x01 - 0x3F[1].	1	R/W
7:6	SJW	(Re)synchronization jump width Valid programmed values are 0 to 3[1].	0	R/w
11:8	TSEG1	Time segment after the sample point Valid values are 0 to 7[1].	0011	R/W
14:12	TSEG2	Time segment before the sample point Valid values are 1 to 15[1].	010	R/W
31:15	-	Reserved	-	-

[1] Hardware interprets the value programmed into these bits as the bit value + 1.

Remark: With a module clock CAN_CLK of 8 MHz, the reset value of 0x2301 configures the C_CAN for a bit rate of 500 kBit/s. The registers are only writable if a configuration change is enabled in CANCTRL and the controller is initialized by software (bits CCE and INIT in the CAN Control Register are set).

42.10.6.1.5 CAN interrupt register

Table 1020.CAN interrupt register (INT, address 0x400E 2010) bit description

Bit	Symbol	Description	Reset value	Access
15:0	INTID15_0	0x0000 = No interrupt is pending 0x0001 to 0x0020 = Number of message object which caused the interrupt. 0x0021 to 0x7FFF = Unused 0x8000 = Status interrupt 0x8001 to 0xFFFF = Unused	0	R
31:16	-	Reserved	-	-

If several interrupts are pending, the CAN Interrupt Register will point to the pending interrupt with the highest priority, disregarding their chronological order. An interrupt remains pending until the CPU has cleared it. If INTID is different from 0x0000 and IE is set, the interrupt line to the CPU is active. The interrupt line remains active until INTID is back to value 0x0000 (the cause of the interrupt is reset) or until IE is reset.

The Status Interrupt has the highest priority. Among the message interrupts, the Message Object’ s interrupt priority decreases with increasing message number.

A message interrupt is cleared by clearing the Message Object’s INTPND bit. The StatusInterrupt is cleared by reading the Status Register.

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42.10.6.1.6 CAN test register

Write access to the Test Register is enabled by setting bit Test in the CAN Control Register.

The different test functions may be combined, but when TX[1:0] ≠ “00” is selected, the message transfer is disturbed.

Table 1021.CAN test register (TEST, address 0x400E 2014) bit description

Bit	Symbol	Value	Description	Reset value	Access
1:0	-	-			-
2	BASIC		Basic mode	0	R/W
		1	IF1 registers used as TX buffer, IF2 registers used as RX buffer.		
		0	Basic mode disabled.		
3	SILENT		Silent mode	0	R/W
		1	The module is in silent mode.		
		0	Normal operation.		
4	LBACK		Loop back mode	0	R/W
		1	Loop back mode is enabled.		
		0	Loop back mode is disabled.		
6:5	TX1_0		Control of TD pins	00	R/W
		0x0	Level at the TD pin is controlled by the CAN controller. This is the value at reset.		
		0x1	The sample point can be monitored at the TD pin.		
		0x2	TD pin is driven LOW/dominant.		
		0x3	TD pin is driven HIGH/recessive.		
7	RX		Monitors the actual value of the RD Pin	0	R
		1	The CAN bus is recessive (RD = 1).		
		0	The CAN bus is dominant (RD = 0).		
31:8	-		Reserved		-

42.10.6.1.7 CAN baud rate prescaler extension register

Table 1022.CAN baud rate prescaler extension register (BRPE, address 0x400E 2018) bit description

Bit	Symbol	Description	Reset value	Access
3:0	BRPE	Baud rate prescaler extension By programming BRPE the Baud Rate Prescaler can be extended to values up to 1023. Hardware interprets the value as the value of BRPE (MSBs) and BRP (LSBs) plus one. Allowed values are 0x00 to 0x0F	0x0000	R/W
31:4	-	Reserved	-	-

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42.10.6.2 Message interface registers

There are two sets of interface registers which are used to control the CPU access to the Message RAM. The interface registers avoid conflicts between CPU access to the Message RAM and CAN message reception and transmission by buffering the data to be transferred. A complete Message Object (see Section 42.10.6.2.1) or parts of the Message Object may be transferred between the Message RAM and the IFx Message Buffer registers in one single transfer.

The function of the two interface register sets is identical (except for test mode Basic). One set of registers may be used for data transfer to the Message RAM while the other set of registers may be used for the data transfer from the Message RAM, allowing both processes to be interrupted by each other.

Each set of interface registers consists of message buffer registers controlled by their own command registers. The command mask register specifies the direction of the data transfer and which parts of a message object will be transferred. The command request register is used to select a message object in the message RAM as target or source for the transfer and to start the action specified in the command mask register.

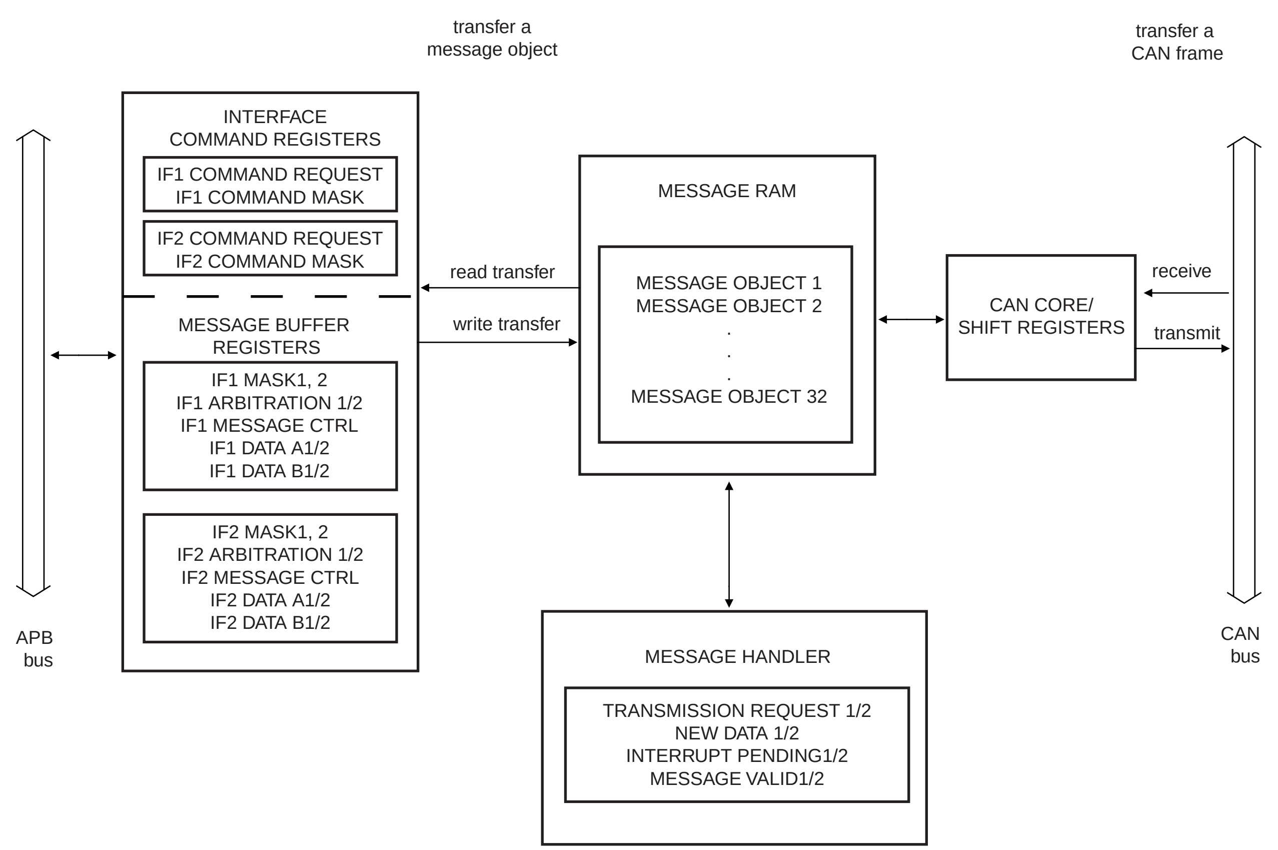


Fig 171. Block diagram of a message object transfer

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Table 1023. Message interface registers

IF1 register names	IF1 register set	IF2 register names	IF2 register set
IF1_CMDREQ	IF1 command request	IF2_CMDREQ	IF2 command request
IF1_CMDMASK	IF1 command mask	IF2_CMDMASK	IF2 command mask
IF1_MASK1	IF1 mask 1	IF2_MSK1	IF2 mask 1
IF1_MASK2	IF1 mask 2	IF2_MSK2	IF2 mask 2
IF1_ARB1	IF1 arbitration 1	IF2_ARB1	IF2 arbitration 1
IF1_ARB2	IF1 arbitration 2	IF2_ARB2	IF2 arbitration 2
IF1_MCTRL	IF1 message control	IF2_MCTRL	IF2 message control
IF1_DA1	IF1 data A1	IF2_DA1	IF2 data A1
IF1_DA2	IF1 data A2	IF2_DA2	IF2 data A2
CIF1_DB1	IF1 data B1	IF2_DB1	IF2 data B1
IF1_DB2	IF1 data B2	IF2_DB2	IF2 data B2

There are 32 Message Objects in the Message RAM. To avoid conflicts between CPU access to the Message RAM and CAN message reception and transmission, the CPU cannot directly access the Message Objects. The message objects are accessed through the IFx Interface Registers.

42.10.6.2.1 Message objects

A message object contains the information from the various bits in the message interface registers. Table 1024 below shows a schematic representation of the structure of the message object. The bits of a message object and the respective interface register where this bit is set or cleared are shown. For bit functions see the corresponding interface register.

Table 1024. Structure of a message object in the message RAM

<table>
<tr><th>UMASK</th><th>MSK[28:0]</th><th>MXTD</th><th>MDIR</th><th>EOB</th><th>NEWDAT</th><th>MSGLST</th><th>RXIE</th><th>TXIE</th><th>INTPND</th></tr>
<tr><td>IF1/2_MCTRL</td><td colspan="3">IF1/2_MSK1/2</td><td colspan="6">IF1/2_MCTRL</td></tr>
<tr><th>RMTEN</th><th>TXRQST</th><th>MSGVAL</th><th>ID[28:0]</th><th>XTD</th><th>DIR</th><th>DLC3</th><th>DLC2</th><th>DLC1</th><th>DLC0</th></tr>
<tr><td colspan="2">IF1/2_MCTRL</td><td colspan="4">IF1/2_ARB1/2</td><td colspan="4">IF1/2_MCTRL</td></tr>
<tr><th>DATA0</th><th>DATA1</th><th>DATA2</th><th>DATA3</th><th>DATA4</th><th>DATA5</th><th>DATA6</th><th colspan="3">DATA7</th></tr>
<tr><td colspan="2">IF1/2_DA1</td><td colspan="2">IF1/2_DA2</td><td colspan="2">IF1/2_DB1</td><td colspan="4">IF1/2_DB2</td></tr>
</table>

42.10.6.2.2 CAN message interface command request registers

A message transfer is started as soon as the CPU has written the message number to the Command Request Register. With this write operation the BUSY bit is automatically set to ‘1’ and the signal CAN_WAIT_B is pulled LOW) to notify the CPU that a transfer is in progress. After a wait time of 3 to 6 CAN_CLK periods, the transfer between the Interface Register and the Message RAM has completed. The BUSY bit is set back to zero and the signal CAN_WAIT_B is set back).

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Table 1025. CAN message interface command request registers (IF1_CMDREQ, address 0x400E 2020 and IF2_CMDREQ, address 0x400E 2080) bit description

Bit	Symbol	Description	Reset value	Access
5:0	Message Number	Message number 0x01 to 0x20 = Valid message numbers The message object in the message RAM is selected for data transfer. 0x00 = Not a valid message number. This value is interpreted as 0x20.[1] 0x21 to 0x3F = Not a valid message number. This value is interpreted as 0x01 - 0x1F.[1]	0x01	R/W
14:6	-	Reserved		
15	BUSY	BUSY flag	0	R
		Set to one by hardware when writing to this Command request register.		
		Set to zero by hardware when read/write action to this Command request register has finished.		
31:16	-	Reserved	-	-

[1] When a message number that is not valid is written into the Command request registers, the message number will be transformed into a valid value and that message object will be transferred.

42.10.6.2.3 CAN message interface command mask registers

The control bits of the IFx Command Mask Register specify the transfer direction and select which of the IFx Message Buffer Registers are source or target of the data transfer.The functions of the register bits depend on the transfer direction (read or write) which is selected in the WR/RD bit (bit 7) of this Command mask register.

Select the WR/RD to

one for the Write transfer direction (write to message RAM)

zero for the Read transfer direction (read from message RAM)

Transfer direction Write

Table 1026. CAN message interface command mask registers write direction (IF1_CMDMSK, address 0x400E 2024 and IF2_CMDMSK, address 0x400E 2084) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	DATA_B		Access data bytes 4-7	0	R/W
		1	Transfer data bytes 4-7 to message object.		
		0	data bytes 4-7 unchanged.		
1	DATA_A		Access data bytes 0-3	0	R/W
		1	Transfer data bytes 0-3 to message object.		
		0	data bytes 0-3 unchanged.		

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Table 1026. CAN message interface command mask registers write direction (IF1_CMDMSK, address 0x400E 2024 and IF2_CMDMSK, address 0x400E 2084) bit description

Bit	Symbol	Value	Description	Reset value	Access
2	TXRQST		Access transmission request bit	0	R/W
		1	Request a transmission. Set the TXRQST bit IF1/2_MCTRL.		
		0	No transmission request. TXRQSRT bit unchanged in IF1/2_MCTRL. **Remark:** If a transmission is requested by programming this bit, the TXRQST bit in the CANIFn_MCTRL register is ignored.		
3	CLRINTPND	-	This bit is ignored in the write direction.	0	R/W
4	CTRL		Access control bits	0	R/W
		1	Transfer control bits to message object		
		0	Control bits unchanged.		
5	ARB		Access arbitration bits	0	R/W
		1	Transfer Identifier, DIR, XTD, and MSGVAL bits to message object.		
		0	Arbitration bits unchanged.		
6	MASK		Access mask bits	0	R/W
		1	Transfer Identifier MASK + MDIR + MXTD to message object.		
		0	Mask bits unchanged.		
7	WR_RD	1	Write transfer Transfer data from the selected message buffer registers to the message object addressed by the command request register CANIFn_CMDREQ.	0	R/W
31:8	-	-	reserved	0	-

Transfer direction Read

Table 1027. CAN message interface command mask registers read direction (IF1_CMDMSK, address 0x400E 2024 and IF2_CMDMSK, address 0x400E 2084) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	DATA_B		Access data bytes 4-7	0	R/W
		1	Transfer data bytes 4-7 to IFx message buffer register.		
		0	data bytes 4-7 unchanged.		
1	DATA_A		Access data bytes 0-3	0	R/W
		1	Transfer data bytes 0-3 to IFx message buffer.		
		0	data bytes 0-3 unchanged.		

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Table 1027.CAN message interface command mask registers read direction (IF1_CMDMSK, address 0x400E 2024 and IF2_CMDMSK, address 0x400E 2084) bit description

Bit	Symbol	Value	Description	Reset value	Access
2	NEWDAT		Access new data bit	0	R/W
		1	Clear NEWDAT bit in the message object.		
		0	NEWDAT bit remains unchanged. **Remark:** A read access to a message object can be combined with the reset of the control bits INTPND and NEWDAT in IF1/2_MCTRL. The values of these bits transferred to the IFx Message Control Register always reflect the status before resetting these bits.		
3	CLRINTPND		Clear interrupt pending bit.	0	R/W
		1	Clear INTPND bit in the message object.		
		0	INTPND bit remains unchanged.		
4	CTRL		Access control bits	0	R/W
		1	Transfer control bits to IFx message buffer.		
		0	Control bits unchanged.		
5	ARB		Access arbitration bits	0	R/W
		1	Transfer Identifier, DIR, XTD, and MSGVAL bits to IFx message buffer register.		
		0	Arbitration bits unchanged.		
6	MASK		Access mask bits	0	R/W
		1	Transfer Identifier MASK + MDIR + MXTD to IFx message buffer register.		
		0	Mask bits unchanged.		
7	WR_RD	0	Read transfer Transfer data from the message object addressed by the command request register to the selected message buffer registers CANIFn_CMDREQ.	0	R/W
31:8	-	-	reserved	0	-

42.10.6.2.4 IF1 and IF2 message buffer registers

The bits of the Message Buffer registers mirror the Message Objects in the Message RAM.

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CAN message interface command mask 1 registers

Table 1028. CAN message interface command mask 1 registers (IF1_MSK1, address 0x400E 2028 and IF2_MSK1, address 0x400E 2088) bit description

Bit	Symbol	Description	Reset value	Access
15:0	MSK15_0	Identifier mask 0 = The corresponding bit in the identifier of the message can not inhibit the match in the acceptance filtering. 1 = The corresponding identifier bit is used for acceptance filtering.	0xFFFF	R/W
31:16	-	reserved	0	-

CAN message interface command mask 2 registers

Table 1029. CAN message interface command mask 2 registers (IF1_MSK2, address 0x400E 202C and IF2_MSK2, 0x400E 208C) bit description

Bit	Symbol	Value	Description	Reset value	Access
12:0	MSK28_16		Identifier mask 0 = The corresponding bit in the identifier of the message can not inhibit the match in the acceptance filtering. 1 = The corresponding identifier bit is used for acceptance filtering.	0xFFF	R/W
13	-		Reserved	1	-
14	MDIR		Mask message direction	1	R/W
		1	The message direction bit (DIR) is used for acceptance filtering.		
		0	The message direction bit (DIR) has no effect on acceptance filtering.		
15	MXTD		Mask extend identifier	1	R/W
		1	The extended identifier bit (IDE) is used for acceptance filtering.		
		0	The extended identifier bit (IDE) has no effect on acceptance filtering.		
31:16	-	-	Reserved	0	-

CAN message interface command arbitration 1 registers

Table 1030. CAN message interface command arbitration 1 registers (IF1_ARB1, address 0x400E 2030 and IF2_ARB1, address 0x400E 2090) bit description

Bit	Symbol	Description	Reset value	Access
15:0	ID15_0	Message identifier 29-bit identifier (“extended frame”) 11-bit identifier (“standard frame”)	0x00	R/W
31:16	-	Reserved	0	-

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CAN message interface command arbitration 2 registers

Table 1031. CAN message interface command arbitration 2 registers (IF1_ARB2, address 0x400E 2034 and IF2_ARB2, address 0x400E 2094) bit description

Bit	Symbol	Value	Description	Reset value	Access
12:0	ID28_16		Message identifier 29-bit identifier (“extended frame”) 11-bit identifier (“standard frame”)	0x00	R/W
13	DIR		Message direction	0x00	R/W
		1	Direction = transmit. On TXRQST, the respective Message Object is transmitted as a Data Frame. On reception of a Remote Frame with matching identifier, the TXRQST bit of this Message Object is set (if RMTEN = one).		
		0	Direction = receive. On TXRQST, a Remote Frame with the identifier of this Message Object is transmitted. On reception of a Data Frame with matching identifier, that message is stored in this Message Object.		
14	XTD		Extend identifier	0x00	R/W
		1	The 29-bit extended identifier will be used for this message object.		
		0	The 11-bit standard identifier will be used for this message object.		
15	MSGVAL		Message valid **Remark:** The MSGVAL bit of all unused Messages Objects is reset during the initialization before bit INIT is reset in the CAN Control Register. This bit must be set to zero before the identifier ID28:0, the control bits XTD, DIR, or the Data Length Code DLC3:0 are modified, or if the Messages Object is no longer required.	0	R/W
		1	The message object is configured and should be considered by the message handler.		
		0	The message object is ignored by the message handler.		
31:16	-	-	Reserved	0	-

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CAN message interface message control registers

Table 1032.CAN message interface message control registers (IF1_MCTRL, address 0x400E 2038 and IF2_MCTRL, address 0x400E 2098) bit description

Bit	Symbol	Value	Description	Reset value	Access
3:0	DLC[3:0]		Data length code **Remark:** The Data Length Code of a Message Object must be defined the same as in all the corresponding objects with the same identifier at other nodes. When the Message Handler stores a data frame, it will write the DLC to the value given by the received message. 0000 to 1000 = Data frame has 0 - 8 data bytes. 1001 to 1111 = Data frame has 8 data bytes.	0000	R/W
6:4	-		reserved	-	-
7	EOB		End of buffer	0	R/W
		1	Single message object or last message object of a FIFO buffer.		
		0	Message object belongs to a FIFO buffer and is not the last message object of that FIFO buffer.		
8	TXRQST		Transmit request	0	R/W
		1	The transmission of this message object is requested and is not yet done		
		0	This message object is not waiting for transmission.		
9	RMTEN		Remote enable	0	R/W
		1	At the reception of a remote frame, TXRQST is set.		
		0	At the reception of a remote frame, TXRQST is left unchanged.		
10	RXIE		Receive interrupt enable	0	R/W
		1	INTPND will be set after successful reception of a frame.		
		0	INTPND will be left unchanged after successful reception of a frame.		
11	TXIE		Transmit interrupt enable	0	R/W
		1	INTPND will be set after a successful reception of a frame.		
		0	The INTPND bit will be left unchanged after a successful reception of a frame.		
12	UMASK		Use acceptance mask **Remark:** If UMASK is set to 1, the message object's mask bits have to be programmed during initialization of the message object before MAGVAL is set to 1.	0	R/W
		1	Use mask (MSK[28:0], MXTD, and MDIR) for acceptance filtering.		
		0	Mask ignored.		

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Table 1032. CAN message interface message control registers (IF1_MCTRL, address 0x400E 2038 and IF2_MCTRL, address 0x400E 2098) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
13	INTPND		Interrupt pending	0	R/W
		1	This message object is the source of an interrupt. The Interrupt Identifier in the Interrupt Register will point to this message object if there is no other interrupt source with higher priority.		
		0	This message object is not the source of an interrupt.		
14	MSGLST		Message lost (only valid for message objects in the direction receive).	0	R/W
		1	The Message Handler stored a new message into this object when NEWDAT was still set, the CPU has lost a message.		
		0	No message lost since this bit was reset last by the CPU.		
15	NEWDAT		New data	0	R/W
		1	The message handler or the CPU has written new data into the data portion of this message object.		
		0	No new data has been written into the data portion of this message object by the message handler since this flag was cleared last by the CPU.		
31:16	-	-	Reserved	0	-

CAN message interface data A1 registers : In a CAN Data Frame, DATA0 is the first, DATA7 (in CAN_IF1B2 AND CAN_IF2B2) is the last byte to be transmitted or received. In CAN's serial bit stream, the MSB of each byte will be transmitted first.

Remark: Byte DATA0 is the first data byte shifted into the shift register of the CAN Core during a reception, byte DATA7 is the last. When the Message Handler stores a Data Frame, it will write all the eight data bytes into a Message Object. If the Data Length Code is less than 8, the remaining bytes of the Message Object will be overwritten by non specified values.

Table 1033. CAN message interface data A1 registers (IF1_DA1, address 0x400E 203C and IF2_DA1, address 0x400E 209C) bit description

Bit	Symbol	Description	Reset value	Access
7:0	DATA0	Data byte 0	0x00	R/W
15:8	DATA1	Data byte 1	0x00	R/W
31:16	-	Reserved	-	-

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CAN message interface data A2 registers

Table 1034. CAN message interface data A2 registers (IF1_DA2, address 0x400E 2040 and IF2_DA2, address 0x400E 20A0) bit description

Bit	Symbol	Description	Reset value	Access
7:0	DATA2	Data byte 2	0x00	R/W
15:8	DATA3	Data byte 3	0x00	R/W
31:16	-	Reserved	-	-

CAN message interface data B1 registers

Table 1035. CAN message interface data B1 registers (IF1_DB1, address 0x400E 2044 and IF2_DB1, address 0x400E 20A4) bit description

Bit	Symbol	Description	Reset value	Access
7:0	DATA4	Data byte 4	0x00	R/W
15:8	DATA5	Data byte 5	0x00	R/W
31:16	-	Reserved	-	-

CAN message interface data B2 registers

Table 1036. CAN message interface data B2 registers (IF1_DB2, address 0x400E 2048 and IF2_DB2, address 0x400E 20A8) bit description

Bit	Symbol	Description	Reset value	Access
7:0	DATA6	Data byte 6	0x00	R/W
15:8	DATA7	Data byte 7	0x00	R/W
31:16	-	Reserved	-	-

42.10.6.3 Message handler registers

All Message Handler registers are read-only. Their contents (TXRQST, NEWDAT, INTPND, and MSGVAL bits of each Message Object and the Interrupt Identifier) is status information provided by the Message Handler FSM.

42.10.6.3.1 CAN transmission request 1 register

This register contains the TXRQST bits of message objects 1 to 16. By reading out the TXRQST bits, the CPU can check for which Message Object a Transmission Request is pending. The TXRQST bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers or by the Message Handler after reception of a Remote Frame or after a successful transmission.

Table 1037. CAN transmission request 1 register (TXREQ1, address 0x400E 2100) bit description

Bit	Symbol	Description	Reset value	Access
15:0	TXRQST16_1	Transmission request bit of message objects 16 to 1. 0 = This message object is not waiting for transmission. 1 = The transmission of this message object is requested and not yet done.	0x00	R
31:16	-	Reserved	-	-

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42.10.6.3.2 CAN transmission request 2 register

This register contains the TXRQST bits of message objects 32 to 17. By reading out the TXRQST bits, the CPU can check for which Message Object a Transmission Request is pending. The TXRQST bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers or by the Message Handler after reception of a Remote Frame or after a successful transmission.

Table 1038.CAN transmission request 2 register (TXREQ2, address 0x400E 2104) bit description

Bit	Symbol	Description	Reset value	Access
15:0	TXRQST32_17	Transmission request bit of message objects 32 to 17. 0 = This message object is not waiting for transmission. 1 = The transmission of this message object is requested and not yet done.	0x00	R
31:16	-	Reserved	-	-

42.10.6.3.3 CAN new data 1 register

This register contains the NEWDAT bits of message objects 16 to 1. By reading out the NEWDAT bits, the CPU can check for which Message Object the data portion was updated. The NEWDAT bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers or by the Message Handler after reception of a Data Frame or after a successful transmission.

Table 1039.CAN new data 1 register (ND1, address 0x400E 2120) bit description

Bit	Symbol	Description	Reset value	Access
15:0	NEWDAT16_1	New data bits of message objects 16 to 1. 0 = No new data has been written into the data portion of this Message Object by the Message Handler since last time this flag was cleared by the CPU. 1 = The Message Handler or the CPU has written new data into the data portion of this Message Object.	0x00	R
31:16	-	Reserved	-	-

42.10.6.3.4 CAN new data 2 register

This register contains the NEWDAT bits of message objects 32 to 17. By reading out the NEWDAT bits, the CPU can check for which Message Object the data portion was updated. The NEWDAT bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers or by the Message Handler after reception of a Data Frame or after a successful transmission.

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Table 1040.CAN new data 2 register (ND2, address 0x400E 2124) bit description

Bit	Symbol	Description	Reset value	Access
15:0	NEWDAT32_17	New data bits of message objects 32 to 17. 0 = No new data has been written into the data portion of this Message Object by the Message Handler since last time this flag was cleared by the CPU. 1 = The Message Handler or the CPU has written new data into the data portion of this Message Object.	0x00	R
31:16	-	Reserved	-	-

42.10.6.3.5 CAN interrupt pending 1 register

This register contains the INTPND bits of message objects 16 to 1. By reading out the INTPND bits, the CPU can check for which Message Object an interrupt is pending. The INTPND bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers or by the Message Handler after reception or after a successful transmission of a frame. This will also affect the value of INTPND in the Interrupt Register.

Table 1041.CAN interrupt pending 1 register (IR1, address 0x400E 2140) bit description

Bit	Symbol	Description	Reset value	Access
15:0	INTPND16_1	Interrupt pending bits of message objects 16 to 1. 0 = This message object is ignored by the message handler. 1 = This message object is the source of an interrupt.	0x00	R
31:16	-	Reserved	-	-

42.10.6.3.6 CAN interrupt pending 2 register

This register contains the INTPND bits of message objects 32 to 17. By reading out the INTPND bits, the CPU can check for which Message Object an interrupt is pending. The INTPND bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers or by the Message Handler after reception or after a successful transmission of a frame. This will also affect the value of INTPND in the Interrupt Register.

Table 1042.CAN interrupt pending 2 register (IR2, addresses 0x400E 2144) bit description

Bit	Symbol	Description	Reset value	Access
15:0	INTPND32_17	Interrupt pending bits of message objects 32 to 17. 0 = This message object is ignored by the message handler. 1 = This message object is the source of an interrupt.	0x00	R
31:16	-	Reserved	-	-

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42.10.6.3.7 CAN message valid 1 register

This register contains the MSGVAL bits of message objects 16 to 1. By reading out the MSGVAL bits, the CPU can check which Message Object is valid. The MSGVAL bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers.

Table 1043. CAN message valid 1 register (MSGV1, addresses 0x400E 2160) bit description

Bit	Symbol	Description	Reset value	Access
15:0	MSGVAL16_1	Message valid bits of message objects 16 to 1. 0 = This message object is ignored by the message handler. 1 = This message object is configured and should be considered by the message handler.	0x00	R
31:16	-	Reserved	-	-

42.10.6.3.8 CAN message valid 2 register

This register contains the MSGVAL bits of message objects 32 to 17. By reading out the MSGVAL bits, the CPU can check which Message Object is valid. The MSGVAL bit of a specific Message Object can be set/reset by the CPU via the IFx Message Interface Registers.

Table 1044. CAN message valid 2 register (MSGV2, address 0x400E 2164) bit description

Bit	Symbol	Description	Access	Reset value
15:0	MSGVAL32_17	Message valid bits of message objects 32 to 17. 0 = This message object is ignored by the message handler. 1 = This message object is configured and should be considered by the message handler.	R	0x00
31:16	-	Reserved	-	-

42.10.6.4 CAN timing register

42.10.6.4.1 CAN clock divider register

This register determines the CAN clock signal. The CAN_CLK is derived from the peripheral clock PCLK divided by the values in this register.

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Table 1045.CAN clock divider register (CLKDIV, address 0x400E 2180) bit description

Bit	Symbol	Description	Reset value	Access
3:0	CLKDIVVAL	Clock divider value CAN_CLK = PCLK/($2^{CLKDIVVAL\ -1}$+1) 0000: CAN_CLK = PCLK divided by 1. 0001: CAN_CLK = PCLK divided by 2. 0010: CAN_CLK = PCLK divided by 3. 0010: CAN_CLK = PCLK divided by 4. 0011: CAN_CLK = PCLK divided by 5. 0100: CAN_CLK = PCLK divided by 9. 0101: CAN_CLK = PCLK divided by 17. ... 1111: CAN_CLK = PCLK divided by 16385.	0000	R/W
31:4	-	reserved	-	-

42.10.7 Functional description

42.10.7.1 C_CAN controller state after reset

After a hardware reset, the registers hold the values described in Table 904. Additionally, the busoff state is reset and the output CAN_TXD is set to recessive (HIGH). The value 0x0001 (INIT = ‘1’) in the CAN Control Register enables the software initialization. The CAN controller does not communicate with the CAN bus until the CPU resets INIT to ‘0’.

The data stored in the message RAM is not affected by a hardware reset. After power-on, the contents of the message RAM is undefined.

42.10.7.2 C_CAN operating modes

42.10.7.2.1 Software initialization

The software initialization is started by setting the bit INIT in the CAN Control Register, either by software or by a hardware reset, or by entering the busoff state.

During software initialization (INIT bit is set), the following conditions are present:

- All message transfer from and to the CAN bus is stopped.
- The status of the CAN output CAN_TXD is recessive (HIGH).
- The EML counters are unchanged.
- The configuration registers are unchanged.
- Access to the bit timing register and the BRP extension register is enabled if the CCE bit in the CAN control register is also set.

To initialize the CAN controller, software has to set up the bit timing register and each message object. If a message object is not needed, it is sufficient to set its MSGVAL bit to not valid. Otherwise, the whole message object has to be initialized.

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Resetting the INIT bit finishes the software initialization. Afterwards the Bit Stream Processor BSP synchronizes itself to the data transfer on the CAN bus by waiting for the occurrence of a sequence of 11 consecutive recessive bits (Bus Idle) before it can take part in bus activities and starts the message transfer.

Remark: The initialization of the Message Objects is independent of INIT and also can be done on the fly, but the Message Objects should all be configured to particular identifiers or set to not valid during software initialization before the BSP starts the message transfer. To change the configuration of a Message Object during normal operation, the CPU has to start by setting the MSGVAL bit to not valid. When the configuration is completed, MSAGVALis set to valid again.

42.10.7.2.2 CAN message transfer

Once the CAN controller is initialized and INIT is reset to zero, the CAN core synchronizes itself to the CAN bus and starts the message transfer.

Received messages are stored into their appropriate Message Objects if they pass the Message Handler's acceptance filtering. The whole message including all arbitration bits, DLC and eight data bytes is stored into the Message Object. If the Identifier Mask is used, the arbitration bits which are masked to “don't care” may be overwritten in the Message Object.

The CPU may read or write each message any time via the Interface Registers. The Message Handler guarantees data consistency in case of concurrent accesses.

Messages to be transmitted are updated by the CPU. If a permanent Message Object (arbitration and control bits set up during configuration) exists for the message, only the data bytes are updated and then TXRQUT bit with NEWDAT bit are set to start the transmission. If several transmit messages are assigned to the same Message Object (when the number of Message Objects is not sufficient), the whole Message Object has to be configured before the transmission of this message is requested.

The transmission of any number of Message Objects may be requested at the same time, and they are transmitted subsequently according to their internal priority. Messages may be updated or set to not valid any time, even when their requested transmission is still pending. The old data will be discarded when a message is updated before its pending transmission has started.

Depending on the configuration of the Message Object, the transmission of a message may be requested autonomously by the reception of a remote frame with a matching identifier.

42.10.7.2.3 Disabled Automatic Retransmission (DAR)

According to the *CAN Specification (ISO11898, 6.3.3 Recovery Management)*, the CAN controller provides means for automatic retransmission of frames that have lost arbitration or that have been disturbed by errors during transmission. The frame transmission service will not be confirmed to the user before the transmission is successfully completed. By default, the automatic retransmission on lost arbitration or error is enabled. It can be disabled to enable the CAN controller to work within a Time Triggered CAN (TTCAN, see ISO11898-1) environment.

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The Disable Automatic Retransmission mode is enabled by programming bit DAR in the CAN Control Register to one. In this operation mode the programmer has to consider the different behavior of bits TXRQST and NEWDAT in the Control Registers of the Message Buffers:

- When a transmission starts, bit TXRQST of the respective Message Buffer is reset while bit NEWDAT remains set.
- When the transmission completed successfully, bit NEWDAT is reset.
- When a transmission failed (lost arbitration or error), bit NEWDAT remains set. To restart the transmission, the CPU has to set TXRQST back to one.

42.10.7.2.4 Test modes

The Test mode is entered by setting bit TEST in the CAN Control Register to one. In Test mode the bits TX1, TX0, LBACK, SILENT, and BASIC in the Test Register are writable. Bit RX monitors the state of pins RD0,1 and therefore is only readable. All Test register functions are disabled when bit TEST is reset to zero.

Silent mode: The CAN core can be set in Silent mode by programming the Test register bit SILENT to one.

In Silent Mode, the CAN controller is able to receive valid data frames and valid remote frames, but it sends only recessive bits on the CAN bus, and it cannot start a transmission. If the CAN Core is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is rerouted internally so that the CAN Core monitors this dominant bit, although the CAN bus may remain in recessive state. The Silent mode can be used to analyze the traffic on a CAN bus without affecting it by the transmission of dominant bits (Acknowledge Bits, Error Frames).

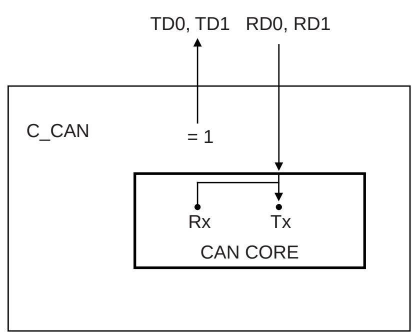


Fig 172. CAN core in Silent mode

Loop-back mode: The CAN Core can be set in Loop-back mode by programming the Test Register bit LBACK to one. In Loop-back Mode, the CAN Core treats its own transmitted messages as received messages and stores them (if they pass acceptance filtering) into a Receive Buffer.

This mode is provided for self-test functions. To be independent from external stimulation, the CAN Core ignores acknowledge errors (recessive bit sampled in the acknowledge slot of a data/remote frame) in Loop-back mode. In this mode the CAN core performs an internal feedback from its CAN_TXD output to its CAN_RXD input. The actual value of the CAN_RXD input pin is disregarded by the CAN Core. The transmitted messages can be monitored at the CAN_TXD pin.

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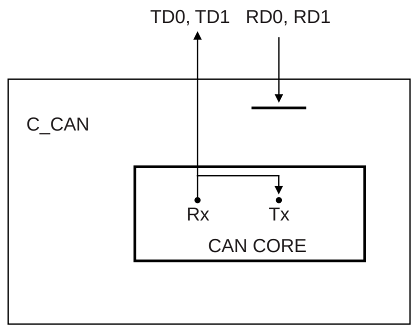


Fig 173. CAN core in Loop-back mode

Loop-back mode combined with Silent mode: It is also possible to combine Loop-back mode and Silent mode by programming bits LBACK and SILENT to one at the same time. This mode can be used for a “Hot Selftest”, meaning the C_CAN can be tested without affecting a running CAN system connected to the pins CAN_TXD and CAN_RXD. In this mode the CAN_RXD pin is disconnected from the CAN Core and the CAN_TXD pin is held recessive.

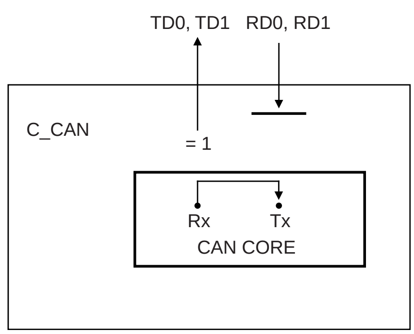


Fig 174. CAN core in Loop-back mode combined with Silent mode

Basic mode: The CAN Core can be set in Basic mode by programming the Test Register bit BASIC to one. In this mode the CAN controller runs without the Message RAM.

The IF1 Registers are used as Transmit Buffer. The transmission of the contents of the IF1 Registers is requested by writing the BUSY bit of the IF1 Command Request Register to ‘1’. The IF1 Registers are locked while the BUSY bit is set. The BUSY bit indicates that the transmission is pending.

As soon the CAN bus is idle, the IF1 Registers are loaded into the shift register of the CAN Core and the transmission is started. When the transmission has completed, the BUSY bit is reset and the locked IF1 Registers are released.

A pending transmission can be aborted at any time by resetting the BUSY bit in the IF1 Command Request Register while the IF1 Registers are locked. If the CPU has reset the BUSY bit, a possible retransmission in case of lost arbitration or in case of an error is disabled.

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The IF2 Registers are used as Receive Buffer. After the reception of a message the contents of the shift register is stored into the IF2 Registers, without any acceptance filtering.

Additionally, the actual contents of the shift register can be monitored during the message transfer. Each time a read Message Object is initiated by writing the BUSY bit of the IF2 Command Request Register to '1', the contents of the shift register is stored into the IF2 Registers.

In Basic mode the evaluation of all Message Object related control and status bits and of the control bits of the IFx Command Mask Registers is turned off. The message number of the Command request registers is not evaluated. The NEWDAT and MSGLST bits of the IF2 Message Control Register retain their function, DLC3-0 will show the received DLC, the other control bits will be read as '0'.

In Basic mode the ready output CAN_WAIT_B is disabled (always '1')

Software control of pin CAN_TXD: Four output functions are available for the CAN transmit pin CAN_TXD:

1. serial data output (default).
2. drives CAN sample point signal to monitor the CAN controller's timing.
3. drives recessive constant value.
4. drives dominant constant value.

The last two functions, combined with the readable CAN receive pin CAN_RXD, can be used to check the CAN bus' physical layer.

The output mode of pin CAN_TXD is selected by programming the Test Register bits TX1 and TX0 as described Section 42.10.6.1.6.

Remark: The three test functions for pin CAN_TXD interfere with all CAN protocol functions. The CAN_TXD pin must be left in its default function when CAN message transfer or any of the test modes Loo-back mode, Silent mode, or Basic mode are selected.

42.10.7.3 CAN message handler

The Message handler controls the data transfer between the Rx/Tx Shift Register of the CAN Core, the Message RAM and the IFx Registers, see Figure 171.

The message handler controls the following functions:

- Data Transfer between IFx Registers and the Message RAM
- Data Transfer from Shift Register to the Message RAM
- Data Transfer from Message RAM to Shift Register
- Data Transfer from Shift Register to the Acceptance Filtering unit
- Scanning of Message RAM for a matching Message Object
- Handling of TXRQST flags
- Handling of interrupts

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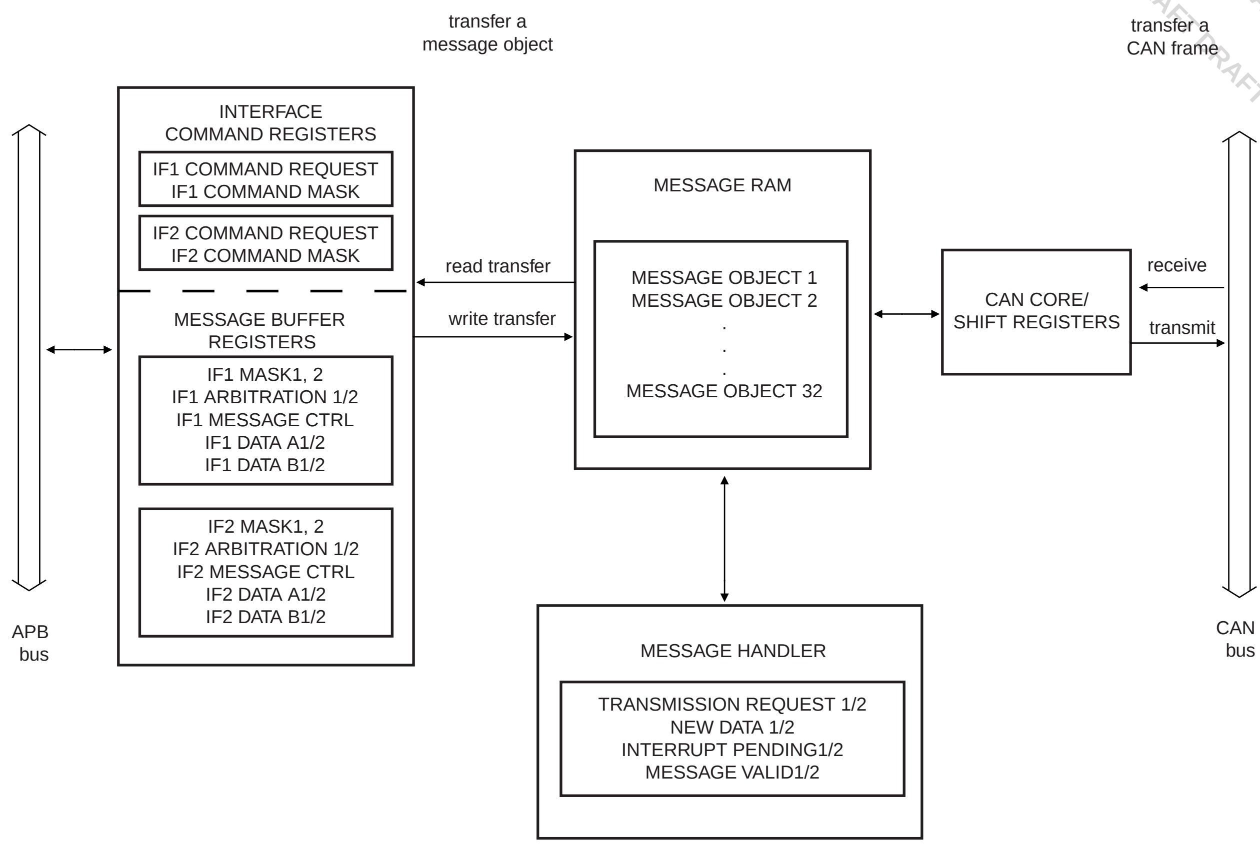


Fig 175. Block diagram of a message object transfer

42.10.7.3.1 Management of message objects

The configuration of the Message Objects in the Message RAM will (with the exception of the bits MSGVAL, NEWDAT, INTPND, and TXRQST) is not be affected by resetting the chip. All the Message Objects must be initialized by the CPU or they must be set to not valid (MSGVAL = ‘0’).The bit timing must be configured before the CPU clears the INIT bit in the CAN Control Register.

The configuration of a Message Object is done by programming Mask, Arbitration, Control and Data field of one of the two interface register sets to the desired values. By writing to the corresponding IFx Command Request Register, the IFx Message Buffer Registers are loaded into the addressed Message Object in the Message RAM.

When the INIT bit in the CAN Control Register is cleared, the CAN Protocol Controller state machine of the CAN core and the Message Handler State Machine control the CAN controller’s internal data flow. Received messages that pass the acceptance filtering are stored into the Message RAM, and messages with pending transmission request are loaded into the CAN core’s shift register and are transmitted via the CAN bus.

The CPU reads received messages and updates messages to be transmitted via the IFx Interface Registers. Depending on the configuration, the CPU is interrupted on certain CAN message and CAN error events.

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42.10.7.3.2 Data Transfer between IFx Registers and the Message RAM

When the CPU initiates a data transfer between the IFx Registers and Message RAM, the Message Handler sets the BUSY bit in the respective Command Register to ‘1’. After the transfer has completed, the BUSY bit is set back to ‘0’.

The Command Mask Register specifies whether a complete Message Object or only parts of it will be transferred. Due to the structure of the Message RAM it is not possible to write single bits/bytes of one Message Object. Software must always write a complete Message Object into the Message RAM. Therefore the data transfer from the IFx Registers to the Message RAM requires a read-modify-write cycle:

1. Read the parts of the message object that are not to be changed from the message RAM using the command mask register.
   – After the partial read of a Message Object, the Message Buffer Registers that are not selected in the Command Mask Register will be left unchanged.
2. Write the complete contents of the message buffer registers into the message object.
   – After the partial write of a Message Object, the Message Buffer Registers that are not selected in the Command Mask Register will set to the actual contents of the selected Message Object.

42.10.7.3.3 Transmission of messages between the shift registers in the CAN core and the Message buffer

If the shift register of the CAN Core cell is ready for loading and if there is no data transfer between the IFx Registers and Message RAM, the MSGVAL bits in the Message Valid Register TXRQST bits in the Transmission Request Register are evaluated. The valid Message Object with the highest priority pending transmission request is loaded into the shift register by the Message Handler and the transmission is started. The Message Object’s NEWDAT bit is reset.

After a successful transmission and if no new data was written to the Message Object (NEWDAT = ‘0’) since the start of the transmission, the TXRQST bit will be reset. If TXIE is set, INTPND will be set after a successful transmission. If the CAN controller has lost the arbitration or if an error occurred during the transmission, the message will be retransmitted as soon as the CAN bus is free again. If meanwhile the transmission of a message with higher priority has been requested, the messages will be transmitted in the order of their priority.

42.10.7.3.4 Acceptance filtering of received messages

When the arbitration and control field (Identifier + IDE + RTR + DLC) of an incoming message is completely shifted into the Rx/Tx Shift Register of the CAN Core, the Message Handler state machine starts the scanning of the Message RAM for a matching valid Message Object.

To scan the Message RAM for a matching Message Object, the Acceptance Filtering unit is loaded with the arbitration bits from the CAN Core shift register. Then the arbitration and mask fields (including MSGVAL, UMASK, NEWDAT, and EOB) of Message Object 1 are loaded into the Acceptance Filtering unit and compared with the arbitration field from the shift register. This is repeated with each following Message Object until a matching Message Object is found or until the end of the Message RAM is reached.

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If a match occurs, the scanning is stopped and the Message Handler state machine proceeds depending on the type of frame (Data Frame or Remote Frame) received.

Reception of a data frame: The Message Handler state machine stores the message from the CAN Core shift register into the respective Message Object in the Message RAM. The data bytes, all arbitration bits, and the Data Length Code are stored into the corresponding Message Object. This is implemented to keep the data bytes connected with the identifier even if arbitration mask registers are used.

The NEWDAT bit is set to indicate that new data (not yet seen by the CPU) has been received. The CPU/software should reset NEWDAT when it reads the Message Object. If at the time of the reception the NEWDAT bit was already set, MSGLST is set to indicate that the previous data (supposedly not seen by the CPU) is lost. If the RxIE bit is set, the INTPND bit is also set, causing the Interrupt Register to point to this Message Object.

The TXRQST bit of this Message Object is reset to prevent the transmission of a Remote Frame, while the requested Data Frame has just been received.

Reception of a remote frame: When a Remote Frame is received, three different configurations of the matching Message Object have to be considered:

1. DIR = ‘1’ (direction = transmit), RMTEN = ‘1’, UMASK = ‘1’ or ’0’

   On the reception of a matching Remote Frame, the TXRQST bit of this Message Object is set. The rest of the Message Object remains unchanged.
2. DIR = ‘1’ (direction = transmit), RMTEN = ‘0’, UMASK = ’0’

   On the reception of a matching Remote Frame, the TXRQST bit of this Message Object remains unchanged; the Remote Frame is ignored.
3. DIR = ‘1’ (direction = transmit), RMTEN = ‘0’, UMASK = ’1’

   On the reception of a matching Remote Frame, the TXRQST bit of this Message Object is reset. The arbitration and control field (Identifier + IDE + RTR + DLC) from the shift register is stored into the Message Object in the Message RAM, and the NEWDAT bit of this Message Object is set. The data field of the Message Object remains unchanged; the Remote Frame is treated similar to a received Data Frame.

42.10.7.3.5 Receive/transmit priority

The receive/transmit priority for the Message Objects is attached to the message number. Message Object 1 has the highest priority, while Message Object 32 has the lowest priority. If more than one transmission request is pending, they are serviced due to the priority of the corresponding Message Object.

42.10.7.3.6 Configuration of a transmit object

Table 1046 shows how a transmit object should be initialized by software (see also Table 1024):

Table 1046. Initialization of a transmit object

MSGVAL	Arbitration bits	Data bits	Mask bits	EOB	DIR	NEWDAT
1	application dependent	application dependent	application dependent	1	1	0

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MSGLST	RXIE	TXIE	INTPND	RMTEN	TXRQST
0	0	application dependent	0	application dependent	0

The Arbitration Registers (ID28:0 and XTD bit) are given by the application. They define the identifier and the type of the outgoing message. If an 11-bit Identifier (“Standard Frame”) is used, it is programmed to ID28. In this case ID18, ID17 to ID0 can be disregarded.

If the TXIE bit is set, the INTPND bit will be set after a successful transmission of the Message Object.

If the RMTEN bit is set, a matching received Remote Frame will cause the TXRQST bit to be set, and the Remote Frame will autonomously be answered by a Data Frame.

The Data Registers (DLC3:0, Data0:7) are given by the application. TXRQST and RMTEN may not be set before the data is valid.

The Mask Registers (Msk28-0, UMASK, MXTD, and MDIR bits) may be used (UMASK=’1’) to allow groups of Remote Frames with similar identifiers to set the TXRQST bit. For details see Section . The DIR bit should not be masked.

42.10.7.3.7 Updating a transmit object

The CPU may update the data bytes of a Transmit Object any time via the IFx Interface registers. Neither MSGVAL nor TXRQST have to be reset before the update.

Even if only a part of the data bytes are to be updated, all four bytes of the corresponding IFx Data A Register or IFx Data B Register have to be valid before the content of that register is transferred to the Message Object. Either the CPU has to write all four bytes into the IFx Data Register or the Message Object is transferred to the IFx Data Register before the CPU writes the new data bytes.

When only the (eight) data bytes are updated, first 0x0087 is written to the Command Mask Register. Then the number of the Message Object is written to the Command Request Register, concurrently updating the data bytes and setting TXRQST.

To prevent the reset of TXRQST at the end of a transmission that may already be in progress while the data is updated, NEWDAT has to be set together with TXRQST. For details see Section 42.10.7.3.3.

When NEWDAT is set together with TXRQST, NEWDAT will be reset as soon as the new transmission has started.

42.10.7.3.8 Configuration of a receive object

Table 1047 shows how a receive object should be initialized by software (see also Table 1024)

Table 1047.Initialization of a receive object

MSGVAL	Arbitration bits	Data bits	Mask bits	EOB	DIR	NEWDAT
1	application dependent	application dependent	application dependent	1	0	0

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MSGLST	RXIE	TXIE	INTPND	RMTEN	TXRQST
0	application dependent	0	0	0	0

The Arbitration Registers (ID28-0 and XTD bit) are given by the application. They define the identifier and type of accepted received messages. If an 11-bit Identifier (“Standard Frame”) is used, it is programmed to ID28 to ID18. ID17 to ID0 can then be disregarded. When a Data Frame with an 11-bit Identifier is received, ID17 to ID0 will be set to ‘0’.

If the RxIE bit is set, the INTPND bit will be set when a received Data Frame is accepted and stored in the Message Object.

The Data Length Code (DLC[3:0] is given by the application. When the Message Handler stores a Data Frame in the Message Object, it will store the received Data Length Code and eight data bytes. If the Data Length Code is less than 8, the remaining bytes of the Message Object will be overwritten by non specified values.

The Mask Registers (Msk[28:0], UMASK, MXTD, and MDIR bits) may be used (UMASK=’1’) to allow groups of Data Frames with similar identifiers to be accepted. For details see section Section . The DIR bit should not be masked in typical applications.

42.10.7.3.9 Handling of received messages

The CPU may read a received message any time via the IFx Interface registers. The data consistency is guaranteed by the Message Handler state machine.

To transfer the entire received message from message RAM into the message buffer, software must write first 0x007F to the Command Mask Register and then the number of the Message Object to the Command Request Register. Additionally, the bits NEWDAT and INTPND are cleared in the Message RAM (not in the Message Buffer).

If the Message Object uses masks for acceptance filtering, the arbitration bits show which of the matching messages has been received.

The actual value of NEWDAT shows whether a new message has been received since last time this Message Object was read. The actual value of MSGLST shows whether more than one message has been received since last time this Message Object was read. MSGLST will not be automatically reset.

Using a Remote Frame, the CPU may request another CAN node to provide new data for a receive object. Setting the TXRQST bit of a receive object will cause the transmission of a Remote Frame with the receive object’s identifier. This Remote Frame triggers the other CAN node to start the transmission of the matching Data Frame. If the matching Data Frame is received before the Remote Frame could be transmitted, the TXRQST bit is automatically reset.

42.10.7.3.10 Configuration of a FIFO buffer

With the exception of the EOB bit, the configuration of Receive Objects belonging to a FIFO Buffer is the same as the configuration of a (single) Receive Object, see section Section 42.10.7.3.8.

To concatenate two or more Message Objects into a FIFO Buffer, the identifiers and masks (if used) of these Message Objects have to be programmed to matching values. Due to the implicit priority of the Message Objects, the Message Object with the lowest

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number will be the first Message Object of the FIFO Buffer. The EOB bit of all Message Objects of a FIFO Buffer except the last have to be programmed to zero. The EOB bits of the last Message Object of a FIFO Buffer is set to one, configuring it as the End of the Block.

Reception of messages with FIFO buffers: Received messages with identifiers matching to a FIFO Buffer are stored into a Message Object of this FIFO Buffer starting with the Message Object with the lowest message number.

When a message is stored into a Message Object of a FIFO Buffer the NEWDAT bit of this Message Object is set. By setting NEWDAT while EOB is zero the Message Object is locked for further write accesses by the Message Handler until the CPU has written the NEWDAT bit back to zero.

Messages are stored into a FIFO Buffer until the last Message Object of this FIFO Buffer is reached. If none of the preceding Message Objects is released by writing NEWDAT to zero, all further messages for this FIFO Buffer will be written into the last Message Object of the FIFO Buffer and therefore overwrite previous messages.

Reading from a FIFO buffer: When the CPU transfers the contents of Message Object to the IFx Message Buffer registers by writing its number to the IFx Command Request Register, bits NEWDAT and INTPND in the corresponding Command Mask Register should be reset to zero (TXRQST/NEWDAT = ‘1’ and ClrINTPND = ‘1’). The values of these bits in the Message Control Register always reflect the status before resetting the bits.

To assure the correct function of a FIFO Buffer, the CPU should read out the Message Objects starting at the FIFO Object with the lowest message number.

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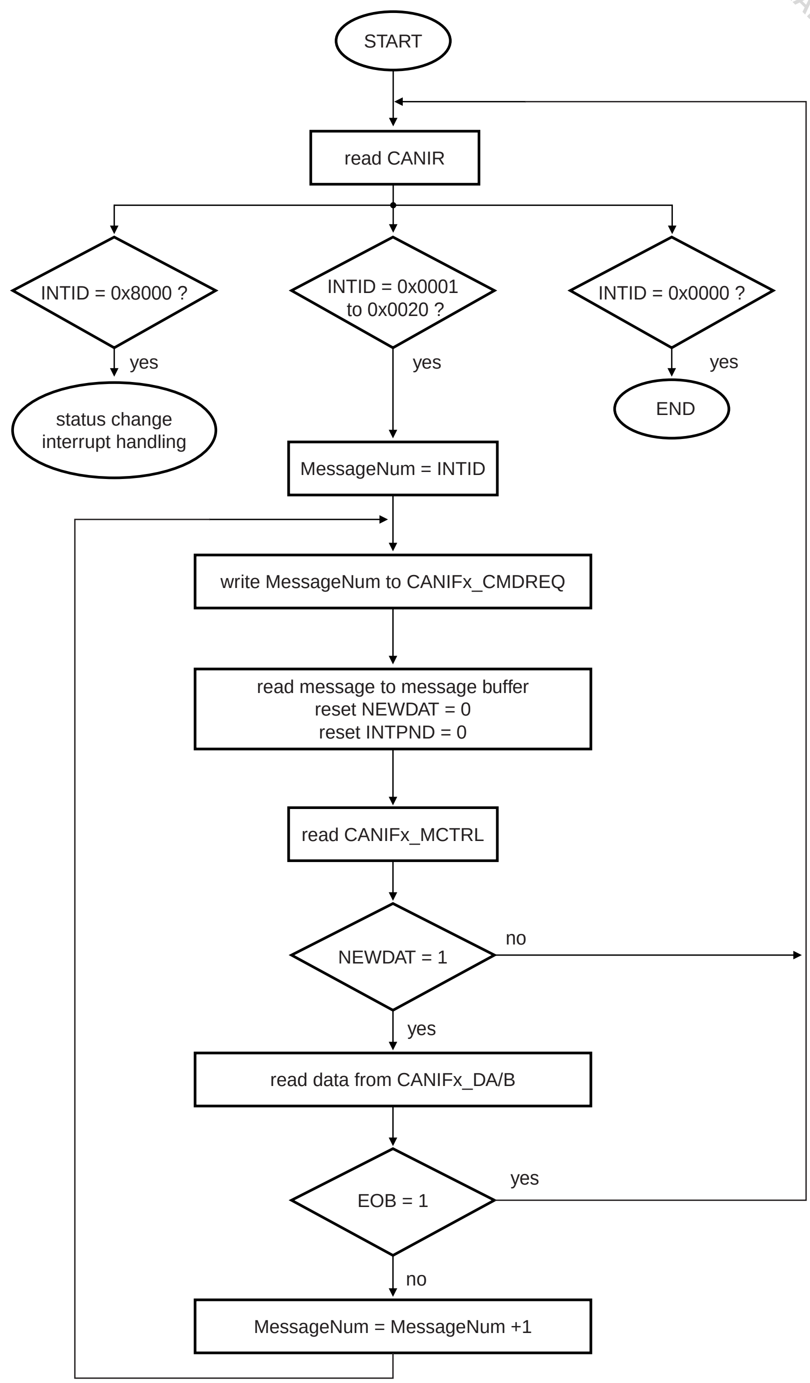


Fig 176. Reading a message from the FIFO buffer to the message buffer

42.10.7.4 Interrupt handling

If several interrupts are pending, the CAN Interrupt Register will point to the pending interrupt with the highest priority, disregarding their chronological order. An interrupt remains pending until the CPU has cleared it.

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The Status Interrupt has the highest priority. Among the message interrupts, the Message Object's interrupt priority decreases with increasing message number.

A message interrupt is cleared by clearing the Message Object's INTPND bit. The Status Interrupt is cleared by reading the Status Register.

The interrupt identifier INTID in the Interrupt Register indicates the cause of the interrupt. When no interrupt is pending, the register will hold the value zero. If the value of the Interrupt Register is different from zero, then there is an interrupt pending and, if IE is set, the interrupt line to the CPU, IRQ_B, is active. The interrupt line remains active until the Interrupt Register is back to value zero (the cause of the interrupt is reset) or until IE is reset.

The value 0x8000 indicates that an interrupt is pending because the CAN Core has updated (not necessarily changed) the Status Register (Error Interrupt or Status Interrupt). This interrupt has the highest priority. The CPU can update (reset) the status bits RXOK, TXOK and LEC, but a write access of the CPU to the Status Register can never generate or reset an interrupt.

All other values indicate that the source of the interrupt is one of the Message Objects where INTID points to the pending message interrupt with the highest interrupt priority.

The CPU controls whether a change of the Status Register may cause an interrupt (bits EIE and SIE in the CAN Control Register) and whether the interrupt line becomes active when the Interrupt Register is different from zero (bit IE in the CAN Control Register). The Interrupt Register will be updated even when IE is reset.

The CPU has two possibilities to follow the source of a message interrupt:

- Software can follow the INTID in the Interrupt Register.
- Software can poll the interrupt pending register.

An interrupt service routine reading the message that is the source of the interrupt may read the message and reset the Message Object's INTPND at the same time (bit ClrINTPND in the Command Mask Register). When INTPND is cleared, the Interrupt Register will point to the next Message Object with a pending interrupt.

42.10.7.5 Bit timing

Even if minor errors in the configuration of the CAN bit timing do not result in immediate failure, the performance of a CAN network can be reduced significantly. In many cases, the CAN bit synchronization will amend a faulty configuration of the CAN bit timing to such a degree that only occasionally an error frame is generated. In the case of arbitration however, when two or more CAN nodes simultaneously try to transmit a frame, a misplaced sample point may cause one of the transmitters to become error passive.

The analysis of such sporadic errors requires a detailed knowledge of the CAN bit synchronization inside a CAN node and of the CAN nodes' interaction on the CAN bus.

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42.10.7.5.1 Bit time and bit rate

CAN supports bit rates in the range of lower than 1 kBit/s up to 1000 kBit/s. Each member of the CAN network has its own clock generator, usually a quartz oscillator. The timing parameter of the bit time (i.e. the reciprocal of the bit rate) can be configured individually for each CAN node, creating a common bit rate even though the CAN nodes' oscillator periods (f_{osc}) may be different.

The frequencies of these oscillators are not absolutely stable, as small variations are caused by changes in temperature or voltage and by deteriorating components. As long as the variations remain inside a specific oscillator tolerance range (df), the CAN nodes are able to compensate for the different bit rates by re-synchronizing to the bit stream.

According to the CAN specification, the bit time is divided into four segments (Figure 177). The Synchronization Segment, the Propagation Time Segment, the Phase Buffer Segment 1, and the Phase Buffer Segment 2. Each segment consists of a specific, programmable number of time quanta (see Table 1048). The length of the time quantum (t_q), which is the basic time unit of the bit time, is defined by the CAN controller's system clock f and the Baud Rate Prescaler (BRP): $t_q = BRP / f_{sys}$. The C_CAN's system clock f_{sys} is the frequency C_CAN peripheral clock.

The Synchronization Segment Sync_Seg is the part of the bit time where edges of the CAN bus level are expected to occur; the distance between an edge that occurs outside of Sync_Seg and the Sync_Seg is called the phase error of that edge. The Propagation Time Segment Prop_Seg is intended to compensate for the physical delay times within the CAN network. The Phase Buffer Segments Phase_Seg1 and Phase_Seg2 surround the Sample Point. The (Re-)Synchronization Jump Width (SJW) defines how far a re-synchronization may move the Sample Point inside the limits defined by the Phase Buffer Segments to compensate for edge phase errors.

Table 1048 describes the minimum programmable ranges required by the CAN protocol. Bit time parameters are programmed through the BT register, Table 1019. For details on bit timing and examples, see the *C_CAN user's manual, revision 1.2*.

Table 1048. Parameters of the C_CAN bit time

Parameter	Range	Function
BRP	(1...32)	Defines the length of the time quantum t_q.
SYNC_SEG	$1t_q$	Synchronization segment. Fixed length. Synchronization of bus input to system clock.
PROP_SEG	$(1...8) \times t_q$	Propagation time segment. Compensates for physical delay times. This parameter is determined by the system delay times in the C_CAN network.
TSEG1	$(1...8) \times t_q$	Phase buffer segment 1. May be lengthened temporarily by synchronization.
TSEG2	$(1...8) \times t_q$	Phase buffer segment 2. May be shortened temporarily by synchronization.
SJW	$(1...4) \times t_q$	(Re-) synchronization jump width. May not be longer than either phase buffer segment.

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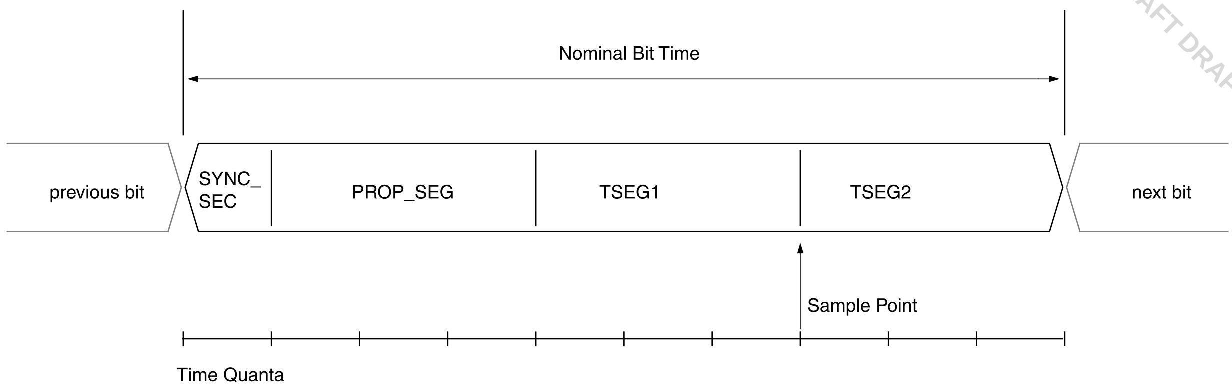
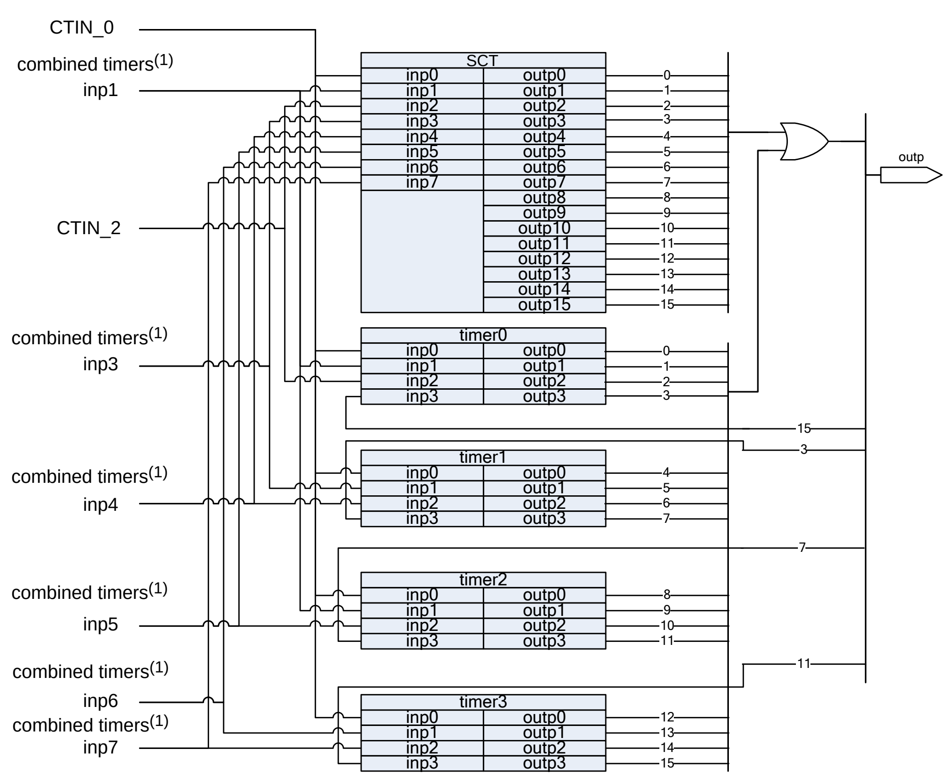


Fig 177. Bit timing

42.11 LPC1850/30/20/10 Rev '-' SCT interconnections

42.11.1 Input muxing for State Configurable Timer and general purpose timers



(1) See Figure 179.

Fig 178. SCT/general purpose timers cross connections

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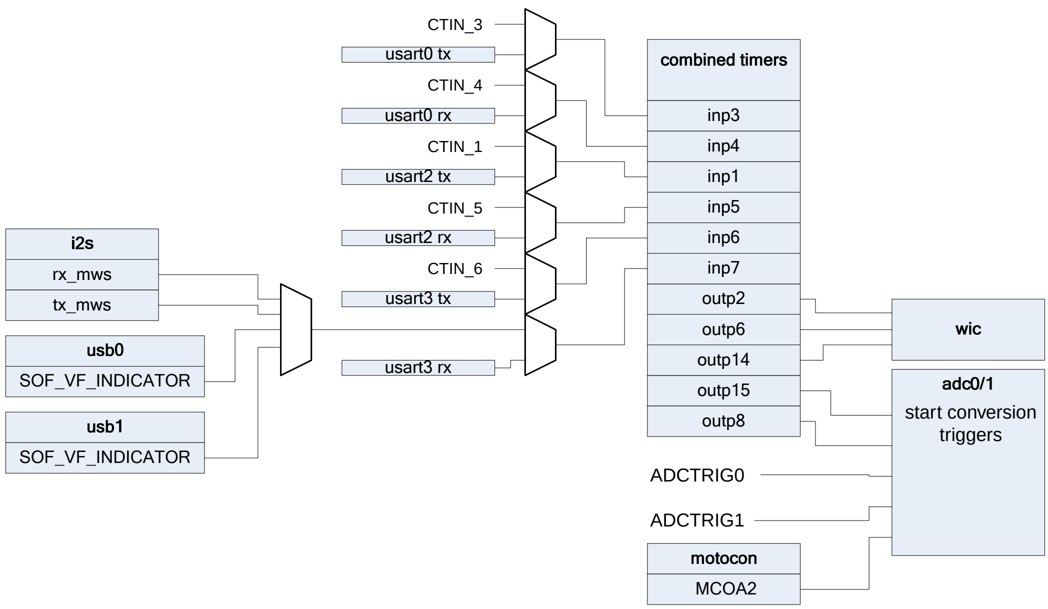


Fig 179. Input muxing for SCT and general purpose timers

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43.1 Abbreviations

Table 1049. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
BOD	BrownOut Detection
CAN	Controller Area Network
CMAC	Cipher-based Message Authentication Code
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DAC	Digital-to-Analog Converter
DC-DC	Direct Current-to-Direct Current
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MAC	Media Access Control
MCU	MicroController Unit
MIIM	Media Independent Interface Management
n.c.	not connected
OHCI	Open Host Controller Interface
OTG	On-The-Go
PHY	Physical Layer
PLL	Phase-Locked Loop
PMC	Power Mode Control
PWM	Pulse Width Modulator
RIT	Repetitive Interrupt Timer
RMII	Reduced Media Independent Interface
SDRAM	Synchronous Dynamic Random Access Memory
SIMD	Single Instruction Multiple Data
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TCP/IP	Transmission Control Protocol/Internet Protocol

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Table 1049. Abbreviations *…continued*

Acronym	Description
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
USART	Universal Synchronous Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
UTMI	USB2.0 Transceiver Macrocell Interface

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Date of release: 20 July 2011
Document identifier: <Document ID>