

HD74LS641

Octal Bus Transceivers (non-inverted open-collector outputs)

REJ03D0488-0200

Rev.2.00

Feb.18.2005

This octal bus transceivers is designed for asynchronous two-way communication between data buses. The devices transmit data, from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\bar{G}$) can be used to disable the device so that the buses are effectively isolated.

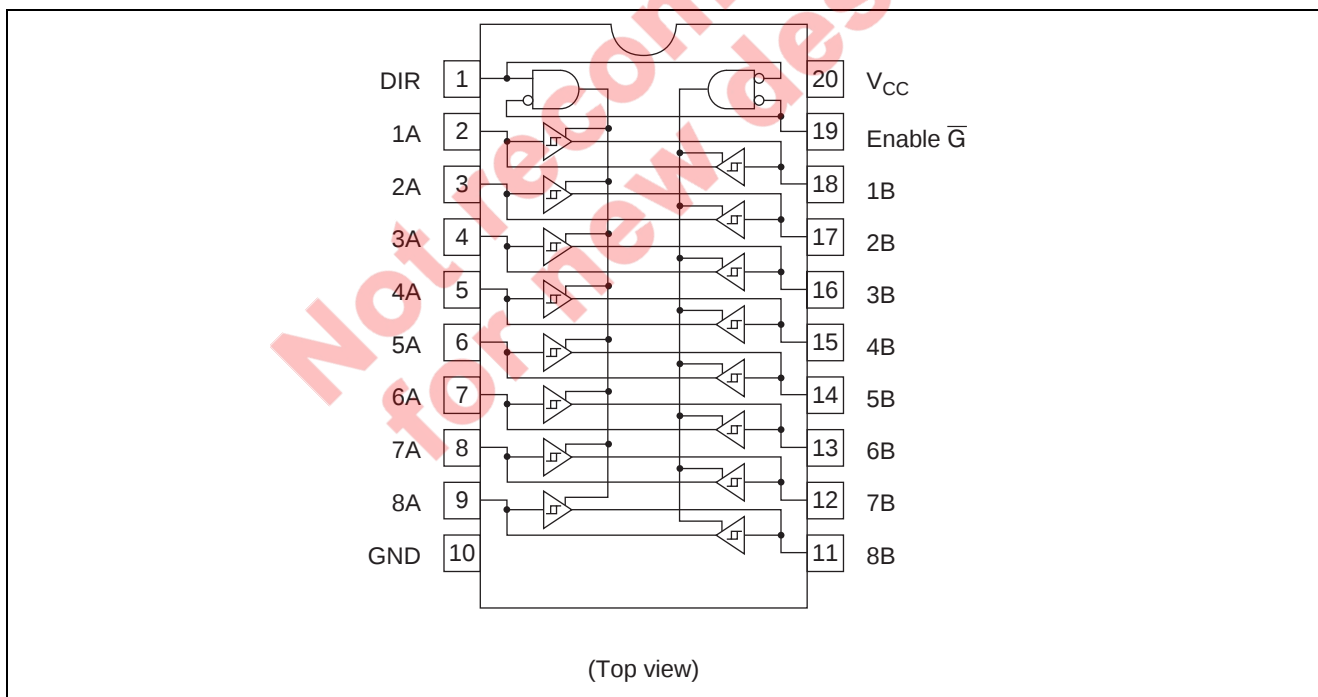
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS641P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74LS641FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement

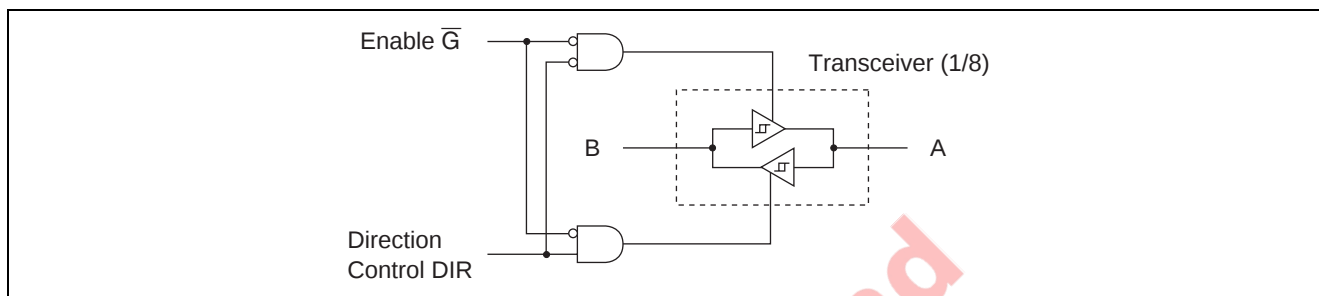


Function Table

Enable	Direction Control	Operation
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Note: H; high level, L; low level, X; irrelevant

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output voltage	V_{OH}	—	—	5.5	V
Output current	I_{OL}	—	—	24	mA
Operating temperature	T_{opr}	-20	25	75	°C

Electrical Characteristics

(Ta = -20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition		
Input voltage		V _{IH}	2.0	—	—	V			
		V _{IL}	—	—	0.8	V			
Hysteresis		V _T ⁺ – V _T [–]	0.2	—	—	V	V _{CC} = 4.75 V		
Output current		I _{OH}	—	—	100	μA	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V, V _{OH} = 5.5 V		
Output voltage		V _{OL}	—	—	0.4	V	I _{OL} = 12 mA	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V	
			—	—	0.5	V	I _{OL} = 24 mA		
Input current		I _{IH}	—	—	20	μA	V _{CC} = 5.25 V, V _I = 2.7 V		
		I _{IL}	—	—	–400	μA	V _{CC} = 5.25 V, V _I = 0.4 V		
		A or B DIR or $\overline{G}$	I _I	—	—	0.1	mA	V _I = 5.5 V	V _{CC} = 5.25 V
				—	—	0.1	mA	V _I = 7 V	
Supply current		I _{CCH}	—	48	70	mA	V _{CC} = 5.25 V, Output open		
		I _{CCL}	—	62	90	mA			
		I _{CCZ}	—	64	95	mA			
Input clamp voltage		V _{IK}	—	—	–1.5	V	V _{CC} = 4.75 V, I _{IN} = –18 mA		

Note: * V_{CC} = 5 V, Ta = 25°C

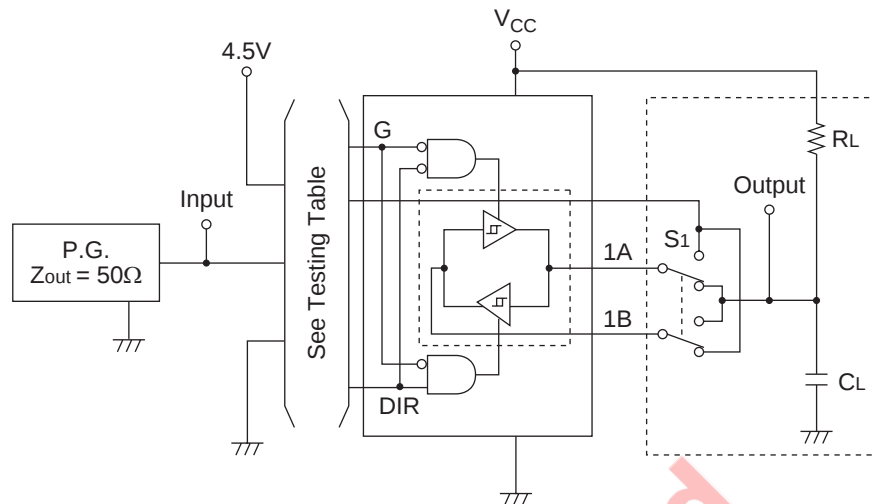
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Propagation delay time	t _{PLH}	A	B	—	17	25	ns	C _L = 45 pF, R _L = 667 Ω
		B	A	—	17	25	ns	
	t _{PHL}	A	B	—	16	25	ns	
		B	A	—	16	25	ns	
Output enable time	t _{PLH}	$\overline{G}$	A	—	23	40	ns	
		$\overline{G}$	B	—	25	40	ns	
	t _{PHL}	$\overline{G}$	A	—	34	50	ns	
		$\overline{G}$	B	—	37	50	ns	

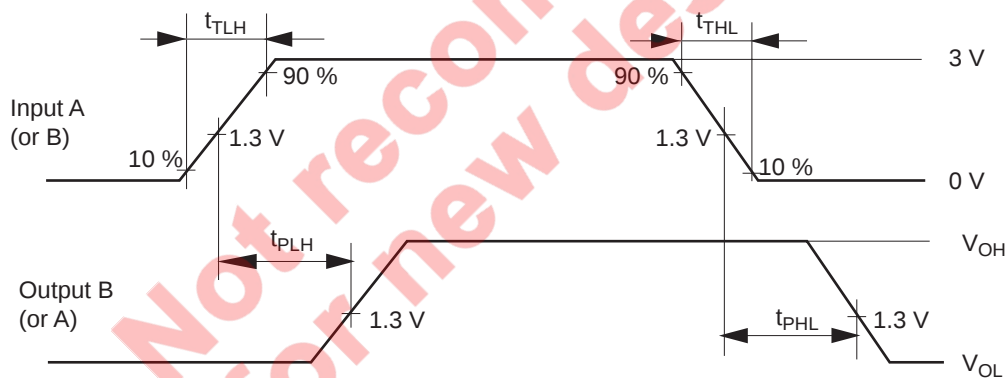
Testing Method

Test Circuit



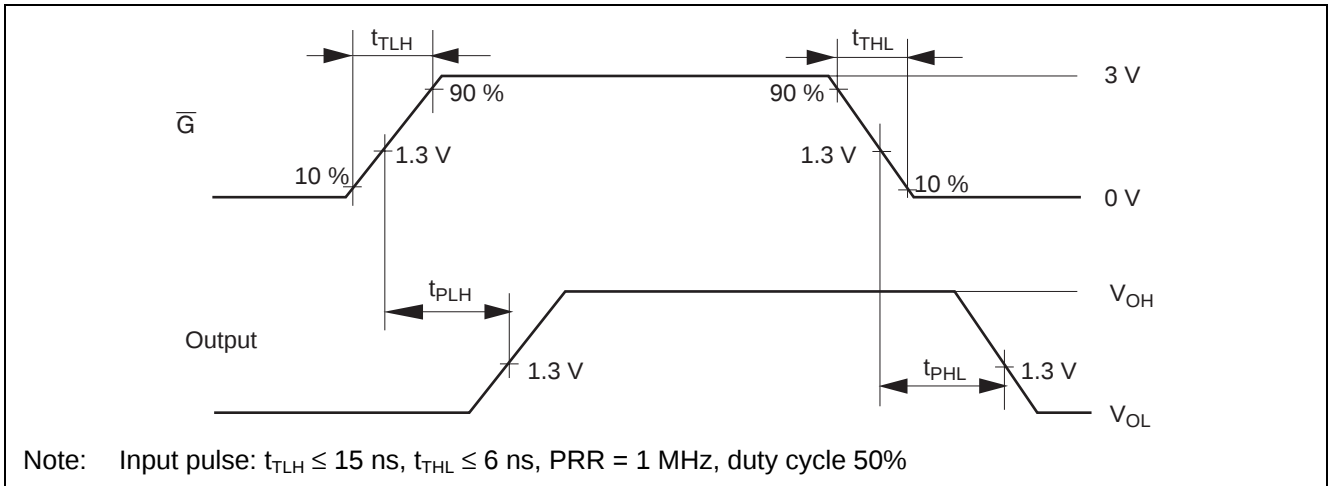
- Notes:
1. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B, are identical to above load circuit.
 2. C_L includes probe and jig capacitance.
 3. S_1 is a input-output switch.

Waveforms 1



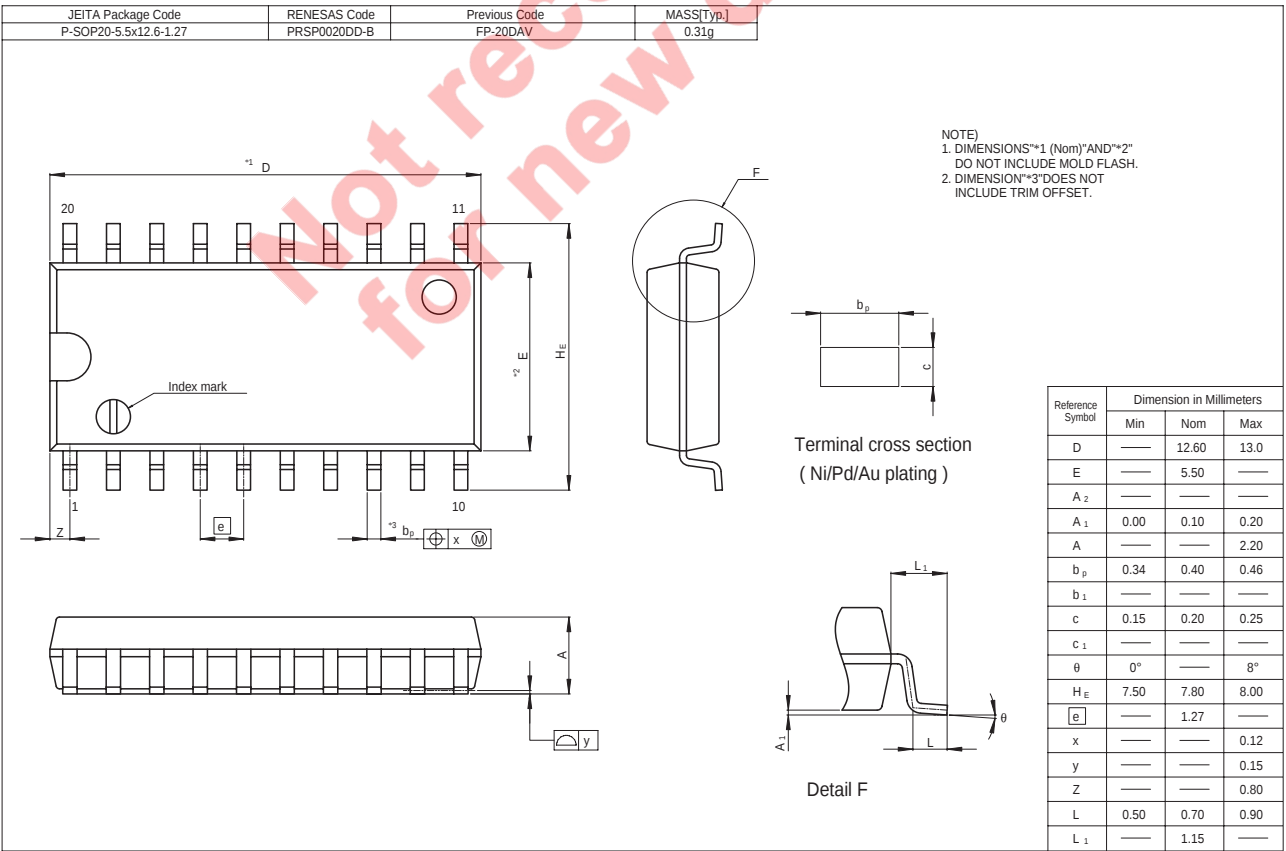
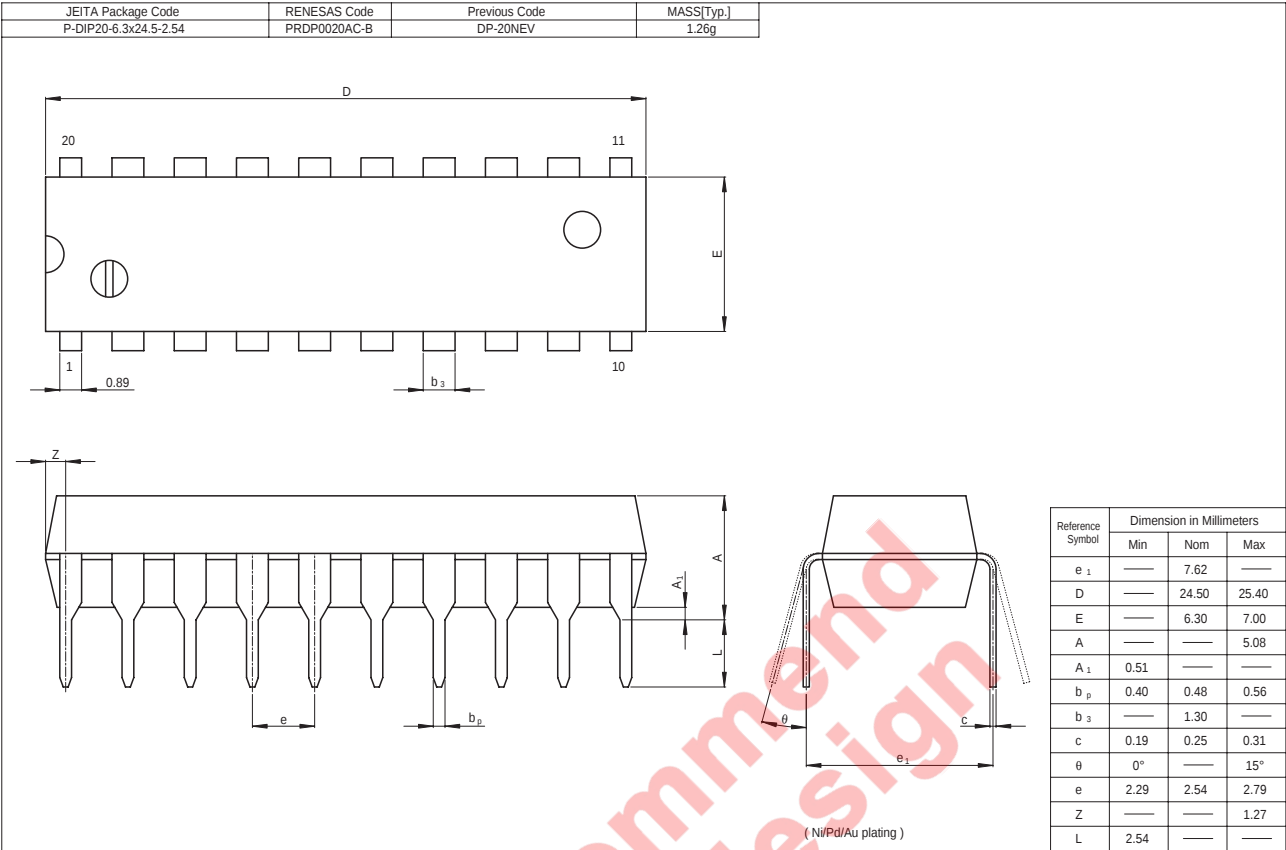
Note: Input pulse: $t_{TLH} \leq 15 \text{ ns}$, $t_{THL} \leq 6 \text{ ns}$, PRR = 1 MHz, duty cycle 50%

Waveforms 2



Not recommend
for new design

Package Dimensions



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