Dual Channel PWM Controller with Integrated Driver for IMVP8 CPU Core Power Supply

General Description

The RT3606BC is an IMVP8 compliant CPU power controller which includes two voltage rails : a 3/2/1 phase synchronous Buck controller, the CORE VR and a 2/1 phase synchronous Buck controller, the AXG VR. The RT3606BC adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3606BC also features a quick response mechanism for optimized AVP performance during load transient. The RT3606BC supports mode transition function with various operating states. A serial VID (SVID) interface is built in the RT3606BC to communicate with Intel IMVP8 compliant CPU. The RT3606BC supports VID on-the-fly function with three different slew rates : Fast, Slow and Decay. By utilizing the G-NAVP™ topology, the operating frequency of the RT3606BC varies with VID, load and input voltage to further enhance the efficiency even in CCM. Moreover, the G-NAVP™ with CCRCOT (Constant Current Ripple COT) technology provides superior output voltage ripple over the entire input/output range. The built-in high accuracy DAC converts the SVID code ranging from 0.25V to 1.52V with 5mV per step. The RT3606BC integrates a high accuracy ADC for platform setting functions, such as quick response trigger level or over-current level. Besides, the setting function also supports this two rails address exchange. The RT3606BC provides VR ready output signals. It also features complete fault protection functions including over-voltage (OV), negative voltage (NV), over-current (OC) and under-voltage lockout (UVLO). The RT3606BC is available in the WQFN-60L 7x7 small foot print package.

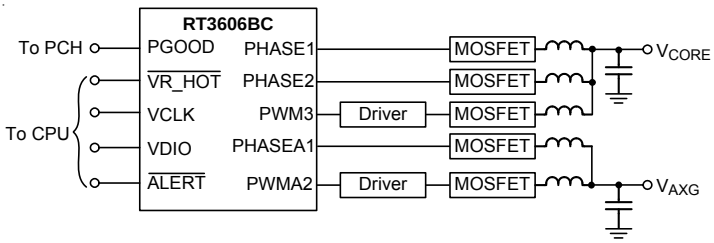
Features

- **Intel IMVP8 Serial VID Interface Compatible Power Management States**
- **3/2/1 Phase (CORE VR) + 2/1 Phase (AXG VR) PWM Controller**
- **2 Embedded MOSFET Drivers at the CORE VR, 1 Embedded MOSFET Driver at the AXG VR**
- **G-NAVP™ (Green Native Adaptive Voltage Positioning) Topology**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Platform Programming**
- **Accurate Current Balance**
- **System Thermal Compensated AVP**
- **Diode Emulation Mode at Light Load Condition for Single Phase Operation**
- **Fast Transient Response**
- **VR Ready Indicator**
- **Thermal Throttling**
- **Current Monitor Output**
- **OVP, OCP, NVP, UVLO**
- **Slew Rate Setting/Address Flip Function**
- **Rail Address Flexibility**
- **DVID Enhancement**

Applications

- IMVP8 Intel Core Supply
- Notebook/ Desktop Computer/ Servers Multi-phase CPU Core Supply
- AVP Step-Down Converter

Simplified Application Circuit



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Ordering Information

RT3606BC□□

- Package Type
  QW : WQFN-60L 7x7 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

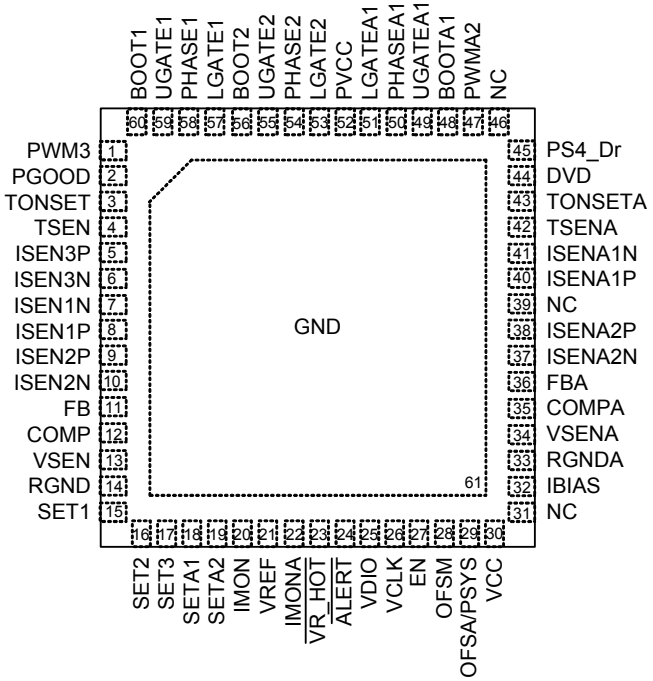
Marking Information

RT3606BCGQW : Product Number

YMDNN : Date Code

Pin Configurations

(TOP VIEW)



WQFN-60L 7x7

Functional Pin Description

Pin No	Pin Name	Pin Function
1	PWM3	PWM Output for CORE rail VR of Channel 3.
2	PGOOD	VR Ready Indicator.
3	TONSET	CORE rail VR On-time Setting. An on-time setting resistor is connected from this pin to input voltage.
4	TSEN	Thermal Sense Input for CORE rail VR.
8, 9, 5	ISEN[1:3]P	Positive Current Sense Inputs of Multi-Phase CORE rail VR Channel 1, 2 and 3.
7, 10, 6	ISEN[1:3]N	Negative Current Sense Inputs of Multi-Phase CORE rail VR Channel 1, 2 and 3.
11	FB	Negative Input of the Error Amplifier. This pin is for CORE rail VR output voltage feedback to controller.
12	COMP	CORE rail VR Compensation. This pin is the error amplifier output pin.
13	VSEN	CORE rail VR Voltage Sense Input. This pin is connected to the terminal of CORE rail VR output voltage.
14	RGND	Return Ground for CORE rail VR. This pin is the negative node of the differential remote voltage sensing.
15	SET1	1st Platform Setting. Platform can use this pin to set OCS, DVID threshold and ICCMAX for CORE rail VR.
16	SET2	2nd Platform Setting. Platform can use this pin to set RSET, QRTH, QRWIDTH and DVID width for CORE rail VR. Moreover, SET2 pin features a special function for users to confirm the soldering condition of the controller under zero VBOOT condition. Connect the SET2 pin to 5V and turn on the EN pin, if the soldering is good, both rails will output 0.8V.

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Pin No	Pin Name	Pin Function
17	SET3	3rd Platform setting. Platform can use this pin to set VR address, Zero load-line, Anti-overshoot function and behavior, AI gain, Disable DVID compensation, Decrease GTU and SA ramp (only in maximum phase = 1-phase), high frequency ramp, DVID slew rate, and PSYS function for CORE VR and AXG VR.
18	SETA1	1st Platform Setting. Platform can use this pin to set OCS, DVID threshold and ICCMAX for AXG rail VR.
19	SETA2	2nd Platform Setting. Platform can use this pin to set RSET, QRTH, QRWIDTH and DVID width for AXG rail VR.
20	IMON	CORE rail VR Current Monitor Output. This pin outputs a voltage proportional to the loading current.
21	VREF	Fixed 0.6V Output Reference Voltage. This voltage is only used to offset the output voltage of IMON pin. Between this pin and GND must be placed a RC circuit with R = 1Ω and C = 0.47μF.
22	IMONA	AXG rail VR Current Monitor Output. This pin outputs a voltage proportional to the loading current.
23	$\overline{\text{VR_HOT}}$	Thermal Monitor Output, this Pin is Active Low.
24	$\overline{\text{ALERT}}$	SVID Alert. (Active low)
25	VDIO	VR and CPU Data Transmission Interface.
26	VCLK	Synchronous Clock from the CPU.
27	EN	VR Enable Control Input.
28	OFSM	Output Voltage Offset Setting for CORE rail VR.
29	OFSA/PSYS	Output Voltage Offset Setting for AXG rail VR / System Input Power Monitor. Place the PSYS resistor as close to the IC as possible.
30	VCC	Controller Power Supply. Connect this pin to 5V and place a decoupling capacitor 2.2μF at least. The decoupling capacitor is placed as close VR controller as possible.
31, 39, 46	NC	No Internal Connection.
32	IBIAS	Internal Bias Current Setting. Connect a 100kΩ resistor from this pin tied to GND to set the internal current. Don't connect a bypass pass capacitor from this pin to GND.
33	RGNDA	Return Ground for AXG rail VR. This pin is the negative node of the differential remote voltage sensing.
34	VSENA	AXG rail VR Voltage Sense Input. This pin is connected to the terminal of AXG rail VR output voltage.
35	COMPA	AXG rail VR Compensation. This pin is the error amplifier output pin.
36	FBA	Negative Input of the Error Amplifier. This pin is for AXG rail VR output voltage feedback to controller.
40, 38	ISENA[1:2]P	Positive Current Sense Input of Multi-Phase AXG rail VR Channel 1, 2.
41, 37	ISENA[1:2]N	Negative Current Sense Input of Multi-Phase AXG rail VR Channel 1, 2.
42	TSENA	Thermal Sense Input for AXG rail VR.
43	TONSETA	AXG rail VR On-time Setting. An on-time setting resistor is connected from this pin to input voltage.
44	DVD	Divided Input Voltage Detection of Power Stage. Connect this pin to a voltage divider from input voltage of power stage to detect input voltage.

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Pin No	Pin Name	Pin Function
45	PS4_Dr	Dr.MOS Enable Control. Connecting to Dr.MOS PS4 function pin. As received PS4 command, this pin will be floating. If the Dr. MOS needs active low to enter PS4 or use discrete MOSFET, please reserve a 100k resistor to GND.
47	PWMA2	PWM Output for AXG rail VR Channel 2.
48	BOOTA1	Bootstrap Supply for High-Side Gate MOSFET Driver for AXG rail VR.
49	UGATEA1	High-Side Drive Outputs for AXG rail VR. Connect the pin to the gate of high-side MOSFET.
50	PHASEA1	Switch Node of High-Side Driver for AXG rail VR. Connect the pin to high-side MOSFE source together with the low-side MOSFET drain and inductor.
51	LGATEA1	Low-Side Driver Output for AXG rail VR. This pin drives the gate of low-side MOSFET.
52	PVCC	Driver Power Supply Input. Connect this pin to GND by a minimum 2.2μF ceramic Capacitor.
57, 53	LGATE[1:2]	Low-Side Driver Output for CORE rail VR. This pin drives the gate of low-side MOSFET.
58, 54	PHASE[1:2]	Switch Node of High-Side Driver for CORE rail VR. Connect the pin to high-side MOSFE source together with the low-side MOSFET drain and inductor.
59, 55	UGATE[1:2]	High-Side Drive Outputs for CORE rail VR. Connect the pin to the gate of high-side MOSFET.
60, 56	BOOT[1:2]	Bootstrap Supply for High-Side Gate MOSFET Driver for CORE rail VR.
61 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

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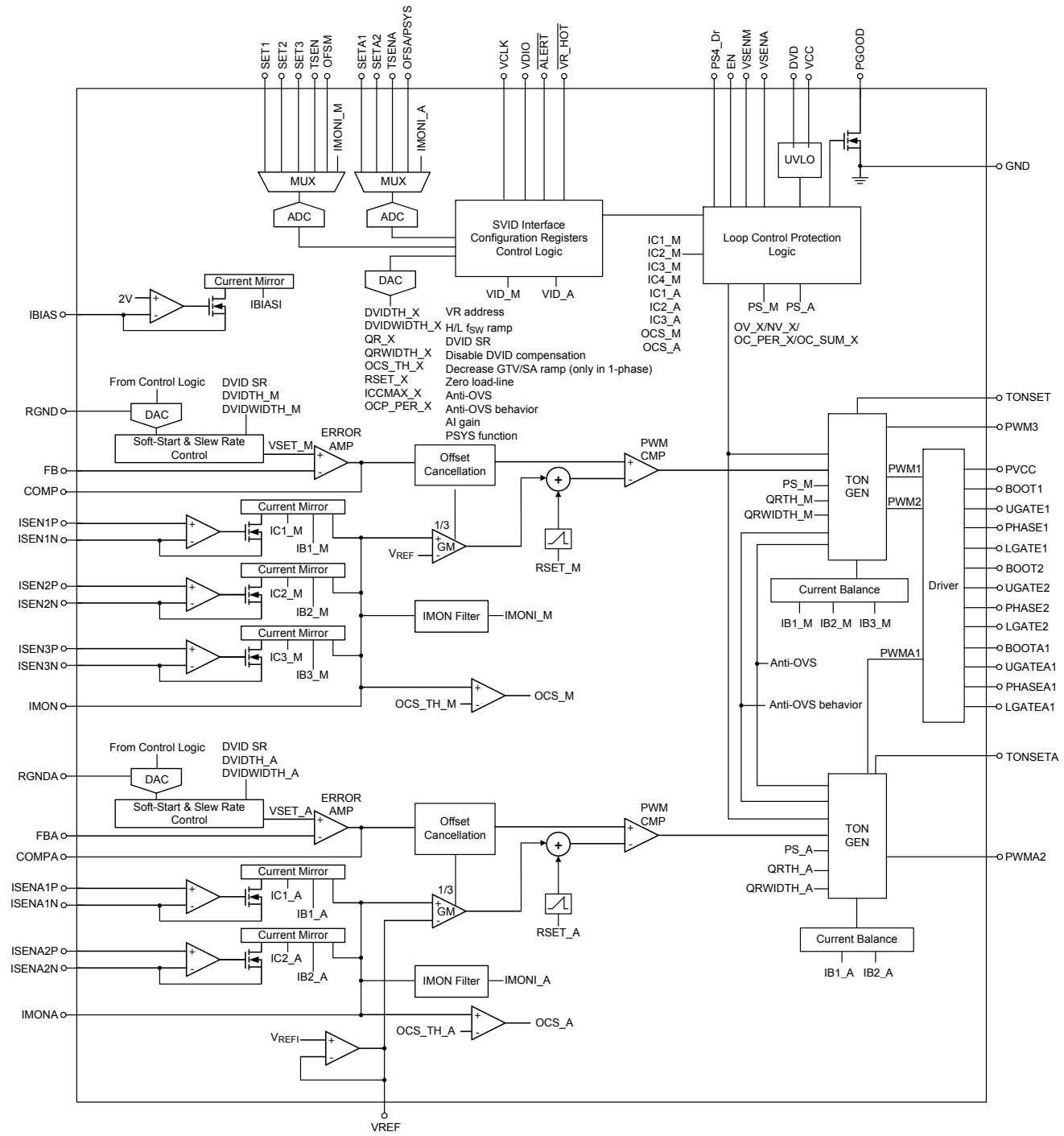
Functional Block Diagram



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Operation

The RT3606BC adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning).

The G-NAVP™ controller is one type of current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. When current feedback signal reaches COMP signal, the RT3606BC generates an on-time width to achieve PWM modulation.

TON GEN/Driver Interface

Generate the PWM1 to PWM3 sequentially according to the phase control signal from the Loop Control/Protection Logic. Pulse width is determined by current balance result and TONSET pin setting. Once quick response mechanism is triggered, VR will allow all PWM to turn on at the same time. PWM status is also controlled by Protection Logic. Different protections may cause different PWM status (Both High-Z or LG turn-on).

SVID Interface/Configuration Registers/Control Logic

The interface receives the SVID signal from CPU and sends the relative signals to Loop Control/Protection Logic for loop control to execute the action by CPU. The registers save the pin setting data from ADC output. The Control Logic controls the ADC timing and generates the digital code of the VID for VSEN voltage.

Loop Control/Protection Logic

It controls the power on sequence, the protection behavior, and the operational phase number.

MUX and ADC

The MUX supports the inputs from SET1, SET2, SET3, SETA1, SETA2, IMONI_M, IMONI_A, TSEN or TSENA. The ADC converts these analog signals to digital codes for reporting or performance adjustment.

Current Balance

Each phase current sense signal is sent to the current balance circuit which adjusts the on-time of each phase to optimize current sharing.

Offset Cancellation

Cancel the current/voltage ripple issue to get the accurate VSEN.

UVLO

Detect the DVD and VCC voltage and issue POR signal as they are high enough.

DAC

Generate an analog signal according to the digital code generated by Control Logic.

Soft-Start & Slew Rate Control

Control the Dynamic VID slew rate of DAC according to the SetVID fast or SetVID slow.

Error Amp

Error amplifier generates COMP/COMPA signal by the difference between VSEN/VSENA and FB/FBA.

RSET/RSETA

The Ramp generator is designed to improve noise immunity and reduce jitter.

PWM CMP

The PWM comparator compares COMP signal and current feedback signal to generate a signal for TON trigger.

IMON Filter

IMON Filter is used to average sum current signal by analog RC filter.

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Table 1. IMVP8 VID Code Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	0	0	0	0	0	0	1	01	0.25
0	0	0	0	0	0	1	0	02	0.255
0	0	0	0	0	0	1	1	03	0.26
0	0	0	0	0	1	0	0	04	0.265
0	0	0	0	0	1	0	1	05	0.27
0	0	0	0	0	1	1	0	06	0.275
0	0	0	0	0	1	1	1	07	0.28
0	0	0	0	1	0	0	0	08	0.285
0	0	0	0	1	0	0	1	09	0.29
0	0	0	0	1	0	1	0	0A	0.295
0	0	0	0	1	0	1	1	0B	0.3
0	0	0	0	1	1	0	0	0C	0.305
0	0	0	0	1	1	0	1	0D	0.31
0	0	0	0	1	1	1	0	0E	0.315
0	0	0	0	1	1	1	1	0F	0.32
0	0	0	1	0	0	0	0	10	0.325
0	0	0	1	0	0	0	1	11	0.33
0	0	0	1	0	0	1	0	12	0.335
0	0	0	1	0	0	1	1	13	0.34
0	0	0	1	0	1	0	0	14	0.345
0	0	0	1	0	1	0	1	15	0.35
0	0	0	1	0	1	1	0	16	0.355
0	0	0	1	0	1	1	1	17	0.36
0	0	0	1	1	0	0	0	18	0.365
0	0	0	1	1	0	0	1	19	0.37
0	0	0	1	1	0	1	0	1A	0.375
0	0	0	1	1	0	1	1	1B	0.38
0	0	0	1	1	1	0	0	1C	0.385
0	0	0	1	1	1	0	1	1D	0.39
0	0	0	1	1	1	1	0	1E	0.395
0	0	0	1	1	1	1	1	1F	0.4
0	0	1	0	0	0	0	0	20	0.405
0	0	1	0	0	0	0	1	21	0.41
0	0	1	0	0	0	1	0	22	0.415
0	0	1	0	0	0	1	1	23	0.42
0	0	1	0	0	1	0	0	24	0.425

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VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	0	1	0	0	1	0	1	25	0.43
0	0	1	0	0	1	1	0	26	0.435
0	0	1	0	0	1	1	1	27	0.44
0	0	1	0	1	0	0	0	28	0.445
0	0	1	0	1	0	0	1	29	0.45
0	0	1	0	1	0	1	0	2A	0.455
0	0	1	0	1	0	1	1	2B	0.46
0	0	1	0	1	1	0	0	2C	0.465
0	0	1	0	1	1	0	1	2D	0.47
0	0	1	0	1	1	1	0	2E	0.475
0	0	1	0	1	1	1	1	2F	0.48
0	0	1	1	0	0	0	0	30	0.485
0	0	1	1	0	0	0	1	31	0.49
0	0	1	1	0	0	1	0	32	0.495
0	0	1	1	0	0	1	1	33	0.5
0	0	1	1	0	1	0	0	34	0.505
0	0	1	1	0	1	0	1	35	0.51
0	0	1	1	0	1	1	0	36	0.515
0	0	1	1	0	1	1	1	37	0.52
0	0	1	1	1	0	0	0	38	0.525
0	0	1	1	1	0	0	1	39	0.53
0	0	1	1	1	0	1	0	3A	0.535
0	0	1	1	1	0	1	1	3B	0.54
0	0	1	1	1	1	0	0	3C	0.545
0	0	1	1	1	1	0	1	3D	0.55
0	0	1	1	1	1	1	0	3E	0.555
0	0	1	1	1	1	1	1	3F	0.56
0	1	0	0	0	0	0	0	40	0.565
0	1	0	0	0	0	0	1	41	0.57
0	1	0	0	0	0	1	0	42	0.575
0	1	0	0	0	0	1	1	43	0.58
0	1	0	0	0	1	0	0	44	0.585
0	1	0	0	0	1	0	1	45	0.59
0	1	0	0	0	1	1	0	46	0.595
0	1	0	0	0	1	1	1	47	0.6
0	1	0	0	1	0	0	0	48	0.605
0	1	0	0	1	0	0	1	49	0.61

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VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	1	0	0	1	0	1	0	4A	0.615
0	1	0	0	1	0	1	1	4B	0.62
0	1	0	0	1	1	0	0	4C	0.625
0	1	0	0	1	1	0	1	4D	0.63
0	1	0	0	1	1	1	0	4E	0.635
0	1	0	0	1	1	1	1	4F	0.64
0	1	0	1	0	0	0	0	50	0.645
0	1	0	1	0	0	0	1	51	0.65
0	1	0	1	0	0	1	0	52	0.655
0	1	0	1	0	0	1	1	53	0.66
0	1	0	1	0	1	0	0	54	0.665
0	1	0	1	0	1	0	1	55	0.67
0	1	0	1	0	1	1	0	56	0.675
0	1	0	1	0	1	1	1	57	0.68
0	1	0	1	1	0	0	0	58	0.685
0	1	0	1	1	0	0	1	59	0.69
0	1	0	1	1	0	1	0	5A	0.695
0	1	0	1	1	0	1	1	5B	0.7
0	1	0	1	1	1	0	0	5C	0.705
0	1	0	1	1	1	0	1	5D	0.71
0	1	0	1	1	1	1	0	5E	0.715
0	1	0	1	1	1	1	1	5F	0.72
0	1	1	0	0	0	0	0	60	0.725
0	1	1	0	0	0	0	1	61	0.73
0	1	1	0	0	0	1	0	62	0.735
0	1	1	0	0	0	1	1	63	0.74
0	1	1	0	0	1	0	0	64	0.745
0	1	1	0	0	1	0	1	65	0.75
0	1	1	0	0	1	1	0	66	0.755
0	1	1	0	0	1	1	1	67	0.76
0	1	1	0	1	0	0	0	68	0.765
0	1	1	0	1	0	0	1	69	0.77
0	1	1	0	1	0	1	0	6A	0.775
0	1	1	0	1	0	1	1	6B	0.78
0	1	1	0	1	1	0	0	6C	0.785
0	1	1	0	1	1	0	1	6D	0.79
0	1	1	0	1	1	1	0	6E	0.795

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VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	1	1	0	1	1	1	1	6F	0.8
0	1	1	1	0	0	0	0	70	0.805
0	1	1	1	0	0	0	1	71	0.81
0	1	1	1	0	0	1	0	72	0.815
0	1	1	1	0	0	1	1	73	0.82
0	1	1	1	0	1	0	0	74	0.825
0	1	1	1	0	1	0	1	75	0.83
0	1	1	1	0	1	1	0	76	0.835
0	1	1	1	0	1	1	1	77	0.84
0	1	1	1	1	0	0	0	78	0.845
0	1	1	1	1	0	0	1	79	0.85
0	1	1	1	1	0	1	0	7A	0.855
0	1	1	1	1	0	1	1	7B	0.86
0	1	1	1	1	1	0	0	7C	0.865
0	1	1	1	1	1	0	1	7D	0.87
0	1	1	1	1	1	1	0	7E	0.875
0	1	1	1	1	1	1	1	7F	0.88
1	0	0	0	0	0	0	0	80	0.885
1	0	0	0	0	0	0	1	81	0.89
1	0	0	0	0	0	1	0	82	0.895
1	0	0	0	0	0	1	1	83	0.9
1	0	0	0	0	1	0	0	84	0.905
1	0	0	0	0	1	0	1	85	0.91
1	0	0	0	0	1	1	0	86	0.915
1	0	0	0	0	1	1	1	87	0.92
1	0	0	0	1	0	0	0	88	0.925
1	0	0	0	1	0	0	1	89	0.93
1	0	0	0	1	0	1	0	8A	0.935
1	0	0	0	1	0	1	1	8B	0.94
1	0	0	0	1	1	0	0	8C	0.945
1	0	0	0	1	1	0	1	8D	0.95
1	0	0	0	1	1	1	0	8E	0.955
1	0	0	0	1	1	1	1	8F	0.96
1	0	0	1	0	0	0	0	90	0.965
1	0	0	1	0	0	0	1	91	0.97
1	0	0	1	0	0	1	0	92	0.975
1	0	0	1	0	0	1	1	93	0.98

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VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	0	0	1	0	1	0	0	94	0.985
1	0	0	1	0	1	0	1	95	0.99
1	0	0	1	0	1	1	0	96	0.995
1	0	0	1	0	1	1	1	97	1
1	0	0	1	1	0	0	0	98	1.005
1	0	0	1	1	0	0	1	99	1.01
1	0	0	1	1	0	1	0	9A	1.015
1	0	0	1	1	0	1	1	9B	1.02
1	0	0	1	1	1	0	0	9C	1.025
1	0	0	1	1	1	0	1	9D	1.03
1	0	0	1	1	1	1	0	9E	1.035
1	0	0	1	1	1	1	1	9F	1.04
1	0	1	0	0	0	0	0	A0	1.045
1	0	1	0	0	0	0	1	A1	1.05
1	0	1	0	0	0	1	0	A2	1.055
1	0	1	0	0	0	1	1	A3	1.06
1	0	1	0	0	1	0	0	A4	1.065
1	0	1	0	0	1	0	1	A5	1.07
1	0	1	0	0	1	1	0	A6	1.075
1	0	1	0	0	1	1	1	A7	1.08
1	0	1	0	1	0	0	0	A8	1.085
1	0	1	0	1	0	0	1	A9	1.09
1	0	1	0	1	0	1	0	AA	1.095
1	0	1	0	1	0	1	1	AB	1.1
1	0	1	0	1	1	0	0	AC	1.105
1	0	1	0	1	1	0	1	AD	1.11
1	0	1	0	1	1	1	0	AE	1.115
1	0	1	0	1	1	1	1	AF	1.12
1	0	1	1	0	0	0	0	B0	1.125
1	0	1	1	0	0	0	1	B1	1.13
1	0	1	1	0	0	1	0	B2	1.135
1	0	1	1	0	0	1	1	B3	1.14
1	0	1	1	0	1	0	0	B4	1.145
1	0	1	1	0	1	0	1	B5	1.15
1	0	1	1	0	1	1	0	B6	1.155
1	0	1	1	0	1	1	1	B7	1.16
1	0	1	1	1	0	0	0	B8	1.165

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VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	0	1	1	1	0	0	1	B9	1.17
1	0	1	1	1	0	1	0	BA	1.175
1	0	1	1	1	0	1	1	BB	1.18
1	0	1	1	1	1	0	0	BC	1.185
1	0	1	1	1	1	0	1	BD	1.19
1	0	1	1	1	1	1	0	BE	1.195
1	0	1	1	1	1	1	1	BF	1.2
1	1	0	0	0	0	0	0	C0	1.205
1	1	0	0	0	0	0	1	C1	1.21
1	1	0	0	0	0	1	0	C2	1.215
1	1	0	0	0	0	1	1	C3	1.22
1	1	0	0	0	1	0	0	C4	1.225
1	1	0	0	0	1	0	1	C5	1.23
1	1	0	0	0	1	1	0	C6	1.235
1	1	0	0	0	1	1	1	C7	1.24
1	1	0	0	1	0	0	0	C8	1.245
1	1	0	0	1	0	0	1	C9	1.25
1	1	0	0	1	0	1	0	CA	1.255
1	1	0	0	1	0	1	1	CB	1.26
1	1	0	0	1	1	0	0	CC	1.265
1	1	0	0	1	1	0	1	CD	1.27
1	1	0	0	1	1	1	0	CE	1.275
1	1	0	0	1	1	1	1	CF	1.28
1	1	0	1	0	0	0	0	D0	1.285
1	1	0	1	0	0	0	1	D1	1.29
1	1	0	1	0	0	1	0	D2	1.295
1	1	0	1	0	0	1	1	D3	1.3
1	1	0	1	0	1	0	0	D4	1.305
1	1	0	1	0	1	0	1	D5	1.31
1	1	0	1	0	1	1	0	D6	1.315
1	1	0	1	0	1	1	1	D7	1.32
1	1	0	1	1	0	0	0	D8	1.325
1	1	0	1	1	0	0	1	D9	1.33
1	1	0	1	1	0	1	0	DA	1.335
1	1	0	1	1	0	1	1	DB	1.34
1	1	0	1	1	1	0	0	DC	1.345
1	1	0	1	1	1	0	1	DD	1.35

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VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	1	0	1	1	1	1	0	DE	1.355
1	1	0	1	1	1	1	1	DF	1.36
1	1	1	0	0	0	0	0	E0	1.365
1	1	1	0	0	0	0	1	E1	1.37
1	1	1	0	0	0	1	0	E2	1.375
1	1	1	0	0	0	1	1	E3	1.38
1	1	1	0	0	1	0	0	E4	1.385
1	1	1	0	0	1	0	1	E5	1.39
1	1	1	0	0	1	1	0	E6	1.395
1	1	1	0	0	1	1	1	E7	1.4
1	1	1	0	1	0	0	0	E8	1.405
1	1	1	0	1	0	0	1	E9	1.41
1	1	1	0	1	0	1	0	EA	1.415
1	1	1	0	1	0	1	1	EB	1.42
1	1	1	0	1	1	0	0	EC	1.425
1	1	1	0	1	1	0	1	ED	1.43
1	1	1	0	1	1	1	0	EE	1.435
1	1	1	0	1	1	1	1	EF	1.44
1	1	1	1	0	0	0	0	F0	1.445
1	1	1	1	0	0	0	1	F1	1.45
1	1	1	1	0	0	1	0	F2	1.455
1	1	1	1	0	0	1	1	F3	1.46
1	1	1	1	0	1	0	0	F4	1.465
1	1	1	1	0	1	0	1	F5	1.47
1	1	1	1	0	1	1	0	F6	1.475
1	1	1	1	0	1	1	1	F7	1.48
1	1	1	1	1	0	0	0	F8	1.485
1	1	1	1	1	0	0	1	F9	1.49
1	1	1	1	1	0	1	0	FA	1.495
1	1	1	1	1	0	1	1	FB	1.5
1	1	1	1	1	1	0	0	FC	1.505
1	1	1	1	1	1	0	1	FD	1.51
1	1	1	1	1	1	1	0	FE	1.515
1	1	1	1	1	1	1	1	FF	1.52

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Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6.5V
- PVCC to GND ---------- –0.3V to 15V
- RGND to GND ---------- –0.3V to 0.3V
- TONSET to GND ---------- –0.3V to 28
- BOOTx to PHASEx ---------- –0.3V to 15V
- PHASEx to GND
  DC ---------- –0.3V to 30V
  <20ns ---------- –10V to 35V
- LGATEx to GND
  DC ---------- –0.3V to (VCC + 0.3V)
  <20ns ---------- –2V to (VCC + 0.3V)
- UGATEx to GND
  DC ---------- (V_{PHASE} – 0.3V) to (V_{BOOT} + 0.3V)
  <20ns ---------- (V_{PHASE} – 2V) to (V_{BOOT} + 0.3V)
- Other Pins ---------- –0.3V to (V_{CC} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-60L 7x7 ---------- 3.92W
- Package Thermal Resistance (Note 2)
  WQFN-60L 7x7, θ_{JA} ---------- 25.5°C/W
  WQFN-60L 7x7, θ_{JC} ---------- 6.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

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Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{VCC}	V_{EN} = H, No Switching	--	13	--	mA
Supply Current at PS4	I_{VCC_PS4}	V_{EN} = H, No Switching	--	0.1	--	mA
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	5	μA
Reference and DAC						
DAC Accuracy	V_{FB}	VDAC = 0.75V – 1.52V	–0.5%	0	0.5%	% of VID
		VDAC = 0.5V – 0.745V	–8	0	8	mV
		VDAC = 0.25V – 0.495V	–10	0	10	mV
Slew Rate						
Dynamic VID Slew Rate	SR (S Line)	Set VID Fast	--	11.25	--	mV/μs
		Set VID Slow	--	5.625	--	mV/μs
Dynamic VID Slew Rate	SR (H, Y, U Line)	Set VID Fast	--	33.75	--	mV/μs
		Set VID Slow	--	16.875	--	mV/μs
EA						
DC Gain	EAGAIN	R_L = 47kΩ	70	--	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	--	5	--	MHz
Output Voltage Range	V_{COMP}	R_L = 47kΩ	0.5	--	3.6	V
Max Source/Sink Current	I_{OUTEA}	V_{COMP} = 2V	--	5	--	mA
Load Line Current Gain Amplifier						
Input Offset Voltage	V_{ILOFS}	V_{IMON} = 1V	–5	--	5	mV
Current Gain	AILGAIN	$V_{IMON} – V_{VREF}$ = 1V $V_{FB} = V_{COMP}$ = 1V	--	1/3	--	A/A
Current Sensing Amplifier						
Input Offset Voltage	V_{OSCS}		–0.5	--	0.5	mV
Impedance at Positive Input	RISENxP		1	--	--	MΩ
Current Mirror Gain	AMIRROR	IIMON/ISENxN	0.97	1	1.03	A/A
TON Setting						
TON Pin Voltage	V_{TON}	I_{RTON} = 26.8μA, VDAC = 1V	0.9	1	1.1	V
On-Time Setting	T_{ON}	I_{RTON} = 26.8μA, VDAC = 1V	189	210	231	ns
Input Current Range	I_{RTON}	VDAC = 1V	6	--	70	μA
Minimum Off time	T_{OFF}	VDAC = 1V	--	180	--	ns
IBIAS						
IBIAS Pin Voltage	V_{IBIAS}	R_{IBIAS} = 100kΩ	1.9	2	2.1	V

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protections						
Under-Voltage Lockout Threshold	V_{UVLO}	Falling edge	3.95	4.05	4.15	V
	ΔV_{UVLO}	Rising edge hysteresis	--	190	--	mV
Over-Voltage Protection Threshold	V_{OV}	Respect to VID voltage	VID + 300	VID + 350	VID + 400	mV
		Lower limit to 1V	1300	1350	1400	mV
Negative Voltage Protection Threshold	V_{NV}		–100	–70	--	mV
EN and VR_REDAY						
EN Input Voltage	V_{IH}	Respect to 1V, 70%	0.7	--	--	V
	V_{IL}	Respect to 1V, 30%	--	--	0.3	V
Leakage Current of EN			–1	--	1	μA
PGOOD Pull Low Voltage	V_{PGOOD}	I_{VR_Ready} = 10mA	--	--	0.13	V
DVD (Note 5)						
DVD Input High Voltage	V_{IH}	V_{DVD} = 2V or above, VR judge VIN high	2	--	--	V
DVD Input low Voltage	V_{IL}	V_{DVD} = 1.3V or below, VR judge VIN low	--	--	1.3	V
Serial VID and $\overline{\text{VR_HOT}}$						
VCLK, VDIO	V_{IH}	Respect to INTEL Spec. with 50mV hysteresis	0.65	--	--	V
	V_{IL}		--	--	0.45	
Leakage Current of VCLK, VDIO, $\overline{\text{ALERT}}$ and $\overline{\text{VR_HOT}}$	I_{LEAK_IN}		–1	--	1	μA
VDIO, $\overline{\text{ALERT}}$ and $\overline{\text{VR_HOT}}$ Pull Low Voltage		I_{VDIO} = 10mA	--	--	0.13	V
		$I_{\overline{ALERT}}$ = 10mA				
		$I_{\overline{VR_HOT}}$ = 10mA				
VREF						
VREF Voltage	V_{REF}		0.55	0.6	0.65	V
ADC						
Digital IMON Setting	V_{IMON}	$V_{IMON} - V_{IMON_INI}$ = 1.6V	--	255	--	Decimal
		$V_{IMON} - V_{IMON_INI}$ = 0.8V	--	128	--	Decimal
		$V_{IMON} - V_{IMON_INI}$ = 0V	--	0	--	Decimal
PSYS						
Digital PSYS Setting	V_{PSYS}	V_{PSYS} = 3.2V	--	255	--	Decimal
		V_{PSYS} = 1.6V	--	128	--	Decimal
		V_{PSYS} = 0V	--	0	--	Decimal

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Update Period	T_{IMON}		--	125	--	μs
TSEN Threshold for Tmp_Zone[7] Transition	V_{TSEN}	100°C	--	1.092	--	V
TSEN Threshold for Tmp_Zone[6] Transition		97°C	--	1.132	--	
TSEN Threshold for Tmp_Zone[5] Transition		94°C	--	1.176	--	
TSEN Threshold for Tmp_Zone[4] Transition		91°C	--	1.226	--	
TSEN Threshold for Tmp_Zone[3] Transition		88°C	--	1.283	--	
TSEN Threshold for Tmp_Zone[2] Transition		85°C	--	1.346	--	
TSEN Threshold for Tmp_Zone[1] Transition		82°C	--	1.418	--	
TSEN Threshold for Tmp_Zone[0] Transition		75°C	--	1.624	--	
Update Period	T_{tsen}		--	100	--	μs
Digital Code of ICCMAX	CICCMAX1	V_{REF} = 3.2V, V_{SETI} = 0.404V, V_{SETA1} = 0.404V	61	64	67	Decimal
	CICCMAX2	V_{REF} = 3.2V, V_{SETI} = 0.804V, V_{SETA1} = 0.804V	125	128	131	Decimal
	CICCMAX3	V_{REF} = 3.2V, V_{SETI} = 1.592V, V_{SETA1} = 1.592V	251	254	255	Decimal
Timing						
UGATEx Rising Time	t_{UGATEr}	3nF load	--	25	--	ns
UGATEx Falling Time	t_{UGATEf}	3nF load	--	12	--	ns
LGATEx Rising Time	t_{LGATEr}	3nF load	--	24	--	ns
LGATEx Falling Time	t_{LGATEf}	3nF load	--	10	--	ns
Propagation Delay	$t_{UGATEpgh}$	V_{BOOTx} – V_{PHASEx} = 12V See Timing Diagram	--	60	--	ns
	$t_{UGATEpdl}$		--	22	--	
	$t_{LGATEpdh}$	See Timing Diagram	--	30	--	ns
	$t_{LGATEpdl}$		--	8	--	
Output						
UGATEx Drive Source	$R_{UGATEsr}$	V_{BOOT} – V_{PHASE} = 12V, I_{Source} = 100mA	--	1.7	--	Ω
UGATEx Drive Sink	$R_{UGATEsk}$	V_{BOOT} – V_{PHASE} = 12V, I_{Sink} = 100mA	--	1.4	--	Ω
LGATEx Drive Source	$R_{LGATEsr}$	I_{Source} = 100mA	--	1.6	--	Ω
LGATEx Drive Sink	$R_{LGATEsk}$	I_{Sink} = 100mA	--	1.1	--	Ω
PWM Driving Capability						
PWM Source Resistance	R_{PWM_SRC}		--	30	--	Ω
PWM Sink Resistance	R_{PWM_SNK}		--	10	--	Ω

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Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5.(1) DVD Input High Voltage: DVD pin is an input pin of VR. VR always identify high level while the voltage given at DVD pin >= 2V. The high-low transition is within 1.3V ~2V.

(2) DVD Input low Voltage: DVD pin is an input pin of VR. VR always identify low level while the voltage given at DVD pin <= 1.3V. The high-low transition is within 1.3V ~2V.

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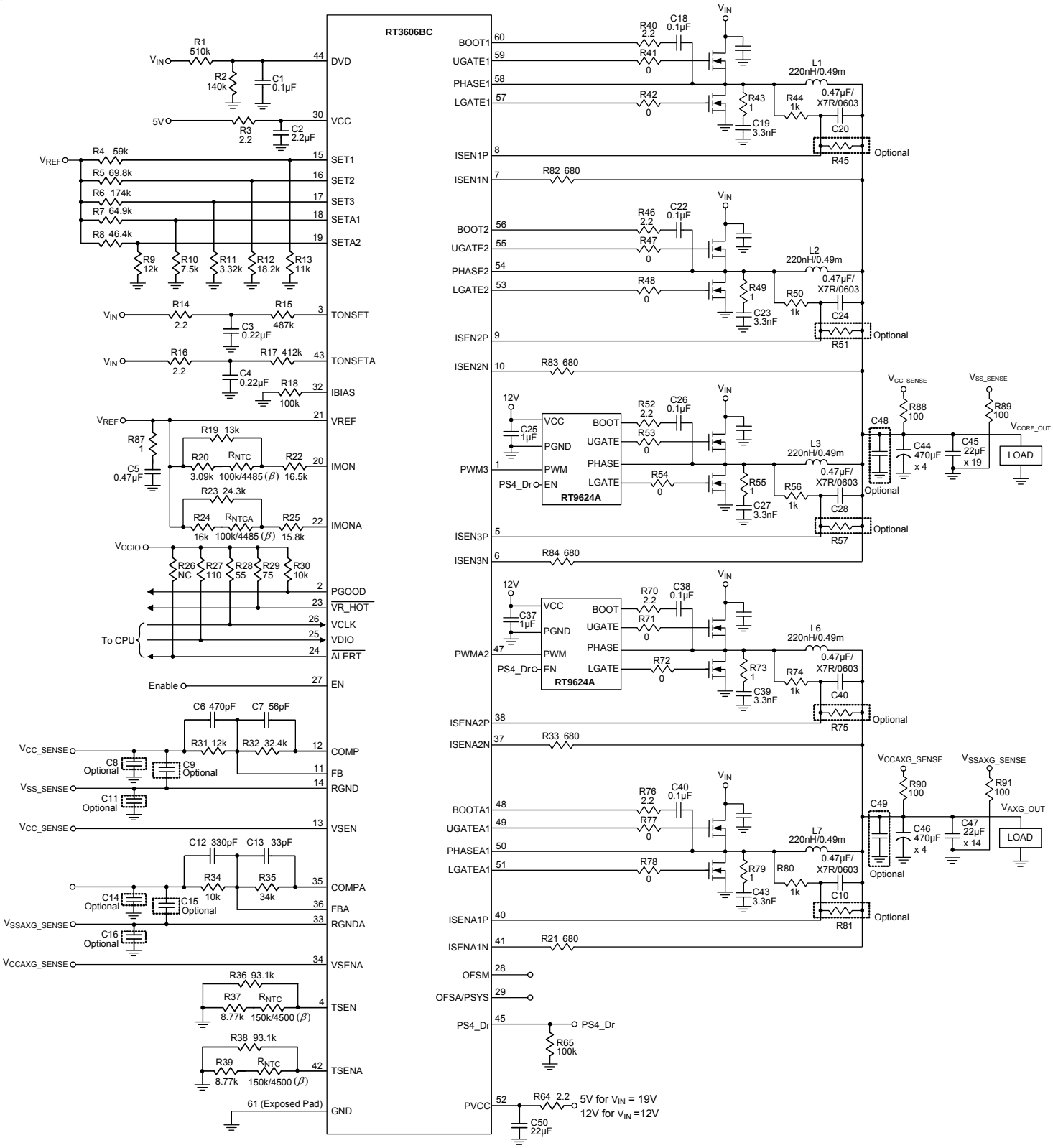
Typical Application Circuit

Discrete MOS



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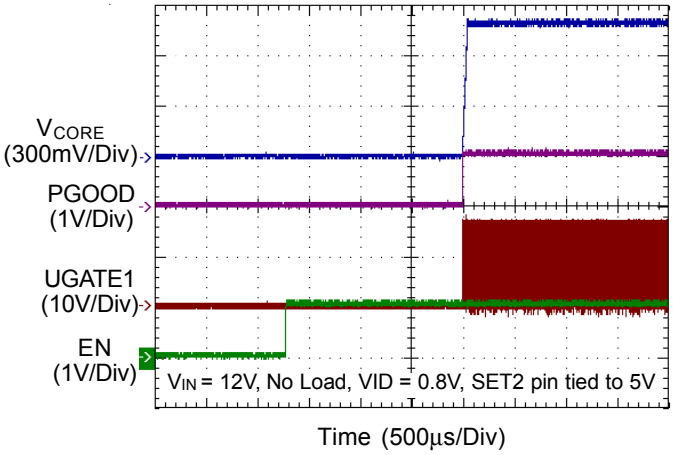
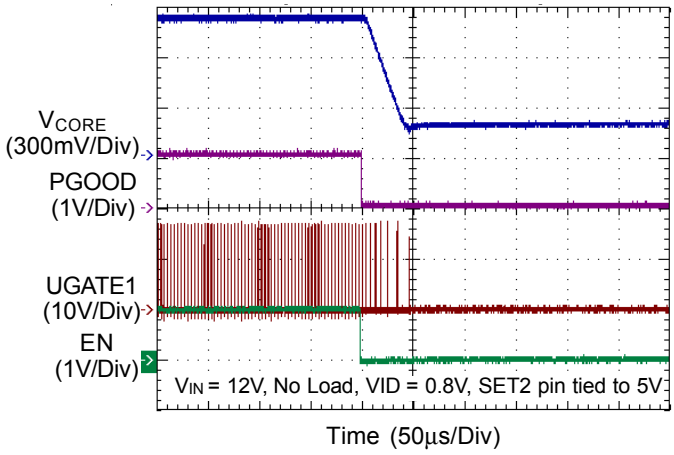
Typical Operating Characteristics

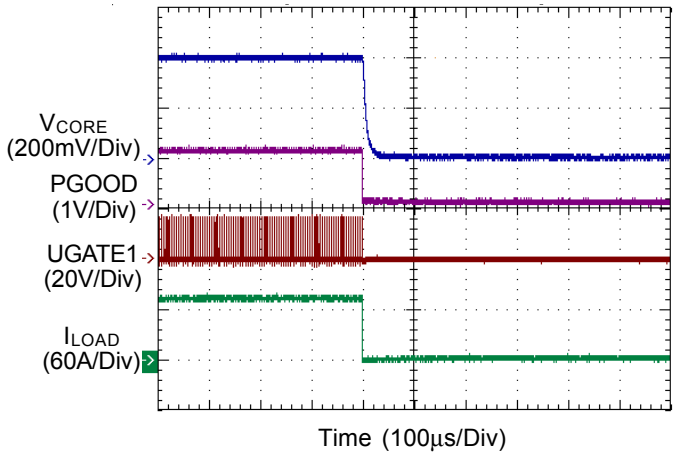
CORE VR Power On from EN



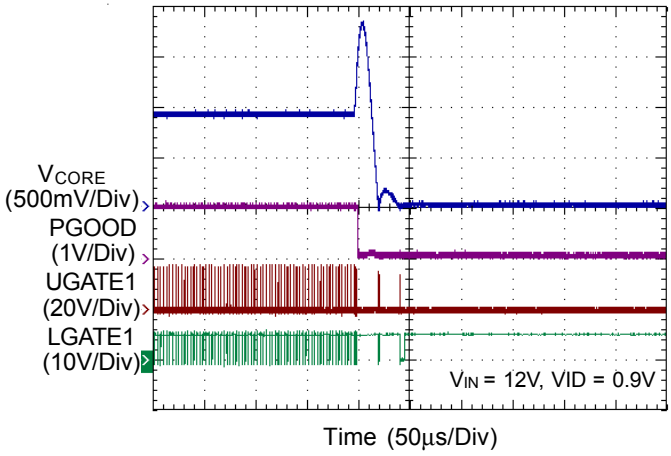
CORE VR Power Off from EN



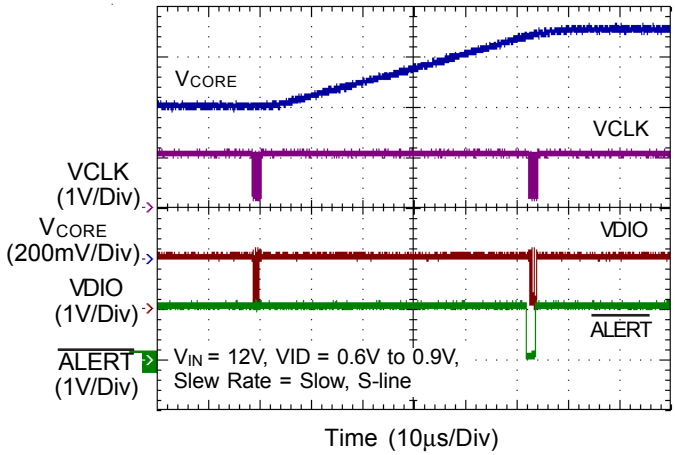
CORE VR OCP



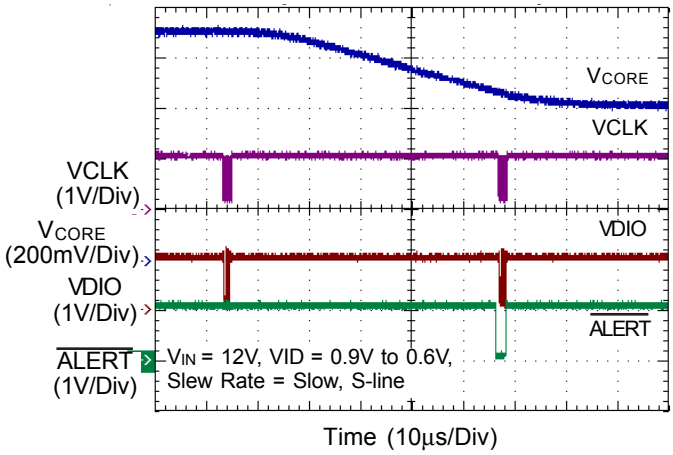
CORE VR OVP



CORE VR Dynamic VID Up



CORE VR Dynamic VID Down



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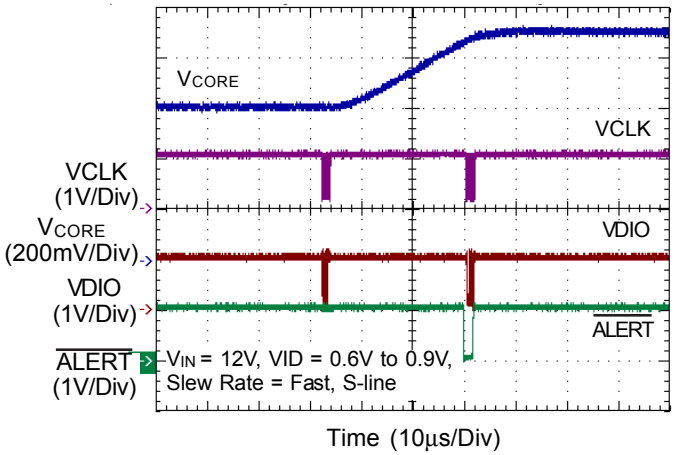
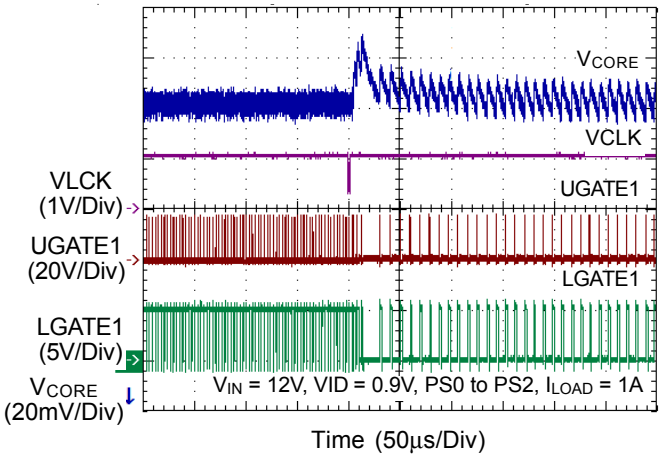
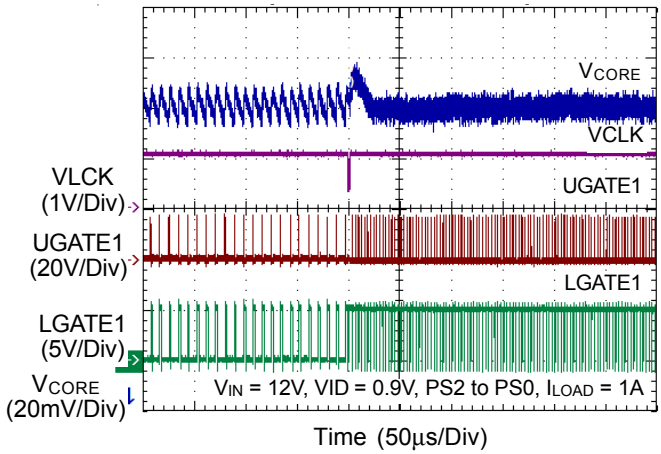
CORE VR Dynamic VID Up



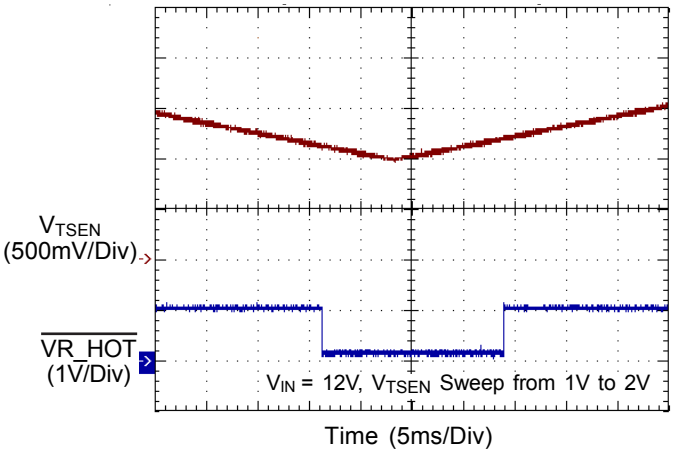
CORE VR Mode Transient



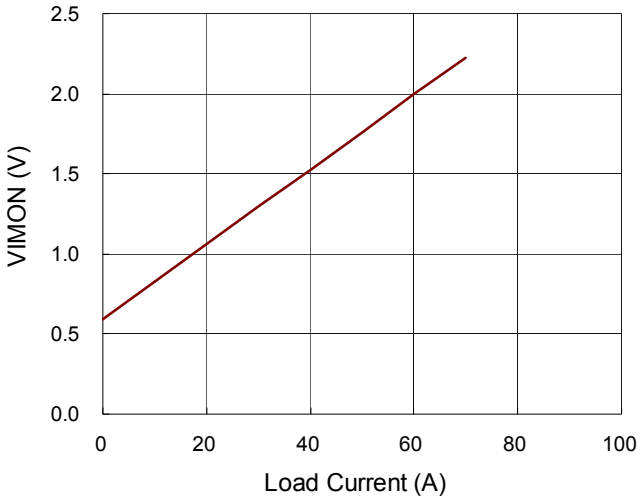
CORE VR Mode Transient



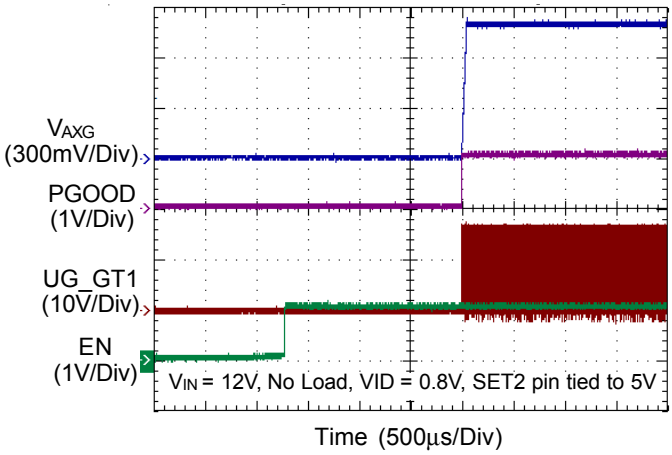
CORE VR Thermal Monitioring



VIMON vs. Load Current



AXG VR Power On from EN



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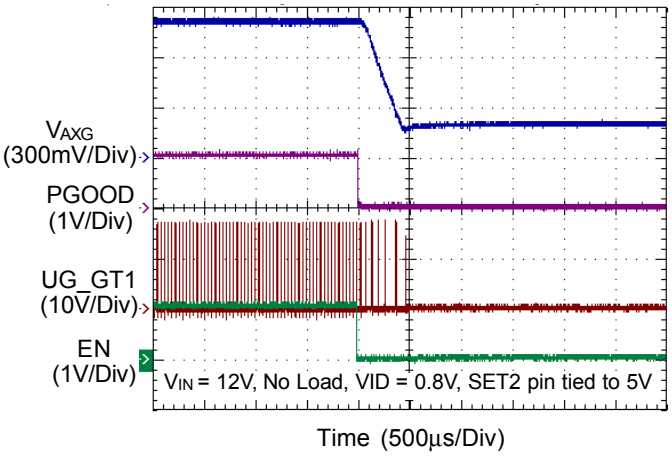
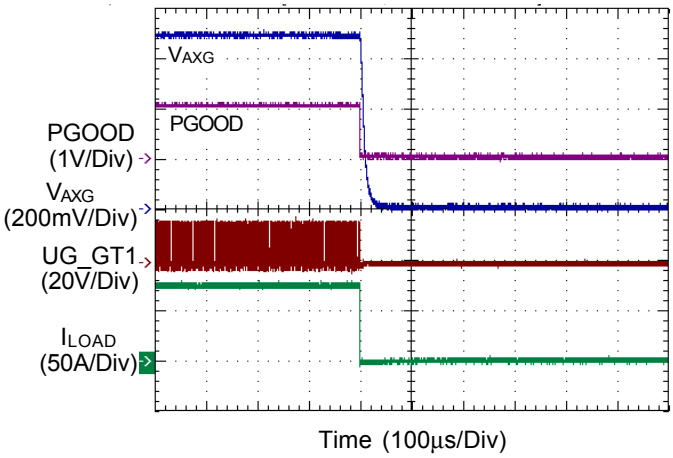
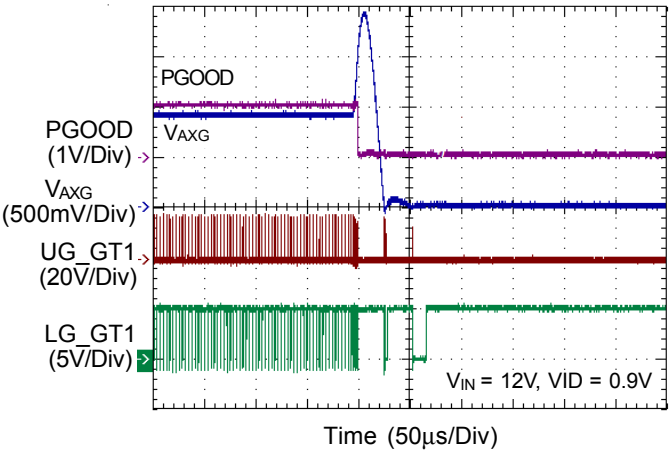
AXG VR Power Off from EN



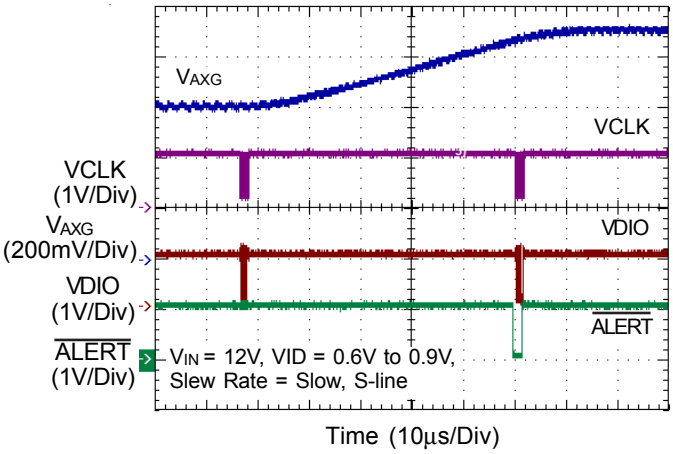
AXG VR OCP



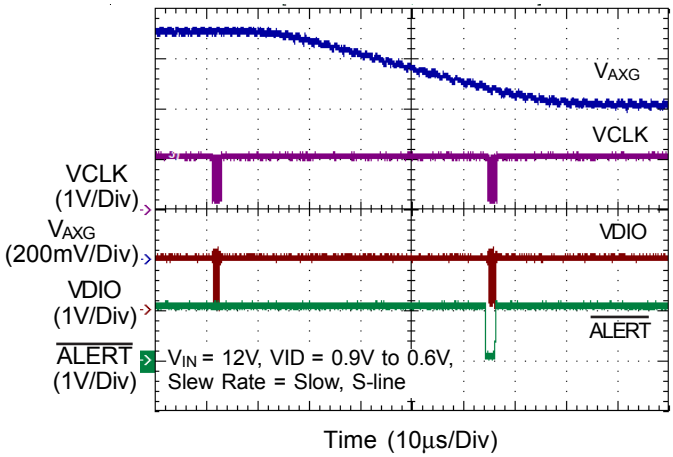
AXG VR OVP



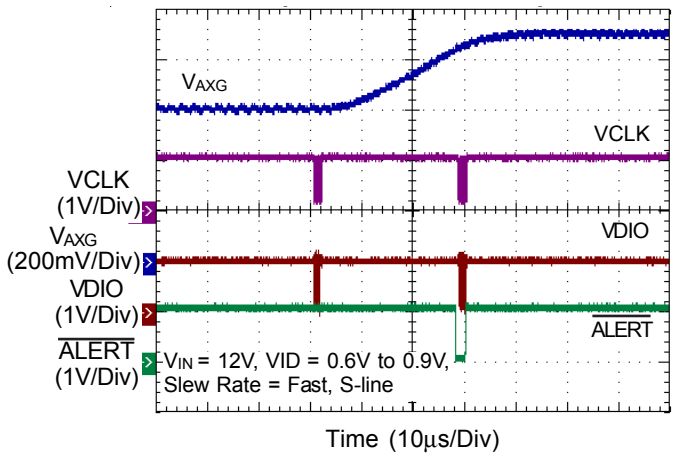
AXG VR Dynamic VID Up



AXG VR Dynamic VID Down



AXG VR Dynamic VID Up



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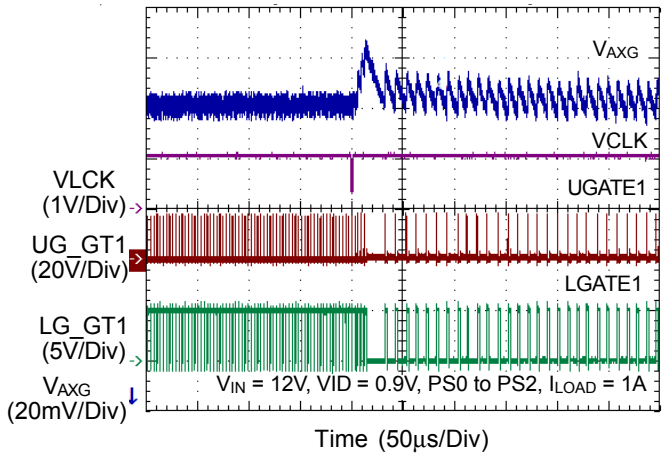
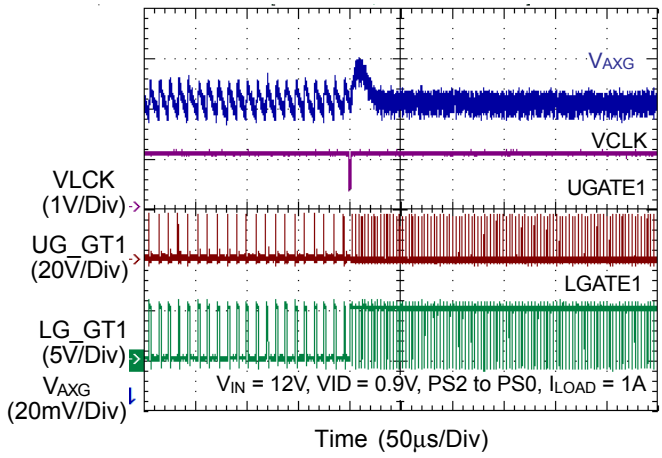
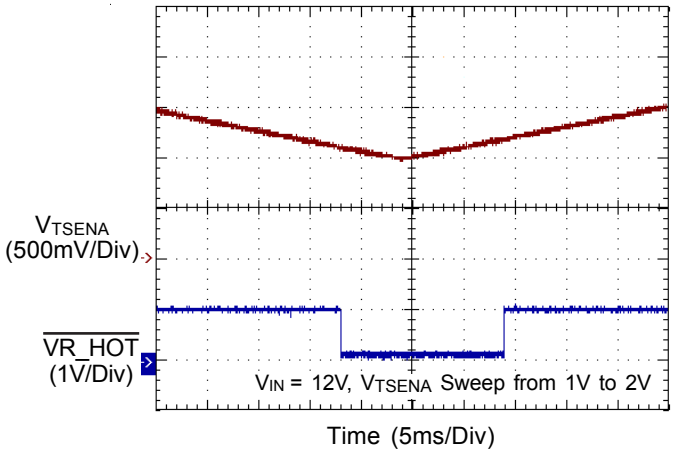
AXG VR Mode Transient



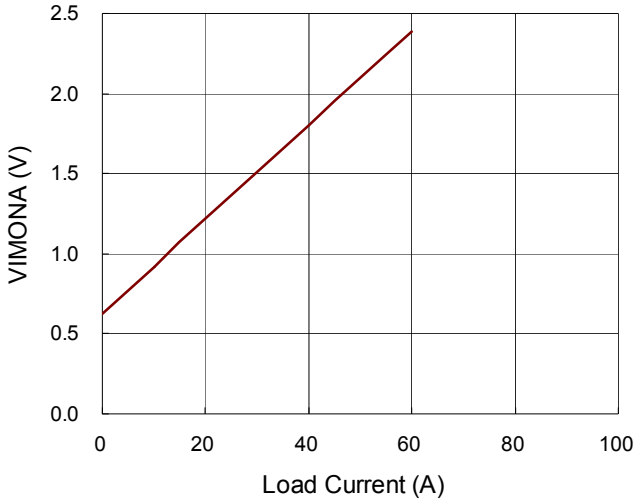
AXG VR Mode Transient



AXG VR Thermal Monitioring



VIMONA vs. Load Current



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Applications information

The RT3606BC includes two voltage rails : a 3/2/1 multiphase synchronous buck controller, the CORE VR, and a 2/1 multiphase synchronous buck controller, the AXG VR, designed to meet Intel IMVP8 compatible CPUs specification with a serial SVID control interface. The controller uses an ADC to implement the all kinds of settings to save total pin number for easy use and increasing PCB space utilization. RT3606BC is used in notebook, desktop computers and servers.

General loop Function

G-NAVP™ Control Mode

The RT3606BC adopts the G-NAVP™ controller, which is a current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. When current feedback signal reaches comp signal, the RT3606BC generates an on-time width to achieve PWM modulation. Figure 1 shows the basic G-NAVP™ behavior waveforms in continuous conduct mode (CCM).

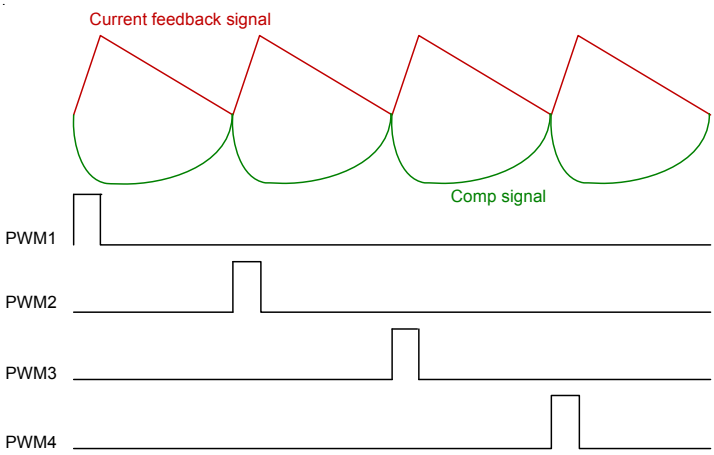

Figure 1 (a). G-NAVP™ CCM behavior waveforms in CCM in Steady State

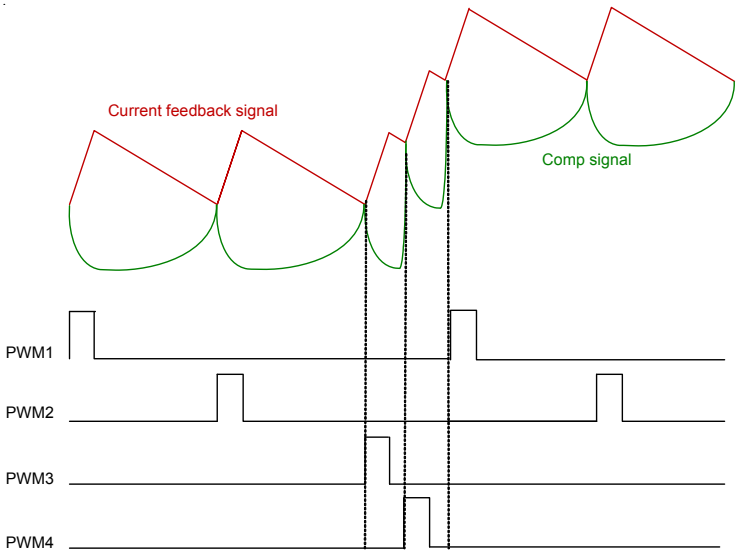

Figure 1 (b). G-NAVP™ CCM behavior waveforms in CCM in Load Transient.

Diode Emulation Mode (DEM)

As well-known, the dominate power loss is switching related loss during light load, hence VR needs to be operated in asynchronous mode (or called discontinuous conduct mode, DCM) to reduce switching related loss since switching frequency is dependent on loading in the asynchronous mode. The RT3606BC can operate in diode emulation mode (DEM) to improve light load efficiency. In DEM operation, the behavior of the low side MOSFET(s) needs to work like a diode, that is, the low side MOSFET(s) will be turned on when the phase voltage is a negative value, i.e. the inductor current follows from Source to Drain of low-side MOSFET(s). And the low-side MOSFET(s) will be turned off when phase voltage is a positive value, i.e. reversed current is not allowed. Figure 2 shows the control behavior in DEM. Figure 3 shows the G-NAVP™ operation in DEM to illustrate the control behaviors. When load decreases, the discharge time of output capacitors increases during UGATE and LGATE are turned off. Hence, the switching frequency and switching loss will be reduced to improve efficiency in light load condition.

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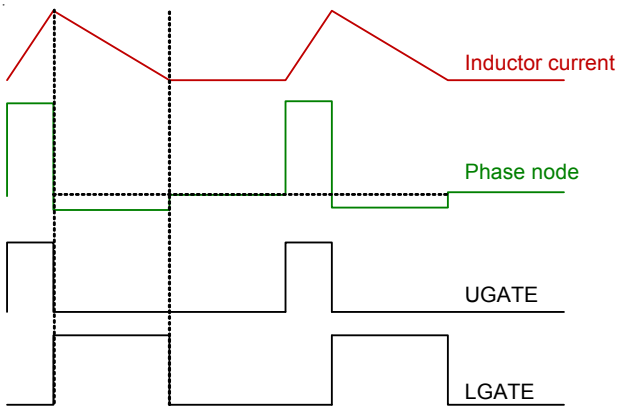

Figure 2. Diode Emulation Mode (DEM) in Steady State

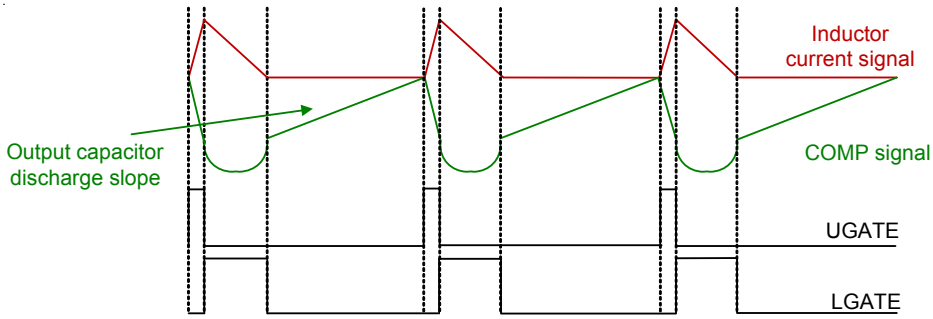

Figure 3. (a)

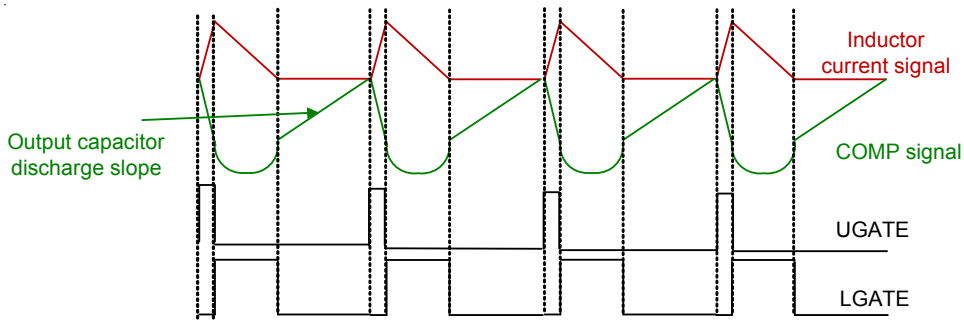

Figure 3. (b)

Figure 3. G-NAVP^{TM} operation in DEM. (a) : The load is lighter, output capacitor discharge slope is smaller and the switching frequency is lower. (b) : The load is increasing, output capacitor discharge slope is increased and switching frequency is increased, too.

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Phase Interleaving Function

RT3606BC is a multiphase controller, which has a phase interleaving function, 120 degree phase shift for 3-phase operation and 180 degree phase shift for 2-phase operation which can help reduce output voltage ripple and EMI problem.

Multi-Function Pin Setting Mechanism

For reducing total pin number of package, SET [1:3] and SETA[1:2] pins adopt the multi-function pin setting mechanism in the RT3606BC. SET [1:3] and SETA[1:2] are used to set CORE VR and AXG VR, respectively. Figure 4 illustrates this operating mechanism. The voltage at VREF pin will be pulled up to 3.2V after power ready (POR). First, external voltage divider is used to set the Function1 and then internal current source 80μA is used to set the Function2. The setting voltage of Function1 and Function2 can be represented as

$$V_{Function1} = \frac{R2}{R1+R2} \times 3.2V$$

$$V_{Function2} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

All function setting will be done within 500ì s after power ready (POR), and the voltage at VREF pin will fix to 0.6V after all function setting over.

If $V_{Function1}$ and $V_{Function2}$ are determined, R1 and R2 can be calculated as follows :

$$R1 = \frac{3.2V \times V_{Function2}}{80\mu A \times V_{Function1}}$$

$$R2 = \frac{R1 \times V_{Function1}}{3.2V - V_{Function1}}$$

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the SETx and SETAx resistor network for RT3606BC.

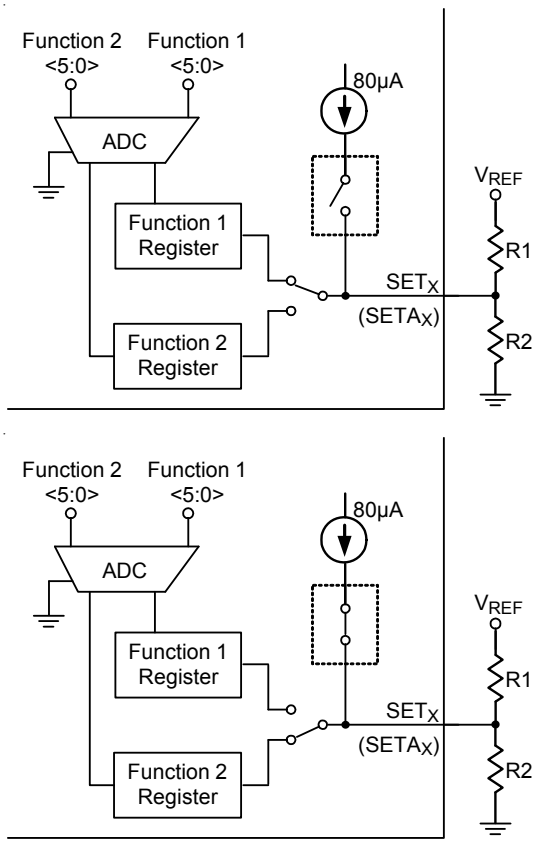

Figure 4. Multi-Function Pin Setting Mechanism

Connects a R3 resistor from SETx pin or SETAx pin to the middle node of voltage divider can help to fine tune the set voltage of Function2, which does not affect the set voltage of Function1. The Figure 5 shows the setting method and the set voltage of Function 1 and Function2 can be represented as :

$$V_{Function1} = \frac{R2}{R1+R2} \times 3.2V$$

$$V_{Function2} = 80\mu A \times \left(R3 + \frac{R1 \times R2}{R1+R2}\right)$$

By the way, SET1 and SET2 are used to set CORE rail setting and SETA1 and SETA2 are used to set AXG rail setting. The setting of SET3 is suitable for both CORE rail and AXG rail. Table 2 summarizes the overall pin setting function. Table 3 and Table 4 show the SET3 pin setting function table.

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Table 2. Pin Setting Function Table

	Function1	Function2
Set1 (CORE Rail)	ICCMAX	DVID threshold Over Current Protection (OCP) threshold
Set2 (CORE Rail)	DVID width Ramp Amplitude	Quick Response (QR) threshold Quick Response (QR) width
Set3 (CORE / AXG Rail)	VR Address Enable Zero Load-line Enable Anti-overshoot Function Anti-overshoot Behavior Current Gain AI	Enable PSYS Function Enable High Switching Frequency Ramp DVID Slew Rate Disable DVID compensation Decrease GTU/SA Ramp Amplitude (Only Active in max phase = 1 Application)
SetA1 (AXG Rail)	ICCMAXA	DVID threshold Over Current Protection (OCP) threshold
SetA2 (AXG Rail)	DVID width Ramp Amplitude	Quick Response (QR) threshold Quick Response (QR) width

Table 3. SET3 Pin Setting for VR Address, Enable Zero Load-line, Enable Anti-overshoot Function, Anti-overshoot Behavior, and Current Gain AI

$V_{SET3} = \frac{R2}{R1+R2} \times 3.2V$				VR Address	Zero Load Line	ANTI_OVS	AHTI_OVS Behavior	AI GAIN
Min	Typical	Max	Unit					
0.000	10.948	21.896	mV	CORE : 00 AXG : 01	CORE : With LL AXG : With LL	Disable	High-Low-Floating	1X
25.024	35.973	46.921	mV					2X
50.049	60.997	71.945	mV				High-Floating	1X
75.073	86.022	96.970	mV					2X
100.098	111.046	121.994	mV			Enable	High-Low-Floating	1X
125.122	136.070	147.019	mV					2X
150.147	161.095	172.043	mV				High-Floating	1X
175.171	186.119	197.067	mV					2X
200.196	211.144	222.092	mV		CORE : With LL AXG : W/O LL	Disable	High-Low-Floating	1X
225.220	236.168	247.116	mV					2X
250.244	261.193	272.141	mV				High-Floating	1X
275.269	286.217	297.165	mV					2X
300.293	311.241	322.190	mV			Enable	High-Low-Floating	1X
325.318	336.266	347.214	mV					2X
350.342	361.290	372.239	mV				High-Floating	1X
375.367	386.315	397.263	mV					2X

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$V_{SET3} = \frac{R2}{R1+R2} \times 3.2V$				VR Address	Zero Load Line	ANTI_OVS	AHTI_OVS Behavior	AI GAIN
Min	Typical	Max	Unit					
400.391	411.339	422.287	mV	CORE : 00 AXG : 02	CORE : With LL AXG : With LL	Disable	High-Low-Floating	1X
425.415	436.364	447.312	mV					2X
450.440	461.388	472.336	mV				High-Floating	1X
475.464	486.413	497.361	mV					2X
500.489	511.437	522.385	mV			Enable	High-Low-Floating	1X
525.513	536.461	547.410	mV					2X
550.538	561.486	572.434	mV				High-Floating	1X
575.562	586.510	597.458	mV					2X
600.587	611.535	622.483	mV		CORE : With LL AXG : W/O LL	Disable	High-Low-Floating	1X
625.611	636.559	647.507	mV					2X
650.635	661.584	672.532	mV				High-Floating	1X
675.660	686.608	697.556	mV					2X
700.684	711.632	722.581	mV			Enable	High-Low-Floating	1X
725.709	736.657	747.605	mV					2X
750.733	761.681	772.630	mV				High-Floating	1X
775.758	786.706	797.654	mV					2X
800.782	811.730	822.678	mV	CORE : 01 AXG : 00	CORE : With LL AXG : With LL	Disable	High-Low-Floating	1X
825.806	836.755	847.703	mV					2X
850.831	861.779	872.727	mV				High-Floating	1X
875.855	886.804	897.752	mV					2X
900.880	911.828	922.776	mV			Enable	High-Low-Floating	1X
925.904	936.852	947.801	mV					2X
950.929	961.877	972.825	mV				High-Floating	1X
975.953	986.901	997.849	mV					2X
1000.978	1011.926	1022.874	mV		CORE : W/O LL AXG : With LL	Disable	High-Low-Floating	1X
1026.002	1036.950	1047.898	mV					2X
1051.026	1061.975	1072.923	mV				High-Floating	1X
1076.051	1086.999	1097.947	mV					2X
1101.075	1112.023	1122.972	mV			Enable	High-Low-Floating	1X
1126.100	1137.048	1147.996	mV					2X
1151.124	1162.072	1173.021	mV				High-Floating	1X
1176.149	1187.097	1198.045	mV					2X

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$V_{SET3} = \frac{R2}{R1+R2} \times 3.2V$				VR Address	Zero Load Line	ANTI_OVS	AHTI_OVS Behavior	AI GAIN
Min	Typical	Max	Unit					
1201.173	1212.121	1223.069	mV	CORE : 01 AXG : 03	CORE : With LL AXG : With LL	Disable	High-Low-Floating	1X
1226.197	1237.146	1248.094	mV					2X
1251.222	1262.170	1273.118	mV				High-Floating	1X
1276.246	1287.195	1298.143	mV					2X
1301.271	1312.219	1323.167	mV			Enable	High-Low-Floating	1X
1326.295	1337.243	1348.192	mV					2X
1351.320	1362.268	1373.216	mV				High-Floating	1X
1376.344	1387.292	1398.240	mV					2X
1401.369	1412.317	1423.265	mV		CORE : With LL AXG : W/O LL	Disable	High-Low-Floating	1X
1426.393	1437.341	1448.289	mV					2X
1451.417	1462.366	1473.314	mV				High-Floating	1X
1476.442	1487.390	1498.338	mV					2X
1501.466	1512.414	1523.363	mV			Enable	High-Low-Floating	1X
1526.491	1537.439	1548.387	mV					2X
1551.515	1562.463	1573.412	mV				High-Floating	1X
1576.540	1587.488	1598.436	mV					2X

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Table 4. SET3 Pin Setting for Enable PSYS Function, Enable High Switching Frequency Ramp, DVID Slew Rate, Disable DVID compensation, Decrease GTU/SA Ramp Amplitude (Only Active in max phase =1 Application)

$\Delta V_{SET3} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$				EN PSYS	EN HIGH FREQ RAMP	DVID SR	Disable DIVD Compensation	Decrease GTU/SA Ramp (Only active as max phase number =1)
Min	Typical	Max	Unit					
0.000	10.948	21.896	mV	Disable	Disable	33.75mV/μs	Disable	Disable
25.024	35.973	46.921	mV					Enable
50.049	60.997	71.945	mV				Enable	Disable
75.073	86.022	96.970	mV					Enable
100.098	111.046	121.994	mV			11.25mV/μs	Disable	Disable
125.122	136.070	147.019	mV					Enable
150.147	161.095	172.043	mV				Enable	Disable
175.171	186.119	197.067	mV					Enable
200.196	211.144	222.092	mV		Enable	33.75mV/μs	Disable	Disable
225.220	236.168	247.116	mV					Enable
250.244	261.193	272.141	mV				Enable	Disable
275.269	286.217	297.165	mV					Enable
300.293	311.241	322.190	mV			11.25mV/μs	Disable	Disable
325.318	336.266	347.214	mV					Enable
350.342	361.290	372.239	mV				Enable	Disable
375.367	386.315	397.263	mV					Enable
400.391	411.339	422.287	mV					
425.415	436.364	447.312	mV					
450.440	461.388	472.336	mV					
475.464	486.413	497.361	mV					
500.489	511.437	522.385	mV					
525.513	536.461	547.410	mV					
550.538	561.486	572.434	mV					
575.562	586.510	597.458	mV					
600.587	611.535	622.483	mV					
625.611	636.559	647.507	mV					
650.635	661.584	672.532	mV					
675.660	686.608	697.556	mV					
700.684	711.632	722.581	mV					
725.709	736.657	747.605	mV					
750.733	761.681	772.630	mV					
775.758	786.706	797.654	mV					

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$\Delta V_{SET3} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$				EN PSYS	EN HIGH FREQ RAMP	DVID SR	Disable DIVD Compensation	Decrease GTU/SA Ramp (Only active as max phase number = 1)
Min	Typical	Max	Unit					
800.782	811.730	822.678	mV	Enable	Disable	33.75mV/μs	Disable	Disable
825.806	836.755	847.703	mV					Enable
850.831	861.779	872.727	mV				Enable	Disable
875.855	886.804	897.752	mV					Enable
900.880	911.828	922.776	mV			11.25mV/μs	Disable	Disable
925.904	936.852	947.801	mV					Enable
950.929	961.877	972.825	mV				Enable	Disable
975.953	986.901	997.849	mV					Enable
1000.978	1011.926	1022.874	mV		Enable	33.75mV/μs	Disable	Disable
1026.002	1036.950	1047.898	mV					Enable
1051.026	1061.975	1072.923	mV				Enable	Disable
1076.051	1086.999	1097.947	mV					Enable
1101.075	1112.023	1122.972	mV			11.25mV/μs	Disable	Disable
1126.100	1137.048	1147.996	mV					Enable
1151.124	1162.072	1173.021	mV				Enable	Disable
1176.149	1187.097	1198.045	mV					Enable
1201.173	1212.121	1223.069	mV			33.75mV/μs	Disable	Disable
1226.197	1237.146	1248.094	mV					Enable
1251.222	1262.170	1273.118	mV				Enable	Disable
1276.246	1287.195	1298.143	mV					Enable
1301.271	1312.219	1323.167	mV			11.25mV/μs	Disable	Disable
1326.295	1337.243	1348.192	mV					Enable
1351.320	1362.268	1373.216	mV				Enable	Disable
1376.344	1387.292	1398.240	mV					Enable

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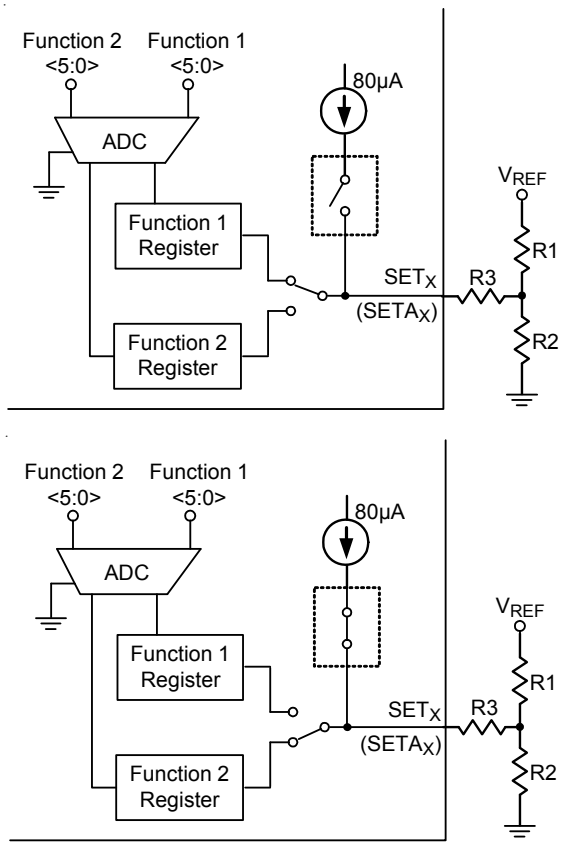

Figure 5. Multi-Function Pin Setting Mechanism with a R3 Resistor to Fine Tune the Set Voltage of Function2

VR Rail Addressing Setting

The VR address of RT3606BC can be flipped by setting the voltage on SET3 with an external voltage divider as shown in Figure 6. The voltage at VREF pin will be pulled up to 3.2V after power ready (POR) and the voltage at VREF pin will fix to 0.6V within 500μs after power ready (POR). Besides, when AXG rail address is set to 2, the boot voltage of AXG rail is 1.05V.

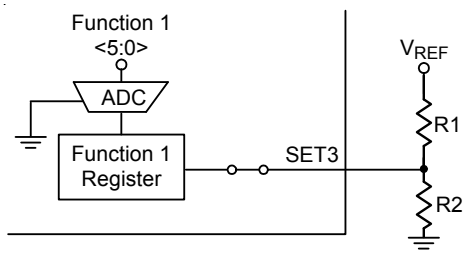

Figure 6. VR Rail Addressing and Zero Load-Line Setting for SET3

Anti-Overshoot and Anti-Overshoot Behavior

The anti-overshoot function can be enabled or disabled by setting the voltage on SET3 with an external voltage divider. During the anti-overshoot function is triggered, the high side and low side MOS will both turn off. Therefore, the output voltage adds the forward voltage of the MOS parasitic body diode will crosses on the inductor to speed up the discharge speed and eases the overshoot magnitude. However, if the MOS driver has tri-state delay time, the performance of the anti-overshoot function will be degenerated. To prevent this phenomenon, RT3606BC provides two kinds of anti-overshoot low side MOS behavior. With the driver has tri-state delay time, the behavior of anti-overshoot can choose as high-low-floating, and with the driver without tri-state delay time, the behavior of anti-overshoot can choose as high-floating.

High Switching Frequency Ramp

The switching frequency of RT3606BC can support from 300kHz to 1.1MHz, however, with higher switching frequency, the ramp is needed to increase simultaneously to improve the system stability and smooth the mode transient performance. As switching is higher than 550kHz, the high switching frequency ramp is suggested to be enabled. The high switching frequency ramp can be enabled or disabled by the internal current source 80μA and the parallel of the high low side resistor on SET3 pin.

Decrease GTU/SA Ramp Amplitude (Only Active in max phase = 1 Application)

If RT3606BC apply in GTU or SA application and the maximum phase number is 1. The ramp amplitude will automatically increase to improve the stability. This function can be disabled to improve the transient performance by the internal current source 80μA and the parallel of the high low side resistor on SET3 pin.

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Precise Reference Current Generation, IBIAS

Analog circuits need very precise reference voltage/current to drive/set these analog devices. The RT3606BC provides a 2V voltage source at the IBIAS pin, and a 100kΩ resistor is required to be connected between the IBIAS pin and analog ground to generate a very precise reference current. Through this connection, the RT3606BC will generate a 20μA current from the IBIAS pin to analog ground, and this 20μA current will be mirrored inside the RT3606BC for internal use. The IBIAS pin can only be connected with a 100kΩ resistor to GND for internal analog circuit use. The resistance error of this resistor is recommended to be 1% or smaller. Figure 7 shows the IBIAS setting circuit.

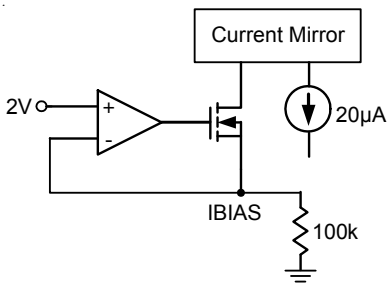

Figure 7. IBIAS Setting Circuit

TSEN, TSENA and $\overline{\text{VR_HOT}}$

The $\overline{\text{VR_HOT}}$ signal is an open-drain signal which is used for VR thermal protection. When the sensed voltage in TSEN(A) pin is less than 1.092, the $\overline{\text{VR_HOT}}$ signal will be pulled-low to notify CPU that the thermal protection needs to work. According to Intel VR definition, $\overline{\text{VR_HOT}}$ signal needs acting if VR power chain temperature exceeds 100°C. Placing an NTC thermistor at the hottest area in the VR power chain and its connection is shown in Figure 8, to design the voltage divider elements (R1, R2 and NTC) so that VTSEN(A) = 1.092V at 100°C. The resistance error of TSEN network is recommended to be 1% or smaller.

$$V_{TSEN(A)} = 80\mu A \times (R1//(R2 + R_{NTC\ (100°C)}))$$

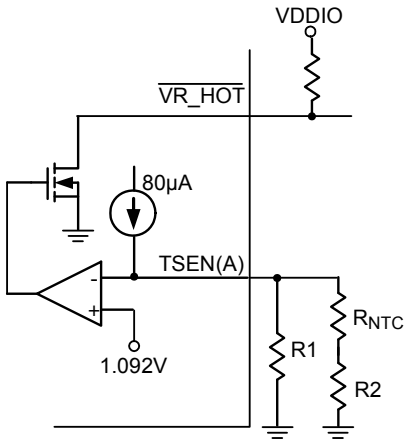

Figure 8. $\overline{\text{VR_HOT}}$ Circuit

Power Ready (POR) Detection

During start-up, the RT3606BC detects the voltage at the voltage input pins: V_{CC}, EN and DVD. When V_{CC} > 4.34V and V_{DVD} > 2V, the RT3606BC recognizes the power state of system to be ready (POR = high) and waits for enable command at the EN pin. After POR = high and V_{EN} > 0.7V, the RT3606BC will enter start-up sequence. If the voltage at any voltage pin drops below low threshold (POR = low), the RT3606BC will enter power down sequence and all the functions will be disabled. Normally, connecting system voltage V_{TT} (1.05V) to the EN pin and power stage VIN (12V, through a voltage divider) to the DVD pin is recommended. 2ms (max) after the chip has been enabled, the SVID circuitry will be ready. All the protection latches (OVP, OCP, UVP) will be cleared only by VCC. The condition of VEN = low will not clear these latches. Figure 9 and Figure 10 show the POR detection and the timing chart for POR process, respectively.

Under Voltage Lockout (UVLO)

During normal operation, if the voltage at the VCC drops below POR threshold 3.95V (min) or DVD voltage drops below POR threshold 1.3V, the VR triggers UVLO. The UVLO protection forces all high-side MOSFETs and low-side MOSFETs off by shutting down internal PWM logic drivers.

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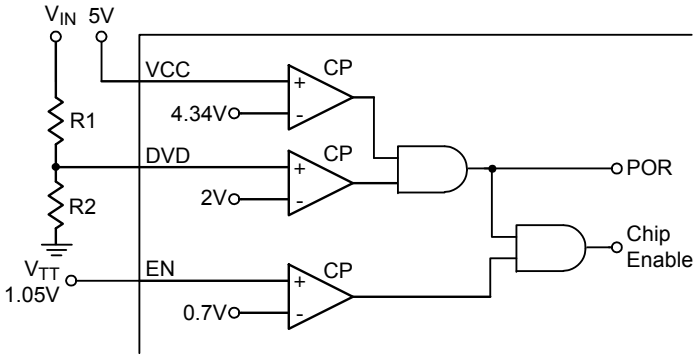

Figure 9. POR Detection

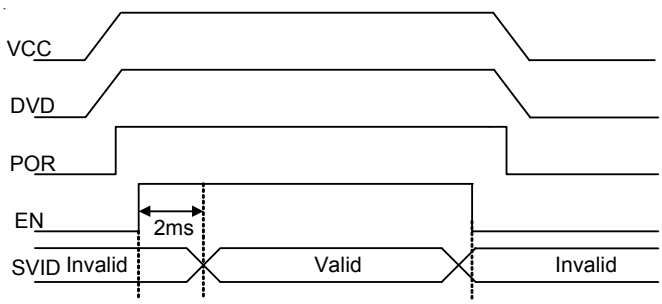

Figure 10. Timing Chart for POR Process

CORE VR

Phase Disable (Before POR)

The number of active phases is determined by the internal circuitry that monitors the ISENxN voltages during startup. Normally, the VR operates as a 3-phase PWM controller. Pulling ISEN3N to VCC programs a 2-phase operation, and pulling ISEN2N and ISEN3N to VCC programs a 1-phase operation. Before POR, VR detects whether the voltages of ISEN2N and ISEN3N are higher than "VCC–1V" respectively to decide how many phases should be active. Phase selection is only active during POR. When POR = high, the number of active phases is determined and latched. The unused ISENxP pins are recommended to be connected to VCC and unused PWM pins can be left floating.

NO Load Offset (Platform)

The CORE VR features no load offset function which provides the possibility of wide range positive offset of output voltage. Users can disable offset function by simply connecting OFSM pin to GND. Figure 11 shows a voltage divider used to set no load offset voltage. No load offset voltage setting is :

$$V_{OFS_CORE} = 0.4 \times (V_{OFSM} - 1.7)$$

The range of V_{OFS_CORE} is between –500mV and 590mV and the resolution is 10mV.

For example, a 100mV no load offset requirement, V_{OFSM} needs to be set as 1.95V.

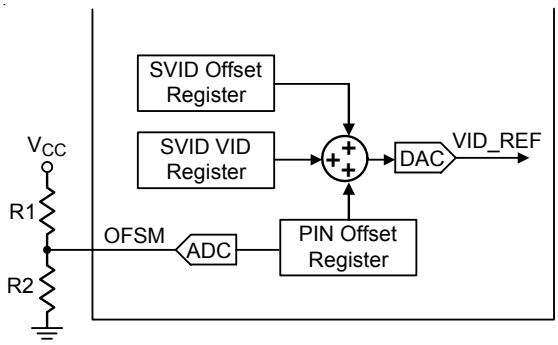

Figure 11. No Load Offset Circuit

Switching Frequency Setting

RT3606BC is one kind of constant on-time control. The patented CCRCOT (Constant Current Ripple COT) technology can generate an adaptive on-time, the on-time will vary with the input voltage and VID code to obtain a constant current ripple, so that the output voltage ripple can be controlled nearly like a constant as different input and output voltages change.

For CORE VR, connect a resistor R_{TON} between input terminal and TONSET pin to set the on-time width.

$$T_{ON} = \frac{R_{TON} \times 4.73p \times 1.2}{V_{IN} - V_{DAC}} \quad (V_{DAC} < 1.2)$$

$$T_{ON} = \frac{R_{TON} \times 4.73p \times V_{DAC}}{V_{IN} - V_{DAC}} \quad (V_{DAC} \geq 1.2)$$

For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$F_{SW(MAX)} = \frac{VID1 + \frac{IccTDC}{N} \cdot \left(DCR + \frac{R_{ON_LS,max}}{\eta_{LS}} - N \cdot R_{LL}\right)}{\left[V_{IN(MAX)} + \frac{IccTDC}{N} \cdot \left(\frac{R_{ON_LS,max}}{\eta_{LS}} - \frac{R_{ON_HS,max}}{\eta_{HS}}\right)\right] \cdot (T_{ON} - T_D + T_{ON,VAR}) + \frac{IccTDC}{N} \cdot \left(\frac{R_{ON_LS,max}}{\eta_{LS}}\right) \cdot T_D}$$

Where $F_{sw(MAX)}$ is the maximum switching frequency, VID1 is the typical VID of application, $V_{IN(MAX)}$ is the maximum application input voltage, IccTDC is the thermal design current of application, N is the phase number. The $R_{ON_HS,max}$ is the maximum equivalent high-side $R_{DS(ON)}$,

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and n_{HS} is the number of high-side MOSFETs; $R_{ON_LS,max}$ is the maximum equivalent low-side $R_{DS(ON)}$, and n_{LS} is the number of low-side MOSFETs. T_D is the summation of the high-side MOSFET delay time and the rising time, $T_{ON,VAR}$ is the T_{ON} variation value. DCR is the inductor DCR, and R_{LL} is the loadline setting. In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the R_{TON} for RT3606BC.

When load increases, on-time keeps constant. The off-time width will be reduced so that loading can load more power from input terminal to regulate output voltage. Hence the loading current usually increases in case the switching frequency also increases. Higher switching frequency operation can reduce power components' size and PCB space, trading off the whole efficiency since switching related switching related loss increases, vice versa.

Per Phase Current Sense

In the RT3606BC, the current signal is used for load-line setting and over-current protection (OCP). The inductor current sense method adopts the lossless current sensing for allowing high efficiency as illustrated in Figure 12. When inductance and DCR time constant is equal to R_XC_X filter network time constant, a voltage I_{Lx} x DCR will drop on C_x to generate inductor current signal. According to the Figure 12, the ISENxN is as follows :

$$ISENxN = \frac{I_{LX} \times DCR}{R_{CSx}}$$

Where Lx/DCR = R_XC_X is held. The method can get high efficiency performance, but DCR value will be drifted by temperature, a NTC resistor should add in the resistor network in the IMON pin to achieve DCR thermal compensation.

In RT3606BC design, the resistance of R_{CSx} is restricted to 680Ω; moreover, the error of R_{CSx} is recommended to be 1% or smaller.

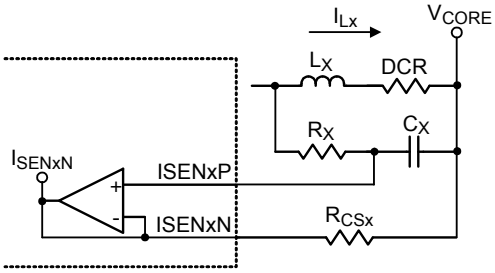

Figure 12. Lossless Current Sense Method

Total Current Sense

Total current sense method is a patented topology, unlike conventional current sense method need a NTC resistor in per phase current loop for thermal compensation. RT3606BC adopts the total current sense method requiring only one NTC resistor for thermal compensation, and NTC resistor cost can be saved by using this method. Figure 13 shows the total current sense method which connects the resistor network between IMON pin and VREF pin to set a part of current loop gain for load line (droop) setting and set accurate over current protection.

$$V_{IMON} - V_{REF} = \frac{DCR}{R_{CS}} \times R_{EQ} \times (I_{L1} + I_{L2} + I_{L3})$$

R_{EQ} includes a NTC resistor to compensate DCR thermal drifting for high accuracy load-line (droop).

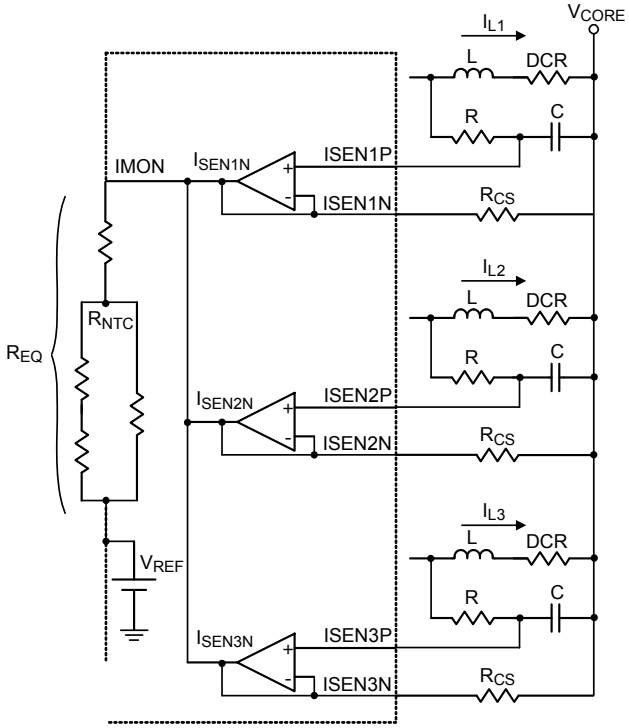

Figure 13. Total Current Sense Method

Load-Line Setting (Droop)

The G-NAVP™ topology can set load-line (droop) via the current loop and the voltage loop, the load-line is a slope between load current I_{CC} and output voltage V_{CORE} as shown Figure 14. Figure 15 shows the voltage control and current loop. By using the both loops, the load-line (droop) can be set easily. The load-line set equation is :

$$R_{LL} = \frac{A_I}{A_V} = \frac{\frac{1}{3} \times \frac{DCR}{R_{CS}} \times R_{EQ}}{\frac{R2}{R1}} (m\Omega)$$

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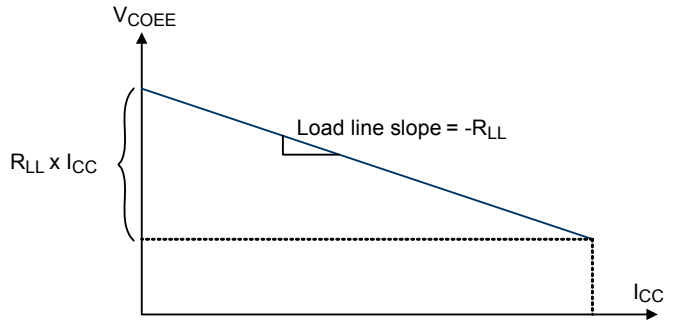

Figure 14. Load-Line (Droop)

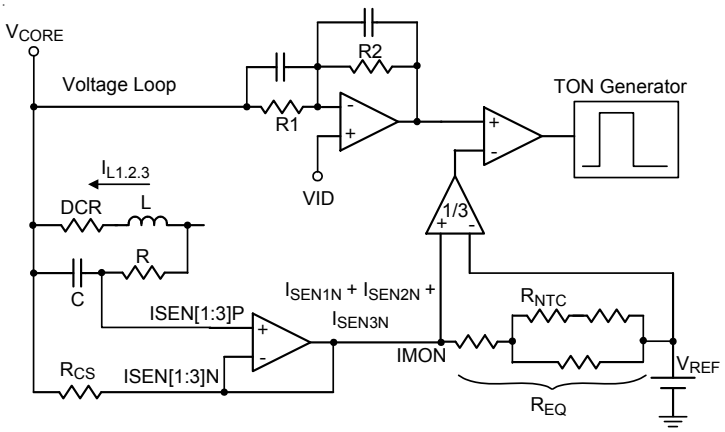

Figure 15. Voltage Loop and Current Loop

Compensator Design

The compensator of RT3606BC doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in G-NAVP™ topology to achieve constant output impedance design for Intel IMVP8 ACLL specification. The one pole one zero compensator is shown as Figure 16, the transfer function of compensator should be design as following transfer function to achieve constant output impedance, i.e. Zo(s) = load-line slope in the entire frequency range

$$G_{CON}(S) \approx \frac{A_I}{R_{LL}} \frac{1+\frac{s}{\omega \times f_{SW}}}{1+\frac{s}{\omega_{ESR}}}$$

Where A_I is current loop gain, R_{LL} is load line, f_{SW} is switching frequency and ω_{ESR} is a pole that should be located at 1 / (C_{OUT} x ESR). Then the C1 and C2 should be designed as

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}} \qquad C2 = \frac{C_{OUT} \times ESR}{R2}$$

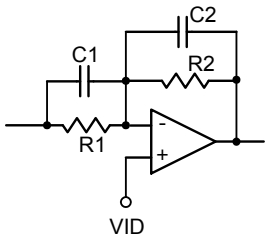

Figure 16. Type I Compensator

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{CC_SENSE} and V_{SS_SENSE}. Connect RGND to V_{SS_SENSE} and connect FB to V_{CC_SENSE} with a resistor to build the negative input path of the error amplifier as shown in Figure 17. The V_{DAC} and the precision voltage reference are referred to RGND for accurate remote sensing.

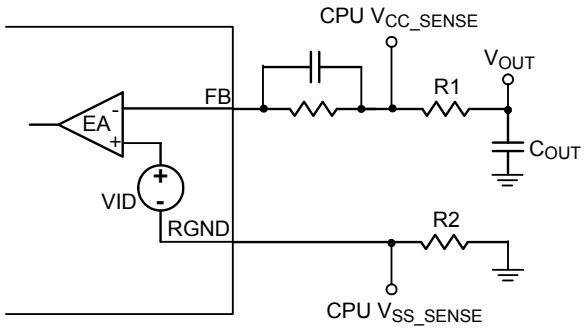

Figure 17. Remote Sensing Circuit

Maximum Processor Current Setting, ICCMAX

The maximum processor current ICCMAX can be set by the SET1 pin. ICCMAX register is set by an external voltage divider with the multi-function mechanism. The table 5 shows the ICCMAX setting on the SET1 pin. For example, ICCMAX = 80A, the V_{ICCMAX} needs to set as 0.503 typical. Additionally, $V_{IMON} - V_{REF}$ needs to be set as 1.6V at ICCMAX when the maximum phase > 1. As in 1-phase application, the $V_{IMON} - V_{REF}$ needs to be set as 0.4V at ICCMAX. The ICCMAX alert signal will be pulled to low level if $V_{IMON} - V_{REF}$ = 1.6V (for maximum phase > 1) or $V_{IMON} - V_{REF}$ = 0.4 (for 1-phase application).

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Table 5. SET1 Pin Setting in ICCMAX

$V_{SET1} = \frac{R2}{R1+R2} \times 3.2V$				ICCMAX	Unit
Min	Typical	Max	Unit		
0.000	3.128	6.256	mV	0	A
12.512	15.640	18.768	mV	2	A
25.024	28.152	31.281	mV	4	A
37.537	40.665	43.793	mV	6	A
50.049	53.177	56.305	mV	8	A
62.561	65.689	68.817	mV	10	A
75.073	78.201	81.329	mV	12	A
87.586	90.714	93.842	mV	14	A
100.098	103.226	106.354	mV	16	A
112.610	115.738	118.866	mV	18	A
125.122	128.250	131.378	mV	20	A
137.634	140.762	143.891	mV	22	A
150.147	153.275	156.403	mV	24	A
162.659	165.787	168.915	mV	26	A
175.171	178.299	181.427	mV	28	A
187.683	190.811	193.939	mV	30	A
200.196	203.324	206.452	mV	32	A
212.708	215.836	218.964	mV	34	A
225.220	228.348	231.476	mV	36	A
237.732	240.860	243.988	mV	38	A
250.244	253.372	256.500	mV	40	A
262.757	265.885	269.013	mV	42	A
275.269	278.397	281.525	mV	44	A
287.781	290.909	294.037	mV	46	A
300.293	303.421	306.549	mV	48	A
312.805	315.934	319.062	mV	50	A
325.318	328.446	331.574	mV	52	A
337.830	340.958	344.086	mV	54	A
350.342	353.470	356.598	mV	56	A
362.854	365.982	369.110	mV	58	A
375.367	378.495	381.623	mV	60	A
387.879	391.007	394.135	mV	62	A
400.391	403.519	406.647	mV	64	A
412.903	416.031	419.159	mV	66	A
425.415	428.543	431.672	mV	68	A
437.928	441.056	444.184	mV	70	A
450.440	453.568	456.696	mV	72	A
462.952	466.080	469.208	mV	74	A

$V_{SET1} = \frac{R2}{R1+R2} \times 3.2V$				ICCMAX	Unit
Min	Typical	Max	Unit		
475.464	478.592	481.720	mV	76	A
487.977	491.105	494.233	mV	78	A
500.489	503.617	506.745	mV	80	A
513.001	516.129	519.257	mV	82	A
525.513	528.641	531.769	mV	84	A
538.025	541.153	544.282	mV	86	A
550.538	553.666	556.794	mV	88	A
563.050	566.178	569.306	mV	90	A
575.562	578.690	581.818	mV	92	A
588.074	591.202	594.330	mV	94	A
600.587	603.715	606.843	mV	96	A
613.099	616.227	619.355	mV	98	A
625.611	628.739	631.867	mV	100	A
638.123	641.251	644.379	mV	102	A
650.635	653.763	656.891	mV	104	A
663.148	666.276	669.404	mV	106	A
675.660	678.788	681.916	mV	108	A
688.172	691.300	694.428	mV	110	A
700.684	703.812	706.940	mV	112	A
713.196	716.325	719.453	mV	114	A
725.709	728.837	731.965	mV	116	A
738.221	741.349	744.477	mV	118	A
750.733	753.861	756.989	mV	120	A
763.245	766.373	769.501	mV	122	A
775.758	778.886	782.014	mV	124	A
788.270	791.398	794.526	mV	126	A
800.782	803.910	807.038	mV	128	A
813.294	816.422	819.550	mV	130	A
825.806	828.935	832.063	mV	132	A
838.319	841.447	844.575	mV	134	A
850.831	853.959	857.087	mV	136	A
863.343	866.471	869.599	mV	138	A
875.855	878.983	882.111	mV	140	A
888.368	891.496	894.624	mV	142	A
900.880	904.008	907.136	mV	144	A
913.392	916.520	919.648	mV	146	A
925.904	929.032	932.160	mV	148	A
938.416	941.544	944.673	mV	150	A

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$V_{SET1} = \frac{R2}{R1+R2} \times 3.2V$				ICCMAX	Unit
Min	Typical	Max	Unit		
950.929	954.057	957.185	mV	152	A
963.441	966.569	969.697	mV	154	A
975.953	979.081	982.209	mV	156	A
988.465	991.593	994.721	mV	158	A
1000.978	1004.106	1007.234	mV	160	A
1013.490	1016.618	1019.746	mV	162	A
1026.002	1029.130	1032.258	mV	164	A
1038.514	1041.642	1044.770	mV	166	A
1051.026	1054.154	1057.283	mV	168	A
1063.539	1066.667	1069.795	mV	170	A
1076.051	1079.179	1082.307	mV	172	A
1088.563	1091.691	1094.819	mV	174	A
1101.075	1104.203	1107.331	mV	176	A
1113.587	1116.716	1119.844	mV	178	A
1126.100	1129.228	1132.356	mV	180	A
1138.612	1141.740	1144.868	mV	182	A
1151.124	1154.252	1157.380	mV	184	A
1163.636	1166.764	1169.892	mV	186	A
1176.149	1179.277	1182.405	mV	188	A
1188.661	1191.789	1194.917	mV	190	A
1201.173	1204.301	1207.429	mV	192	A
1213.685	1216.813	1219.941	mV	194	A
1226.197	1229.326	1232.454	mV	196	A
1238.710	1241.838	1244.966	mV	198	A
1251.222	1254.350	1257.478	mV	200	A
1263.734	1266.862	1269.990	mV	202	A
1276.246	1279.374	1282.502	mV	204	A
1288.759	1291.887	1295.015	mV	206	A
1301.271	1304.399	1307.527	mV	208	A
1313.783	1316.911	1320.039	mV	210	A
1326.295	1329.423	1332.551	mV	212	A
1338.807	1341.935	1345.064	mV	214	A
1351.320	1354.448	1357.576	mV	216	A
1363.832	1366.960	1370.088	mV	218	A
1376.344	1379.472	1382.600	mV	220	A
1388.856	1391.984	1395.112	mV	222	A
1401.369	1404.497	1407.625	mV	224	A
1413.881	1417.009	1420.137	mV	226	A

$V_{SET1} = \frac{R2}{R1+R2} \times 3.2V$				ICCMAX	Unit
Min	Typical	Max	Unit		
1426.393	1429.521	1432.649	mV	228	A
1438.905	1442.033	1445.161	mV	230	A
1451.417	1454.545	1457.674	mV	232	A
1463.930	1467.058	1470.186	mV	234	A
1476.442	1479.570	1482.698	mV	236	A
1488.954	1492.082	1495.210	mV	238	A
1501.466	1504.594	1507.722	mV	240	A
1513.978	1517.107	1520.235	mV	242	A
1526.491	1529.619	1532.747	mV	244	A
1539.003	1542.131	1545.259	mV	246	A
1551.515	1554.643	1557.771	mV	248	A
1564.027	1567.155	1570.283	mV	250	A
1576.540	1579.668	1582.796	mV	252	A
1589.052	1592.180	1595.308	mV	254	A

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Dynamic VID (DVID) Compensation

When VID transition event occurs, a charger current will be generated in the loop to cause DVID performance. However, the DVID performance will be deteriorated by this induced charger current, this phenomenon is called droop effect. The droop effect is shown in Figure 18, when VID up transition occurs, the output capacitor will be charged by inductor current. Since current signal is sensed in inductor, an induced charge current will appear in control loop. The induced charge current will produce a voltage drop in R1 to cause output voltage to have a droop effect. Due to this, VID transition performance will be deteriorated.

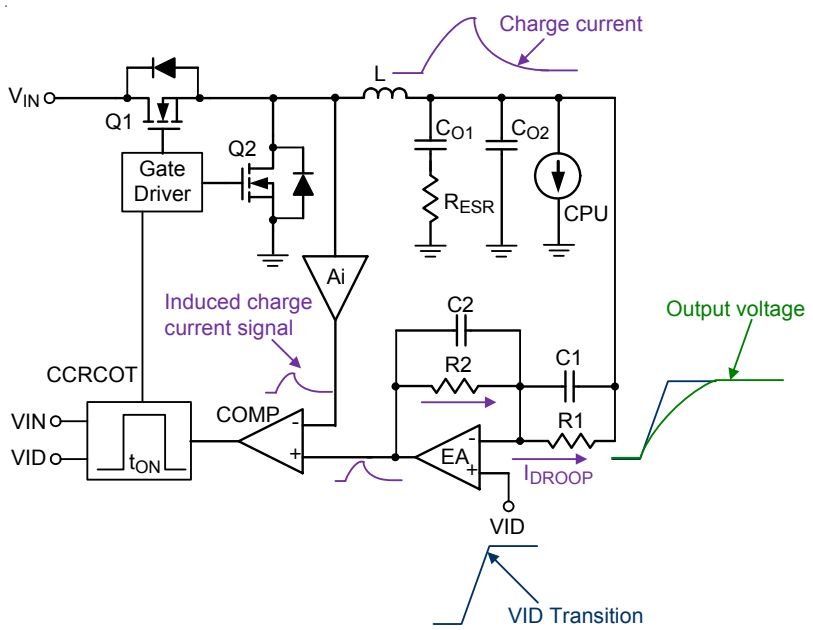

Figure 18. Droop Effect in VID transition

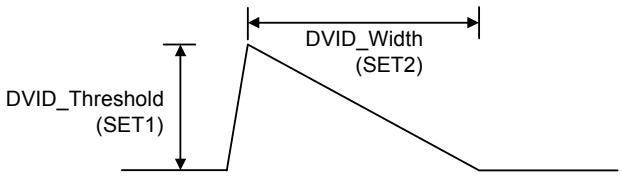

Figure 19. Definition of Virtual Charge Current Signal

RT3606BC provide a DVID compensation function. A virtual charge current signal can be established by the SET1/SET2 pins to cancel the real induced charge current signal and the virtual charge current signal is defined in Figure 19. Figure 20 shows the operation of canceling droop effect. A virtual charge current signal is established first and then VID signal plus virtual charge current signal to be generated on the FB pin. Hence, an induced charge current signal flows to R1 and is cancelled to reduce droop effect.

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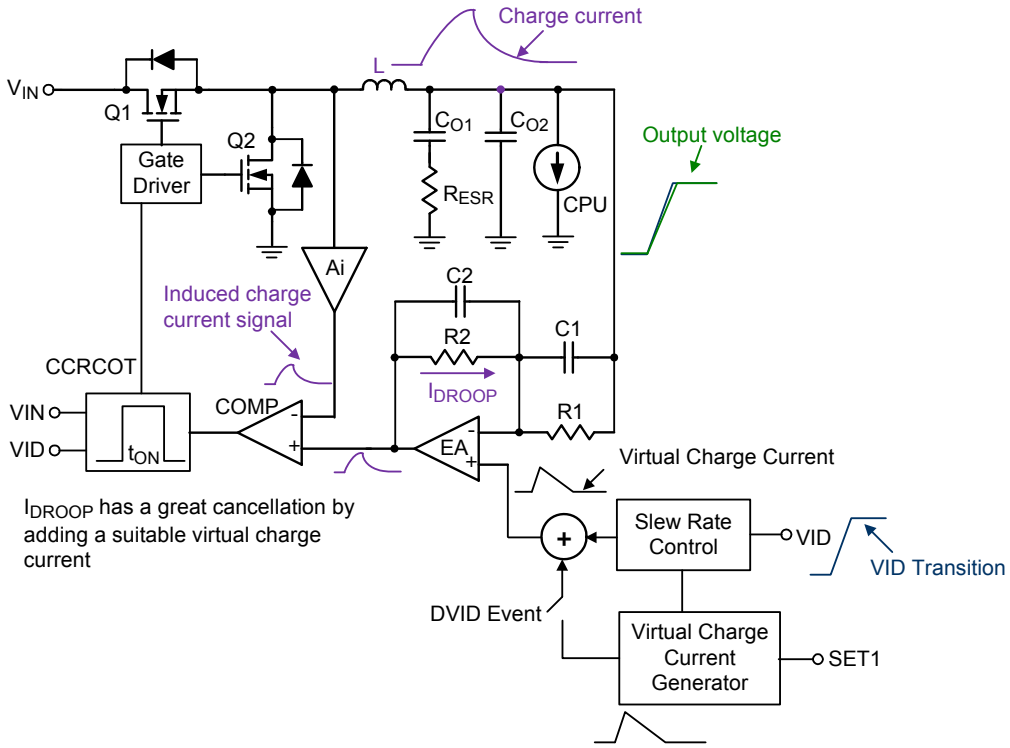

Figure 20. DVID Compensation

Table 6 show the DVID_Threshold on the SET1 pin with internal 80μA current source and Table 7 describes DVID_Width settings in SET2 pin with external voltage divider. For example, 39.67mV DVID_Threshold (SR = 11.25mV/μs) / 119mV DVID_threshold (SR = 33.75mV/μs) and 36μs DVID_Width are designed (OCP sets as 110% ICCMAX, RSET sets as 133% low frequency ramp / 200% high frequency ramp). According to the Table 6 and Table 7, the DVID_Threshold set voltage should be between 0.4254V to 0.4473V and the DVID_Width set voltage should be between 1.051V to 1.073V. Please note that a high accuracy resistor is needed for this setting, < 1% error tolerance is recommended.

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Table 6. SET1 Pin Setting for DVID_Threshold

$\Delta V_{SET1} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$				DVID_Threshold		OCP = %ICCMAX
Min	**Typical**	**Max**	**Unit**	**DVID SR = 11.25mV/μs**	**DVID SR = 33.75mV/μs**	
0.000	10.948	21.896	mV	18.33mV	55mV	NA
25.024	35.973	46.921	mV			110%
50.049	60.997	71.945	mV			120%
75.073	86.022	96.970	mV			130%
100.098	111.046	121.994	mV			140%
125.122	136.070	147.019	mV			150%
150.147	161.095	172.043	mV			160%
175.171	186.119	197.067	mV			NA
200.196	211.144	222.092	mV	29mV	87mV	NA
225.220	236.168	247.116	mV			110%
250.244	261.193	272.141	mV			120%
275.269	286.217	297.165	mV			130%
300.293	311.241	322.190	mV			140%
325.318	336.266	347.214	mV			150%
350.342	361.290	372.239	mV			160%
375.367	386.315	397.263	mV			NA
400.391	411.339	422.287	mV	39.67mV	119mV	NA
425.415	436.364	447.312	mV			110%
450.440	461.388	472.336	mV			120%
475.464	486.413	497.361	mV			130%
500.489	511.437	522.385	mV			140%
525.513	536.461	547.410	mV			150%
550.538	561.486	572.434	mV			160%
575.562	586.510	597.458	mV			NA
600.587	611.535	622.483	mV	50.33mV	151mV	NA
625.611	636.559	647.507	mV			110%
650.635	661.584	672.532	mV			120%
675.660	686.608	697.556	mV			130%
700.684	711.632	722.581	mV			140%
725.709	736.657	747.605	mV			150%
750.733	761.681	772.630	mV			160%
775.758	786.706	797.654	mV			NA

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$\Delta V_{SET1} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$				DVID_Threshold		OCP = %ICCMAX
Min	Typical	Max	Unit	DVID SR = 11.25mV/μs	DVID SR = 33.75mV/μs	
800.782	811.730	822.678	mV	61mV	183mV	NA
825.806	836.755	847.703	mV			110%
850.831	861.779	872.727	mV			120%
875.855	886.804	897.752	mV			130%
900.880	911.828	922.776	mV			140%
925.904	936.852	947.801	mV			150%
950.929	961.877	972.825	mV			160%
975.953	986.901	997.849	mV			NA
1000.978	1011.926	1022.874	mV	71.67mV	215mV	NA
1026.002	1036.950	1047.898	mV			110%
1051.026	1061.975	1072.923	mV			120%
1076.051	1086.999	1097.947	mV			130%
1101.075	1112.023	1122.972	mV			140%
1126.100	1137.048	1147.996	mV			150%
1151.124	1162.072	1173.021	mV			160%
1176.149	1187.097	1198.045	mV			NA
1201.173	1212.121	1223.069	mV	82.33mV	247mV	NA
1226.197	1237.146	1248.094	mV			110%
1251.222	1262.170	1273.118	mV			120%
1276.246	1287.195	1298.143	mV			130%
1301.271	1312.219	1323.167	mV			140%
1326.295	1337.243	1348.192	mV			150%
1351.320	1362.268	1373.216	mV			160%
1376.344	1387.292	1398.240	mV			NA
1401.369	1412.317	1423.265	mV	93mV	279mV	NA
1426.393	1437.341	1448.289	mV			110%
1451.417	1462.366	1473.314	mV			120%
1476.442	1487.390	1498.338	mV			130%
1501.466	1512.414	1523.363	mV			140%
1526.491	1537.439	1548.387	mV			150%
1551.515	1562.463	1573.412	mV			160%
1576.540	1587.488	1598.436	mV			NA

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Table 7. SET2 Pin Setting for DVID_Width

$V_{SET2} = 3.2V \times \frac{R2}{R1+R2}$				DVID_Width	RSET %410k RTON	
Min	Typical	Max	Unit		Low F_{SW} Ramp	High F_{SW} Ramp
0.000	10.948	21.896	mV	6μs	100%	133%
25.024	35.973	46.921	mV		117%	167%
50.049	60.997	71.945	mV		133%	200%
75.073	86.022	96.970	mV		150%	233%
100.098	111.046	121.994	mV		167%	267%
125.122	136.070	147.019	mV		183%	300%
150.147	161.095	172.043	mV		200%	333%
175.171	186.119	197.067	mV		217%	367%
200.196	211.144	222.092	mV	12μs	100%	133%
225.220	236.168	247.116	mV		117%	167%
250.244	261.193	272.141	mV		133%	200%
275.269	286.217	297.165	mV		150%	233%
300.293	311.241	322.190	mV		167%	267%
325.318	336.266	347.214	mV		183%	300%
350.342	361.290	372.239	mV		200%	333%
375.367	386.315	397.263	mV		217%	367%
400.391	411.339	422.287	mV	18μs	100%	133%
425.415	436.364	447.312	mV		117%	167%
450.440	461.388	472.336	mV		133%	200%
475.464	486.413	497.361	mV		150%	233%
500.489	511.437	522.385	mV		167%	267%
525.513	536.461	547.410	mV		183%	300%
550.538	561.486	572.434	mV		200%	333%
575.562	586.510	597.458	mV		217%	367%
600.587	611.535	622.483	mV	24μs	100%	133%
625.611	636.559	647.507	mV		117%	167%
650.635	661.584	672.532	mV		133%	200%
675.660	686.608	697.556	mV		150%	233%
700.684	711.632	722.581	mV		167%	267%
725.709	736.657	747.605	mV		183%	300%
750.733	761.681	772.630	mV		200%	333%
775.758	786.706	797.654	mV		217%	367%
800.782	811.730	822.678	mV	30μs	100%	133%
825.806	836.755	847.703	mV		117%	167%
850.831	861.779	872.727	mV		133%	200%
875.855	886.804	897.752	mV		150%	233%
900.880	911.828	922.776	mV		167%	267%
925.904	936.852	947.801	mV		183%	300%
950.929	961.877	972.825	mV		200%	333%
975.953	986.901	997.849	mV		217%	367%

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$V_{SET2} = 3.2V \times \frac{R2}{R1+R2}$				DVID_Width	RSET %130k RTON	
Min	Typical	Max	Unit		Low F_{SW} Ramp	High F_{SW} Ramp
1000.978	1011.926	1022.874	mV	36μs	100%	133%
1026.002	1036.950	1047.898	mV		117%	167%
1051.026	1061.975	1072.923	mV		133%	200%
1076.051	1086.999	1097.947	mV		150%	233%
1101.075	1112.023	1122.972	mV		167%	267%
1126.100	1137.048	1147.996	mV		183%	300%
1151.124	1162.072	1173.021	mV		200%	333%
1176.149	1187.097	1198.045	mV		217%	367%
1201.173	1212.121	1223.069	mV	42μs	100%	133%
1226.197	1237.146	1248.094	mV		117%	167%
1251.222	1262.170	1273.118	mV		133%	200%
1276.246	1287.195	1298.143	mV		150%	233%
1301.271	1312.219	1323.167	mV		167%	267%
1326.295	1337.243	1348.192	mV		183%	300%
1351.320	1362.268	1373.216	mV		200%	333%
1376.344	1387.292	1398.240	mV		217%	367%
1401.369	1412.317	1423.265	mV	48μs	100%	133%
1426.393	1437.341	1448.289	mV		117%	167%
1451.417	1462.366	1473.314	mV		133%	200%
1476.442	1487.390	1498.338	mV		150%	233%
1501.466	1512.414	1523.363	mV		167%	267%
1526.491	1537.439	1548.387	mV		183%	300%
1551.515	1562.463	1573.412	mV		200%	333%
1576.540	1587.488	1598.436	mV		217%	367%

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Ramp Compensation

The G-NAVP™ topology is one type of ripple based control that has fast transient response and can lower BOM cost. However, ripple based control usually has poor noise immunity. RT3606BC provides the ramp compensation to increase noise immunity and reduce jitter at the switching node. Figure 21 shows the ramp compensation.

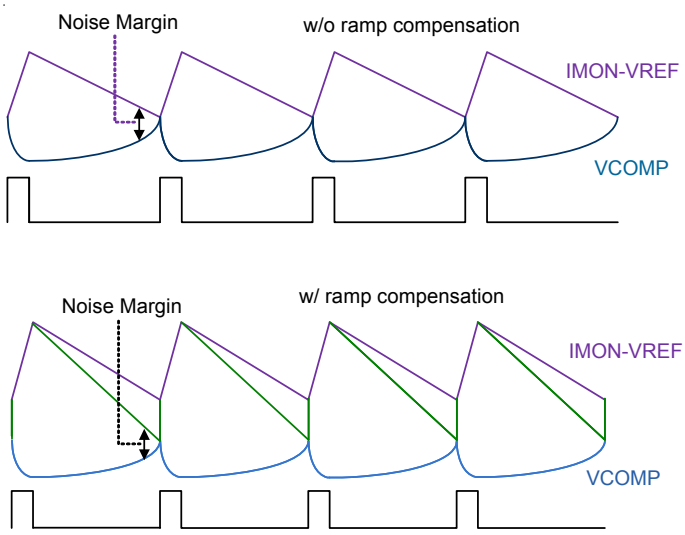

Figure 21. Ramp Compensation

For the RT3606BC, the ramp compensation also needs to be considered during mode transition from PS0/1 to PS2. For achieving smooth mode transition into PS2, a proper ramp compensation design is necessary. Since the ramp compensation needs to be proportional to the on-time, then RAMP is set as

$$133\% \times \frac{F_S}{400k}$$

Quick Response (QR) Mechanism

When the transient load step-up becomes quite large, it is difficult for loop response to meet the energy transfer. Hence, that output voltage generate undershoot to fail specification. The RT3606BC has Quick Response (QR) mechanism being able to improve this issue. It adopts a nonlinear control mechanism which can disable interleaving function and simultaneously turn on all UGATE one pulse at instantaneous step-up transient load to restrain the output voltage drooping, Figure 22 shows the QR behavior.

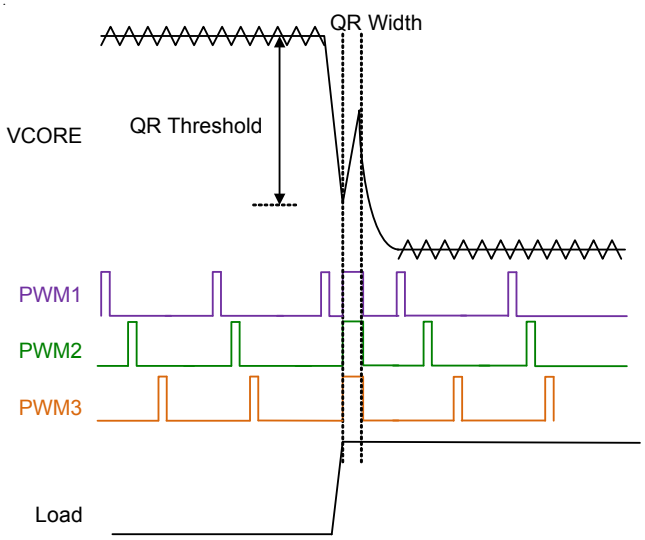

Figure 22. Quick Response Mechanism

The output voltage signal behavior needs to be detected so that QR mechanism can be trigged. The output voltage signal is via a remote sense line to connect at VSEN pin that is shown in Figure 23. The QR mechanism needs to set QR width and QR threshold. Both definitions are shown in Figure 22. A proper QR mechanism set can meet different applications. SET2 can set QR threshold and QR width by internal current source 80μA with multi-function pin setting mechanism.

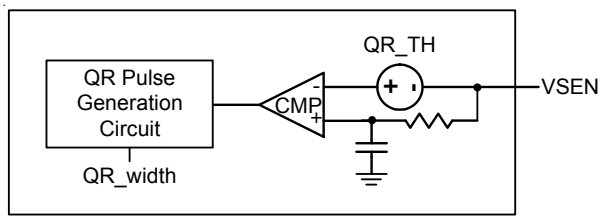

Figure 23. Simplified QR Trigger Schematic

For example, QR threshold 20mV/10mV at PS0/PS1 and 2.22 x TON QR width are set. According to the Table 8, the set voltage should be between 0.4505V and 0.4723V. Please note that a high accuracy resistor is needed for this setting accuracy, < 1% error tolerance is recommended. In the Table 8, there are some "NA" marks in QRWIDTH section. It means that users should not use it to avoid the possibility of shift digital code due to tolerance concern.

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Table 8. SET2 Pin Setting for QR Threshold and QR Width

$\Delta V_{SET2} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$				QR Threshold		QR Width (%TON)
Min	Typical	Max	Unit	PS0	PS1	
0.000	10.948	21.896	mV	15mV	10mV	NA
25.024	35.973	46.921	mV			Disable
50.049	60.997	71.945	mV			222%
75.073	86.022	96.970	mV			177.6%
100.098	111.046	121.994	mV			133.2%
125.122	136.070	147.019	mV			88%
150.147	161.095	172.043	mV			44%
175.171	186.119	197.067	mV			NA
200.196	211.144	222.092	mV	15mV	15mV	NA
225.220	236.168	247.116	mV			Disable
250.244	261.193	272.141	mV			222%
275.269	286.217	297.165	mV			177.6%
300.293	311.241	322.190	mV			133.2%
325.318	336.266	347.214	mV			88%
350.342	361.290	372.239	mV			44%
375.367	386.315	397.263	mV			NA
400.391	411.339	422.287	mV	20mV	10mV	NA
425.415	436.364	447.312	mV			Disable
450.440	461.388	472.336	mV			222%
475.464	486.413	497.361	mV			177.6%
500.489	511.437	522.385	mV			133.2%
525.513	536.461	547.410	mV			88%
550.538	561.486	572.434	mV			44%
575.562	586.510	597.458	mV			NA
600.587	611.535	622.483	mV	20mV	15mV	NA
625.611	636.559	647.507	mV			Disable
650.635	661.584	672.532	mV			222%
675.660	686.608	697.556	mV			177.6%
700.684	711.632	722.581	mV			133.2%
725.709	736.657	747.605	mV			88%
750.733	761.681	772.630	mV			44%
775.758	786.706	797.654	mV			NA

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$\Delta V_{SET2} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$				QR Threshold		QR Width (%TON)
Min	Typical	Max	Unit	PS0	PS1	
800.782	811.730	822.678	mV	25mV	10mV	NA
825.806	836.755	847.703	mV			Disable
850.831	861.779	872.727	mV			222%
875.855	886.804	897.752	mV			177.6%
900.880	911.828	922.776	mV			133.2%
925.904	936.852	947.801	mV			88%
950.929	961.877	972.825	mV			44%
975.953	986.901	997.849	mV			NA
1000.978	1011.926	1022.874	mV	25mV	15mV	NA
1026.002	1036.950	1047.898	mV			Disable
1051.026	1061.975	1072.923	mV			222%
1076.051	1086.999	1097.947	mV			177.6%
1101.075	1112.023	1122.972	mV			133.2%
1126.100	1137.048	1147.996	mV			88%
1151.124	1162.072	1173.021	mV			44%
1176.149	1187.097	1198.045	mV			NA
1201.173	1212.121	1223.069	mV	30mV	10mV	NA
1226.197	1237.146	1248.094	mV			Disable
1251.222	1262.170	1273.118	mV			222%
1276.246	1287.195	1298.143	mV			177.6%
1301.271	1312.219	1323.167	mV			133.2%
1326.295	1337.243	1348.192	mV			88%
1351.320	1362.268	1373.216	mV			44%
1376.344	1387.292	1398.240	mV			NA
1401.369	1412.317	1423.265	mV	30mV	15mV	NA
1426.393	1437.341	1448.289	mV			Disable
1451.417	1462.366	1473.314	mV			222%
1476.442	1487.390	1498.338	mV			177.6%
1501.466	1512.414	1523.363	mV			133.2%
1526.491	1537.439	1548.387	mV			88%
1551.515	1562.463	1573.412	mV			44%
1576.540	1587.488	1598.436	mV			NA

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Current Monitor, IMON

RT3606BC includes a current monitor (IMON) function which can be used to detect over-current protection and the maximum processor current ICCMAX, and also sets a part of current gain in the load-line setting. It produces an analog voltage proportional to output current between the IMON and VREF pins.

The calculation for IMON-VREF voltage is shown as below :

$$V_{IMON} - V_{REF} = \frac{DCR}{R_{CS}} \times R_{EQ} \times (I_{L1} + I_{L2} + I_{L3})$$

Where $I_{L1} + I_{L2} + I_{L3}$ are output current and the definitions of DCR, R_{CS} and R_{EQ} can refer to Figure 13.

Over-Current Protection

The RT3606BC provides Over-Current Protection (OCP) which is set by the SET1 pin. The OCP threshold setting can refer to ICCMAX current in Table 5. For example, if ICCMAX is set as 120A, users can set voltage by using the external voltage divider on the SET1 pin as 0.754V typically. If 156A OCP (130% x ICCMAX) threshold and DVID_TH (SR = 11.25mV/μs) = 39.67mV / DVID_TH (SR = 33.75mV/μs) = 119mV will be set. According to Table 6, the set voltage should be between 0.4755V and 0.4974V. When output current is higher than the OCP threshold, OCP is latched with a 40μs delay to prevent false trigger. Besides, the OCP function is masked when dynamic VID transient occurs, and soft-start period. And the OCP function will re-active after 46μs of DVID or soft-start alert is asserted.

Output Over-Voltage Protection

An OVP condition is detected when the VSEN pin is 350mV more than VID as VID > 1V. If VID < 1V, the OVP is detected when the VSEN pin is 350mV more than 1V. When OVP is detected, the high-side gate voltage UGATEx is pulled low and the low-side gate voltage LGATEx is pulled high. OVP is latched with a 0.5μs delay to prevent false trigger. Besides, the OVP function will be masked during DVID and soft-start period. After 46μs of DVID or soft-start alert is asserted, the OVP function will re-active.

Negative Voltage Protection

Since the OVP latch continuously turns on all low side MOSFETs of the VR, the VR will suffer negative output voltage. When the VSEN detects a voltage below –0.07V after triggering OVP, the VR triggers NVP to turn off all low-side MOSFETs of the VR while the high-side MOSFETs remains off. After triggering NVP, if the output voltage rises above 0V, the OVP latch restarts to turn on all low-side MOSFETs. Therefore, the output voltage may bounce between 0V and –0.07V due to OVP latch and NVP triggering. The NVP function will be active only after OVP is triggered.

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Current Loop Design in Details

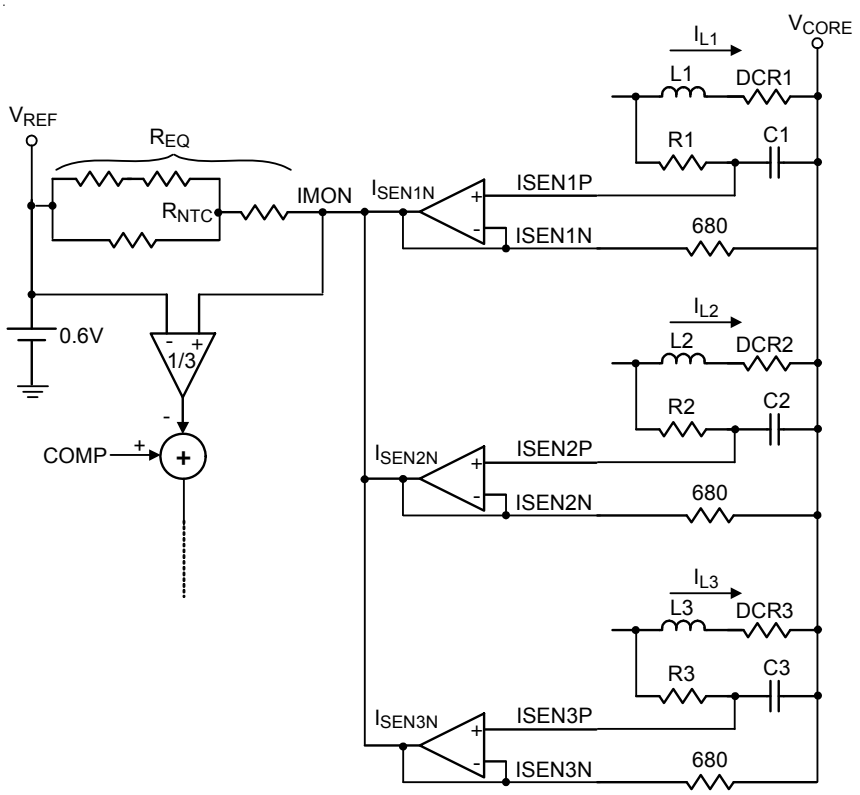

Figure 24. Current Loop Structure

Figure 24 shows the whole current loop structure. The current loop plays an important role in RT3606BC that can decide ACLL performance, DCLL accuracy and ICCMAX accuracy. For ACLL performance, the correct compensator design is assumed, if RC network time constant matches inductor time constant L_X / DCR_X, an expected load transient waveform can be designed. If R_XC_X network time constant is larger than inductor time constant L_X / DCR_X, V_{CORE} waveform has a sluggish droop during load transient. If R_XC_X network is smaller than inductor time constant L_X / DCR_X, a worst V_{CORE} waveform will sag to create an undershooting to fail the specification. Figure 25 shows the variety R_XC_X constant corresponding to the output waveforms.

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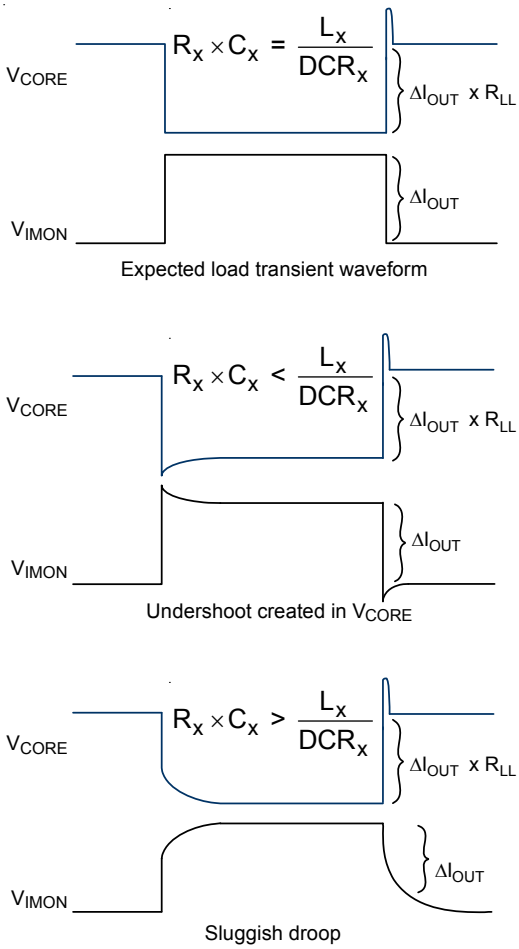

Figure 25. All Kinds of RxCx Constants

For DCLL performance and ICCMAX accuracy, since the copper wire of inductor has a positive temperature coefficient, when temperature goes high in the heavy load condition, DCR value goes large simultaneously. A resistor network with NTC thermistor compensation connecting between IMON and REF pins is necessary, to compensate the positive temperature coefficient of inductor DCR. The design flow is as follows :

Step1 : Given the three system temperature T_L, T_R and T_H, at which are compensated.

Step2 : Three equations can be listed as

$$\frac{DCR(T_L)}{680} \times \sum_{i=1}^{4} i_{Li} \times R_{EQ}(T_L) = 1.6$$

$$\frac{DCR(T_R)}{680} \times \sum_{i=1}^{4} i_{Li} \times R_{EQ}(T_R) = 1.6$$

$$\frac{DCR(T_H)}{680} \times \sum_{i=1}^{4} i_{Li} \times R_{EQ}(T_H) = 1.6$$

Where :

(1) The relationship between DCR and temperature is as follows :

$$DCR(T) = DCR(25°C) \times [1 + 0.00393(T - 25)]$$

(2) $R_{EQ}(T)$ is the equivalent resistor of the resistor network with a NTC thermistor

$$R_{EQ}(T) = R_{IMON1} + \{R_{IMON2} // [R_{IMON3} + R_{NTC}(T)]\}$$

And the relationship between NTC and temperature is as follows :

$$R_{NTC}(T) = R_{NTC}(25°C) \times e^{\beta(\frac{1}{T+273} - \frac{1}{298})}$$

β is in the NTC thermistor datasheet.

Step3 : Three equations and three unknowns, R_{IMON1}, R_{IMON2} and R_{IMON3} can be found out unique solution.

$$R_{IMON1} = K_{TR} - \frac{R_{IMON2} \times (R_{NTCTR} + R_{IMON3})}{R_{IMON2} + R_{NTCTR} + R_{IMON3}}$$

$$R_{IMON2} = \sqrt{[K_{R3}^2 + K_{R3}(R_{NTCTL} + R_{NTCTR}) + R_{NTCTL}R_{NTCTR}]\alpha_{TL}}$$

$$R_{IMON3} = -R_{IMON2} + K_{R3}$$

Where :

$$\alpha_{TH} = \frac{K_{TH} - K_{TR}}{R_{NTCTH} - R_{NTCTR}}$$

$$\alpha_{TL} = \frac{K_{TL} - K_{TR}}{R_{NTCTL} - R_{NTCTR}}$$

$$K_{R3} = \frac{(\alpha_{TH} / \alpha_{TL})R_{NTCTH} - R_{NTCTL}}{1 - (\alpha_{TH} / \alpha_{TL})}$$

$$K_{TL} = \frac{1.6}{G_{CS(TL)} \times I_{CC\text{-}MAX}}$$

$$K_{TR} = \frac{1.6}{G_{CS(TR)} \times I_{CC\text{-}MAX}}$$

$$K_{TH} = \frac{1.6}{G_{CS(TH)} \times I_{CC\text{-}MAX}}$$

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Design Step :

RT3606BC excel based design tool is available. Users can contact your Richtek representative to get the spreadsheet. Three main design procedures for RT3606BC design, first step is initial settings, second step is loop design and the last step is protection settings. The following design example is to explain the RT3606BC design procedure :

	V_{CORE} Specification
Input Voltage	12V
No. of Phases	3
ICCMAX	90A
ICC-DY	69A
ICC-TDC	68A
Load Line	2.1mΩ
Fast Slew Rate	10mV/μs
Max Switching Frequency	400kHz

In IMVP8 VRTB Guideline, the output filter requirements of VRTB specification for desktop platform are :

Output Inductor : 220nH/0.49mΩ

Output Bulk Capacitor : 560μF/2.5V/5mΩ (max) 4 to 5pcs

Output Ceramic Capacitor : 22μF/0805 (19pcs max in cavity)

(1) Initial Settings :

- IBIAS needs to connect a 100kΩ resistor to ground.
- A voltage divider for setting DVD can choose R_{DVD_U} = 510kΩ and R_{DVD_L} = 125kΩ to set V_{DVD} > 2V, RT3606BC enabled.

(2) Loop Design :

- On time setting : Using the specification, T_{ON} is

$$T_{ON} = \frac{R_{TON} \times 4.73p \times 1.2}{V_{IN} - V_{DAC}} (V_{DAC} < 1.2) = 246n$$

The on time setting resistor R_{TON} = 483kΩ

- Current sensor adopts lossless RC filter to sense current signal in DCR. For getting an expect load transient waveform, RxCx time constant needs to match Lx / DCRx per phase. Cx = 0.47μF is set, then

$$R_X = \frac{L_X}{0.47\mu F \times DCR_X} = 960\Omega$$

- IMON resistor network design : T_L = 25°C, T_R = 50°C and T_H = 100°C are decided, NTC thermistor = 100kΩ@25°C, β = 4485 and ICCMAX = 90A. According to the sub-section "Current Loop Design in Details", R_{IMON1} = 10.66kΩ, R_{IMON2} = 16.16kΩ and R_{IMON3} = 1 2.63kΩ can be decided. The R_{EQ} (25°C) = 24.91kΩ.
- Load-line design : 2.1mΩ droop is requirement, because R_{EQ} (25°C) has decided, the voltage loop Av gain is also can be decided by following equation

$$R_{LL} = \frac{A_I}{A_V} = \frac{\frac{1}{3} \times \frac{DCR}{R_{CS}} \times R_{EQ}}{\frac{R2}{R1}} (m\Omega)$$

Where DCR (25°C) = 0.49mΩ, R_{CS} = 680Ω and R_{EQ} (25°C) = 24.91kΩ. Hence the A_V = R2 / R1 = 2.85 can be obtained. R1 = 10kΩ usually decided, so R2 = 28.5kΩ.

- Typical compensator design can use the following equations to design the C1 and C2 values

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}} \approx 470pF$$

$$C2 = \frac{C_{OUT} \times ESR}{R2} \approx 98pF$$

For Intel platform, in order to induce the band width to enhance transient performance to meet Intel's criterion, the compensator of zero can be designed close to 1/10 of switching frequency.

- SET1 resistor network design : First the ICCMAX is design as 90A. Next, OCP threshold is designed as 1.5 x ICCMAX. Last, DVID compensation parameters need to be decided. The DVID_TH can be calculated as following equation

$$V_{DVID_TH} = LL \times C_{OUT} \times \frac{dVID}{dt}$$

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Where LL is load-line, C_{OUT} is total output capacitance and dVID/dt is DVID fast slew rate. Thus V_{DVID_TH} = 50.33mV is needed in this case. By using above information, the two equations can be listed by using multi-function pin setting mechanism

$$0.566 = \frac{R2}{R1+R2} \times 3.2$$

$$0.736 = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

R1 = 52kΩ, R2 = 11.2kΩ.

- SET2 resistor network design :

  RAMP = 133% x $\frac{400k}{400k}$ = 133%, 133% is set. And DVID_Width is chosen as 24μsec typical. Last, the QR mechanism parameters need to be designed first. Initial QR_TH is designed as 25mV and QR_Width is designed as 0.44 x T_{ON}. By using the information, the two equations can be listed by using multi-function pin setting mechanism

$$0.661 = \frac{R2}{R1+R2} \times 3.2$$

$$1.162 = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

R 1= 70.3kΩ, R2 = 18.2kΩ.

(1) Protection Settings :

- OVP protections : When VSEN pin voltage is 350mV more than VID, the OVP will be latched.
- TSEN and $\overline{VR_HOT}$ design : Using the following equation to calculate related resistances for $\overline{VR_HOT}$ setting.

$$V_{TSEN} = 80\mu A \times \left(R1 // \left(R2 + R_{NTC\ (100°C)}\right)\right)$$

- Choosing R1 is open and an NTC thermistor R_{NTC}(25°C) = 100kΩ which β = 4485. When temperature is 100°C, the R_{NTC} (100!) = 4.85kΩ. Then R2 = 8.8kΩ can be calculated.

AXG VR

Phase Disable (Before POR)

The number of active phases is determined by the internal circuitry that monitors the ISENAxN voltages during startup. Normally, the VR operates as a 2-phase PWM controller. Pulling ISENA2N to VCC programs a 1-phase operation. Before POR, VR detects whether the voltages of ISENA2N is higher than "VCC-1V" respectively to decide how many phases should be active. Phase selection is only active during POR. When POR = high, the number of active phases is determined and latched. The unused ISENAxP pins are recommended to be connected to VCC and unused PWM pins can be left floating.

No Load Offset (Platform)

The AXG VR features no load offset function which provides the possibility of wide range positive offset of output voltage. Users can disable offset function by simply connecting OFSA/PSYS pin to GND. Figure 26 shows a voltage divider used to set no load offset voltage. No load offset voltage setting is :

$$V_{OFS_AXG} = 0.4 \times (V_{OFSA} - 1.7)$$

The range of V_{OFS_AXG} is between –500mV and 590mV and the resolution is 10mV.

For example, a 100mV no load offset requirement, V_{OFSA} needs to be set as 1.95V.

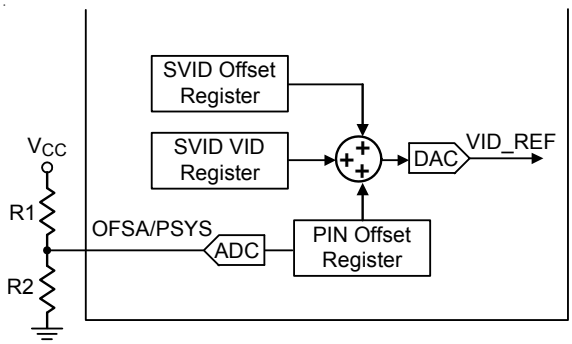

Figure 26. No Load Offset Circuit

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Switching Frequency Setting

As mention in switching frequency setting section of CORE VR, connect a resistor R_{TONA} between input terminal and TONSETA pin to set the on-time width.

$$T_{ONA} = \frac{R_{TONA} \times 4.793p \times 1.2}{V_{IN} - V_{DAC}} \quad (V_{DAC} < 1.2)$$

$$T_{ONA} = \frac{R_{TONA} \times 4.793p \times V_{DAC}}{V_{IN} - V_{DAC}} \quad (V_{DAC} \geq 1.2)$$

For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$F_{SWA(MAX)} = \frac{VID1 + \frac{IccTDC}{N} \cdot \left(DCR + \frac{R_{ON_LS,max}}{n_{LS}} - N \cdot R_{LL} \right)}{\left[V_{IN(MAX)} + \frac{IccTDC}{N} \cdot \left(\frac{R_{ON_LS,max}}{n_{LS}} - \frac{R_{ON_HS,max}}{n_{HS}} \right) \right] \cdot (T_{ONA} - T_D + T_{ONA,VAR}) + \frac{IccTDC}{N} \cdot \left(\frac{R_{ON_LS,max}}{n_{LS}} \right) \cdot T_D}$$

where $F_{SW(MAX)}$ is the maximum switching frequency, VID1 is the typical VID of application, $V_{IN\,(MAX)}$ is the maximum application input voltage, IccTDC is the thermal design current of application, N is the phase number. The $R_{ON_HS,max}$ is the maximum equivalent high-side $R_{DS(ON)}$, and n_{HS} is the number of high-side MOSFETs; $R_{ON_LS,max}$ is the maximum equivalent low-side $R_{DS(ON)}$, and n_{LS} is the number of low-side MOSFETs. T_D is the summation of the high-side MOSFET delay time and the rising time, $T_{ON,VAR}$ is the T_{ON} variation value. DCR is the inductor DCR, and R_{LL} is the loadline setting. In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the R_{TON} for RT3606BC.

When load increases, on-time keeps constant. The off-time width will be reduced so that loading can load more power from input terminal to regulate output voltage. Hence the loading current usually increases in case the switching frequency also increases. Higher switching frequency operation can reduce power components' size and PCB space, trading off the whole efficiency since switching related switching related loss increases, vice versa.

Per Phase Current Sense

In the RT3606BC, the current signal is used for load-line setting and Over-Current Protection (OCP). The inductor current sense method adopts the lossless current sensing for allowing high efficiency as illustrated in the Figure 27. When inductance and DCR time constant is equal to $R_{AX}C_{AX}$ filter network time constant, a voltage I_{LAx} x DCR will drop on C_{AX} to generate inductor current signal. According to the Figure 27, the ISENAxN is as follows :

$$ISENAxN = \frac{I_{LAX} \times DCR}{R_{CSAx}}$$

Where L_{AX} / DCR = $R_{AX}C_{AX}$ is held. The method can get high efficiency performance, but DCR value will be drifted by temperature, a NTC resistor should add in the resistor network in the IMONA pin to achieve DCR thermal compensation.

In RT3606BC design, the resistance of R_{CSAx} is restricted to 680Ω; moreover, the error of R_{CSAx} is recommended to be 1% or smaller.

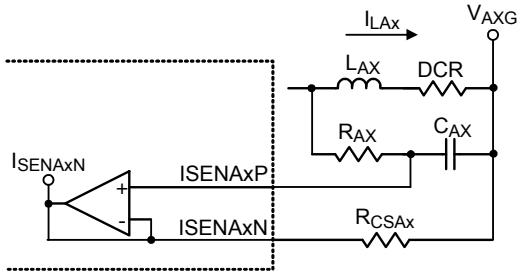

Figure 27. Lossless Current Sense Method

Total Current Sense

As presented in total current sense section of AXG VR, Figure 28 shows the total current sense method which connects the resistor network between IMONA and VREF pins to set a part of current loop gain for load-line (droop) setting and set accurate over current protection.

$$V_{IMONA} - V_{REF} = \frac{DCR}{R_{CS}} \times R_{EQA} \times (I_{LA1} + I_{LA2})$$

R_{EQA} includes a NTC resistor to compensate DCR thermal drifting for high accuracy load-line (droop).

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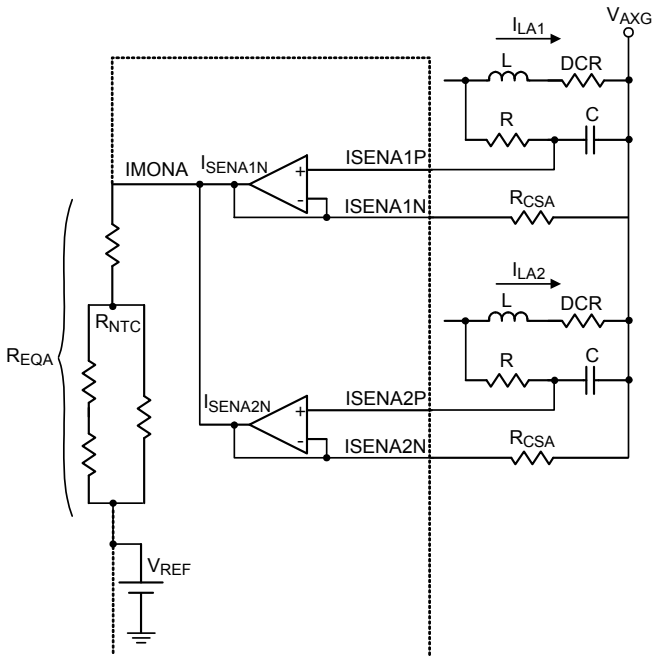

Figure 28. Total Current Sense Method

Load-Line (Droop) Setting

The G-NAVP^{TM} topology can set load-line (droop) via the current loop and the voltage loop, the load-line is a slope between load current I_{CCA} and output voltage V_{AXG} as shown Figure 29. Figure 30 shows the voltage control and current loop. By using the both loops, the load-line (droop) can be set easily. The load-line set equation is :

$$R_{LLA} = \frac{A_I}{A_V} = \frac{\frac{1}{3} \times \frac{DCR}{R_{CS}} \times R_{EQA}}{\frac{RA2}{RA1}} (m\Omega)$$

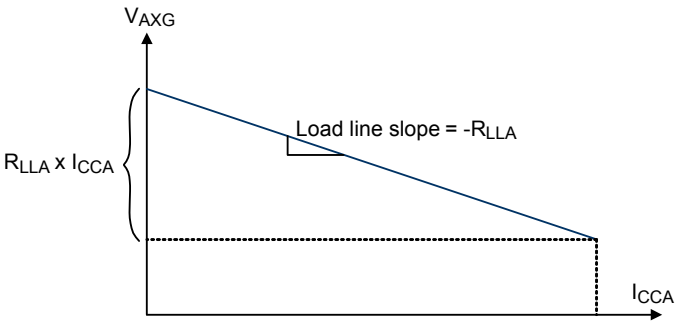

Figure 29. Load-Line (Droop)

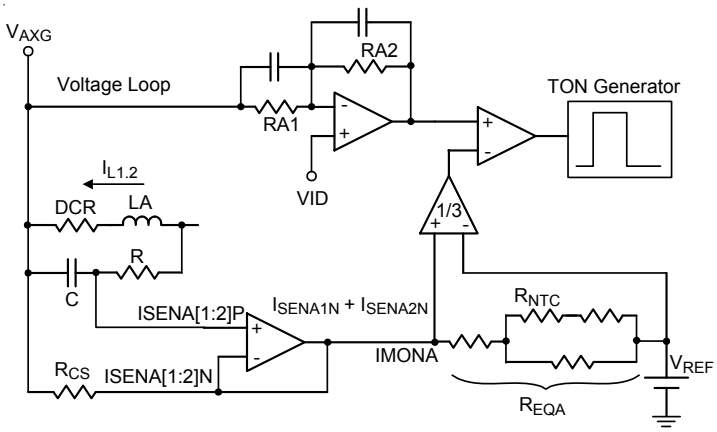

Figure 30. Voltage Loop and Current Loop

Compensator Design

The compensator of RT3606BC doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in G-NAVP^{TM} topology to achieve constant output impedance design for Intel IMVP8 ACLL specification. The one pole one zero compensator is shown as Figure 31, the transfer function of compensator should be design as following transfer function to achieve constant output impedance, i.e. Zo(s) = load-line slope in the entire frequency range

$$G_{CON}(S) \approx \frac{A_I}{R_{LLA}} \frac{1 + \frac{s}{\omega \times f_{SWA}}}{1 + \frac{s}{\omega_{ESRA}}}$$

Where A_I is current loop gain, R_{LLA} is load line for AXG VR, f_{SWA} is switching frequency for AXG VR and ω_{ESRA} is a pole that should be located at 1 / (C_{OUTA} x ESR). Then the CA1 and CA2 should be designed as follows :

$$CA1 = \frac{1}{RA1 \times \pi \times f_{SWA}}$$

$$CA2 = \frac{C_{OUTA} \times ESR}{RA2}$$

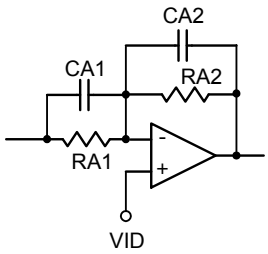

Figure 31. Type I Compensator

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Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{CCAXG_SENSE} and V_{SSAXG_SENSE}. Connect RGNDA to V_{SSAXG_SENSE} and connect FBA to V_{CCAXG_SENSE} with a resistor to build the negative input path of the error amplifier as shown in Figure 32. The V_{DAC} and the precision voltage reference are referred to RGNDA for accurate remote sensing.

Maximum Processor Current Setting, ICCMAXA

The maximum processor current ICCMAXA can be set by the SETA1 pin. ICCMAXA register is set by an external voltage divider with the multi-function mechanism. Table 9 shows the ICCMAXA setting on the SETA1 pin. For example, ICCMAXA = 40A, the VICCMAXA needs to set as 0.253 typical. Additionally, $V_{IMONA} - V_{REF}$ needs to be set as 1.6V at ICCMAXA when the maximum phase >1. As in 1-phase application, the $V_{IMONA} - V_{REF}$ needs to be set as 0.4V at ICCMAXA. The ICCMAXA alert signal will be pulled to low level.

if $V_{IMONA} - V_{REF}$ = 1.6V (for maximum phase >1) or $V_{IMONA} - V_{REF}$ = 0.4V (for 1-phase application)

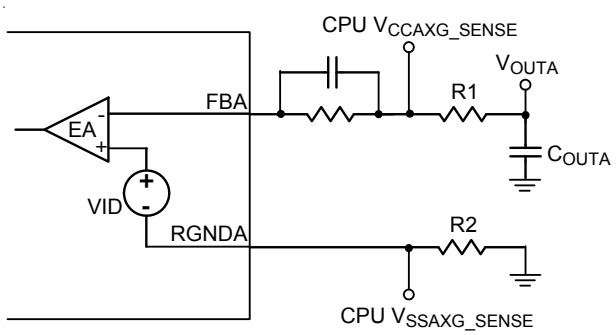

Figure 32. Remote Sensing Circuit

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Table 9. SETA1 Pin Setting for ICCMAXA

$V_{SETA1} = \frac{R2}{R1+R2} \times 3.2V$				ICCMAXA	Unit
Min	Typical	Max	Unit		
0.000	3.128	6.256	mV	0	A
12.512	15.640	18.768	mV	2	A
25.024	28.152	31.281	mV	4	A
37.537	40.665	43.793	mV	6	A
50.049	53.177	56.305	mV	8	A
62.561	65.689	68.817	mV	10	A
75.073	78.201	81.329	mV	12	A
87.586	90.714	93.842	mV	14	A
100.098	103.226	106.354	mV	16	A
112.610	115.738	118.866	mV	18	A
125.122	128.250	131.378	mV	20	A
137.634	140.762	143.891	mV	22	A
150.147	153.275	156.403	mV	24	A
162.659	165.787	168.915	mV	26	A
175.171	178.299	181.427	mV	28	A
187.683	190.811	193.939	mV	30	A
200.196	203.324	206.452	mV	32	A
212.708	215.836	218.964	mV	34	A
225.220	228.348	231.476	mV	36	A
237.732	240.860	243.988	mV	38	A
250.244	253.372	256.500	mV	40	A
262.757	265.885	269.013	mV	42	A
275.269	278.397	281.525	mV	44	A
287.781	290.909	294.037	mV	46	A
300.293	303.421	306.549	mV	48	A
312.805	315.934	319.062	mV	50	A
325.318	328.446	331.574	mV	52	A
337.830	340.958	344.086	mV	54	A
350.342	353.470	356.598	mV	56	A
362.854	365.982	369.110	mV	58	A
375.367	378.495	381.623	mV	60	A
387.879	391.007	394.135	mV	62	A
400.391	403.519	406.647	mV	64	A
412.903	416.031	419.159	mV	66	A

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$V_{SETA1} = \frac{R2}{R1+R2} \times 3.2V$				ICCMAXA	Unit
Min	Typical	Max	Unit		
425.415	428.543	431.672	mV	68	A
437.928	441.056	444.184	mV	70	A
450.440	453.568	456.696	mV	72	A
462.952	466.080	469.208	mV	74	A
475.464	478.592	481.720	mV	76	A
487.977	491.105	494.233	mV	78	A
500.489	503.617	506.745	mV	80	A
513.001	516.129	519.257	mV	82	A
525.513	528.641	531.769	mV	84	A
538.025	541.153	544.282	mV	86	A
550.538	553.666	556.794	mV	88	A
563.050	566.178	569.306	mV	90	A
575.562	578.690	581.818	mV	92	A
588.074	591.202	594.330	mV	94	A
600.587	603.715	606.843	mV	96	A
613.099	616.227	619.355	mV	98	A
625.611	628.739	631.867	mV	100	A
638.123	641.251	644.379	mV	102	A
650.635	653.763	656.891	mV	104	A
663.148	666.276	669.404	mV	106	A
675.660	678.788	681.916	mV	108	A
688.172	691.300	694.428	mV	110	A
700.684	703.812	706.940	mV	112	A
713.196	716.325	719.453	mV	114	A
725.709	728.837	731.965	mV	116	A
738.221	741.349	744.477	mV	118	A
750.733	753.861	756.989	mV	120	A
763.245	766.373	769.501	mV	122	A
775.758	778.886	782.014	mV	124	A
788.270	791.398	794.526	mV	126	A
800.782	803.910	807.038	mV	128	A
813.294	816.422	819.550	mV	130	A
825.806	828.935	832.063	mV	132	A
838.319	841.447	844.575	mV	134	A
850.831	853.959	857.087	mV	136	A

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$V_{SETA1} = \frac{R2}{R1+R2} \times 3.2V$				ICCMAXA	Unit
Min	Typical	Max	Unit		
863.343	866.471	869.599	mV	138	A
875.855	878.983	882.111	mV	140	A
888.368	891.496	894.624	mV	142	A
900.880	904.008	907.136	mV	144	A
913.392	916.520	919.648	mV	146	A
925.904	929.032	932.160	mV	148	A
938.416	941.544	944.673	mV	150	A
950.929	954.057	957.185	mV	152	A
963.441	966.569	969.697	mV	154	A
975.953	979.081	982.209	mV	156	A
988.465	991.593	994.721	mV	158	A
1000.978	1004.106	1007.234	mV	160	A
1013.490	1016.618	1019.746	mV	162	A
1026.002	1029.130	1032.258	mV	164	A
1038.514	1041.642	1044.770	mV	166	A
1051.026	1054.154	1057.283	mV	168	A
1063.539	1066.667	1069.795	mV	170	A
1076.051	1079.179	1082.307	mV	172	A
1088.563	1091.691	1094.819	mV	174	A
1101.075	1104.203	1107.331	mV	176	A
1113.587	1116.716	1119.844	mV	178	A
1126.100	1129.228	1132.356	mV	180	A
1138.612	1141.740	1144.868	mV	182	A
1151.124	1154.252	1157.380	mV	184	A
1163.636	1166.764	1169.892	mV	186	A
1176.149	1179.277	1182.405	mV	188	A
1188.661	1191.789	1194.917	mV	190	A
1201.173	1204.301	1207.429	mV	192	A
1213.685	1216.813	1219.941	mV	194	A
1226.197	1229.326	1232.454	mV	196	A
1238.710	1241.838	1244.966	mV	198	A
1251.222	1254.350	1257.478	mV	200	A
1263.734	1266.862	1269.990	mV	202	A
1276.246	1279.374	1282.502	mV	204	A
1288.759	1291.887	1295.015	mV	206	A

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$V_{SETA1} = \frac{R2}{R1+R2} \times 3.2V$				ICCMAXA	Unit
Min	Typical	Max	Unit		
1301.271	1304.399	1307.527	mV	208	A
1313.783	1316.911	1320.039	mV	210	A
1326.295	1329.423	1332.551	mV	212	A
1338.807	1341.935	1345.064	mV	214	A
1351.320	1354.448	1357.576	mV	216	A
1363.832	1366.960	1370.088	mV	218	A
1376.344	1379.472	1382.600	mV	220	A
1388.856	1391.984	1395.112	mV	222	A
1401.369	1404.497	1407.625	mV	224	A
1413.881	1417.009	1420.137	mV	226	A
1426.393	1429.521	1432.649	mV	228	A
1438.905	1442.033	1445.161	mV	230	A
1451.417	1454.545	1457.674	mV	232	A
1463.930	1467.058	1470.186	mV	234	A
1476.442	1479.570	1482.698	mV	236	A
1488.954	1492.082	1495.210	mV	238	A
1501.466	1504.594	1507.722	mV	240	A
1513.978	1517.107	1520.235	mV	242	A
1526.491	1529.619	1532.747	mV	244	A
1539.003	1542.131	1545.259	mV	246	A
1551.515	1554.643	1557.771	mV	248	A
1564.027	1567.155	1570.283	mV	250	A
1576.540	1579.668	1582.796	mV	252	A
1589.052	1592.180	1595.308	mV	254	A

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Dynamic VID (DVID) Compensation for AXG VR

As mention in DVID compensation section of CORE VR, the RT3606BC also provide a DVID compensation function for AXG VR. A virtual charge current signal can be established by SETA1 and SETA2 pins to cancel the real induced charge current signal.

Table 10 show the DVID_Threshold in SETA1 pin with internal 80μA current source and Table 11 describes DVID_Width settings on SETA2 pin with external voltage divider. For example, 39.67mV DVID_Threshold (SR = 11.25mV/μs) / 119mV DVID_Threshold (SR = 33.75mV/μs) and 36μs DVID_Width are designed (OCPA sets as 110% ICCMAXA, RSETA sets as 133% low frequency ramp / 200% high frequency ramp). According to the Table 10 and Table 11, the DVID_Threshold set voltage should be between 0.4254V to 0.4473V and the DVID_Width set voltage should be between 1.051V to 1.073V. Please note that a high accuracy resistor is needed for this setting, < 1% error tolerance is recommended.

Table 10. SETA1 Pin Setting for DVID_Threshold

$\Delta V_{SETA1} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$				DVID_Threshold		OCP = %ICCMAX
Min	Typical	Max	Unit	DVID SR = 11.25mV/μs	DVID SR = 33.75mV/μs	
0.000	10.948	21.896	mV	18.33mV	55mV	NA
25.024	35.973	46.921	mV			110%
50.049	60.997	71.945	mV			120%
75.073	86.022	96.970	mV			130%
100.098	111.046	121.994	mV			140%
125.122	136.070	147.019	mV			150%
150.147	161.095	172.043	mV			160%
175.171	186.119	197.067	mV			NA
200.196	211.144	222.092	mV	29mV	87mV	NA
225.220	236.168	247.116	mV			110%
250.244	261.193	272.141	mV			120%
275.269	286.217	297.165	mV			130%
300.293	311.241	322.190	mV			140%
325.318	336.266	347.214	mV			150%
350.342	361.290	372.239	mV			160%
375.367	386.315	397.263	mV			NA
400.391	411.339	422.287	mV	39.67mV	119mV	NA
425.415	436.364	447.312	mV			110%
450.440	461.388	472.336	mV			120%
475.464	486.413	497.361	mV			130%
500.489	511.437	522.385	mV			140%
525.513	536.461	547.410	mV			150%
550.538	561.486	572.434	mV			160%
575.562	586.510	597.458	mV			NA

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$\Delta V_{SETA1} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$				DVID_Threshold		OCP = %ICCMAX
Min	Typical	Max	Unit	DVID SR = 11.25mV/μs	DVID SR = 33.75mV/μs	
600.587	611.535	622.483	mV	50.33mV	151mV	NA
625.611	636.559	647.507	mV			110%
650.635	661.584	672.532	mV			120%
675.660	686.608	697.556	mV			130%
700.684	711.632	722.581	mV			140%
725.709	736.657	747.605	mV			150%
750.733	761.681	772.630	mV			160%
775.758	786.706	797.654	mV			NA
800.782	811.730	822.678	mV	61mV	183mV	NA
825.806	836.755	847.703	mV			110%
850.831	861.779	872.727	mV			120%
875.855	886.804	897.752	mV			130%
900.880	911.828	922.776	mV			140%
925.904	936.852	947.801	mV			150%
950.929	961.877	972.825	mV			160%
975.953	986.901	997.849	mV			NA
1000.978	1011.926	1022.874	mV	71.67mV	215mV	NA
1026.002	1036.950	1047.898	mV			110%
1051.026	1061.975	1072.923	mV			120%
1076.051	1086.999	1097.947	mV			130%
1101.075	1112.023	1122.972	mV			140%
1126.100	1137.048	1147.996	mV			150%
1151.124	1162.072	1173.021	mV			160%
1176.149	1187.097	1198.045	mV			NA
1201.173	1212.121	1223.069	mV	82.33mV	247mV	NA
1226.197	1237.146	1248.094	mV			110%
1251.222	1262.170	1273.118	mV			120%
1276.246	1287.195	1298.143	mV			130%
1301.271	1312.219	1323.167	mV			140%
1326.295	1337.243	1348.192	mV			150%
1351.320	1362.268	1373.216	mV			160%
1376.344	1387.292	1398.240	mV			NA
1401.369	1412.317	1423.265	mV	93mV	279mV	NA
1426.393	1437.341	1448.289	mV			110%
1451.417	1462.366	1473.314	mV			120%
1476.442	1487.390	1498.338	mV			130%
1501.466	1512.414	1523.363	mV			140%
1526.491	1537.439	1548.387	mV			150%
1551.515	1562.463	1573.412	mV			160%
1576.540	1587.488	1598.436	mV			NA

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Table 11. SETA2 Pin Setting for DVID_Width

$V_{SETA2} = 3.2V \times \frac{R2}{R1+R2}$				DVID_Width	RSET %410k RTON	
Min	Typical	Max	Unit		Low F_{SW} Ramp	High F_{SW} Ramp
0.000	10.948	21.896	mV	6μs	100%	133%
25.024	35.973	46.921	mV		117%	167%
50.049	60.997	71.945	mV		133%	200%
75.073	86.022	96.970	mV		150%	233%
100.098	111.046	121.994	mV		167%	267%
125.122	136.070	147.019	mV		183%	300%
150.147	161.095	172.043	mV		200%	333%
175.171	186.119	197.067	mV		217%	367%
200.196	211.144	222.092	mV	12μs	100%	133%
225.220	236.168	247.116	mV		117%	167%
250.244	261.193	272.141	mV		133%	200%
275.269	286.217	297.165	mV		150%	233%
300.293	311.241	322.190	mV		167%	267%
325.318	336.266	347.214	mV		183%	300%
350.342	361.290	372.239	mV		200%	333%
375.367	386.315	397.263	mV		217%	367%
400.391	411.339	422.287	mV	18μs	100%	133%
425.415	436.364	447.312	mV		117%	167%
450.440	461.388	472.336	mV		133%	200%
475.464	486.413	497.361	mV		150%	233%
500.489	511.437	522.385	mV		167%	267%
525.513	536.461	547.410	mV		183%	300%
550.538	561.486	572.434	mV		200%	333%
575.562	586.510	597.458	mV		217%	367%
600.587	611.535	622.483	mV	24μs	100%	133%
625.611	636.559	647.507	mV		117%	167%
650.635	661.584	672.532	mV		133%	200%
675.660	686.608	697.556	mV		150%	233%
700.684	711.632	722.581	mV		167%	267%
725.709	736.657	747.605	mV		183%	300%
750.733	761.681	772.630	mV		200%	333%
775.758	786.706	797.654	mV		217%	367%

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$V_{SETA2} = 3.2V \times \frac{R2}{R1+R2}$				DVID_Width	RSET %410k RTON	
Min	Typical	Max	Unit		Low F_{SW} Ramp	High F_{SW} Ramp
800.782	811.730	822.678	mV	30μs	100%	133%
825.806	836.755	847.703	mV		117%	167%
850.831	861.779	872.727	mV		133%	200%
875.855	886.804	897.752	mV		150%	233%
900.880	911.828	922.776	mV		167%	267%
925.904	936.852	947.801	mV		183%	300%
950.929	961.877	972.825	mV		200%	333%
975.953	986.901	997.849	mV		217%	367%
1000.978	1011.926	1022.874	mV	36μs	100%	133%
1026.002	1036.950	1047.898	mV		117%	167%
1051.026	1061.975	1072.923	mV		133%	200%
1076.051	1086.999	1097.947	mV		150%	233%
1101.075	1112.023	1122.972	mV		167%	267%
1126.100	1137.048	1147.996	mV		183%	300%
1151.124	1162.072	1173.021	mV		200%	333%
1176.149	1187.097	1198.045	mV		217%	367%
1201.173	1212.121	1223.069	mV	42μs	100%	133%
1226.197	1237.146	1248.094	mV		117%	167%
1251.222	1262.170	1273.118	mV		133%	200%
1276.246	1287.195	1298.143	mV		150%	233%
1301.271	1312.219	1323.167	mV		167%	267%
1326.295	1337.243	1348.192	mV		183%	300%
1351.320	1362.268	1373.216	mV		200%	333%
1376.344	1387.292	1398.240	mV		217%	367%
1401.369	1412.317	1423.265	mV	48μs	100%	133%
1426.393	1437.341	1448.289	mV		117%	167%
1451.417	1462.366	1473.314	mV		133%	200%
1476.442	1487.390	1498.338	mV		150%	233%
1501.466	1512.414	1523.363	mV		167%	267%
1526.491	1537.439	1548.387	mV		183%	300%
1551.515	1562.463	1573.412	mV		200%	333%
1576.540	1587.488	1598.436	mV		217%	367%

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Ramp Compensation

G-NAVP^{TM} topology is one type of ripple based control that has fast transient response and can lower BOM cost. However, ripple based control usually has poor noise immunity. The RT3606BC provides the ramp compensation in AXG VR to increase noise immunity and reduce jitter at the switching node. Figure 33 shows the ramp compensation.

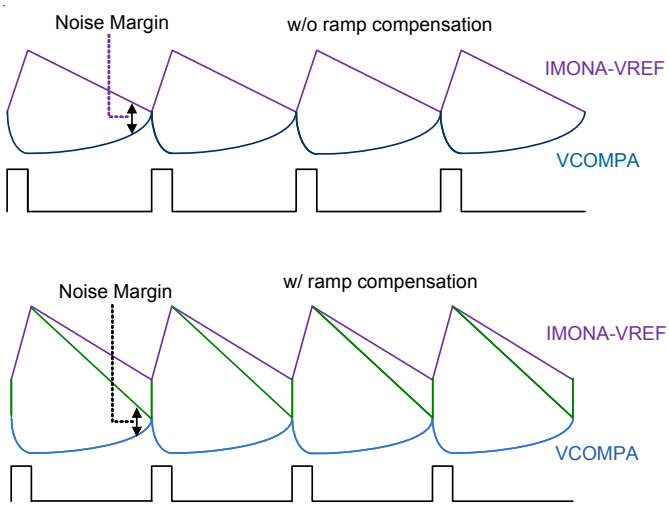

Figure 33. Ramp Compensation

For the RT3606BC, the ramp compensation also needs to be considered during mode transition from PS0/1 to PS2. For achieving smooth mode transition into PS2, a proper ramp compensation design is necessary. Since the ramp compensation needs to be proportional to the on-time, then RAMP is set as

$$133\% \times \frac{F_S}{400k}$$

Quick Response (QR) Mechanism

As presented in QR mechanism section of CORE VR, RT3606BC also supports QR function in AXG VR. The output voltage signal behavior needs to be detected so that QR mechanism can be trigged. The output voltage signal is via a remote sense line to connect at VSENA pin that is shown in Figure 34. The QR mechanism needs to set QR width and QR threshold. Both definitions are shown in Figure 22. A proper QR mechanism set can meet different applications. SETA2 can set QR threshold and QR width by internal current source 80μA with multi-function pin setting mechanism.

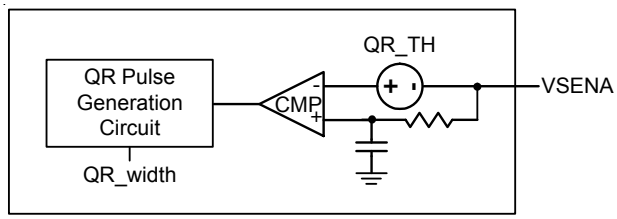

Figure 34. Simplified QR Trigger Schematic

For example, QR threshold 20mV/10mV at PS0/PS1 and 2.22 x TON QR width are set. According to the Table 12, the set voltage should be between 0.4504V and 0.4723V. Please note that a high accuracy resistor is needed for this setting accuracy, < 1% error tolerance is recommended. In the Table 12, there are some "NA" marks in QRWIDTH section. It means that user should not use it to avoid the possibility of shift digital code due to tolerance concern.

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Table 12. SETA2 Pin Setting for QR Threshold and QR Width

$\Delta V_{SETA2} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$				QR Threshold		QR Width (%TON)
Min	Typical	Max	Unit	PS0	PS1	
0.000	10.948	21.896	mV	15mV	10mV	NA
25.024	35.973	46.921	mV			Disable
50.049	60.997	71.945	mV			222%
75.073	86.022	96.970	mV			177.6%
100.098	111.046	121.994	mV			133.2%
125.122	136.070	147.019	mV			88%
150.147	161.095	172.043	mV			44%
175.171	186.119	197.067	mV			NA
200.196	211.144	222.092	mV	15mV	15mV	NA
225.220	236.168	247.116	mV			Disable
250.244	261.193	272.141	mV			222%
275.269	286.217	297.165	mV			177.6%
300.293	311.241	322.190	mV			133.2%
325.318	336.266	347.214	mV			88%
350.342	361.290	372.239	mV			44%
375.367	386.315	397.263	mV			NA
400.391	411.339	422.287	mV	20mV	10mV	NA
425.415	436.364	447.312	mV			Disable
450.440	461.388	472.336	mV			222%
475.464	486.413	497.361	mV			177.6%
500.489	511.437	522.385	mV			133.2%
525.513	536.461	547.410	mV			88%
550.538	561.486	572.434	mV			44%
575.562	586.510	597.458	mV			NA
600.587	611.535	622.483	mV	20mV	15mV	NA
625.611	636.559	647.507	mV			Disable
650.635	661.584	672.532	mV			222%
675.660	686.608	697.556	mV			177.6%
700.684	711.632	722.581	mV			133.2%
725.709	736.657	747.605	mV			88%
750.733	761.681	772.630	mV			44%
775.758	786.706	797.654	mV			NA

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$\Delta V_{SETA2} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$				QR Threshold		QR Width (%TON)
Min	Typical	Max	Unit	PS0	PS1	
800.782	811.730	822.678	mV	25mV	10mV	NA
825.806	836.755	847.703	mV			Disable
850.831	861.779	872.727	mV			222%
875.855	886.804	897.752	mV			177.6%
900.880	911.828	922.776	mV			133.2%
925.904	936.852	947.801	mV			88%
950.929	961.877	972.825	mV			44%
975.953	986.901	997.849	mV			NA
1000.978	1011.926	1022.874	mV	25mV	15mV	NA
1026.002	1036.950	1047.898	mV			Disable
1051.026	1061.975	1072.923	mV			222%
1076.051	1086.999	1097.947	mV			177.6%
1101.075	1112.023	1122.972	mV			133.2%
1126.100	1137.048	1147.996	mV			88%
1151.124	1162.072	1173.021	mV			44%
1176.149	1187.097	1198.045	mV			NA
1201.173	1212.121	1223.069	mV	30mV	10mV	NA
1226.197	1237.146	1248.094	mV			Disable
1251.222	1262.170	1273.118	mV			222%
1276.246	1287.195	1298.143	mV			177.6%
1301.271	1312.219	1323.167	mV			133.2%
1326.295	1337.243	1348.192	mV			88%
1351.320	1362.268	1373.216	mV			44%
1376.344	1387.292	1398.240	mV			NA
1401.369	1412.317	1423.265	mV	30mV	15mV	NA
1426.393	1437.341	1448.289	mV			Disable
1451.417	1462.366	1473.314	mV			222%
1476.442	1487.390	1498.338	mV			177.6%
1501.466	1512.414	1523.363	mV			133.2%
1526.491	1537.439	1548.387	mV			88%
1551.515	1562.463	1573.412	mV			44%
1576.540	1587.488	1598.436	mV			NA

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Current Monitor, IMONA

RT3606BC includes a current monitor (IMONA) function which can be used to detect over current protection and the maximum processor current ICCMAXA, and also sets a part of current gain in the load-line setting. It produces an analog voltage proportional to output current between the IMONA and VREF pins.

The calculation for IMONA-VREF voltage is shown as below :

$$V_{IMONA} - V_{REF} = \frac{DCR}{R_{CSA}} \times R_{EQA} \times (I_{LA1} + I_{LA2})$$

Where $I_{LA1} + I_{LA2}$ are output current and the definitions of DCR, R_{CSA} and R_{EQA} can refer to Figure 28.

Over Current Protection

RT3606BC provides the Over Current Protection (OCP) which is set by the SETA1 pin in AXG VR. The OCP threshold setting can refer to ICCMAXA current in the Table 9. For example, if ICCMAXA is set as 120A, user can set voltage by using the external voltage divider on SETA1 pin as 0.759V typically. If 156A OCP (130% x ICCMAX) threshold and DVID_TH (SR = 11.25mV/μs) = 39.67mV / DVID_TH (SR = 33.75mV/μs) = 119mV will be set. According to Table 10, the set voltage should be between 0.4755V and 0.4974V. When output current is higher than the OCP threshold, OCP is latched with a 40μs delay to prevent false trigger. Besides, the OCP function is masked when dynamic VID transient occurs, and soft-start period. And the OCP function will re-active after 46μs of DVID or soft-start alert is asserted.

Output Over-Voltage Protection

An OVP condition is detected when the VSENA pin is 150mV more than VID. as VID > 1V. If VID < 1V, the OVP is detected when the VSEN pin is 350mV more than 1V. When OVP is detected, the high-side gate voltage UGATEAx is pulled low and the low-side gate voltage LGATEAx is pulled high, OVP is latched with a 0.5μs delay to prevent false trigger. Besides, the OVP function will be masked during DVID and soft-start period. After 46μs of DVID or soft-start alert is asserted, the OVP function will re-active.

Negative Voltage Protection

Since the OVP latch continuously turns on all low-side MOSFETs of the VR, the VR will suffer negative output voltage. When the VSENA detects a voltage below –0.07V after triggering OVP, the VR triggers NVP to turn off all low-side MOSFETs of the VR while the high-side MOSFETs remain off. After triggering NVP, if the output voltage rises above 0V, the OVP latch restarts to turn on all low-side MOSFETs. Therefore, the output voltage may bounce between 0V and –0.07V due to OVP latch and NVP triggering. The NVP function will be active only after OVP is triggered.

Current Loop Design in Details

Figure 35 shows the whole current loop structure. The current loop plays an important role in the RT3606BC that can decide ACLL performance, DCLL accuracy and ICCMAXA accuracy. For ACLL performance, the correct compensator design is assumed, if RC network time constant matches inductor time constant L_{AX} / DCR_X, an expected load transient waveform can be designed. If R_XC_X network time constant is larger than inductor time constant L_{AX} / DCR_X, V_{AXG} waveform has a sluggish droop during load transient. If R_XC_X network is smaller than inductor time constant L_{AX} /DCR_X, a worst V_{AXG} waveform will sag to create an undershooting to fail the specification.

For DCLL performance and ICCMAXA accuracy, since the copper wire of inductor has a positive temperature coefficient, when temperature goes high in the heavy load condition, DCR value goes large simultaneously. A resistor network with NTC thermistor compensation connecting between the IMONA to REF pins is necessary, to compensate the positive temperature coefficient of inductor DCR. The design flow is as presented in current loop design in details of CORE VR.

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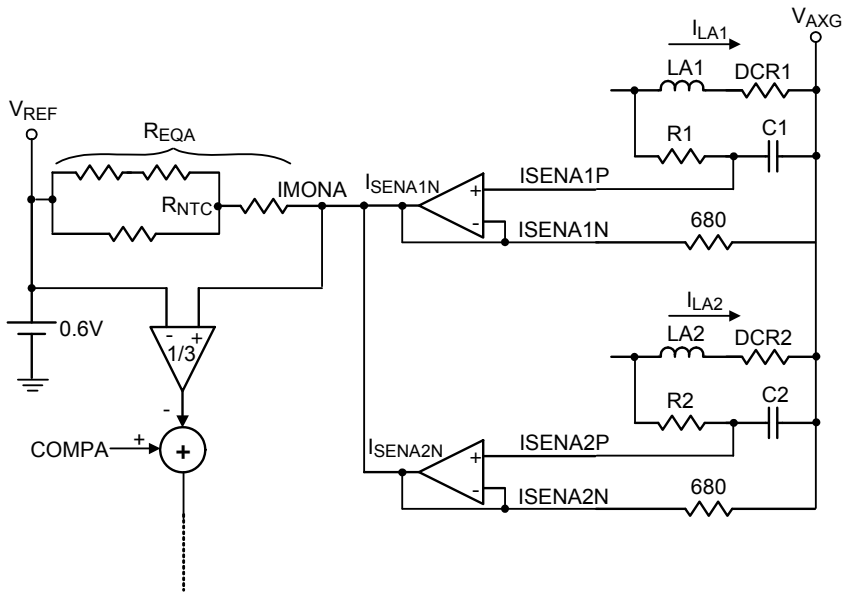

Figure 35. Current Loop Structure

System Input Power Monitor, PSYS

The RT3606BC provides PSYS function to monitor total platform system power, and the obtained information will be provided directly to the CPU via the SVID interface. The PSYS function can be enabled/disabled by the SET3 pin. The PSYS function can be described as in Figure36. When PSYS voltage V_{PSYS} = 3.2V, the RT3606BC will generate an 8-bit code, FF, for 100% Pmax, which will be stored in the 1Bh register. To choose the resistor value R, for example, if the maximum current from the PSYS "Meter" I = 320μA in conjunction with V_{PSYS} = 3.2V for 100% Pmax, R = V_{PSYS} / I =10kΩ can be obtained. The resistor must be as close to the RT3606BC as.

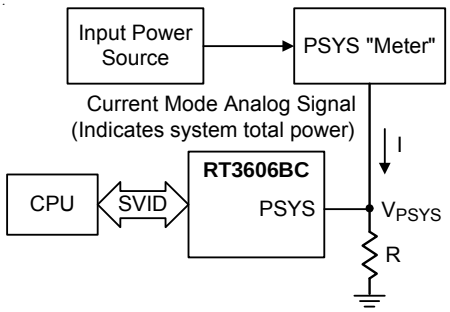

Figure 36. PSYS Function Block Diagram

Design Step

The RT3606BC excel based design tool is available. Users can contact your Richtek representative to get the spreadsheet. Three main design procedures for RT3606BC design, first step is initial settings, second step is loop design and the last step is protection settings. The following design example is to explain RT3606BC design procedure :

	V_{AXG} Specification
Input Voltage	12V
No. of Phases	2
Vboot	0.9V
ICCMAX	76A
ICC-DY	42A
ICC-TDC	45A
Load Line	3.1mΩ
Fast Slew Rate	10mV/μs
Max Switching Frequency	400kHz

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In IMVP8 VRTB Guideline, the output filter requirements of VRTB specification for desktop platform are :

Output Inductor : 220nH/0.49mΩ

Output Bulk Capacitor : 470μF/2.5V/7mΩ (max) 4 to 5pcs

Output Ceramic Capacitor : 22μF/0805 (14pcs max in cavity)

(1) Initial Settings :

RT3606BC initial voltage is 0.9V

(2) Loop Design :

On time setting : Using the specification, T_{ONA} is

$$T_{ONA} = \frac{T_{ONA} \times 4.73p \times 1.2}{V_{IN}-V_{DAC}} (V_{DAC} < 1.2) = 204n$$

The on time setting resistor R_{TONA} = 400kΩ

- Current sensor adopts lossless RC filter to sense current signal in DCR. For getting an expect load transient waveform, RxCx time constant needs to match Lx / DCRx per phase. Cx = 0.47μF is set, then

$$R_X = \frac{L_X}{0.47\mu F \times DCR_X} = 780\Omega$$

- IMONA resistor network design : T_L = 25°C, T_R = 50°C and T_H = 100°C are decided, NTC thermistor = 100kΩ@25°C, β = 4485 and ICCMAXA = 76A. According to the sub-section "Current Loop Design in Details", R_{IMONA1} = 10.6kΩ, R_{IMONA2} = 15.05kΩ and R_{IMONA3} = 11.46kΩ can be decided. The R_{EQA} (25°C) = 23.86kΩ.
- Load-line design : 2.1mΩ droop is requirement, because R_{EQA}(25°C) has decided, the voltage loop Av gain is also can be decided by following equation

$$R_{LLA} = \frac{A_I}{A_V} = \frac{\frac{1}{3} \times \frac{DCR}{R_{CSA}} \times R_{EQA}}{\frac{R2}{R1}} (m\Omega)$$

Where DCR (25°C) = 0.6mΩ, R_{CS} = 680Ω and R_{EQA} (25°C) = 23.86kΩ. Hence the A_V = R2 / R1 = 2.26 can be obtained. R = 10kΩ usually is decided, so R2 = 22.6kΩ.

- Typical compensator design can use the following equations to design the C1 and C2 values

$$C2 = \frac{1}{R1 \times \pi \times f_{SWA}} \approx 87pF$$

$$C2 = \frac{C_{OUT} \times ESR}{R2} \approx 115pF$$

For Intel platform, in order to induce the band width to enhance transient performance to meet Intel's criterion, the compensator of zero can be designed close to 1/10 of switching frequency.

- SETA1 resistor network design : First the ICCMAX is design as 76A. Next, OCP threshold is designed as 1.5 x ICCMAX. Last, DVID compensation parameters need to be decided. The DVID_TH can be calculated as following equation

$$V_{DVID_TH} = LL \times C_{OUT} \times \frac{dVID}{dt}$$

Where LL is load line, C_{OUT} is total output capacitance and dVID/dt is DVID fast slew rate. Thus V_{DVID_TH} = 39.67mV is needed in this case. By using above information, the two equations can be listed by using multi-function pin setting mechanism

$$0.479 = \frac{R2}{R1+R2} \times 3.2$$

$$0.536 = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

R1 = 44.84kΩ, R2 = 7.89kΩ.

- SETA2 resistor network design :

RAMP = 133% x $\frac{400k}{400k}$ = 133%, 133% is set. And DVID_Width is chosen as 24μsec typical. Last, the QR mechanism parameters need to be designed first. Initial QR_TH is designed as 20mV and QR_Width is designed as 0.44 x T_{ON}. By using the information, the two equations can be listed by using multi-function pin setting mechanism

$$0.661 = \frac{R2}{R1+R2} \times 3.2$$

$$0.761 = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

R1 = 46.05kΩ, R2 = 12kΩ.

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(3) Protection Settings :

- OVP protections : When the VSENA pin voltage is 350mV more than VID, the OVP will be latched. When VSENA pin voltage is 350mV less than VID, the UVP will be latched.
- TSEN and $\overline{\text{VR_HOT}}$ design : Using the following equation to calculate related resistances for $\overline{\text{VR_HOT}}$ setting.

$$V_{TSENA} = 80\mu A \times \left(RA1 // \left(RA2 + R_{ANTC\ (100°C)}\right)\right)$$

(4) Addressing Settings :

- SET3 resistor network design : Based on table13 information, the two equations can be listed as following

$$0.060 = \frac{R2}{R1+R2} \times 3.2V$$

$$0.261 = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

R1 = 171.3kΩ, R2 = 3.32kΩ.

Table 13. SET3 design information

Function1	Main address:00 Auxiliary address:01	Main and auxiliary rail disable zero load	Anti-overshoot function disable	Anti-overshoot PWM behavior is high to tri stage.	AI gain is 1.
Function2	PSYS function disable	Select low frequency ramp table	DVID slew rate is 11.25mV/μs	Enable DVID compensation function	When 1 phase application, ramp increase.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-60L 7x7 package, the thermal resistance, θ_{JA}, is 25.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (25.5°C/W) = 3.92W for WQFN-60L 7x7 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 37 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

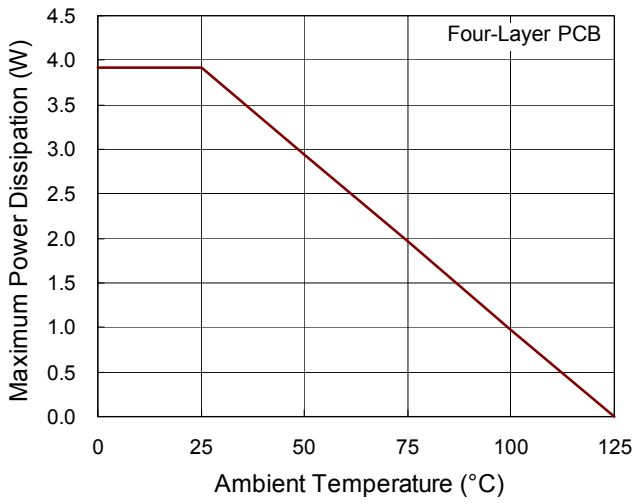

Figure 37. Derating Curve of Maximum Power Dissipation

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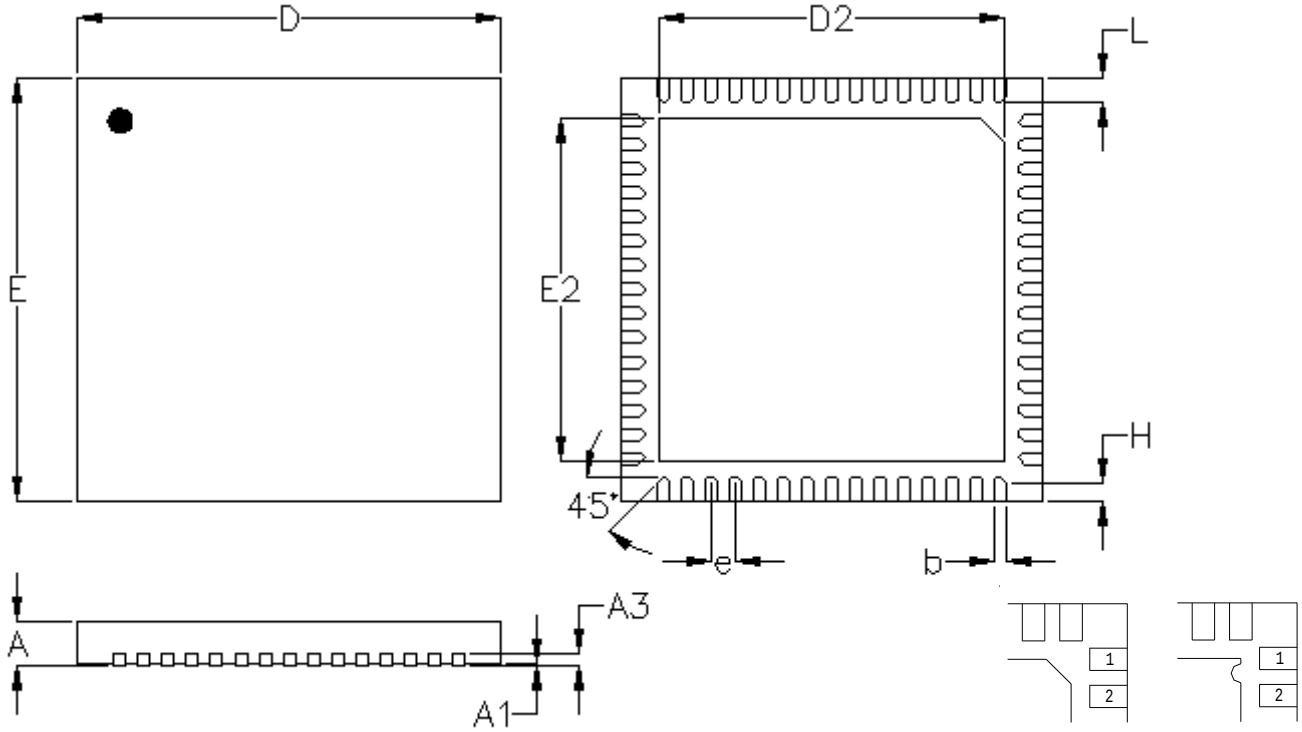
Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	6.900	7.100	0.272	0.280
D2	5.650	5.750	0.222	0.226
E	6.900	7.100	0.272	0.280
E2	5.650	5.750	0.222	0.226
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
H	0.250	0.350	0.010	0.014

W-Type 60L QFN 7x7 Package

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