

# BLF4G10-160

## UHF power LDMOS transistor

Rev. 01 — 22 June 2007

Product data sheet

## 1. Product profile

### 1.1 General description

160 W LDMOS power transistor for base station applications at frequencies from 800 MHz to 1000 MHz.

**Table 1. Typical performance**

RF performance at  $T_{case} = 25^{\circ}C$  in a common source class-AB test circuit.

Mode of operation	f (MHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	P <sub>L(AV)</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)	ACPR <sub>400</sub> (dBc)	ACPR <sub>600</sub> (dBc)	ACPR <sub>750</sub> (dBc)	ACPR <sub>1980</sub> (dBc)	EVM <sub>rms</sub> (%)	IMD3 (dBc)
CW	894	28	200	-	19.0	59	-	-	-	-	-	-
2-tone	894	28	-	80	19.7	42.5	-	-	-	-	-	-29
GSM EDGE	894	28	-	80	19.7	41.5	-61 <sup>[1]</sup>	-72 <sup>[1]</sup>	-	-	3.0	-
CDMA	881.5	28	-	40	19.0	29.5	-	-	-45 <sup>[2]</sup>	-64 <sup>[2]</sup>	-	-

[1] ACPR<sub>400</sub> and ACPR<sub>600</sub> at 30 kHz resolution bandwidth.

[2] Test signal: IS-95, with PAR = 9.9 dB at 0.01 % probability.

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

### 1.2 Features

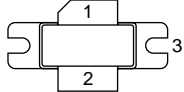
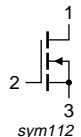
- Typical GSM EDGE performance at f = 894 MHz, V<sub>DS</sub> = 28 V and I<sub>Dq</sub> = 900 mA:
  - ◆ Average output power = 80 W
  - ◆ Gain = 19.7 dB
  - ◆ Efficiency = 41.5 %
  - ◆ ACPR<sub>400</sub> = -61 dBc
  - ◆ ACPR<sub>600</sub> = -72 dBc
  - ◆ EVM<sub>rms</sub> = 3.0 %
- Easy power control
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (800 MHz to 1000 MHz)
- Internally matched for ease of use

**1.3 Applications**

- RF power amplifiers for GSM, GSM EDGE and CDMA base stations and multi carrier applications in the 800 MHz to 1000 MHz frequency range.

**2. Pinning information**

**Table 2. Pinning**

Pin	Description	Simplified outline	Symbol
1	drain		
2	gate		
3	source		

[1] Connected to flange

**3. Ordering information**

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BLF4G10-160	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A

**4. Limiting values**

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+15	V
$I_D$	drain current		-	15	A
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	200	°C

**5. Thermal characteristics**

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Max	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C};$ $P_L = 50\text{ W}$	0.55	0.64	K/W

## 6. Characteristics

**Table 6. Characteristics**

$T_j = 25\text{ }^\circ\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ ; $I_D = 2.1\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$ ; $I_D = 230\text{ mA}$	2.5	2.9	3.5	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$ ; $I_D = 900\text{ mA}$	2.65	3.15	3.65	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 28\text{ V}$	-	-	5	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 6\text{ V}$ ; $V_{DS} = 10\text{ V}$	35	42	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 15\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	420	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}$ ; $I_D = 7.5\text{ A}$	-	11	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 6\text{ V}$ ; $I_D = 7.5\text{ A}$	-	0.065	-	$\Omega$
$C_{rs}$	feedback capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 28\text{ V}$ ; $f = 1\text{ MHz}$	-	3.0	-	pF

## 7. Application information

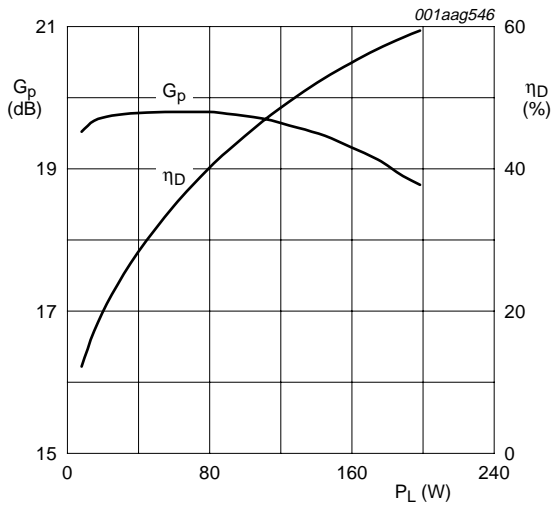
**Table 7. Application information**

Mode of operation: 2-tone;  $f_1 = 894\text{ MHz}$ ;  $f_2 = 894.2\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}$ ;  
 $I_{Dq} = 900\text{ mA}$ ;  $T_{case} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified; in a class-AB test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(PEP)} = 160\text{ W}$	18.5	19.7	-	dB
$RL_{in}$	input return loss	$P_{L(PEP)} = 160\text{ W}$	-	-10	-6	dB
$\eta_D$	drain efficiency	$P_{L(PEP)} = 160\text{ W}$	40	42.5	-	%
IMD3	third order intermodulation distortion	$P_{L(PEP)} = 160\text{ W}$	-	-29	-26	dBc
IMD5	fifth order intermodulation distortion	$P_{L(PEP)} = 160\text{ W}$	-	-38	-35	dBc
IMD7	seventh order intermodulation distortion	$P_{L(PEP)} = 160\text{ W}$	-	-57	-53	dBc

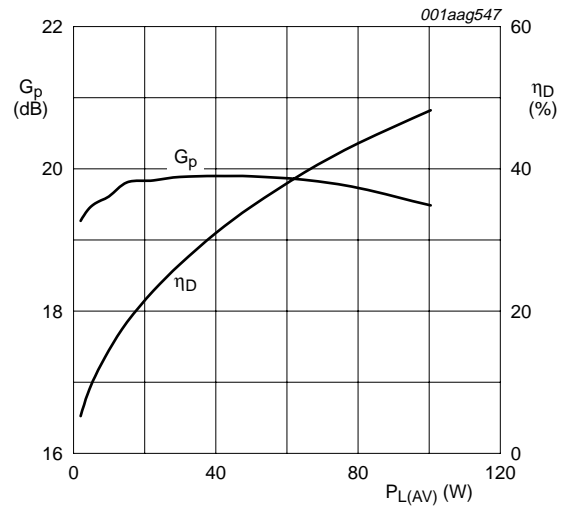
### 7.1 Ruggedness in class-AB operation

The BLF4G10-160 is capable of withstanding a load mismatch corresponding to  $VSWR = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 28\text{ V}$ ;  
 $I_{Dq} = 900\text{ mA}$ ;  $P_L = 160\text{ W}$  (CW);  $f = 894\text{ MHz}$ .



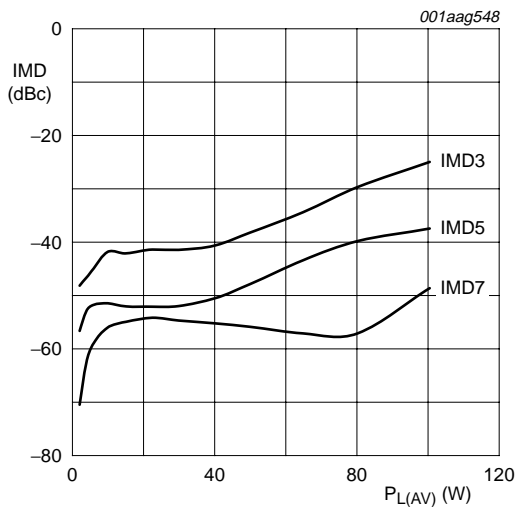
$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 900\text{ mA}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ;  
 $f = 894\text{ MHz}$ .

**Fig 1. One-tone CW power gain and drain efficiency as functions of load power; typical values**



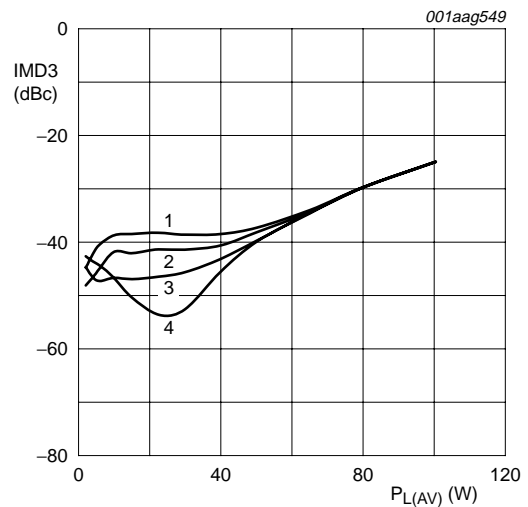
$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 900\text{ mA}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ;  
 $f = 894\text{ MHz}$ .

**Fig 2. Two-tone power gain and drain efficiency as functions of average load power; typical values**



$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 900\text{ mA}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ;  
 $f = 894\text{ MHz}$ .

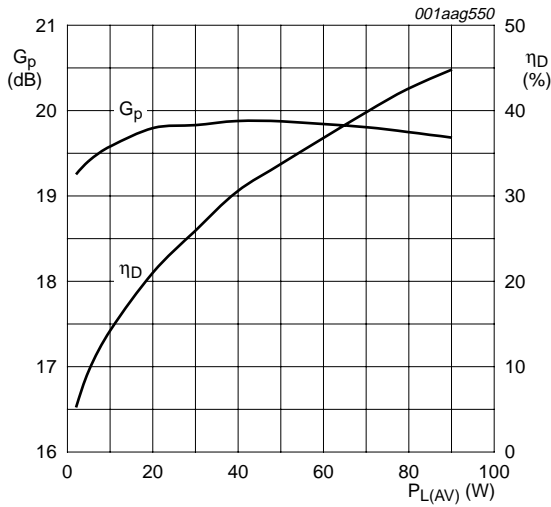
**Fig 3. Intermodulation distortion a function of average load power; typical values**



$V_{DS} = 28\text{ V}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ;  $f = 894\text{ MHz}$ .

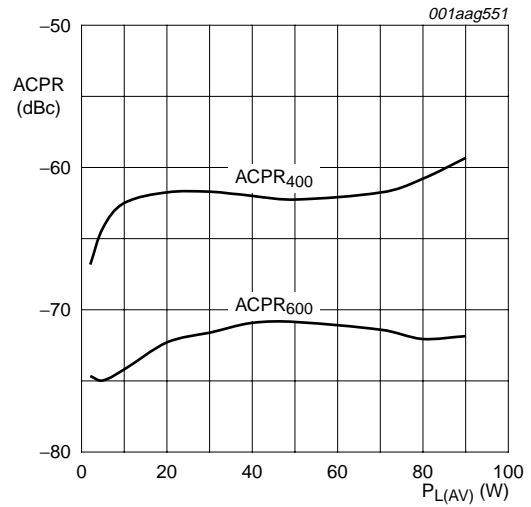
- (1)  $I_{Dq} = 800\text{ mA}$ .
- (2)  $I_{Dq} = 900\text{ mA}$ .
- (3)  $I_{Dq} = 1000\text{ mA}$ .
- (4)  $I_{Dq} = 1100\text{ mA}$ .

**Fig 4. IMD3 as a function of average load power; typical values**



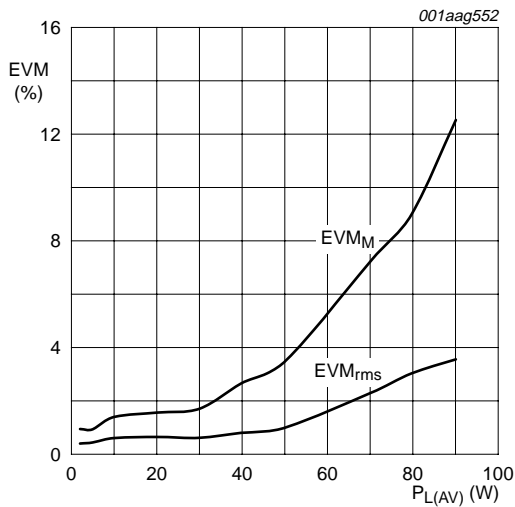
$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 900\text{ mA}$ ;  $T_{case} = 25\text{ }^\circ\text{C}$ ;  
 $f = 894\text{ MHz}$ .

Fig 5. GSM EDGE power gain and drain efficiency as functions of average load power; typical values



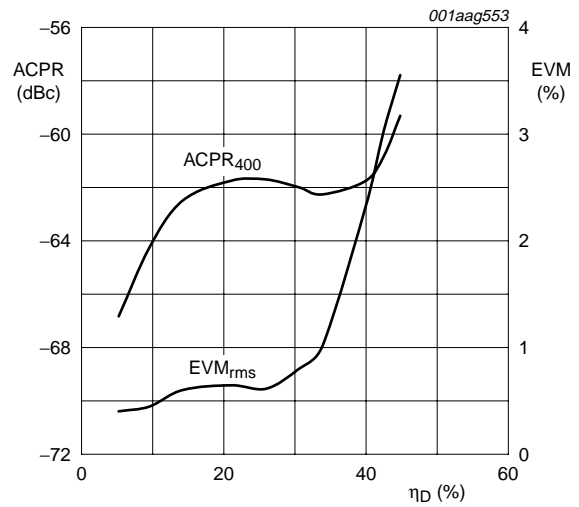
$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 900\text{ mA}$ ;  $T_{case} = 25\text{ }^\circ\text{C}$ ;  
 $f = 894\text{ MHz}$ .

Fig 6. GSM EDGE ACPR at 400 kHz and at 600 kHz as a function of average load power; typical values



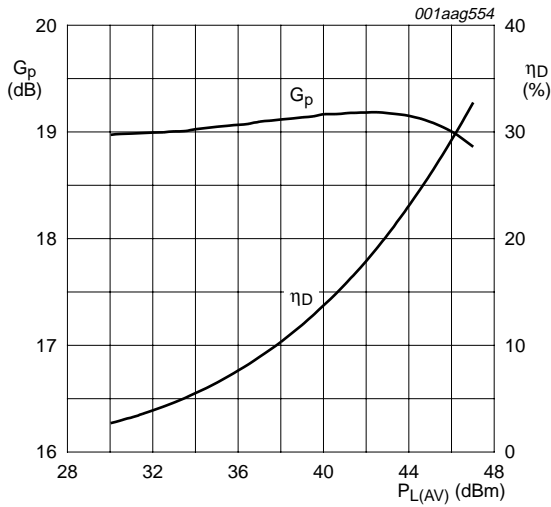
$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 900\text{ mA}$ ;  $T_{case} = 25\text{ }^\circ\text{C}$ ;  
 $f = 894\text{ MHz}$ .

Fig 7. GSM EDGE rms EVM and peak EVM as functions of average load power; typical values



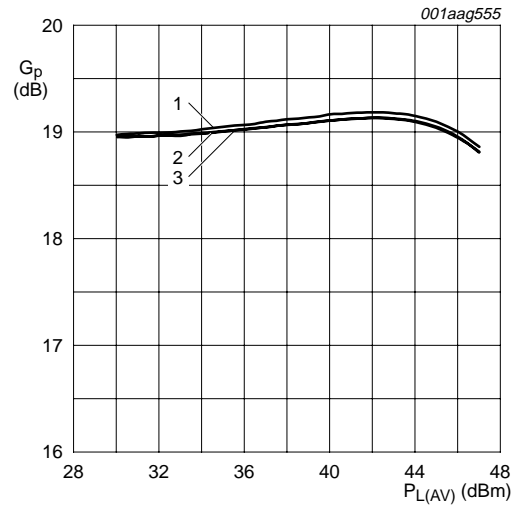
$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 900\text{ mA}$ ;  $T_{case} = 25\text{ }^\circ\text{C}$ ;  
 $f = 894\text{ MHz}$ .

Fig 8. GSM EDGE ACPR and rms EVM as functions of drain efficiency; typical values



$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 1100\text{ mA}$ ;  $f = 881.5\text{ MHz}$ .  
 Test signal: IS-95 with PAR = 9.9 dB at 0.01 % probability.

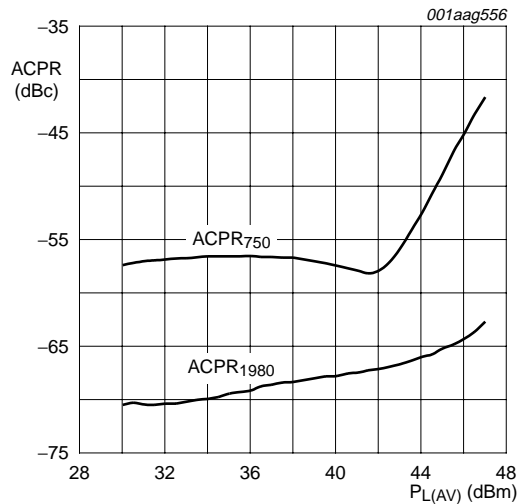
**Fig 9. CDMA power gain and drain efficiency as functions of average load power; typical values, measured in a CDMA demo test circuit**



$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 1100\text{ mA}$ .

- (1)  $f = 869\text{ MHz}$ .
- (2)  $f = 881.5\text{ MHz}$ .
- (3)  $f = 894\text{ MHz}$ .

**Fig 10. CDMA power gain as a function of average load power at various frequencies; typical values, measured in a CDMA demo test circuit**



$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 1100\text{ mA}$ ;  $T_{case} = 25\text{ }^\circ\text{C}$ ;  $f = 881.5\text{ MHz}$ .

**Fig 11. CDMA ACPR at 750 kHz and at 1980 kHz as functions of average load power; typical values, measured in a CDMA demo test circuit**

**8. Test information**

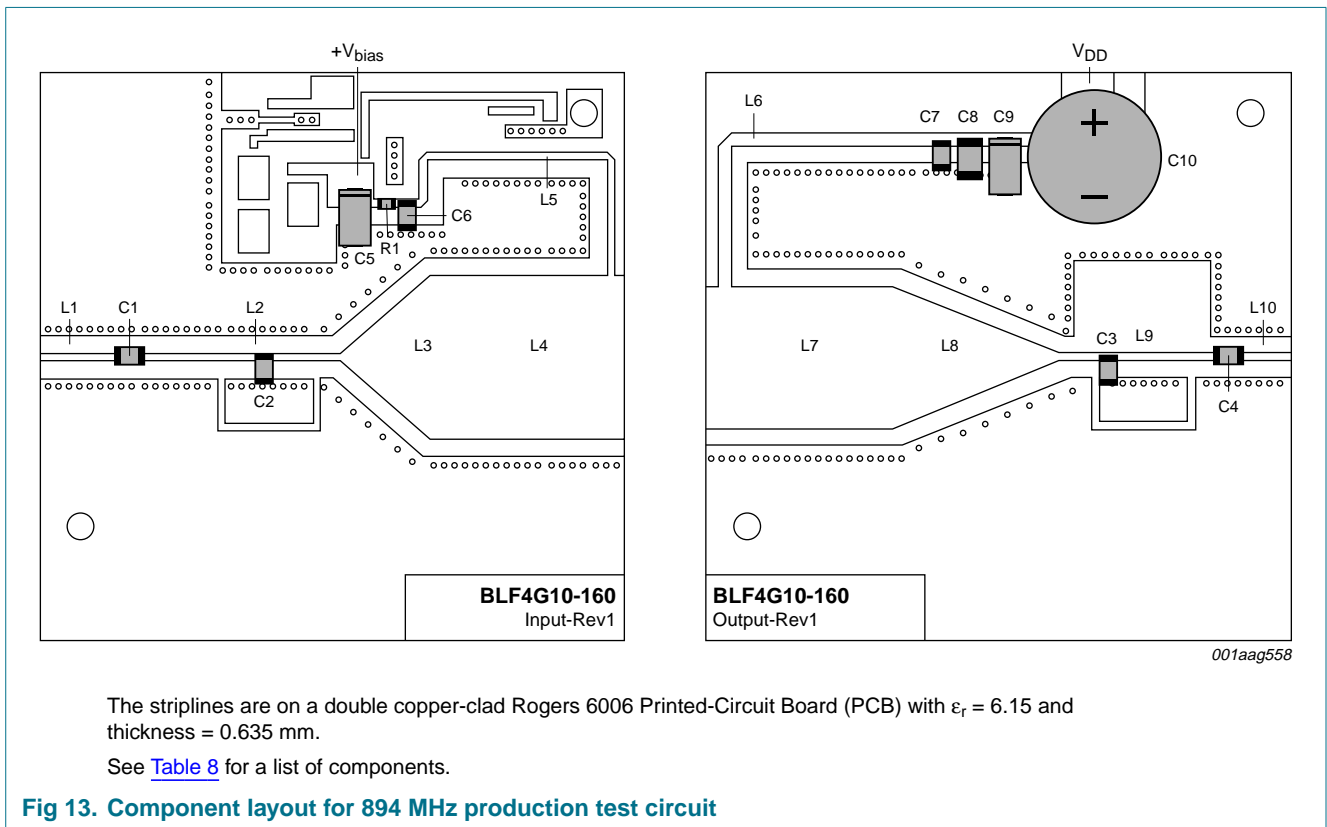
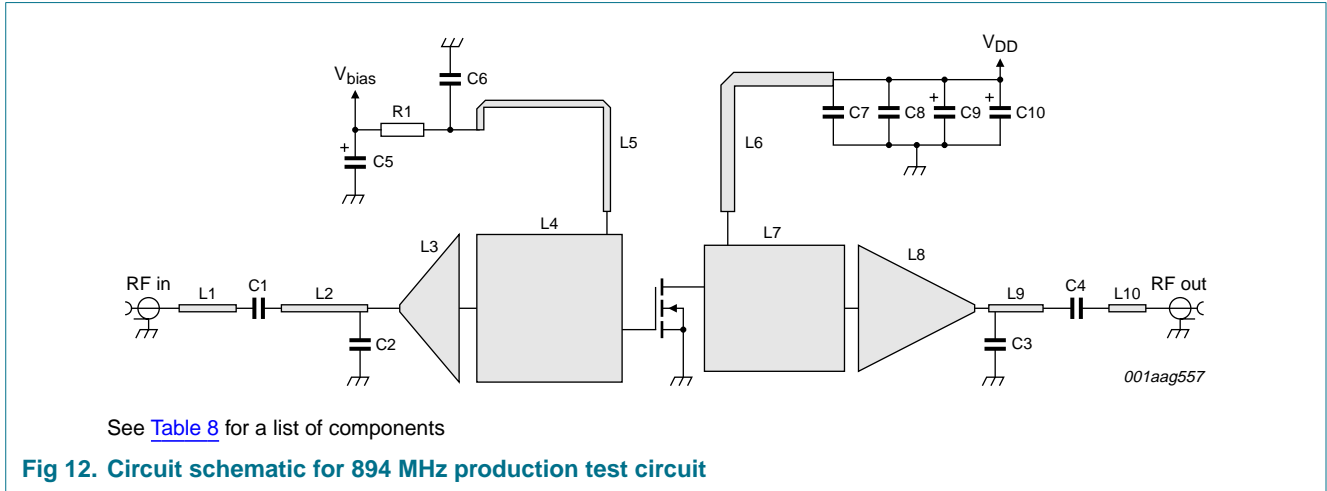


Table 8. List of components (see Figure 12 and Figure 13).

Component	Description	Value	Remarks
C1, C4, C6, C7	multilayer ceramic chip capacitor	68 pF	[1]
C2	multilayer ceramic chip capacitor	1.5 pF	[1]
C3	multilayer ceramic chip capacitor	1.4 pF	[1]
C5, C9	tantalum capacitor	10 $\mu$ F	
C8	ceramic capacitor	1 $\mu$ F	1812X7R105KL2AB
C10	electrolytic capacitor	220 $\mu$ F	
L1	stripline	-	[2] (W $\times$ L) 0.914 mm $\times$ 10.160 mm
L2	stripline	-	[2] (W $\times$ L) 0.914 mm $\times$ 24.384 mm
L3	tapered stripline	-	[2] (W1 $\times$ W2 $\times$ L) 0.914 mm $\times$ 19.812 mm $\times$ 11.024 mm
L4	stripline	-	[2] (W $\times$ L) 19.812 mm $\times$ 21.438 mm
L5	stripline	-	[2] (W $\times$ L) 0.914 mm $\times$ 42.342 mm
L6	stripline	-	[2] (W $\times$ L) 1.524 mm $\times$ 42.418 mm
L7	stripline	-	[2] (W $\times$ L) 17.221 mm $\times$ 22.479 mm
L8	tapered stripline	-	[2] (W1 $\times$ W2 $\times$ L) 17.221 mm $\times$ 0.914 mm $\times$ 20.625 mm
L9	stripline	-	[2] (W $\times$ L) 0.914 mm $\times$ 19.126 mm
L10	stripline	-	[2] (W $\times$ L) 0.914 mm $\times$ 6.858 mm
R1	SMD resistor	5.1 $\Omega$	

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] The striplines are on a double copper-clad Rogers 6006 Printed-Circuit Board (PCB) with  $\epsilon_r = 6.15$  and thickness = 0.635 mm.



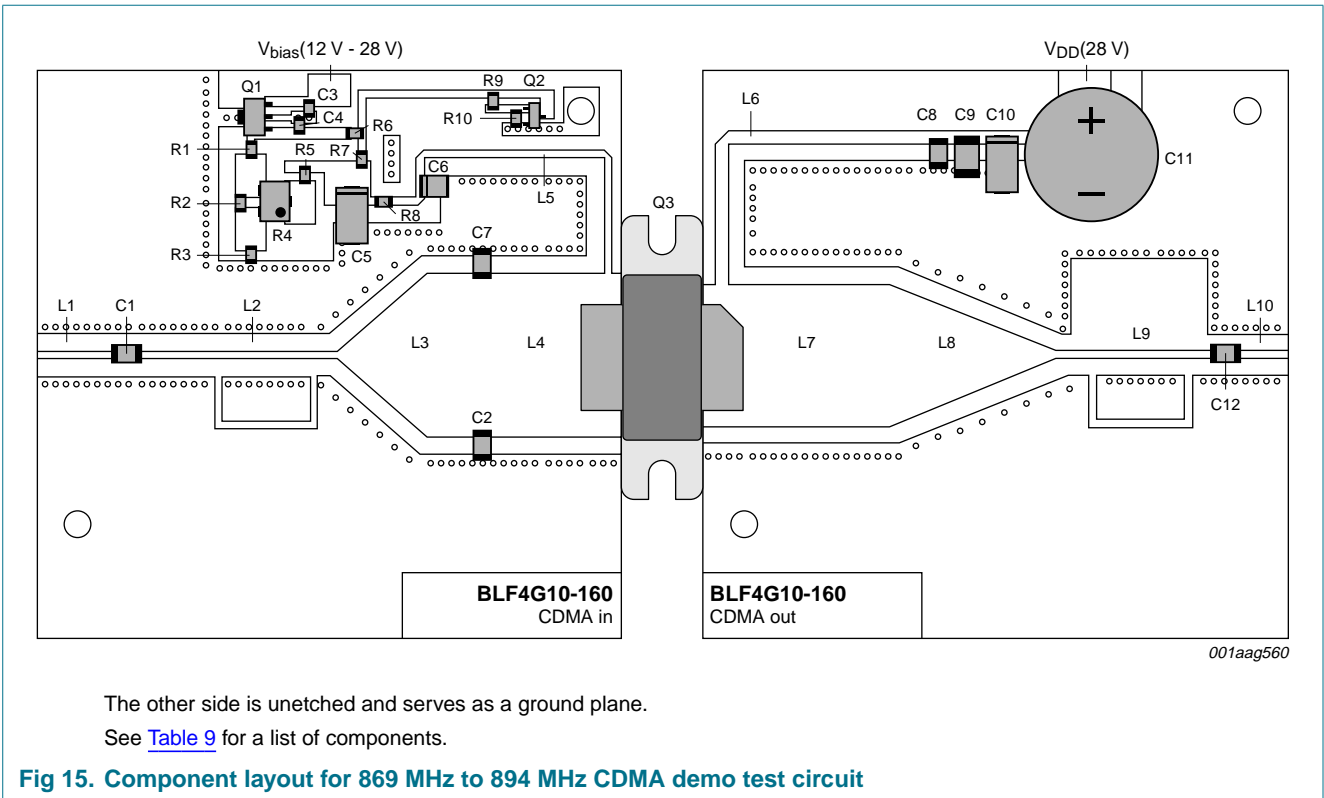
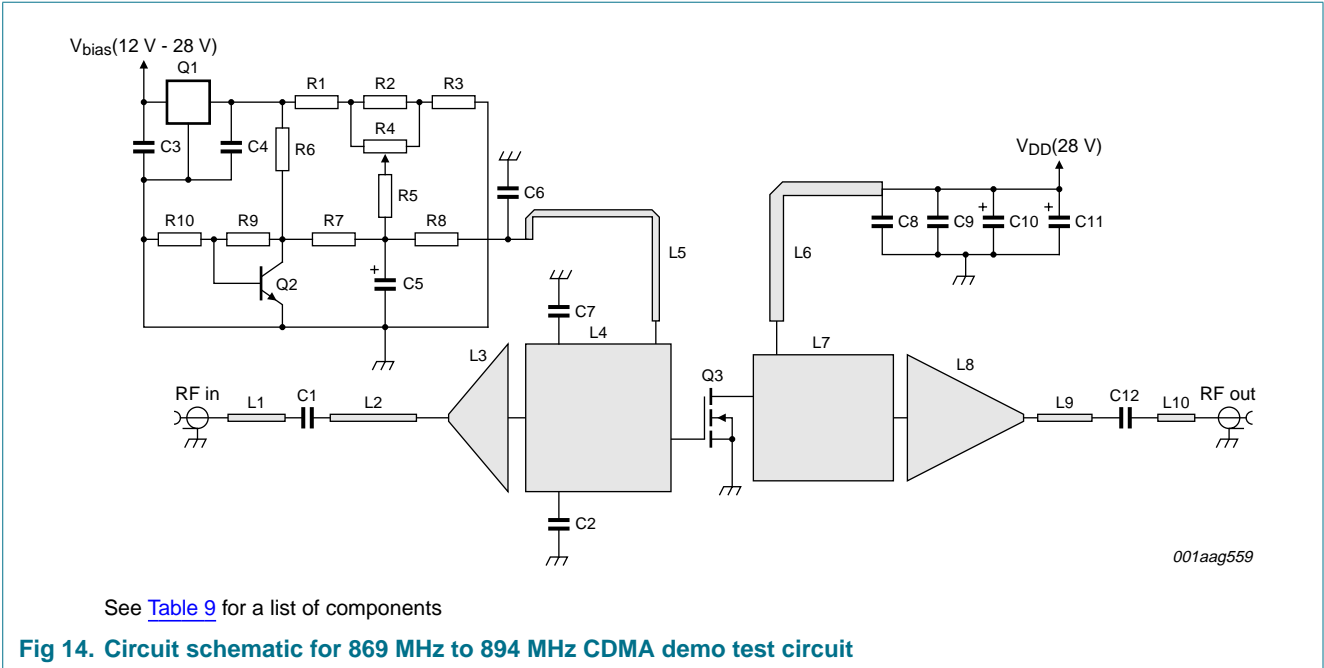


Table 9. List of components (see Figure 14 and Figure 15).

Component	Description	Value	Remarks
C1, C6, C8	multilayer ceramic chip capacitor	68 pF	[1]
C2, C7	multilayer ceramic chip capacitor	1.3 pF	[1]
C3, C4	ceramic capacitor	100 nF	
C5, C10	tantalum capacitor	10 $\mu$ F	
C9	ceramic capacitor	1 $\mu$ F	
C11	electrolytic capacitor	2200 $\mu$ F	
C12	multilayer ceramic chip capacitor	18 pF	[1]
L1	stripline	-	[2] (W $\times$ L) 0.914 mm $\times$ 10.160 mm
L2	stripline	-	[2] (W $\times$ L) 0.914 mm $\times$ 24.384 mm
L3	tapered stripline	-	[2] (W1 $\times$ W2 $\times$ L) 0.914 mm $\times$ 19.812 mm $\times$ 11.024 mm
L4	stripline	-	[2] (W $\times$ L) 19.812 mm $\times$ 21.438 mm
L5	stripline	-	[2] (W $\times$ L) 0.914 mm $\times$ 42.342 mm
L6	stripline	-	[2] (W $\times$ L) 1.524 mm $\times$ 42.418 mm
L7	stripline	-	[2] (W $\times$ L) 17.221 mm $\times$ 22.479 mm
L8	tapered stripline	-	[2] (W1 $\times$ W2 $\times$ L) 17.221 mm $\times$ 0.914 mm $\times$ 20.625 mm
L9	stripline	-	[2] (W $\times$ L) 0.914 mm $\times$ 19.126 mm
L10	stripline	-	[2] (W $\times$ L) 0.914 mm $\times$ 6.858 mm
R1, R2	SMD resistor	430 $\Omega$	
R3	SMD resistor	300 $\Omega$	
R4	potentiometer	200 $\Omega$	
R5	SMD resistor	2 k $\Omega$	
R6	SMD resistor	1.1 k $\Omega$	
R7	SMD resistor	11 k $\Omega$	
R8	SMD resistor	5.1 $\Omega$	
R9	SMD resistor	5.1 k $\Omega$	
R10	SMD resistor	910 $\Omega$	
Q1	voltage regulator	-	78L08
Q2	transistor	-	2N2222
Q3	BLF4G10-160	-	

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] The striplines are on a double copper-clad Rogers 6006 Printed-Circuit Board (PCB) with  $\epsilon_r = 6.15$  and thickness = 0.635 mm.

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A

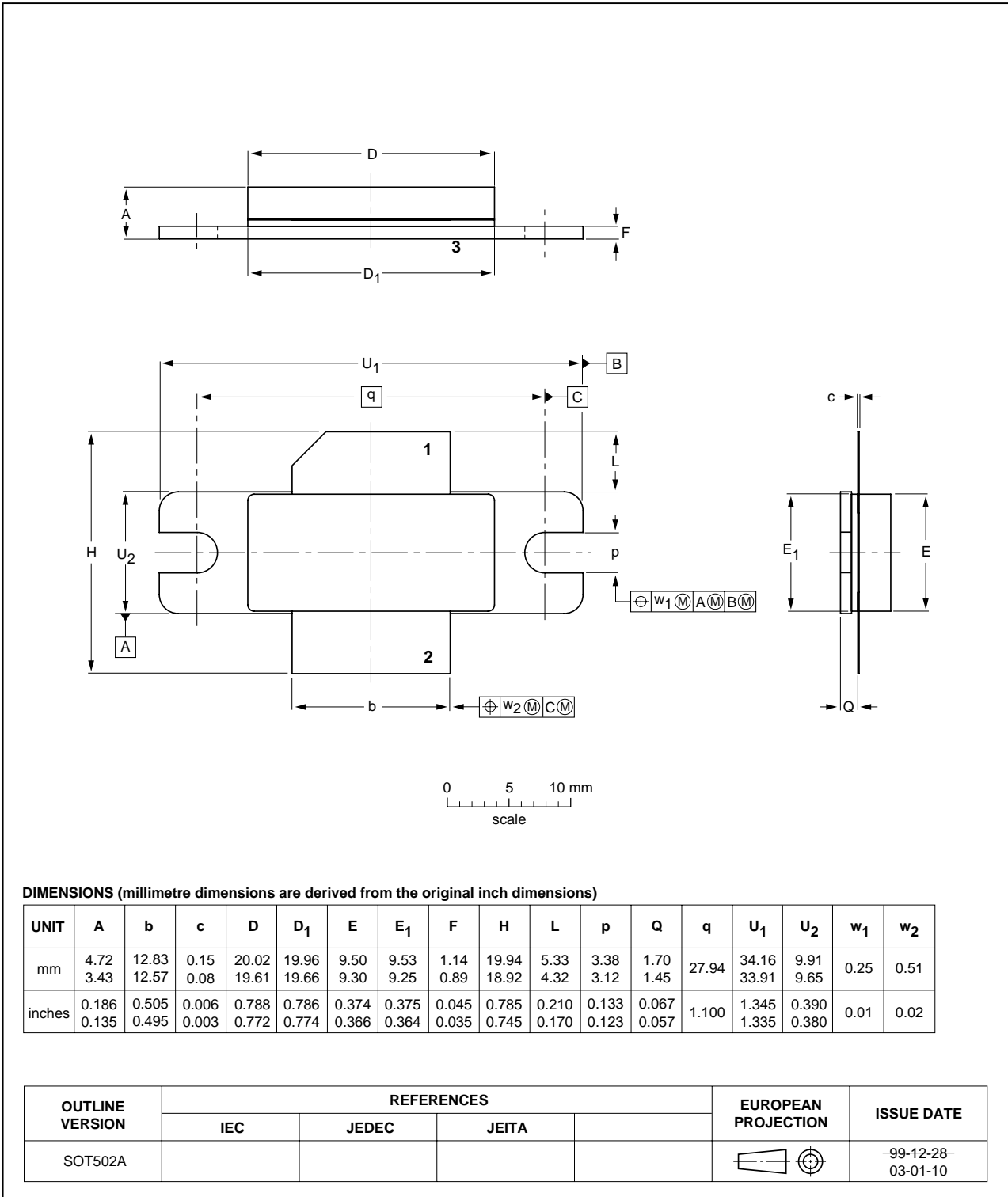


Fig 16. Package outline SOT502A

## 10. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CDMA	Code Division Multiple Access
CW	Continuous Waveform
EDGE	Enhanced Data GSM Environment
EVM	Error Vector Magnitude
GSM	Global System for Mobile communications
IS-95	CDMA Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
RMS	Root Mean Square
SMD	Surface-Mount Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF4G10-160_1	20070622	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 22 June 2007

Document identifier: BLF4G10-160\_1