

DS1689/DS1693

3V/5V Serialized Real-Time Clocks with NV RAM Control

www.maxim-ic.com

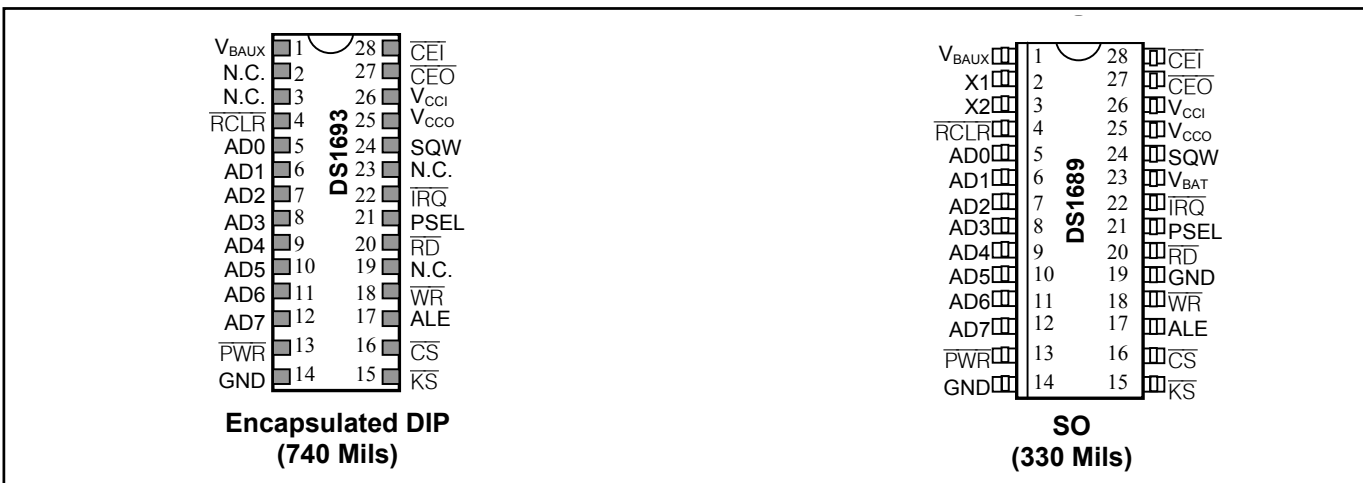
FEATURES

Incorporates Industry Standard DS1287 PC Clock Plus Enhanced Features:

- +3V or +5V Operation
- 64-Bit Silicon Serial Number
- 64-Bit Customer Specific ROM or Additional Serial Number Available
- Power Control Circuitry Supports System Power-On from Date/Time Alarm or Key Closure
- Automatic Battery Backup and Write Protection to External SRAM
- Crystal Select Bit Allows RTC to Operate with 6pF or 12.5pF Crystal
- 114 Bytes User NV RAM
- Auxiliary Battery Input

- RAM Clear Input
- Century Register
- 32kHz Output for Power Management
- 32-Bit V_{CC} Powered Elapsed Time Counter
- 32-Bit V_{BAT} Powered Elapsed Time Counter
- 16-Bit Power Cycle Counter
- Compatible with Existing BIOS for Original DS1287 Functions
- Available as IC (DS1689) or Stand-Alone Module with Embedded Battery and Crystal (DS1693)
- Available in Industrial Temperature Version
- Timekeeping Algorithm Includes Leap Year Compensation Valid Up to 2100

PIN CONFIGURATIONS



ORDERING INFORMATION

PART	TEMP RANGE	VOLTAGE (V)	PIN-PACKAGE	TOP MARK*
DS1689S	0°C to +70°C	3 to 5	28 SO (0.330")	DS1689S
DS1689S+	0°C to +70°C	3 to 5	28 SO (0.330")	DS1689S
DS1689SN	-40°C to +85°C	3 to 5	28 SO (0.330")	DS1689S
DS1689SN+	-40°C to +85°C	3 to 5	28 SO (0.330")	DS1689S
DS1689S/T&R	0°C to +70°C	3 to 5	28 SO (0.330")/Tape & Reel	DS1689S
DS1689S+T&R	0°C to +70°C	3 to 5	28 SO (0.330")/Tape & Reel	DS1689S
DS1689SN/T&R	-40°C to +85°C	3 to 5	28 SO (0.330")/Tape & Reel	DS1689S
DS1689SN+T&R	-40°C to +85°C	3 to 5	28 SO (0.330")/Tape & Reel	DS1689S
DS1693	0°C to +70°C	3 to 5	28 EDIP (0.740")	DS1693

+ Denotes a lead-free/RoHS-compliant device.

* A "+" anywhere on the top mark denotes a lead-free/RoHS-compliant device. An "N" denotes an industrial temperature device.

PIN DESCRIPTION

PIN		NAME	FUNCTION
SO	EDIP		
1	1	V _{BAUX}	Auxiliary Battery Supply. Auxiliary battery input required for kickstart and wake-up features. This input also supports clock/calendar and External NV RAM if V _{BAT} is at lower voltage or is not present. A standard +3V lithium cell or other energy source can be used. Battery voltage must be held between +2.5V and +3.7V for proper operation. If V _{BAUX} is not going to be used it should be grounded and auxiliary battery enable bit bank 1, register 4BH, should = 0.
2, 3	—	X1, X2	Connections for Standard 32.768kHz Quartz Crystal. For greatest accuracy, the DS1689 must be used with a crystal that has a specified load capacitance of either 6pF or 12.5pF. The crystal select (CS) bit in Extended Control Register 4B is used to select operation with a 6pF or 12.5pF crystal. The crystal is attached directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high-impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high-frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, refer to <i>Application Note 58: Crystal Considerations with Dallas Real Time Clocks</i>. The DS1689 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
4	4	$\overline{\text{RCLR}}$	Active-Low RAM Clear Input. If enabled by software, taking $\overline{\text{RCLR}}$ low will result in the clearing of the 114 bytes of user RAM. When enabled, $\overline{\text{RCLR}}$ can be activated whether or not V _{CC} is present.
5–12	5–12	AD0–AD7	Multiplexed Address/Data Bus. Multiplexed buses save pins because address information and data information time-share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1689 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, at which time the DS1689/DS1693 latches the address. Valid write data must be present and held stable during the latter portion of the $\overline{\text{WR}}$ pulse. In a read cycle, the DS1689/DS1693 outputs 8 bits of data during the latter portion of the $\overline{\text{RD}}$ pulse. The read cycle is terminated and the bus returns to a high impedance state as $\overline{\text{RD}}$ transitions high. The address/data bus also serves as a bidirectional data path for the external extended RAM.

PIN		NAME	FUNCTION
SO	EDIP		
13	13	$\overline{\text{PWR}}$	Active-Low Power-On Interrupt Output. The $\overline{\text{PWR}}$ pin is intended for use as an on/off control for the system power. With V_{CC} voltage removed from the DS1689/DS1693, $\overline{\text{PWR}}$ may be automatically activated from a kickstart input via the $\overline{\text{KS}}$ pin or from a wake-up interrupt. Once the system is powered on, the state of $\overline{\text{PWR}}$ can be controlled via bits in the Dallas registers.
14, 19	14	GND	Ground. DC power is provided to the device on this pin.
15	15	$\overline{\text{KS}}$	Active-Low Kickstart Input. When V_{CC} is removed from the DS1689/DS1693, the system can be powered on in response to an active low transition on the $\overline{\text{KS}}$ pin, as might be generated from a key closure. V_{BAUX} must be present and auxiliary battery enable bit (ABE) must be set to 1 if the kickstart function is used, and the $\overline{\text{KS}}$ pin must be pulled up to the V_{BAUX} supply. While V_{CC} is applied, the $\overline{\text{KS}}$ pin can be used as an interrupt input.
16	16	$\overline{\text{CS}}$	Active-Low Chip Select Input. This signal must be asserted low during a bus cycle for the RTC portion of the DS1689/DS1693 to be accessed. $\overline{\text{CS}}$ must be kept in the active state during $\overline{\text{RD}}$ and $\overline{\text{WR}}$ timing. Bus cycles, which take place with ALE asserted but without asserting, $\overline{\text{CS}}$ will latch addresses. However, no data transfer will occur.
17	17	ALE	Address Strobe Input (Active High). A pulse on the address strobe pin serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1689/DS1693.
18	18	$\overline{\text{WR}}$	Active-Low Write Data Strobe. The $\overline{\text{WR}}$ signal is an active low signal. The $\overline{\text{WR}}$ signal defines the time period during which data is written to the addressed register.
20	20	$\overline{\text{RD}}$	Active-Low Read Data Strobe. $\overline{\text{RD}}$ identifies the time period when the DS1689/DS1693 drives the bus with RTC read data. The $\overline{\text{RD}}$ signal is an enable signal for the output buffers of the clock.
21	21	PSEL	+3V or +5V Power Select. When PSEL is logic 1, 5V operation is selected. When PSEL is logic 0 or is floated, the device is in autosense mode and determines the correct mode of operation based on the voltage on V_{CCI} .
22	22	$\overline{\text{IRQ}}$	Active-Low Interrupt Request Output (Open Drain). The $\overline{\text{IRQ}}$ pin is an active-low output of the DS1689/DS1693 that can be tied to the interrupt input of a processor. The $\overline{\text{IRQ}}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{\text{IRQ}}$ pin, the application software must clear all enabled flag bits contributing to $\overline{\text{IRQ}}$'s active state. When no interrupt conditions are present, the $\overline{\text{IRQ}}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{\text{IRQ}}$ bus. The $\overline{\text{IRQ}}$ pin is an open-drain output and requires an external pullup resistor.
23	—	V_{BAT}	Battery Input for Any Standard 3V Lithium Cell or Other Energy Source. Battery voltage must be held between 2.5V and 3.7V for proper operation.

PIN		NAME	FUNCTION
SO	EDIP		
24	24	SQW	Square-Wave Output. The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in Register B. A 32kHz SQW signal is output when SQWE = 1, the Enable 32kHz (E32K) bit in extended register 04BH is logic 1, and V_{CC} is above V_{PF} . A 32kHz square wave is also available when V_{CC} is less than V_{PF} if E32K = 1, ABE = 1, and voltage is applied to V_{BAUX} .
25	25	V_{CCO}	External SRAM Power-Supply Output. This pin is internally connected to V_{CCI} when V_{CCI} is within nominal limits. However, during power fail, V_{CCO} is internally connected to the V_{BAT} or V_{BAUX} (whichever is larger). For 5V operation, switchover from V_{CCI} to the backup supply occurs when V_{CCI} drops below the larger of V_{BAT} and V_{BAUX} . For 3V operation, switchover from V_{CCI} to the backup supply occurs at V_{PF} if V_{PF} is less than V_{BAT} and V_{BAUX} . If V_{PF} is greater than V_{BAT} and V_{BAUX} , the switch from V_{CCI} to the backup supply occurs when V_{CCI} drops below the larger of V_{BAT} and V_{BAUX} .
26	26	V_{CCI}	+3V or +5V Main Supply. DC power is provided to the device on these pins. 5V operation is selected when the PSEL pin is at logic 1. If PSEL is floated or at logic 0, the device is in autosense mode and determines the correct operating voltage based on the V_{CCI} voltage level.
27	27	$\overline{CEO}$	Active-Low RAM Chip Enable Output. When power is valid, $\overline{CEO}$ will equal $\overline{CEI}$. When power is not valid, $\overline{CEO}$ will be driven high regardless of $\overline{CEI}$.
28	28	$\overline{CEI}$	Active-Low RAM Chip Enable Input. $\overline{CEI}$ should be driven low to enable the external RAM.
—	2, 3, 19, 23	N.C.	No Connection

DETAILED DESCRIPTION

The DS1689/DS1693 are real-time clocks (RTCs) designed as successors to the industry standard DS1285, DS1385, DS1485, and DS1585 PC real-time clocks. These devices provide the industry standard DS1285 clock function with the new feature of either +3.0V or +5.0V operation and automatic backup and write protection to an external SRAM. The DS1689 also incorporates a number of enhanced features including a silicon serial number, power-on/off control circuitry, and 114 bytes of user NV SRAM, power-on elapsed timer, and power-cycle counter.

Each DS1689/DS1693 is individually manufactured with a unique 64-bit serial number as well as an additional 64-bit customer specific ROM or serial number. The serial number is programmed and tested at Dallas to ensure that no two devices are alike. The serial number can be used to electronically identify a system for purposes such as establishment of a network node address or for maintenance tracking. Customers can reserve blocks of available numbers from Dallas Semiconductor.

The serialized RTCs also incorporate power control circuitry, which allows the system to be powered on via an external stimulus, such as a keyboard or by a time and date (wake-up) alarm. The $\overline{\text{PWR}}$ output pin can be triggered by one or either of these events, and can be used to turn on an external power supply. The $\overline{\text{PWR}}$ pin is under software control, so that when a task is complete, the system power can then be shut down.

The DS1689/DS1693 incorporate a power-on elapsed time counter, a power-on cycle counter, and a battery powered continuous counter. These three counters provide valuable information for maintenance and warranty requirements.

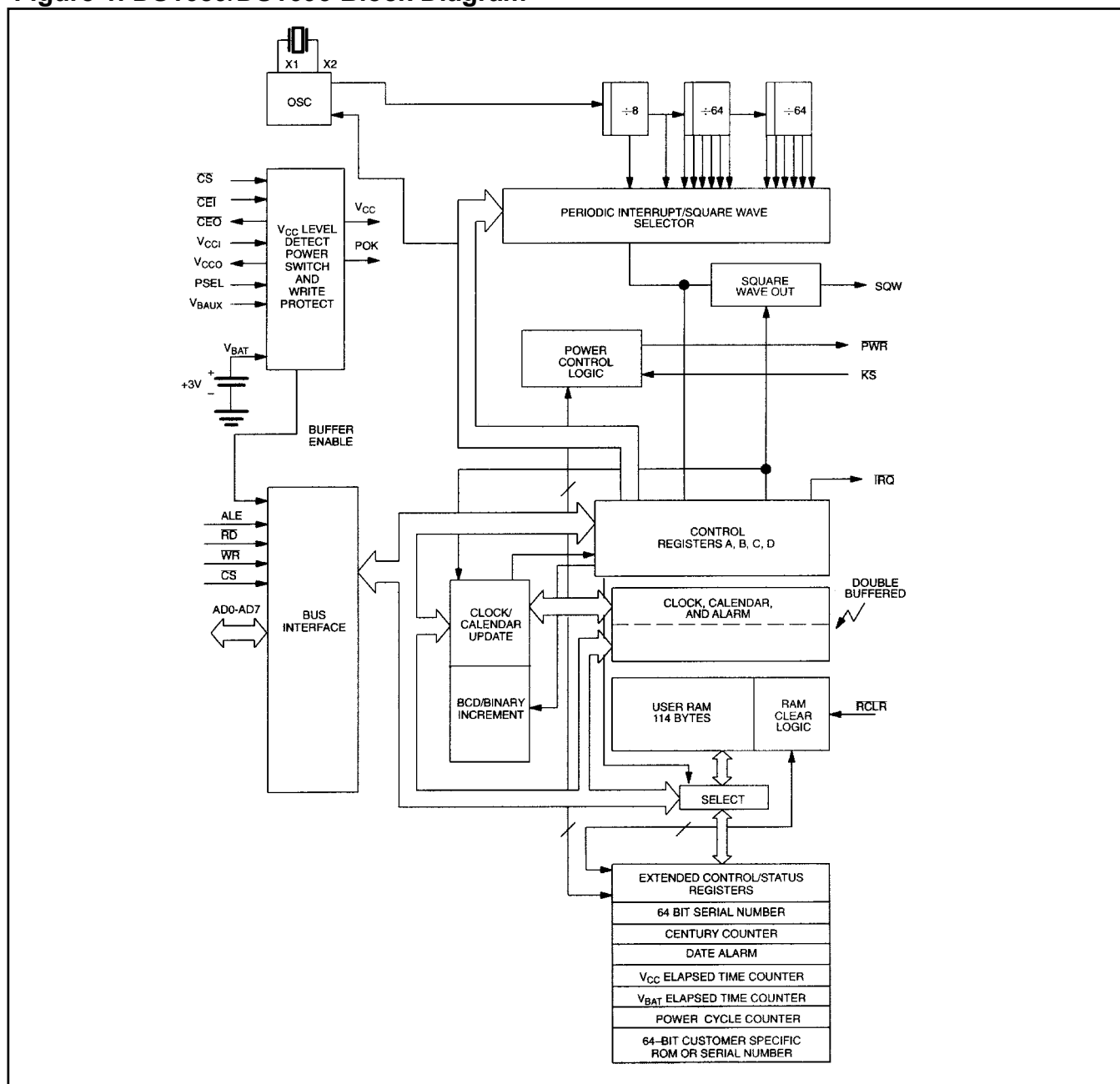
Automatic backup and write protection for an external SRAM is provided through the V_{CCO} and $\overline{\text{CEO}}$ pins. The lithium energy source used to permanently power the real time clock is also used to retain RAM data in the absence of V_{CC} power through the V_{CCO} pin. The chip enable output to RAM ($\overline{\text{CEO}}$) is controlled during power transients to prevent data corruption.

The DS1689 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. The DS1693 incorporates the DS1689 chip, a 32.768kHz crystal, and a lithium battery in a complete, self-contained timekeeping module. The entire unit is fully tested at Dallas Semiconductor such that a minimum of 10 years of timekeeping and data retention in the absence of V_{CC} is guaranteed.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1689/DS1693. The following paragraphs describe the function of each pin.

Figure 1. DS1689/DS1693 Block Diagram



POWER-DOWN/POWER-UP CONSIDERATIONS

The real-time clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CCI} input. When V_{CCI} is applied to the DS1689/DS1693 and reaches a level of greater than V_{PF} (power fail trip point), the device becomes accessible after t_{REC} , provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied.

When PSEL is floating or logic 0, the DS1689 is in autosense mode and 3V or 5V operation is determined based on the voltage on V_{CCI} . Selection of 5V operation is automatically invoked when V_{CCI} rises above 4.5V for a minimum of t_{REC} . However, 3V operation is automatically selected if V_{CCI} does not rise above the level of 4.25V. Selection of the power supply input levels requires 150ms of input stability before operation can commence.

When 5V operation is selected, the device is fully accessible and data can be written and read only when V_{CCI} is greater than 4.5V. When V_{CCI} is below 4.5V, read and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below the greater of V_{BAT} and V_{BAUX} , the RAM and timekeeper are switched over to a lithium battery connected either to the V_{BAT} pin or V_{BAUX} pin.

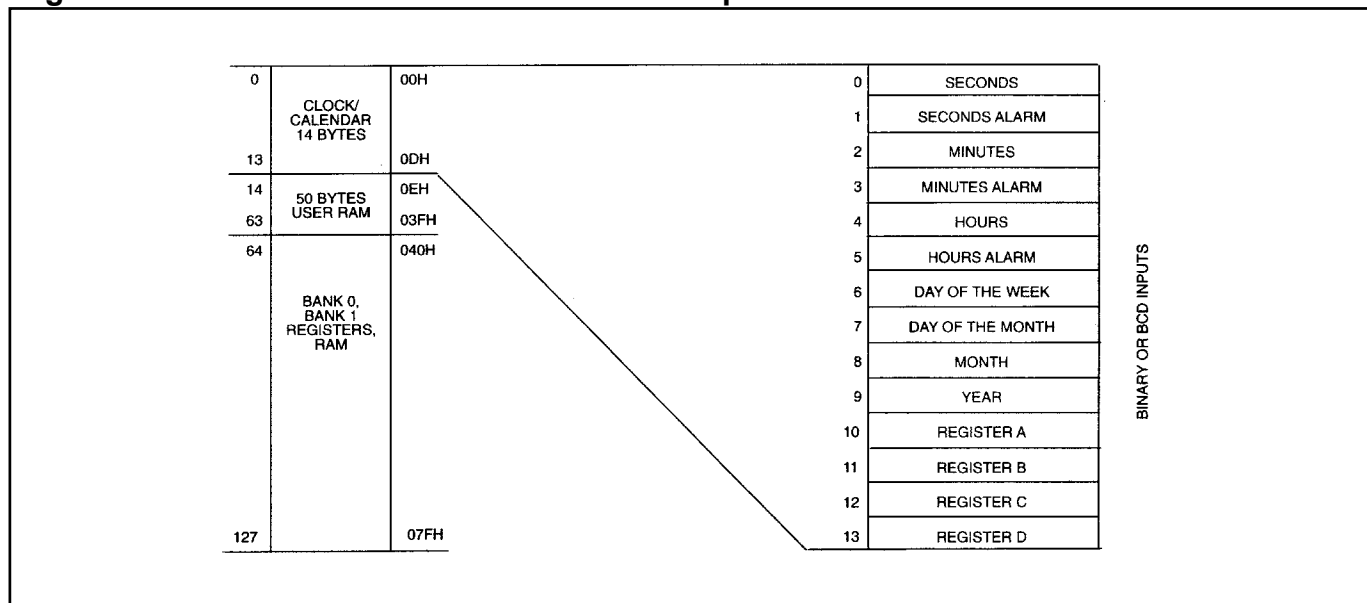
When 3V operation is selected and applied within normal limits, the device is fully accessible and data can be written or read. When V_{CCI} falls below V_{PF} , access to the device is inhibited. If V_{PF} is less than V_{BAT} and V_{BAUX} , the power supply is switched from V_{CCI} to the backup supply (the greater of V_{BAT} and V_{BAUX}) when V_{CCI} drops below V_{PF} . If V_{PF} is greater than V_{BAT} and V_{BAUX} , the power supply is switched from V_{CCI} to the backup supply when V_{CCI} drops below the larger of V_{BAT} and V_{BAUX} .

When V_{CC} falls below V_{PF} , the chip is write-protected. With the possible exception of the $\overline{KS}$, $\overline{PWR}$, and SQW pins, all inputs are ignored and all outputs are in a high impedance state.

RTC ADDRESS MAP

The address map for the RTC registers of the DS1689/DS1693 is shown in Figure 2. The address map consists of the 14-clock/calendar registers. Ten registers contain the time, calendar, and alarm data, and four bytes are used for control and status. All registers can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

Figure 2. DS1689 Real-Time Clock Address Map

TIME, CALENDAR, AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations that reside in both bank 0 and in bank 1, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching will be explained later in this text).

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic 1 to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD) should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the 10 data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic 1. The time, calendar, and alarm bytes are always accessible because they are double-buffered. Once per second the 10 bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The four alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a “don’t care” state in one or more of the four alarm bytes. The “don’t care” code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the “don’t care” condition when at logic 1. An alarm will be generated each hour when the “don’t care” bits are set in the hours byte. Similarly, an alarm is generated every

minute with “don’t care” codes in the hours and minute alarm bytes. The “don’t care” codes in all three alarm bytes create an interrupt every second. The three alarm bytes may be used in conjunction with the date alarm as described in the *Wakeup/Kickstart* section. The century counter will be discussed later in this text.

Table 1. Time, Calendar, and Alarm Data Modes

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
00H	Seconds	0-59	00-3B	00-59
01H	Seconds Alarm	0-59	00-3B	00-59
02H	Minutes	0-59	00-3B	00-59
03H	Minutes Alarm	0-59	00-3B	00-59
04H	Hours 12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours 24-hr Mode	0-23	00-17	00-23
05H	Hours Alarm 12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours Alarm 24-hr Mode	0-23	00-17	00-23
06H	Day of Week Sunday=1	1-7	01-07	01-07
07H	Date of Month	1-31	01-1F	01-31
08H	Month	1-12	01-0C	01-12
09H	Year	0-99	00-63	00-99
BANK1, 48H	Century	0-99	00-63	00-99
BANK 1, 49H	Date Alarm	1-31	01-1F	01-31

CONTROL REGISTERS

The four control registers; A, B, C, and D reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

NONVOLATILE RAM—RTC

The 114 general-purpose nonvolatile RAM bytes are not dedicated to any special function within the DS1689/DS1693. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible when bank 0 is selected.

INTERRUPT CONTROL

The DS1689/DS1693 include six separate, fully automatic sources of interrupt for a processor:

1. Alarm interrupt
2. Periodic interrupt
3. Update-ended interrupt
4. Wake-up interrupt
5. Kickstart interrupt
6. RAM clear interrupt

The conditions, which generate each of these independent interrupt conditions, are described in greater detail elsewhere in this data sheet. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, are to be used. A total of 6 bits, including 3 bits in Register B and 3 bits in Extended Register B, enable the interrupts. The extended register locations are described later. Writing logic 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt enable bit prohibits the $\overline{\text{IRQ}}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{\text{IRQ}}$ is immediately set at an active level, even though the event initiating the interrupt condition may have occurred much earlier. As a result, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to a logic 1 in Register C or in Extended Register A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C as they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that bits that are set remain stable throughout the read cycle. All bits which were set are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, 2, or 3 bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The flag bits in Extended Register A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the $\overline{\text{IRQ}}$ line is driven low when an interrupt flag bit is set and its corresponding enable bit is also set. $\overline{\text{IRQ}}$ is held low as long as at least one of the six possible interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is 1 whenever the $\overline{\text{IRQ}}$ pin is being driven low as a result of one of the six possible active sources. Therefore, determination that the DS1689/DS1693 initiated an interrupt is accomplished by reading Register C and finding $\text{IRQF} = 1$. IRQF remains set until all enabled interrupt flag bits are cleared to 0.

SQUARE-WAVE OUTPUT SELECTION

The SQW pin can be programmed to output a variety of frequencies divided down from the 32.768kHz crystal tied to X1 and X2. The square-wave output is enabled and disabled via the SQWE bit in Register B. If the square wave is enabled ($\text{SQWE} = 1$), the output frequency is determined by the settings of the E32K bit in Extended Register B and by the RS3–RS0 bits in Register A. If the $\text{E32K} = 1$, then a 32.768kHz square wave is output on the SQW pin regardless of the settings of RS3–RS0.

If $\text{E32K} = 0$, then the square-wave output frequency is determined by the RS3–RS0 bits. These bits control a 1-of-15 decoder, which selects one of 13 taps that divide the 32.768kHz frequency. The RS3–RS0 bits establish the SQW output frequency as shown in Table 2. In addition, RS3–RS0 bits control the periodic interrupt selection as described below.

If $\text{SQWE} = 1$, $\text{E32K} = 1$, and the auxiliary battery enable bit (ABE, bank 1; register 04BH) is enabled, and voltage is applied to V_{BAUX} , then the 32kHz square-wave output signal is output on the SQW pin in the absence of V_{CC} . This facility is provided to clock external power management circuitry. If any of the above requirements are not met, no square-wave output signal is generated on the SQW pin in the absence of V_{CC} .

A pattern of 01X in the DV2, DV1, and DV0, bits respectively, turns the oscillator on and enables the countdown chain. Note that this is different than the DS1287, which required a pattern of 010 in these bits. DV0 is now a “don’t care” because it is used for selection between register banks 0 and 1. A pattern of 11X turns the oscillator on, but the oscillator’s countdown chain is held in reset, as it was in the DS1287. Any other bit combination for DV2 and DV1 keeps the oscillator off.

PERIODIC INTERRUPT SELECTION

The periodic interrupt causes the $\overline{\text{IRQ}}$ pin to go to an active state from once every 500ms to once every 122 μ s. This function is separate from the alarm interrupt, which can be output from once per second to once per day. The periodic interrupt rate is selected using the same RS3–RS0 bits in Register A, which select the square-wave frequency (Table 2). Changing the bits affects both the square-wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square-wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

The serialized RTC executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to 1, the user copy of the double-buffered time, calendar, alarm and elapsed time byte is frozen and does not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows the time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a “don’t care” code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

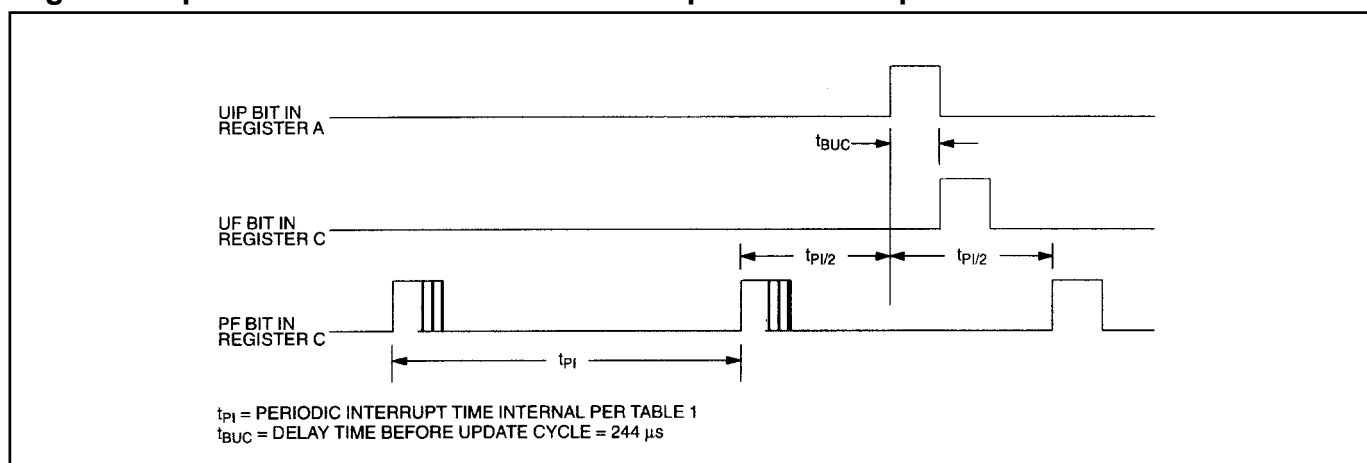
A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 μ s later. If a low is read on the UIP bit, the user has at least 244 μ s before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 μ s.

Table 2. Periodic Interrupt Rate and Square-Wave Output Frequency

EXT. REG. B	SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
E32K	RS3	RS2	RS1	RS0		
0	0	0	0	0	None	None
0	0	0	0	1	3.90625ms	256Hz
0	0	0	1	0	7.8125ms	128Hz
0	0	0	1	1	122.070 μ s	8.192kHz
0	0	1	0	0	244.141 μ s	4.096kHz
0	0	1	0	1	488.281 μ s	2.048kHz
0	0	1	1	0	976.5625 μ s	1.024kHz
0	0	1	1	1	1.953125ms	512Hz
0	1	0	0	0	3.90625ms	256Hz
0	1	0	0	1	7.8125ms	128Hz
0	1	0	1	0	15.625ms	64Hz
0	1	0	1	1	31.25ms	32Hz
0	1	1	0	0	62.5ms	16Hz
0	1	1	0	1	125ms	8Hz
0	1	1	1	0	250ms	4Hz
0	1	1	1	1	500ms	2Hz
1	X	X	X	X	(See Note)	32.768kHz

Note: RS3–RS0 determine periodic interrupt rates as listed for E32K = 0.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within $(t_{PI} / 2 + t_{BUC})$ to ensure that data is not read during the update cycle.

Figure 3. Update-Ended and Periodic Interrupt Relationship

REGISTER A

MSB

LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

Bit 7: UIP (Update In Progress). This bit is a status flag that can be monitored. When the UIP bit is 1, the update transfer will soon occur. When UIP is 0, the update transfer will not occur for at least 244ms. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is 0. The UIP bit is read-only. Writing the SET bit in Register B to 1 inhibits any update transfer and clears the UIP status bit.

Bits 6, 5, 4: DV0, DV1, DV2. These bits are defined as follows:

- DV2 = Countdown Chain
 - 1 - resets countdown chain only if DV1 = 1
 - 0 - countdown chain enabled
- DV1 = Oscillator Enable
 - 0 - oscillator off
 - 1 - oscillator on
- DV0 = Bank Select
 - 0 - original bank
 - 1 - extended registers

A pattern of 01X is the only combination of bits that turn the oscillator on and allow the RTC to keep time. A pattern of 11X enables the oscillator but holds the countdown chain in reset. The next update occurs at 500ms after a pattern of 01X is written to DV2, DV1, and DV0.

Bits 3 to 0: RS3 to RS0 (Rate Selection Bits). These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

- Enable the interrupt with the PIE bit;
- Enable the SQW output pin with the SQWE bit;
- Enable both at the same time and the same rate; or
- Enable neither.

Table 2 lists the periodic interrupt rates and the square-wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB

LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

Bit 7: SET. When the SET bit is 0, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to 1, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1689/DS1693.

Bit 6: PIE (Periodic Interrupt Enable). This bit is a read/write bit that allows the periodic interrupt flag (PF) bit in Register C to drive the $\overline{\text{IRQ}}$ pin low. When the PIE bit is set to 1, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3–RS0 bits of Register A. A 0 in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1689/DS1693 functions.

Bit 5: AIE (Alarm Interrupt Enable). This bit is a read/write bit which, when set to 1, permits the alarm flag (AF) bit in Register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes, including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to 0, the AF bit does not initiate the $\overline{\text{IRQ}}$ signal. The internal functions of the DS1689/DS1693 do not affect the AIE bit.

Bit 4: UIE (Update-Ended Interrupt Enable). This bit is a read/write that enables the update-end flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$. The SET bit going high clears the UIE bit.

Bit 3: SQWE (Square-Wave Enable). When this bit is set to 1, a square-wave signal at the frequency set by the rate-selection bits RS3–RS0 and the E32K bit is driven out on the SQW pin. When the SQWE bit is set to 0, the SQW pin is held low. SQWE is a read/write bit.

Bit 2: DM (Data Mode). This bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A 1 in DM signifies binary data while a 0 in DM specifies Binary Coded Decimal (BCD) data.

Bit 1: 24/12 (24/12 Control Bit). This bit establishes the format of the hours byte. A 1 indicates the 24-hour mode and a 0 indicates the 12-hour mode. This bit is read/write.

Bit 0: DSE (Daylight Saving Enable). This bit is a read/write bit which enables two special updates when DSE is set to 1. On the first Sunday in April the time increments from 1:59:59 am to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is 0. This bit is not affected by internal functions.

REGISTER C

MSB

LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

Bit 7: IRQF (Interrupt Request Flag). This bit is set to 1 when one or more of the following are true:

$$\begin{array}{ll}
 \text{PF} = \text{PIE} = 1 & \text{WF} = \text{WIE} = 1 \\
 \text{AF} = \text{AIE} = 1 & \text{KF} = \text{KSE} = 1 \\
 \text{UF} = \text{UIE} = 1 & \text{RF} = \text{RIE} = 1
 \end{array}$$

$$\text{i.e., } \text{IRQF} = (\text{PF} \bullet \text{PIE}) + (\text{AF} \bullet \text{AIE}) + (\text{UF} \bullet \text{UIE}) + (\text{WF} \bullet \text{WIE}) + (\text{KF} \bullet \text{KSE}) + (\text{RF} \bullet \text{RIE})$$

Any time the IRQF bit is 1, the $\overline{\text{IRQ}}$ pin is driven low. Flag bits PF, AF, and UF are cleared after Register C is read by the program.

Bit 6: PF (Periodic Interrupt Flag). This bit is a read-only bit that is set to a 1 when an edge is detected on the selected tap of the divider chain. The RS3–RS0 bits establish the periodic rate. PF is set to 1 independent of the state of the PIE bit. When both PF and PIE are 1s, the $\overline{\text{IRQ}}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

Bit 5: AF (Alarm Interrupt Flag). A 1 in the AF bit indicates that the current time has matched the alarm time. If the AIE bit is also 1, the $\overline{\text{IRQ}}$ pin goes low and a 1 appears in the IRQF bit. A read of Register C clears AF.

Bit 4: UF (Update-Ended Interrupt Flag). This bit is set after each update cycle. When the UIE bit is set to 1, the 1 in UF causes the IRQF bit to be 1, which asserts the $\overline{\text{IRQ}}$ pin. UF is cleared by reading Register C.

Bits 3 to 0: Unused. These bits always read 0 and cannot be written.

REGISTER D

MSB

LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

Bit 7: VRT (Valid RAM and Time). This bit indicates the condition of the battery connected to the V_{BAT} pin or the battery connected to V_{BAUX} , whichever is at a higher voltage. This bit is not writable and should always be a 1 when read. If a 0 is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

Bits 6 to 0: Unused. These bits cannot be written and always read 0 when read.

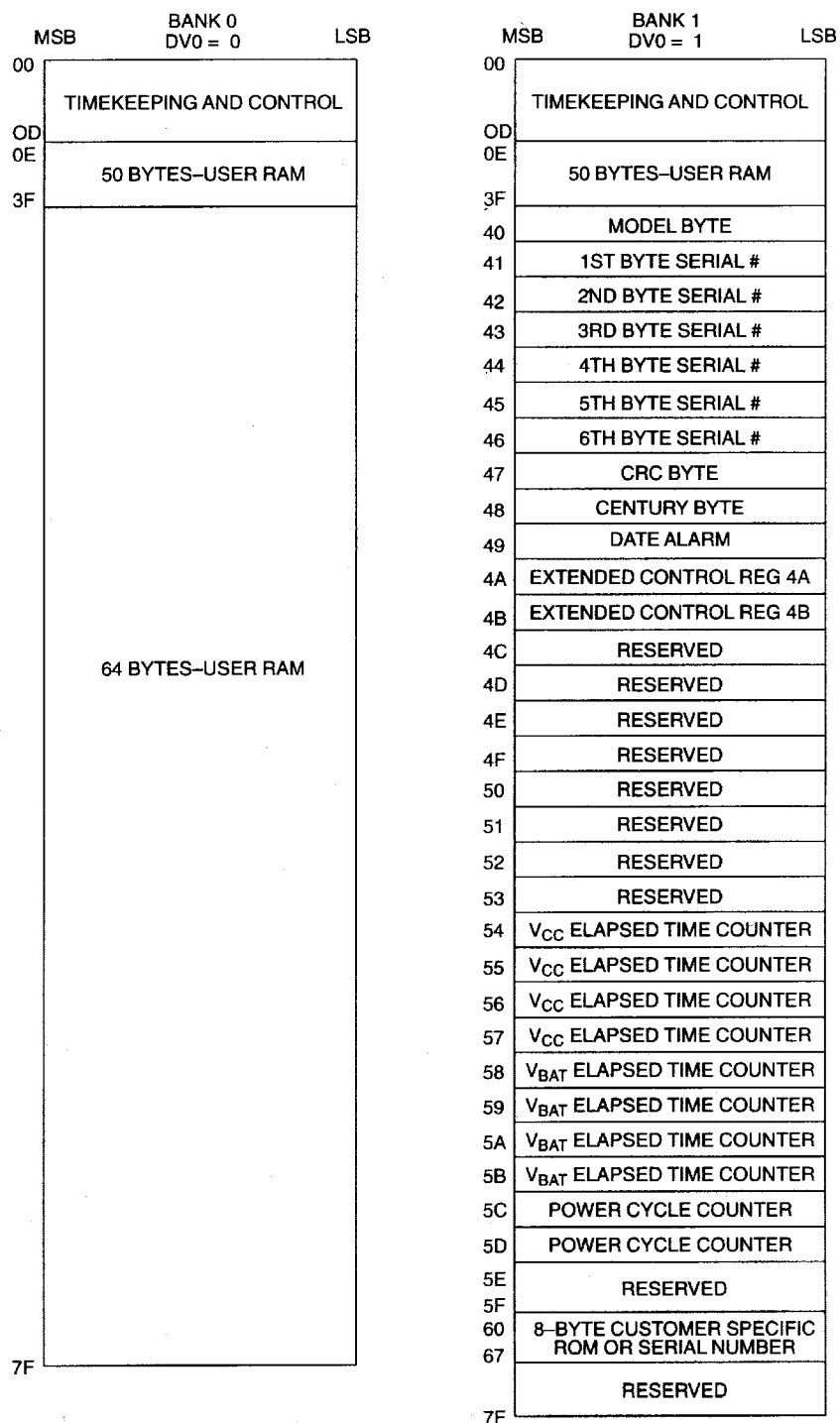
EXTENDED FUNCTIONS

The extended functions provided by the DS1689/DS1693 that are new to the RAMified RTC family are accessed via a software-controlled bank-switching scheme, as illustrated in Figure 4. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1287. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the DS1689/DS1693 clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the Dallas registers which provide control and status for the extended functions will be accessed in place of the additional 64 bytes of user RAM. The major extended functions controlled by the Dallas registers are listed below:

1. Silicon Revision byte
2. Serial Number
3. 8-Byte Customer Specific ROM or Serial Number
4. Century counter
5. Auxiliary Battery Control/Status
6. Wake-Up
7. Kickstart
8. RAM Clear Control/Status
9. V_{CC} Powered Elapsed Time Counter
10. V_{BAT} Powered Elapsed Time Counter
11. Power-on Cycle Counter

The bank selection is controlled by the state of the DV0 bit in Register A. To access bank 0 the DV0 bit should be written to 0. To access bank 1, DV0 should be written to 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Dallas Semiconductor. Bits in these locations cannot be written and return a 0 if read.

Figure 4. DS1689/DS1693 Extended Register Bank Definition

SILICON SERIAL NUMBER/CUSTOMER SPECIFIC ROM

A total of 128 bits are available for use as serial number/ROM. These bits can be used as a 128-bit serial number or as a unique 64-bit serial number and 64-bit customer specific serial number or ROM. The unique 64-bit serial number is located in bank 1 registers 40H–47H. This serial number is divided into three parts. The first byte in register 40H contains a model number to identify the device type and revision of the DS1689/DS1693. Registers 41H–46H contain a unique binary number. Register 47H contains a CRC byte used to validate the data in registers 40H–46H. The method used to create the CRC byte is proprietary to Dallas Semiconductor, but can be made available if required. Typical applications should consider this byte simply as part of the overall unique serial number. All 8 bytes of the serial number are read-only registers.

The DS1689/DS1693 are manufactured such that no two devices contain an identical number in locations 41H–47H. Customers can reserve blocks of numbers for these locations. Contact Dallas Semiconductor for special ordering information for DS1689/DS1693 with reserved blocks of serial numbers.

As already mentioned, another 64 bits are available for use as an additional serial number or customer specific ROM. These 64 bits are located in bank 1 registers 60H–67H.

CENTURY COUNTER

A register has been added in bank 1, location 48H, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

AUXILIARY BATTERY

The V_{BAUX} input is provided to supply power from an auxiliary battery for the DS1689/DS1693 kickstart, wake-up, and SQW output features in the absence of V_{CC} . This power source must be available in order to use these auxiliary features when no V_{CC} is applied to the device.

The auxiliary battery enable (ABE; bank 1, register 04BH) bit in extended Control Register B is used to turn on and off the auxiliary battery for the above functions in the absence of V_{CC} . When set to a 1, V_{BAUX} battery power is enabled, and when cleared to 0, V_{BAUX} battery power is disabled to these functions.

In the DS1689/DS1693, this auxiliary battery can be used as the primary backup power source for maintaining the clock/calendar, user RAM, and extended external RAM functions. This occurs if the V_{BAT} pin is at a lower voltage than V_{BAUX} . If the DS1689 is to be backed up using a single battery with the auxiliary features enabled, then V_{BAUX} should be used and connected to V_{BAT} . If V_{BAUX} is not to be used, it should be grounded and ABE should be cleared to 0.

WAKE-UP/KICKSTART

The DS1689/DS1693 incorporate a wake-up feature, which can power the system on at a predetermined date through activation of the $\overline{PWR}$ output pin. In addition, the kickstart feature can allow the system to be powered-up in response to a low-going transition on the $\overline{KS}$ pin, without operating voltage applied to the V_{CC} pin. As a result, system power can be applied upon such events as a key closure, or modem ring detect signal. To use either the wake-up or the kickstart features, the DS1689/DS1693 must have an auxiliary battery connected to the V_{BAUX} pin, and the oscillator must be running and the countdown chain must not be in reset (Register A DV2, DV1, DV0 = 01X). If DV2, DV1, and DV0 are not in this required state, the $\overline{PWR}$ pin is not driven low in response to a kickstart or wake-up condition, while in battery-backed mode.

The wake-up feature is controlled through the wake-up interrupt enable bit in extended Control Register B (WIE, bank 1, 04BH). Setting WIE to 1 enables the wake-up feature, clearing WIE to 0 disables it. Similarly, the kickstart feature is controlled through the kickstart interrupt enable bit in Extended Control Register B (KSE, bank 1, 04BH).

A wake-up sequence occurs as follows: When wake-up is enabled via $WIE = 1$ while the system is powered down (no V_{CC} voltage), the clock/calendar monitors the current date for a match condition with the date alarm register (bank 1, register 049H). In conjunction with the date alarm register, the hours, minutes, and seconds alarm bytes in the clock/calendar register map (bank 0, registers 05H, 03H, and 01H) are also monitored. As a result, a wake-up occurs at the date and time specified by the date, hours, minutes, and seconds alarm register values. This additional alarm occurs regardless of the programming of the AIE bit (bank 0, register B, 0BH). When the match condition occurs, the $\overline{PWR}$ pin is automatically driven low. This output can be used to turn on the main system power supply, which provides V_{CC} voltage to the DS1689/DS1693 as well as the other major components in the system. Also at this time, the wake-up flag (WF, bank 1, register 04AH) is set, indicating that a wake-up condition has occurred.

A kickstart sequence occurs when kickstarting is enabled via $KSE = 1$. While the system is powered down, the KS input pin is monitored for a low-going transition of minimum pulse width t_{KSPW} . When such a transition is detected, the $\overline{PWR}$ line is pulled low, as it is for a wake-up condition. Also at this time, the kickstart flag (KF, bank 1, register 04AH) is set, indicating that a kickstart condition has occurred.

The timing associated with both the wake-up and kickstarting sequences is illustrated in the *Wake-Up/Kickstart Timing Diagram* in the *Electrical Specifications* section of this data sheet. The timing associated with these functions is divided into 5 intervals, labeled 1–5 on the diagram.

The occurrence of either a kickstart or wake-up condition causes the $\overline{PWR}$ pin to be driven low, as described above. During interval 1, if the supply voltage on the DS1689/DS1693 V_{CC} pin rises above the 3V power-fail level before the power-on timeout period (t_{POTO}) expires, then $\overline{PWR}$ remains at the active low level. If V_{CC} does not rise above the 3V power-fail voltage in this time, then the $\overline{PWR}$ output pin is turned off and returns to its high-impedance level. In this event, the $\overline{IRQ}$ pin also remains tri-stated. The interrupt flag bit (either WF or KF) associated with the attempted power-on sequence remains set until cleared by software during a subsequent system power-on.

If V_{CC} is applied within the timeout period, then the system power-on sequence continues as shown in intervals 2–5 in the timing diagram. During interval 2, $\overline{PWR}$ remains active and $\overline{IRQ}$ is driven to its active low level, indicating that either WF or KF was set in initiating the power-on. In the diagram, $\overline{KS}$ is assumed to be pulled up to the V_{BAUX} supply. Also at this time, the PAB bit is automatically cleared to 0 in response to a successful power-on. The $\overline{PWR}$ line remains active as long as the PAB remains cleared to 0.

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing 0s to both of these control bits. As long as no other interrupt within the DS1689/DS1693 is pending, the $\overline{IRQ}$ line is taken inactive once these bits are reset. Execution of the application software can proceed. During this time, both the wake-up and kickstart functions can be used to generate status and interrupts. WF is set in response to a date, hours, and minutes match condition. KF is set in response to a low-going transition on $\overline{KS}$. If the associated interrupt enable bit is set (WIE and/or KSE), then the $\overline{IRQ}$ line is driven active low in response to enabled event. In addition, the other possible interrupt sources within the DS1689/DS1693 can cause $\overline{IRQ}$ to be driven low. While system power is

applied, the on-chip logic always attempts to drive the $\overline{\text{PWR}}$ pin active in response to the enabled kickstart or wake-up condition. This is true even if $\overline{\text{PWR}}$ was previously inactive as the result of power being applied by some means other than wake-up or kickstart.

The system can be powered down under software control by setting the PAB bit to logic 1. This causes the open-drain $\overline{\text{PWR}}$ pin to be placed in a high-impedance state, as shown at the beginning of interval 4 in the timing diagram. As V_{CC} voltage decays, the $\overline{\text{IRQ}}$ output pin is placed in a high-impedance state when V_{CC} goes below V_{PF} . If the system is to be again powered on in response to a wake-up or kickstart, then both the WF and KF flags should be cleared and WIE and/or KSE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and NV RAM is in effect, $\overline{\text{PWR}}$ and $\overline{\text{IRQ}}$ are tri-stated, and monitoring of wake-up and kickstart takes place.

RAM CLEAR

The DS1689/DS1693 provide a RAM clear function for the 114 bytes of user RAM. When enabled, this function can be performed regardless of the condition of the V_{CC} pin.

The RAM clear function is enabled or disabled via the RAM Clear Enable bit (RCE; bank 1, register 04BH). When this bit is set to logic 1, the 114 bytes of user RAM are cleared (all bits set to 1) when an active-low transition is sensed on the $\overline{\text{RCLR}}$ pin. This action has no effect on either the clock/calendar settings or upon the contents of the external extended RAM. The RAM clear flag (RF, bank 1, register 04BH) is set when the RAM clear operation has been completed. If V_{CC} is present at the time of the RAM clear and $\text{RIE} = 1$, the $\overline{\text{IRQ}}$ line is also driven low upon completion. The interrupt condition can be cleared by writing a 0 to the RF bit. The $\overline{\text{IRQ}}$ line then returns to its inactive high level, provided there are no other pending interrupts. Once the $\overline{\text{RCLR}}$ pin is activated, all read/write accesses are locked out for a minimum recover time, specified as t_{REC} in the *Electrical Characteristics* section.

When RCE is cleared to 0, the RAM clear function is disabled. The state of the $\overline{\text{RCLR}}$ pin has no effect on the contents of the user RAM, and transitions on the $\overline{\text{RCLR}}$ pin have no effect on RF.

EXTENDED CONTROL REGISTERS

Two extended control registers are provided to supply controls and status information for the extended features offered by the DS1689/DS1693. These are designated as extended control registers A and B and are located in register bank 1, locations 04AH and 04BH, respectively. The functions of the bits within these registers are described as follows.

Extended Control Register 4A

MSB				LSB			
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	*	*	PAB	RF	WF	KF

**Reserved bits. These bits are reserved for future use by Dallas Semiconductor. They can be read and written, but have no effect on operation.*

Bit 7: VRT2. This status bit gives the condition of the auxiliary battery. It is set to a logic 1 condition when the external lithium battery is connected to the V_{BAUX} . If this bit is read as logic 0, the external battery should be replaced.

Bit 6: INCR (Increment in Progress Status). This bit is set to 1 when an increment to the time/date registers is in progress and the alarm checks are being made. INCR is set to 1 at 122 μ s before the update cycle starts and is cleared to 0 at the end of each update cycle.

Bit 4: PAB (Power Active Bar Control). When this bit is 0, the $\overline{PWR}$ pin is in the active-low state. The user can write this bit to logic 1 or logic 0. If either [WF and WIE = 1] or [KF and KSE = 1], the PAB bit is cleared to 0.

Bit 2: RF (RAM Clear Flag). This bit is set to logic 1 when a high-to-low transition occurs on the $\overline{RCLR}$ input if RCE = 1. The RF bit is cleared by writing it to logic 0. This bit can also be written to logic 1 to force an interrupt condition.

Bit 1: WF (Wake-Up Alarm Flag). This bit is set to 1 when a wake-up alarm condition occurs or when the user writes it to 1. WF is cleared by writing it to 0.

Bit 0: KF (Kickstart Flag). This bit is set to 1 when a kickstart condition occurs or when the user writes it to 1. This bit is cleared by writing it to logic 0.

Extended Control Register 4B

MSB

LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	E32K	CS	RCE	PRS	RIE	WIE	KSE

Bit 7: ABE (Auxiliary Battery Enable). This bit, when written to logic 1, enables the V_{BAUX} pin for extended functions.

Bit 6: E32K (Enable 32.768kHz Output). This bit, when written to logic 1, enables the 32,768Hz oscillator frequency to be output on the SQW pin provided SQWE = 1.

Bit 5: CS (Crystal Select). When CS is set to 0, the oscillator is configured for operation with a crystal that has a 6pF specified load capacitance. When CS = 1, the oscillator is configured for a 12.5pF crystal.

Bit 4: RCE (RAM Clear Enable). When set to a 1, this bit enables a low level on pin 4 ($\overline{RCLR}$) to clear all 114 bytes of user RAM. When RCE = 0, the RAM clear function is disabled.

Bit 3: PRS (PAB Reset Select). When set to 0 the $\overline{PWR}$ pin is set high impedance when the DS1689 goes into power-fail. When set to 1, the $\overline{PWR}$ pin remains active upon entering power-fail.

Bit 2: RIE (RAM Clear Interrupt Enable). When RIE is set to 1, the $\overline{IRQ}$ pin is driven low when a RAM clear function is completed.

Bit 1: WIE (Wake-Up Alarm Interrupt Enable). When V_{CC} voltage is absent and WIE is set to 1, the $\overline{PWR}$ pin is driven active low when a wake-up condition occurs, causing the WF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin is also driven low. If WIE is set while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ are driven low in response to WF being set to 1. When WIE is cleared to 0, the WF bit has no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

Bit 0: KSE (Kickstart Interrupt Enable). When V_{CC} voltage is absent and KSE is set to 1, the $\overline{PWR}$ pin is driven active low when a kickstart condition occurs ($\overline{KS}$ pulsed low), causing the KF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin is also driven low. If KSE is set to 1 while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ are driven low in response to KF being set to 1. When KSE is cleared to 0, the KF bit has no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

ELAPSED TIME COUNTERS

The DS1689/DS1693 has two 32-bit elapsed time counters, which reside in bank 1 of the RTC registers. To access these counters the DV0 bit in register A must first be set to a logical 1.

The V_{CC} powered elapsed time counter resides in register 54H through 57H. The LSB of this counter resides in register 54 and the MSB is in 57H. The V_{CC} powered elapsed time counter runs only while the V_{CCI} input is within nominal limits. The elapsed time counter is a binary counter that records the number of seconds that have elapsed. The counter can be read or written at the user's discretion. The V_{BAT} -powered elapsed time counter resides in register 58H through 5BH. The LSB of this counter resides in register 58 and the MSB is in 5BH.

The V_{BAT} powered elapsed time counter runs continually as long as the V_{BAT} or V_{BAUX} pin is within nominal limits regardless of the condition of V_{CCI} . The number of seconds that have elapsed is recorded in a binary counter and the counter can be read or written at the user's discretion.

In a typical application, the V_{BAT} -powered elapsed time counter can be used to record the length of time that has elapsed from which the equipment that contains the device was first put into service. The V_{CC} powered counter can then be used to record the length of time that V_{CC} power is applied. These functions can be particularly useful for warranty and maintenance information. In addition, battery life can be predicted based on known loading factors. However, it is worth noting that a properly selected battery should power the DS1689/DS1693 and external RAM for the useful life of most equipment.

POWER-CYCLE COUNTER

The DS1689/DS1693 has a 16-bit power-cycle counter that resides in register 5C and 5D of bank 1. The LSB of this counter resides in 5C and the MSB is in 5D. This binary counter is incremented by one count each time V_{CCI} power is applied within nominal limits. This counter can be read or written at the user's discretion.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground.....	-0.3V to +7.0V
Storage Temperature Range.....	-40°C to +70°C
Soldering Temperature.....	260°C for 10 seconds (See Note 18)
Soldering Temperature (Surface Mount).....	See IPC/JEDEC J-STD-020 Standard

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V _{CC}
Commercial	0°C to +70°C	3V ±10% or 5V ±10%
Industrial	-40°C to 85°C	3V ±10% or 5V ±10%

RECOMMENDED DC OPERATING CONDITIONS

(Over the operating range.)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power-Supply Voltage	5V	V _{CCI}	4.5	5.0	5.5	V	1
	3V	V _{CCI}	2.7	3.0	4.0	V	1
Input Logic 1		V _{IH}	2.2		V _{CC} + 0.3	V	1
Input Logic 0		V _{IL}	-0.3		+0.6	V	1
Battery Voltage		V _{BAT}	2.5		3.7	V	1
Auxiliary Battery Voltage		V _{BAUX}	2.5		3.7	V	1

DC ELECTRICAL CHARACTERISTICS—5V

(Over the operating range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power-Supply Current	I_{CC1}		7	15	mA	2, 3
CMOS Standby Current ($\overline{CS} = V_{CC} - 0.2V$)	I_{CC2}		1	3	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	μA	
$\overline{CEI}$ Input Leakage	$I_{\overline{CEI}}$	-200		+1	μA	15
PSEL Input Leakage	I_{PSEL}	-1		+200	μA	16
Output Leakage Current	I_{OL}	-1		+1	μA	8
Output Logic 1 Voltage ($I_{OUT} = -1.0mA$)	V_{OH}	2.4			V	
Output Logic 0 Voltage ($I_{OUT} = +2.1mA$)	V_{OL}			0.4	V	
Output Voltage	V_{CCO1}	$V_{CC} - 0.3$			V	4
Output Current	I_{CCO1}			85	mA	4
Power-Fail Trip Point	V_{PF}	4.25	4.37	4.5	V	5
Battery Switch Voltage	V_{SW}		$V_{BAT},$ V_{BAUX}		V	
Output Voltage	V_{CCO2}	$V_{BAT} - 0.3$			V	6
Output Current	I_{CCO2}			100	μA	6
Battery Leakage OSC ON	I_{BAT1}		500	1000	nA	
Battery Leakage OSC OFF	I_{BAT2}		50	150	nA	17
I/O Leakage	I_{LO}	-1		+1	μA	7
$\overline{PWR}$ Output at 0.4V	I_{OLPWR}			10.0	mA	1
$\overline{CEI}$ to $\overline{CEO}$ Impedance	Z_{CE}			60	Ω	12

DC ELECTRICAL CHARACTERISTICS—3V

(Over the operating range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power-Supply Current	I_{CC1}		5	10	mA	2, 3
CMOS Standby Current ($\overline{CS} = V_{CC} - 0.2V$)	I_{CC2}		0.5	2	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	μA	
$\overline{CEI}$ Input Leakage	$I_{\overline{CEI}}$	-160		+1	μA	15
PSEL Input Leakage	I_{PSEL}	+1		-160	μA	16
Output Leakage Current	I_{OL}	+160		-1	μA	8
Output Logic 1 Voltage ($I_{OUT} = 0.4mA$)	V_{OH}	2.4			V	
Output Logic 0 Voltage ($I_{OUT} = 0.8mA$)	V_{OL}			0.4	V	
Output Voltage	V_{CCO1}	$V_{CC} - 0.3$			V	4
Output Current	I_{CCO1}			50	mA	4
Power-Fail Trip Point	V_{PF}	2.5	2.6	2.7	V	5
Output Voltage	V_{CCO2}	$V_{BAT} - 0.3$			V	6
Output Current	I_{CCO2}			100	μA	6
Battery Leakage OSC ON	I_{BAT1}		500	1000	nA	
Battery Leakage OSC OFF	I_{BAT2}		50	150	nA	17
I/O Leakage	I_{LO}	-1		+1	μA	7
$\overline{PWR}$ Output at 0.4V	I_{OLPWR}			4	mA	1
$\overline{CEI}$ to $\overline{CEO}$ Impedance	Z_{CE}			120	Ω	12

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	305		DC	ns	
Pulse Width, $\overline{RD}/\overline{WR}$ Low	PW_{RWL}	125			ns	
Pulse Width, $\overline{RD}/\overline{WR}$ High	PW_{RWH}	150			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip-Select Setup Time Before $\overline{WR}$ or $\overline{RD}$	t_{CS}	20			ns	
Chip-Select Hold Time	t_{CH}	0			ns	
Read-Data Hold Time	t_{DHR}	10		80	ns	
Write-Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE Fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse Width, ALE High	PW_{ASH}	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	40			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	9
Data Setup Time	t_{DSW}	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	μs	
$\overline{CEI}$ to $\overline{CEO}$ Delay	t_{CED}			10	ns	

The timing diagram illustrates the relationship between the 68000 microprocessor's control and data signals during a memory access cycle. The signals shown are ALE, $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, and the multiplexed $AD0-AD7$ bus. The diagram is divided into two main sections: a memory write cycle (left) and a memory read cycle (right). Key timing parameters are labeled as follows:

- t_{Cyc} : The duration of one clock cycle.
- PW_{ASH} : Address setup time before the first clock edge.
- t_{ASD} : Address setup time relative to the start of the data bus valid period.
- t_{ASD} : Address setup time relative to the start of the data bus valid period (repeated for $\overline{RD}$).
- PW_{RWH} : $\overline{WR}$ pulse width high.
- PW_{RWL} : $\overline{WR}$ pulse width low.
- t_{CS} : Chip select setup time before the first clock edge.
- t_{DSW} : Data bus setup time before the first clock edge.
- t_{CH} : Chip select hold time after the last clock edge.
- t_{ASL} : Address setup time relative to the start of the data bus valid period (for the second clock edge).
- t_{AHL} : Address hold time relative to the end of the data bus valid period (for the second clock edge).
- t_{DHW} : Data bus hold time after the last clock edge.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	915		DC	ns	
Pulse Width, $\overline{RD}/\overline{WR}$ Low	PW_{RWL}	375			ns	
Pulse Width, $\overline{RD}/\overline{WR}$ High	PW_{RWH}	450			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip-Select Setup Time Before $\overline{WR}$ or $\overline{RD}$	t_{CS}	75			ns	
Chip-Select Hold Time	t_{CH}	0			ns	
Read-Data Hold Time	t_{DHR}	10		120	ns	
Write-Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	90			ns	
Muxed Address Hold Time from ALE Fall	t_{AHL}	30			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	30			ns	
Pulse Width, ALE High	PW_{ASH}	180			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	120			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		370	ns	9
Data Setup Time	t_{DSW}	180			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	μs	
$\overline{CEI}$ to $\overline{CEO}$ Delay	t_{CED}			20	ns	

The timing diagram illustrates the relationship between the 68000 microprocessor and the 68000-000 cache. The signals shown are:

- ALE**: Address Latch Enable. It is active high. t_{ASD} is the setup time before the address is latched, and t_{ASED} is the hold time after the address is latched. PW_{ASH} is the pulse width of the address strobe.
- $\overline{RD}$** : Read control signal. It is active low. PW_{RWH} is the pulse width of the read enable, and PW_{RWL} is the pulse width of the read enable after the address is latched.
- $\overline{WR}$** : Write control signal. It is active low. t_{ASD} is the setup time before the address is latched.
- $\overline{CS}$** : Cache chip select. It is active low. t_{CS} is the setup time before the cache is enabled, and t_{CH} is the hold time after the cache is enabled.
- AD0-AD7**: Data bus. t_{ASL} is the setup time before the data is latched, t_{AHL} is the hold time after the data is latched, t_{DHR} is the data hold time, and t_{JRD} is the data retention time.
- $\overline{iRQ}$** : Interrupt request signal. It is active low.

The diagram also shows the cycle time t_{CYC} and the data bus retention time t_{DDR} .

POWER-UP/POWER-DOWN TIMING—5V(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{\text{CS}}$ High to Power-Fail	t _{PF}			0	ns	
Recovery at Power-Up	t _{REC}		150		ms	
V _{CC} Slew Rate Power-Down	t _F 4.0 ≤ V _{CC} ≤ 4.5V	300			μs	
V _{CC} Slew Rate Power-Down	t _{FB} 3.0 ≤ V _{CC} ≤ 4.0V	10			μs	
V _{CC} Slew Rate Power-Up	t _R 4.5V ≥ V _{CC} ≥ 4.0V	0			μs	
Expected Data Retention	t _{DR}	10			years	13, 14

POWER-UP/POWER-DOWN TIMING—3V(T_A = +25°C)

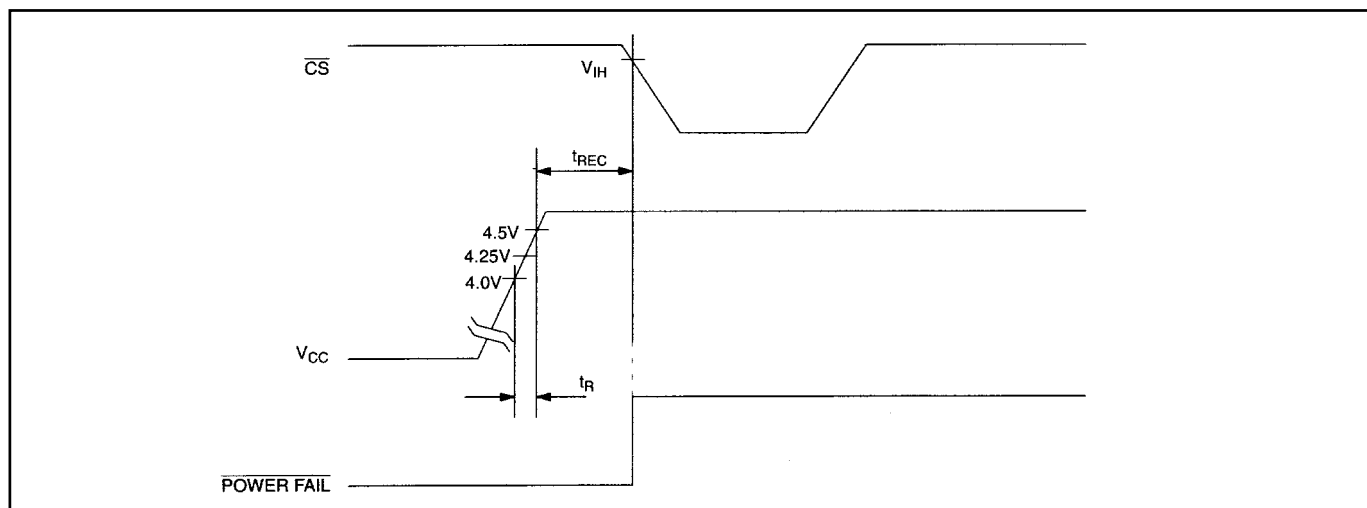
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{\text{CS}}$ High to Power-Fail	t _{PF}			0	ns	
Recovery at Power-Up	t _{REC}		150		ms	
V _{CC} Slew Rate Power-Down	t _F 2.5 ≤ V _{CC} ≤ 3.0V	300			μs	
V _{CC} Slew Rate Power-Up	t _R 3.0V ≥ V _{CC} ≥ 2.5V	0			μs	
Expected Data Retention	t _{DR}	10			years	13, 14

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

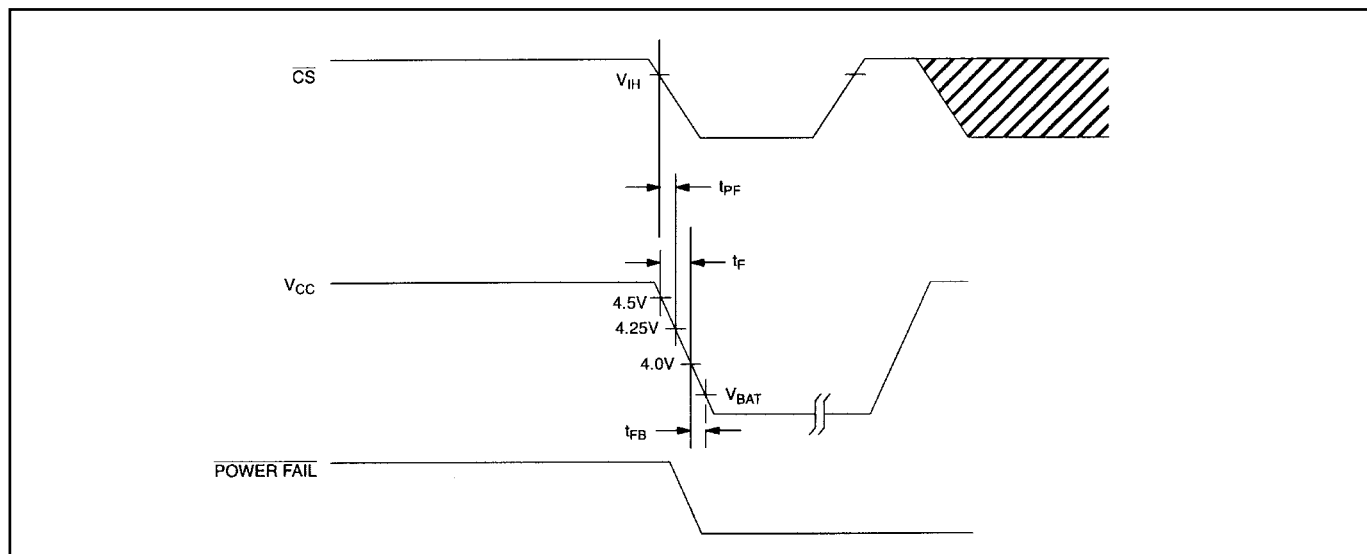
CAPACITANCE(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C _{IN}			12	pF	
Output Capacitance	C _{OUT}			12	pF	

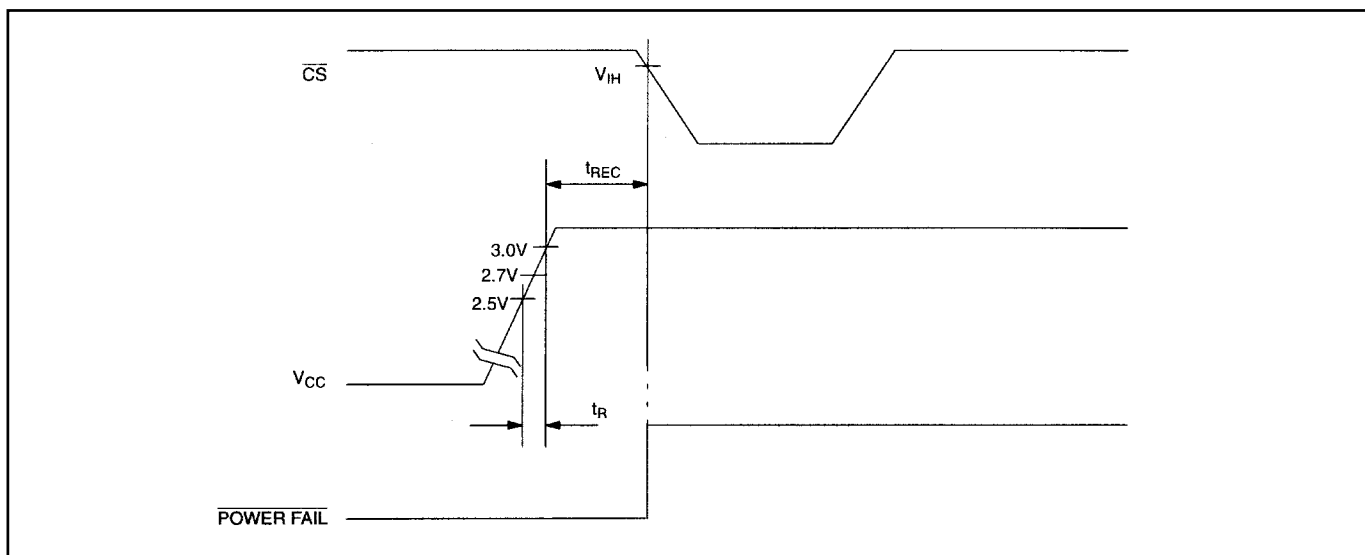
POWER-UP CONDITION—5V OPERATION



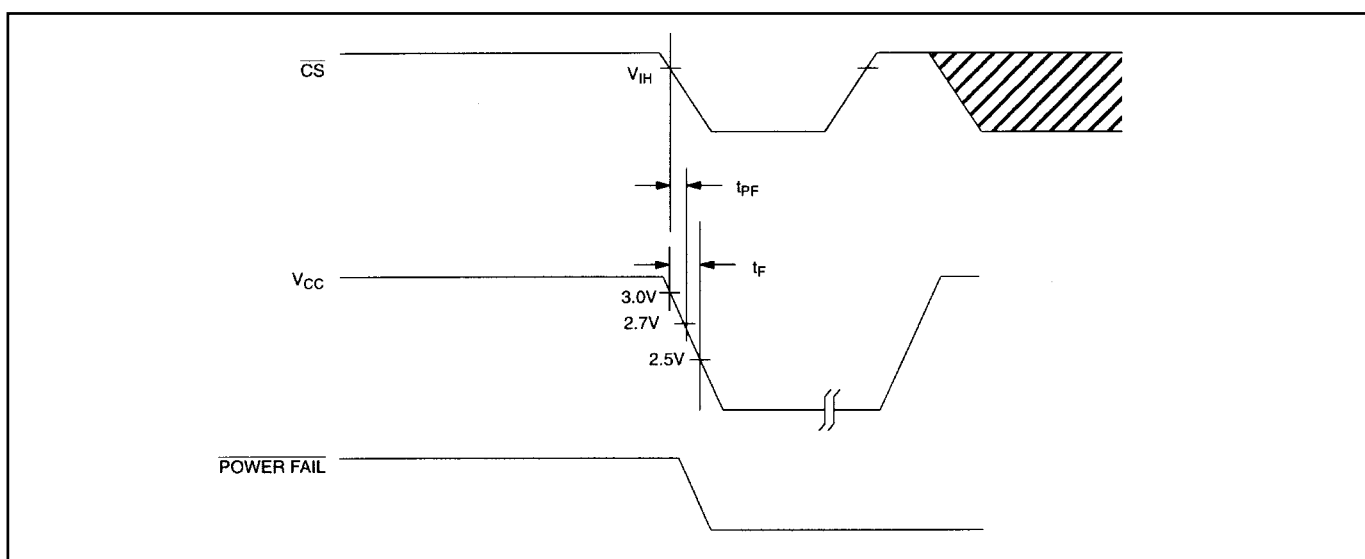
POWER-DOWN CONDITION—5V OPERATION



POWER-UP CONDITION—3V OPERATION



POWER-DOWN CONDITION—3V OPERATION

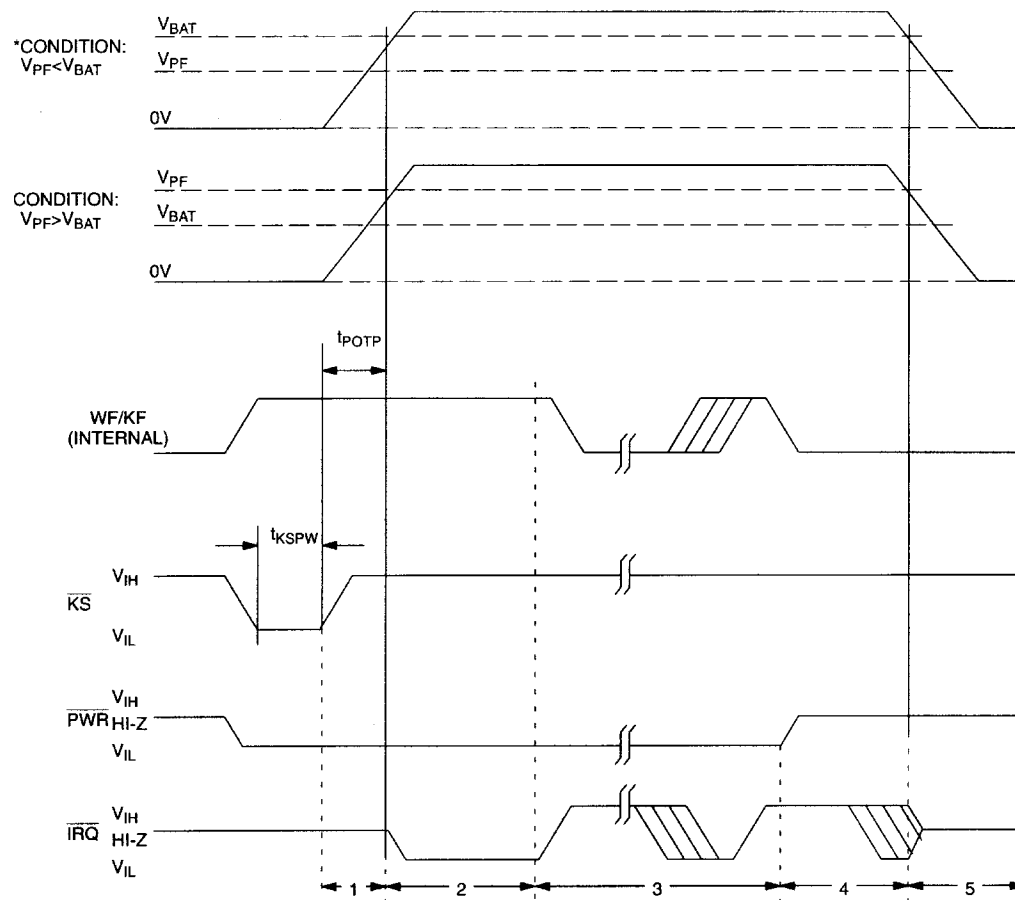


WAKE-UP/KICKSTART TIMING

($T_A = +25^\circ\text{C}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart Input Pulse Width	t_{KSPW}	2			μs	
Wake-Up/Kickstart Power-On Timeout	t_{POTO}	2			seconds	10

WAKE-UP/KICKSTART TIMING



NOTE: TIME INTERVALS SHOWN ABOVE ARE REFERENCED IN WAKE-UP/KICKSTART SECTION.

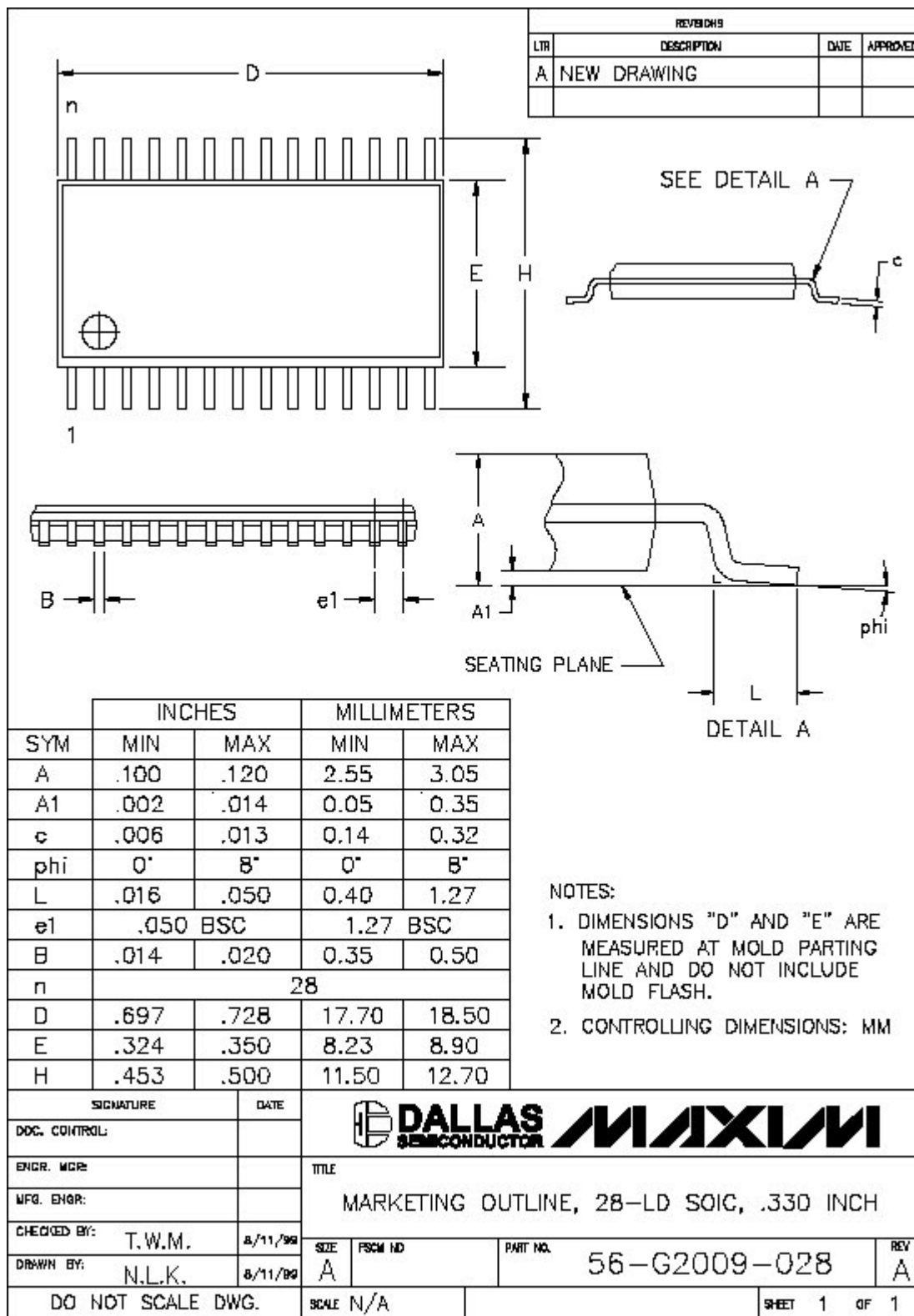
*THIS CONDITION CAN OCCUR WHEN THE DEVICE IS OPERATED IN 3V MODE.

NOTES:

- 1) All voltages are referenced to ground.
- 2) Typical values are at +25°C and nominal supplies.
- 3) Outputs are open.
- 4) Value for voltage and currents is from the V_{CCI} input pin to the V_{CCO} pin.
- 5) Write protection trip point occurs during power fail prior to switchover from V_{CC} to V_{BAT} .
- 6) Value for voltage and currents is from the V_{BAT} input pin to the V_{CCO} pin.
- 7) Applies to the AD0–AD7 pins, and the SQW pin when each is in a high impedance state.
- 8) The $\overline{IRQ}$ pin is open drain.
- 9) Measured with a load of 50pF + 1 TTL gate.
- 10) Wake-up/kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.
- 11) V_{SW} is determined by the larger of V_{BAT} and V_{BAUX} .
- 12) Z_{CE} is an average input to output impedance as the input is swept from GND to V_{CCI} and less than 4mA is forced through Z_{CE} .
- 13) The DS1693 keeps time to an accuracy of ± 1 minute per month during data retention time for the period of t_{DR} .
- 14) t_{DR} is the amount of time that the internal battery can power the internal oscillator and internal registers of the DS1693. As such, t_{DR} is specified with V_{CCO} floating. If V_{CCO} is powering an external SRAM, an auxiliary battery must be connected to the V_{BAUX} pin. The auxiliary battery should be sized such that it can power the external SRAM for the t_{DR} period.
- 15) The $\overline{CEI}$ pin has an internal pullup of 60k Ω .
- 16) The PSEL pin has an internal pulldown of 60k Ω .
- 17) For industrial grade parts, I_{BAT} (with OSC off) limit increases to 250nA.
- 18) Real-time clock modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used.

PACKAGE INFORMATION

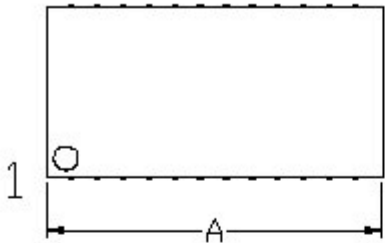
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.)



PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.)

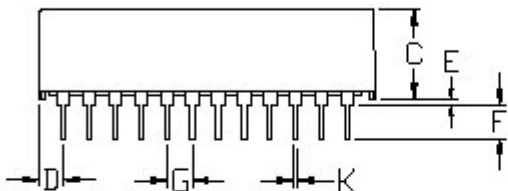
REVISIONS			
UTR	DESCRIPTION	DATE	APPROVED
A	ECN 35439		



1

A

Some pins may be missing by design



C

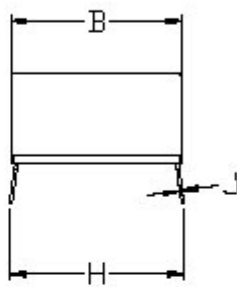
E

F

D

G

K



B

H

J

ALL DIMENSIONS ARE IN INCHES. See page 2 for dimensions in mm

	24 PIN		28 PIN		32 PIN 740		40 PIN 720	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	1.320	1.340	1.520	1.540	1.680	1.720	2.075	2.115
C	0.330	0.370	0.330	0.370	0.330	0.370	0.280	0.320
D	0.100	0.130	0.100	0.130	0.070	0.100	0.070	0.100

	MIN	MAX
B	0.68	0.72
B	0.720	0.740

ALL PACKAGES	
E	0.010 0.040
F	0.120 0.160
G	0.090 0.110
H	0.590 0.630
J	0.008 0.012
K	0.015 0.021

SIGNATURE	DATE	 Marketing Outline Encapsulated DIP Package
DOC. CONTROL:		
ENGR. MGR:		
MFG. ENGR:		
CHECKED BY:		
DRAWN BY: RMA	2/03	SIZE A SCALE N/A PSON NO DWG NO. 56-G0001-001 REV A SHEET 1 OF 2

PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.)

REVISIONS									
LTR	DESCRIPTION						DATE	APPROVED	
A	ECN 35439								

ALL DIMENSIONS ARE IN MM									
	24 PIN		28 PIN		32 PIN 740		40 PIN 720		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
A	33.53	34.04	38.61	39.12	42.67	43.69	52.71	53.72	
C	0.30	9.40	8.38	9.40	8.38	9.40	7.11	0.13	
D	2.54	3.30	2.54	3.30	1.78	2.54	1.78	2.54	

	MIN	MAX	
B	17.27	18.29	24 PIN 720, 28 PIN 720 and 40 PIN 720
B	18.29	18.80	24 PIN 740, 28 PIN 740 and 32 PIN 740

ALL PACKAGES		
	MIN	MAX
E	0.25	1.02
F	3.05	4.06
G	2.29	2.79
H	14.99	16.00
J	0.20	0.30
K	0.38	0.53

			SIZE	FORM NO	DWG NO.	56-G0001-001	REV	A
			SCALE	N/A			SHEET	2 OF 2