



# ST8016S

---

**COM/SEG LCD Driver**

---

## **Datasheet**

**Version 0.24**

**2009/10/01**

Note: This is not a final specification.  
Some parameters are subject to change.

## 1. FEATURES

- Number of LCD drive outputs: 160
- Supply voltage for LCD drive: +15.0 to +30.0 V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Low output impedance

### (Segment mode)

- Shift clock frequency
  - 20 MHz (MAX.):  $V_{DD} = +5.0 \pm 0.5 \text{ V}$
  - 15 MHz (MAX.):  $V_{DD} = +3.0 \text{ to } +4.5 \text{ V}$
  - 12 MHz (MAX.):  $V_{DD} = +2.5 \text{ to } +3.0 \text{ V}$
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 160 bits of input data
- Line latch circuits are reset when /DISPOFF active

### (Common mode)

- Shift clock frequency: 4 MHz (MAX.)
- Built-in 160-bit bi-directional shift register (divisible into 80 bits x 2)
- Available in a single mode (160-bit shift register) or in a dual mode (80-bit shift register x 2)
  - $Y_1 \rightarrow Y_{160}$  Single mode
  - $Y_{160} \rightarrow Y_1$  Single mode
  - $Y_1 \rightarrow Y_{80}, Y_{81} \rightarrow Y_{160}$  Dual mode
  - $Y_{160} \rightarrow Y_{81}, Y_{80} \rightarrow Y_1$  Dual mode

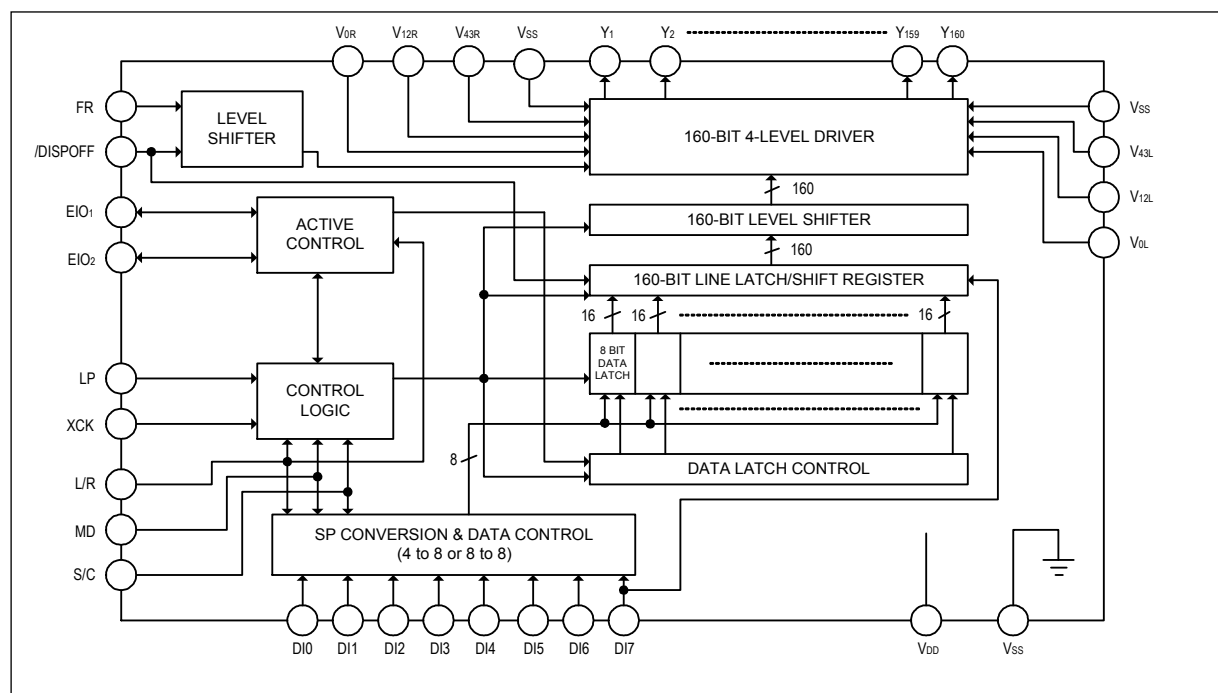
The above 4 shift directions are pin-selectable

- Shift register circuits are reset when /DISPOFF active

## 2. DESCRIPTION

The ST8016S is a 160-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work stations. The ST8016S is good both as a segment driver and a common driver, and it can create a low power consuming, high-resolution LCD.

### 3. BLOCK DIAGRAM



### 4. FUNCTIONAL OPERATIONS OF EACH BLOCK

| BLOCK                        | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Active Control               | In case of segment mode, controls the selection or non-selection of the chip. Following an LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 160 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins.   |
| SP Conversion & Data Control | In case of segment mode, keeps input data which are 2 clocks of XCK at 4-bit parallel input mode in latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel input mode in latch circuit; after that they are put on the internal data bus 8 bits at a time.                                                                                                                                                                      |
| Data Latch Control           | In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.                                                                                                                                                                            |
| Data Latch                   | In case of segment mode, latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 160 bits of data are read in 20 sets of 8 bits.                                                                                                                                                                                                                                 |
| Line Latch/Shift Register    | In case of segment mode, all 160 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block. In case of common mode, shifts data from the data input pin at the falling edge of the LP signal.                                                                                                                                                           |
| Level Shifter                | The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.                                                                                                                                                                                                                                                                                                                                           |
| 4-Level Driver               | Drives the LCD drive output pins from the line latch/shift register data, and selects one of 4 levels (V0, V12, V43 or VSS) based on the S/C, FR and /DISPOFF signals.                                                                                                                                                                                                                                                                                 |
| Control Logic                | Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 160 bits of data are read in, and the chip is non-selected. In case of common mode, controls the direction of data shift. |

## 5. INPUT/OUTPUT CIRCUITS

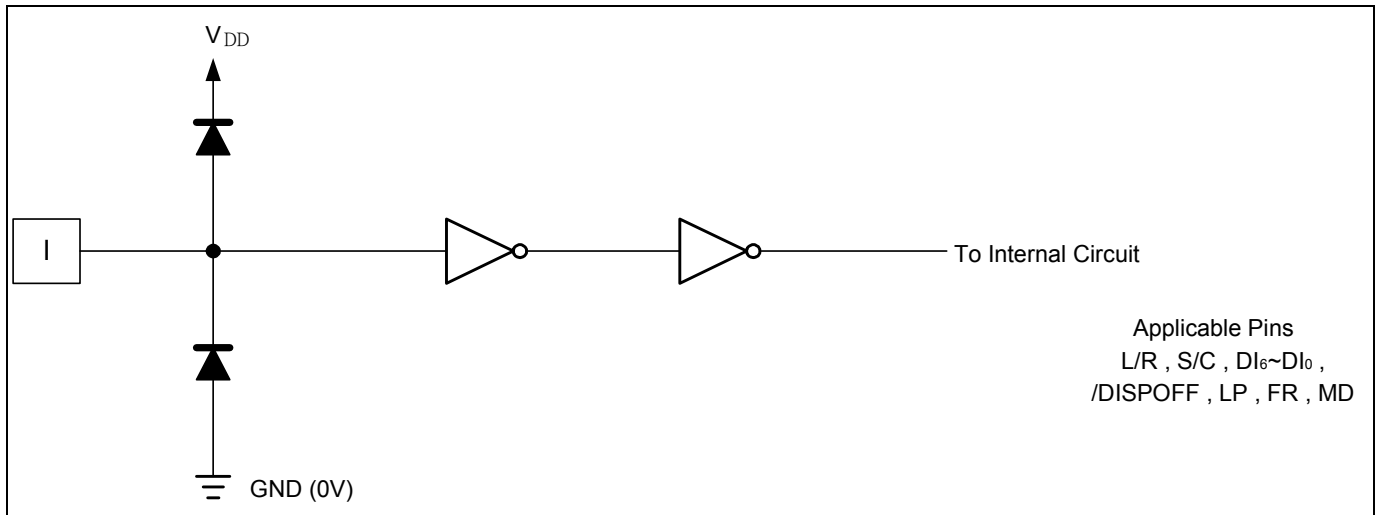


Figure 1 Input Circuit (1)

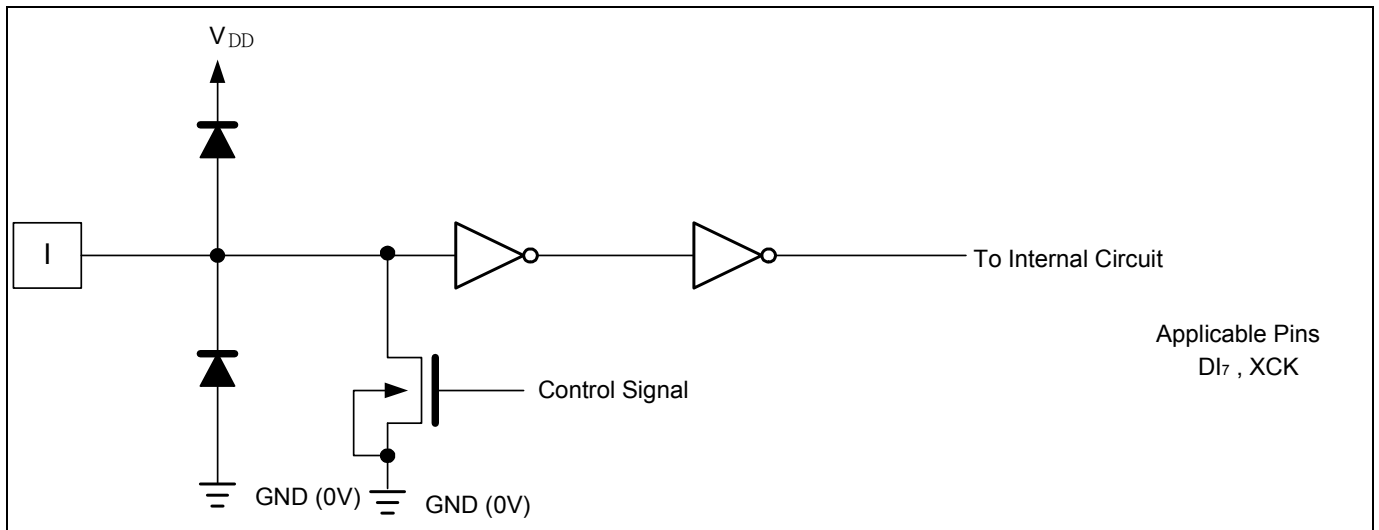


Figure 2 Input Circuit (2)

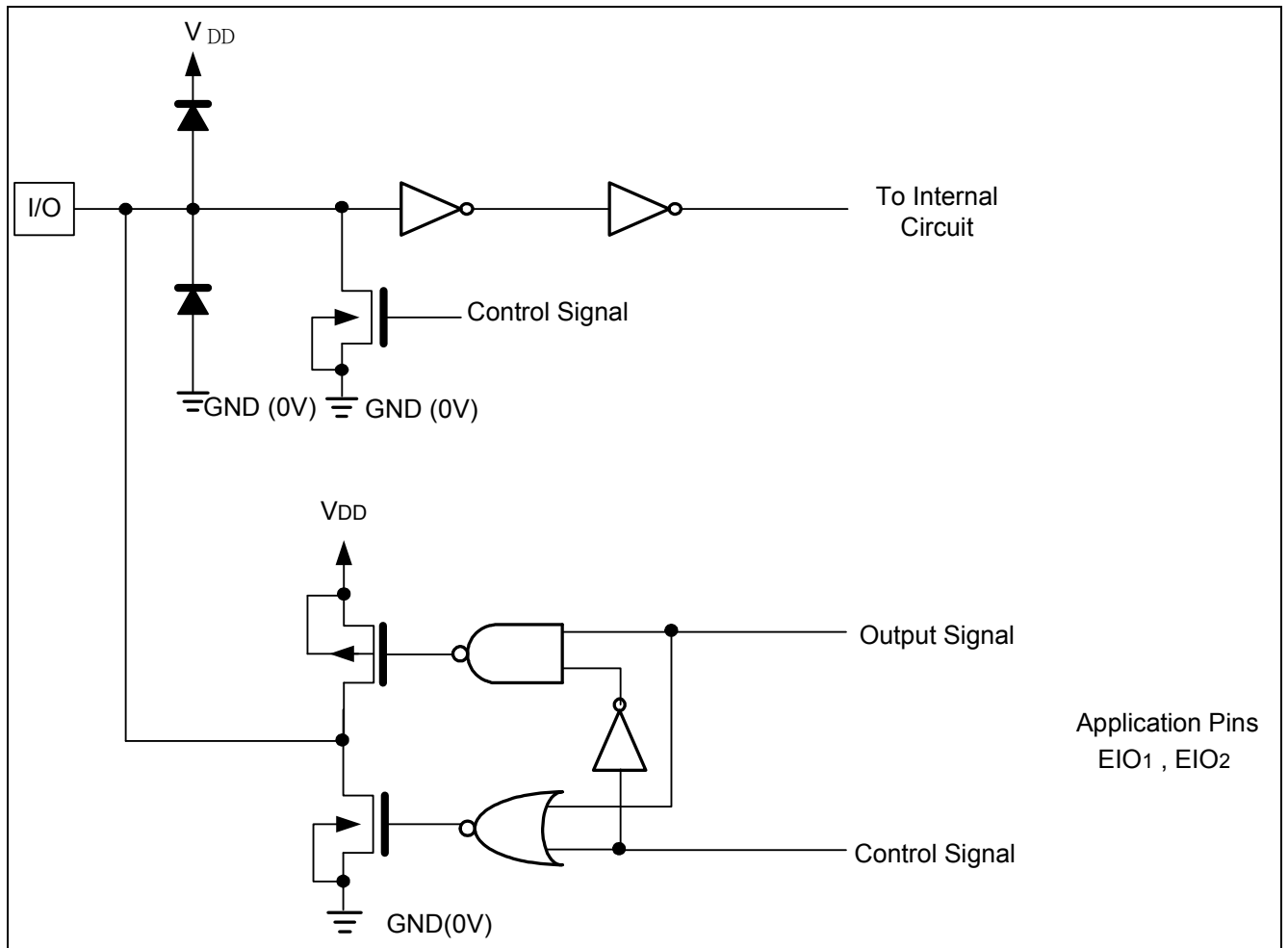


Figure 3 Input/Output Circuit

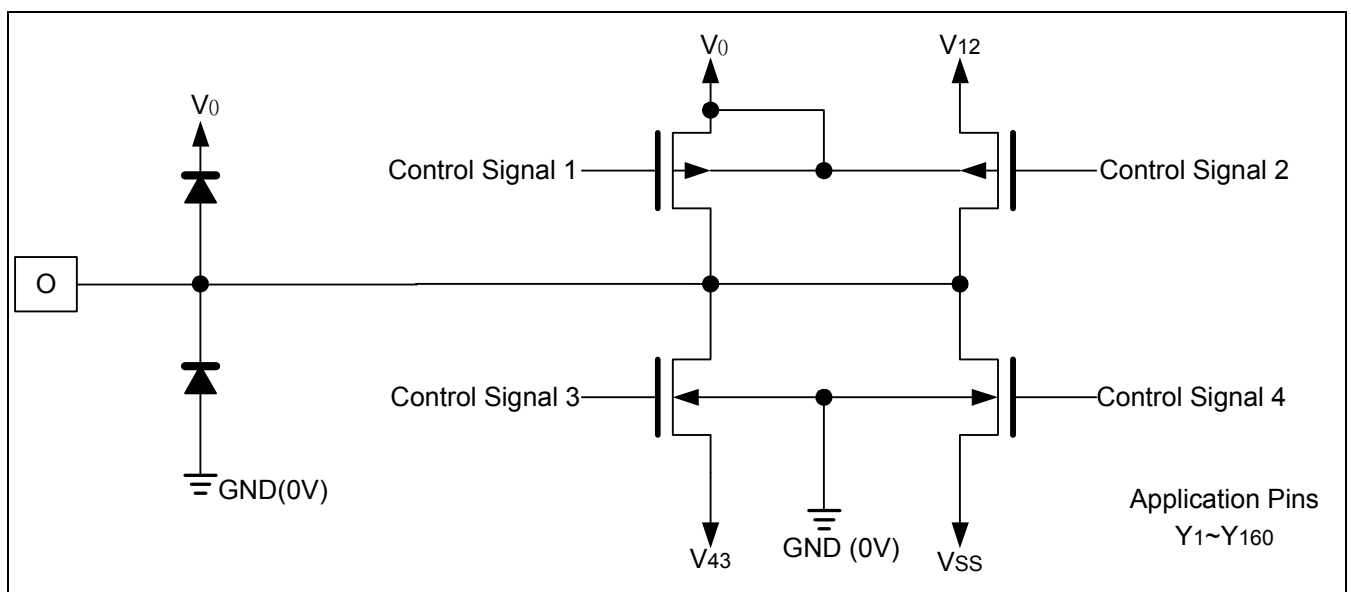


Figure 4 LCD Drive Output Circuit

## 6. FUNCTIONAL DESCRIPTION

### 6.1 Pin Functions

(Segment mode)

| SYMBOL                                                                                                          | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>DD</sub>                                                                                                 | Logic system power supply pin<br>• Connected to +2.5 to +5.5 V.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| GND                                                                                                             | Ground pin                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| LGND                                                                                                            | Logic system power ground pin<br>• Do not short LGND with GND and V <sub>SS</sub> by ITO on LCD panel<br>• Connect it to GND on PCB or FPC.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| V <sub>SS</sub>                                                                                                 | Connect to GND by ITO on LCD panel.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| V <sub>0L</sub> , V <sub>0R</sub><br>V <sub>12L</sub> , V <sub>12R</sub><br>V <sub>43L</sub> , V <sub>43R</sub> | Bias power supply pins for LCD drive voltage<br>• Normally use the bias voltages set by a resistor divider<br>• Ensure that voltages are set such that V <sub>SS</sub> < V <sub>43</sub> < V <sub>12</sub> < V <sub>0</sub> .<br>• V <sub>iL</sub> and V <sub>iR</sub> (i = 0, 12, 43) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| DI7-DI0                                                                                                         | Input pins for display data<br>• In 4-bit parallel mode, DI3-DI0 are the display data input pins, and DI7-DI4 must be connected to LGND or V <sub>DD</sub> .<br>• In 8-bit parallel mode, All DI7-DI0 pins are the display data input pins.<br>• Refer to section 6.2.2.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| XCK                                                                                                             | Clock input pin for taking display data<br>• Data is read at the falling edge of the clock pulse.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| LP                                                                                                              | Latch pulse input pin for display data<br>• Data is latched at the falling edge of the clock pulse.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| L/R                                                                                                             | Input pin for selecting the reading direction of display data<br>• When set to LGND level "L", data is read sequentially from Y <sub>160</sub> to Y <sub>1</sub> .<br>• When set to V <sub>DD</sub> level "H", data is read sequentially from Y <sub>1</sub> to Y <sub>160</sub> .<br>• Refer to section 6.2.2.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| /DISPOFF                                                                                                        | Control input pin for output of non-select level<br>• The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit.<br>• When set to LGND level "L", the LCD drive output pins (Y <sub>1</sub> -Y <sub>160</sub> ) are set to level V <sub>SS</sub> .<br>• When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled the driver outputs non-select level (V <sub>12</sub> or V <sub>43</sub> ), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, it cannot output the reading data correctly.<br>• Table of truth-values is shown in "TRUTH TABLE" in Functional Operations. |
| FR                                                                                                              | AC signal input pin for LCD drive waveform<br>• The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit.<br>• Normally it inputs a frame inversion signal.<br>• The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal.<br>• Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| MD                                                                                                              | Mode selection pin<br>• When set to LGND level "L", 4-bit parallel input mode is set.<br>• When set to V <sub>DD</sub> level "H", 8-bit parallel input mode is set.<br>• Refer to section 6.2.2.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| S/C                                                                                                             | Segment mode/common mode selection pin<br>• When set to V <sub>DD</sub> level "H", segment mode is set.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| EIO <sub>1</sub> , EIO <sub>2</sub>                                                                             | Input/output pins for chip selection<br>• When L/R input is at LGND level "L", EIO <sub>1</sub> is set for output, and EIO <sub>2</sub> is set for input.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

|                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                 | <ul style="list-style-type: none"> <li>• When L/R input is at <math>V_{DD}</math> level "H", <math>EIO_1</math> is set for input, and <math>EIO_2</math> is set for output.</li> <li>• During output, set to "H" while LP • XCK is "H" and after 160 bits of data have been read, set to "L" for one cycle (from falling edge to failing edge of XCK), after which it returns to "H".</li> <li>• During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 160 bits of data have been read.</li> </ul> |
| $Y_1 - Y_{160}$ | <p>LCD drive output pins</p> <ul style="list-style-type: none"> <li>• Corresponding directly to each bit of the data latch, one level (<math>V_0</math>, <math>V_{12}</math> or <math>V_{43}</math>) is selected and output.</li> <li>• Table of truth values is shown in "TRUTH TABLE" in Functional Operations.</li> </ul>                                                                                                                                                                                                                                        |

(Common mode)

| SYMBOL                                                       | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|--------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $V_{DD}$                                                     | <p>Logic system power supply pin</p> <ul style="list-style-type: none"> <li>• Connected to +2.5 to +5.5 V.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| GND                                                          | Ground pin                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| LGND                                                         | <p>Logic system power ground pin</p> <ul style="list-style-type: none"> <li>• Do not short LGND with GND and <math>V_{SS}</math> by ITO on LCD panel</li> <li>• Connect it to GND on PCB or FPC.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| $V_{SS}$                                                     | Connect to GND by ITO on LCD panel.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| $V_{0L}, V_{0R}$<br>$V_{12L}, V_{12R}$<br>$V_{43L}, V_{43R}$ | <p>Bias power supply pins for LCD drive voltage</p> <ul style="list-style-type: none"> <li>• Normally use the bias voltages set by a resistor divider.</li> <li>• Ensure that voltages are set such that <math>V_{SS} &lt; V_{43} &lt; V_{12} &lt; V_0</math>.</li> <li>• <math>V_{iL}</math> and <math>V_{iR}</math> (<math>i = 0, 12, 43</math>) must connect to an external power supply, and supply regular voltage that is assigned by specification for each power pin.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                        |
| $EIO_1$                                                      | <p>Shift data input/output pin for bi-directional shift register</p> <ul style="list-style-type: none"> <li>• Output pin when L/R is at LGND level "L", input pin when L/R is at <math>V_{DD}</math> level "H".</li> <li>• When L/R = H, <math>EIO_1</math> is used as input pin, it will be pulled down.</li> <li>• When L/R = L, <math>EIO_1</math> is used as output pin, it won't be pulled down.</li> <li>• Refer to section 6.2.2.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| $EIO_2$                                                      | <p>Shift data input/output pin for bi-directional shift register</p> <ul style="list-style-type: none"> <li>• Input pin when L/R is at LGND level "L", output pin when L/R is at <math>V_{DD}</math> level "H".</li> <li>• When L/R = L, <math>EIO_2</math> is used as input pin, it will be pulled down.</li> <li>• When L/R = H, <math>EIO_2</math> is used as output pin, it won't be pulled down.</li> <li>• Refer to section 6.2.2.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| LP                                                           | <p>Shift clock pulse input pin for bi-directional shift register</p> <ul style="list-style-type: none"> <li>• * Data is shifted at the falling edge of the clock pulse.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| L/R                                                          | <p>Input pin for selecting the shift direction of bi-directional shift register</p> <ul style="list-style-type: none"> <li>• Data is shifted from <math>Y_{160}</math> to <math>Y_1</math> when set to LGND level "L", and data is shifted from <math>Y_1</math> to <math>Y_{160}</math> when set to <math>V_{DD}</math> level "H".</li> <li>• Refer to section 6.2.2.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| /DISPOFF                                                     | <p>Control input pin for output of non-select level</p> <ul style="list-style-type: none"> <li>• The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit.</li> <li>• When set to LGND level "L", the LCD drive output pins (<math>Y_1 - Y_{160}</math>) are set to level <math>V_{SS}</math>.</li> <li>• When set to "L", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (<math>V_{12}</math> or <math>V_{43}</math>), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly.</li> <li>• Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.</li> </ul> |
| FR                                                           | <p>AC signal input pin for LCD drive waveform</p> <ul style="list-style-type: none"> <li>• The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit.</li> <li>• Normally it inputs a frame inversion signal.</li> <li>• The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal.</li> <li>• Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                  |

|                                  |                                                                                                                                                                                                                                                                                                                                                                        |
|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MD                               | Mode selection pin<br>• When set to LGND level "L", single mode operation is selected; when set to V <sub>DD</sub> level "H" dual mode operation is selected.<br>• Refer to section 6.2.2.                                                                                                                                                                             |
| DI7                              | Dual mode data input pin<br>• According to the data shift direction of the data shift register, data can be input starting from the 81st bit.<br>When the chip is used in dual mode, DI7 will be pulled down.<br>When the chip is used in single mode, DI7 won't be pulled down(Connect to LGND or V <sub>DD</sub> , avoiding floating.).<br>• Refer to section 6.2.2. |
| S/C                              | Segment mode/common mode selection pin<br>• When set to LGND level "L", common mode is set.                                                                                                                                                                                                                                                                            |
| DI6-DI0                          | Not used<br>• Connect DI6-DI0 to LGND or V <sub>DD</sub> , avoiding floating.                                                                                                                                                                                                                                                                                          |
| XCK                              | Not used<br>• XCK is pulled down in common mode, so connect to LGND or open.                                                                                                                                                                                                                                                                                           |
| Y <sub>1</sub> -Y <sub>160</sub> | LCD drive output pins<br>• Corresponding directly to each bit of the shift register, one level (V <sub>0</sub> , V <sub>12</sub> , V <sub>43</sub> , or V <sub>SS</sub> ) is selected and output.<br>• Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.                                                                                       |

## 6.2 Functional Operations

### 6.2.1 Truth table

(Segment Mode)

| FR | LATCH DATA | /DISPOFF | LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y160) |
|----|------------|----------|------------------------------------------|
| L  | L          | H        | V <sub>43</sub>                          |
| L  | H          | H        | V <sub>SS</sub>                          |
| H  | L          | H        | V <sub>12</sub>                          |
| H  | H          | H        | V <sub>0</sub>                           |
| X  | X          | L        | V <sub>SS</sub>                          |

(Common Mode)

| FR | LATCH DATA | /DISPOFF | LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y160) |
|----|------------|----------|------------------------------------------|
| L  | L          | H        | V <sub>43</sub>                          |
| L  | H          | H        | V <sub>0</sub>                           |
| H  | L          | H        | V <sub>12</sub>                          |
| H  | H          | H        | V <sub>SS</sub>                          |
| X  | X          | L        | V <sub>SS</sub>                          |

NOTES:

- $V_{SS} < V_{43} < V_{12} < V_0$
  - L : LGND (0 V), H : V<sub>DD</sub> (+2.5 to +5.5 V), X : Don't care
  - "Don't care" should be fixed to "H" or "L", avoiding floating.
- There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.  
Supply regular voltage that is assigned by specification for each power pin.

## 6.2.2 Relationship between the display data and LCD drive output Pins

(Segment Mode)

(a) 4-bit Parallel Input Mode

| MD | L/R | EIO <sub>1</sub> | EIO <sub>2</sub> | DATA INPUT      | NUMBER OF CLOCKS |                  |                  |     |                  |                  |                  |
|----|-----|------------------|------------------|-----------------|------------------|------------------|------------------|-----|------------------|------------------|------------------|
|    |     |                  |                  |                 | 40 CLOCK         | 39 CLOCK         | 38 CLOCK         | ... | 3 CLOCK          | 2 CLOCK          | 1 CLOCK          |
| L  | L   | Output           | Input            | DI <sub>0</sub> | Y <sub>1</sub>   | Y <sub>5</sub>   | Y <sub>9</sub>   | ... | Y <sub>149</sub> | Y <sub>153</sub> | Y <sub>157</sub> |
|    |     |                  |                  | DI <sub>1</sub> | Y <sub>2</sub>   | Y <sub>6</sub>   | Y <sub>10</sub>  | ... | Y <sub>150</sub> | Y <sub>154</sub> | Y <sub>158</sub> |
|    |     |                  |                  | DI <sub>2</sub> | Y <sub>3</sub>   | Y <sub>7</sub>   | Y <sub>11</sub>  | ... | Y <sub>151</sub> | Y <sub>155</sub> | Y <sub>159</sub> |
|    |     |                  |                  | DI <sub>3</sub> | Y <sub>4</sub>   | Y <sub>8</sub>   | Y <sub>12</sub>  | ... | Y <sub>152</sub> | Y <sub>156</sub> | Y <sub>160</sub> |
| L  | H   | Input            | Output           | DI <sub>0</sub> | Y <sub>160</sub> | Y <sub>156</sub> | Y <sub>152</sub> | ... | Y <sub>12</sub>  | Y <sub>8</sub>   | Y <sub>4</sub>   |
|    |     |                  |                  | DI <sub>1</sub> | Y <sub>159</sub> | Y <sub>155</sub> | Y <sub>151</sub> | ... | Y <sub>11</sub>  | Y <sub>7</sub>   | Y <sub>3</sub>   |
|    |     |                  |                  | DI <sub>2</sub> | Y <sub>158</sub> | Y <sub>154</sub> | Y <sub>150</sub> | ... | Y <sub>10</sub>  | Y <sub>6</sub>   | Y <sub>2</sub>   |
|    |     |                  |                  | DI <sub>3</sub> | Y <sub>157</sub> | Y <sub>153</sub> | Y <sub>149</sub> | ... | Y <sub>9</sub>   | Y <sub>5</sub>   | Y <sub>1</sub>   |

(b) 8-bit Parallel Input Mode

| MD | L/R | EIO <sub>1</sub> | EIO <sub>2</sub> | DATA INPUT      | NUMBER OF CLOCKS |                  |                  |     |                  |                  |                  |
|----|-----|------------------|------------------|-----------------|------------------|------------------|------------------|-----|------------------|------------------|------------------|
|    |     |                  |                  |                 | 20 CLOCK         | 19 CLOCK         | 18 CLOCK         | ... | 3 CLOCK          | 2 CLOCK          | 1 CLOCK          |
| H  | L   | Output           | Input            | DI <sub>0</sub> | Y <sub>1</sub>   | Y <sub>9</sub>   | Y <sub>17</sub>  | ... | Y <sub>137</sub> | Y <sub>145</sub> | Y <sub>153</sub> |
|    |     |                  |                  | DI <sub>1</sub> | Y <sub>2</sub>   | Y <sub>10</sub>  | Y <sub>18</sub>  | ... | Y <sub>138</sub> | Y <sub>146</sub> | Y <sub>154</sub> |
|    |     |                  |                  | DI <sub>2</sub> | Y <sub>3</sub>   | Y <sub>11</sub>  | Y <sub>19</sub>  | ... | Y <sub>139</sub> | Y <sub>147</sub> | Y <sub>155</sub> |
|    |     |                  |                  | DI <sub>3</sub> | Y <sub>4</sub>   | Y <sub>12</sub>  | Y <sub>20</sub>  | ... | Y <sub>140</sub> | Y <sub>148</sub> | Y <sub>156</sub> |
|    |     |                  |                  | DI <sub>4</sub> | Y <sub>5</sub>   | Y <sub>13</sub>  | Y <sub>21</sub>  | ... | Y <sub>141</sub> | Y <sub>149</sub> | Y <sub>157</sub> |
|    |     |                  |                  | DI <sub>5</sub> | Y <sub>6</sub>   | Y <sub>14</sub>  | Y <sub>22</sub>  | ... | Y <sub>142</sub> | Y <sub>150</sub> | Y <sub>158</sub> |
|    |     |                  |                  | DI <sub>6</sub> | Y <sub>7</sub>   | Y <sub>15</sub>  | Y <sub>23</sub>  | ... | Y <sub>143</sub> | Y <sub>151</sub> | Y <sub>159</sub> |
|    |     |                  |                  | DI <sub>7</sub> | Y <sub>8</sub>   | Y <sub>16</sub>  | Y <sub>24</sub>  | ... | Y <sub>144</sub> | Y <sub>152</sub> | Y <sub>160</sub> |
| H  | H   | Input            | Output           | DI <sub>0</sub> | Y <sub>160</sub> | Y <sub>152</sub> | Y <sub>144</sub> | ... | Y <sub>24</sub>  | Y <sub>16</sub>  | Y <sub>8</sub>   |
|    |     |                  |                  | DI <sub>1</sub> | Y <sub>159</sub> | Y <sub>151</sub> | Y <sub>143</sub> | ... | Y <sub>23</sub>  | Y <sub>15</sub>  | Y <sub>7</sub>   |
|    |     |                  |                  | DI <sub>2</sub> | Y <sub>158</sub> | Y <sub>150</sub> | Y <sub>142</sub> | ... | Y <sub>22</sub>  | Y <sub>14</sub>  | Y <sub>6</sub>   |
|    |     |                  |                  | DI <sub>3</sub> | Y <sub>157</sub> | Y <sub>149</sub> | Y <sub>141</sub> | ... | Y <sub>21</sub>  | Y <sub>13</sub>  | Y <sub>5</sub>   |
|    |     |                  |                  | DI <sub>4</sub> | Y <sub>156</sub> | Y <sub>148</sub> | Y <sub>140</sub> | ... | Y <sub>20</sub>  | Y <sub>12</sub>  | Y <sub>4</sub>   |
|    |     |                  |                  | DI <sub>5</sub> | Y <sub>155</sub> | Y <sub>147</sub> | Y <sub>139</sub> | ... | Y <sub>19</sub>  | Y <sub>11</sub>  | Y <sub>3</sub>   |
|    |     |                  |                  | DI <sub>6</sub> | Y <sub>154</sub> | Y <sub>146</sub> | Y <sub>138</sub> | ... | Y <sub>18</sub>  | Y <sub>10</sub>  | Y <sub>2</sub>   |
|    |     |                  |                  | DI <sub>7</sub> | Y <sub>153</sub> | Y <sub>145</sub> | Y <sub>137</sub> | ... | Y <sub>17</sub>  | Y <sub>9</sub>   | Y <sub>1</sub>   |

(Common Mode)

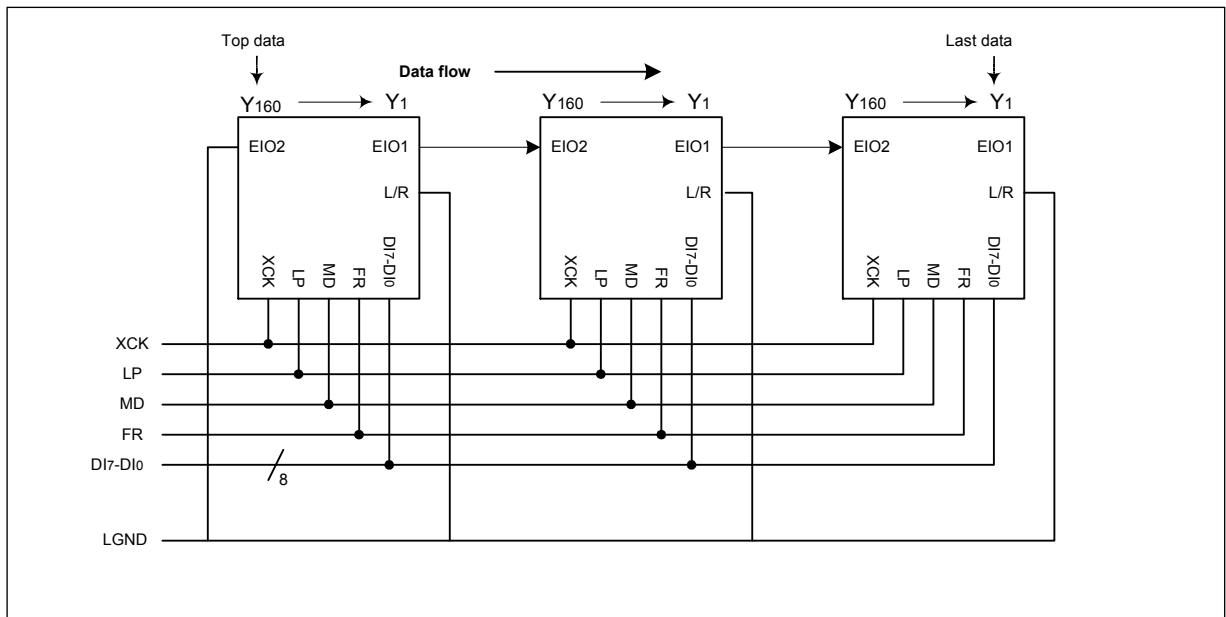
| MD            | L/R | DATA TRANSFER DIRECTION                                                | EIO <sub>1</sub> | EIO <sub>2</sub> | DI <sub>7</sub> |
|---------------|-----|------------------------------------------------------------------------|------------------|------------------|-----------------|
| L<br>(Single) | L   | Y <sub>160</sub> → Y <sub>1</sub>                                      | Output           | Input            | X               |
|               | H   | Y <sub>1</sub> → Y <sub>160</sub>                                      | Input            | Output           | X               |
| H<br>(Dual)   | L   | Y <sub>160</sub> → Y <sub>81</sub><br>Y <sub>80</sub> → Y <sub>1</sub> | Output           | Input            | Input           |
|               | H   | Y <sub>1</sub> → Y <sub>80</sub><br>Y <sub>81</sub> → Y <sub>160</sub> | Input            | Output           | Input           |

NOTES:

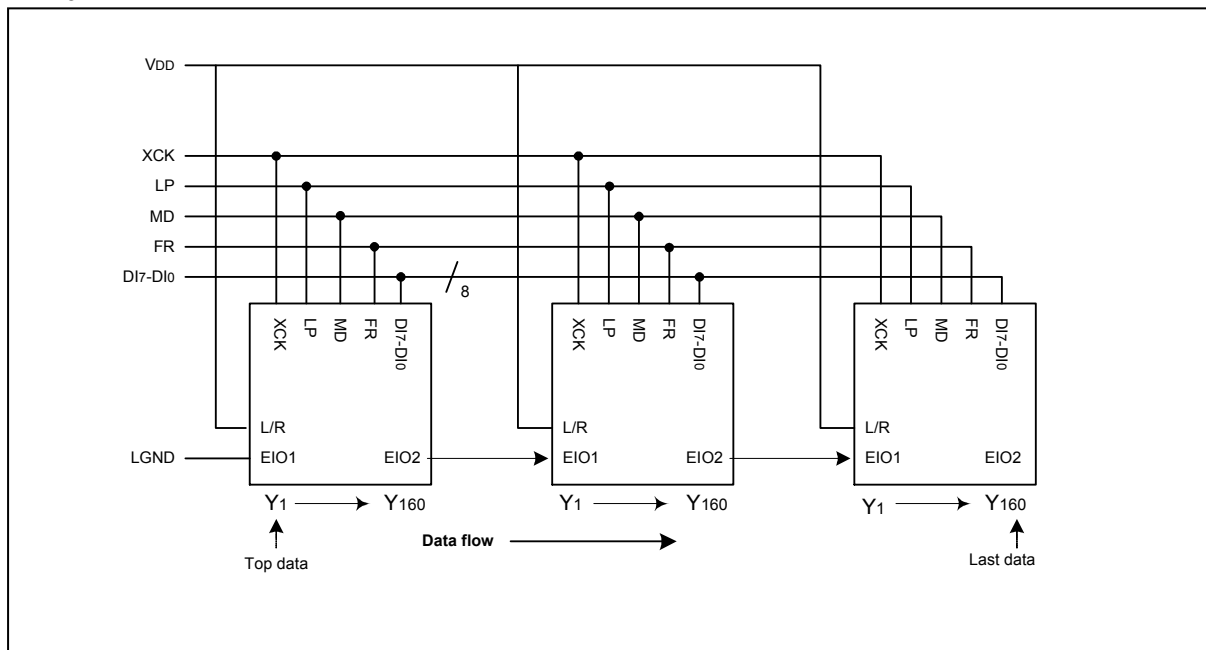
- L : LGND (0 V), H : V<sub>DD</sub> (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

### 6.2.3 Connection examples of plural segment drivers

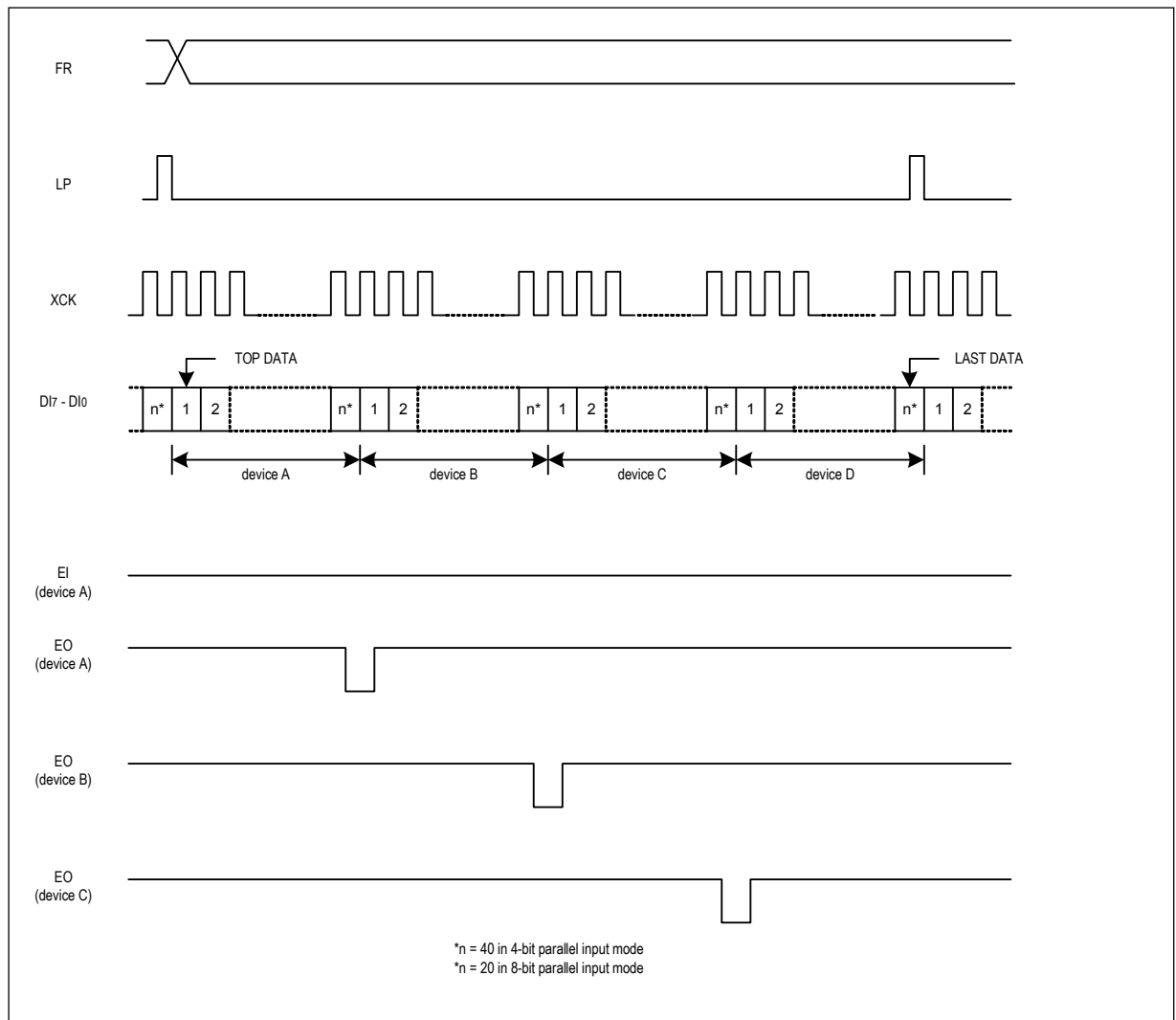
(a) When L/R = "L"



(b) When L/R = "H"

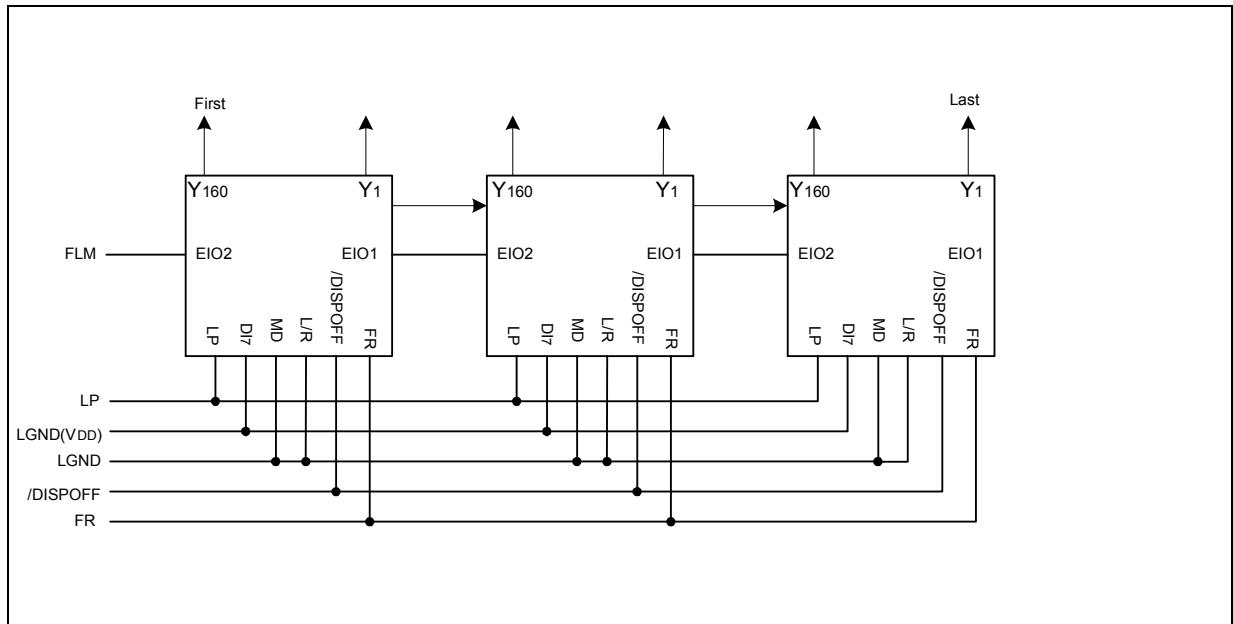


## 6.2.4 Timing chart of 4-device cascade connection of segment drivers

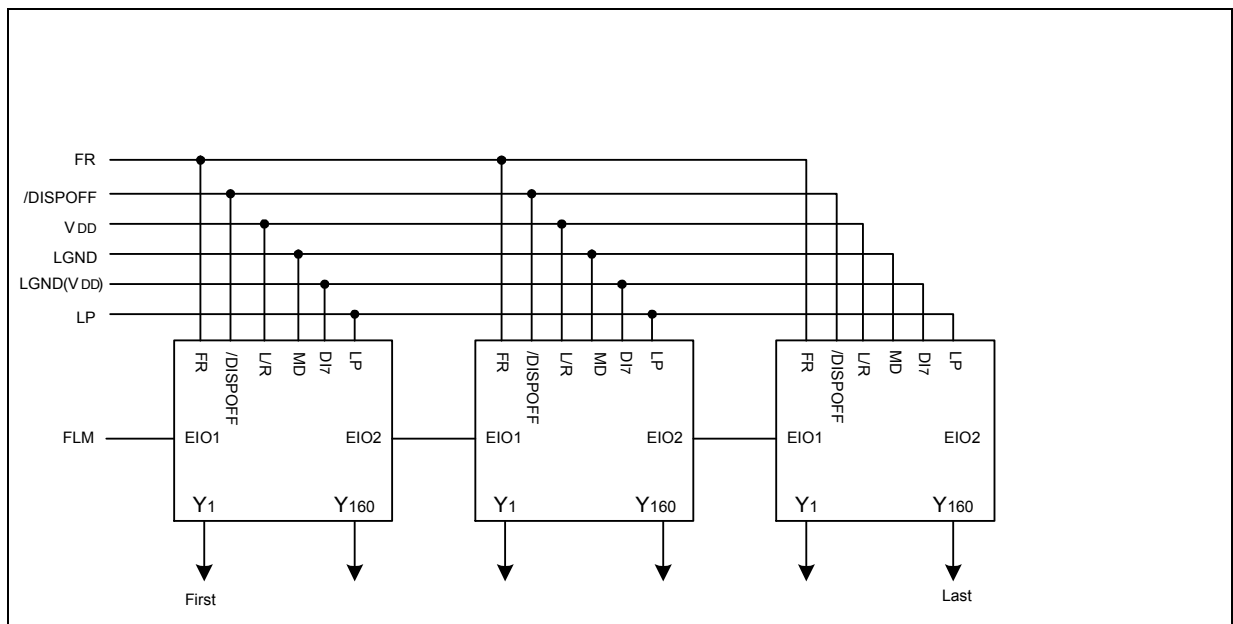


## 6.2.5 Connection examples for plural common drivers

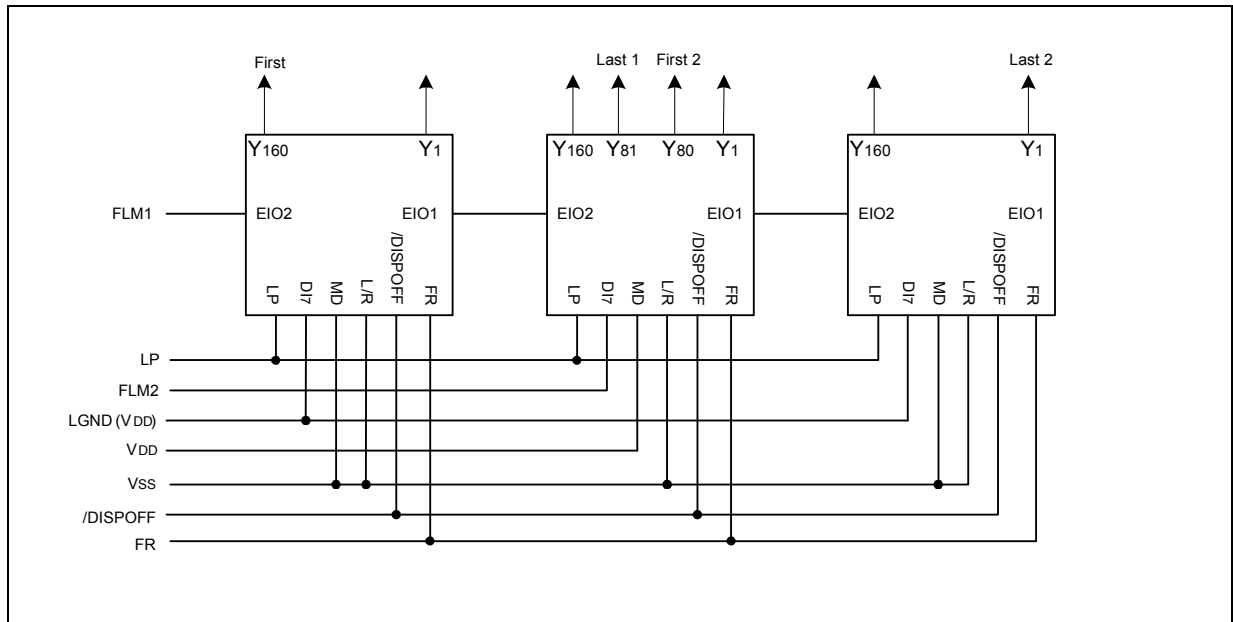
### (a) Single Mode (L/R = "L")



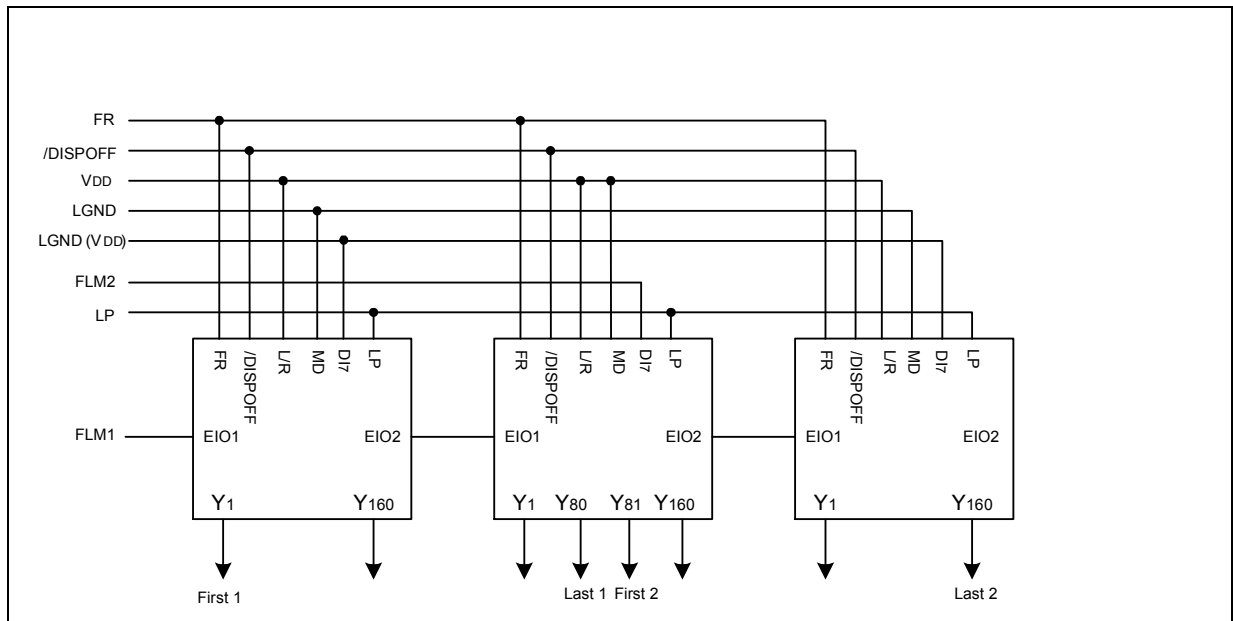
### (b) Single Mode (L/R = "H")



(c) Dual Mode (L/R = "L")



(d) Dual mode (L/R = "H")



## 7. PRECAUTIONS

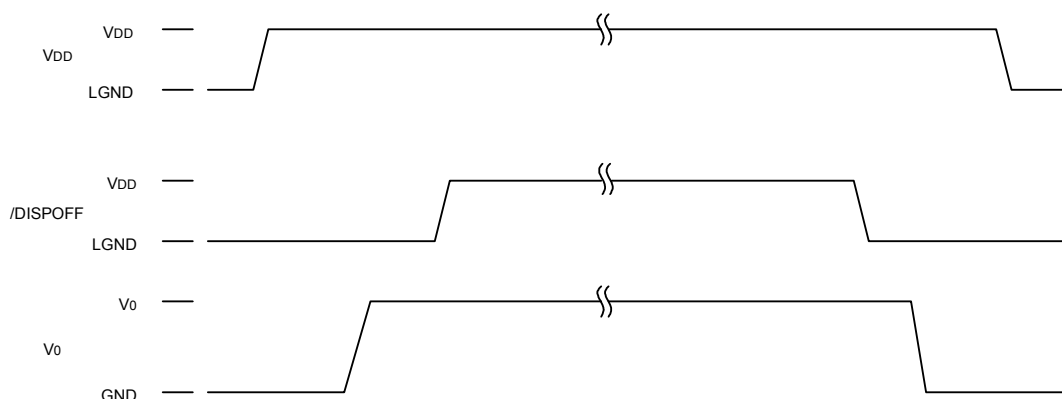
### Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so a high current that may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating may permanently damage it. The details are as follows,

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power
- It is advisable to connect the serial resistor ( $4.7\Omega$  to  $50\Omega$ ) or fuse to the LCD drive power  $V_0$  of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level LGND on /DISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here



## 8. ABSOLUTE MAXIMUM RATINGS

| PARAMETER           | SYMBOL    | APPLICABLE PINS                                          | RATING                    | UNIT | NOTE |
|---------------------|-----------|----------------------------------------------------------|---------------------------|------|------|
| Supply voltage (1)  | $V_{DD}$  | $V_{DD}$                                                 | -0.3 ~ +7.0               | V    | 1, 2 |
| Supply voltage (2)  | $V_0$     | $V_{0L}, V_{0R}$                                         | -0.3 ~ +33.0              | V    |      |
|                     | $V_{12}$  | $V_{12L}, V_{12R}$                                       | $V_0 - 10 \sim V_0 + 0.3$ | V    |      |
|                     | $V_{43}$  | $V_{43L}, V_{43R}$                                       | -0.3 ~ $V_{SS} + 10$      | V    |      |
| Input voltage       | $V_I$     | D17-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, /DISPOFF | -0.3 to $V_{DD} + 0.3$    | V    |      |
| Storage temperature | $T_{STG}$ |                                                          | -45 to +125               | °C   |      |

### NOTES:

1.  $T_A = +25\text{ °C}$
2. The applicable voltage on logic pins with respect to LGND, high voltage pins with  $V_{SS}$  (0 V).
3. Stress over the "Absolute Max. Ratings" conditions will damage the device permanently.

## 9. RECOMMENDED OPERATING CONDITIONS

| PARAMETER             | SYMBOL    | APPLICABLE PINS  | MIN.  | TYP. | MAX.  | UNIT | NOTE |
|-----------------------|-----------|------------------|-------|------|-------|------|------|
| Supply voltage (1)    | $V_{DD}$  | $V_{DD}$         | +2.5  |      | +5.5  | V    | 1, 2 |
| Supply voltage (2)    | $V_0$     | $V_{0L}, V_{0R}$ | +15.0 |      | +30.0 | V    |      |
| Operating temperature | $T_{OPR}$ |                  | -25   |      | +85   | °C   |      |

### NOTES:

1. The applicable voltage on logic pins with respect to LGND, high voltage pins with  $V_{SS}$  (0 V).
2. Ensure that voltages are set such that  $V_{SS} < V_{43} < V_{12} < V_0$ .

## 10. ELECTRICAL CHARACTERISTICS

### 10.1 DC Characteristics

(Segment Mode) (LGND =  $V_{SS} = 0$  V,  $V_{DD} = +2.5$  to  $+5.5$  V,  $V_0 = +15.0$  to  $+30.0$  V,  $T_{OPR} = -25$  to  $+85^{\circ}\text{C}$ )

| PARAMETER                             | SYMBOL    | CONDITIONS                                   | APPLICABLE PINS                                                                    | MIN.         | TYP. | MAX.        | UNIT          | NOTE |
|---------------------------------------|-----------|----------------------------------------------|------------------------------------------------------------------------------------|--------------|------|-------------|---------------|------|
| Input "Low" voltage                   | $V_{IL}$  |                                              | DI7-DI0, XCK, LP, L/R                                                              |              |      | $0.2V_{DD}$ | V             |      |
| Input "High" voltage                  | $V_{IH}$  |                                              | FR, MD, S/C, EIO <sub>1</sub> , EIO <sub>2</sub> , /DISPOFF                        | $0.8V_{DD}$  |      |             | V             |      |
| Output "Low" voltage                  | $V_{OL}$  | $I_{OL} = +0.4$ mA                           | EIO <sub>1</sub> , EIO <sub>2</sub>                                                |              |      | +0.4        | V             |      |
| Output "High" voltage                 | $V_{OH}$  | $I_{OH} = -0.4$ mA                           |                                                                                    | $V_{DD}-0.4$ |      |             | V             |      |
| Input leakage current                 | $I_{LIL}$ | $V_i = \text{LGND}$                          | DI7-DI0, XCK, LP, LIR, FR, MD, S/C, EIO <sub>1</sub> , EIO <sub>2</sub> , /DISPOFF |              |      | -10         | $\mu\text{A}$ |      |
|                                       | $I_{LIH}$ | $V_i = V_{DD}$                               |                                                                                    |              |      | +10         | $\mu\text{A}$ |      |
| Output resistance                     | $R_{ON}$  | $ \Delta V_{ON}  = 0.5\text{V}$ $V_0 = 30$ V | Y <sub>1</sub> -Y <sub>160</sub>                                                   |              | 1.0  | 1.5         | k $\Omega$    |      |
| Standby current                       | $I_{STB}$ |                                              | LGND                                                                               |              |      | 50          | $\mu\text{A}$ | 1    |
| Supply current (1)<br>(Non-selection) | $I_{DD1}$ |                                              | $V_{DD}$                                                                           |              |      | 2.0         | mA            | 2    |
| Supply current (2)<br>(Selection)     | $I_{DD2}$ |                                              | $V_{DD}$                                                                           |              |      | 7.0         | mA            | 3    |
| Supply current (3)                    | $I_0$     |                                              | $V_{OL}$ , $V_{OR}$                                                                |              |      | 0.9         | mA            | 4    |

#### NOTES:

- $V_{DD} = +5.0$  V,  $V_0 = +30.0$  V,  $V_i = \text{LGND}$ .
- $V_{DD} = +5.0$  V,  $V_0 = +30.0$  V,  $f_{XCK} = 8$  MHz, no-load, EI =  $V_{DD}$ . The input data is turned over by data taking clock (4-bit parallel input mode).
- $V_{DD} = +5.0$  V,  $V_0 = +30.0$  V,  $f_{XCK} = 8$  MHz, no-load, EI = LGND. The input data is turned over by data taking clock (4-bit parallel input mode).
- $V_{DD} = +5.0$  V,  $V_0 = +30.0$  V,  $f_{XCK} = 8\text{MHz}$ ,  $f_{LP} = 19.2$  kHz,  $f_{FR} = 80$  Hz, no-load. The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) (LGND =  $V_{SS} = 0$  V,  $V_{DD} = +2.5$  to  $+5.5$  V,  $V_0 = +15.0$  to  $+30.0$  V,  $T_{OPR} = -25$  to  $+85^{\circ}\text{C}$ )

| PARAMETER               | SYMBOL    | CONDITIONS                                   | APPLICABLE PINS                                                                    | MIN.         | TYP. | MAX.        | UNIT          | NOTE |
|-------------------------|-----------|----------------------------------------------|------------------------------------------------------------------------------------|--------------|------|-------------|---------------|------|
| Input "Low" voltage     | $V_{IL}$  |                                              | DI7-DI0, XCK, LP, L/R                                                              |              |      | $0.2V_{DD}$ | V             |      |
| Input "High" voltage    | $V_{IH}$  |                                              | FR, MD, S/C, EIO <sub>1</sub> , EIO <sub>2</sub> , /DISPOFF                        | $0.8V_{DD}$  |      |             | V             |      |
| Output "Low" voltage    | $V_{OL}$  | $I_{OL} = +0.4$ mA                           | EIO <sub>1</sub> , EIO <sub>2</sub>                                                |              |      | +0.4        | V             |      |
| Output "High" voltage   | $V_{OH}$  | $I_{OH} = -0.4$ mA                           |                                                                                    | $V_{DD}-0.4$ |      |             | V             |      |
| Input leakage current   | $I_{LIL}$ | $V_i = \text{LGND}$                          | DI7-DI0, XCK, LP, LIR, FR, MD, S/C, EIO <sub>1</sub> , EIO <sub>2</sub> , /DISPOFF |              |      | -10.0       | $\mu\text{A}$ |      |
|                         | $I_{LIH}$ | $V_i = V_{DD}$                               | DI6-DI0, LP, L/R, FR, MD, S/C, /DISPOFF                                            |              |      | +10.0       | $\mu\text{A}$ |      |
| Input pull-down current | $I_{PD}$  | $V_i = V_{DD}$                               | DI7, XCK, EIO <sub>1</sub> , EIO <sub>2</sub>                                      |              |      | 100         | $\mu\text{A}$ |      |
| Output resistance       | $R_{ON}$  | $ \Delta V_{ON}  = 0.5\text{V}$ $V_0 = 30$ V | Y <sub>1</sub> -Y <sub>160</sub>                                                   |              | 1.0  | 1.5         | k $\Omega$    |      |
| Standby current         | $I_{SPD}$ |                                              | LGND                                                                               |              |      | 50          | $\mu\text{A}$ | 1    |
| Supply current (1)      | $I_{DD}$  |                                              | $V_{DD}$                                                                           |              |      | 80          | $\mu\text{A}$ | 2    |
| Supply current (2)      | $I_0$     |                                              | $V_{OL}$ , $V_{OR}$                                                                |              |      | 130         | $\mu\text{A}$ | 2    |

#### NOTES:

- $V_{DD} = +5.0$  V,  $V_0 = +30.0$  V,  $V_i = \text{LGND}$
- $V_{DD} = +5.0$  V,  $V_0 = +30.0$  V,  $f_{LP} = 19.2$  kHz,  $f_{FR} = 80$  Hz, 1/240 duty operation, no-load.

## 10.2 AC Characteristics

(Segment Mode 1) (LGND =  $V_{SS} = 0$  V,  $V_{DD} = +2.5$  to  $+3.0$  V,  $V_0 = +15.0$  to  $+30.0$  V,  $T_{OPR} = -25$  to  $+85$  °C)

| PARAMETER                                 | SYMBOL             | CONDITIONS            | MIN | TYP. | MAX. | UNIT    | NOTE |
|-------------------------------------------|--------------------|-----------------------|-----|------|------|---------|------|
| Shift clock period                        | $t_{WCK}$          | $t_R, t_F \leq 11$ ns | 125 |      |      | ns      | 1    |
| Shift clock "H" pulse width               | $t_{WCKH}$         |                       | 51  |      |      | ns      |      |
| Shift clock "L" pulse width               | $t_{WCKL}$         |                       | 51  |      |      | ns      |      |
| Data setup time                           | $t_{DS}$           |                       | 30  |      |      | ns      |      |
| Data hold time                            | $t_{DH}$           |                       | 40  |      |      | ns      |      |
| Latch pulse "H" pulse width               | $t_{WLPH}$         |                       | 51  |      |      | ns      |      |
| Shift clock rise to latch pulse rise time | $t_{LD}$           |                       | 0   |      |      | ns      |      |
| Shift clock fall to latch pulse fall time | $t_{SL}$           |                       | 51  |      |      | ns      |      |
| Latch pulse rise to shift clock rise time | $t_{LS}$           |                       | 51  |      |      | ns      |      |
| Latch pulse fall to shift clock fall time | $t_{LH}$           |                       | 51  |      |      | ns      |      |
| Enable setup time                         | $t_S$              |                       | 36  |      |      | ns      |      |
| Input signal rise time                    | $t_R$              |                       |     |      | 50   | ns      | 2    |
| Input signal fall time                    | $t_F$              |                       |     |      | 50   | ns      | 2    |
| DISPOFF removal time                      | $t_{SD}$           |                       | 100 |      |      | ns      |      |
| DISPOFF "L" pulse width                   | $t_{WDL}$          |                       | 1.2 |      |      | $\mu$ s |      |
| Output delay time (1)                     | $t_D$              | CL = 15 pF            |     |      | 78   | ns      |      |
| Output delay time (2)                     | $t_{PD1}, t_{PD2}$ | CL = 15 pF            |     |      | 1.2  | $\mu$ s |      |
| Output delay time (3)                     | $t_{PD3}$          | CL = 15 pF            |     |      | 1.2  | $\mu$ s |      |

NOTES:

1. Takes the cascade connection into consideration.
2.  $(t_{WCK} - t_{WCKH} - t_{WCKL})/2$  is maximum in the case of high speed operation.

(Segment Mode 2) (LGND =  $V_{SS} = 0$  V,  $V_{DD} = +5.0 \pm 0.5$  V,  $V_0 = +15.0$  to  $+30.0$  V,  $T_{OPR} = -25$  to  $+85$  °C)

| PARAMETER                                 | SYMBOL             | CONDITIONS            | MIN. | TYP. | MAX. | UNIT    | NOTE |
|-------------------------------------------|--------------------|-----------------------|------|------|------|---------|------|
| Shift clock period                        | $t_{WCK}$          | $t_R, t_F \leq 10$ ns | 66   |      |      | ns      | 1    |
| Shift clock "H" pulse width               | $t_{WCKH}$         |                       | 23   |      |      | ns      |      |
| Shift clock "L" pulse width               | $t_{WCKL}$         |                       | 23   |      |      | ns      |      |
| Data setup time                           | $t_{DS}$           |                       | 15   |      |      | ns      |      |
| Data hold time                            | $t_{DH}$           |                       | 23   |      |      | ns      |      |
| Latch pulse "H" pulse width               | $t_{WLPH}$         |                       | 30   |      |      | ns      |      |
| Shift clock rise to latch pulse rise time | $t_{LD}$           |                       | 0    |      |      | ns      |      |
| Shift clock fall to latch pulse fall time | $t_{SL}$           |                       | 50   |      |      | ns      |      |
| Latch pulse rise to shift clock rise time | $t_{LS}$           |                       | 30   |      |      | ns      |      |
| Latch pulse fall to shift clock fall time | $t_{LH}$           |                       | 30   |      |      | ns      |      |
| Enable setup time                         | $t_S$              |                       | 15   |      |      | ns      |      |
| Input signal rise time                    | $t_R$              |                       |      |      | 50   | ns      | 2    |
| Input signal fall time                    | $t_F$              |                       |      |      | 50   | ns      | 2    |
| DISPOFF removal time                      | $t_{SD}$           |                       | 100  |      |      | ns      |      |
| DISPOFF "L" pulse width                   | $t_{WDL}$          |                       | 1.2  |      |      | $\mu$ s |      |
| Output delay time (1)                     | $t_D$              | CL = 15 pF            |      |      | 41   | ns      |      |
| Output delay time (2)                     | $t_{PD1}, t_{PD2}$ | CL = 15 pF            |      |      | 1.2  | $\mu$ s |      |
| Output delay time (3)                     | $t_{PD3}$          | CL = 15 pF            |      |      | 1.2  | $\mu$ s |      |

NOTES:

1. Takes the cascade connection into consideration.
2.  $(t_{WCK} - t_{WCKH} - t_{WCKL})/2$  is maximum in the case of high speed operation.

(Segment Mode 3) (LGND =  $V_{SS} = 0$  V,  $V_{DD} = +3.0$  to  $+4.5$  V,  $V_0 = +15.0$  to  $+30.0$  V,  $T_{OPR} = -25$  to  $+85$  °C)

| PARAMETER                                 | SYMBOL             | CONDITIONS            | MIN. | TYP. | MAX. | UNIT    | NOTE |
|-------------------------------------------|--------------------|-----------------------|------|------|------|---------|------|
| Shift clock period                        | $t_{WCK}$          | $t_R, t_F \leq 10$ ns | 82   |      |      | ns      | 1    |
| Shift clock "H" pulse width               | $t_{WCKH}$         |                       | 28   |      |      | ns      |      |
| Shift clock "L" pulse width               | $t_{WCKL}$         |                       | 28   |      |      | ns      |      |
| Data setup time                           | $t_{DS}$           |                       | 20   |      |      | ns      |      |
| Data hold time                            | $t_{DH}$           |                       | 23   |      |      | ns      |      |
| Latch pulse "H" pulse width               | $t_{WLPH}$         |                       | 30   |      |      | ns      |      |
| Shift clock rise to latch pulse rise time | $t_{LD}$           |                       | 0    |      |      | ns      |      |
| Shift clock fall to latch pulse fall time | $t_{SL}$           |                       | 51   |      |      | ns      |      |
| Latch pulse rise to shift clock rise time | $t_{LS}$           |                       | 30   |      |      | ns      |      |
| Latch pulse fall to shift clock fall time | $t_{LH}$           |                       | 30   |      |      | ns      |      |
| Enable setup time                         | $t_S$              |                       | 15   |      |      | ns      |      |
| Input signal rise time                    | $t_R$              |                       |      |      | 50   | ns      | 2    |
| Input signal fall time                    | $t_F$              |                       |      |      | 50   | ns      | 2    |
| DISPOFF removal time                      | $t_{SD}$           |                       | 100  |      |      | ns      |      |
| DISPOFF "L" pulse width                   | $t_{WDL}$          |                       | 1.2  |      |      | $\mu$ s |      |
| Output delay time (1)                     | $t_D$              | CL = 15 pF            |      |      | 57   | ns      |      |
| Output delay time (2)                     | $t_{PD1}, t_{PD2}$ | CL = 15 pF            |      |      | 1.2  | $\mu$ s |      |
| Output delay time (3)                     | $t_{PD3}$          | CL = 15 pF            |      |      | 1.2  | $\mu$ s |      |

**NOTES:**

1. Takes the cascade connection into consideration.
2.  $(t_{WCK} - t_{WCKH} - t_{WCKL})/2$  is maximum in the case of high speed operation.

(Common Mode) (LGND =  $V_{SS} = 0$  V,  $V_{DD} = +2.5$  to  $+5.5$  V,  $V_0 = +15.0$  to  $+30.0$  V,  $T_{OPR} = -25$  to  $+85$  °C)

| PARAMETER                   | SYMBOL             | CONDITIONS                  | MIN. | TYP. | MAX. | UNIT    |
|-----------------------------|--------------------|-----------------------------|------|------|------|---------|
| Shift clock period          | $t_{WLP}$          | $t_R, t_F \leq 20$ ns       | 250  |      |      | ns      |
| Shift clock "H" pulse width | $t_{WLPH}$         | $V_{DD} = +5.0 \pm 0.5$ V   | 15   |      |      | ns      |
|                             |                    | $V_{DD} = +2.5$ to $+4.5$ V | 30   |      |      | ns      |
| Data setup time             | $t_{SU}$           |                             | 30   |      |      | ns      |
| Data hold time              | $t_H$              |                             | 50   |      |      | ns      |
| Input signal rise time      | $t_R$              |                             |      |      | 50   | ns      |
| Input signal fall time      | $t_F$              |                             |      |      | 50   | ns      |
| DISPOFF removal time        | $t_{SD}$           |                             | 100  |      |      | ns      |
| DISPOFF "L" pulse width     | $t_{WDL}$          |                             | 1.2  |      |      | $\mu$ s |
| Output delay time (1)       | $t_{DL}$           | CL = 15 pF                  |      |      | 200  | ns      |
| Output delay time (2)       | $t_{PD1}, t_{PD2}$ | CL = 15 pF                  |      |      | 1.2  | $\mu$ s |
| Output delay time (3)       | $t_{PD3}$          | CL = 15 pF                  |      |      | 1.2  | $\mu$ s |

### 10.3 Timing Chart of Segment Mode

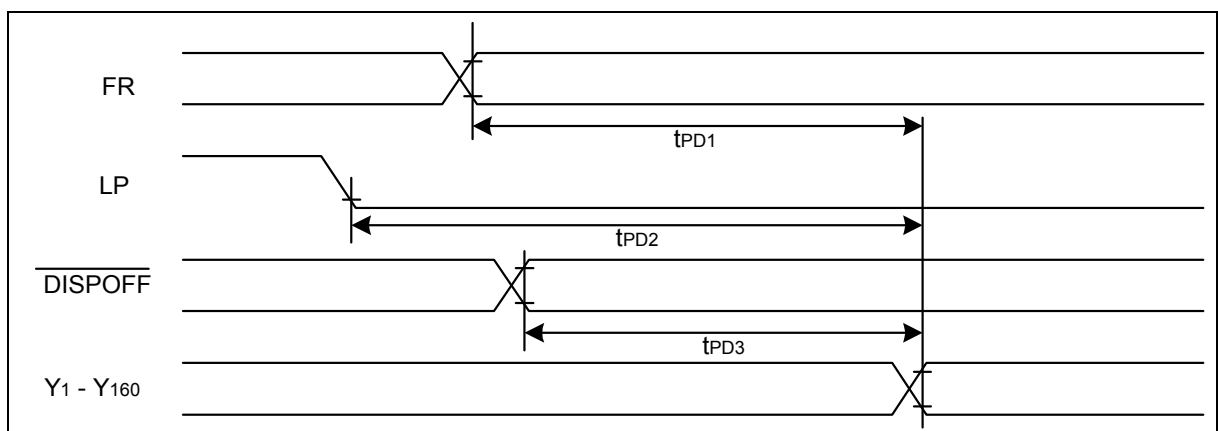
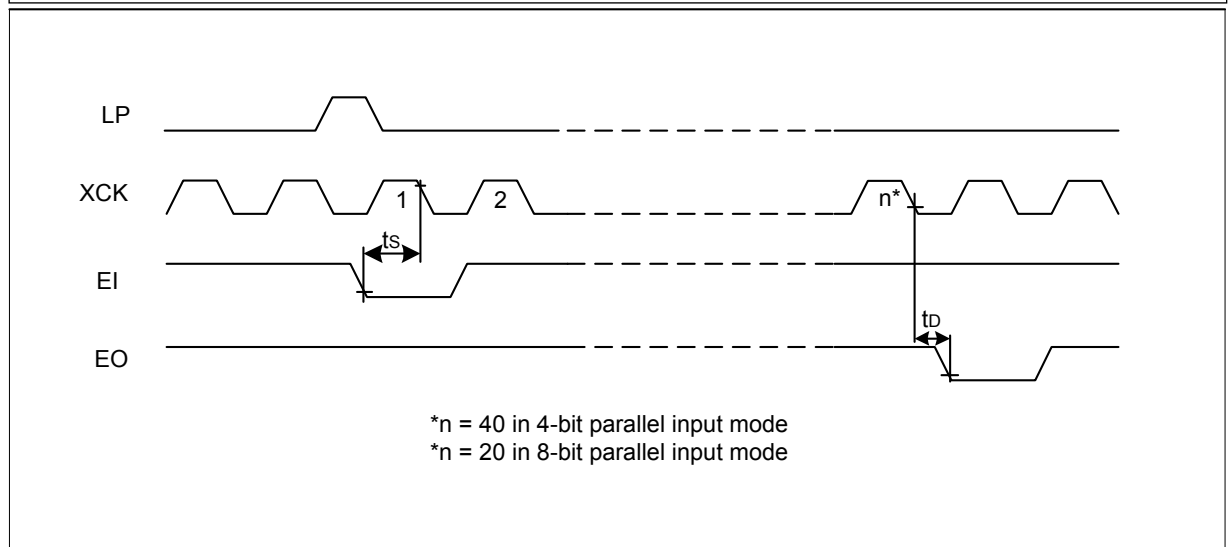
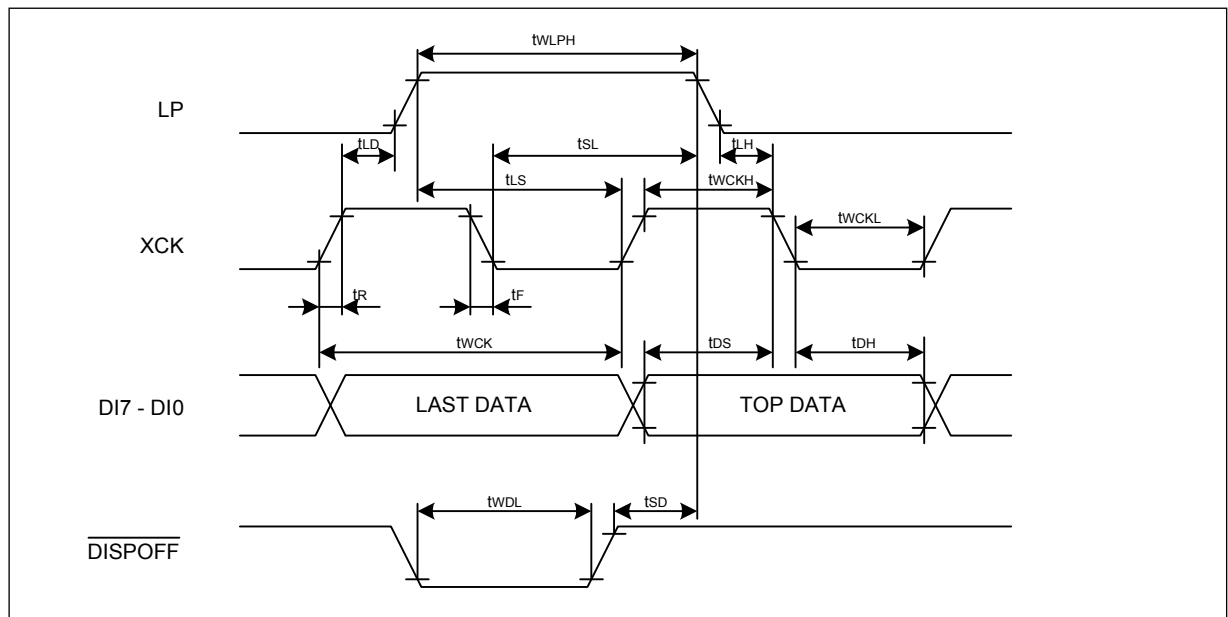
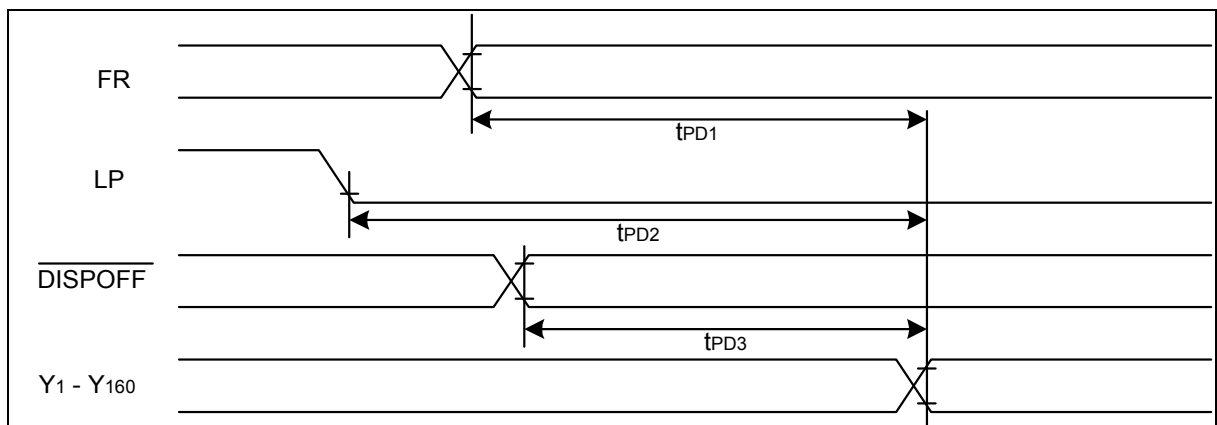
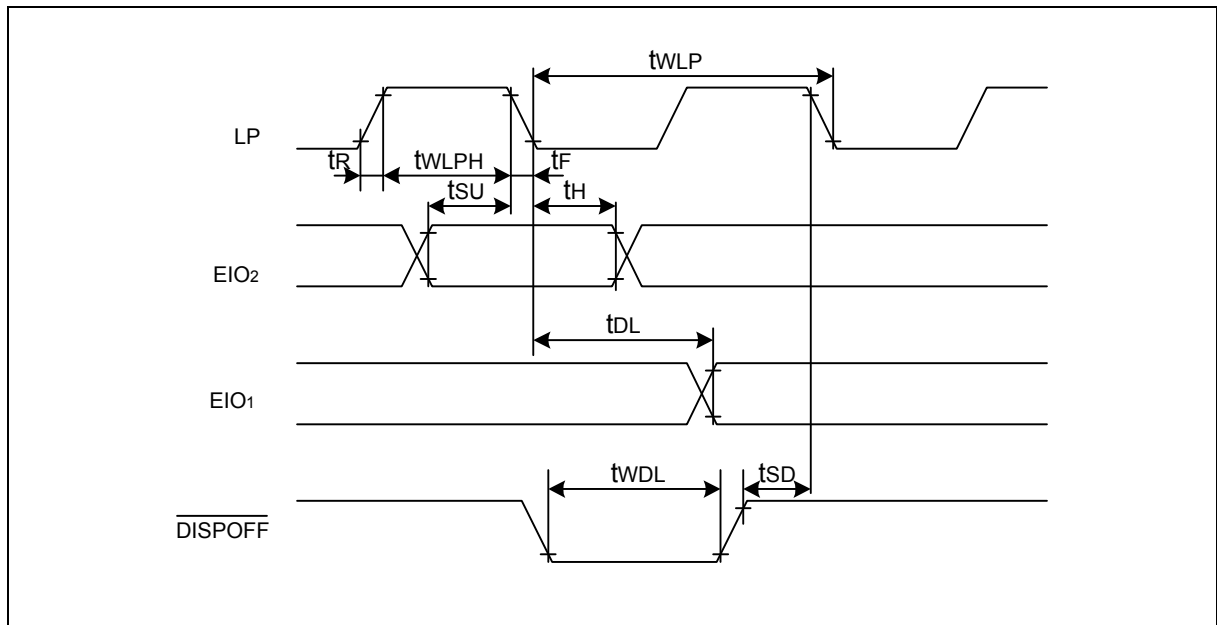


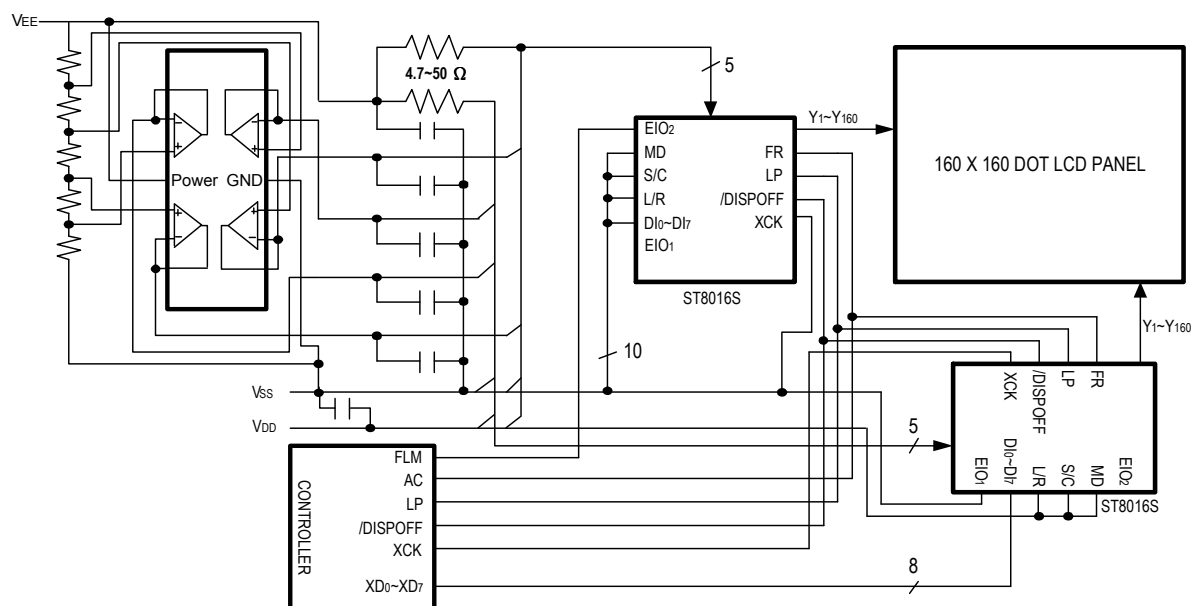
Fig. 8 Timing Characteristics (3)

## 10.4 Timing Chart of Common Mode

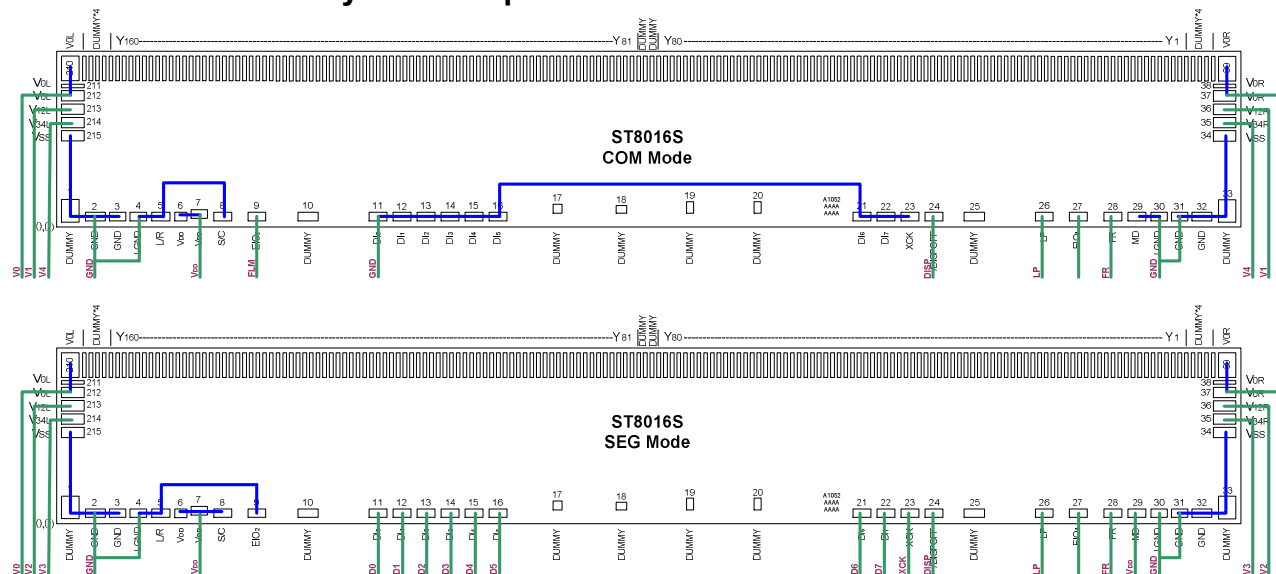


## 11. APPLICATION CIRCUIT

### 11.1 Application Circuit for Module



### 11.2 LCD Panel Layout Example



R1 : 4.7Ω ~ 50Ω

C1 : 0.1uF ~ 4.7uF

C2 : 0.1uF ~ 4.7uF

— Circuit on PCB

— Circuit on LCD

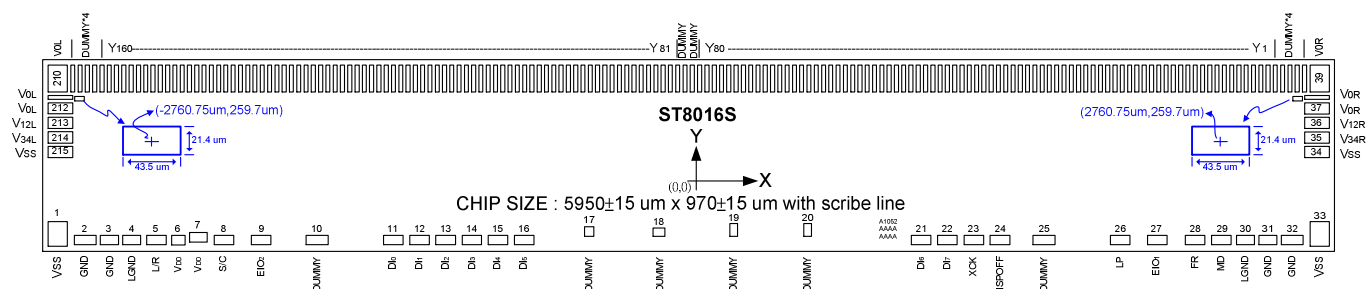
#### ITO layout Notices (for reference only)

1. We suggest the ITO resistor for LCD panel is about 15Ω/Square, and the resistor value is as smaller as better.
2. Among the interface pins, please to be sure the ITO resistor value of power pins are less than the following values that we suggest.

| Pin Name               | ITO Resistor Values Suggestion                            |
|------------------------|-----------------------------------------------------------|
| LGND, GND, VDD, VSS    | Less than 75Ω when VDD ≥ 3.0V, and the smaller the better |
| V0R, V0L               | Less than 150Ω, and the smaller the better                |
| V12R, V12L, V34R, V12L | Less than 250Ω, and the smaller the better                |

PS : Above resistor value test on 3" LCD panel.

# 12. PAD DIAGRAM



Note: Substrate should be connected to GND.

Unit: μm

| PIN# | Name             | X         | Y        | PIN# | Name             | X        | Y       |
|------|------------------|-----------|----------|------|------------------|----------|---------|
| 1    | V <sub>SS</sub>  | -2857.500 | -355.000 | 34   | V <sub>SS</sub>  | 2845.000 | 16.500  |
| 2    | GND              | -2733.000 | -383.100 | 35   | V <sub>34R</sub> | 2845.000 | 82.500  |
| 3    | GND              | -2622.850 | -383.150 | 36   | V <sub>12R</sub> | 2845.000 | 148.500 |
| 4    | LGND             | -2521.550 | -383.150 | 37   | V <sub>0R</sub>  | 2845.000 | 214.500 |
| 5    | L/R              | -2410.100 | -383.100 | 38   | V <sub>0R</sub>  | 2845.000 | 264.000 |
| 6    | V <sub>DD</sub>  | -2310.675 | -383.350 | 39   | V <sub>0R</sub>  | 2857.500 | 350.000 |
| 7    | V <sub>DD</sub>  | -2220.450 | -370.650 | 40   | DUMMY            | 2788.700 | 350.000 |
| 8    | S/C              | -2103.600 | -383.100 | 41   | DUMMY            | 2755.700 | 350.000 |
| 9    | EIO <sub>2</sub> | -1935.850 | -383.100 | 42   | DUMMY            | 2722.700 | 350.000 |
| 10   | DUMMY            | -1682.850 | -383.100 | 43   | DUMMY            | 2689.700 | 350.000 |
| 11   | DI <sub>0</sub>  | -1337.575 | -383.100 | 44   | Y1               | 2656.700 | 350.000 |
| 12   | DI <sub>1</sub>  | -1218.950 | -383.100 | 45   | Y2               | 2623.700 | 350.000 |
| 13   | DI <sub>2</sub>  | -1100.250 | -383.100 | 46   | Y3               | 2590.700 | 350.000 |
| 14   | DI <sub>3</sub>  | -981.550  | -383.100 | 47   | Y4               | 2557.700 | 350.000 |
| 15   | DI <sub>4</sub>  | -862.850  | -383.100 | 48   | Y5               | 2524.700 | 350.000 |
| 16   | DI <sub>5</sub>  | -744.150  | -383.100 | 49   | Y6               | 2491.700 | 350.000 |
| 17   | DUMMY            | -450.500  | -344.400 | 50   | Y7               | 2458.700 | 350.000 |
| 18   | DUMMY            | -134.775  | -347.675 | 51   | Y8               | 2425.700 | 350.000 |
| 19   | DUMMY            | 204.125   | -337.725 | 52   | Y9               | 2392.700 | 350.000 |
| 20   | DUMMY            | 538.725   | -337.725 | 53   | Y10              | 2359.700 | 350.000 |
| 21   | DI <sub>6</sub>  | 1053.350  | -383.100 | 54   | Y11              | 2326.700 | 350.000 |
| 22   | DI <sub>7</sub>  | 1172.050  | -383.100 | 55   | Y12              | 2293.700 | 350.000 |
| 23   | XCK              | 1291.050  | -383.100 | 56   | Y13              | 2260.700 | 350.000 |
| 24   | /DISPOFF         | 1409.750  | -383.100 | 57   | Y14              | 2227.700 | 350.000 |
| 25   | DUMMY            | 1608.650  | -383.100 | 58   | Y15              | 2194.700 | 350.000 |
| 26   | LP               | 1953.925  | -383.100 | 59   | Y16              | 2161.700 | 350.000 |
| 27   | EIO <sub>1</sub> | 2121.600  | -383.100 | 60   | Y17              | 2128.700 | 350.000 |
| 28   | FR               | 2293.000  | -383.100 | 61   | Y18              | 2095.700 | 350.000 |
| 29   | MD               | 2411.700  | -383.100 | 62   | Y19              | 2062.700 | 350.000 |
| 30   | LGND             | 2521.550  | -383.150 | 63   | Y20              | 2029.700 | 350.000 |
| 31   | GND              | 2622.850  | -383.150 | 64   | Y21              | 1996.700 | 350.000 |
| 32   | GND              | 2733.000  | -383.100 | 65   | Y22              | 1963.700 | 350.000 |
| 33   | V <sub>SS</sub>  | 2857.500  | -355.000 | 66   | Y23              | 1930.700 | 350.000 |

|     |     |          |         |     |       |           |         |
|-----|-----|----------|---------|-----|-------|-----------|---------|
| 67  | Y24 | 1897.700 | 350.000 | 114 | Y71   | 346.700   | 350.000 |
| 68  | Y25 | 1864.700 | 350.000 | 115 | Y72   | 313.700   | 350.000 |
| 69  | Y26 | 1831.700 | 350.000 | 116 | Y73   | 280.700   | 350.000 |
| 70  | Y27 | 1798.700 | 350.000 | 117 | Y74   | 247.700   | 350.000 |
| 71  | Y28 | 1765.700 | 350.000 | 118 | Y75   | 214.700   | 350.000 |
| 72  | Y29 | 1732.700 | 350.000 | 119 | Y76   | 181.700   | 350.000 |
| 73  | Y30 | 1699.700 | 350.000 | 120 | Y77   | 148.700   | 350.000 |
| 74  | Y31 | 1666.700 | 350.000 | 121 | Y78   | 115.700   | 350.000 |
| 75  | Y32 | 1633.700 | 350.000 | 122 | Y79   | 82.700    | 350.000 |
| 76  | Y33 | 1600.700 | 350.000 | 123 | Y80   | 49.700    | 350.000 |
| 77  | Y34 | 1567.700 | 350.000 | 124 | DUMMY | 16.700    | 350.000 |
| 78  | Y35 | 1534.700 | 350.000 | 125 | DUMMY | -16.700   | 350.000 |
| 79  | Y36 | 1501.700 | 350.000 | 126 | Y81   | -49.700   | 350.000 |
| 80  | Y37 | 1468.700 | 350.000 | 127 | Y82   | -82.700   | 350.000 |
| 81  | Y38 | 1435.700 | 350.000 | 128 | Y83   | -115.700  | 350.000 |
| 82  | Y39 | 1402.700 | 350.000 | 129 | Y84   | -148.700  | 350.000 |
| 83  | Y40 | 1369.700 | 350.000 | 130 | Y85   | -181.700  | 350.000 |
| 84  | Y41 | 1336.700 | 350.000 | 131 | Y86   | -214.700  | 350.000 |
| 85  | Y42 | 1303.700 | 350.000 | 132 | Y87   | -247.700  | 350.000 |
| 86  | Y43 | 1270.700 | 350.000 | 133 | Y88   | -280.700  | 350.000 |
| 87  | Y44 | 1237.700 | 350.000 | 134 | Y89   | -313.700  | 350.000 |
| 88  | Y45 | 1204.700 | 350.000 | 135 | Y90   | -346.700  | 350.000 |
| 89  | Y46 | 1171.700 | 350.000 | 136 | Y91   | -379.700  | 350.000 |
| 90  | Y47 | 1138.700 | 350.000 | 137 | Y92   | -412.700  | 350.000 |
| 91  | Y48 | 1105.700 | 350.000 | 138 | Y93   | -445.700  | 350.000 |
| 92  | Y49 | 1072.700 | 350.000 | 139 | Y94   | -478.700  | 350.000 |
| 93  | Y50 | 1039.700 | 350.000 | 140 | Y95   | -511.700  | 350.000 |
| 94  | Y51 | 1006.700 | 350.000 | 141 | Y96   | -544.700  | 350.000 |
| 95  | Y52 | 973.700  | 350.000 | 142 | Y97   | -577.700  | 350.000 |
| 96  | Y53 | 940.700  | 350.000 | 143 | Y98   | -610.700  | 350.000 |
| 97  | Y54 | 907.700  | 350.000 | 144 | Y99   | -643.700  | 350.000 |
| 98  | Y55 | 874.700  | 350.000 | 145 | Y100  | -676.700  | 350.000 |
| 99  | Y56 | 841.700  | 350.000 | 146 | Y101  | -709.700  | 350.000 |
| 100 | Y57 | 808.700  | 350.000 | 147 | Y102  | -742.700  | 350.000 |
| 101 | Y58 | 775.700  | 350.000 | 148 | Y103  | -775.700  | 350.000 |
| 102 | Y59 | 742.700  | 350.000 | 149 | Y104  | -808.700  | 350.000 |
| 103 | Y60 | 709.700  | 350.000 | 150 | Y105  | -841.700  | 350.000 |
| 104 | Y61 | 676.700  | 350.000 | 151 | Y106  | -874.700  | 350.000 |
| 105 | Y62 | 643.700  | 350.000 | 152 | Y107  | -907.700  | 350.000 |
| 106 | Y63 | 610.700  | 350.000 | 153 | Y108  | -940.700  | 350.000 |
| 107 | Y64 | 577.700  | 350.000 | 154 | Y109  | -973.700  | 350.000 |
| 108 | Y65 | 544.700  | 350.000 | 155 | Y110  | -1006.700 | 350.000 |
| 109 | Y66 | 511.700  | 350.000 | 156 | Y111  | -1039.700 | 350.000 |
| 110 | Y67 | 478.700  | 350.000 | 157 | Y112  | -1072.700 | 350.000 |
| 111 | Y68 | 445.700  | 350.000 | 158 | Y113  | -1105.700 | 350.000 |
| 112 | Y69 | 412.700  | 350.000 | 159 | Y114  | -1138.700 | 350.000 |
| 113 | Y70 | 379.700  | 350.000 | 160 | Y115  | -1171.700 | 350.000 |

|     |      |           |         |     |                  |           |         |
|-----|------|-----------|---------|-----|------------------|-----------|---------|
| 161 | Y116 | -1204.700 | 350.000 | 189 | Y144             | -2128.700 | 350.000 |
| 162 | Y117 | -1237.700 | 350.000 | 190 | Y145             | -2161.700 | 350.000 |
| 163 | Y118 | -1270.700 | 350.000 | 191 | Y146             | -2194.700 | 350.000 |
| 164 | Y119 | -1303.700 | 350.000 | 192 | Y147             | -2227.700 | 350.000 |
| 165 | Y120 | -1336.700 | 350.000 | 193 | Y148             | -2260.700 | 350.000 |
| 166 | Y121 | -1369.700 | 350.000 | 194 | Y149             | -2293.700 | 350.000 |
| 167 | Y122 | -1402.700 | 350.000 | 195 | Y150             | -2326.700 | 350.000 |
| 168 | Y123 | -1435.700 | 350.000 | 196 | Y151             | -2359.700 | 350.000 |
| 169 | Y124 | -1468.700 | 350.000 | 197 | Y152             | -2392.700 | 350.000 |
| 170 | Y125 | -1501.700 | 350.000 | 198 | Y153             | -2425.700 | 350.000 |
| 171 | Y126 | -1534.700 | 350.000 | 199 | Y154             | -2458.700 | 350.000 |
| 172 | Y127 | -1567.700 | 350.000 | 200 | Y155             | -2491.700 | 350.000 |
| 173 | Y128 | -1600.700 | 350.000 | 201 | Y156             | -2524.700 | 350.000 |
| 174 | Y129 | -1633.700 | 350.000 | 202 | Y157             | -2557.700 | 350.000 |
| 175 | Y130 | -1666.700 | 350.000 | 203 | Y158             | -2590.700 | 350.000 |
| 176 | Y131 | -1699.700 | 350.000 | 204 | Y159             | -2623.700 | 350.000 |
| 177 | Y132 | -1732.700 | 350.000 | 205 | Y160             | -2656.700 | 350.000 |
| 178 | Y133 | -1765.700 | 350.000 | 206 | DUMMY            | -2689.700 | 350.000 |
| 179 | Y134 | -1798.700 | 350.000 | 207 | DUMMY            | -2722.700 | 350.000 |
| 180 | Y135 | -1831.700 | 350.000 | 208 | DUMMY            | -2755.700 | 350.000 |
| 181 | Y136 | -1864.700 | 350.000 | 209 | DUMMY            | -2788.700 | 350.000 |
| 182 | Y137 | -1897.700 | 350.000 | 210 | V <sub>0L</sub>  | -2857.500 | 350.000 |
| 183 | Y138 | -1930.700 | 350.000 | 211 | V <sub>0L</sub>  | -2845.000 | 264.000 |
| 184 | Y139 | -1963.700 | 350.000 | 212 | V <sub>0L</sub>  | -2845.000 | 214.500 |
| 185 | Y140 | -1996.700 | 350.000 | 213 | V <sub>12L</sub> | -2845.000 | 148.500 |
| 186 | Y141 | -2029.700 | 350.000 | 214 | V <sub>34L</sub> | -2845.000 | 82.500  |
| 187 | Y142 | -2062.700 | 350.000 | 215 | V <sub>SS</sub>  | -2845.000 | 16.500  |
| 188 | Y143 | -2095.700 | 350.000 |     |                  |           |         |

## 12.1 Gold Bump size (unit: $\mu\text{m}$ )

| Pad No.                 | X      | Y      | Area ( $\mu\text{m}^2$ ) |
|-------------------------|--------|--------|--------------------------|
| 1,33                    | 87.00  | 112.00 | 9744.0000                |
| 6                       | 59.75  | 42.90  | 2563.2750                |
| 7                       | 80.70  | 42.40  | 3421.6800                |
| 2,32                    | 99.00  | 42.40  | 4197.6000                |
| 3,4,30,31               | 81.30  | 42.30  | 3438.9900                |
| 5,8,9,12~16,21~24,27~29 | 88.70  | 42.40  | 3760.8800                |
| 10,25                   | 100.20 | 42.40  | 4248.4800                |
| 11,26                   | 88.55  | 42.40  | 3754.5200                |
| 17                      | 43.30  | 44.40  | 1922.5200                |
| 18                      | 52.85  | 37.85  | 2000.3725                |
| 19,20                   | 34.65  | 57.75  | 2001.0375                |
| 40~209                  | 18.00  | 122.00 | 2196.0000                |
| 38,211                  | 112.00 | 18.00  | 2016.0000                |
| 39,210                  | 87.00  | 122.00 | 10614.0000               |
| 34~37,212~215           | 112.00 | 51.00  | 5712.0000                |

Wafer Thickness =  $480.0 \pm 20 \mu\text{m}$ , Bump pad height (pad 1~215) =  $15 \mu\text{m}$ , strength=30g

### 13. APPLICATION NOTE(REFERENCE ONLY)

- 13.1 Adjust V1 and V4 voltage to keep the  $V0-V1 = V4-VSS$  relation to get better display quality. The  $(V0-V1)-(V4-VSS)$  value had better less than 100mV.
- 13.2 Add 0.1uF high frequency by-pass capacitor to filter the noise on V0~V4 to VSS.
- 13.3 When OP follower circuit is used, please be sure the OP power is higher than V0 at least 1.5V.
- 13.4 EIO1 and EIO2 is enable pin for driver, please pay attention to the distance to avoid noise when cascade function is used. Two chip connecting distance is as shorter as better.

## 14. REVISION

| REVISION | DESCRIPTION                                                                                                                                 | PAGE     | DATE       |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------|----------|------------|
| 0.10     | First release                                                                                                                               | 1-25     | 2005/8/4   |
| 0.11     | Delete TCP information                                                                                                                      | 1-25     | 2005/9/8   |
| 0.12     | Add LGND definition, and re-define the pin function                                                                                         | 1-25     | 2005/11/22 |
| 0.13     | Modify suggestion resistor value for V0 and bond pad height to 18um.<br>Add alignment mark data and LCD Panel Layout Example.               | 21-22    | 2006/4/4   |
| 0.14     | Modify LCD panel layout example S/C of COM to connect to LGND, and add the ITO resistor value suggestion.                                   | 21       | 2006/5/23  |
| 0.15     | Modify the center of pad coordinate to the IC center.                                                                                       | 22-24    | 2006/5/30  |
| 0.16     | Modify the Bump pad height and add wafer thickness.                                                                                         | 24       | 2006/6/7   |
| 0.17     | Modify all Vss for logic setting pins to LGND                                                                                               | 21-24    | 2006/7/21  |
| 0.18     | Modify Description of LGND                                                                                                                  | 1-25     | 2006/7/21  |
| 0.19     | Change Sitronix Logo and Modify description of LGND for COM mode                                                                            | 1-25     | 2006/7/21  |
| 0.20     | Modify arrangement                                                                                                                          | 1-25     | 2006/8/3   |
| 0.21     | Modify Chip size and thickness with scribe line<br>Modify "ABSOLUTE MAXIMUM RATINGS" max value<br>Modify "Output resistance" test condition | 15,22,24 | 2006/10/26 |
| 0.22     | Modify all the data about absolute max voltage and recommend max voltage                                                                    | 2,16-18  | 2007/5/25  |
| 0.23     | Modify the ITO resistor value suggestion<br>Add application note                                                                            | 21,26    | 2008/5/05  |
| 0.24     | Modify LCD Panel Layout Example                                                                                                             | 21       | 2009/10/01 |

The above information is the exclusive intellectual property of Sitronix Technology Corp. and shall not be disclosed, distributed or reproduced without permission from Sitronix.