# FastEdge™ Series
# CY2PP3210

# Dual 1:5 Differential Clock/Data Fanout Buffer

## Features

- **Dual sets of five ECL/PECL differential outputs**
- **Two ECL/PECL differential inputs**
- **Hot-swappable/-insertable**
- **50 ps output-to-output skew**
- **150 ps device-to-device skew**
- **500 ps propagation delay (typical)**
- **0.8 ps RMS period jitter (max.)**
- **1.5 GHz Operation (2.2 GHz max. toggle frequency)**
- **PECL mode supply range: $V_{CC}$ = 2.5V± 5% to 3.3V±5% with $V_{EE}$ = 0V**
- **ECL mode supply range: $V_{EE}$ = –2.5V± 5% to –3.3V±5% with $V_{CC}$ = 0V**
- **Industrial temperature range: –40°C to 85°C**
- **32-pin 1.4-mm TQFP package**
- **Temperature compensation like 100K ECL**
- **Pin compatible with MC100ES6210**

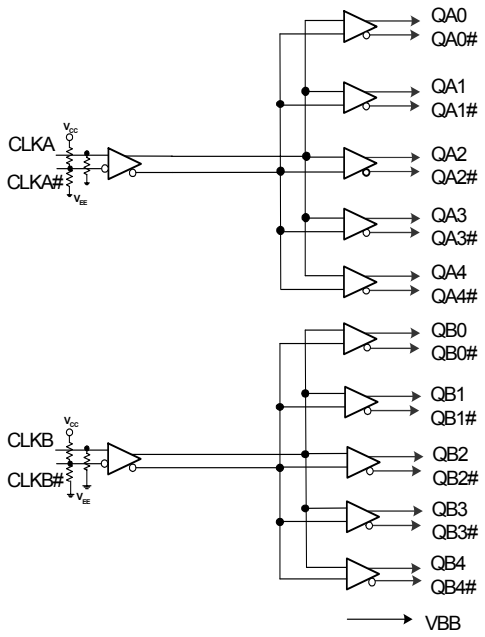
## Functional Description

The CY2PP3210 is a low-skew, low propagation delay dual 1-to-5 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on SiGe technology and has a fully differential internal architecture that is optimized to achieve low signal skews at operating frequencies of up to 1.5 GHz.

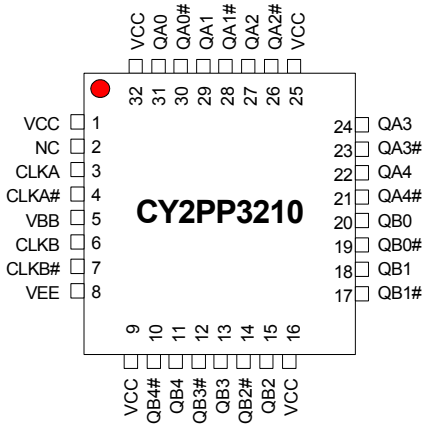
The device features two differential input paths that are differential internally. The CY2PP3210 may function not only as a differential clock buffer but also as a signal-level translator and fanout distributing a single-ended signal. An external bias pin, VBB, is provided for this purpose. In such an application, the VBB pin should be connected to either one of the CLKA# or CLKB# inputs and bypassed to ground via a 0.01-μF capacitor. Traditionally, in ECL, it is used to provide the reference level to a receiving single-ended input that might have a differential bias point.

Since the CY2PP3210 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high frequency, high precision clocks across back-planes and boards in communication systems. Furthermore, advanced circuit design schemes, such as internal temperature compensation, ensure that the CY2PP3210 delivers consistent performance over various platforms.

## Block Diagram




## Pin Configuration



## Pin Definitions[1, 2, 3]

| Pin | Name | I/O[1] | Type | Description |
|---|---|---|---|---|
| 2 | NC | | | **No connect.** |
| 3 | CLKA, | I,PD | ECL/PECL | **ECL/PECL Differential Input Clocks.** |
| 4 | CLKA# | I,PD/PU | ECL/PECL | **ECL/PECL Differential Input Clocks.** |
| 5 | VBB[3] | O | Bias | **Reference Voltage Output.** |
| 6 | CLKB, | I,PD | ECL/PECL | **ECL/PECL Differential Input Clocks.** |
| 7 | CLKB# | I,PD/PU | ECL/PECL | **ECL/PECL Differential Input Clocks.** |
| 8 | VEE[2] | –PWR | Power | **Negative Supply.** |
| 1,9,16,25,32 | VCC | +PWR | Power | **Positive Supply.** |
| 31,29,27,24,22 | QA(0:4) | O | ECL/PECL | **True output** |
| 30,28,26,23,21 | QA#(0:4) | O | ECL/PECL | **Complement output** |
| 20,18,15,13,11 | QB(0:4) | O | ECL/PECL | **True output** |
| 19,17,14,12,10 | QB#(0:4) | O | ECL/PECL | **Complement output** |

## Governing Agencies

The following agencies provide specifications that apply to the CY2PP3210. The agency name and relevant specification is listed below in *Table 2*.

**Table 1.**

| Agency Name | Specification |
|---|---|
| JEDEC | JESD 020B (MSL)<br>JESD 51 (Theta JA)<br>JESD 8–2 (ECL)<br>JESD 65–B (skew,jitter) |
| Mil-Spec | 883E Method 1012.1 (Thermal Theta JC) |

**Notes:**
1. In the I/O column, the following notation is used: I for Input, O for Output, PD for Pull-Down, PU for Pull-Up, and PWR for Power
2. In ECL mode (negative power supply mode), $V_{EE}$ is either –3.3V or –2.5V and $V_{CC}$ is connected to GND (0V). In PECL mode (positive power supply mode), $V_{EE}$ is connected to GND (0V) and $V_{CC}$ is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply ($V_{CC}$) and are between $V_{CC}$ and $V_{EE}$.
3. $V_{BB}$ is available for use for single-ended bias mode for |3.3V| supplies (not |2.5V|).

## Absolute Maximum Ratings

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive Supply Voltage | Non-Functional | –0.3 | 4.6 | V |
| $V_{EE}$ | Negative Supply Voltage | Non-Functional | -4.6 | 0.3 | V |
| $T_S$ | Temperature, Storage | Non-Functional | –65 | +150 | °C |
| $T_J$ | Temperature, Junction | Non-Functional | | 150 | °C |
| $ESD_h$ | ESD Protection | Human Body Model | 2000 | | V |
| $M_{SL}$ | Moisture Sensitivity Level | | 3 | | N.A. |
| Gate Count | Total Number of Used Gates | Assembled Die | 50 | | gates |

**Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

## Operating Conditions

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{BB}$ | Output Reference Current | Relative to $V_{BB}$ | – | \|200\| | uA |
| $LU_I$ | Latch Up Immunity | Functional, typical | 100 | | mA |
| $T_A$ | Temperature, Operating Ambient | Functional | –40 | +85 | °C |
| $Ø_{Jc}$ | Dissipation, Junction to Case | Functional | 29[4] | | °C/W |
| $Ø_{Ja}$ | Dissipation, Junction to Ambient | Functional | 76[4] | | °C/W |
| $I_{EE}$ | Maximum Quiescent Supply Current | $V_{EE}$ pin[5] | – | 130 | mA |
| $C_{IN}$ | Input pin capacitance | | – | 3 | pF |
| $L_{IN}$ | Pin Inductance | | | 1 | nH |
| $V_{IN}$ | Input Voltage | Relative to $V_{CC}$[6] | –0.3 | $V_{CC}$ + 0.3 | V |
| $V_{TT}$ | Output Termination Voltage | Relative to $V_{CC}$[6] | $V_{CC}$ – 2 | | V |
| $V_{OUT}$ | Output Voltage | Relative to $V_{CC}$[6] | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current[7] | $V_{IN} = V_{IL}$, or $V_{IN} = V_{IH}$ | | I150I | uA |

## PECL DC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Operating Voltage | 2.5V ± 5%, $V_{EE}$ = 0.0V<br>3.3V ± 5%, $V_{EE}$ = 0.0V | 2.375<br>3.135 | 2.625<br>3.465 | V<br>V |
| $V_{CMR}$ | Differential Cross Point Voltage[8] | Differential operation | 1.2 | $V_{CC}$ | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –30 mA[9] | $V_{CC}$ – 1.25 | $V_{CC}$ – 0.7 | V |
| $V_{OL}$ | Output Low Voltage<br>$V_{CC}$ = 3.3V ± 5%<br>$V_{CC}$ = 2.5V ± 5% | $I_{OL}$ = –5 mA[9] | <br>$V_{CC}$ – 1.995<br>$V_{CC}$ –1.995 | <br>$V_{CC}$ – 1.5<br>$V_{CC}$ – 1.3 | <br>V<br>V |
| $V_{IH}$ | Input Voltage, High | Single-ended operation | $V_{CC}$ – 1.165 | $V_{CC}$ – 0.880 [10] | V |
| $V_{IL}$ | Input Voltage, Low | Single-ended operation | $V_{CC}$ – 1.945 [10] | $V_{CC}$ – 1.625 | V |
| $V_{BB}$[3] | Output Reference Voltage | Relative to $V_{CC}$[6] | $V_{CC}$ – 1.620 | $V_{CC}$ – 1.220 | V |

**Notes:**
4. Theta JA EIA JEDEC 51 test board conditions (typical value); Theta JC 883E Method 1012.1
5. Power Calculation: $V_{CC} * I_{EE} + 0.5 (I_{OH} + I_{OL}) (V_{OH} – V_{OL})$ (number of differential outputs used); $I_{EE}$ does not include current going off chip.
6. where $V_{CC}$ is 3.3V±5% or 2.5V±5%
7. Inputs have internal pull-up/pull-down or biasing resistors which affect the input current.
8. Refer to Figure 1
9. Equivalent to a termination of 50Ω to VTT. $I_{OHMIN}=(V_{OHMIN}-V_{TT})/50$; $I_{OHMAX}=(V_{OHMAX}-V_{TT})/50$; $I_{OLMIN}=(V_{OLMIN}-V_{TT})/50$; $I_{OLMAX}=(V_{OLMAX}-V_{TT})/50$;
10. $V_{IL}$ will operate down to $V_{EE}$; $V_{IH}$ will operate up to $V_{CC}$

## ECL DC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{EE}$ | Negative Power Supply | –2.5V ± 5%, $V_{CC}$ = 0.0V<br>–3.3V ± 5%, $V_{CC}$ = 0.0V | –2.625<br>–3.465 | –2.375<br>–3.135 | V |
| $V_{CMR}$ | Differential cross point voltage[8] | Differential operation | $V_{EE}$ + 1.2 | 0V | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –30 mA[9] | –1.25 | –0.7 | V |
| $V_{OL}$ | Output Low Voltage<br>$V_{EE}$ = –3.3V ± 5%<br>$V_{EE}$ = –2.5V ± 5% | $I_{OL}$ = –5 mA[9] | <br>–1.995<br>–1.995 | <br>–1.5<br>–1.3 | V |
| $V_{IH}$ | Input Voltage, High | Single-ended operation | –1.165 | –0.880 [10] | V |
| $V_{IL}$ | Input Voltage, Low | Single-ended operation | –1.945 [10] | –1.625 | V |
| $V_{BB}$[3] | Output Reference Voltage | | – 1.620 | – 1.220 | V |

## AC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{PP}$ | Differential Input Voltage[8] | Differential operation | 0.1 | 1.3 | V |
| $F_{CLK}$ | Input Frequency | 50% duty cycle Standard load | | 1.5 | GHz |
| $T_{PD}$ | Propagation Delay CLKA or CLKB to Output pair | 660 MHz [11] | 280 | 750 | ps |
| Vo | Output Voltage (peak-to-peak; see Figure 2) | < 1 GHz | 0.375 | – | V |
| $V_{CMRO}$ | Output Common Voltage Range (typ.) | | $V_{CC}$ – 1.425 | | V |
| $tsk_{(0)}$ | Output-to-output Skew | 660 MHz [11], See Figure 3 | – | 50 | ps |
| $tsk_{(PP)}$ | Part-to-Part Output Skew | 660 MHz [11] | – | 150 | ps |
| $T_{PER}$ | Output Period Jitter (rms)[12] | 660 MHz [11] | – | 0.8 | ps |
| $tsk_{(P)}$ | Output Pulse Skew[13] | 660 MHz [11], See Figure 3 | – | 50 | ps |
| $T_R$,$T_F$ | Output Rise/Fall Time (see Figure 2) | 660 MHz 50% duty cycle Differential 20% to 80% | 0.08 | 0.3 | ns |

## Timing Definitions

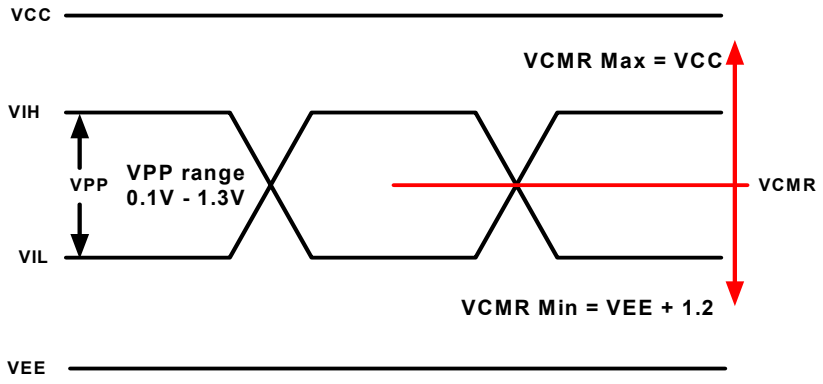



**Figure 1. PECL/ECL Input Waveform Definitions**

**Notes:**
11. 50% duty cycle; standard load; differential operation
12. For 3.3V supplies. Jitter measured differentially using an Agilent 8133A Pulse Generator with an 8500A LeCroy Wavemaster Oscilloscope using at least 10,000 data points
13. Output pulse skew is the absolute difference of the propagation delay times: $| t_{PLH} – t_{PHL} |$.

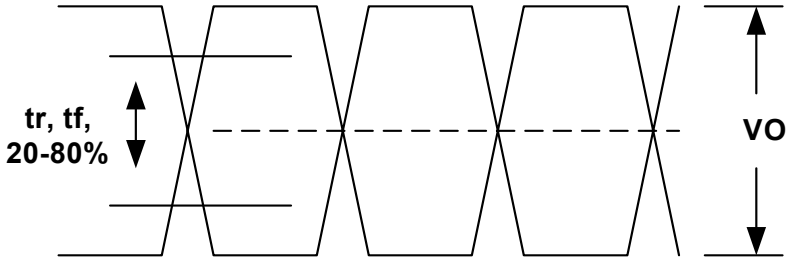



**Figure 2. ECL/LVPECL Output**

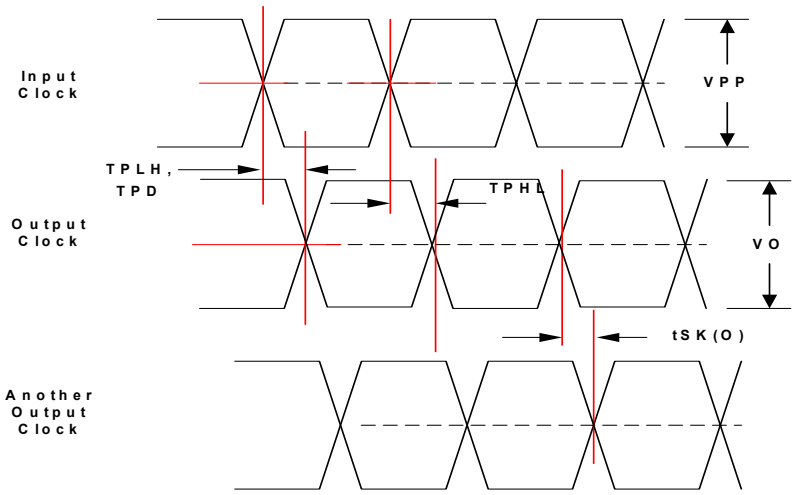



**Figure 3. Propagation Delay ($T_{PD}$), output pulse skew ($|t_{PLH}-t_{PHL}|$), and output-to-output skew ($t_{SK(O)}$) for both CLKA or CLKB to Output Pair, PECL/ECL to PECL/ECL**

## Test Configuration

Standard test load using a differential pulse generator and differential measurement instrument.

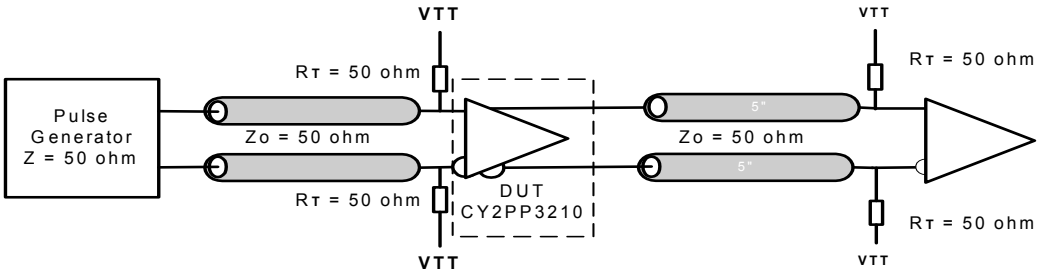



**Figure 4. CY2PP318 AC Test Reference**

## Applications Information

### Termination Examples

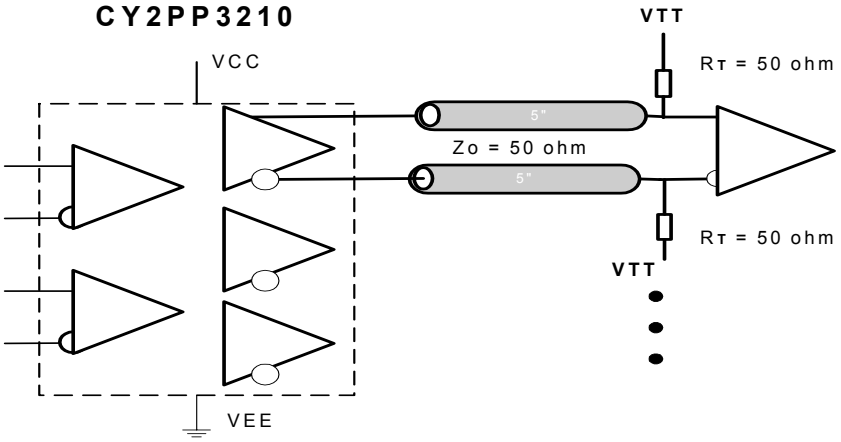



**Figure 5. Standard LVPECL – PECL Output Termination**

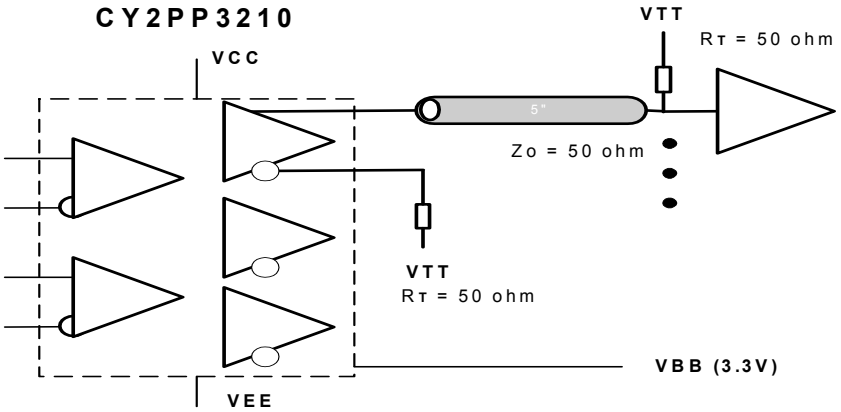



**Figure 6. Driving a PECL/ECL Single-ended Input**

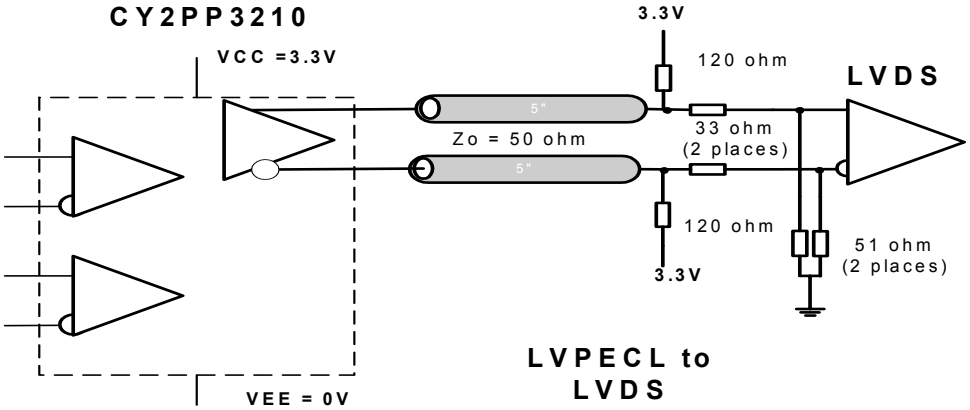
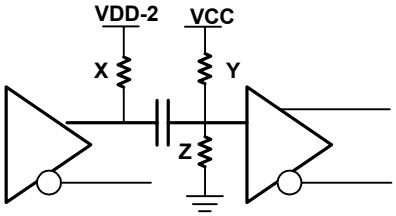



**Figure 7. Low-voltage Positive Emitter-coupled Logic (LVPECL) to a Low-voltage Differential Signaling (LVDS) Interface**




**One output is shown for clarity**

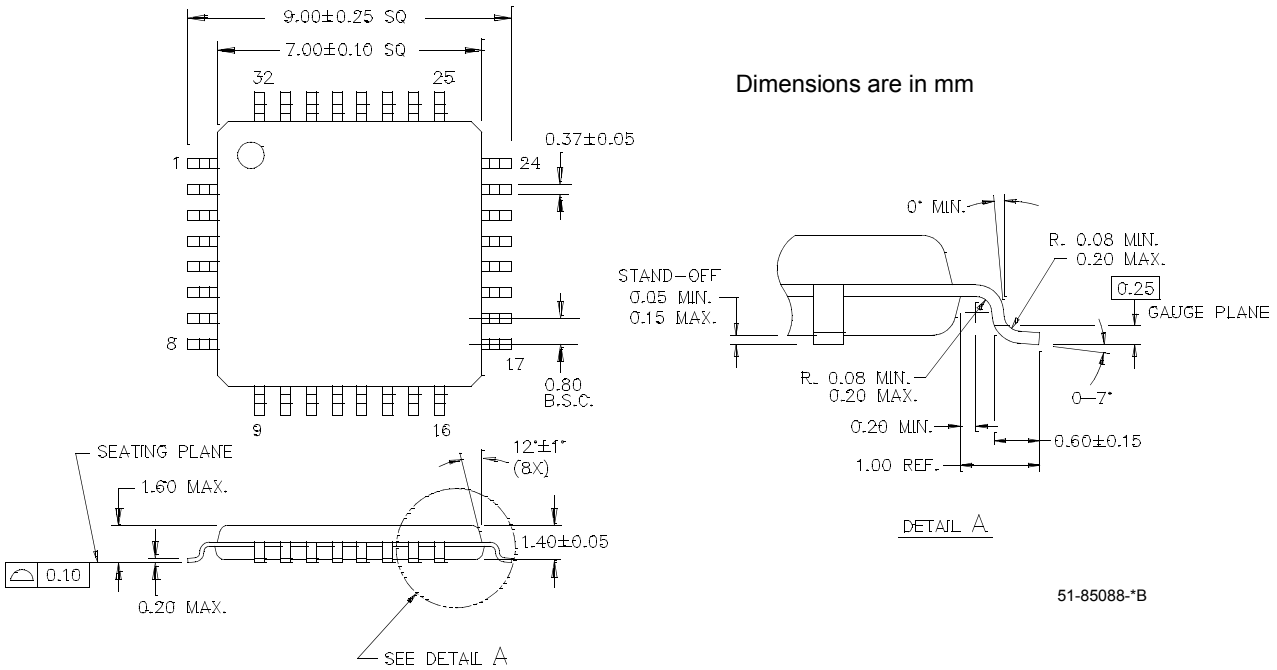
**Figure 8. Termination for LVPECL to HTSL interface for VCC=2.5V would use X=50 Ohms, Y=2300 Ohms, and Z=1000 Ohms. See application note titled, "PECL Translation, SAW Oscillators, and Specs" for other signalling standards and supplies.**

## Ordering Information

| Part Number | Package Type | Product Flow |
|---|---|---|
| CY2PP3210AI | 32-pin TQFP | Industrial, –40° to 85°C |
| CY2PP3210AIT | 32-pin TQFP – Tape and Reel | Industrial, –40° to 85°C |

## Package Drawing and Dimension

**32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.4 mm A32.14**




FastEdge is a trademark of Cypress Semiconductor. All product and company names mentioned in this document are the trademarks of their respective holders.


© Cypress Semiconductor Corporation, 2004. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

## Document History Page

| Document Title: CY2PP3210 FastEdge™ Series Dual 1:5 Differential Clock/Data Fanout Buffer<br>Document Number: 38-07508 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 122396 | 02/12/03 | RGL | New Data Sheet |
| *A | 125458 | 04/17/03 | RGL | Corrected pins 26 to 31 from Q2#, Q2, Q1#, Q1, Q0#, Q0 to QA2#, QA2, QA1#, QA1,QA0#, QA0 in the Pin Configuration diagram<br>Changed pins 9, 16, 25, 32 from VCC to VCCO<br>Changed the title to FastEdge™ Series Dual 1:5 Differential Clock/Data Fanout Buffer |
| *B | 229370 | See ECN | RGL | Supplied data to all the TBD's to match the device |
| *C | 247616 | See ECN | RGL/GGK | Changed $V_{OH}$ and $V_{OL}$ to match the Char Data |