

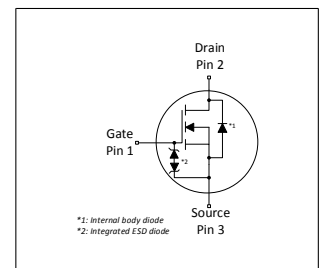
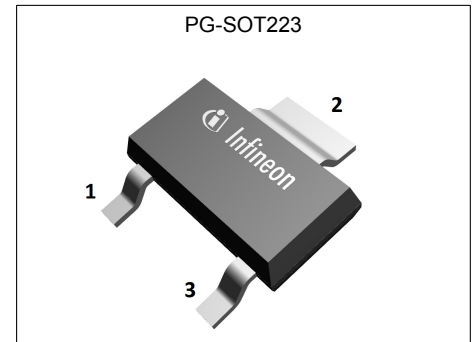
MOSFET

600V CoolMOS™ PFD7 SJ Power Device

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

The latest CoolMOS™ PFD7 is an optimized platform tailored to target cost sensitive applications in consumer markets such as charger, adapter, motor drive, lighting, etc.

The new series provides all the benefits of a fast switching Superjunction MOSFET, combined with an excellent price/performance ratio and state of the art ease-of-use level. The technology meets highest efficiency standards and supports high power density, enabling customers going towards very slim designs.



Features

- Extremely low losses due to very low FOM $R_{DS(on)} * Q_g$ and $R_{DS(on)} * E_{oss}$
- Low switching losses E_{oss} , excellent thermal behavior
- Fast body diode
- Wide range portfolio of $R_{DS(on)}$ and package variations
- Integrated zener diode

Benefits

- Enables high power density designs and small form factors
- Enables efficiency gains at higher switching frequencies
- Excellent commutation ruggedness
- Easy to select right parts and optimize the design
- High ESD ruggedness

Potential applications

Recommended for ZVS topologies used in high density chargers, adapters, lighting and motor drives applications, etc.

Product validation

Qualified according to JEDEC Standard

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	1500	mΩ
$Q_{g,typ}$	4.6	nC
$I_{D,pulse}$	6.0	A
$E_{oss} @ 400V$	0.5	μJ
Body diode di_f/dt	1300	A/μs
ESD Class (HBM)	2	-

Type / Ordering Code	Package	Marking	Related Links
IPN60R1K5PFD7S	PG-SOT223	60S1K5D7	see Appendix A



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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	3.6 2.2	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	6.0	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	7	mJ	$I_D=0.7\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.04	mJ	$I_D=0.7\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	0.7	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	6	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	-	Ncm	-
Continuous diode forward current ¹⁾	I_S	-	-	3.6	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	6.0	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	70	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 2.5\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di _F /dt	-	-	1300	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 2.5\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$; DPAK / IPAK equivalent.

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_θ

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - solder point	R_{thJS}	-	-	19.73	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	160	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	75	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	$V_{DS}=V_{GS}, I_D=0.04mA$
Zero gate voltage drain current ¹⁾	I_{DSS}	-	-	1	μA	$V_{DS}=600V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=600V, V_{GS}=0V, T_j=125^\circ C$
Gate-source leakage current	I_{GSS}	-	-	1000	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.230 2.893	1.500	Ω	$V_{GS}=10V, I_D=0.7A, T_j=25^\circ C$ $V_{GS}=10V, I_D=0.7A, T_j=150^\circ C$
Gate resistance	R_G	-	11.0	-	Ω	$f=1MHz, \text{open drain}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	169	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Output capacitance	C_{oss}	-	4	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Effective output capacitance, energy related ²⁾	$C_{o(er)}$	-	7	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related ³⁾	$C_{o(tr)}$	-	59	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	6.4	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=0.7A,$ $R_G=10.2\Omega; \text{see table 9}$
Rise time	t_r	-	8	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=0.7A,$ $R_G=10.2\Omega; \text{see table 9}$
Turn-off delay time	$t_{d(off)}$	-	41.5	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=0.7A,$ $R_G=10.2\Omega; \text{see table 9}$
Fall time	t_f	-	75	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=0.7A,$ $R_G=10.2\Omega; \text{see table 9}$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	1.0	-	nC	$V_{DD}=400V, I_D=0.7A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	Q_{gd}	-	1.8	-	nC	$V_{DD}=400V, I_D=0.7A, V_{GS}=0 \text{ to } 10V$
Gate charge total	Q_g	-	4.6	-	nC	$V_{DD}=400V, I_D=0.7A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	5.6	-	V	$V_{DD}=400V, I_D=0.7A, V_{GS}=0 \text{ to } 10V$

¹⁾ Maximum specification is defined by calculated six sigma upper confidence bound

²⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

³⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1.0	-	V	$V_{GS}=0V, I_F=0.7A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	40	59	ns	$V_R=400V, I_F=0.7A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	0.06	0.12	μC	$V_R=400V, I_F=0.7A, di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	2.8	-	A	$V_R=400V, I_F=0.7A, di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

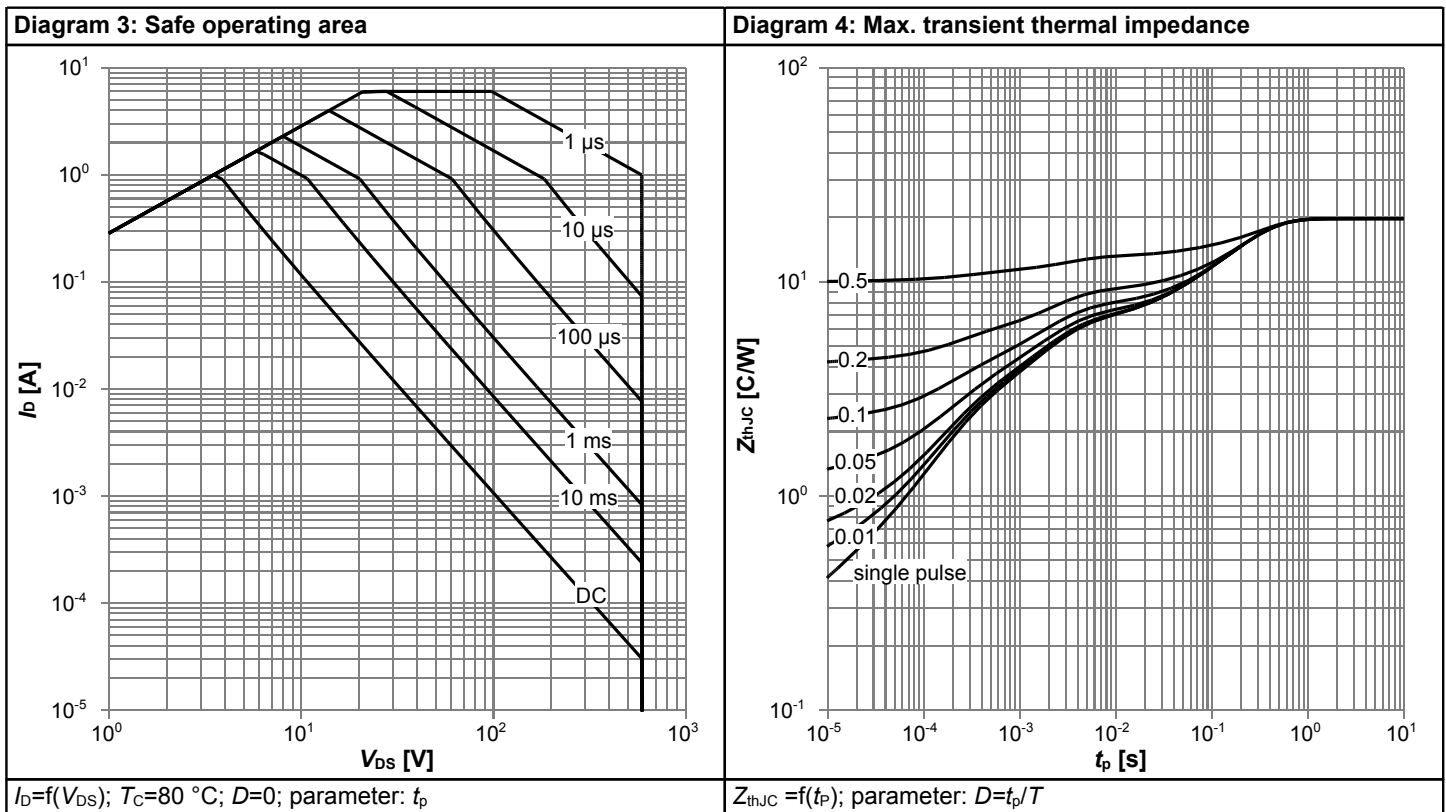
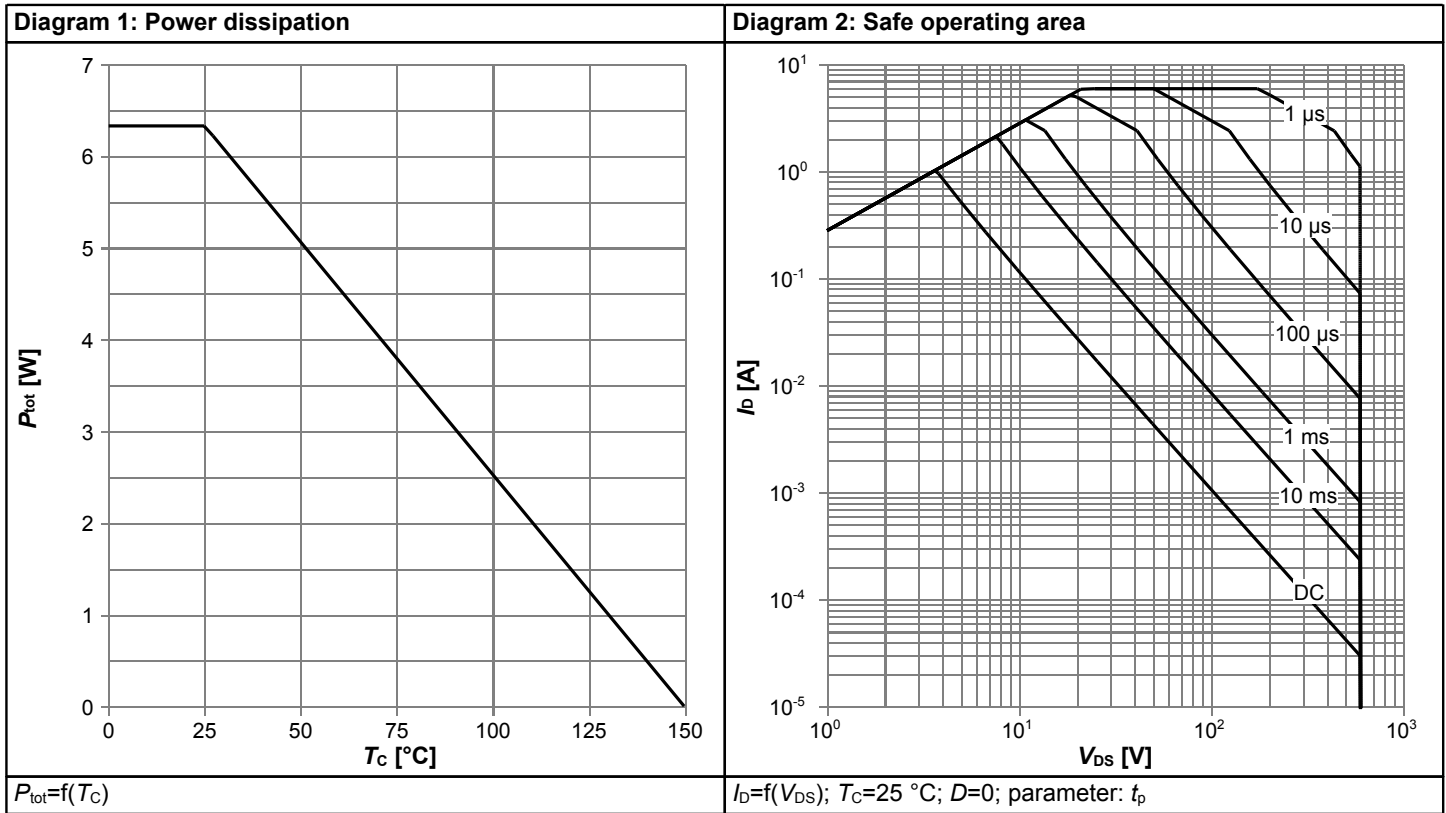
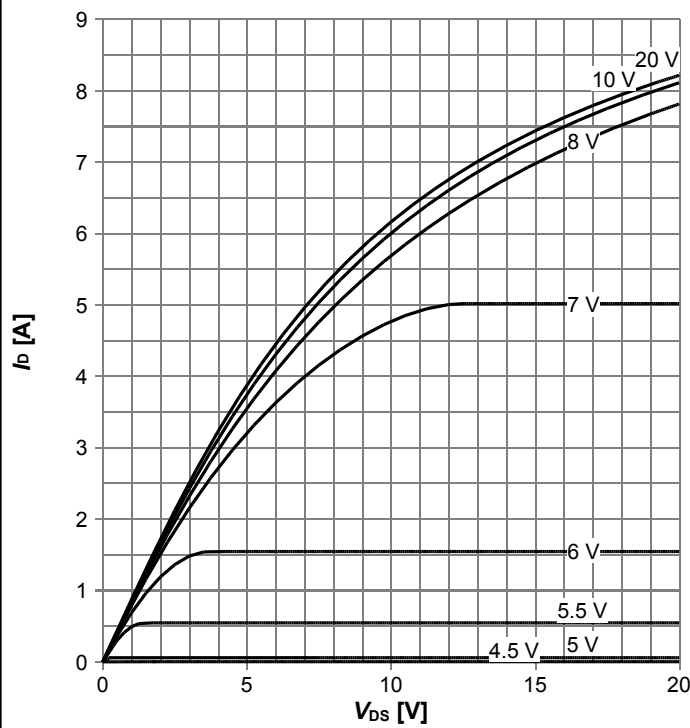
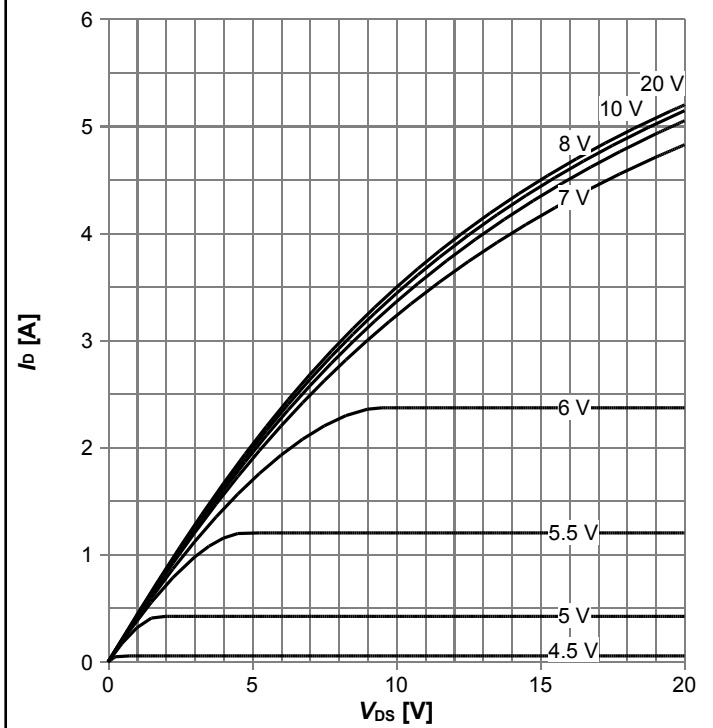


Diagram 5: Typ. output characteristics



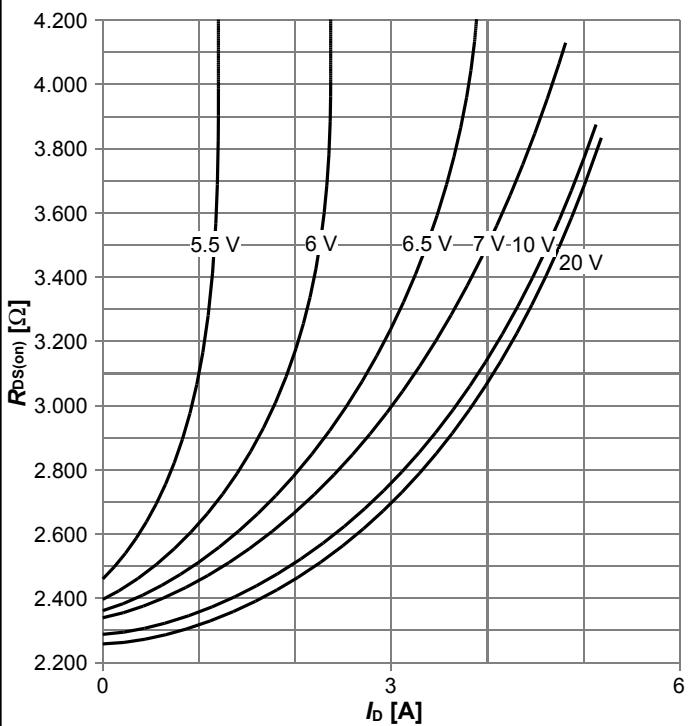
$I_D=f(V_{DS})$; $T_j=25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



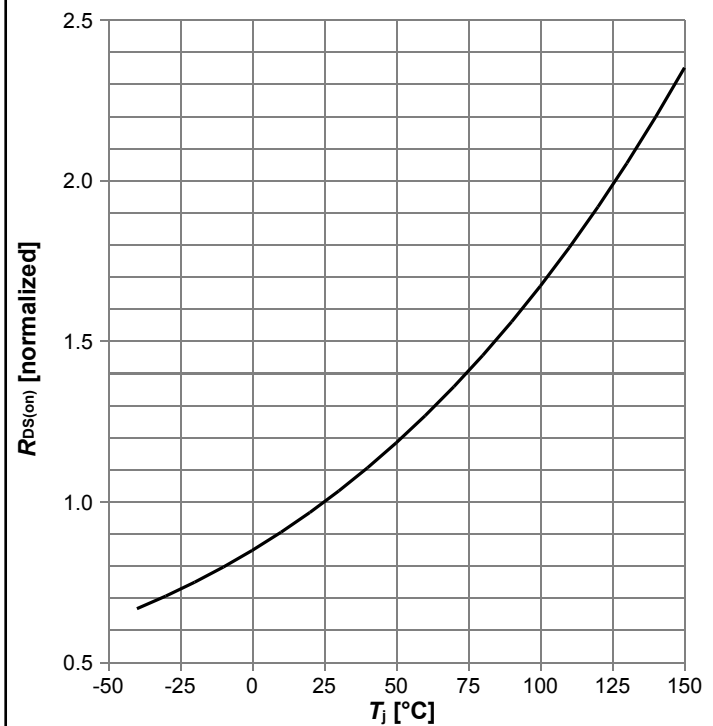
$I_D=f(V_{DS})$; $T_j=125^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



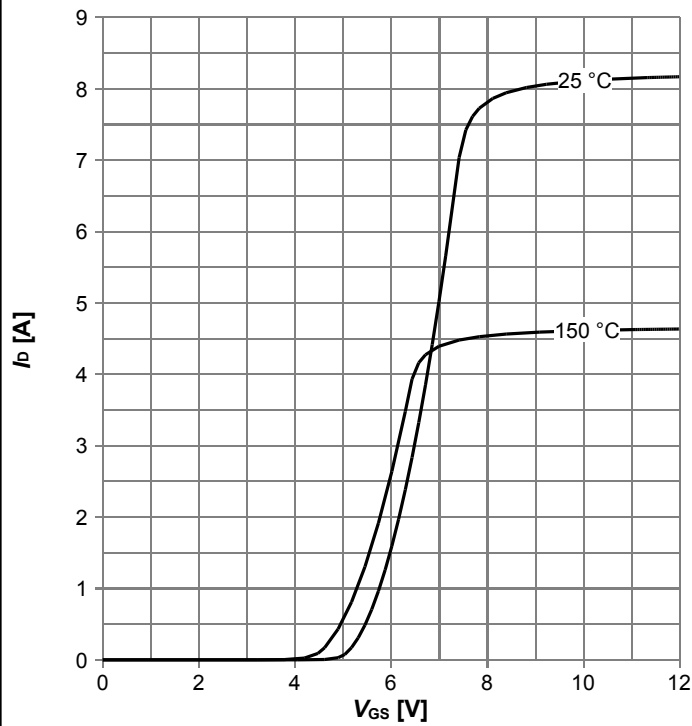
$R_{DS(on)}=f(I_D)$; $T_j=125^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



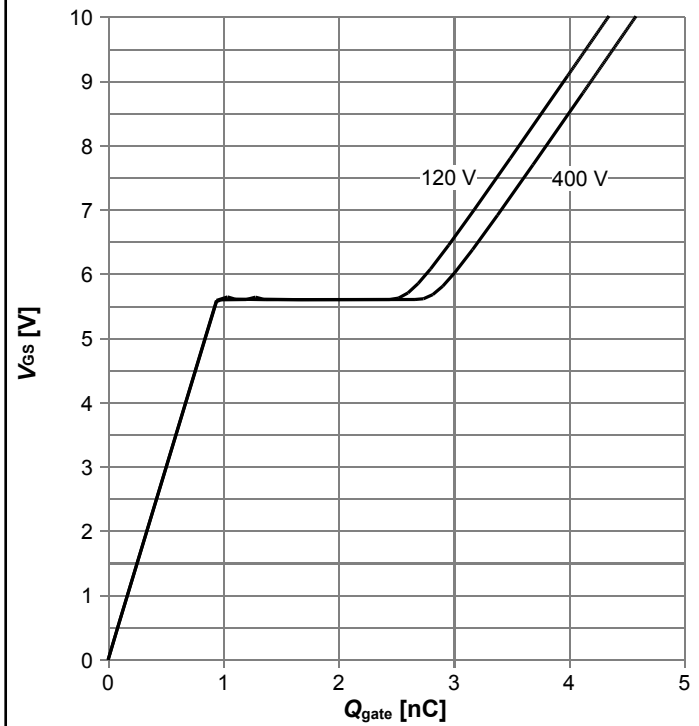
$R_{DS(on)}=f(T_j)$; $I_D=0.7\text{ A}$; $V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



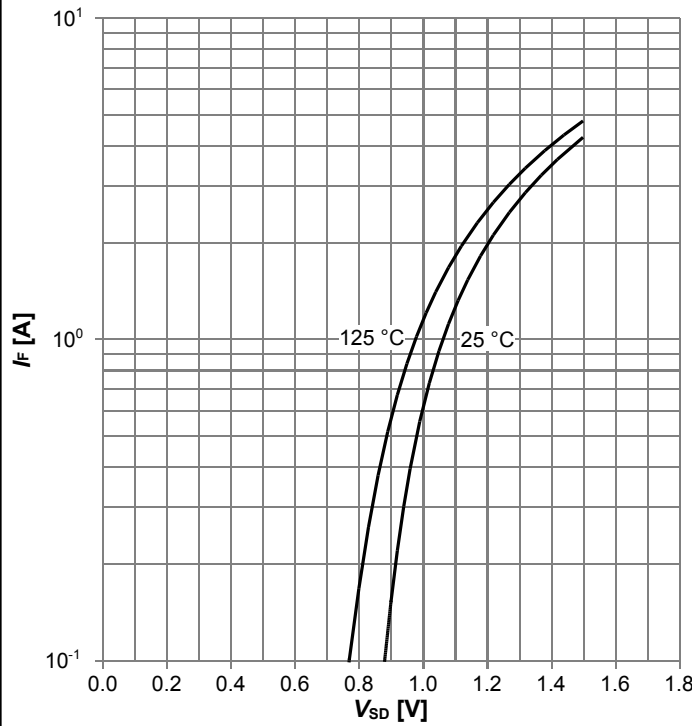
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



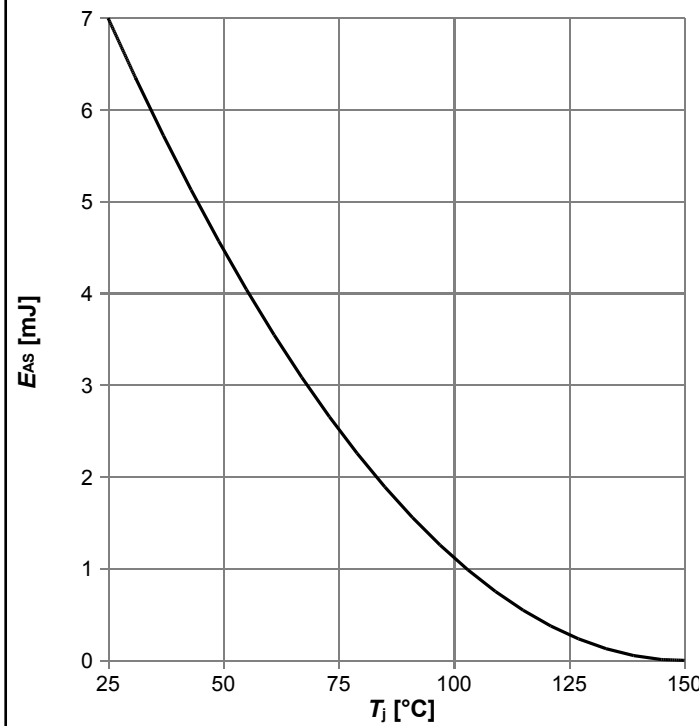
$V_{GS} = f(Q_{gate}); I_D = 0.7 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



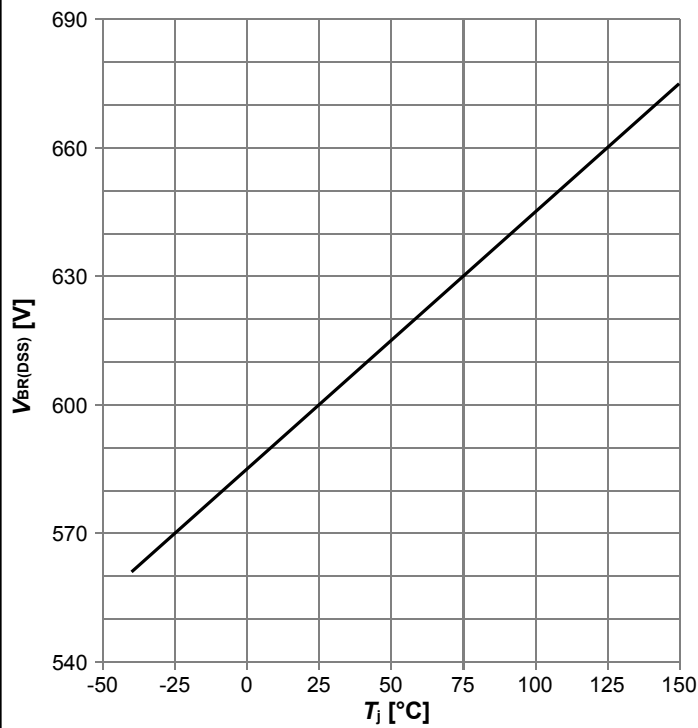
$I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy



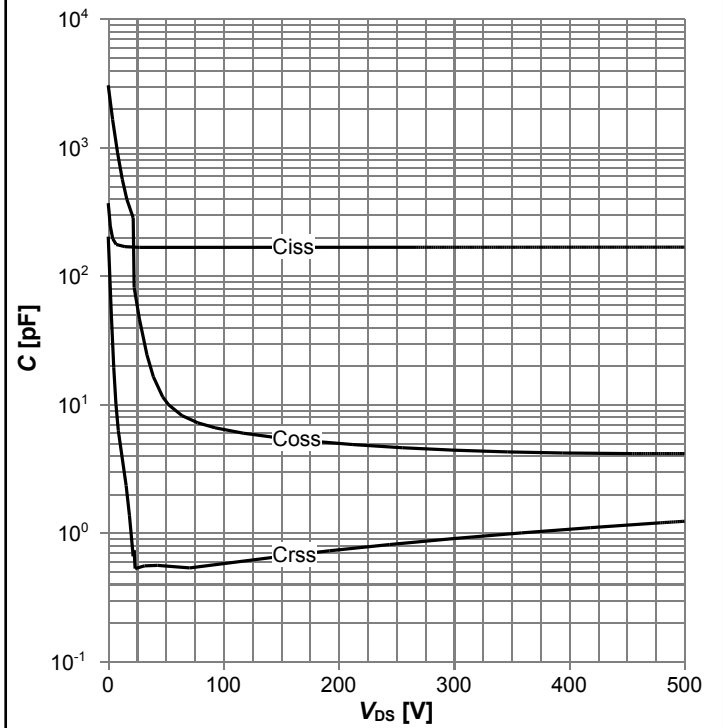
$E_{AS} = f(T_j); I_D = 0.7 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



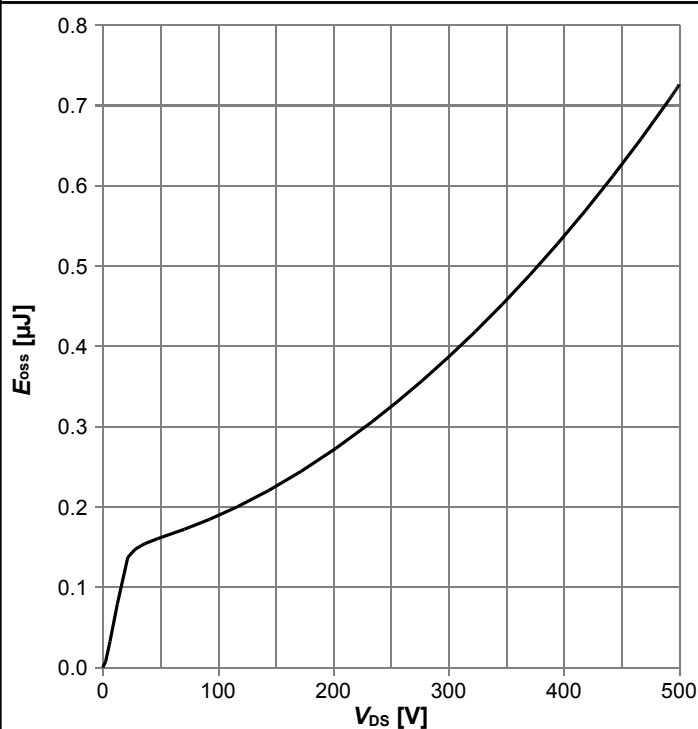
$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics



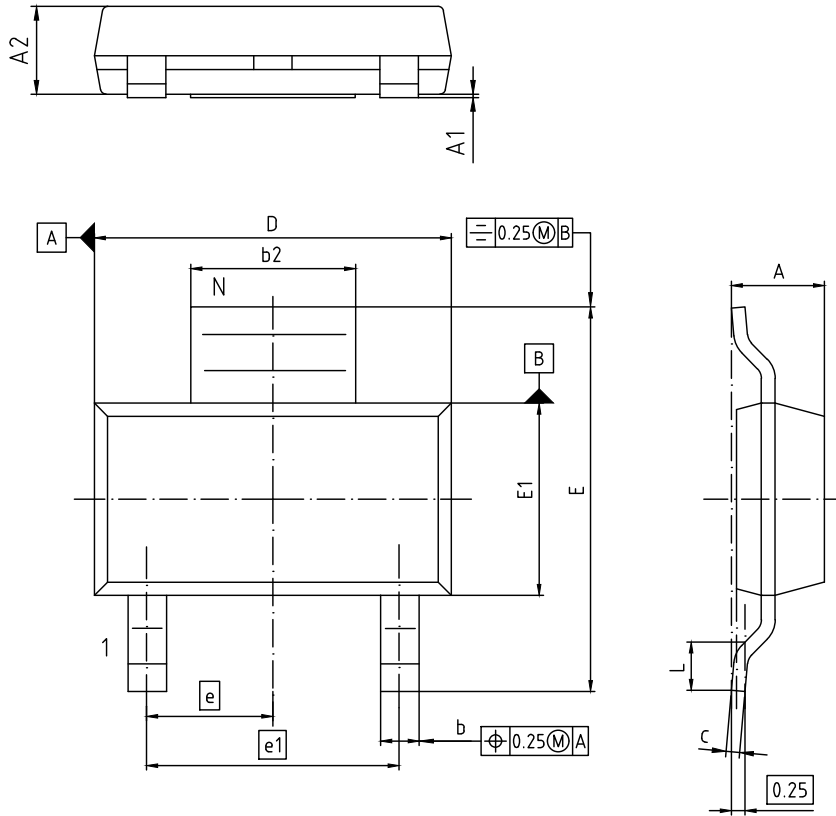
Table 9 Switching times



Table 10 Unclamped inductive load



6 Package Outlines



NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-261

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.52	1.80	0.060	0.071
A1	-	0.10	-	0.004
A2	1.50	1.70	0.059	0.067
b	0.60	0.80	0.024	0.031
b2	2.95	3.10	0.116	0.122
c	0.24	0.32	0.009	0.013
D	6.30	6.70	0.248	0.264
E	6.70	7.30	0.264	0.287
E1	3.30	3.70	0.130	0.146
e	2.3 BASIC		0.091 BASIC	
e1	4.6 BASIC		0.181 BASIC	
L	0.75	1.10	0.030	0.043
N	3		3	
O	0°	10°	0°	10°

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REVISION 01

Figure 1 Outline PG-SOT223, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- IFX CoolMOS PFD7 Webpage: www.infineon.com
- IFX CoolMOS PFD7 application note: www.infineon.com
- IFX CoolMOS PFD7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPN60R1K5PFD7S

Revision: 2019-09-27, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2019-09-27	Release of final version

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