PAC1931/2/3/4

Single/Multi-Channel DC Power/Energy Monitor with Accumulator

Features

- High-Side Current Monitor with One, Two, Three or Four Channels
  - 100 mV full-scale range for current sense voltage,16-bit resolution
  - Selectable bidirectional current sense capability, -100 mV to +100 mV range, 16-bit two's complement (signed) data format
  - External sense resistor sets full scale current range
  - Very low input current simplifies routing
- Wide Bus Voltage Range for Voltage Monitor
  - 0V to 32V input common-mode voltage
  - 16-bit resolution for voltage measurements; 14 bits are used for power calculations
- Real Time Auto-Calibration of Offset and Gain Errors for Voltage and Current, No User Adjustment Required
- 1% Power Measurement Accuracy over a Wide Dynamic Range
- On-Chip Accumulation of 28-bit Power Results for Energy Measurement
  - 48-bit power accumulator register for recording accumulated power data
  - 24-bit Accumulator Count
  - User programmable sampling rates of 8, 64, 256 and 1024 samples per second
  - 17 minutes of power data accumulation minimum at 1024 S/s
  - Over 36 hours of power data accumulation minimum at 8 S/s
- 2.7V to 5.5V Supply Operation
  - Separate V_{DD} I/O pin for digital I/O
  - 1.62-5.5V capable SMBus and digital I/O
  - SMBus 3.0 and I^2C Fast Mode Plus (1 Mb/S)
- SMBus Address – 16 Options, set with Resistor
- No Input Filters Required
- ALERT Features that can be Enabled:
  - ALERT on accumulator overflow
  - ALERT on Conversion Complete
- 4 × 4 × 0.5 mm UQFN Package
- 2.225 × 2.17 mm WLCSP Package

Applications

- Embedded Computing
- Networking
- FPGA Systems
- Automotive
- Low Voltage/High Power – AI, GPU
- Industrial
- Linux® Applications
- Notebook and Tablet Computing
- Cloud, Linux and Server Computing
- Optical Networking Modules

Computing Platform Support

- Windows® 10 Driver
- Linux Driver
- Python™ Script

Description

The PAC1931/2/3/4 are one, two, three and four-channel power and energy monitoring devices. A high-voltage multiplexer sequentially connects the inputs to a bus voltage monitor and current sense amplifier that feed high-resolution ADCs. Digital circuitry performs power calculations and energy accumulation.

This enables energy monitoring with integration periods from 1 ms up to 36 hours or longer. Bus voltage, sense resistor voltage and accumulated proportional power are stored in registers for retrieval by the system master or Embedded Controller.

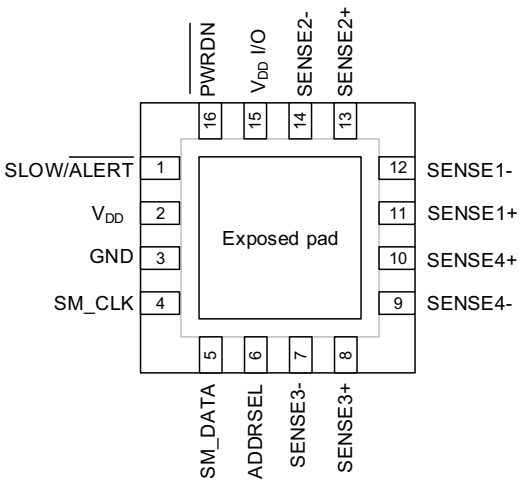
The sampling rate and energy integration period can be controlled over SMBus or I^2C. Active channel selection, one-shot measurements and other controls are also configurable by SMBus or I^2C.

The PAC1931/2/3/4 device family uses real time calibration to minimize offset and gain errors. No input filters are required for this device.

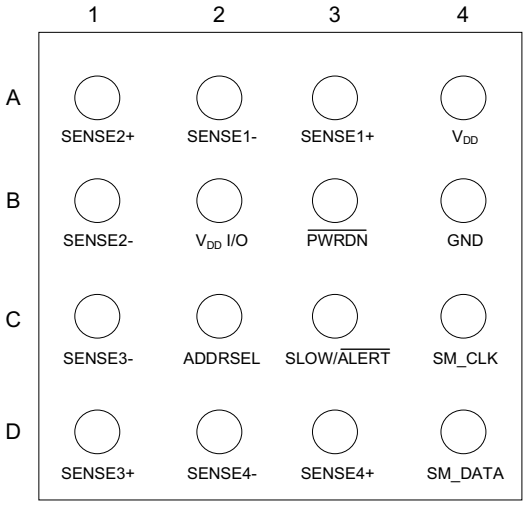
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Package Types

PAC1932/3/4 – Top View
4 × 4 × 0.5 mm UQFN*

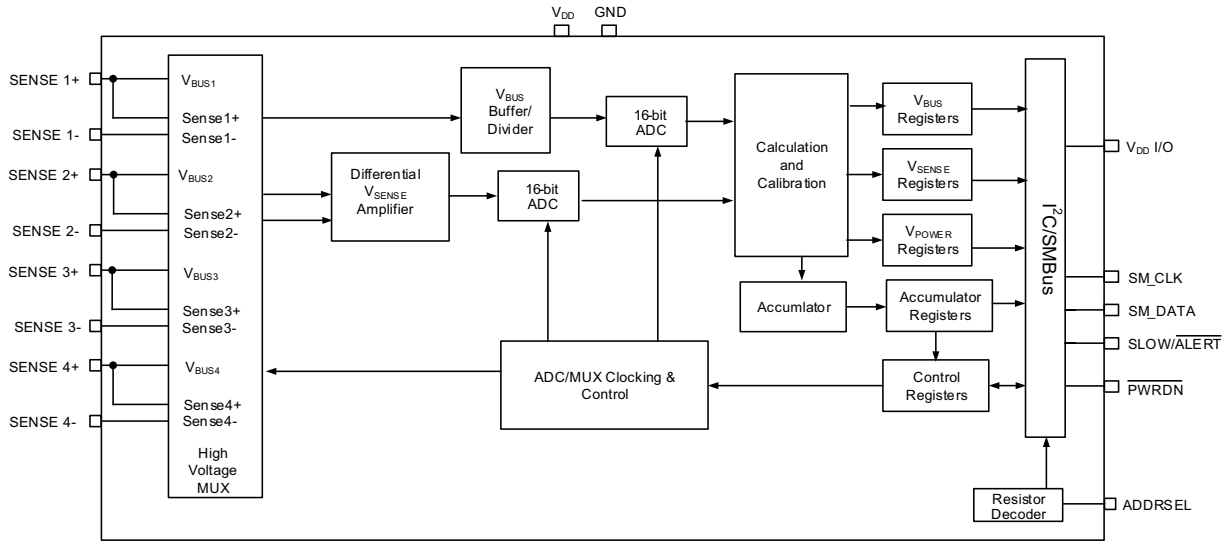


PAC1931/2/3/4 – Top View
2.225 × 2.17 mm WLCSP



*Includes Exposed Thermal Pad; see Table 3-1.

Device Block Diagram



Note: For PAC1931, channels 2, 3 and 4 are inactive.
For PAC1932, channels 3 and 4 are inactive.
For PAC1933, channel 4 is inactive.

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1.0 ELECTRICAL CHARACTERISTICS

1.1 Electrical Specifications

Absolute Maximum Ratings(†)

V_{DD} pin ..... -0.3 to 6.0V

Voltage on SENSE- and SENSE+ pins ..... -0.3 to 40V

Voltage on any other pin to GND ..... GND -0.3 to +6.0V

Voltage between Sense pins (|(SENSE+ – SENSE-)|) ..... 500 mV

Input current to any pin except V_{DD} ..... ±100 mA

Output short-circuit current ..... Continuous

Junction to Ambient (θ_{J-A}) ..... +78°C/W

Operating Ambient Temperature Range ..... -40 to +150°C

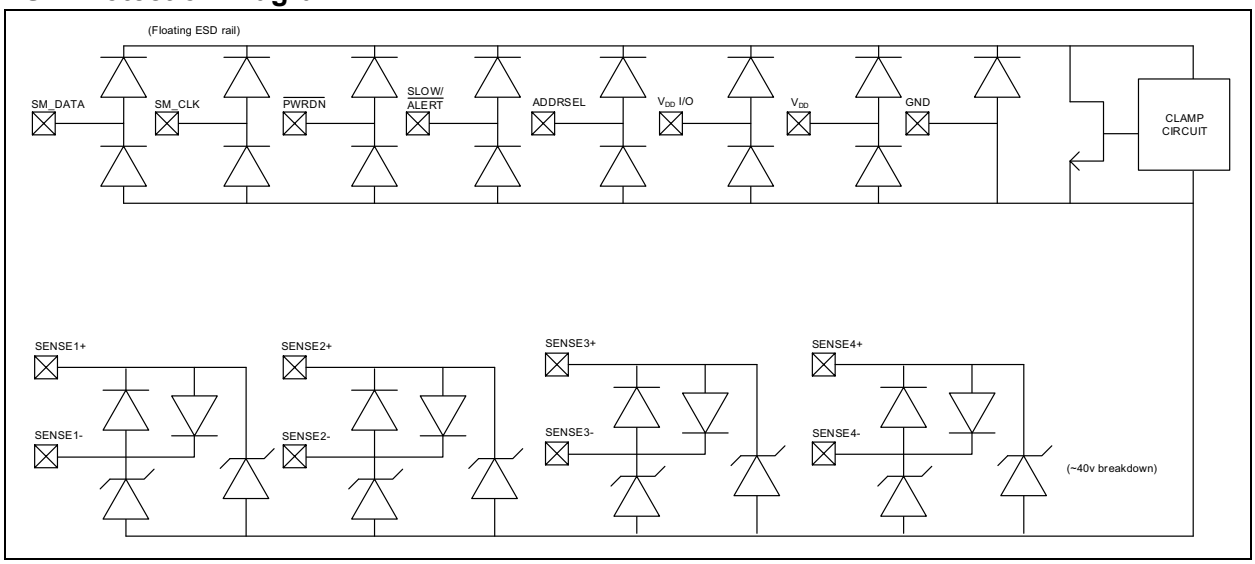
Storage Temperature Range ..... -55 to +150°C

ESD Rating – all pins – HBM 4000V

ESD Rating – all pins – CDM 2000V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

ESD Protection Diagram



This diagram represents the ESD protection circuitry on the PAC1934. The SENSE pins are allowed to be at 32V if V_{DD} is at zero. The back-to-back diodes between the Sense+ and Sense- pins have 1 kΩ resistors in series with them.

For PAC1931, PAC1932 and PAC1933, some of the SENSE pins are not electrically connected inside. These unconnected pins should be grounded.

TABLE 1-1: DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, $V_{DD\ I/O}$= 1.62V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C V_{DD} = $V_{DD\ I/O}$ = 3.3V, V_{BUS} = 32V, V_{SENSE} = (SENSE+ – SENSE-) = 0V

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Supply						
V_{DD} Range	V_{DD}	2.7	—	5.5	V	
$V_{DD\ I/O}$ Range	V_{DD} I/O	1.62	—	5.5	V	
V_{DD} Pin Active Current	I_{DD}	—	585	675	µA	1024 Samples/s All IDD specifications are the same for PAC1931/2/3/4
V_{DD} Pin Active Current	$I_{DD\ SLOW}$	—	16	—	µA	4 channels enabled, 8 Samples/s
Minimum V_{DD} Rise Rate	$V_{DD_RISE_MIN}$	—	0.05	—	V/ms	0 to 5V in 100 ms
Maximum V_{DD} Rise Rate	V_{DD_RISE}	—	1000	—	V/ms	0 to 5V in 5 µs
V_{DD} Sleep Current	I_{DD_SLEEP}	—	5	—	µA	Sleep State
V_{DD} Power-Down Current	I_{DD_PWRDN}	—	0.1	—	µA	Power-Down State
$V_{DD\ I/O}$ Current	$I_{DD\ I/O}$	—	—	2	µA	All States
Analog Input Characteristics						
V_{BUS} Voltage Range	V_{BUS}	–0.2V	—	32	V	Common-mode range for SENSE+ and SENSE- pins, referenced to ground (negative range not tested in production)
V_{SENSE} Differential Input Voltage Range	V_{SENSE_DIF}	–100	—	100	mV	
SENSE+, SENSE- Pin Input Current	I_{SENSE+}, I_{SENSE-}	–7	0	7	µA	V_{SENSE}+ = V_{SENSE}- = 32V (Input current is the combined current for the two pins)
SENSE+, SENSE- Pin Input current	I_{SENSE+}, I_{SENSE-}	–1	0	1	µA	V_{SENSE}+ = 6V, V_{SENSE}- = 5.9V
V_{BUS}, V_{SENSE} Input Trace Resistance (allowable trace resistance without measurement error)	R_{TRACE}	—	1	—	kΩ	
V_{SENSE} Measurement Accuracy						
V_{SENSE} Gain Accuracy	$V_{SENSE_GAIN_ERR}$	—	±0.2 ±1	±0.9	% %	At +25°C typical, -40 to +85°C
V_{SENSE} Offset Accuracy, referenced to input	$V_{BUS_OFFSET_ERR}$	—	±0.012 ±0.012	±0.1	mV mV	At +25°C typical, -40 to +85°C
V_{SENSE} – Unidirectional Currents						
V_{SENSE} ADC Resolution	V_{SENSE_RES}	—	—	16	Bits	Straight Binary for unidirectional currents
V_{SENSE} Full Scale Range	V_{SENSE_FSR}	0	—	100	mV	Unidirectional currents
V_{SENSE} LSB Step Size	V_{SENSE_LSB}	—	1.5	—	µV	Unidirectional currents

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TABLE 1-1: DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, $V_{DD\ I/O}$= 1.62V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C V_{DD} = $V_{DD\ I/O}$ = 3.3V, V_{BUS} = 32V, V_{SENSE} = (SENSE+ – SENSE-) = 0V

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{SENSE} – Bidirectional Currents						
V_{SENSE} ADC Resolution	V_{SENSE_RES}	—	—	16	bits	16-bit two's complement (signed)
V_{SENSE} Full Scale Range	V_{SENSE_FSR}	-100	—	100	mV	Bidirectional currents
V_{SENSE} LSB Step Size	V_{SENSE_LSB}	—	3	—	µV	Bidirectional currents
V_{BUS} Measurement Accuracy						
V_{BUS} Gain Accuracy	$V_{BUS_GAIN_ERR}$	—	±0.02 ±0.2	±0.5	% %	At +25°C typical, -40 to +85°C
V_{BUS} Offset Accuracy, referenced to input	$V_{BUS_OFFSET_ERR}$	—	±1 ±2	—	LSB LSB	At +25°C typical, -40 to +85°C
V_{BUS} – Unipolar Voltages						
V_{BUS} ADC Resolution	V_{BUS_RES}	—	—	16	bits	Straight Binary for unidirectional currents
V_{BUS} Unipolar Full-Scale Range	V_{BUS}_FSR	0	—	32	V	Unipolar voltage
V_{BUS} LSB Step Size	V_{BUS}_LSB	—	488	—	µV	FSR = 32V, 16-bit resolution
V_{BUS} – Bipolar Voltages						
V_{BUS} ADC Resolution	V_{BUS_RES}	—	—	16	bits	16-bit two's complement (signed) numbers are reported for V_{BUS} measurement result
V_{BUS} Bipolar Full-Scale Range	V_{BUS}_FSR	–32	—	32	V	Mathematical scaling. Physics limits the negative input voltage to -0.2V
V_{BUS} LSB Step Size	V_{BUS}_LSB	—	976	—	µV	Bipolar voltages
Power Accumulator Accuracy						
Accumulator Error	ACC_Err	—	0.2	—	%	V_{SENSE} = 97 mV
Accumulator Error	ACC_Err	—	0.2	—	%	V_{SENSE} = 10 mV
Accumulator Error	ACC_Err	—	1	—	%	V_{SENSE} = 1 mV
Accumulator Error	ACC_Err	—	3	—	%	V_{SENSE} = 100 µV
Accumulator Error	ACC_Err	—	5	—	%	V_{SENSE} = 50 µV
Active Mode Timing						
Pull-Up Voltage Range	V_{PULLUP}	1.62	—	5.5	V	Pull-up voltage for I^2C/SMBus pins and digital I/O pins. Set by V_{DD} I/O.
Time to First Communications	t_{INT_T}	—	14.25	—	ms	
Transition From Sleep State to Start of Conversion Cycle	$t_{SLEEP_TO_ACTIVE}$	—	3	—	ms	
Digital I/O Pins (SM_CLK, SM_DATA, SLOW/$\overline{\text{ALERT}}$, $\overline{\text{PWRDN}}$)						
Input High Voltage	V_{IH}	V_{DD} I/O x 0.7	—	—	V	
Input Low Voltage	V_{IL}	—	—	V_{DD} I/O x 0.3	V	

TABLE 1-1: DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, $V_{DD\ I/O}$= 1.62V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C V_{DD} = $V_{DD\ I/O}$ = 3.3V, V_{BUS} = 32V, V_{SENSE} = (SENSE+ – SENSE-) = 0V						
Characteristic	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Output Low Voltage	V_{OL}	—	—	0.4	V	Sinking 8 mA for the $\overline{\text{ALERT}}$ pin and 20 mA for the SMCLK pin
Leakage Current	I_{LEAK}	–1	—	+1	µA	

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TABLE 1-2: SMBUS MODULE SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 32V; Typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 32V, V_{SENSE} = (SENSE+ – SENSE-) = 0V, V_{DD} I/O = 1.62V to 5.5V						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SMBus Interface						
Input Capacitance	C_{IN}	—	4	10	pF	Not tested in production
SMBus Timing						
Clock Frequency	f_{SMB}	.010	—	1	MHz	No minimum if Time-Out is not enabled
Spike Suppression	t_{SP}	0	—	50	ns	
Bus Free Time Stop to Start	t_{BUF}	0.5	—	—	µs	Per SMBus 3.0
Hold Time after Repeated Start Condition	$t_{HD:STA}$	0.26	—	—	µs	Per SMBus 3.0
Repeated Start Condition Setup Time	$t_{SU:STA}$	0.26	—	—	µs	Per SMBus 3.0
Setup Time: Stop	$t_{SU:STO}$	0.26	—	—	µs	Per SMBus 3.0
Setup Time: Start	$t_{SU:STA}$	0.26	—	—	µs	
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	
Data Setup Time	$t_{SU:DAT}$	50	—	—	ns	Per SMBus 3.0 (**Note**)
Clock Low Period	t_{LOW}	0.5	—	—	µs	Per SMBus 3.0
Clock High Period	t_{HIGH}	0.26	—	50	µs	
Clock/Data Fall Time	t_{FALL}	—	—	120	ns	Not tested in production
Clock/Data Rise Time	t_{RISE}	—	—	120	ns	Not tested in production
Capacitive Load	C_{LOAD}	—	—	550	pF	Per bus line, C_{LOAD} not tested in production
SLOW Pin Pulse Width	SLOWpw	—	100	—	µs	Pulses narrower than 100 µS may not be detected

Note: A device must internally provide a hold time of at least 300 ns for the SM_DATA signal (with respect to the $V_{IH(min)}$ of the SM_CLK signal) to bridge the undefined region of the falling edge of SM_CLK.

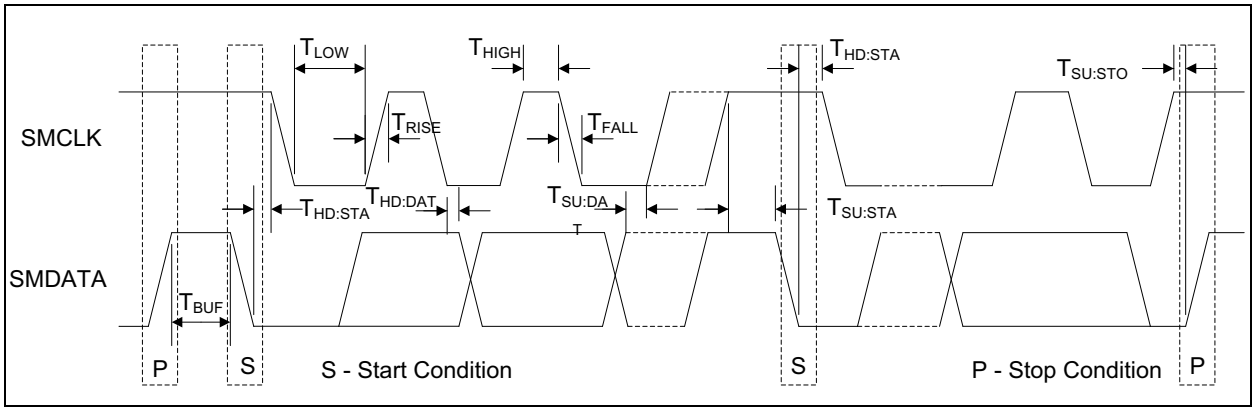


FIGURE 1-1: *SMBus Timing.*

2.0 TYPICAL OPERATING CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 3.3V, V_{SENSE} = (SENSE+ – SENSE-) = 0V, V_{DD} I/O = 1.62 to 5.5V.

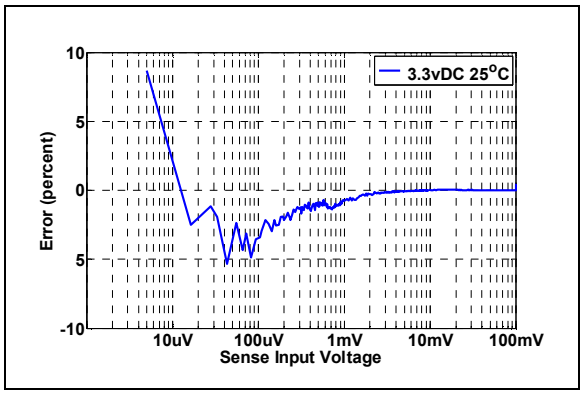


FIGURE 2-1: *V_{SENSE} Error vs. V_{SENSE} Input Voltage.*

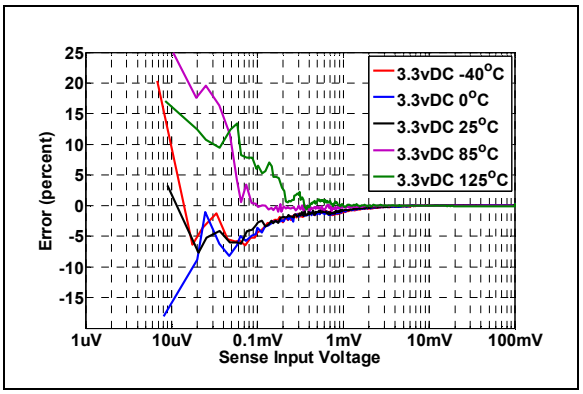


FIGURE 2-4: *V_{SENSE} Error vs. V_{SENSE} Input Voltage and Temperature.*

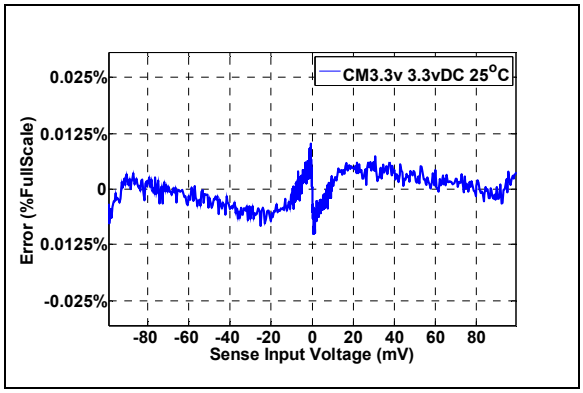


FIGURE 2-2: *V_{SENSE} Error vs. V_{SENSE} Input Voltage Bidirectional Mode.*

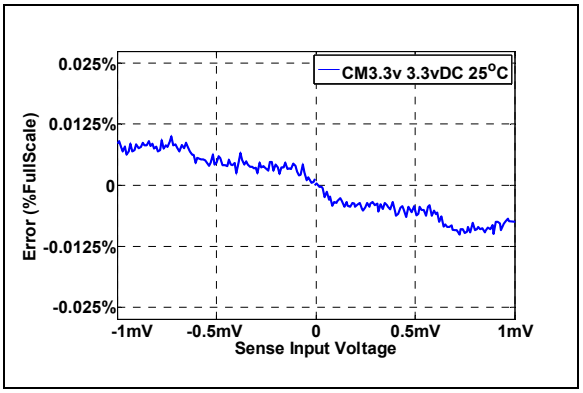


FIGURE 2-5: *V_{SENSE} Error vs. V_{SENSE} Input Voltage Bidirectional Mode (Zoom View).*

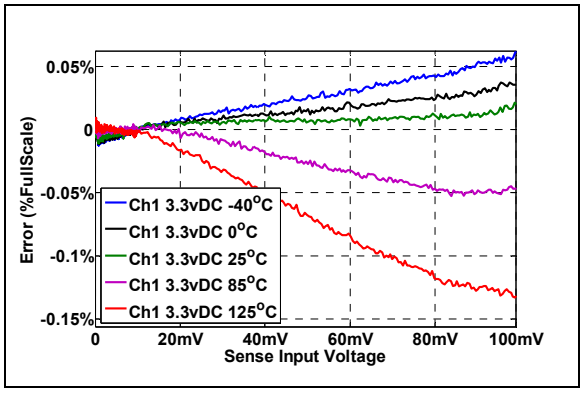


FIGURE 2-3: *V_{SENSE} Error vs. V_{SENSE} Input Voltage vs. Temperature.*

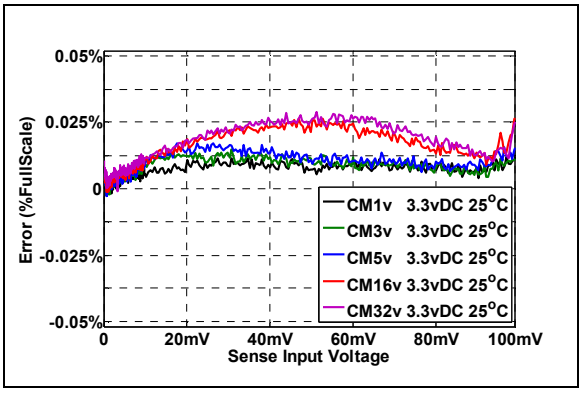


FIGURE 2-6: *V_{SENSE} Error vs. V_{SENSE} and Common Mode.*

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Note: Unless otherwise indicated, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 3.3V, V_{SENSE} = (SENSE+ – SENSE-) = 0V, V_{DD} I/O = 1.62 to 5.5V.

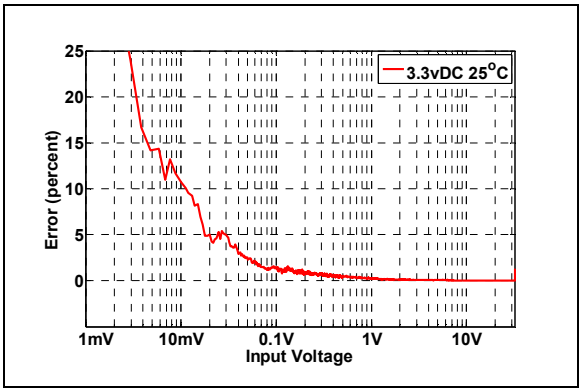


FIGURE 2-7: *V_{BUS} Error vs. V_{BUS} Input Voltage.*

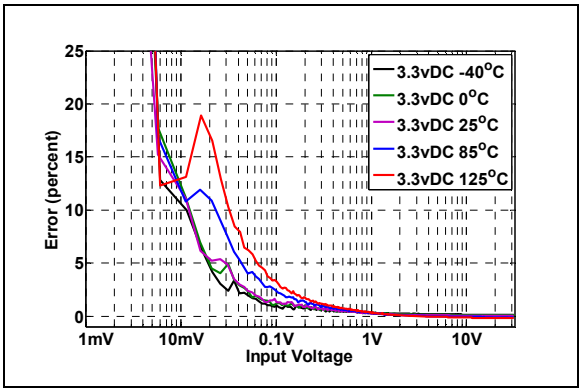


FIGURE 2-10: *V_{BUS} Error vs. V_{BUS} Input Voltage vs. Temperature.*

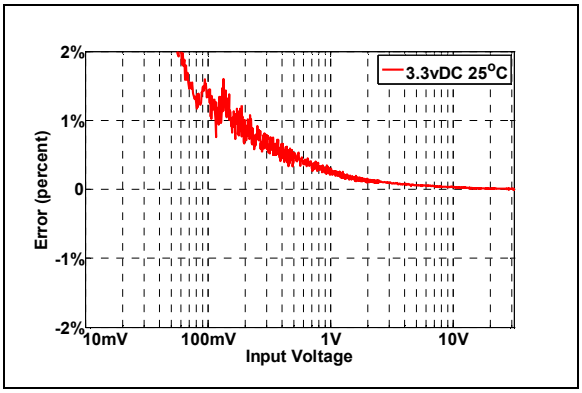


FIGURE 2-8: *V_{BUS} Error vs. V_{BUS} Input Voltage (Zoom View).*

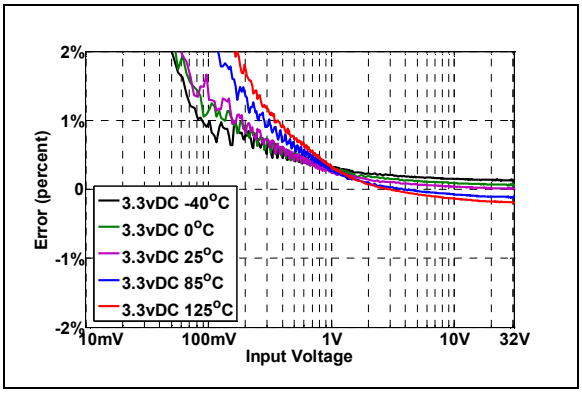


FIGURE 2-11: *V_{BUS} Error vs. V_{BUS} Input Voltage vs. Temperature (Zoom View).*

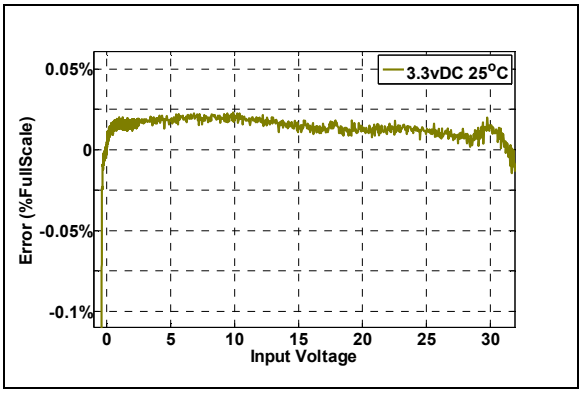


FIGURE 2-9: *V_{BUS} Error vs. V_{BUS} Input Voltage.*

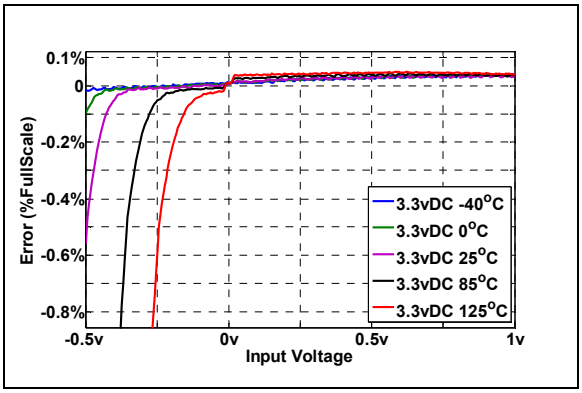


FIGURE 2-12: *V_{BUS} Error vs. V_{BUS} Input Voltage vs. Temperature (Bipolar Voltage Mode).*

Note: Unless otherwise indicated, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 3.3V, V_{SENSE} = (SENSE+ – SENSE-) = 0V, V_{DD} I/O = 1.62 to 5.5V.

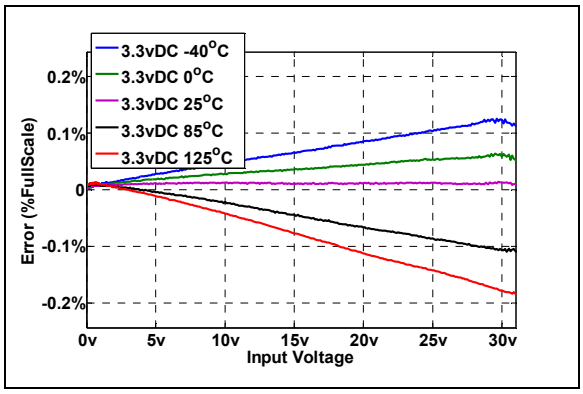


FIGURE 2-13: *V_{BUS} Error vs. V_{BUS} Input Voltage vs. Temperature.*

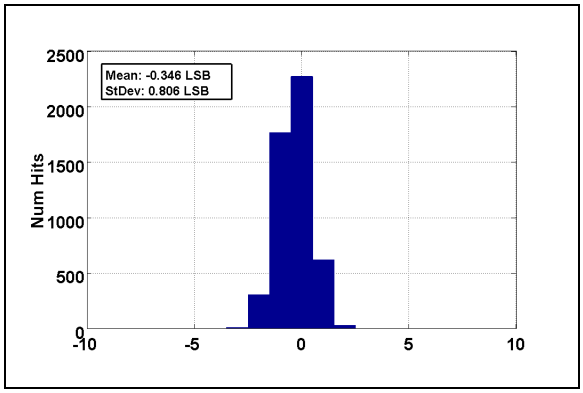


FIGURE 2-14: *Zero Input Histogram for V_{BUS} (LSBs, 8X Average Results, Total Population 5,000 devices).*

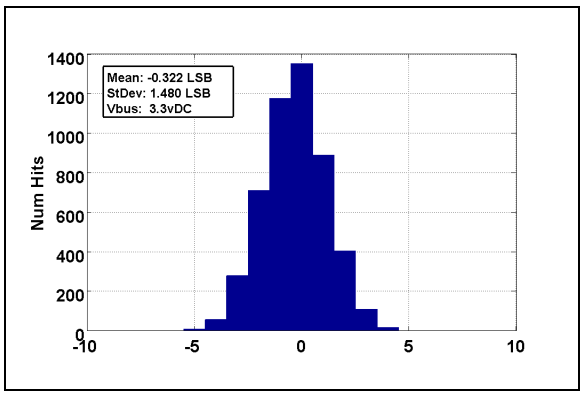


FIGURE 2-15: *Zero Input Histogram for V_{SENSE} (LSBs, 8X Average Results, Total Population 5,000 Devices).*

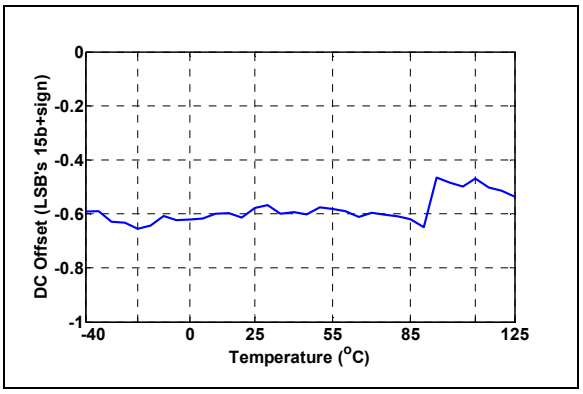


FIGURE 2-16: *Input Offset for V_{BUS} Measurements vs. Temperature.*

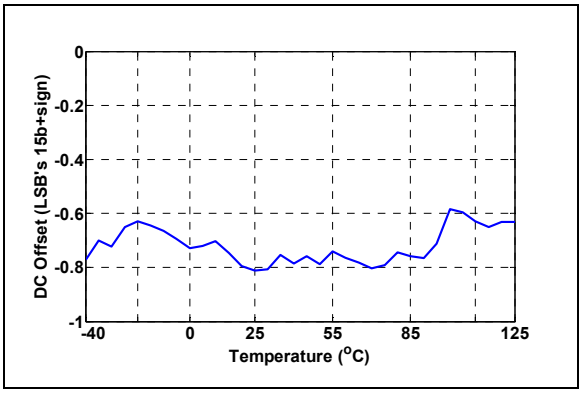


FIGURE 2-17: *Input Offset for V_{SENSE} Measurements vs. Temperature.*

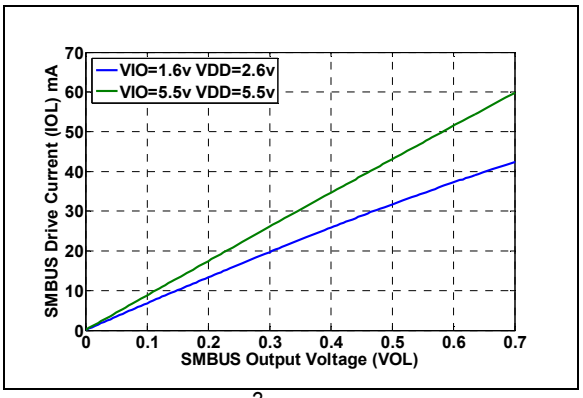


FIGURE 2-18: *I^2C/SMBus Drive Current vs. V_{OL}.*

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Note: Unless otherwise indicated, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 3.3V, V_{SENSE} = (SENSE+ – SENSE-) = 0V, V_{DD} I/O = 1.62 to 5.5V.

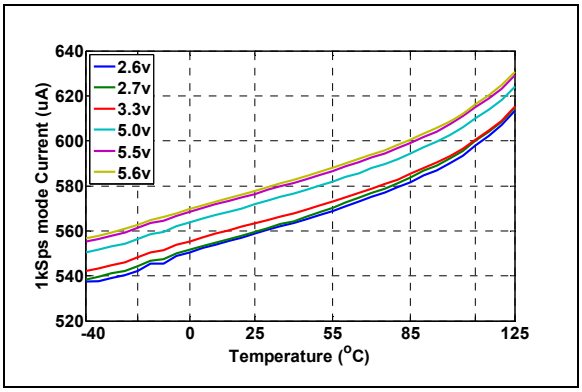


FIGURE 2-19: *I_{DD} vs. Temperature and Supply at 1024 Samples/Second.*

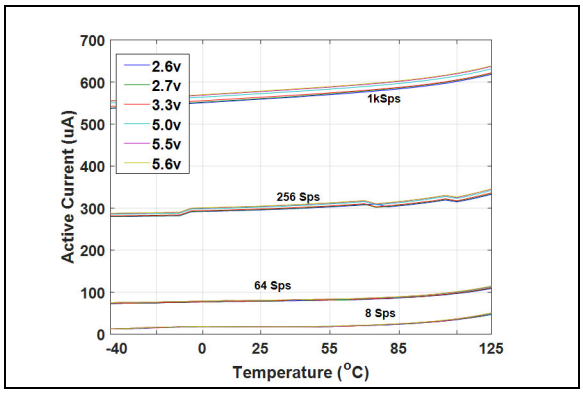


FIGURE 2-22: *I_{DD} vs.Temperature, V_{DD}, and Sample Rate.*

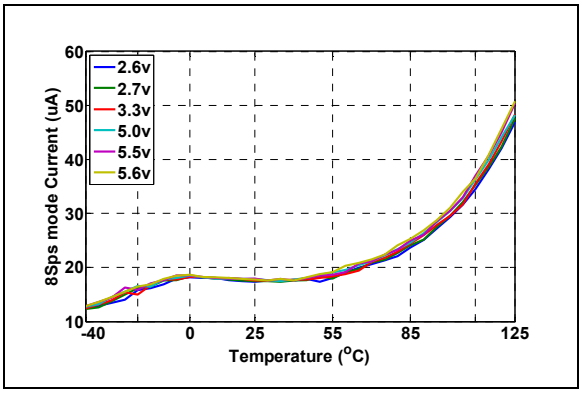


FIGURE 2-20: *I_{DD} in SLOW Mode vs. Temperature and V_{DD}.*

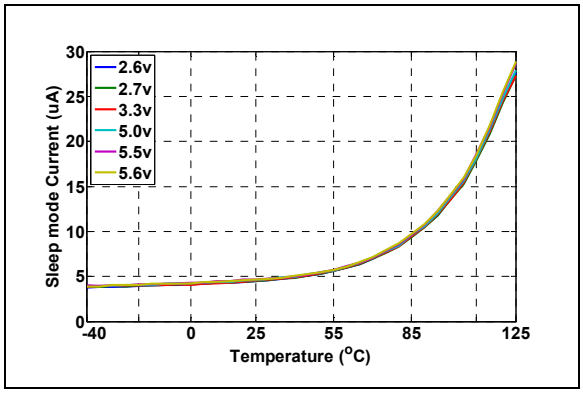


FIGURE 2-23: *I_{DD} in SLEEP Mode vs. Temperature and V_{DD}.*

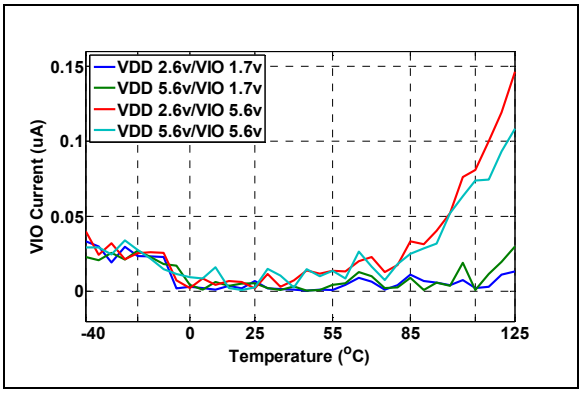


FIGURE 2-21: *I_{DD} for V_{DD} I/O Pin vs. Temperature and V_{DD}.*

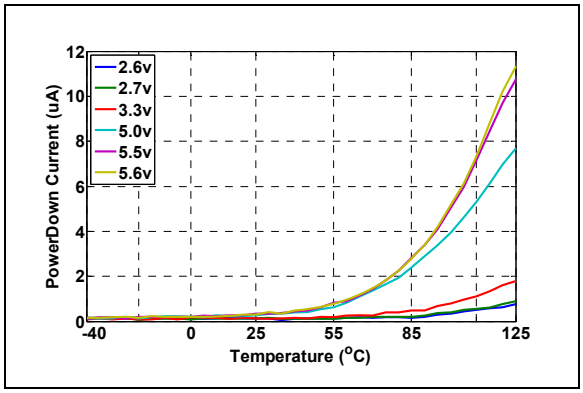


FIGURE 2-24: *I_{DD} in Power Down Mode vs. Temperature and V_{DD}.*

Note: Unless otherwise indicated, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 3.3V, V_{SENSE} = (SENSE+ – SENSE-) = 0V, V_{DD} I/O = 1.62 to 5.5V.

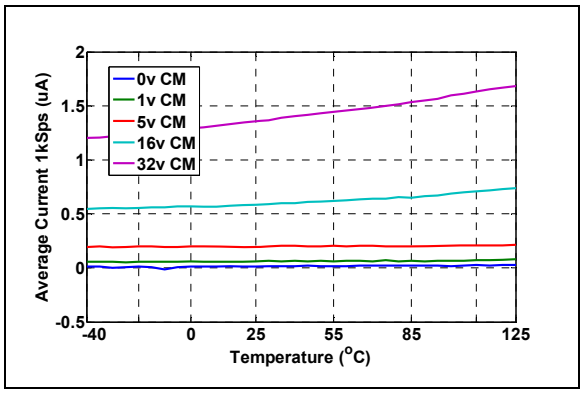


FIGURE 2-25: *V_{SENSE} Input Current – Active Mode, 1024 Samples/Second.*

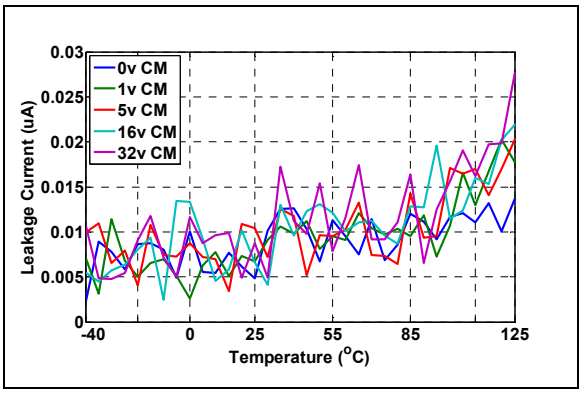


FIGURE 2-28: *V_{SENSE} Input Leakage Current vs. V_{DD} and Temperature.*

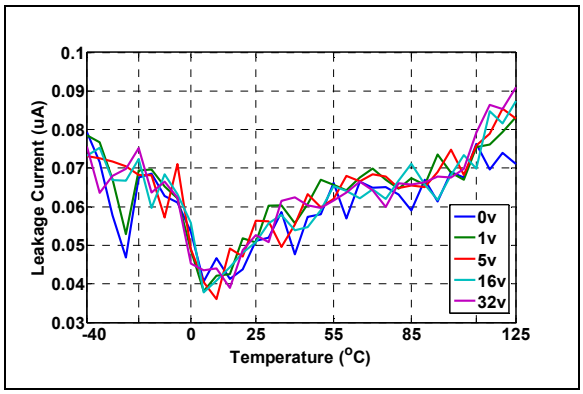


FIGURE 2-26: *V_{BUS} Input Leakage Current vs. V_{DD} and Temperature.*

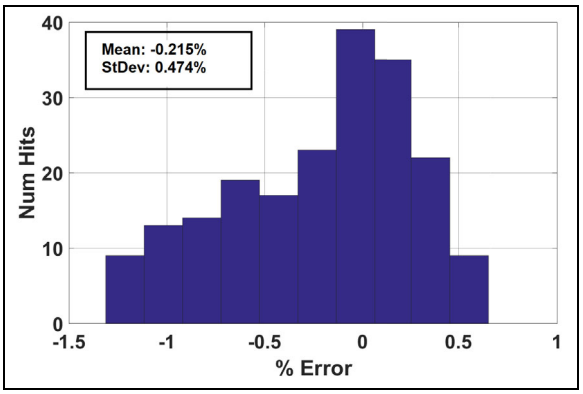


FIGURE 2-29: *Clock Frequency Error -40°C to +85°C. Total Population 200 Devices.*

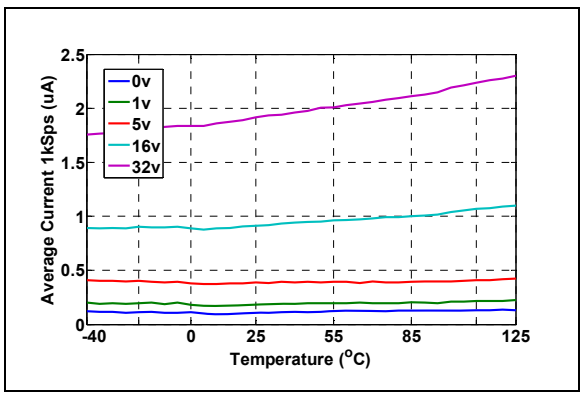


FIGURE 2-27: *V_{BUS} Input Current – Active Mode, 1024 Samples/Second.*

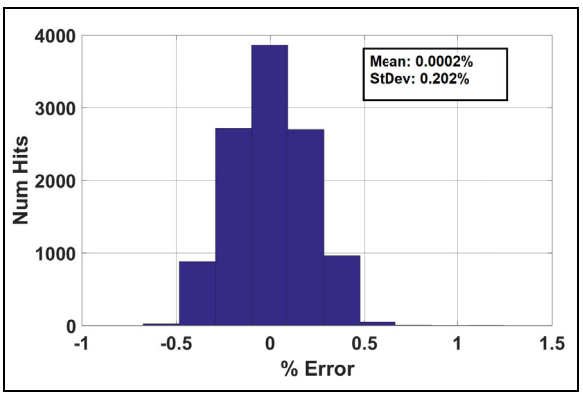


FIGURE 2-30: *Clock Frequency Error at 30°C. Total Population 11,189 Devices.*

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Figure 2-31 shows the equivalent circuitry for the input channels of the PAC193X devices. ESD protection diodes include two 40V breakdown diodes. Input leakage current is very low (no DC bias current). The switched capacitor sampling circuits shown as a switch with equivalent series resistance and sampling capacitor. The switches work at 1024 samples per second (SPS) maximum, independent of sampling rate (at 8 SPS, the device is sleeping in between samples). Input impedance for each input is about 32 MΩ.

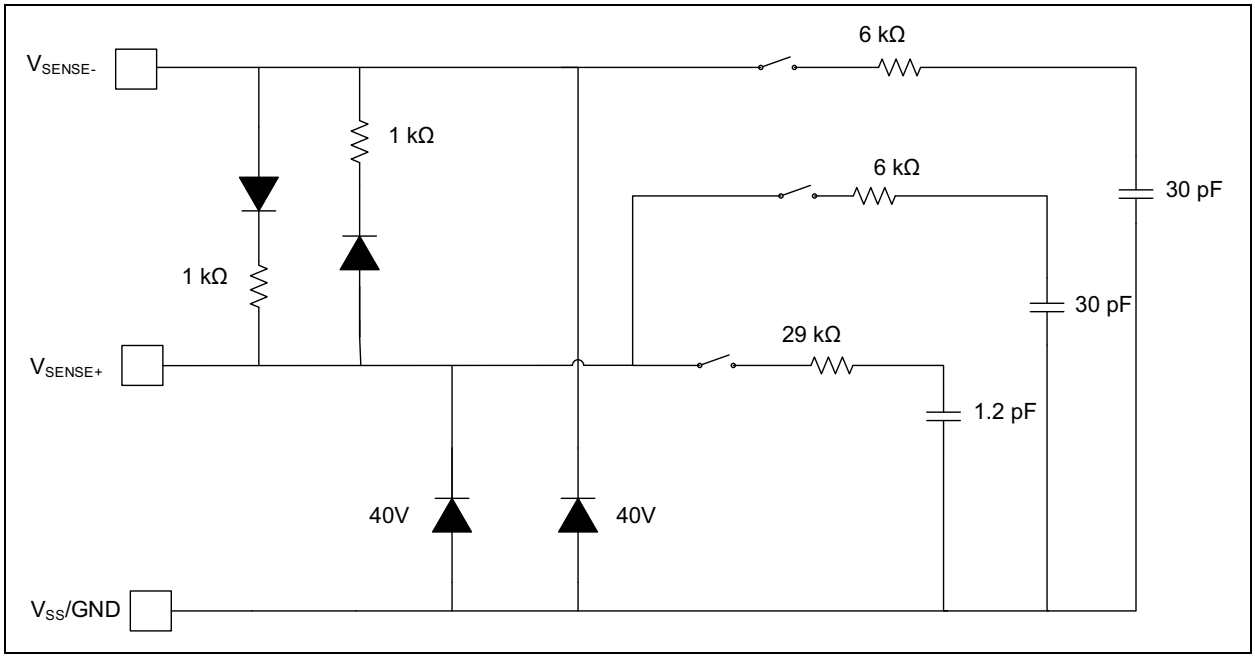


FIGURE 2-31: *Equivalent Input Circuits for PAC193X Devices.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in **Table 3-1**.

TABLE 3-1: PIN DESCRIPTIONS

QFN	WLCSP16	Symbol	Pin Type	Description
1	C3	SLOW/$\overline{\text{ALERT}}$	Digital I/O pin	Voltage range is set by V_{DD} I/O pin. Default function is SLOW, may be programmed to function as $\overline{\text{ALERT}}$ pin (Open Collector when functioning as $\overline{\text{ALERT}}$, requires pull-up resistor to V_{DD} I/O).
2	A4	V_{DD}	Power for IC	Positive power supply voltage
3	B4	GND	Ground pin	Ground for the IC
4	C4	SM_CLK	SMBus clock input	Clock Input pin
5	D4	SM_DATA	SMBus data I/O	Open drain requires pull-up resistor to V_{DD} I/O
6	C2	ADDRSEL	Analog I/O pin	Address selection for the SMBus Slave address
7(1)	C1(2)	SENSE3-	32V analog pin	0-32V range, connect to load side of sense resistor
8(1)	D1(2)	SENSE3+	32V analog pin	0-32V range, connect to supply side of sense resistor
9(1)	D2(2)	SENSE4-	32V analog pin	0-32V range, connect to load side of sense resistor
10(1)	D3(2)	SENSE4+	32V analog pin	0-32V range, connect to supply side of sense resistor
11	A3	SENSE1+	32V analog pin	0-32V range, connect to supply side of sense resistor
12	A2	SENSE1-	32V analog pin	0-32V range, connect to load side of sense resistor
13	A1(2)	SENSE2+	32V analog pin	0-32V range, connect to supply side of sense resistor
14	B1(2)	SENSE2-	32V analog pin	0-32V range, connect to load side of sense resistor
15	B2	V_{DD} I/O	Sets V_{IH} reference for digital I/O	Digital power reference level for digital I/O
16	B3	$\overline{\text{PWRDN}}$	Digital input pin	Voltage range is set by V_{DD} I/O pin. Active low puts the device in power-down state (all circuitry is powered down including SMBus).
17	—	EP	N/C	The Exposed pad is not electrically connected

Note 1: For PAC1932, pins 7,8,9,10 are not connected inside and should be grounded.
For PAC1933, pins 9 and 10 are not connected inside and should be grounded.

2: For PAC1931, solder balls on A1, B1, C1, D1, D2, and D3 are present but the channels are disabled internally and should be grounded. For PAC1932, solder balls on C1, D1, D2, and D3 are present but the channels are disabled internally and should be grounded. For PAC1933, solder balls on D2 and D3 are present but the channels are disabled internally and should be grounded.

3.1 SenseN+/SenseN– (N=1,2,3,4)

These two pins form the differential input for measuring voltage across a sense resistor in the application. The positive input (SenseN+) also acts as the input pin for bus voltage.

3.2 Ground (GND)

System ground.

3.3 SMBus Data (SM_DATA)

This is the bi-directional SMBus data pin. This pin is open drain, and requires a pull-up resistor to V_{DD} I/O.

3.4 SMBus Clock (SM_CLK)

This is the SMBus clock input pin.

3.5 Positive Power Supply Voltage (V_{DD})

Power supply input pin for the device. 2.7-5.5V range, bypass with 100 nF ceramic capacitor to ground near the IC.

3.6 Digital Power Reference Voltage ($V_{DD\ I/O}$)

Connect this pin to the power supply voltage for the digital controller driving the SMBus pins and digital input pins for the device, 1.62V-5.5V. Bypass with 100 nF ceramic capacitor to ground near the IC. This pin does not supply power, instead it acts as the V_{IH} reference.

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3.7 Address Selection (ADDR_SEL)

Connect a resistor from this pin to ground to select SMBus address.

3.8 Enable Pin ($\overline{\text{PWRDN}}$)

Power down input pin for the device, active low.

3.9 SLOW/$\overline{\text{ALERT}}$

In default mode, if this pin is forced high, sampling rate is forced to eight samples/second. When it is forced low, the sampling rate is 1024 samples/second unless a different sample rate has been programmed.This pin may be programmed to act as the $\overline{\text{ALERT}}$ pin, in $\overline{\text{ALERT}}$ mode the pin needs a pull-up resistor to V_{DD} I/O.

3.10 Exposed Thermal Pad Pin (EP)

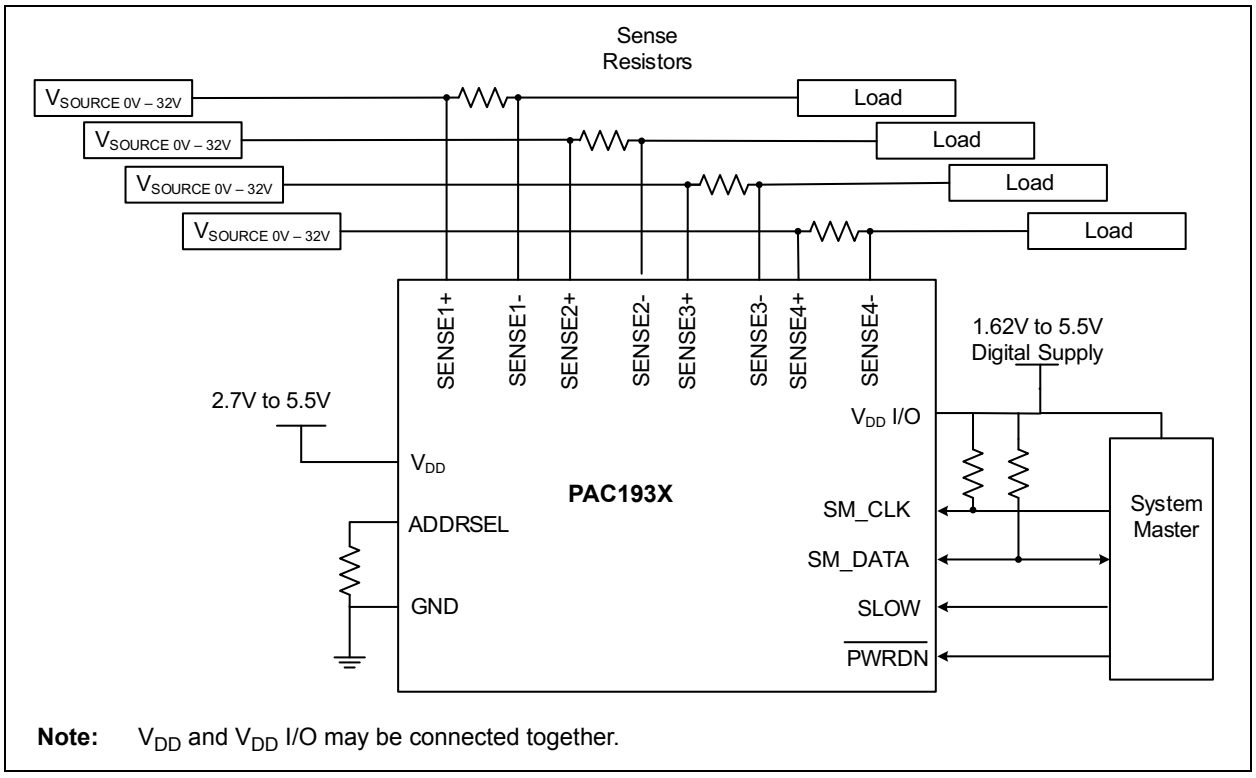
The Exposed pad is not electrically connected. It is recommended that you connect it to ground.

4.0 GENERAL DESCRIPTION

The PAC1934 is a four-channel, bidirectional, high-side current-sensing device with precision voltage measurement capabilities, DSP for power calculation and a power accumulator. PAC1931, PAC1932 and PAC1933 are one, two and three-channel versions of the PAC1934. These devices measure the voltage developed across an external sense resistor (V_{SENSE}) to represent the high-side current of a battery or voltage regulator. The PAC1931/2/3/4 also measures the SENSE+ pin voltages (V_{BUS}). Both V_{BUS} and V_{SENSE} are converted to digital results by a 16-bit ADC, and the digital results are multiplied to give V_{POWER}. The V_{POWER} results are accumulated on-chip, which enables energy measurement over the accumulation period.

The PAC1931/2/3/4 has an I^2C/SMBus interface for digital control and reading results. It also has digital supply reference V_{DD} I/O that is to be connected to the same supply as the digital master for the I^2C/SMBUS, enabling digital I/O voltages as low as 1.62V.

A system diagram is shown in **Figure 4-1**.



Note: V_{DD} and V_{DD} I/O may be connected together.

FIGURE 4-1: *PAC1931/2/3/4 System Diagram.*

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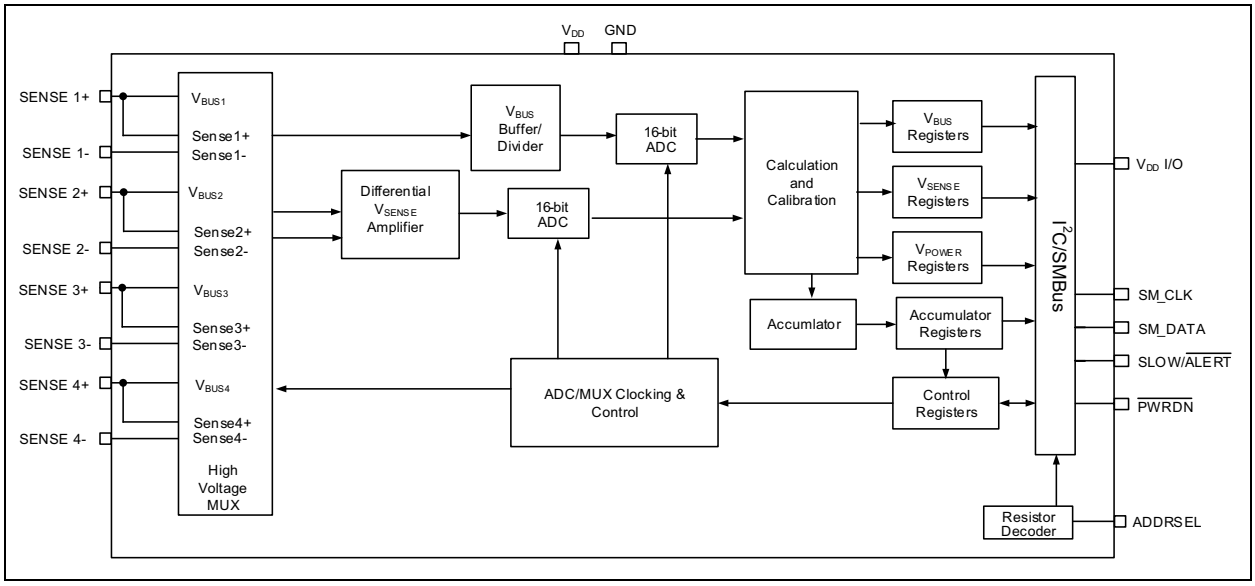


FIGURE 4-2: *PAC1931/2/3/4 Functional Block Diagram.*

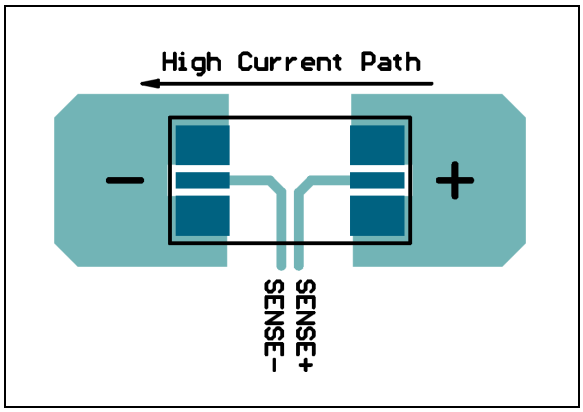


FIGURE 4-3: *PCB Pattern for Sense Resistor.*

Figure 4-3 shows the recommended PCB pattern for sense resistor with wide metal for the high-current path. The drawing shows metal, solder paste openings and resistor outline. V_{SOURCE} connects to the +terminal of the high-current path, and the load connects to the -terminal of the high-current path. Sense+ and Sense- have a Kelvin connection to the current sense resistor to ensure that no metal with high current is included in the V_{SENSE} measurement path. Sense+ and Sense- are shown as a differential pair, route them as a differential pair to the Sense inputs at the chip. The input pins allow for a typical V_{SENSE} trace resistance of 1 kΩ, which allows the routing flexibility far away from the chip itself on the board.

4.1 Detailed Description

A high-voltage multiplexer connects the input pins to the V_{BUS} and V_{SENSE} amplifiers. The amplifier outputs are sampled simultaneously for each channel, converted by 16 bit ADCs and processed for gain and offset error correction. After each conversion, V_{BUS} and V_{SENSE} are multiplied together to give V_{POWER}.

An internal oscillator and digital control signals control the two ADCs and the mux. The mux sequentially connects each channel's amplifiers to the ADC inputs.

The PAC1931/2/3/4 measures the source-side voltage, V_{BUS}, and the voltage V_{SENSE} across an external current sense resistor, R_{SENSE}.

4.1.1 INITIAL OPERATION AND ACTIVE STATE

After POR and a start-up sequence, the device is in the Active state and begins sampling the inputs sequentially. Voltage and current are sampled for all active channels and power is calculated and accumulated. All active channels are sampled at 1024 samples/second by default. Sample rates of 256, 64 or eight samples/second may be programmed over I^2C or SMBus. If the SLOW pin is asserted the sample rate is eight samples per second. For sampling rates lower than 1024 samples/second, the device is in Sleep mode for a portion of the conversion cycle, which results in lower power dissipation. If fewer than four channels are active, power is also reduced.

To read accumulator data and reset the accumulators, the REFRESH command is used. To read the voltage, current, power and accumulator data without resetting the accumulators, the REFRESH_V command is used. Changes to the Control register (01h) are activated by sending either REFRESH or REFRESH_V. When a new value is written to the Control register (01h), the new values take effect at the end of the next round-robin sampling cycle following the next REFRESH or REFRESH_V command.

4.1.2 REFRESH COMMAND

The master sends the REFRESH command after changing the Control register and/or before reading accumulator data from the device. The master controls the accumulation period in this manner.

The readable registers for the V_{BUS}, V_{SENSE}, Power, accumulator outputs and accumulator count are updated by the REFRESH command and the values will be static until the next REFRESH command. These readable registers will be stable within 1 mS from sending the REFRESH command, and may be read by the master at any time up until the next REFRESH command is sent. The internal accumulator values and accumulator count will be reset by the REFRESH command, but the sampling of the inputs, data conversion and power integration is not interrupted and will continue as determined by the settings in the Control register.

Changes written to the control and configuration registers take effect 1 mS after a REFRESH command is sent. Any new commands written within this 1 mS window will be ignored and NACKed to indicate that they are ignored.

The values for V_{BUS} and V_{SENSE} measurement results and Power calculation results respond to the REFRESH command in the same fashion as the accumulators and accumulator count. The readable registers will be stable within 1 mS from sending the REFRESH command and may be read by the master at any time. The internal values continue to be updated according to the sampling plan determined by the settings in the Control register. The results that are sent to the readable registers for V_{BUS}, V_{SENSE} and Power are the values from the most recent complete conversion cycle. See **Register 6-1** REFRESH Command (Address 00h).

4.1.3 REFRESH_G COMMAND

The REFRESH_G is identical in every respect to the REFRESH command, but it is used with the I^2C General Call address (0000 000). This allows the system to issue a REFRESH command to all of the PAC1931/2/3/4 devices in the system with a single command. Then the data from this REFRESH_G command may be read device-by-device to capture a snapshot of the system power and energy for all devices. See **Register 6-12** REFRESH_G Command (Address 1Eh). Note that the REFRESH_G command can also be used with a valid Slave address but in this case only the device with this Slave address will receive the command. In other words it has the same properties as the REFRESH command with the possibility of being compatible with the I^2C General Call address.

4.1.4 REFRESH_V COMMAND

If the user wants to read V_{SENSE} and V_{BUS} results, the most recent Power calculation, and/or the accumulator values and count without resetting the accumulators, the REFRESH_V command may be sent. Sending the REFRESH_V command and waiting 1 mS ensures that the V_{SENSE}, V_{BUS}, Power, accumulator and accumulator count values will be stable when read by the master. The sampling of the inputs, data conversion and power integration are not interrupted and will continue as determined by the settings in the Control register. The data in these readable registers will remain stable until the next REFRESH or REFRESH_V command. The internal accumulator values and accumulator count are unaffected by the REFRESH_V command.

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Note that the REFRESH_V command may also be used to activate changes to the Control register, just like the REFRESH command, except with the REFRESH_V command changes to the Control register will be enacted without resetting the accumulators or accumulator count. See **Register 6-13** REFRESH_V Command (Address 1Fh).

4.1.5 SLEEP STATE

The SLEEP state is a lower power state than the Active state. While in this state, the device will draw a supply current of I_{SLEEP} from the V_{DD} pin. The device automatically goes to this state between conversion cycles when sampling rates lower than 1,024 samples/second are selected, or if fewer than four channels are active. All digital states and data are retained in the SLEEP state. The device can also be put in the Sleep state by setting the SLEEP bit followed by a REFRESH or REFRESH_V command, and sampling will resume when the SLEEP bit is cleared followed by a REFRESH of REFRESH_V command. The device does not go into SLEEP state based on any other condition such as static conditions on the SMBus pins. If SMBus Timeout is enabled, it is supported in SLEEP mode or ACTIVE mode.

4.1.6 POWER-DOWN STATE

The Power-Down state is entered by pulling the $\overline{\text{PWRDN}}$ pin low. In this state, all circuits on the chip including the SMBus pins are inactive, and the device is in a state of minimum power dissipation.

In the Power-Down state, no data is retained in the chip (neither register configuration nor measurement data). When the $\overline{\text{PWRDN}}$ pin is pulled high, integration, measurement and accumulation will begin using the default register settings, as described in **Section 4.1.1 "Initial Operation and Active State"**. The first measurement data may be requested by a REFRESH or REFRESH_V command 20 ms after the $\overline{\text{PWRDN}}$ pin is pulled high.

4.1.7 PROGRAMMING THE SAMPLE RATE AND THE SLOW PIN

The default sampling rate after power-up is 1024 samples/second. Sampling rates of 256, 64 or 8 samples/second may be programmed in the **Register 6-2** CTRL Register (Address 01h). Any time a new sample rate is programmed, it does not take effect until a REFRESH, REFRESH_G, or REFRESH_V command is received. When any of these REFRESH commands are received, any round-robin sampling cycle in progress will complete before the new sampling rate takes effect. For example, if the user is sampling at 8 SPS and program a new sample rate, it may take up to 125 mS for the new sample rate to take effect and for all the sample rate related registers (like CTRL_ACT) to show their updated values.

If one of these lower sample rates is used, power dissipation is reduced. The round-robin sampling and conversion cycle is exactly the same, but the device goes into the sleep state between conversion cycles. See **Section 2.0 "Typical Operating Curves"**.

If the SLOW pin is pulled high, the device will sample at eight samples/second. No matter what the programmed sample rate, this new SLOW sample rate will take effect on the next conversion cycle (if a round-robin conversion cycle is in process when the SLOW pin goes high, that conversion cycle will complete before the SLOW sample rate takes effect.)

If the device is programmed for Single Shot mode, and the SLOW pin is asserted, the first sampling will begin within 125 ms after the SLOW pin is asserted.

If the device is in the Sleep state, asserting the SLOW pin will not cause sampling to start.

Whenever the SLOW pin changes state, a limited REFRESH or REFRESH_V command may be executed by the chip hardware (default is REFRESH). Like any other REFRESH command, this resets the accumulators and accumulator count for a REFRESH command, and updates the readable registers for either REFRESH or REFRESH_V. These are limited REFRESH commands because no programmed changes to the Control or Status registers take effect (Control and Status registers means registers 01h, 1Ch, 1Dh, and 20h-26h). The readable registers are stable with the new values within 1 ms of the SLOW pin transition.

The Slow register enables selection of REFRESH or REFRESH_V on the SLOW pin transitions, which allows this function to be disabled for either edge, and also tracks both the state of the SLOW pin and transitions on the SLOW pin. See **Register 6-14**, SLOW (Address 20h).

This is the default functionality of the SLOW pin, but it may be reconfigured to function as an $\overline{\text{ALERT}}$ pin (see paragraph **Section 4.4 "Alert Functionality"**). If the SLOW pin is configured to serve as an $\overline{\text{ALERT}}$ pin, the slower sampling rate of eight samples/second is only available by programming the Control register 01h.

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4.2 Conversion Cycles

A conversion cycle for the device consists of analog-to-digital conversion being complete for all channels (including the real-time calibration that is part of each conversion cycle). Immediately following the data conversion, the power results are calculated for that channel and the power value is added to the accumulator. Averaged values for V_{SENSE} and V_{BUS} are also updated internally as part of each conversion cycle.

Data conversion and processing is performed for each active channel in sequential fashion until all active channels have been converted, completing the conversion cycle for the device. The sequential sampling of each channel, along with the calculation time and any sleep time needed to set the overall sampling rate, is referred to as a round-robin sampling period.

4.3 Conversion Cycle Controls

4.3.1 REDUCING THE NUMBER OF CHANNELS TO BE SAMPLED

Program **Register 6-10** CHANNEL_DIS and SMBus (Address 1Ch) to reduce the number of channels that are active. The sample rate is unaffected, but power dissipation is reduced very slightly if some channels are disabled. Any or all channels may be disabled; if all channels are disabled, the device goes into Sleep mode. When a channel is disabled due to register programming in the PAC1934, or due to factory programming on the PAC1931, PAC1932 and PAC1933, the auto-incrementing pointer will skip these channels by default (see **Section 5.5 "Auto-Incrementing Pointer"**).

4.3.2 SINGLE SHOT MODE

The Control register also allows the device to operate in Single Shot mode. In Single Shot mode, all active channels will sample and convert once, followed by results being calculated. The accumulator and accumulator count operate the same as for continuous conversion mode, accumulating each single shot power calculation and incrementing the accumulator count. The conversion cycle will start when the REFRESH command (or REFRESH_V or REFRESH_G) is sent.

After the single shot measurements and calculations are complete, the device will go into Sleep mode. A REFRESH, REFRESH_G or REFRESH_V command may be sent to read the data. The user needs to wait 3 ms after the REFRESH command before commanding another Single Shot conversion by means of sending one of the REFRESH commands. This is because a 1 ms delay is required between REFRESH commands, and coming out of Sleep requires 2 ms.

4.4 Alert Functionality

The Alert functionality can serve two purposes: to notify the system that a conversion cycle for all active channels is complete, or to notify the system that the accumulator or accumulator count has overflowed.

4.4.1 USING THE ALERT FUNCTION

To use the ALERT function, configure the SLOW pin to function as $\overline{\text{ALERT}}$ using **Register 6-2** CTRL Register (Address 01h). For this configuration, the $\overline{\text{ALERT}}$ pin must have a pull-up to V_{DD} I/O (it will function as an open drain output). If a pull-up resistor is attached to the pin for Alert functionality, the device will power up in Slow mode. Any of the four sample rates can be programmed using **Register 6-2** CTRL Register (Address 01h).

The Alert function for Accumulator Overflow can also be used without reconfiguring the SLOW pin, by monitoring the OVF bit in **Register 6-2** CTRL Register (Address 01h).

4.4.2 ALERT AFTER COMPLETE CONVERSION

Register 6-2 has an ALERT_CC bit that can be used to enable the ALERT_CC function. If this bit is set, the $\overline{\text{ALERT}}$ pin will go low for 5 µS after each complete conversion cycle is complete.

4.4.3 ALERT ON ACCUMULATOR OVERFLOW

If the ALERT function is enabled, and any of the accumulators or the accumulator count overflow, the $\overline{\text{ALERT}}$ pin may be used to notify the system. To enable this trigger for the $\overline{\text{ALERT}}$ pin, bit `1` in the **Register 6-2** CTRL Register (Address 01h) must be set. Note that the OVF bit in the **Register 6-2** CTRL Register (Address 01h) will be set when these overflows occur.

4.4.4 CLEARING ALERT AND OVF

When the Alert function has been tripped by accumulator or accumulator count overflow, it will remain asserted until a REFRESH command is received. REFRESH_G will also clear the OVF bit and the Alert function, but REFRESH_V will not.

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4.5 Voltage Measurement

The V_{BUS} voltage for each channel is measured by the SENSE+ pin for each channel. A high-voltage multiplexer is connected to each SENSE+ pin, and the multiplexer sequentially connects each SENSE+ input to an ADC for conversion. The result is stored in a 16-bit V_{BUS} results register and the 14 MSBs are multiplied by the V_{SENSE} number for the V_{POWER} results value. The V_{POWER} results are accumulated in the accumulator.

Full-Scale Voltage (FSV) is 32V by default. The device may be programmed for bipolar V_{BUS} measurements. in this bipolar mode, the mathematical range for negative V_{BUS} numbers is -32V, the actual range is limited to about -200mV due to physical factors. This bipolar capability for V_{BUS} enables accurate offset measurement and correction. For bipolar operation, the 16-bit V_{BUS} result is a two's complement (signed) number.

The measured voltage at SENSE+ can be calculated using **Equation 4-1**.

EQUATION 4-1: BUS VOLTAGE

$$V_{Source} = 32V \times \frac{V_{BUS}}{Denominator}$$

Where:

V_{SOURCE}	=	The measured voltage on the SENSE+ pin
V_{BUS}	=	The value read from the V_{BUS} results registers
Denominator	=	2^{16} for unipolar measurements
	=	2^{15} for bipolar measurements

4.6 Current Measurement

The PAC1931/2/3/4 device family includes high-side current sensing circuits. These circuits measure the voltage (V_{SENSE}) induced across a fixed external current sense resistor (R_{SENSE}) and store the voltage as a 16-bit number in the V_{SENSE} Results registers.

The PAC1931/2/3/4 current sensing operates with a Full-Scale Range (FSR) of 100 mV in unidirectional mode (default).

When sensing unidirectional currents (the default mode), the ADC results are presented in straight binary format. For bidirectional current sensing, the ADC results are in two's complement (signed) format. For bipolar current measurements, the range is ±100 mV, but use FSR = 100 mV in the equations that follow. For best accuracy on current values near zero, it is recommended to use the bidirectional current mode and 8x average current results.

4.7 Selecting R_{SENSE} Values

R_{SENSE} can easily be calculated if you know the maximum current you want to sense, as shown in **Equation 4-2**.

Consider that you may need to select a value for IMax that includes current peaks well beyond your nominal current.

EQUATION 4-2: CALCULATING R_{SENSE}

$$Rsense = \frac{FSR}{IMax}$$

Where:

FSR	=	Full Scale V_{SENSE} voltage input
R_{SENSE}	=	External R_{SENSE} resistor value
IMax	=	Maximum current to measure

Full-Scale Current (FSC) can be calculated from **Equation 4-3**.

EQUATION 4-3: FULL-SCALE CURRENT

$$FSC = \frac{100\ mV}{R_{SENSE}}$$

Where:

FSC	=	Full-scale current
R_{SENSE}	=	External sense resistor value

The actual current through R_{SENSE} can then be calculated using **Equation 4-4**.

EQUATION 4-4: SENSE CURRENT

$$I_{SENSE} = FSC \times \frac{V_{SENSE}}{Denominator}$$

Where:

I_{SENSE}	=	Actual bus current
FSC	=	Full-scale current value (from **Equation 4-3**)
V_{SENSE}	=	The value read from the V_{SENSE} results registers
Denominator	=	2^{16} for unipolar measurements
	=	2^{15} for bipolar measurements

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4.8 ADC Measurements, Offset, and 8x Averaging

The PAC1931/2/3/4 is primarily desired for energy measurements where many power readings are accumulated. This is inherently an averaging process. Individual voltage and current measurements can also benefit from averaging to reduce noise and offset. Averaged values are internally calculated for V_{BUS} and V_{SENSE}, with a rolling average of the most recent eight values present in the VBUSn_AVG (**Register 6-7**) and VSENSEn_AVG (**Register 6-6**) registers. The average is updated internally after every conversion cycle. The readable registers are updated with REFRESH, REFRESH_V, or REFRESH_G commands like all the other readable results registers. These averaged results may be used for the most accurate, lowest noise and lowest offset measurements.

The ADC channels use a special offset canceling technique. If the user observes the unaveraged results for near-zero values of V_{BUS} and V_{SENSE}, they may observe a cyclical pattern of offset variation. The user may think this is noise, but in fact it is due to internal circuitry switching through different permutations of offset cancellation circuitry. This small variation in unaveraged offset is canceled in the 8x averaged result. It is also canceled in the Power Accumulator results. The overall effect is offset that is consistently very close to zero LSB over supply and temperature variations.

The offset canceling technique is illustrated in **Figure 4-4**. It is very difficult to accurately observe, as it is a challenge to read the data from every conversion cycle. The effect of capturing data points at a rate that does not correspond exactly to the internal sampling rate of the PAC1931/2/3/4 can make these permutations appear less periodic and deterministic than they are inside the chip. The data conversion uses one of the permute positions 1-4 for each input on each conversion, cycling through all four permutations in four conversions. When averaged the Permute Enabled result shown below is realized, evenly distributed around zero.

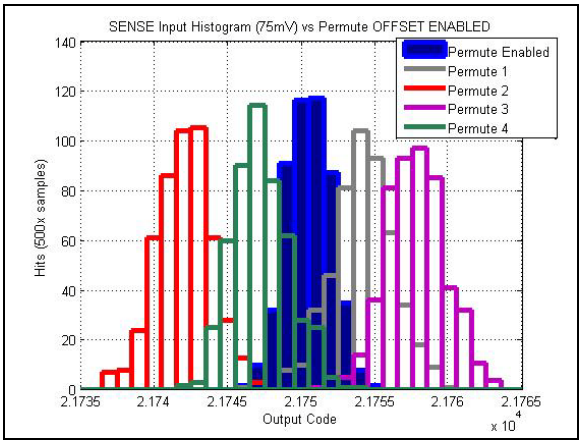


FIGURE 4-4: *Illustration of the Four Permute Combinations that the ADC Cycles through and the Resulting Low Average Offset. Each Bin Represents One Code.*

Results from both the V_{BUS} and V_{SENSE} ADCs are 17b two's complement (signed) internally. There is an additional bit of resolution that is not accessible from the results register. The NEG_PWR (Address 1Dh) register determines whether the conversion results are reported in the readable registers as unipolar or bipolar numbers. Using bipolar numbers can give more accurate results for very small numbers that may actually be negative for some readings, in addition to measuring bidirectional currents (charging/discharging) and voltages that can dip below ground.

Averaged values are also calculated for V_{BUS} and V_{SENSE}. A rolling average of the most recent eight values is present in the VBUSn_AVG (**Register 6-7**) and VSENSEn_AVG (**Register 6-6**) registers. These registers require eight conversion cycles after POR before they represent an accurate value, they are updated after every conversion cycle. The readable registers are updated with REFRESH, REFRESH_V or REFRESH_G commands like all the other readable results registers.

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4.9 Power and Energy

The Full-Scale Range for Power depends on the external sense resistor used, as shown in **Equation 4-5**.

EQUATION 4-5: POWER FSR CALCULATION

$$PowerFSR = (100\ mV / R_{SENSE}\Omega) \times 32V$$
$$= 3.2V^2 / R_{SENSE}\Omega$$

Where:

$R_{SENSE}\Omega$ = External R_{SENSE} resistor value
100 mV = Full-Scale V_{SENSE} voltage input
32V = Full-Scale V_{BUS} voltage input

The device implements Power measurements by multiplying V_{BUS} and the V_{SENSE} to give a result V_{POWER}. V_{POWER} values are used to calculate Proportional Power as shown in **Equation 4-6**. The Proportional Power is the fractional portion of Power FSR measured in one sample. Bipolar mode is where V_{BUS} is bipolar mode, V_{BUS} is bidirectional mode, or both V_{BUS} and V_{SENSE} are bipolar/bidirectional.

EQUATION 4-6: PROPORTIONAL POWER CALCULATION

$$P_{PROP} = \frac{Vpower}{Denominator}$$

Where:

Denominator = 2^{28} (unipolar mode)
= 2^{27} (bipolar mode)

To calculate the actual power from the Proportional Power, multiply by the Power FSR as shown in **Equation 4-7**. This Actual Power number is the power measured in one sample.

EQUATION 4-7: POWER CALCULATION

$$P_{actual} = PowerFSR \times P_{PROP}$$

These V_{POWER} results are digitally accumulated on chip, and stored in the VACCUM registers.

The energy calculation **Equations 4-8** and **4-9** use a different denominator term depending on unipolar or bipolar mode. Bipolar mode for energy applies when bipolar/bidirectional mode is used for V_{BUS} and/or V_{SENSE}. **Equation 4-8** shows how to realize this using the Accumulator results, Accumulator count and the accumulation period, T. In this equation, T must be known from a system clock time stamp or other accurate indicator of the total accumulation period.

EQUATION 4-8: ENERGY CALCULATION

$$Energy = \frac{V(accum)}{Denominator} \times (PwrFSR) \times \frac{T}{AccCount}$$

Where:

Denominator = 2^{28} (unipolar mode)
= 2^{27} (bipolar mode)

EQUATION 4-9: ENERGY CALCULATION

$$Energy = \frac{V(accum)}{Denominator} \times \frac{(PwrFSR)}{f_S}$$

Where:

Denominator = 2^{28} (unipolar mode)
= 2^{27} (bipolar mode)

Equation 4-9 shows how to calculate energy using the accumulated power and the sampling rate, f_S.

4.9.1 ADDITIONAL ACCUMULATOR INFORMATION

The math for the Power calculation and accumulation inside the chip is always done in two's complement math, no matter what the user sets the output registers to show. V_{BUS} and V_{SENSE} are 17-bit two's complement (signed) numbers internally. V_{POWER} is the product of V_{SENSE} multiplied by the 14 MSBs of V_{BUS}, and this is a 31 bit two's complement result (signed) internally. In some cases this results in a Power result that is not identical to the product of the V_{BUS} results register multiplied by the V_{SENSE} register. However, the Power result from the Power results register is more accurate than the product of the V_{BUS} register multiplied by the V_{SENSE} register in these cases, as explained below.

If V_{SENSE} and V_{BUS} are both programmed to be unsigned (unipolar) in register NEG_PWR (Address 1Dh), 16b without sign are exported to V_{BUS} and V_{SENSE} results registers.

If V_{BUS} is programmed to be signed (bipolar) in **Register 6-11** NEG_PWR (Address 1Dh), the corresponding data is truncated to 16-bit two's complement (signed) for the readable results register.

If V_{SENSE} is programmed to be signed (bipolar) in register NEG_PWR (Address 1Dh), the corresponding results register value is truncated to 16-bit two's complement (signed), but the power calculation uses 17-bit two's complement (signed). Therefore, a mismatch is possible between an externally calculated power value (V_{BUS} times V_{SENSE}) and the actual power value calculated internally to the chip. The internally calculated (and accumulated) value is more accurate than the externally calculated value in every case.

The continuous power integration periods (also called the energy accumulation period) can range from ~1ms to many hours, depending on the number of samples per second selected via SMBus. The number of samples is limited by the size of the Accumulator Count register to 16,777,216 (2^{24}). This count corresponds to about 273 minutes at 1024 samples/second, or 582 hours at eight samples/second. This Accumulator Count can overflow, and it will not reset when it overflows.

When the accumulation registers reach their maximum value, this is called accumulator overflow. The accumulator outputs remain at their maximum value; they do not roll over. The user can calculate the worst-case time to roll over and read them at or before that time or use the built in Alert functions to detect rollover and read them at that time.

Worst-case accumulator overflow time can be calculated assuming that every measurement that is accumulated is a full-scale number. Since the power numbers are 28 bits, and the accumulator is 48 bits, 2^{20} samples can be accumulated before overflow if they are all full-scale values. For most applications, they will not all be full-scale numbers; this is especially true if V_{BUS} is not 32V. If V_{BUS} is a lower number, the maximum number of full-scale samples that can be accumulated is scaled by $32V/V_{BUS}$. This limitation can limit the accumulation period before overflow to 17 minutes at 1024 samples/second, or 36 hours at eight samples/second, if most values are near full-scale. The Accumulator Count limit described above will still limit the total number of samples to 2^{24}.

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NOTES:

5.0 SMBUS AND I²C COMMUNICATIONS PROTOCOL

The PAC1931/2/3/4 communicates over a two-wire bus with a controller using SMBus or I²C serial communication protocol. A detailed timing diagram is shown in **Figure 1-1**.

Stretching of the SMCLK signal is supported; however, the PAC1931/2/3/4 will not stretch the clock signal.

5.1 I²C/SMBus Addressing and Control Bits

5.1.1 SMBUS ADDRESS AND RD/$\overline{WR}$ BIT

The SMBus Address Byte consists of the 7-bit slave address followed by a 1-bit RD / $\overline{WR}$ indicator. If this RD / $\overline{WR}$ bit is a logic '0', the SMBus master is writing data to the slave device. If this RD / $\overline{WR}$ bit is a logic '1', the SMBus master is reading data from the slave device.

The PAC1931/2/3/4 I²C/SMBus address is determined by a single pull-down resistor connected between ground and the ADDRSEL pin as shown in **Table 5-1**. The chip translates the resistor value into an address on power-up, and the value is latched until another power-up event takes place. The address cannot be changed on the fly.

5.1.2 SMBUS START BIT

The SMBus Start bit is defined as a transition of the SMBus data line from a logic '1' state to a logic '0' state while the SMBus Clock line is in a logic '1' state.

5.1.3 SMBUS ACK AND NACK BITS

The SMBus slave will ACK (acknowledge) all data bytes that it receives. This is done by the slave device pulling the SMBus data line low after the eighth bit of each byte that is transmitted.

5.1.4 SMBUS STOP BIT

The SMBus Stop bit is defined as a transition of the SMBus data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the PAC1931/2/3/4 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its slave interface and prepare to receive further communications.

5.1.5 SMBUS DATA BYTES

All SMBus data bytes are sent most significant bit first and composed of eight bits of information.

TABLE 5-1: ADDRESS SELECT RESISTOR

Resistor (1%)	SMBus Address
0 (Tie to GND)	0010_000(r/w)
499	0010_001(r/w)
806	0010_010(r/w)
1,270	0010_011(r/w)
2,050	0010_100(r/w)
3,240	0010_101(r/w)
5,230	0010_110(r/w)
8,450	0010_111(r/w)
13,300	0011_000(r/w)
21,500	0011_001(r/w)
34,000	0011_010(r/w)
54,900	0011_011(r/w)
88,700	0011_100(r/w)
140,000	0011_101(r/w)
226,000	0011_110(r/w)
Tie to V_{DD}	0011_111(r/w)

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5.2 SMBus Time-Out

The PAC1931/2/3/4 can support the SMBus Time-Out functionality. This functionality is disabled by default, and can be enabled by writing to the Timeout bit (see **Register 6-10** CHANNEL_DIS and SMBus (Address 1Ch).

If Time-Out is enabled and the clock is held at logic '0' for $t_{TIMEOUT}$ = 25-43 ms, the device will time-out and reset the SMBus interface. Communication is restored with a start condition.

5.3 SMBus and I²C Compatibility

The PAC1931/2/3/4 is compatible with SMBus 3.0 1 MHz class and I²C Fast-mode Plus. The major differences between SMBus and I²C devices are highlighted here. For more information, refer to the SMBus 3.0 and I²C specifications.

1. If Time-Out function is enabled, the minimum frequency for SMBus communications is 10 kHz. If Time-Out function is disabled (default condition), then there is no minimum frequency for SMBus communications.
2. If SMBus Time-Out is enabled in **Register 6-10**: CHANNEL_DIS and SMBus (Address 1Ch),the SMBus slave protocol will reset if the clock is held at a logic '0' for $t_{TIMEOUT}$. I²C does not have a time-out, this is the default condition.
3. I²C devices do not support the Alert Response Address functionality (which is optional for SMBus).The PAC1931/2/3/4 does not support the Alert Response Address functionality; instead, the $\overline{\text{ALERT}}$ is a GPIO pin that may be monitored by the master or Embedded Controller.
4. I²C devices support Block Read and Block Write differently. I²C protocol allows for unlimited number of bytes to be sent in either direction. The SMBus protocol for Block Read and Block Write requires that an additional data byte indicating number of bytes to read/write is transmitted. PAC1931/2/3/4 devices support the I²C protocol for Block Read by default (no byte count information is sent). If the Byte Count bit is set (see **Register 6-10**: CHANNEL_DIS and SMBus (Address 1Ch), it will be sent as the first data byte in response to the Block Read command, per SMBus protocol.

5.4 I²C/SMBus Protocols

The PAC1931/2/3/4 supports Write Byte, Read Byte, Block Read, Send Byte and Receive Byte as valid protocols.

It will not respond to the Alert Response Address protocol. It will respond to the I²C General Call Address.

All of the protocol charts listed below use the convention in **Table 5-2**.

TABLE 5-2: PROTOCOL FORMAT

Data Sent to Device	Data Sent to the Master
# of bits sent	# of bits sent

5.5 Auto-Incrementing Pointer

The PAC1931/2/3/4 has an auto-incrementing address pointer. The pointer has two loops for auto-incrementing, a read loop and a write loop.

The read loop includes all of the readable registers, including all of the configuration and Control registers, the results registers, and the Product ID, Manufacturer ID and Revision ID registers.

The write loop includes only the writable control and configuration registers.

Neither loop includes the REFRESH commands.

The read loop will skip inactive channels, if some channels have been disabled. This automatic channel skipping feature can be disabled by setting the No Skip bit in **Register 6-10**: CHANNEL_DIS and SMBus (Address 1Ch).

If the user elects to read disabled channels, they will return FFh and the register address will by NACKed.

See **Figure 5-1** for a graphic representation.

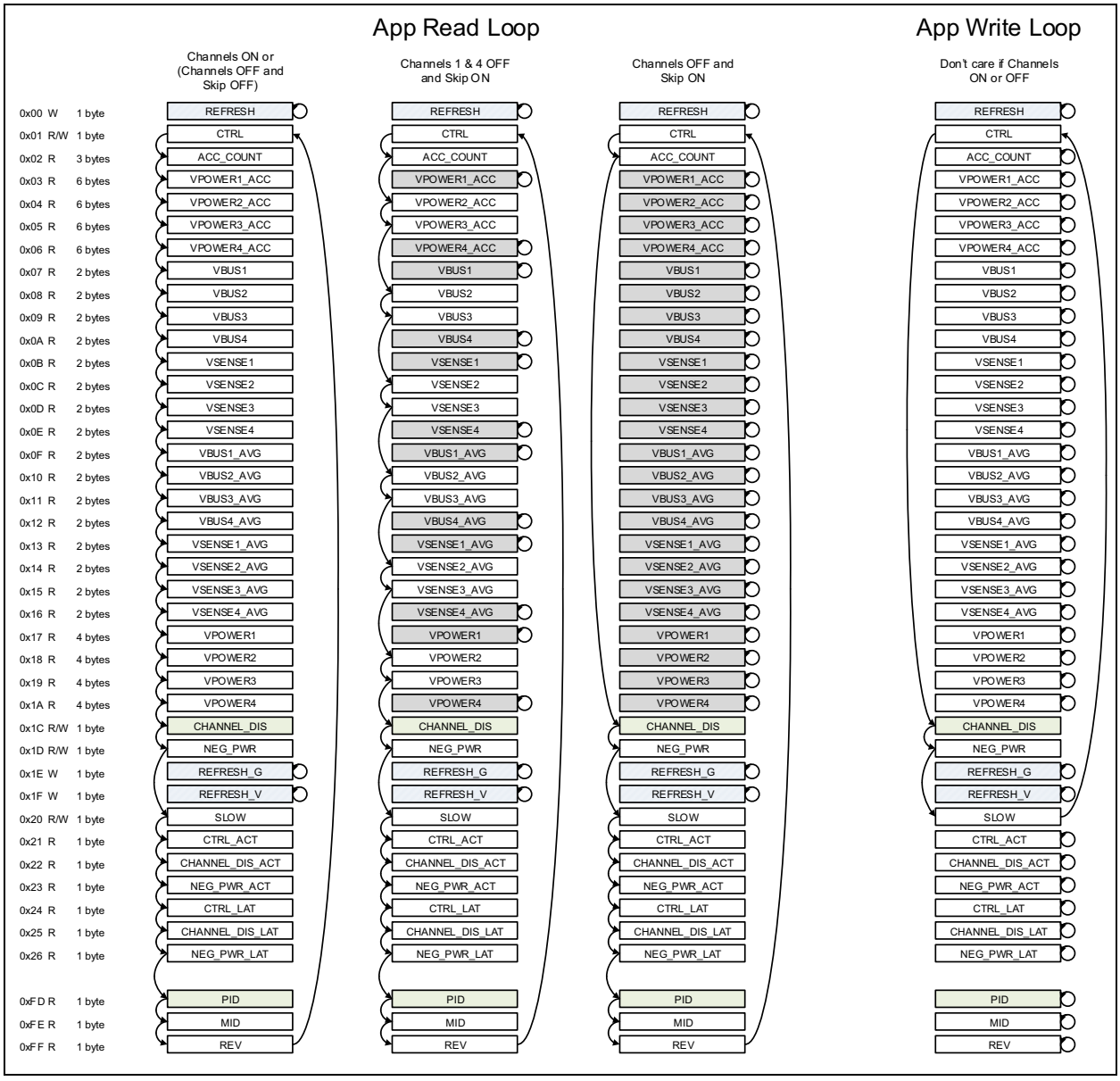


FIGURE 5-1: *READ and WRITE Auto Incrementing Loops.*

Figure 5-1 shows how the auto-incrementing READ loop works with SKIP option on and off, for reading. It also shows how the WRITE loop works with the REFRESH, REFRESH_V, and REFRESH_G commands.

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5.6 I²C/SMBus Commands

5.6.1 REFRESH AND REFRESH_V

REFRESH and REFRESH_V commands are sent using the Send byte command, the Slave Address and the desired command (00h for REFRESH or 1Fh for REFRESH_V. See **Table 5-3**.

TABLE 5-3: REFRESH AND REFRESH_V COMMANDS

START	Slave Address	WR	ACK	REFRESH or REFRESH_V Command	ACK	STOP
1 → 0	YYYY_YYY	0	0	00h or 1Fh	0	0 → 1

5.6.2 GENERAL CALL ADDRESS RESPONSE

When the master sends the General Call address, the PAC1931/2/3/4 will be able to execute the REFRESH command by means of a second version of the REFRESH command called REFRESH_G (see **Register 6-12** REFRESH_G Command (Address 1Eh)).

Just as the REFRESH command is sent using a Send Byte command with the slave address, and the REFRESH command (00h), the REFRESH_G command is sent using Send Byte with the General Call address (0000 000) and the REFRESH_G command (1Eh).

Table 5-4 shows the response to the General Call command for REFRESH_G.

TABLE 5-4: GENERAL CALL RESPONSE

START	General Call Address	WR	ACK	REFRESH_G Command	ACK	STOP
1 → 0	0000_000	0	0	1Eh	0	0 → 1

5.6.3 WRITE BYTE

The Write Byte is used to write one byte of data to the registers, as shown in **Table 5-5**.

TABLE 5-5: WRITE BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	Register Data	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 → 1

5.6.4 READ BYTE

The Read Byte protocol is used to read one byte of data from the registers, as shown in **Table 5-6**.

If an invalid register address is specified, the slave will ACK its address but NACK (not acknowledge) the register address.

The master will NACK the data received from the slave by holding the SMBus data line high after the eighth data bit has been sent.

TABLE 5-6: READ BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

5.6.5 SEND BYTE

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol, as shown in **Table 5-7**.

TABLE 5-7: SEND BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	0 → 1

5.6.6 RECEIVE BYTE

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g., set via Send Byte). This is shown in **Table 5-8**.

When an ACK is received after the REGISTER DATA, then the address pointer automatically increments.

When a NACK is received after the REGISTER DATA, then the address pointer stays at the same position.

If the master wishes to continue clocking and read the next register, the master will ACK after the register data, instead of sending NACK followed by STOP.

If some channels are deactivated, their data registers will be skipped by the auto-incrementing pointer. Alternatively, you may set bit 0 in **Register 6-10** CHANNEL_DIS and SMBus (Address 1Ch) and the pointer will not skip the addresses associated with the inactive channels. The measurement data for these inactive channels will read FFh.

TABLE 5-8: RECEIVE BYTE PROTOCOL

START	Slave Address	RD	ACK	Register Data	NACK	STOP
1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

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5.6.7 BLOCK READ – I²C VERSION

Block Read is used to read multiple data bytes from a register that contains more than one byte of data, or from a group of contiguous registers, as shown in **Table 5-9**. The PAC1931/2/3/4 supports I²C Block Read by default, but the SMBus format can also be supported (see **Table 5-10**).

If an invalid register address is specified, the slave will ACK its address but NACK the register address.

The master will NACK the data received from the slave by holding the SMBus data line high after the 8th data bit has been sent.

TABLE 5-9: BLOCK READ PROTOCOL I²C VERSION (DEFAULT)

START	Slave Address	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data
1 → 0	YYYY_YYY	0	0	XXh	0	1 → 0	YYYY_YYY	1	0	XXh
ACK	**Register Data**	**ACK**	**Register Data**	**ACK**	**Register Data**	**ACK**		**Register Data**	**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	0		XXh	1	0 → 1

5.6.8 BLOCK READ – SMBUS VERSION

PAC1931/2/3/4 can also support the SMBus version of Block Read. If the Byte Count bit is set, Block Read will result in the device sending the Byte Count data before the first data byte. This protocol is shown in **Table 5-10**. Also see **Section 4.3 "Conversion Cycle Controls"** above and **Register 6-10** CHANNEL_DIS and SMBus (Address 1Ch).

TABLE 5-10: BLOCK READ PROTOCOL SMBUS VERSION (MUST SET BYTE COUNT BIT)

START	Slave Address	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Byte Count
1 → 0	YYYY_YYY	0	0	XXh	0	1 → 0	YYYY_YYY	1	0	XXh = N
ACK	**Register Data**	**ACK**	**Register Data**	**ACK**	**Register Data**	**ACK**		**Register Data**	**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	0		XXh	1	0 → 1

6.0 REGISTERS IN HEXADECIMAL ORDER

The registers shown in **Table 6-1** are accessible through the SMBus. In the individual register tables that follow, an entry of '—' indicates that the bit is not used and will always read '0'.

Data represented by the data registers are ensured to be synchronized and stable 1 ms after any of the REFRESH commands are sent. Immediately after the REFRESH commands are sent, the data bytes will be changing dynamically until 1 ms has elapsed. When new data is written to a Control register, and the master reads it back, this new data will be read back even if no REFRESH command has been sent to cause the new data to take effect.

Note: The letter N or n is used to represent 1,2,3,4 in the register and bit names below, in sections that describe registers that are grouped for all four channels.

Note: For PAC1931, channels 2, 3 and 4 do not contain valid data and will read FF. Also, for PAC1932, channels 3 and 4 do not contain valid data and will read FF. The auto-incrementing pointer will skip these channels by default (see **Section 5.5 "Auto-Incrementing Pointer"**). The same applies to channel 4 for the PAC1933.

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER

Register Number	Description	Type	Bytes	POR Value
Register 6-1 REFRESH Command (Address 00h)	Send Byte for REFRESH command	SEND	0	00h
Register 6-2 CTRL Register (Address 01h)	Configuration controls and status	R/W	1	00h
Register 6-3 ACC_COUNT Register (Address 02h)	Accumulator count for all channels	Block Read	3	000000h
Register 6-4 VPOWERN Accumulator Registers: VPOWER1_ACC(03h), VPOWER2_ACC (04h), VPOWER3_ACC (05h), VPOWER4_ACC (06h)	Accumulator output for channel 1	Block Read	6	**Note 1**
	Accumulator output for channel 2	Block Read	6	**Note 1**
	Accumulator output for channel 3	Block Read	6	**Note 1**
	Accumulator output for channel 4	Block Read	6	**Note 1**

Note 1: The VPOWERN Accumulator Registers, 03h-06h, have a POR value that is all zeros: 6 bytes → 000000000000h.

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TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Number	Description	Type	Bytes	POR Value
Register 6-5 VBUSN Result Registers VBUS1 (07h), VBUS2 (08h), VBUS3 (09h),VBUS4 (0Ah)	V_{BUS} measurement for channel 1	Block Read	2	0000h
	V_{BUS} measurement for channel 2	Block Read	2	0000h
	V_{BUS} measurement for channel 3	Block Read	2	0000h
	V_{BUS} measurement for channel 4	Block Read	2	0000h
Register 6-6 VSENSEn Result Registers: VSENSE1 (0Bh), VSENSE2 (0Ch), VSENSE3 (0Dh), VSENSE4 (0Eh)	V_{SENSE} measurement for channel 1	Block Read	2	0000h
	V_{SENSE} measurement for channel 2	Block Read	2	0000h
	V_{SENSE} measurement for channel 3	Block Read	2	0000h
	V_{SENSE} measurement for channel 4	Block Read	2	0000h
Register 6-7 VBUSN_AVG Result Registers VBUS1_AVG (0Fh), VBUS2_AVG (10h), VBUS3_AVG (11h), VBUS4_AVG (12h)	Rolling average of eight most recent V_{BUS1} measurements	Block Read	2	0000h
	Rolling average of eight most recent V_{BUS2} measurements	Block Read	2	0000h
	Rolling average of eight most recent V_{BUS3} measurements	Block Read	2	0000h
	Rolling average of eight most recent V_{BUS4} measurements	Block Read	2	0000h
Register 6-8 VSENSEn AVG Result Register VSENSE1_AVG (13h), VSENSE2_AVG (14h), VSENSE3_AVG(15h), VSENSE4_AVG (16h)	Rolling average of eight most recent V_{SENSE1} measurements	Block Read	2	0000h
	Rolling average of eight most recent V_{SENSE2} measurements	Block Read	2	0000h
	Rolling average of eight most recent V_{SENSE3} measurements	Block Read	2	0000h
	Rolling average of eight most recent V_{SENSE4} measurements	Block Read	2	0000h
Register 6-9 VPOWERN Result Register: VPOWER1 (17h), VPOWER2 (18h), VPOWER3 (19h), VPOWER4 (1Ah)	V_{SENSE} x V_{BUS} for Channel 1	Block Read	4	00000000h
	V_{SENSE} x V_{BUS} for Channel 2	Block Read	4	00000000h
	V_{SENSE} x V_{BUS} for Channel 3	Block Read	4	00000000h
	V_{SENSE} x V_{BUS} for Channel 4	Block Read	4	00000000h
Register 6-10 CHANNEL_DIS and SMBus (Address 1Ch)	Disable selected channels, activate SMBus functionality, pointer increment	R/W	1	PAC1931: 70h PAC1932: 30h PAC1933: 10h PAC1934: 00h
Register 6-11 NEG_PWR (Address 1Dh)	Configuration control for enabling bidirectional current and bipolar voltage measurements	R/W	1	00h

Note 1: The VPOWERN Accumulator Registers, 03h-06h, have a POR value that is all zeros: 6 bytes → 000000000000h.

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Number	Description	Type	Bytes	POR Value
Register 6-12 REFRESH_G Command (Address 1Eh)	REFRESH response to General Call Address	SEND	0	N/A
Register 6-13 REFRESH_V Command (Address 1Fh)	Refreshes $V_{BUS\ and}$ V_{SENSE} data only, no accumulator reset	SEND	0	N/A
Register 6-14 SLOW (Address 20h)	Status and control for SLOW pin functions	R/W	1	15h
Register 6-15 CTRL_ACT Register (Address 21h)	Currently active value of 01h (Control)	R	1	00h
Register 6-16 Channel DIS_ACT (Address 22h)	Currently active value of 1Ch (CHANNEL_DIS and SMBus)	R	1	00h
Register 6-17 NEG_PWR_ACT (Address 23h)	Currently active value of 1Dh(NEG_PWR)	R	1	00h
Register 6-18 CTRL_LAT Register (Address 24h)	Latched image of 21h (CTRL_ACT)	R	1	00h
Register 6-19 Channel DIS_LAT (Address 25h)	Latched image of 22h (Channel DIS_ACT)	R	1	00h
Register 6-20 NEG_PWR _LAT (Address 26h)	Latched image of 23h (NEG_PWR_ACT)	R	1	00h
Register 6-21 Product ID Register (Address FDh)	Stores the Product ID	R	1	See register details
Register 6-22 Manufacturer ID Register (Address FEh)	Stores the Manufacturer ID	R	1	5Dh
Register 6-23 Revision ID Register (Address FFh)	Stores the revision	R	1	03h

Note 1: The VPOWERN Accumulator Registers, 03h-06h, have a POR value that is all zeros: 6 bytes → 000000000000h.

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6.1 Detailed Register Information

REGISTER 6-1: REFRESH COMMAND (ADDRESS 00H)

SEND	SEND	SEND	SEND	SEND	SEND	SEND	SEND
No Data in this command, Send Byte only							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 This command is a SEND Byte, does not contain any data. When it is sent to the device, the REFRESH command is executed. The accumulator data, accumulator count, V_{BUS}, and V_{SENSE} measurements are all refreshed and the accumulators are reset. The master can read the accumulator data and accumulator count anytime 1 ms after the REFRESH command is sent, and anytime after than up until the next REFRESH command is sent. (The master can read V_{BUS} and V_{SENSE} data in the same time period. The accumulator results, accumulator count, V_{BUS} and V_{SENSE} data can be refreshed with the REFRESH_V command without resetting the accumulators, see **Register 6-7**).

REGISTER 6-2: CTRL REGISTER (ADDRESS 01H)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	R-0
Sample_Rate[1:0]		SLEEP	SING	ALERT_PIN	ALERT_CC	OVF ALERT	OVF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 Write to these bits to change settings from default value.

bit 7-6 **Sample_Rate[1:0]**: determines sample rate in Normal mode (if SLOW pin is not asserted).

00b = 1024 samples/s

01b = 256 samples/s

10b = 64 samples/s

11b = 8 samples/s

bit 5 **SLEEP**: setting this bit to 1, followed by the REFRESH or REFRESH_V command, puts the device in SLEEP mode. All programmed, readable, and measured digital data is stable in this mode. Clearing the SLEEP bit and sending a REFRESH or REFRESH_V command causes the device become active and start converting in the mode specified by the Control registers (unless the SLOW pin is asserted, in which case it will start converting at an 8 Hz rate). The SLEEP bit has higher priority than the SING bit or the SLOW pin, if the SLEEP bit is set the device goes into SLEEP mode not matter how the SING bit or the SLOW pin are set.

0 = Active mode

1 = SLEEP mode, no data conversion

REGISTER 6-2: CTRL REGISTER (ADDRESS 01H) (CONTINUED)

bit 4 **SING**: setting this bit to 1 puts the device in Single-shot mode. After writing this bit and sending a REFRESH command, the device resets the accumulators and performs one conversion cycle for any and all active channels, then returns to sleep mode. Another REFRESH command, without changing this bit, will perform another single-shot command. When the bit is cleared, sending a REFRESH command resets the accumulators and causes the device to start converting in the sequential scan mode for active channels. A REFRESH_V command may be used instead of REFRESH to move in and out of Single Shot mode without resetting the accumulators and accumulator count.

0 = Sequential scan mode

1 = Single-shot mode

bit 3 **ALERT_PIN**: setting this bit to 1 causes the SLOW pin to function as an ALERT pin (active low output pin). If this bit is set to 1, the ALERT pin can be triggered by conversion complete if bit 2 is set.

If this bit is set to 1, and the Overflow ALERT enable bit is set to 1, the ALERT pin will be triggered by accumulator or accumulator count overflow (see bit 1 and bit 0 descriptions directly below).

Note that bit 3 only determines the functionality of this pin, SLOW or ALERT, it does not influence the ALERT functionality. If there is a pull-up resistor connected to the pin for ALERT functionality, the device will initially power-up in SLOW mode. Once bit 3 is set to enable ALERT functionality, the conversion rate will change to either the default or programmed value.

0 = Disable the $\overline{\text{ALERT}}$ pin function

1 = Enable the $\overline{\text{ALERT}}$ pin function

bit 2 **ALERT_CC**: setting this bit to 1 causes the $\overline{\text{ALERT}}$ pin to be asserted for 5 µS at the end of each conversion cycle.

0 = No ALERT on Conversion Cycle Complete

1 = ALERT function asserted for 5 µS on each completion of the conversion cycle

Note: If this bit and the OVF ALERT bit are set, OVF ALERT dominates. EOC alerts will not be seen on the ALERT pin if OVF ALERT = 1.

bit 1 **OVF ALERT**: Overflow ALERT enable. If this bit is set and any of the accumulators or the accumulator counter overflow, the ALERT function will be triggered. This will be reflected in bit 0 of this register, and if bit 3 is set to 1, the $\overline{\text{ALERT}}$ pin will be triggered (sent low).

The ALERT function is cleared by REFRESH or REFRESH_G.

0 = no ALERT if accumulator or accumulator counter overflow has occurred.

1 = $\overline{\text{ALERT}}$ pin triggered if accumulator or accumulator counter has overflowed

If this bit and the ALERT_CC bit are set, OVF ALERT dominates. EOC alerts will not be seen on the ALERT pin if OVF ALERT =1.

bit 0 **OVF**: Overflow indication status bit, this bit will be set to 1 if any of the accumulators or the accumulator counter overflows.This bit is by cleared REFRESH or REFRESH_G. These commands also clear the ALERT function.

0 = no accumulator or accumulator counter overflow has occurred

1 = accumulator or accumulator counter has overflowed

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REGISTER 6-3: ACC_COUNT REGISTER (ADDRESS 02h)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ACC_COUNT[23:16]							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ACC_COUNT[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ACC_COUNT[7:0]							
bit 7			bit0				bit0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-0 **ACC_COUNT[23:0]**: contain the count for each time a power result has been summed in the accumulator

REGISTER 6-4: VPOWERN ACCUMULATOR REGISTERS: VPOWER1_ACC(03h), VPOWER2_ACC (04h), VPOWER3_ACC (05h), VPOWER4_ACC (06h)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWERn[47:40]							
bit 47							bit 40

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWERn[39:32]							
bit 39							bit 32

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWERn[31:24]							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWERn[23:16]							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWERn[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWERn[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 47-0 **VPOWERn_ACC[47:0]**: contain the accumulated sum of V_{POWER} samples, where n = 1 to 4, depending on device. These are 48 bit unsigned numbers unless either V_{BUS} or V_{SENSE} are configured to have a bipolar range. In that case they will be 48-bit two's complement (signed) numbers.

Note that power is always calculated and accumulated using signed numbers for V_{BUS} and V_{SENSE}, but if both V_{BUS} and V_{SENSE} are in the default unipolar mode, power is reported as an unsigned number. This can lead to very small discrepancies between a manual comparison of the product of V_{BUS} and V_{SENSE} and the results that the chip calculates and accumulates for V_{POWER}. The digital math in the chip uses more bits than the reported results for V_{BUS} and V_{SENSE}, so the results registers for V_{POWER} and Accumulated Power will in some cases have a more accurate number than calculations using the results registers for V_{SENSE} and V_{BUS} will provide.

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REGISTER 6-5: VBUSN RESULT REGISTERS VBUS1 (07h), VBUS2 (08h), VBUS3 (09h),VBUS4 (0Ah)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VBUSn[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VBUSn[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **VBUSn[15:0]**: contain the most recent digitized value of a V_{BUS} sample, where n = 1 to 4, depending on device. These are 16 bit unsigned numbers unless V_{BUS} is configured to have a bipolar range. In that case they will be 16-bit two's complement (signed) numbers.

REGISTER 6-6: VSENSEn RESULT REGISTERS: VSENSE1 (0Bh), VSENSE2 (0Ch), VSENSE3 (0Dh), VSENSE4 (0Eh)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSENSEn[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSENSEn[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **VSENSEn[15:0]**: contain the most recent digitized value of V_{SENSE} samples, where n = 1 to 4, depending on device. These are 16 bit unsigned numbers unless V_{SENSE} is configured to have a bipolar range. In that case they will be 16-bit two's complement (signed) numbers.

REGISTER 6-7: VBUSN_AVG RESULT REGISTERS VBUS1_AVG (0FH), VBUS2_AVG (10H), VBUS3_AVG (11H), VBUS4_AVG (12H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VBUSn_AVG[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VBUSn_AVG[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **VBUSn_AVG[15:0]**: contain a rolling average of the eight most recent V_{BUS} measurements. They have the same format as the values in the V_{BUS} registers.

REGISTER 6-8: VSENSEn AVG RESULT REGISTER VSENSE1_AVG (13H), VSENSE2_AVG (14H), VSENSE3_AVG(15H), VSENSE4_AVG (16H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSENSEn_AVG[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSENSEn_AVG[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **VSENSEn_AVG[15:0]**: contain a rolling average of the eight most recent V_{SENSE} results. They have the same format as the values in the V_{SENSE} registers.

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REGISTER 6-9: VPOWERN RESULT REGISTER: VPOWER1 (17H), VPOWER2 (18H), VPOWER3 (19H), VPOWER4 (1AH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWERn[27:20]							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWERn[19:12]							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWERn[11:4]							
bit 15							bit 8

R-0	R-0	R-0	R-0	U	U	U	U
VPOWERn[3:0]				—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **VPOWERn[27:0]**: these registers contain the product of V_{BUS} (14 MSBs) and V_{SENSE} which represents Proportional Power for each channel.These are 28 bit unsigned numbers unless either V_{BUS} or V_{SENSE} are configured to have a bipolar range. In that case they will be 28-bit two's complement (signed) numbers.These are the numbers that are accumulated in the accumulators.

Note that power is always calculated using signed numbers for V_{BUS} and V_{SENSE}, but if both V_{BUS} and V_{SENSE} are in the default unipolar mode, power is reported as an unsigned number. This can lead to very small discrepancies between a manual comparison of the product of V_{BUS} and V_{SENSE} and the results that the chip calculates for V_{POWER}.The digital math in the chip uses more bits than the reported results for V_{BUS} and V_{SENSE}, so the results registers for V_{POWER} and Accumulated Power will in some cases have a more accurate number than calculations using the results registers for V_{SENSE} and V_{BUS} will provide.

bit 3-0 Not used at this time, always reads '0'

REGISTER 6-10: CHANNEL_DIS AND SMBUS (ADDRESS 1CH)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	U
CH1_OFF	CH2_OFF	CH3_OFF	CH4_OFF	TIMEOUT	BYTE COUNT	NO SKIP	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **CHn_OFF[7:4]**: allows one or more channels to be inactive during the conversion cycle. These settings apply for normal continuous round-robin conversion cycles or Single-Shot mode, if Single-Shot mode is selected. Note that if a channel is set to inactive, the auto incrementing address pointer will skip addresses associated with that channel unless the Pointer Skipping bit `1` in this register is set.

Changes to bits 7-4 do not take effect until a REFRESH, REFRESH_V, or REFRESH_G command are sent.

Changes to bits 3-1 take place as soon as a new value is written, they are not gated by a REFRESH command like most other control bits.

bit 7 `0` = CH1 ON. Channel 1 active during conversion cycle

`1` = CH1 OFF. Channel 1 inactive during conversion cycle

bit 6 `0` = CH2 ON. Channel 2 active during conversion cycle

`1` = CH2 OFF. Channel 2 inactive during conversion cycle (for PAC1931, this bit is set to '`1`' with factory trim. Although you can program this bit to a '`1`' for PAC1931, you will not be able to read the data from this channel).

bit 5 `0` = CH3 ON. Channel 3 active during conversion cycle

`1` = CH3 OFF. Channel 3 inactive during conversion cycle (for PAC1931 and PAC1932, this bit is set to '`1`' with factory trim. Although you can program this bit to a '`1`' for PAC1931 and PAC1932, you will not be able to read the data from this channel).

bit 4 `0` = CH4 ON. Channel 4 active during conversion cycle

`1` = CH4 OFF. Channel 4 inactive during conversion cycle (for PAC1931, PAC1932 and PAC1933, this bit is set to '`1`' with factory trim. Although you can program this bit to a '`1`' for PAC1931, PAC1932 and PAC1933, you will not be able to read the data from this channel).

bit 3 **TIMEOUT**: Timeout enable bit. The SMBus timeout is disabled by default, and is enabled by setting this bit.

`0` = No SMBus timeout feature

`1` = SMBus timeout feature is available

bit 2 **BYTE COUNT**: causes Byte Count data to be included in the response to the SMBus Block Read command for each register read. This functionality is disabled by default, and Block Read corresponds to I^2C protocol.

`0` = No Byte Count in response to a `Block Read` command

`1` = Data in response to a `Block Read` command includes the Byte Count data

bit 1 **NO SKIP**: controls the auto-incrementing of the address pointer for channels that are inactive

`0` = The auto-incrementing pointer will skip over addresses used by/for channels that are inactive

`1` = The auto-incrementing pointer will not skip over addresses used by/for channels that are inactive. With this setting, these channels that are disabled will read `0xFF` if read.

bit 0 Unimplemented bits always read '`0`'

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REGISTER 6-11: NEG_PWR (ADDRESS 1DH)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
CH1_BIDI	CH2_BIDI	CH3_BIDI	CH4 BIDI	CH1_BIDV	CH2_BIDV	CH3_BIDV	CH4_BIDV
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **CHn_BIDI[7:4]**: these control bits allow the user to enable bidirectional current measurements for any channel, which will result in the V_{SENSE} voltage measurement data being in 16-bit two's complement (signed) format. If the channel is enabled for negative current measurements, the full scale range for V_{SENSE} is -100 mV to +100 mV.

If these bits are enabled for any channel, that channel's power numbers are also capable of reporting bidirectional numbers in two's complement format.

bit 3-0 **CHn_BIDI[3:0]**: these control bits allow the user to enable bidirectional/bipolar voltage measurements for any channel, which will result in the V_{BUS} voltage measurement data being in 16 bit two's complement format.

If the channel is enabled for negative voltage measurements, the full scale range for V_{BUS} is +32V to -32V. Note that this range is the digital FSR, the V_{BUS} input will not give accurate measurements if taken more than 200 mV below ground.

If these bits are enabled for any channel, that channel's power numbers are also capable of reporting bidirectional numbers in two's complement format.

bit 7 0 = Channel 1 V_{SENSE} ADC converts 0 to +100 mV range with 16-bit straight binary output
1 = Channel 1 V_{SENSE} ADC converts -100 mV to +100 mV range with 16-bit two's complement output

bit 6 0 = Channel 2 V_{SENSE} ADC converts 0 to +100 mV range with 16 bit straight binary output
1 = Channel 2 V_{SENSE} ADC converts -100 mV to +100 mV range with 16 bit two's complement output

bit 5 0 = Channel 3 V_{SENSE} ADC converts 0 to +100 mV range with 16-bit straight binary output
1 = Channel 3 V_{SENSE} ADC converts -100 mV to +100 mV range with 16-bit two's complement output

bit 4 0 = Channel 4 V_{SENSE} ADC converts 0 to +100 mV range with 16-bit straight binary output
1 = Channel 4 V_{SENSE} ADC converts -100 mV to +100 mV range with 16 bit two's complement output

bit 3 0 = Channel 1 V_{BUS} ADC converts 0 to +32V range with 16-bit straight binary output
1 = Channel 1 V_{BUS} ADC converts -32V to +32 range with 16-bit two's complement output

bit 2 0 = Channel 2 V_{BUS} ADC converts 0 to +32V range with 16-bit straight binary output
1 = Channel 2 V_{BUS} ADC converts -32V to +32V range with 16-bit two's complement output

bit 1 0 = Channel 3 V_{BUS} ADC converts 0 to +32V range with 16-bit straight binary output
1 = Channel 3 V_{BUS} ADC converts -32V to +32V range with 16-bit two's complement output

bit 0 0 = Channel 4 V_{BUS} ADC converts 0 to +32V range with 16-bit straight binary output
1 = Channel 4 V_{BUS} ADC converts -32V to +32V range with 16-bit two's complement output

REGISTER 6-12: REFRESH_G COMMAND (ADDRESS 1EH)

SEND	SEND	SEND	SEND	SEND	SEND	SEND	SEND
No Data in this command, Send Byte only							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 This command is a SEND Byte, does not contain any data. It is exactly like the REFRESH command but is intended for use with the `General Call` command.

When it is sent to the device, the REFRESH command is executed and the readable accumulator data, readable accumulator count, V_{BUS}, and V_{SENSE} measurements are all refreshed and the internal accumulators values or accumulator count are reset, exactly like the REFRESH command. The master can read the updated data 1 ms after the REFRESH_G command is sent, and anytime after than up until the next REFRESH, REFRESH_G, or REFRESH_V command is sent.

REGISTER 6-13: REFRESH_V COMMAND (ADDRESS 1FH)

SEND	SEND	SEND	SEND	SEND	SEND	SEND	SEND
No Data in this command, Send Byte only							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 This command is a SEND Byte, does not contain any data. When it is sent to the device, the REFRESH_V command is executed.

It is similar to the REFRESH command except the accumulators and accumulator count are not reset. The readable accumulator data, readable accumulator count, V_{BUS}, and V_{SENSE} measurements are all refreshed without affecting the internal accumulators values or accumulator count. The master can read the updated data 1 ms after the REFRESH_V command is sent, and anytime after than up until the next REFRESH, REFRESH_G, or REFRESH_V command is sent.

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REGISTER 6-14: SLOW (ADDRESS 20H)

R-0	R-0	R-0	RW-1	RW-0	RW-1	RW-0	RW-1
SLOW	SLOW-LH	SLOW_HL	R_RISE	R_V_RISE	R_FALL	R_V_FALL	POR
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

This register tracks the state of the SLOW pin, tracks transitions on the SLOW pin, and controls the type of limited REFRESH command (if any) that occurs on a SLOW pin transition. This allows software to monitor the state of the SLOW pin and its transitions over I^2C even though the SLOW pin is asynchronous to the I^2C pins and may have a different controller. All of the bits in this register are updated in real time, they do not require a REFRESH signal to be updated.

Note that if a REFRESH and REFRESH_V are both enabled for a certain SLOW pin transition, REFRESH will be executed (REFRESH wins over REFRESH_V).

On a transition of the SLOW pin, a limited REFRESH function is executed. These limited REFRESH and REFRESH_V functions update all of the readable results registers. For the limited REFRESH function only, it also reset the accumulators and accumulator count. These are called limited REFRESH and limited REFRESH_V functions because there is no activation of any pending changes to the Control registers.

If the SLOW pin is configured to act as an $\overline{\text{ALERT}}$ pin, all of these bits are always 0. The bits are not cleared when read, see the details on each bit for clearing information.

SLOW Control and Status Bits

bit 7 = 0 The SLOW pin is pulled low externally
bit 7 = 1 The SLOW pin is pulled high externally

bit 6 = 0 The SLOW pin has not transitioned low to high since the last REFRESH command
bit 6 = 1 The SLOW pin has transitioned low to high since the last REFRESH command
The bit is reset to 0 by a REFRESH or REFRESH_G command

bit 5 = 0 The SLOW pin has not transitioned high to low since the last REFRESH command
bit 5 = 1 The SLOW pin has transitioned high to low since the last REFRESH command
The bit is reset to 0 by a REFRESH or REFRESH_G command

bit 4 = 0 Disables a limited REFRESH function to take place on the rising edge of the SLOW pin
bit 4 = 1 Enables a limited REFRESH function to take place on the rising edge of the SLOW pin
The bit is not reset automatically, it must be written to be changed.

bit 3 = 0 Disables a limited REFRESH_V function to take place on the rising edge of the SLOW pin
bit 3 = 1 Enables a limited REFRESH_V function to take place on the rising edge of the SLOW pin
The bit is not reset automatically, it must be written to be changed

bit 2 = 0 Disables a limited REFRESH function to take place on the falling edge of the SLOW pin
bit 2 = 1 Enables a limited REFRESH function to take place on the falling edge of the SLOW pin
The bit is not reset automatically, it must be written to be changed

bit 1 = 0 Disables a limited REFRESH_V function to take place on the falling edge of the SLOW pin
bit 1 = 1 Enables a limited REFRESH_V function to take place on the falling edge of the SLOW pin
The bit is not reset automatically, it must be written to be changed

POR Status Bit

The POR bit is a POR flag, for the purpose of enabling the system designer can clear it after POR, and then monitor it to detect if the device was powered cycled or somehow reset since the POR. If the reset is detected in this manner, any non-default programming can be reprogrammed.

bit 0 = 0 This bit has been cleared over I^2C since the last POR occurred
bit 0 = 1 This bit has the POR default value of 1, and has not been cleared since the last reset occurred
This bit is only reset by POR

REGISTER 6-15: CTRL_ACT REGISTER (ADDRESS 21H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
Sample_Rate[1:0]		SLEEP	SING	ALERT_PIN	ALERT_CC	OVF ALERT	OVF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

This register contains an image of the Control register, 01h. The bits in this register reflect the current active value of these settings, whereas the values in register 01h may have been programmed but not activated by one of the REFRESH commands. This register allows the software to determine the actual active setting.

This register is valid when the Results registers are valid, 1 ms after a REFRESH/_V/_G command (in most cases). However, if the users program a conversion rate change followed by REFRESH, the new conversion rate will not become effective until the current conversion cycle is complete. For example, if the old sample rate was 8 Hz, it will take up to 125 mS before the conversion cycle (and the CTRL_ACT register) are updated. This delay can be variable, depending on where we are in the conversion cycle when the REFRESH command is sent.

bit 7-6 **Sample_Rate[1:0]**: shows the value that is currently active since the most recent REFRESH function was received for programmed sample rate in Normal mode (that is, if SLOW pin is not asserted)

00b = 1024 samples/s

01b = 256 samples/s

10b = 64 samples/s

11b = 8 samples/s

bit 5 **SLEEP**: shows the value that is currently active since the most recent REFRESH function was received for the SLEEP bit.

0 = ACTIVE mode

1 = SLEEP mode, no data conversion

bit 4 **SING**: shows the value that is currently active since the most recent REFRESH function was received for the single shot select bit, SING.

0 = Sequential scan mode

1 = Single-shot mode

bit 3 **ALERT_PIN**: shows the value that is currently active since the most recent REFRESH function was received for the ALERT_PIN bit.

0 = Disable the $\overline{\text{ALERT}}$ pin function

1 = Enable the $\overline{\text{ALERT}}$ pin function

bit 2 **ALERT_CC**: shows the value that is currently active since the most recent REFRESH function was received for the ALERT_CC bit.

0 = No ALERT on Conversion Cycle Complete

1 = ALERT function asserted for 5 µS on each completion of the conversion cycle

bit 1 **OVF ALERT**: shows the value that is currently active since the most recent REFRESH function was received for the OVF ALERT bit.

0 = No ALERT if accumulator or accumulator counter overflow has occurred

1 = $\overline{\text{ALERT}}$ pin triggered if accumulator or accumulator counter has overflowed

bit 0 **OVF**: shows the value that is currently active since the most recent REFRESH function was received for the OVF bit.

0 = No accumulator or accumulator counter overflow has occurred

1 = Accumulator or accumulator counter has overflowed

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REGISTER 6-16: CHANNEL DIS_ACT (ADDRESS 22H)

R-0	R-0	R-0	R-0	U	U	U	U
CH1_OFF	CH2_OFF	CH3_OFF	CH4_OFF	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

This register contains an image of the Channel Disable bits in register 1Ch.The bits in this register reflect the value that was activated by the most recent REFRESH function, and is currently active. Whereas the values in register 1Ch may have been programmed but not activated by one of the REFRESH commands, register 22h allows software to determine the actual active setting. This register is valid when the Results registers are valid, 1 ms after a REFRESH/_V/_G command.

bit 7-4 **CHn_OFF[7:4]**: shows the value that is currently active for these bits.

bit 7 0 = CH1 ON. Channel 1 active during conversion cycle
1 = CH1 OFF. Channel 1 inactive during conversion cycle

bit 6 0 = CH2 ON. Channel 2 active during conversion cycle
1 = CH2 OFF. Channel 2 inactive during conversion cycle

bit 5 0 = CH3 ON. Channel 3 active during conversion cycle
1 = CH3 OFF. Channel 3 inactive during conversion cycle

bit 4 0 = CH4 ON. Channel 4 active during conversion cycle
1 = CH4 OFF. Channel 4 inactive during conversion cycle

bit 3-0 Not used, always reads '0'

REGISTER 6-17: NEG_PWR_ACT (ADDRESS 23H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CH1_BIDI	CH2_BIDI	CH3_BIDI	CH4 BIDI	CH1_BIDV	CH2_BIDV	CH3_BIDV	CH4_BIDV
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

This register contains an image of the NEG_PWR register, 1Dh.The bits in this register reflect the current active value of these settings, whereas the values in register 1Dh may have been programmed but not activated by one of the REFRESH commands. This register allows software to determine the actual active setting. This register is valid when the Results registers are valid, 1 ms after a REFRESH/_V/_G command.

bit 7-4 **CH1_BIDI[7:4]**: these bits show the current active value of the corresponding bits in **Register 6-11**, NEG_PWR (Address 1Dh).

bit 3-0 **CH1_BIDV[3:0]**: these bits show the current active value of the corresponding bits in **Register 6-11**, NEG_PWR (Address 1Dh).

bit 7 0 = Channel 1 V_{SENSE} ADC converts 0 to +100 mV range with 16-bit straight binary output
1 = Channel 1 V_{SENSE} ADC converts -100 mV to +100 mV range with 16-bit two's complement output

bit 6 0 = Channel 2 V_{SENSE} ADC converts 0 to +100 mV range with 16-bit straight binary output
1 = Channel 2 V_{SENSE} ADC converts -100 mV to +100 mV range with 16-bit two's complement output

bit 5 0 = Channel 3 V_{SENSE} ADC converts 0 to +100 mV range with 16-bit straight binary output
1 = Channel 3 V_{SENSE} ADC converts -100 mV to +100 mV range with 16-bit two's complement output

bit 4 0 = Channel 4 V_{SENSE} ADC converts 0 to +100 mV range with 16-bit straight binary output
1 = Channel 4 V_{SENSE} ADC converts -100 mV to +100 mV range with 16-bit two's complement output

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REGISTER 6-17: NEG_PWR_ACT (ADDRESS 23H) (CONTINUED)

bit 3 0 = Channel 1 V_{BUS} ADC converts 0 to +32V range with 16-bit straight binary output
1 = Channel 1 V_{BUS} ADC converts -32V to +32V range with 16-bit two's complement output

bit 2 0 = Channel 2 V_{BUS} ADC converts 0 to +32V range with 16-bit straight binary output
1 = Channel 2 V_{BUS} ADC converts -32V to +32V range with 16-bit two's complement output

bit 1 0 = Channel 3 V_{BUS} ADC converts 0 to +32V range with 16-bit straight binary output
1 = Channel 3 V_{BUS} ADC converts -32V to +32V range with 16-bit two's complement output

bit 0 0 = Channel 4 V_{BUS} ADC converts 0 to +32V range with 16-bit straight binary output
1 = Channel 4 V_{BUS} ADC converts -32V to +32V range with 16-bit two's complement output

REGISTER 6-18: CTRL_LAT REGISTER (ADDRESS 24H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
Sample_Rate[1:0]		SLEEP	SING	ALERT_PIN	ALERT_CC	OVF ALERT	OVF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

This register contains an image of the **Register 6-15** CTRL_ACT Register (Address 21h). The bits in this register reflect the value of these settings that was active before the most recent REFRESH command (including REFRESH_V and/or REFRESH_G). The values in register 01h may have been programmed but not activated by one of the REFRESH commands, and the values in 21h are currently active. This register allows software to determine the actual active setting that was active prior to the most recent REFRESH command and therefore corresponds to the dataset that is held in the readable registers. This register is valid when the Results registers are valid, 1 ms after a REFRESH/_V/_G command.

bit 7-6 **Sample_Rate[1:0]**: shows the value of these settings that was latched prior to the most recent REFRESH command (including REFRESH_V and/or REFRESH_G)
00b = 1024 samples/s
01b = 256 samples/s
10b = 64 samples/s
11b = 8 samples/s

bit 5 **SLEEP**: shows the value of these settings that was latched prior to the most recent REFRESH command (including REFRESH_V and/or REFRESH_G).
0 = Active mode
1 = SLEEP mode, no data conversion

bit 4 **SING**: shows the value of these settings that was latched prior to the most recent REFRESH command (including REFRESH_V and/or REFRESH_G).
0 = Sequential scan mode
1 = Single-shot mode

bit 3 **ALERT_PIN**: the value of these settings that was latched prior to the most recent REFRESH command (including REFRESH_V and/or REFRESH_G).
0 = Disable the $\overline{\text{ALERT}}$ pin function
1 = Enable the $\overline{\text{ALERT}}$ pin function

bit 2 **ALERT_CC**: shows the value of these settings that was latched prior to the most recent REFRESH command (including REFRESH_V and/or REFRESH_G) for the ALERT_CC bit.
0 = No ALERT on Conversion Cycle Complete
1 = ALERT function asserted for 5 µS on each completion of the conversion cycle

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REGISTER 6-18: CTRL_LAT REGISTER (ADDRESS 24H) (CONTINUED)

bit 1 **OVF ALERT**: shows the value of these settings that was latched prior to the most recent REFRESH command (including REFRESH_V and/or REFRESH_G) for the OVF_ALERT bit.
0 = No ALERT if accumulator or accumulator counter overflow has occurred
1 = $\overline{\text{ALERT}}$ pin triggered if accumulator or accumulator counter has overflowed

bit 0 **OVF**: shows the value of these settings that was latched prior to the most recent REFRESH command (including REFRESH_V and/or REFRESH_G) for the OVF bit.
0 = No accumulator or accumulator counter overflow has occurred
1 = Accumulator or accumulator counter has overflowed

REGISTER 6-19: CHANNEL DIS_LAT (ADDRESS 25H)

R-0	R-0	R-0	R-0	U	U	U	U
CH1_OFF	CH2_OFF	CH3_OFF	CH4_OFF	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

This register contains an image of the **Register 6-16** Channel DIS_ACT (Address 22h).The bits in this register reflect the value of these settings that was active before the most recent REFRESH command (including REFRESH_V and/or REFRESH_G). The values in register 1Ch may have been programmed but not activated by one of the REFRESH commands, and the values in 22h are currently active. This register allows software to determine the actual active setting that was active prior to the most recent REFRESH command and therefore corresponds to the dataset that is held in the readable registers. This register is valid when the Results registers are valid, 1 ms after a REFRESH/_V/_G command.

bit 7-4 **CHn_OFF[7:4]**: the value of these settings that was latched prior to the most recent REFRESH command (including REFRESH_V and/or REFRESH_G).

bit 7
0 = CH1 ON. Channel 1 active during conversion cycle
1 = CH1 OFF. Channel 1 inactive during conversion cycle

bit 6
0 = CH2 ON. Channel 2 active during conversion cycle
1 = CH2 OFF. Channel 2 inactive during conversion cycle

bit 5
0 = CH3 ON. Channel 3 active during conversion cycle
1 = CH3 OFF. Channel 3 inactive during conversion cycle

bit 4
0 = CH4 ON. Channel 4 active during conversion cycle
1 = CH4 OFF. Channel 4 inactive during conversion cycle

bit 3-0 Not used, always read '0'

REGISTER 6-20: NEG_PWR _LAT (ADDRESS 26H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CH1_BIDI	CH2_BIDI	CH3_BIDI	CH4 BIDI	CH1_BIDV	CH2_BIDV	CH3_BIDV	CH4_BIDV
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

This register contains an image of the **Register 6-17** NEG_PWR_ACT (Address 23h).The bits in this register reflect the value of these settings that was active before the most recent REFRESH command (including REFRESH_V and/or REFRESH_G). The values in register 1Dh may have been programmed but not activated by one of the REFRESH commands, and the values in 23h are currently active. This register allows software to determine the actual active setting that was active prior to the most recent REFRESH command and therefore corresponds to the dataset that is held in the readable registers. This register is valid when the Results registers are valid, 1 ms after a REFRESH/_V/_G command.

bit 7-4 **CHn_BIDI[7:4]**: the value of these settings that was latched prior to the most recent REFRESH command (including REFRESH_V and/or REFRESH_G).

bit 3-0 **CHn_BIDV[3:0]**: the value of these settings that was latched prior to the most recent REFRESH command (including REFRESH_V and/or REFRESH_G).

bit 7 0 = Channel 1 V_{SENSE} ADC converts 0 to +100mV range with 16-bit straight binary output
1 = Channel 1 V_{SENSE} ADC converts -100mV to +100mV range with 16 bit two's complement output

bit 6 0 = Channel 2 V_{SENSE} ADC converts 0 to +100mV range with 16-bit straight binary output
1 = Channel 2 V_{SENSE} ADC converts -100mV to +100mV range with 16-bit two's complement output

bit 5 0 = Channel 3 V_{SENSE} ADC converts 0 to +100mV range with 16-bit straight binary output
1 = Channel 3 V_{SENSE} ADC converts -100mV to +100mV range with 16-bit two's complement output

bit 4 0 = Channel 4 V_{SENSE} ADC converts 0 to +100mV range with 16-bit straight binary output
1 = Channel 4 V_{SENSE} ADC converts -100mV to +100mV range with 16-bit two's complement output

bit 3 0 = Channel 1 V_{BUS} ADC converts 0 to +32V range with 16-bit straight binary output
1 = Channel 1 V_{BUS} ADC converts -32V to +32V range with 16-bit two's complement output

bit 2 0 = Channel 2 V_{BUS} ADC converts 0 to +32V range with 16-bit straight binary output
1 = Channel 2 V_{BUS} ADC converts -32V to +32V range with 16-bit two's complement output

bit 1 0 = Channel 3 V_{BUS} ADC converts 0 to +32V range with 16-bit straight binary output
1 = Channel 3 V_{BUS} ADC converts -32V to +32V range with 16-bit two's complement output

bit 0 0 = Channel 4 V_{BUS} ADC converts 0 to +32V range with 16-bit straight binary output
1 = Channel 4 V_{BUS} ADC converts -32V to +32V range with 16-bit two's complement output

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REGISTER 6-21: PRODUCT ID REGISTER (ADDRESS FDh)

R-0	R-1	R-0	R-1	R-1	R-0	R-1	R-1
PID[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PID[7:0]**: contain the Product ID for the PAC1931/2/3/4.

`0101_1000` for PAC1931
`0101_1001` for PAC1932
`0101_1010` for PAC1933
`0101_1011` for PAC1934 (Default shown in table directly above)

REGISTER 6-22: MANUFACTURER ID REGISTER (ADDRESS FEh)

R-0	R-1	R-0	R-1	R-1	R-1	R-0	R-1
MID[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **MID[7:0]**: the Manufacturer ID register identifies Microchip as the manufacturer of the PAC1931/2/3/4
This value is 5Dh.

REGISTER 6-23: REVISION ID REGISTER (ADDRESS FFh)

R-0	R-0	R-0	R-0	R-0	R-0	R-1	R-1
RID[7:0]							
bit 7							bit 0

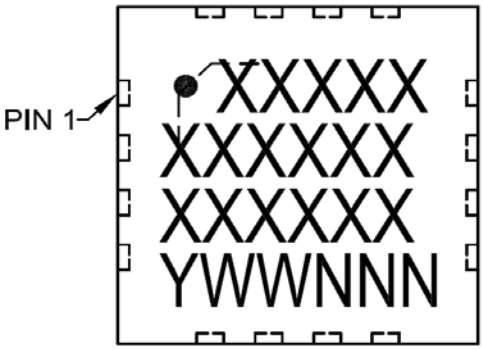
Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **RID[7:0]**: the Revision register identifies the die revision
This register reads 03h.

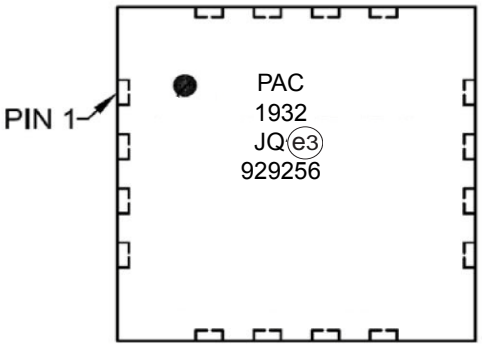
7.0 PACKAGE DESCRIPTION

7.1 Package Marking Information

UQFN
PAC1932/3/4



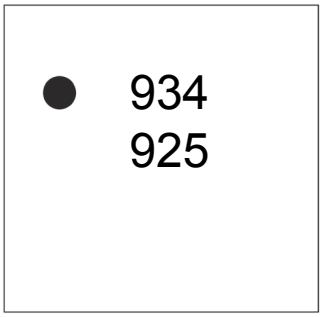
Example



WLCSP-16
PAC1931/2/3/4



Example



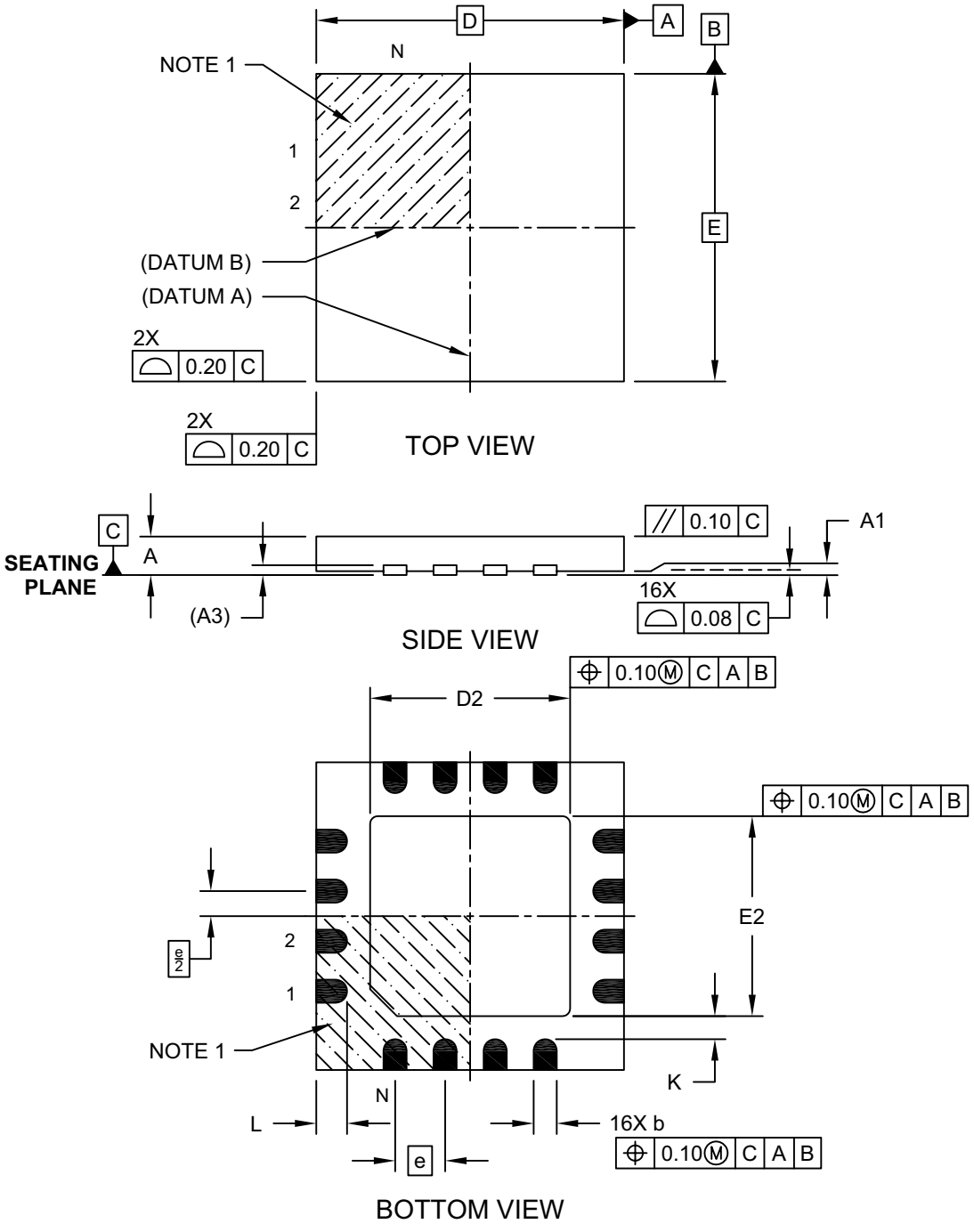
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (JQ) - 4x4x0.5 mm Body [UQFN]

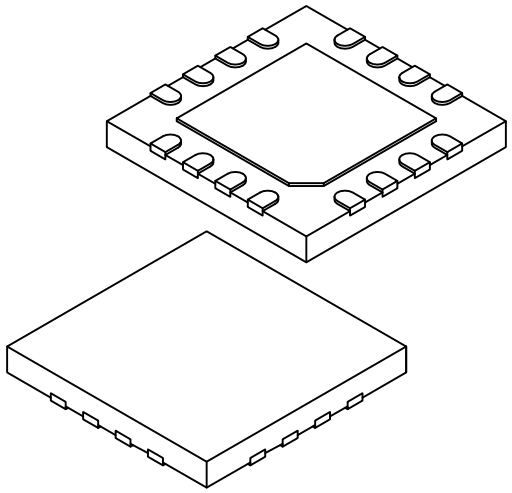
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-257A Sheet 1 of 2

16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (JQ) - 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.127 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.60	2.70
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.60	2.70
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

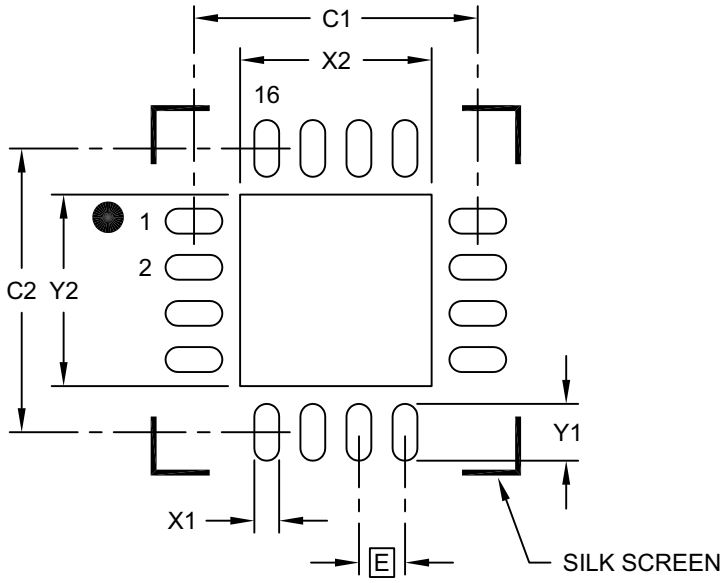
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-257A Sheet 2 of 2

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16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (JQ) - 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			2.70
Optional Center Pad Length	Y2			2.70
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X16)	X1			0.35
Contact Pad Length (X16)	Y1			0.80

Notes:

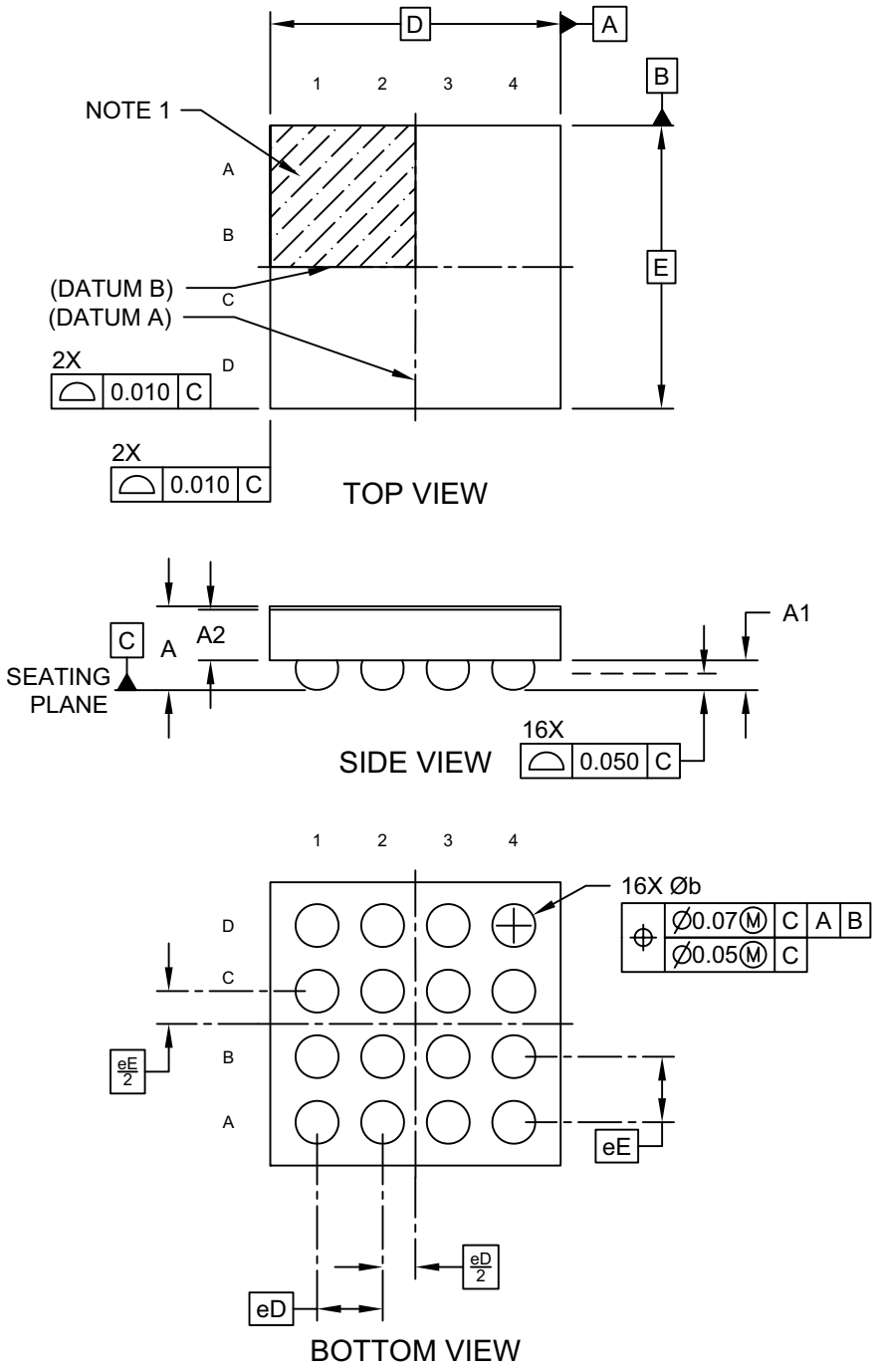
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2257A

16-Ball Wafer Level Chip Scale Package (CS) - 2.225x2.17 mm Body [WLCSP] PAC1934

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

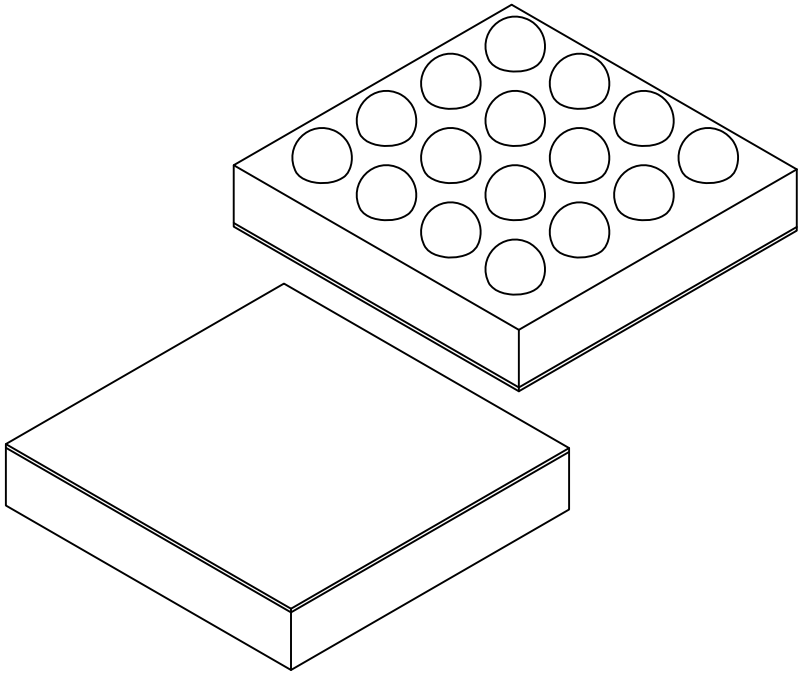


Microchip Technology Drawing C04-6036-01 Rev. B Sheet 1 of 2

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16-Ball Wafer Level Chip Scale Package (CS) - 2.225x2.17 mm Body [WLCSP] PAC1934

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Bump Pitch	eD		0.50 BSC	
Bump Pitch	eE		0.50 BSC	
Length	D		2.225 BSC	
Width	E		2.170 BSC	
Overall Height	A	0.601	0.641	0.679
Bump Height	A1	0.197	-	0.257
Die Thickness	A2	0.363	0.388	0.413
Bump Diameter	b	0.297	0.327	0.357

Notes:

1. Topside A1 indicator is an engraved figure.
2. Under-fill is recommended for best solder joint reliability.
3. Solder diameter at interface to package body is 300µm (nominal).
4. Dimensioning and tolerancing per ASME Y14.5M

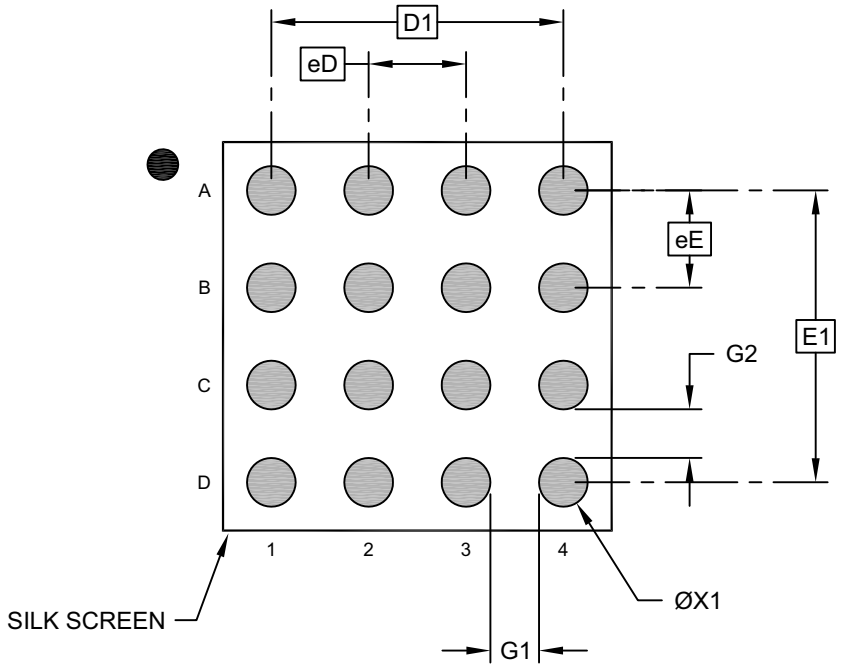
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-6036-01 Rev. B Sheet 2 of 2

16-Ball Wafer Level Chip Scale Package (CS) - 2.225x2.17 mm Body [WLCSP] PAC1934

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	eD		0.50 BSC	
Contact Pitch	eE		0.50 BSC	
Overall Pitch	D1		1.50 BSC	
Overall Pitch	E1		1.50 BSC	
Space Between Contacts	G1		0.25	
Space Between Contacts	G2		0.25	
Contact Diameter	ØX1		0.25	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-8036 Rev. B

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APPENDIX A: REVISION HISTORY

Revision E (August 2019)

The following is the list of modifications:

1. Added the PAC1931 Single-Channel DC Power/Energy Monitor with Accumulator and related information throughout the Data Sheet.

Revision D (May 2019)

The following is the list of modifications:

1. Added the WLCSP package.
2. Updated **Table 1-1**.
3. Replaced **Figure 2-22**.
4. Updated **Register 6-10**, **Register 6-14**, **Register 6-16**, and **Register 6-19**.

Revision C (June 2018)

The following is the list of modifications:

1. Added the entire PAC1932/3/4 device family.
2. Added UQFN package.
3. Updated **Table 1-1**.
4. Updated **Section 2.0 "Typical Operating Curves"**.
5. Updated **Section 3.0 "Pin Descriptions"**.
6. Updated **Register 6-10**.
7. Updated **Register 6-15**.
8. Updated **Register 6-21**.
9. Updated **Section 7.0 "Package Description"**.
10. Updated **Product Identification System**.
11. Fixed minor typographical errors.

Revision B (November 2017)

The following is the list of modifications:

1. Updated **Section 4.5 "Voltage Measurement"**, **Section 4.6 "Current Measurement"**, **Section 4.7 "Selecting R_{SENSE} Values"** and **Section 4.9 "Power and Energy"**.
2. Updated **Register 6-10**.
3. Fixed minor typographical errors.

Revision A (September 2017)

- Initial Release for Advance Data Sheet.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	-X	/XXX
Device	Tape and Reel	Temperature Range	Package

Device:	PAC1931/2/3/4: Single/Multi-Channel DC Power/Energy Monitor with Accumulator	
Tape and Reel:	T	= Tape and Reel
Temperature Range:	I	= -40°C to +85°C (Industrial)
Package:	JQ	= 16-Lead Ultra Thin Plastic Quad Flat, No Lead Package, 4 mm × 4 mm × 0.5 mm Body (UQFN)
	J6CX	= 16-Ball Wafer Level Chip Scale Package, 2.225 mm × 2.17 mm (WLCSP)

Example:

a) PAC1932T-I/JQ: 16-Lead 4 mm × 4 mm UQFN, shipped in a 3,300 piece Tape and Reel

b) PAC1933T-I/JQ: 16-Lead 4 mm × 4 mm UQFN, shipped in a 3,300 piece Tape and Reel

c) PAC1934T-I/JQ: 16-Lead 4 mm × 4 mm UQFN, shipped in a 3,300 piece Tape and Reel

a) PAC1934T-I/J6CX: 16-lead 2.225 mm x 2.17 mm WLCSP, shipped in a 5,000 piece Tape and Reel

b) PAC1933T-I/J6CX: 16-lead 2.225 mm x 2.17 mm WLCSP, shipped in a 5,000 piece Tape and Reel

c) PAC1932T-I/J6CX: 16-lead 2.225 mm x 2.17 mm WLCSP, shipped in a 5,000 piece Tape and Reel

d) PAC1931T-I/J6CX: 16-lead 2.225 mm x 2.17 mm WLCSP, shipped in a 5,000 piece Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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