DS150DF1610 12.5 to 15 Gbps 16-Channel Retimer

1 Features

- Pin-Compatible Family
  - DS150DF1610: 12.5 to 15G
  - DS125DF1610: 9.8 to 12.5G
  - DS110DF1610: 8.5 to 11.3G
- Fully Adaptive CTLE
- Self tuning DFE, with Optional Continuous Adaption
- Configurable VGA
- Adjustable Transmit V_{OD}
- Adjustable 3-tap Transmit FIR Filter
- On-chip AC Coupling on Receive Inputs
- Locks to Half/Quarter/Eighth Data Rates for Legacy Support
- On-chip Eye Monitor(EOM), PRBS Checker, Pattern Generator
- Supports JTAG Boundary Scan
- Programmable Output Polarity Inversion
- Input Signal Detection, CDR Lock Detection
- Single 2.5 V ±5% Power Supply
- SMBus Based Register Configuration
- Optional EEPROM Configuration
- 15 mm x 15 mm, 196-pin FCBGA Package
- Operating Temp Range : –10°C to +85°C

2 Applications

- Backplane/Midplane reach extension

3 Description

The DS150DF1610 is a sixteen-channel multi-rate retimer with integrated signal conditioning features. The device includes a fully adaptive Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), clock and data recovery (CDR), and a transmit FIR filter to enhance the reach and robustness over long, lossy, crosstalk impaired high speed serial links to achieve BER < 1×10^{-15}.

Each channel of the DS150DF1610 independently locks to serial data rates between 12.5 and 15 Gbps plus the divide by 2, 4 and 8 sub-multiples. A simple external oscillator (±100ppm) that is synchronous or asynchronous with the incoming data stream is used as a calibration clock.

A programmable transmit Finite Impulse Response (FIR) filter offers control of the pre-cursor, main tap and post-cursor for transmit equalization. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnects and backplanes with multiple connectors.

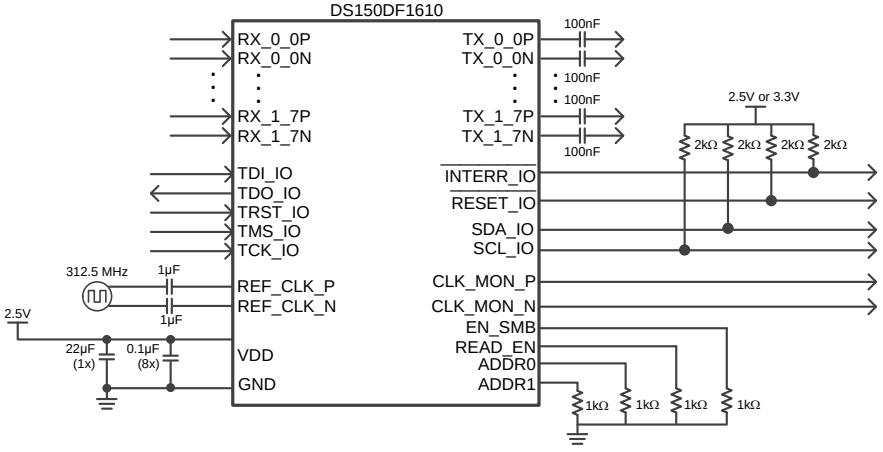
A non-disruptive mission mode eye-monitor feature allows link monitoring internal to the receiver. The built-in PRBS generator and checker compliment the internal diagnostic features to complete standalone BERT measurements. Built-in JTAG enables manufacturing tests.

To download the full datasheet, please send a request to: highspeed_datasheets@list.ti.com

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE NOM
DS150DF1610	FCBGA (196)	15.00 mm x 15.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet



PRODUCT PREVIEW

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCT PREVIEW Information. Product in design phase of development. Subject to change or discontinuance without notice.

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	COMMENTS
November 2014	*	Initial Release

5 Device and Documentation Support

5.1 Trademarks

All trademarks are the property of their respective owners.

5.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designed devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS150DF1610FB/NOPB	PREVIEW	FCBGA	ABB	196		Green (RoHS & no Sb/Br)	SNAGCU	Level-4-245C-72 HR	-10 to 85	DS150 DF1610	
DS150DF1610FBE/NOPB	PREVIEW	FCBGA	ABB	196		Green (RoHS & no Sb/Br)	SNAGCU	Level-4-245C-72 HR	-10 to 85	DS150 DF1610	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

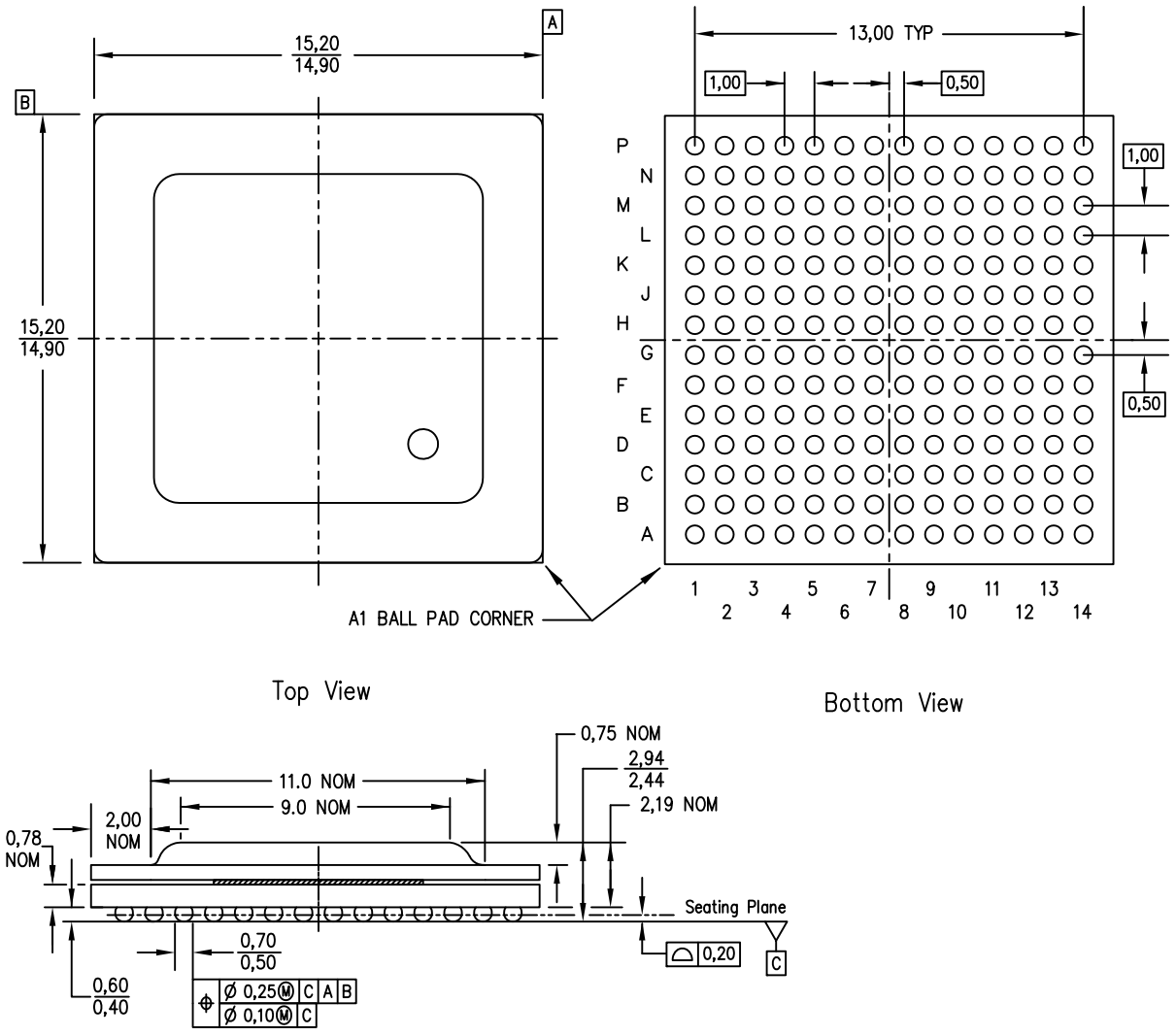
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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ABB (S–FCBGA–N196) PLASTIC BALL GRID ARRAY



PACKAGE IDENTIFIER: ABB–01 4218196–2/B 01/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free die bump and solder ball.

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