

RMPA2450

2.4–2.5 GHz GaAs MMIC Power Amplifier

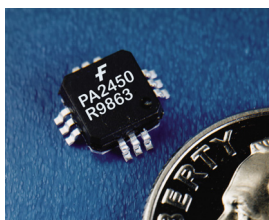
General Description

The Fairchild RMPA2450 is a fully monolithic power amplifier in a surface mount package for use in wireless applications in the 2.4 to 2.5GHz ISM frequency band. The amplifier may be biased for linear, class AB or class F for high efficiency applications. On-chip matching components allow operation in a 50Ω system with no external matching components. The MMIC chip design utilizes our 0.25μm power PHEMT process.

Features

- 35% Power Added Efficiency
- 31dBm Output Power (P1dB) at $V_d = +7V$
- 28dBm Output Power (P1dB) at $V_d = +5V$
- No external RF matching components
- Small Package Outline: 0.28" x 0.28" x 0.07"
- Thermal Resistance (Channel to Case): 33°C/W

Device



Absolute Ratings

Symbol	Parameter	Rating	Units
V _{d1} , V _{d2}	Positive Drain DC Voltage	+8	V
V _{g1} , V _{g2}	Negative Gate DC Voltage	-5	V
V _d -V _g	Simultaneous Drain to Gate Voltage	+10	V
P _{IN}	RF Input Power (from 50Ω source)	+10	dBm
I _{ds}	Drain to Source Current	575	mA
I _g	Gate Current	5	mA
T _{ch}	Channel Temperature	150	°C
T _{CASE}	Operating Case Temperature	-40 to 100	°C
T _{STG}	Storage Temperature Range	-40 to 125	°C

Electrical Characteristics (Note 4, At 25°C, Z_O = 50Ω, Unless Otherwise Noted)

Parameter	Min	Typ	Max	Units
Frequency Range	2400	2450	2500	MHz
Gain ^{1, 2, 4}		30		dB
Output Power, P1dB ^{1,4}		28		dBm
Assoc. Power Added Efficiency		35		%
Output Power, P1dB ³		31		dBm
Assoc. Power Added Efficiency		33		%
Drain Current (I _{dd1} + I _{dd2})			550	mA
Gate Current (I _{gg1} + I _{gg2})			5	mA
Input Return Loss (50Ω)	7.5			dB

Notes:
1: I_{dq} = 360mA, V_{d1} = V_{d2} = 5.0V
2: Pin = -3dBm,
3: V_{d1} = V_{d2} = +7V
4: Production Testing includes Gain, Output Power (P1dB) and Input Return Loss at V_{d1} = V_{d2} = 5.0V, V_{g1} = V_{g2} = -0.5V (nominal) , adjusted for I_{dq} = 360mA, Pin = -3 dBm and at F = 2.45 GHz. Other Parameters are guaranteed by Design Validation Testing.

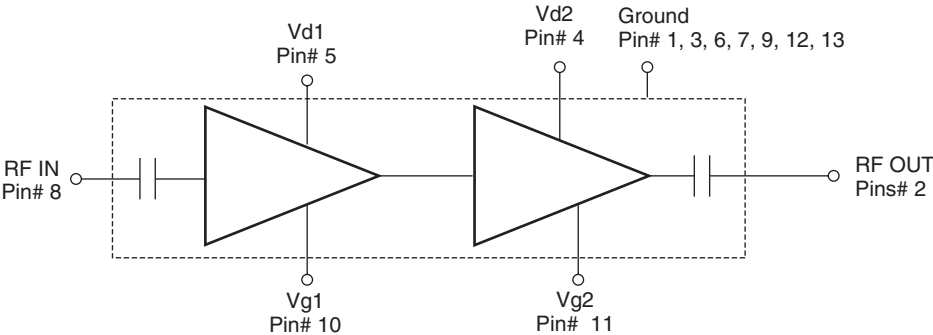


Figure 1. Functional Block Diagram (RMPA2450)

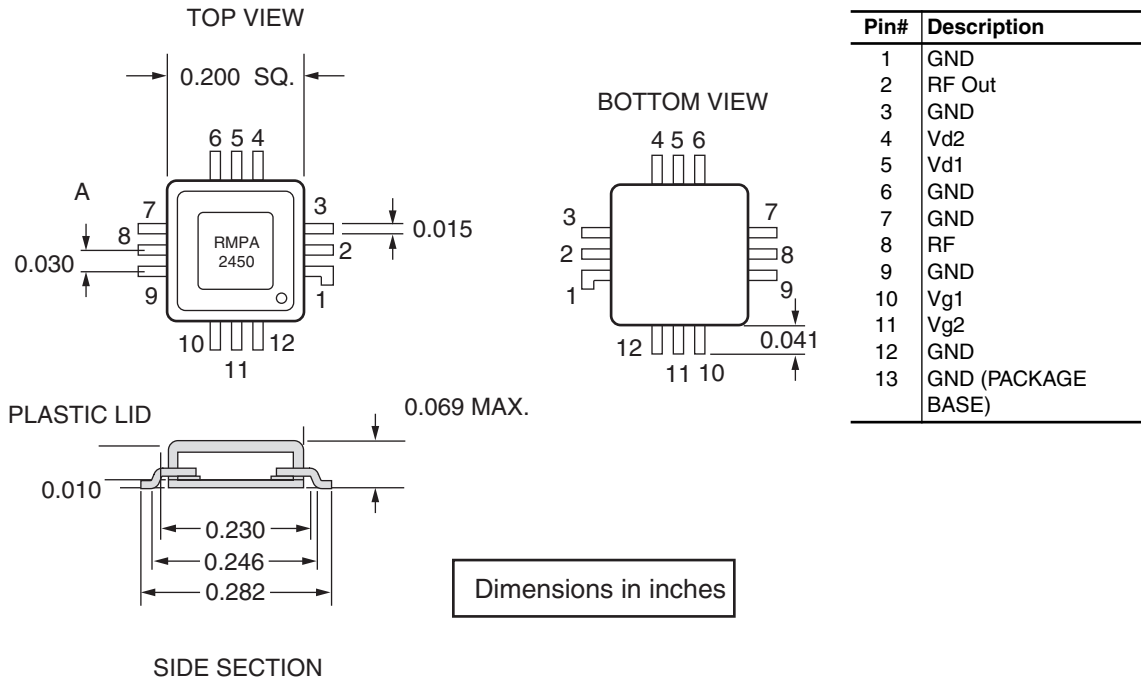


Figure 2. Outline Dimensions (RMPA2450)

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

The following briefly describes a procedure for evaluating the high efficiency PHEMT amplifier packaged in a surface mount package. It may be noted that the chip is a fully monolithic amplifier for ISM band applications. Figure 1 shows the functional block diagram of the packaged product.

Test Fixture

Figure 2 shows the outline and pin-out descriptions for the packaged device. A typical test fixture schematic showing external bias components is shown in Figure 3. Figure 4 shows typical layout of an evaluation board corresponding to the schematic diagram. The following should be noted:

- (1) Package pin designations are as shown in Figure 2.
- (2) V_{g1} , V_{g2} are the Gate Voltages (negative) applied at the pins of the package
- (3) $V_{gg1} = V_{gg2} = V_{gg}$ is the negative supply voltage at the evaluation board terminal
- (4) V_{d1} , V_{d2} are the Drain Voltages (positive) applied at the pins of the package
- (5) $V_{dd1} = V_{dd2} = V_{dd}$ is the positive supply voltage at the evaluation board terminal

Test Procedure for the Evaluation Board (RMPA2450-TB)

The following sequence of procedure must be followed to properly test the power amplifier:

CAUTION: LOSS OF GATE VOLTAGES (V_{g1} , V_{g2}) WHILE DRAIN VOLTAGES (V_{d1} , V_{d2}) ARE PRESENT MAY DAMAGE THE AMPLIFIER.

- Step 1: Turn off RF input power.
- Step 2: Use GND terminal of the evaluation board for DC supplies.
Apply gate supply voltages of typical -0.5V to evaluation board terminals V_{gg} .
- Step 3: Apply drain supply voltages of +5.0V to evaluation board terminals V_{dd} .
Adjust gate supply voltage, if needed, to set the desired quiescent bias currents I_{dq} (or to the values as shown on the data summary accompanying the product samples).
- Step 4: After the bias condition is established, RF input signal may now be applied.
- Step 5: Follow turn-off sequence of:
(i) Turn off RF Input Power (ii) Turn down and off V_{dd} (iii) Turn down and off V_{gg}

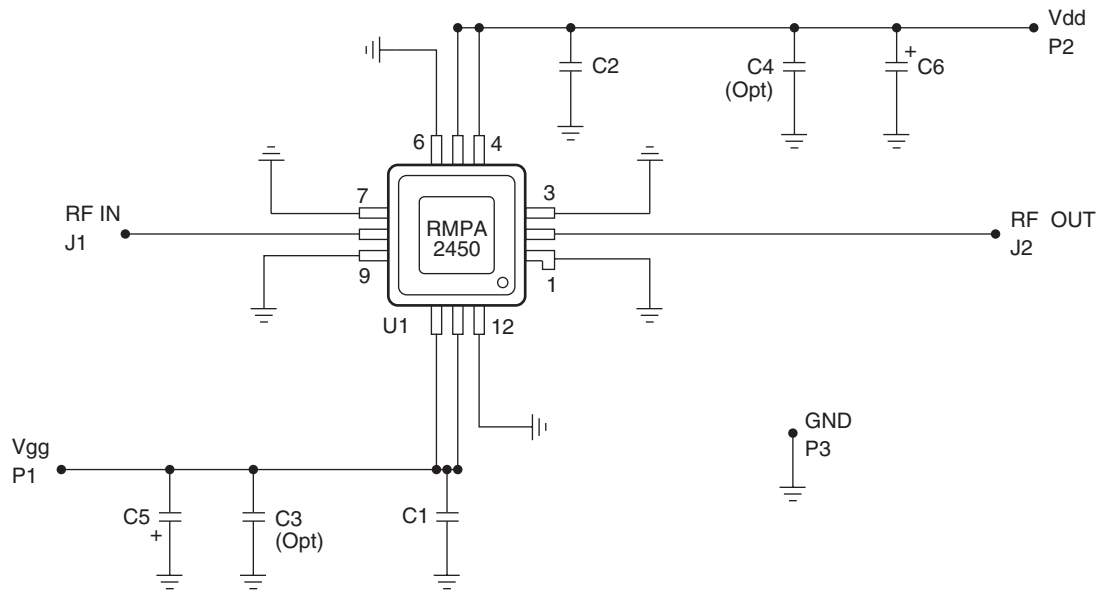


Figure 3. Schematic for a Typical Test Evaluation Board (RMPA2450-TB)

Parts List for Test Evaluation Board (RMPA2450-TB), G654220

Part	Rating	Size (L" X W")	Vendors
C1, C2	330pF	.04" X .02"	AVX, Murata, Novacap
C3, C4	1000pF	.04" X .02"	AVX, Murata, Novacap
C5, C6	4.75μF	.14" X .11"	Sprague, ATC, AVX, Murata
U1	RMPA2550	.28" X .28" X .07	
P1, P2, P3	Terminals		Sametec
J1, J2	SMA Connectors		E.F. Johnson
Board	FR4		

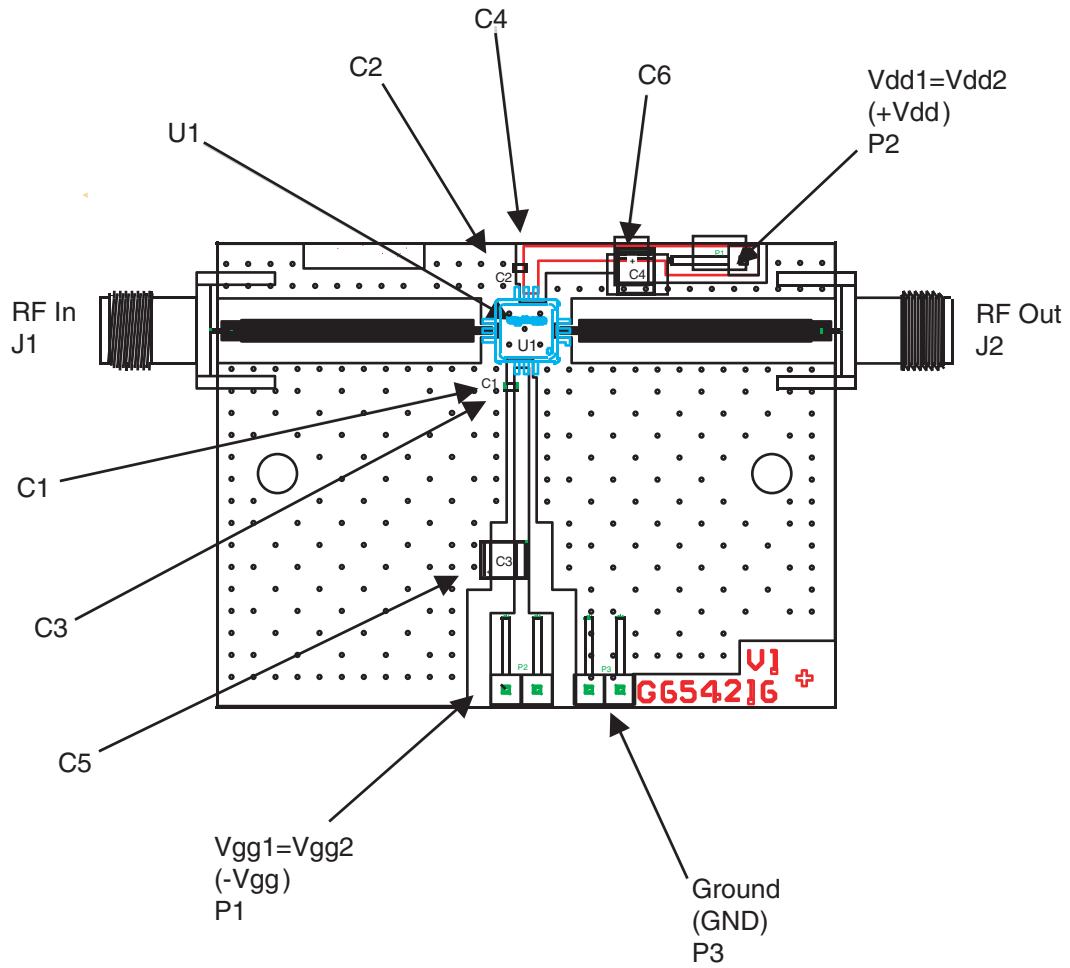


Figure 4. Layout and Assembly of Test Evaluation Board (RMPA2450-TB)

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