GENERAL DESCRIPTION

The XRT86VL3x is a 1.544 Mbit/s or 2.048 Mbit/s DS1/E1/J1 framer and LIU integrated solution featuring R^3 technology (Relayless, Reconfigurable, Redundancy) that comes in a 2-channel, 4-channel, or 8-channel package. The physical interface is optimized with internal impedance, and with the patented pad structure, the XRT86VL3x provides protection from power failures and hot swapping.

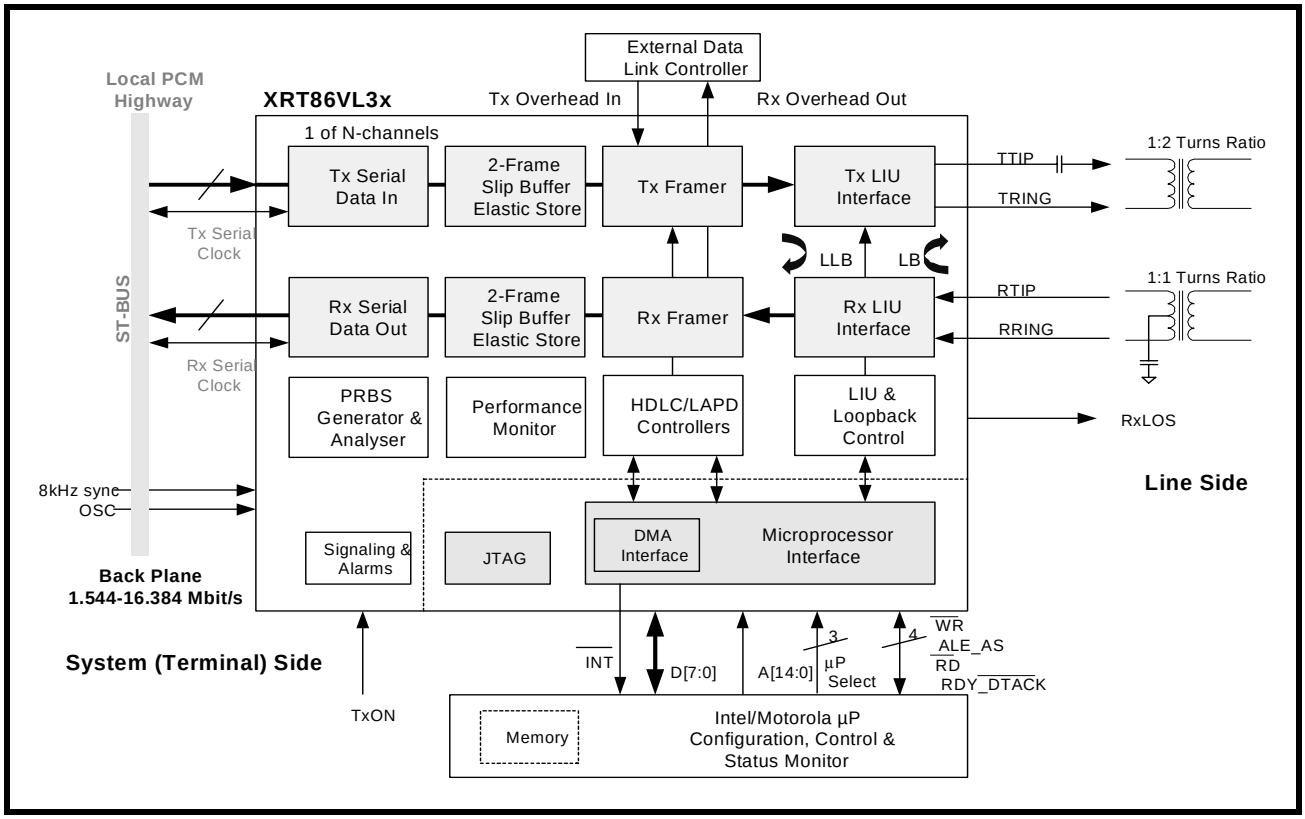
The XRT86VL3x contains an integrated DS1/E1/J1 framer and LIU which provide DS1/E1/J1 framing and error accumulation in accordance with ANSI/ITU_T specifications. Each framer has its own framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats.

Each Framer block contains its own Transmit and Receive T1/E1/J1 Framing function. There are 3 Transmit HDLC controllers per channel which encapsulate contents of the Transmit HDLC buffers into LAPD Message frames. There are 3 Receive HDLC controllers per channel which extract the payload content of Receive LAPD Message frames from the incoming T1/E1/J1 data stream and write the contents into the Receive HDLC buffers. Each framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound T1/E1/J1 frames. Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound T1/E1/J1 frames.

The XRT86VL3x fully meets all of the latest T1/E1/J1 specifications: ANSI T1/E1.107-1988, ANSI T1/E1.403-1995, ANSI T1/E1.231-1993, ANSI T1/E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

Applications and Features (next page)

FIGURE 1. XRT86VL3X N-CHANNEL DS1 (T1/E1/J1) FRAMER/LIU COMBO



APPLICATIONS

- High-Density T1/E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1/E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1/E1/J1 and Fractional T1/E1/J1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- T1/E1/J1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

- Independent, full duplex DS1 Tx and Rx Framer/ LIUs
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data at 1.544, 2.048, 4.096 and 8.192 Mbits. Also supports 4-channel multiplexed 12.352/16.384 (HMVIP/H.100) Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1/E1/ J1
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Extracts and inserts robbed bit signaling (RBS)
- 3 Integrated HDLC controllers per channel for transmit and receive, each controller having two 96-byte buffers (buffer 0 / buffer 1)
- HDLC Controllers Support SS7
- Timeslot assignable HDLC
- V5.1 or V5.2 Interface
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Alarm Indication Signal with Customer Installation signature (AIS-CI)
- Remote Alarm Indication with Customer Installation (RAI-CI)
- Gapped Clock interface mode for Transmit and Receive.
- Intel/Motorola and Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Wide choice of T1 framing structures: SF/D4, ESF, SLC®96, T1DM and N-Frame (non-signaling)
- Direct access to D and E channels for fast transmission of data link information
- PRBS, QRSS, and Network Loop Code generation and detection
- Programmable Interrupt output pin
- Supports programmed I/O and DMA modes of Read-Write access
- Each framer block encodes and decodes the T1/ E1/J1 Frame serial data
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 1.8V Inner Core Voltage
- 3.3V I/O operation with 5V tolerant inputs

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VL38IB	420 Tape Ball Grid Array	-40°C to +85°C
XRT86VL38IB484	484 Shrink Thin Ball Grid Array	-40°C to +85°C
XRT86VL34IB	225 Plastic Ball Grid Array	-40°C to +85°C
XRT86VL32IB	225 Plastic Ball Grid Array	-40°C to +85°C

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Table 28:: Power PC 403 Microprocessor Interface Timing Specifications 141

1.0 GENERAL DESCRIPTION AND INTERFACE

The XRT86VL3x supports multiple interfaces for various modes of operation. The purpose of this section is to present a general overview of the common interfaces and their connection diagrams. Each mode will be described in full detail in later sections of the datasheet.

NOTE: *For a brief tutorial on Framing Formats, see Appendix A in the back of this document.*

1.1 Physical Interface

The Line Interface Unit generates/receives standard return-to-zero (RZ) signals to the line interface for T1/E1/J1 twisted pair or E1 coaxial cable. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The transmitter outputs only require one DC blocking capacitor of 0.68µF and a 1:2 step-up transformer. The receive path inputs only require one bypass capacitor of 0.1µF connected to the center tap (CT) of the transformer and a 1:1 transformer. The receive CT bypass capacitor is required for Long Haul Applications, and recommended for Short Haul Applications. **Figure 2** shows the typical connection diagram for the LIU transmitters. **Figure 3** shows a typical connection diagram for the LIU receivers.

FIGURE 2. LIU TRANSMIT CONNECTION DIAGRAM USING INTERNAL TERMINATION

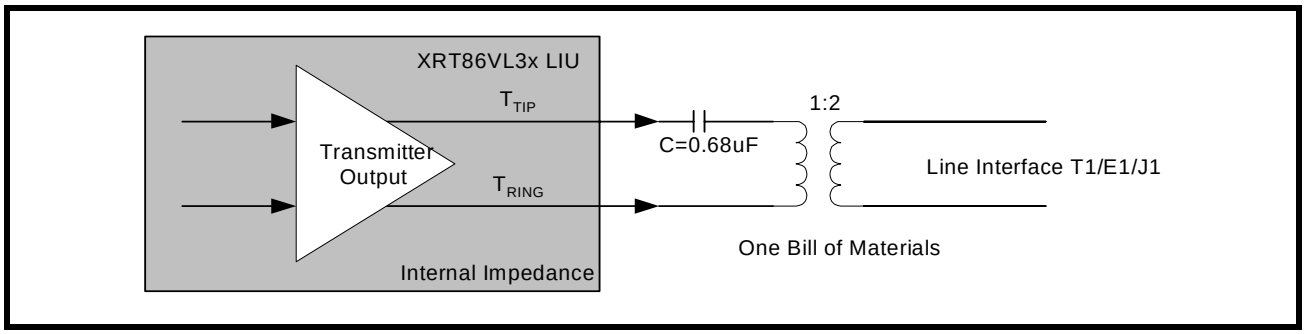
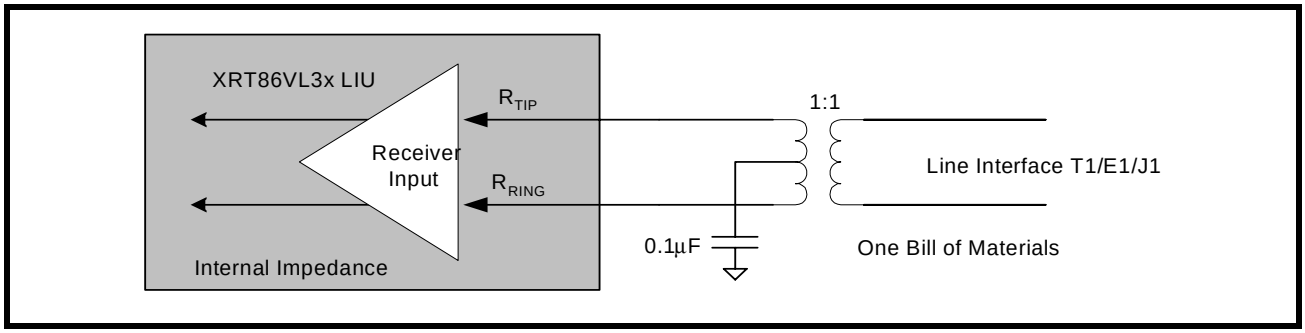


FIGURE 3. LIU RECEIVE CONNECTION DIAGRAM USING INTERNAL TERMINATION



1.2 R^3 Technology (Relayless / Reconfigurable / Redundancy)

Redundancy is used to introduce reliability and protection into network card design. The redundant card in many cases is an exact replicate of the primary card, such that when a failure occurs the network processor can automatically switch to the backup card. EXAR's R^3 technology has re-defined DS-1/E1/J1 physical interface design for 1:1 and 1+1 redundancy applications. Without relays and one Bill of Materials, EXAR offers multi-port, integrated Framer/LIU solutions to assist high density aggregate applications and framing requirements with reliability. The following section can be used as a reference for implementing R^3 Technology with EXAR's world leading Framer/LIU combo.

1.2.1 Line Card Redundancy

Telecommunication system design requires signal integrity and reliability. When a T1/E1 primary line card has a failure, it must be swapped with a backup line card while maintaining connectivity to a backplane without losing data. System designers can achieve this by implementing common redundancy schemes with the XRT86VL3x Framer/LIU. EXAR offers features that are tailored to redundancy applications while reducing the number of components and providing system designers with solid reference designs.

1.2.2 Typical Redundancy Schemes

- 1:1 One backup card for every primary card (Facility Protection)
- 1+1 One backup card for every primary card (Line Protection)
- ·N+1 One backup card for N primary cards

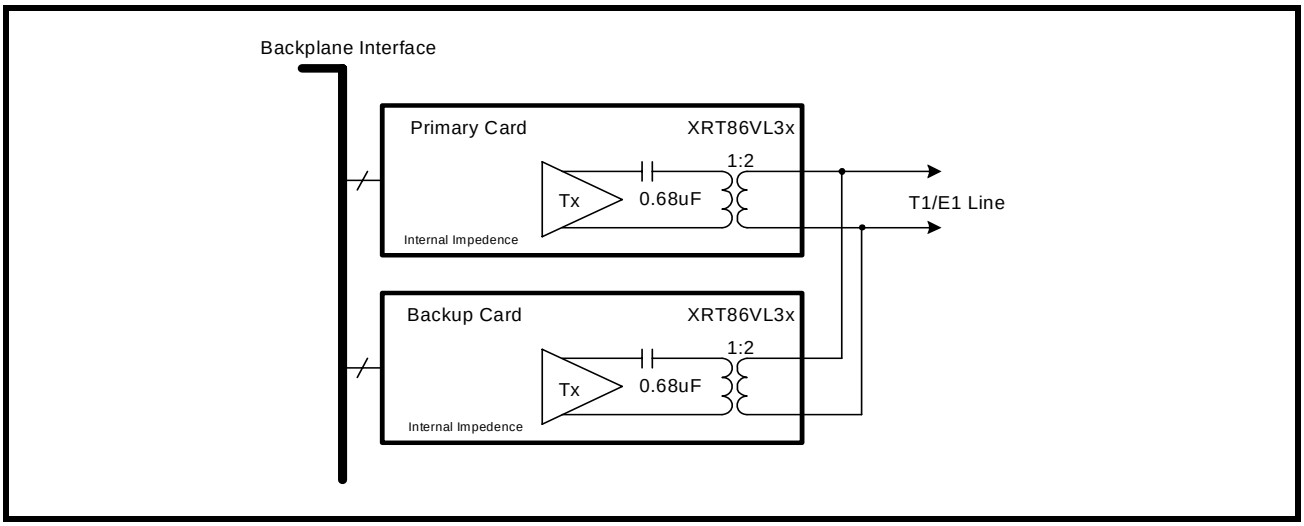
1.2.3 1:1 and 1+1 Redundancy Without Relays

The 1:1 facility protection and 1+1 line protection have one backup card for every primary card. When using 1:1 or 1+1 redundancy, the backup card has its transmitters tri-stated and its receivers in high impedance. This eliminates the need for external relays and provides one bill of materials for all interface modes of operation. For 1+1 line protection, the receiver inputs on the backup card have the ability to monitor the line for bit errors while in high impedance. The transmit and receive sections of the physical interface are described separately.

1.2.4 Transmit Interface with 1:1 and 1+1 Redundancy

The transmitters on the backup card should be tri-stated. Select the appropriate impedance for the desired mode of operation, T1/E1/J1. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See **Figure 4**. for a simplified block diagram of the transmit section for a 1:1 and 1+1 redundancy.

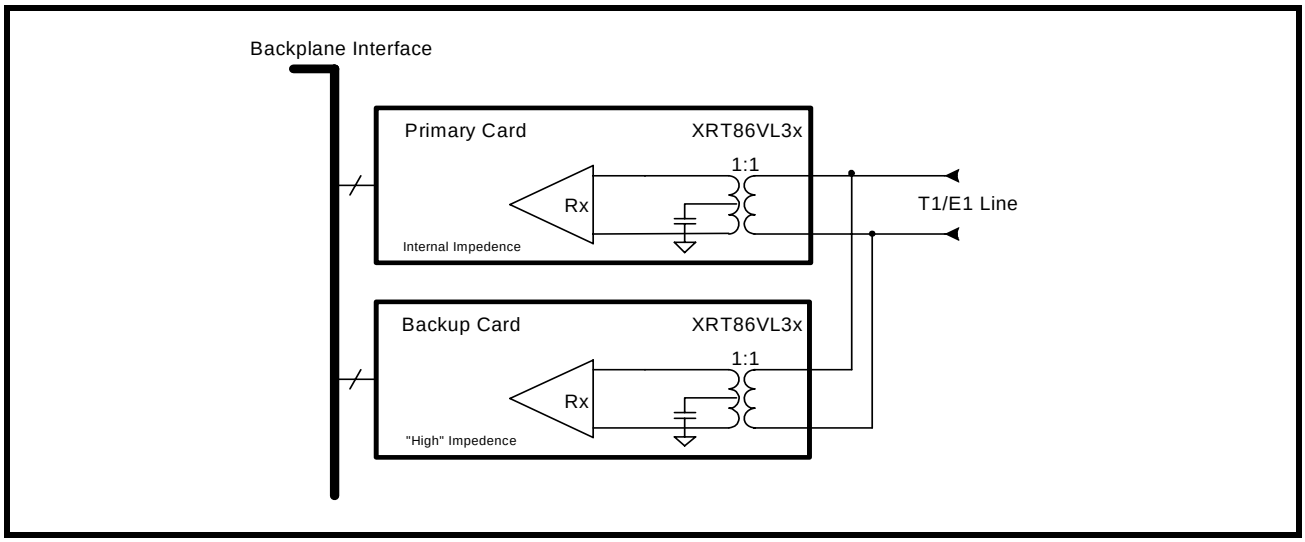
FIGURE 4. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR 1:1 AND 1+1 REDUNDANCY



1.2.5 Receive Interface with 1:1 and 1+1 Redundancy

The receivers on the backup card should be programmed for "High" impedance. Since there is no external resistor in the circuit, the receivers on the backup card will not load down the line interface. This key design feature eliminates the need for relays and provides one bill of materials for all interface modes of operation. Select the impedance for the desired mode of operation, T1/E1/J1. To swap the primary card, set the backup card to internal impedance, then the primary card to "High" impedance. See **Figure 5**. for a simplified block diagram of the receive section for a 1:1 redundancy scheme.

FIGURE 5. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR 1:1 AND 1+1 REDUNDANCY



1.3 Power Failure Protection

For 1:1 or 1+1 line card redundancy in T1/E1 applications, power failure could cause a line card to change the characteristics of the line impedance, causing a degradation in system performance. The XRT86VL3x was designed to ensure reliability during power failures. The LIU has patented high impedance circuits that allow the receiver inputs and the transmitter outputs to be in "High" impedance when the LIU experiences a power failure or when the LIU is powered off.

NOTE: *For power failure protection, a transformer must be used to couple to the line interface. See the TAN-56 application note for more details.*

1.4 Overvoltage and Overcurrent Protection

Physical layer devices such as LIUs that interface to telecommunications lines are exposed to overvoltage transients posed by environmental threats. An Overvoltage transient is a pulse of energy concentrated over a small period of time, usually under a few milliseconds. These pulses are random and exceed the operating conditions of CMOS transceiver ICs. Electronic equipment connecting to data lines are susceptible to many forms of overvoltage transients such as lightning, AC power faults and electrostatic discharge (ESD). There are three important standards when designing a telecommunications system to withstand overvoltage transients.

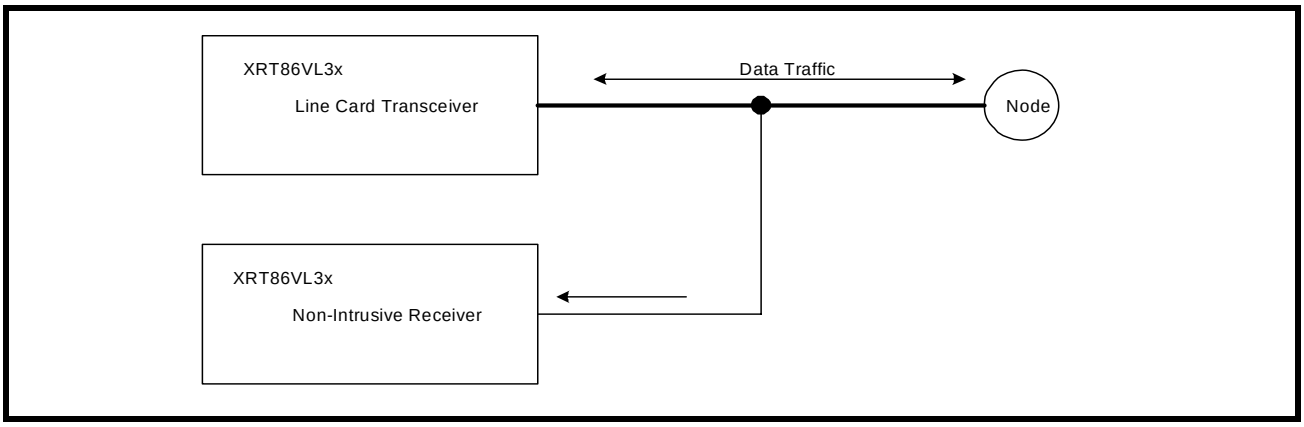
- UL1950 and FCC Part 68
- Telcordia (Bellcore) GR-1089
- ITU-T K.20, K.21 and K.41

NOTE: For a reference design and performance, *contact your local sales representative for more details.*

1.5 Non-Intrusive Monitoring

In non-intrusive monitoring applications, the transmitters are shut off by setting TxON "Low". The receivers must be actively receiving data without interfering with the line impedance. The XRT86VL3x's internal termination ensures that the line termination meets T1/E1 specifications for 75Ω, 100Ω or 120Ω while monitoring the data stream. System integrity is maintained by placing the non-intrusive receiver in "High" impedance, equivalent to that of a 1+1 redundancy application. A simplified block diagram of non-intrusive monitoring is shown in **Figure 6**.

FIGURE 6. SIMPLIFIED BLOCK DIAGRAM OF A NON-INTRUSIVE MONITORING APPLICATION



1.6 T1/E1 Serial PCM Interface

The most common mode is the standard serial PCM interface. Within this mode, only the serial data, serial clock, frame pulse and multi-frame pulse are required for both the transmit and receive paths. For the transmit path, only TxSER is a dedicated input to the device. All other signals to the transmit path in **Figure 7** can be programmed as either input or output. For the receive path, only RxSER and RxMSYNC are dedicated outputs from the device. All other signals in the receive path in **Figure 8** can be programmed as either input or output.

FIGURE 7. TRANSMIT T1/E1 SERIAL PCM INTERFACE

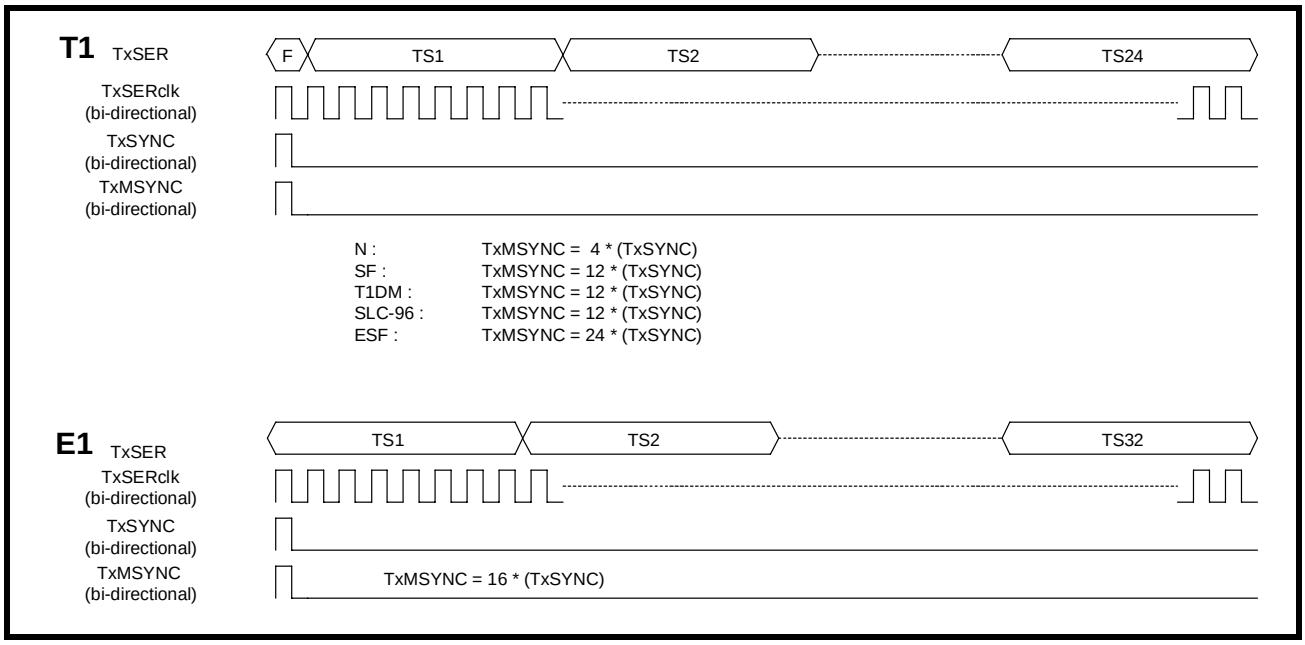
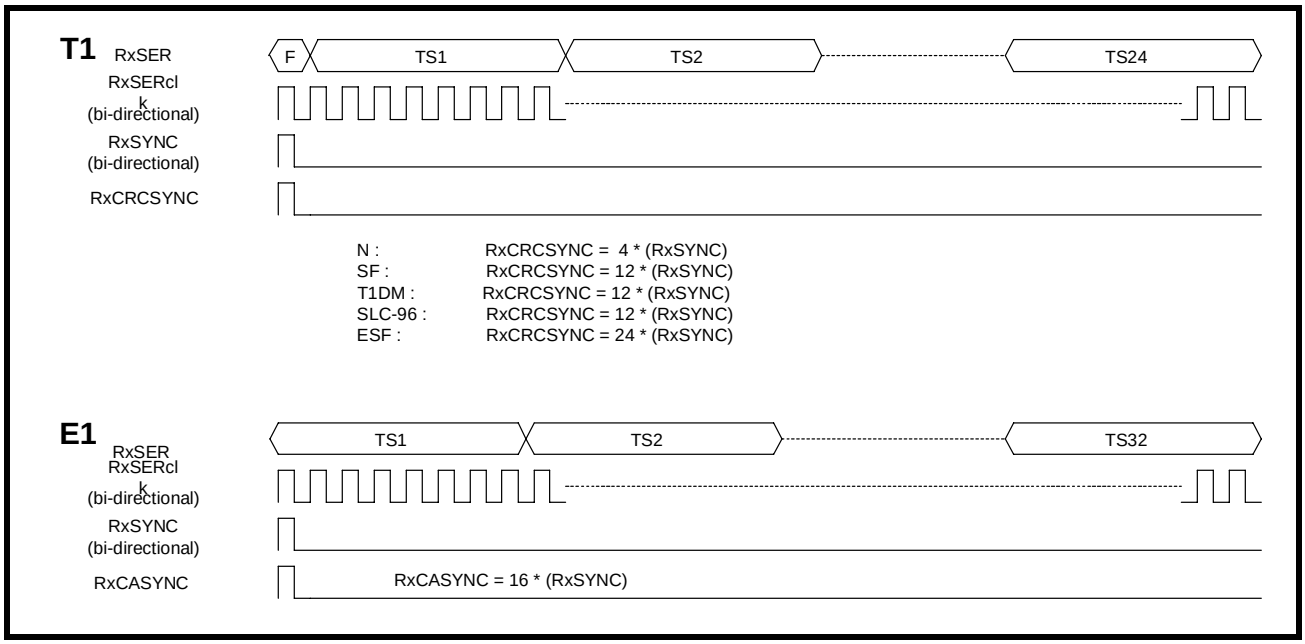


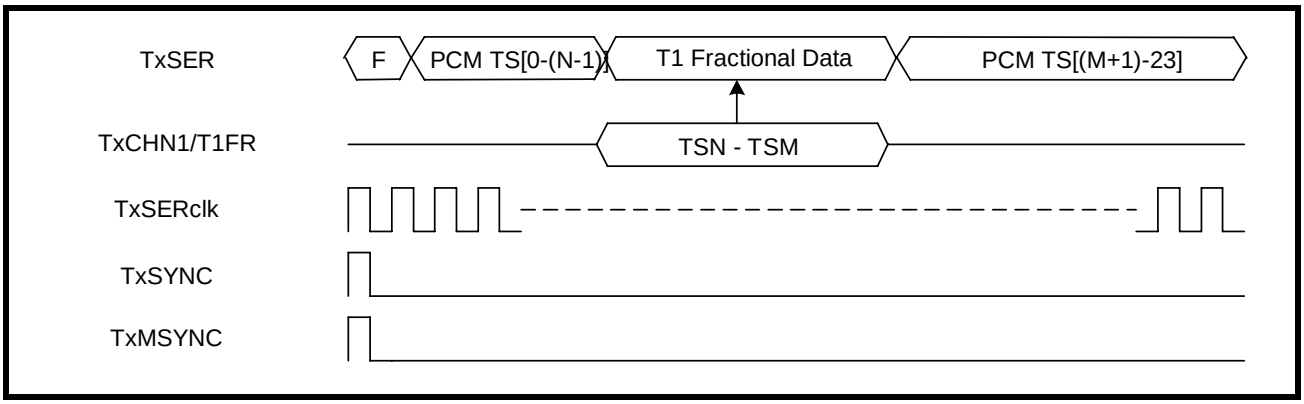
FIGURE 8. RECEIVE T1/E1 SERIAL PCM INTERFACE



1.7 T1/E1 Fractional Interface

The individual time slots can be enabled/disabled to carry fractional DS-0 data. The purpose of this interface is to enable one or more time slots in the PCM data (TxSER) to be replaced with the fractional DS-0 payload. If this mode is selected, the dedicated hardware pin TxCHN1/T1FR is used to input the fractional DS-0 data within the time slots that are enabled. The dedicated hardware pin RxCHN1/R1FR is used to output the fractional DS-0 data within the time slots that are enabled. **Figure 9** is a simplified diagram of the Fractional Interface.

FIGURE 9. T1 FRACTIONAL INTERFACE

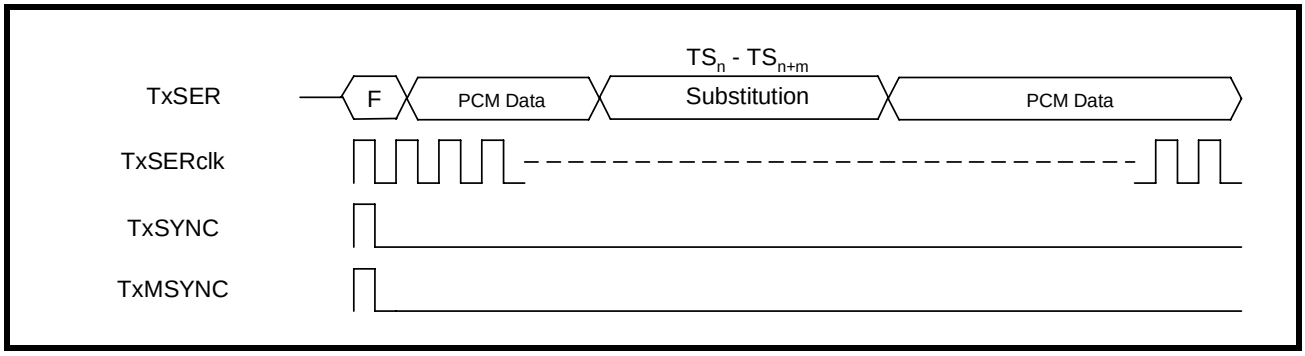


1.8 T1/E1 Time Slot Substitution and Control

The time slots within PCM data are reserved for carrying individual DS-0's. However, the framer block (transmit or receive paths) can substitute the payload with various code definitions. Each time slot can be independently programmed to carry normal PCM data or a variety of user codes. In E1 mode, the user can substitute the transmit time slots 0 and 16, although signaling and Frame Sync cannot be maintained. The following options for time slot substitution are available:

- Unchanged
- Invert all bits
- Invert even bits
- Invert odd bits
- Programmable User Code
- Busy 0xFF
- Vacant 0xD5
- Busy TS, Busy 00
- A-Law, μ-Law
- Invert the MSB bit
- Invert all bits except the MSB bit
- PRBS
- D/E Channel (or Fractional Input)

FIGURE 10. T1/E1 TIME SLOT SUBSTITUTION AND CONTROL



1.9 Robbed Bit Signaling/CAS Signaling

Signaling is used to convey status information relative to the individual DS-0's. If a particular DS-0 is On Hook, Off Hook, etc. this information is carried within the robbed bits in T1 (SF/ESF/SLC-96) or the sixteenth time slot in E1. On the transmit path, the Signaling information can be inserted through the PCM data, internal registers, or a dedicated external Signaling Bus by programming the appropriate registers. On the receive path, the signaling information is extracted (if enabled) to the internal registers and the external signaling bus in addition to being embedded within the PCM data. If the user wishes to substitute the ABCD values, the substitution only occurs in the PCM data. Once substituted, the internal registers and the external signaling bus will not be affected. **Figure 11** is a simplified block diagram showing the Signaling Interface. **Figure 12** is a timing diagram showing how to insert the ABCD values for each time slot in ESF / CAS. **Figure 13** is a timing diagram showing how to insert the AB values for SF / SLC-96 or 4-code signaling in ESF / CAS.

FIGURE 11. ROBBED BIT SIGNALING / CAS SIGNALING

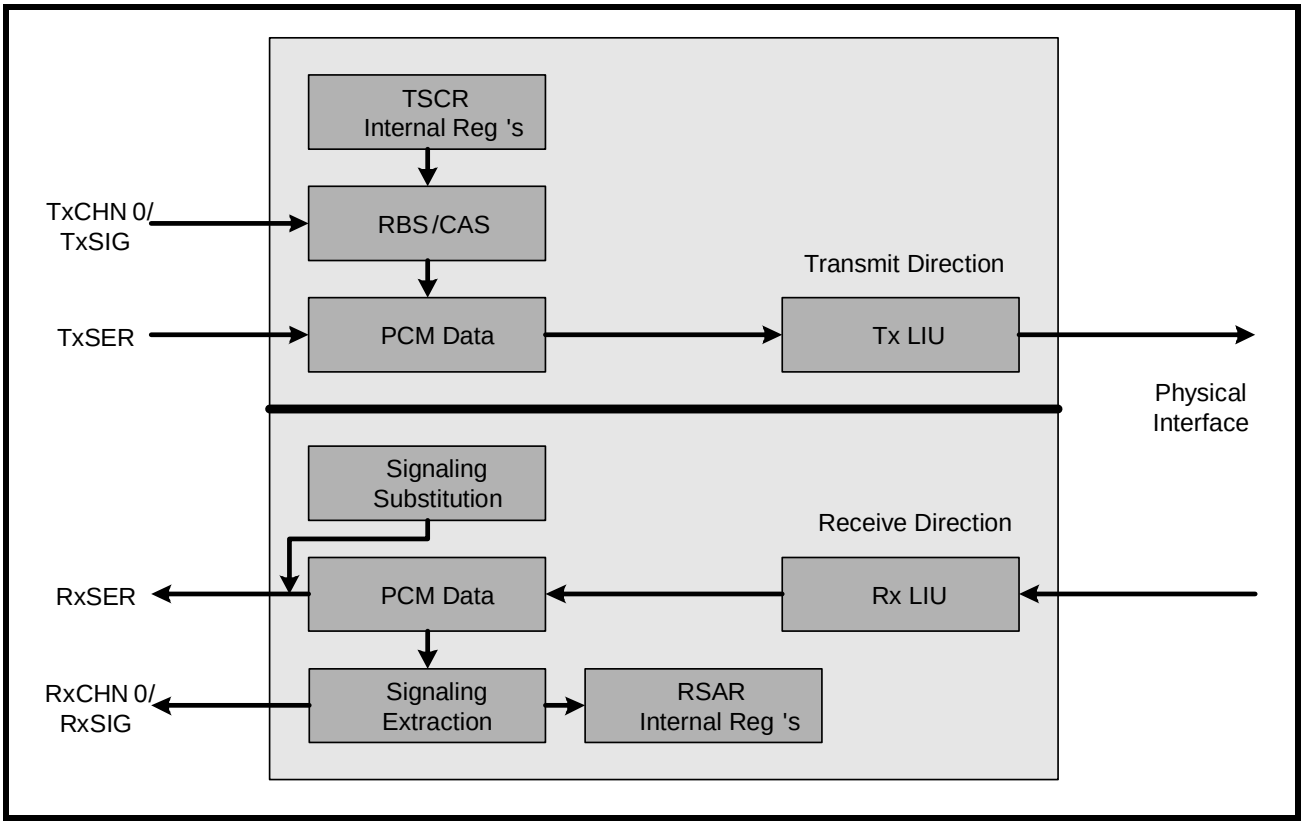


FIGURE 12. ESF / CAS EXTERNAL SIGNALING BUS

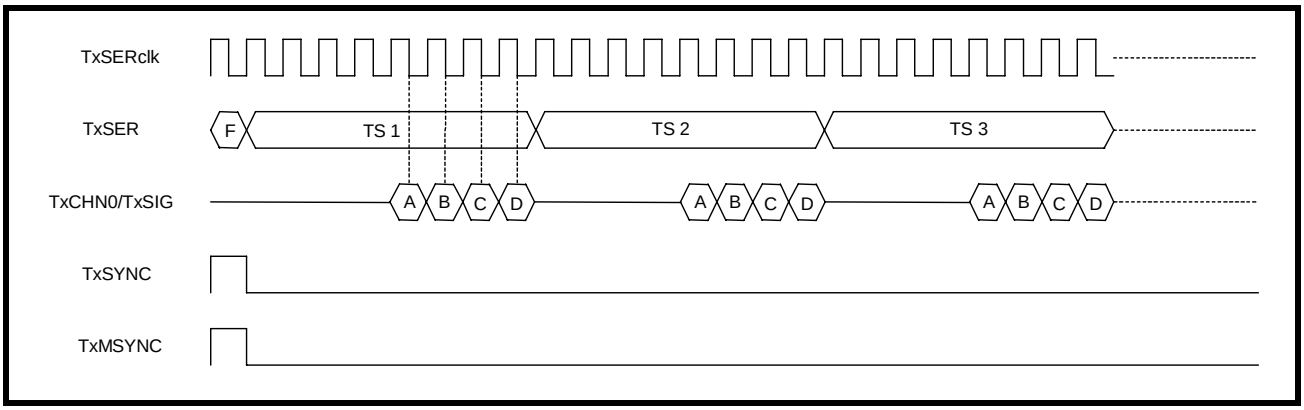
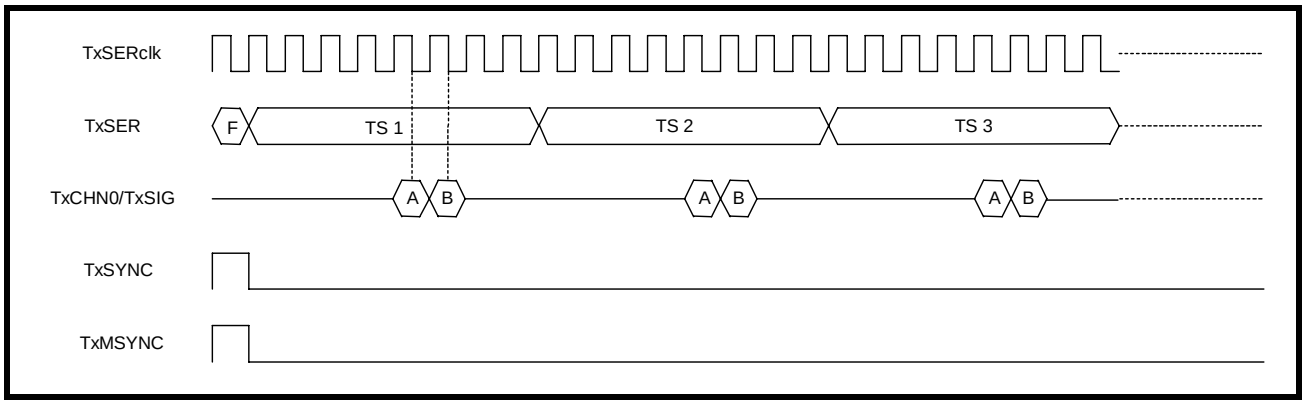


FIGURE 13. SF / SLC-96 OR 4-CODE SIGNALING IN ESF / CAS EXTERNAL SIGNALING BUS



1.10 Overhead Interface

The Overhead interface provides an option for inserting the datalink bits into the transmit PCM data or extracting the datalink bits from the receive PCM data. By default, the datalink information is processed to and from the PCM data directly. On the transmit path, the overhead clock is automatically provided as a clock reference to externally time the datalink bits. The user should provide data on the rising edge of the TxOHclk so that the framer can sample the datalink bits on the falling edge. On the receive path, the datalink bits are updated on the rising edge of the RxOHclk output pin. In T1 ESF mode, a datalink bit occurs every other frame. Therefore, the default overhead interface is operating at 4kbps. In E1 mode, the datalink bits are located in the first time slot of each Non-FAS frame. **Figure 14** is a simplified block diagram of the Overhead Interface. **Figure 15** is a simplified diagram for the T1 external overhead datalink bus. **Figure 16** is a simplified diagram for the E1 external overhead datalink bus.

FIGURE 14. T1/E1 OVERHEAD INTERFACE

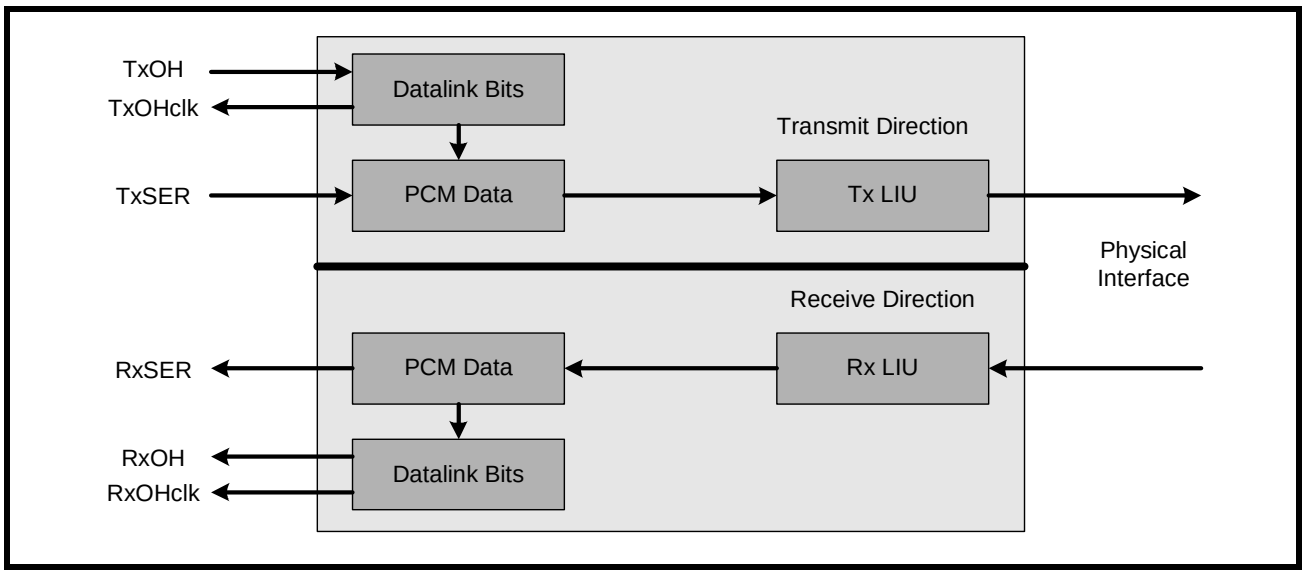


FIGURE 15. T1 EXTERNAL OVERHEAD DATALINK BUS

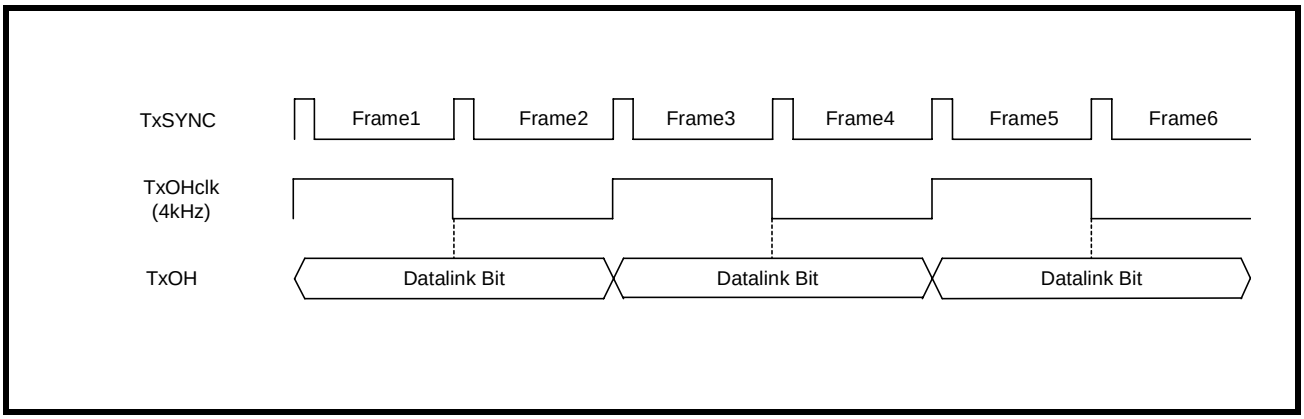
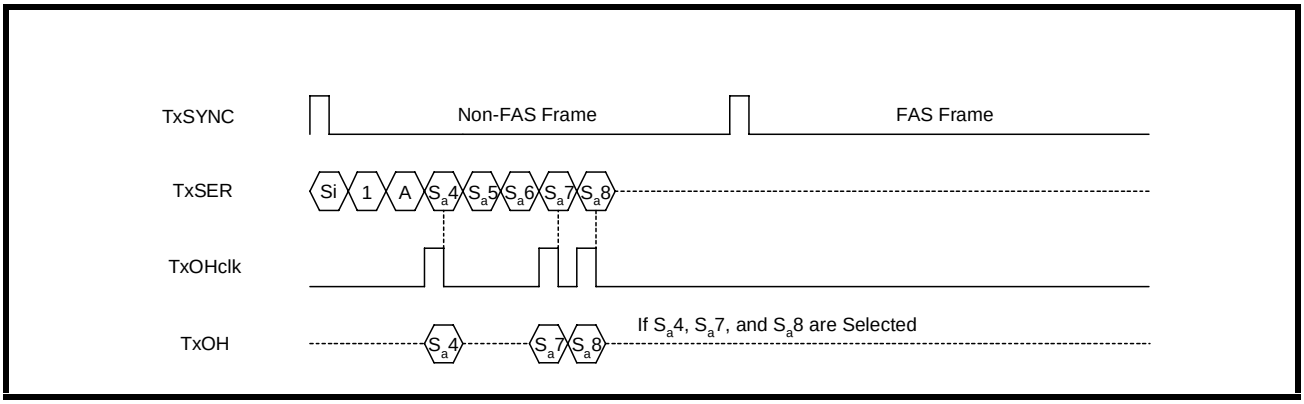


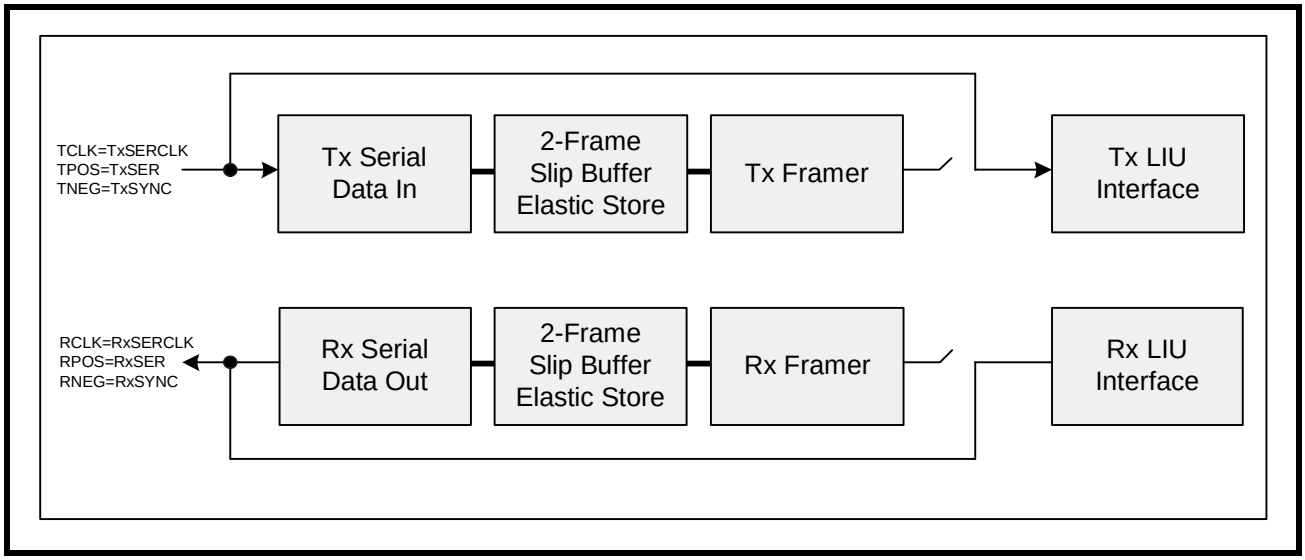
FIGURE 16. E1 OVERHEAD EXTERNAL DATALINK BUS



1.11 Framer Bypass Mode

The framer bypass mode allows the XRT86VL3x to be used as a stand alone Line Interface Unit. In this mode, a few of the backplane interface signals multiplex into the digital Input/output signals to and from the LIU block. Figure 22 shows a simplified block diagram of the framer bypass mode.

FIGURE 17. SIMPLIFIED BLOCK DIAGRAM OF THE FRAMER BYPASS MODE



1.12 High-Speed Non-Multiplexed Interface

The speed of transferring data through a back plane interface in a non-multiplexed manner typically operates at 1.544Mbps, 2.048Mbps, 4.096Mbps, or 8.192Mbps. For 12.352Mbps and 16.384Mbps, see the High-Speed Multiplexed Section. The T1/E1 carrier signal out to or in from the line interface is always 1.544MHz and 2.048MHz respectively. However, the back plane interface may be synchronous to a "Higher" speed clock. For T1, as shown in **Figure 18**, is mapped into an E1 frame. Therefore, every fourth time slot contains non-valid data. For E1, as shown in **Figure** , is simply synchronized to the "Higher" 8.192MHz clock signal supplied to the TxMSYNC input pin.

FIGURE 18. T1 HIGH-SPEED NON-MULTIPLEXED INTERFACE

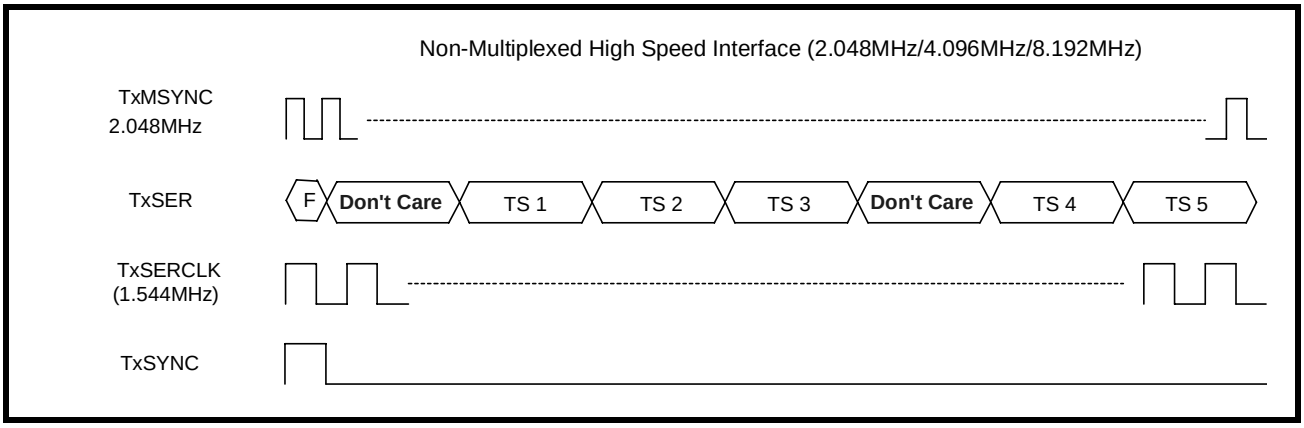
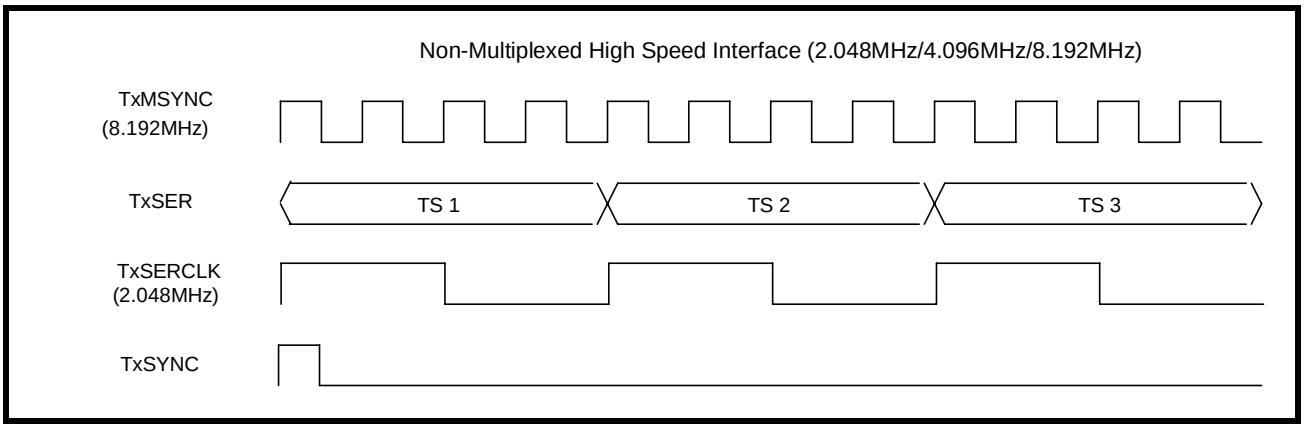


FIGURE 19. E1 HIGH-SPEED NON-MULTIPLEXED INTERFACE



1.13 High-Speed Multiplexed Interface

In addition to the non-multiplexed mode, the framer can interface through the backplane in a high-speed multiplexed application, either through a bit-muxed or byte-muxed (in HMVIP or H.100) manner. In this mode, the chip is divided into two multiplexed blocks, four channels per block. For T1, the high speed multiplexed modes are 12.352Mbps (bit-muxed, TxSYNC is "High" during the F-bit), 16.384Mbps (bit-muxed, TxSYNC is "High" during the F-bit), 16.384Mbps (HMVIP: byte-muxed, TxSYNC is "High" during the last 2-bits of the previous frame and the first 2-bits of the current frame), or 16.384Mbps (H.100: byte-muxed, TxSYNC is "High" during the last bit of the previous frame and the first bit in the current frame). For E1 mode, the only mode that is not supported is the 12.352Mbps. The only other difference is that the F-bit (for T1 mode) becomes the first bit of the E1 frame. **Figure 20** is a simplified block diagram of transmit bit-muxed application. **Figure 21** is a simplified block diagram of receive bit-muxed application. Although the data is only applied to channel 4 or channel 0, the TxSERCLK is necessary for all channels so that the transmit line rate is always equal to the T1/E1 carrier rate.

FIGURE 20. TRANSMIT HIGH-SPEED BIT MULTIPLEXED BLOCK DIAGRAM

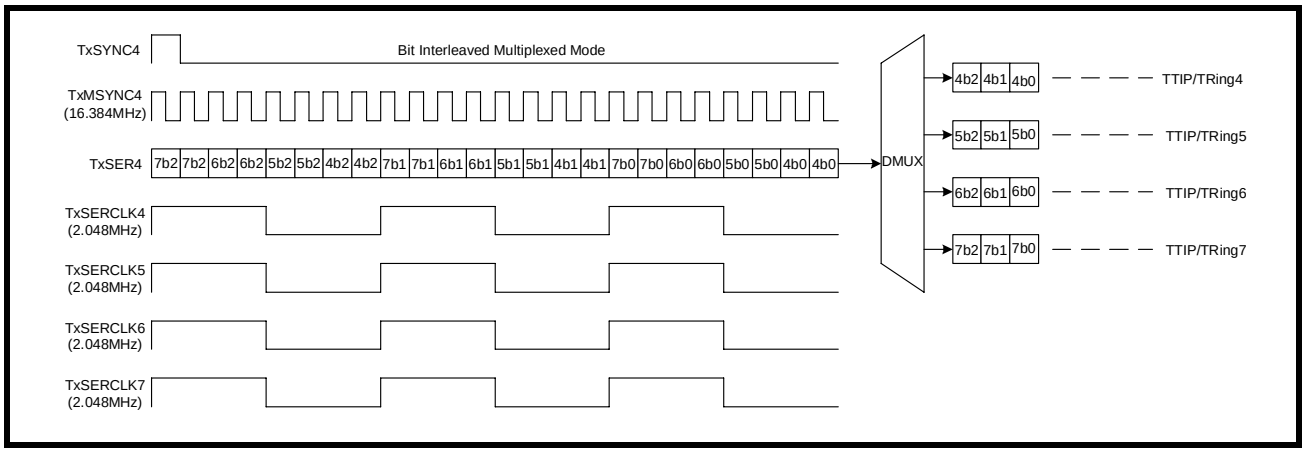
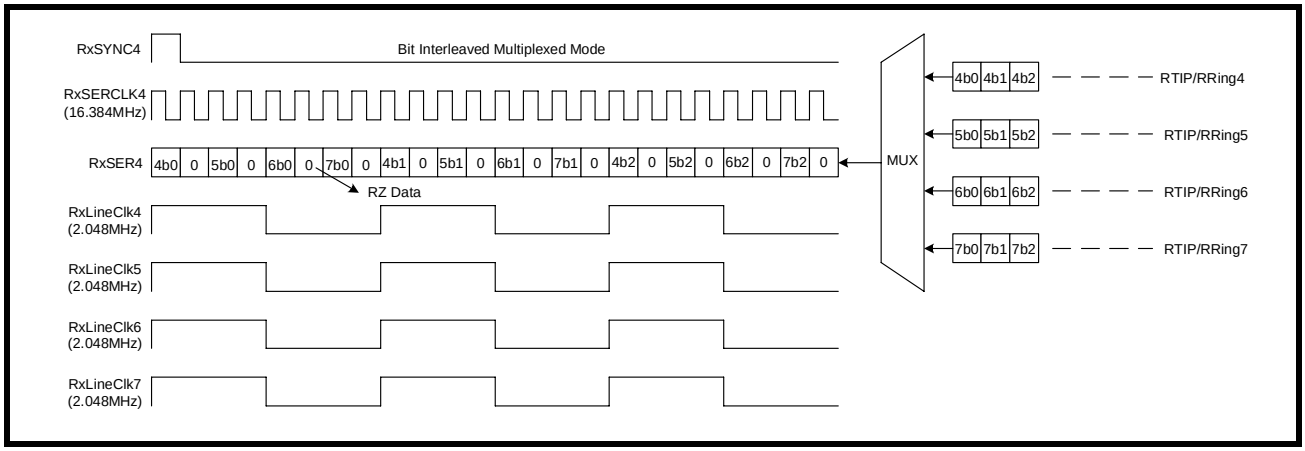


FIGURE 21. RECEIVE HIGH-SPEED BIT MULTIPLEXED BLOCK DIAGRAM



2.0 LOOPBACK MODES OF OPERATION

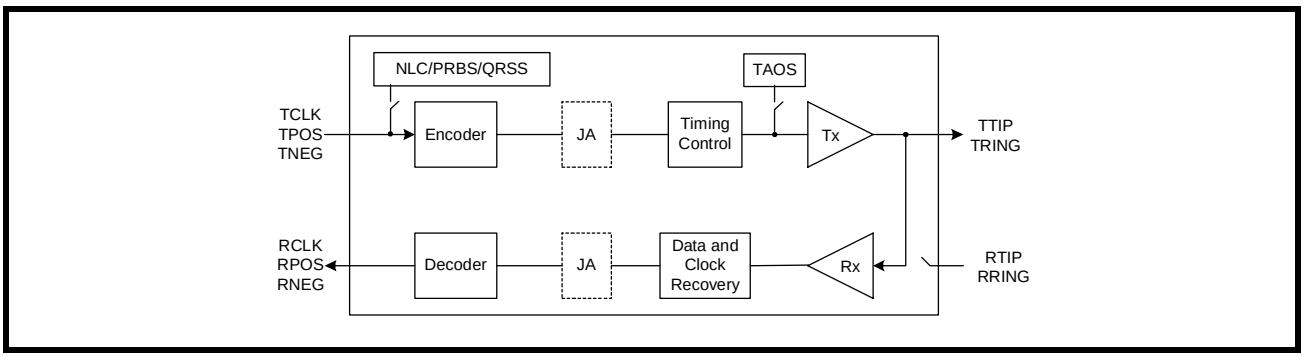
2.1 LIU Physical Interface Loopback Diagnostics

The XRT86VL3x supports several loopback modes for diagnostic testing. The following section describes the local analog loopback, remote loopback, digital loopback, and dual loopback modes. The LIU physical interface loopback modes are independent from the Framer loopback modes. Therefore, it is possible to configure multiple loopback modes creating tremendous flexibility within the looped diagnostic features.

2.1.1 Local Analog Loopback

With local analog loopback activated, the transmit output data at TTIP/TRING is internally looped back to the analog inputs at RTIP/RRING. External inputs at RTIP/RRING are ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of local analog loopback is shown in **Figure 22**.

FIGURE 22. SIMPLIFIED BLOCK DIAGRAM OF LOCAL ANALOG LOOPBACK

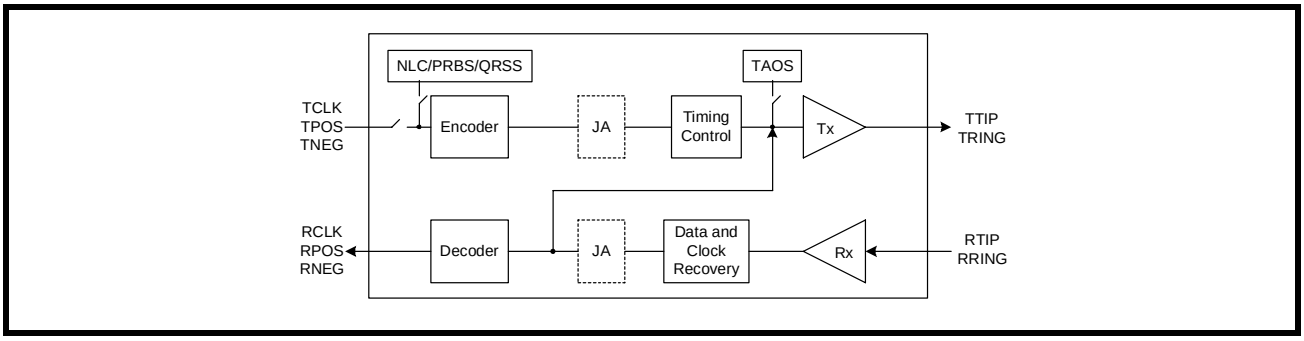


NOTE: *The transmit diagnostic features such as TAOS, NLC generation, and QRSS take priority over the transmit input data at TCLK/TPOS/TNEG.*

2.1.2 Remote Loopback

With remote loopback activated, the receive input data at RTIP/RRING is internally looped back to the transmit output data at TTIP/TRING. The remote loopback includes the Receive JA (if enabled). The transmit input data at TCLK/TPOS/TNEG are ignored while valid receive output data continues to be sent to the system. A simplified block diagram of remote loopback is shown in **Figure 23**.

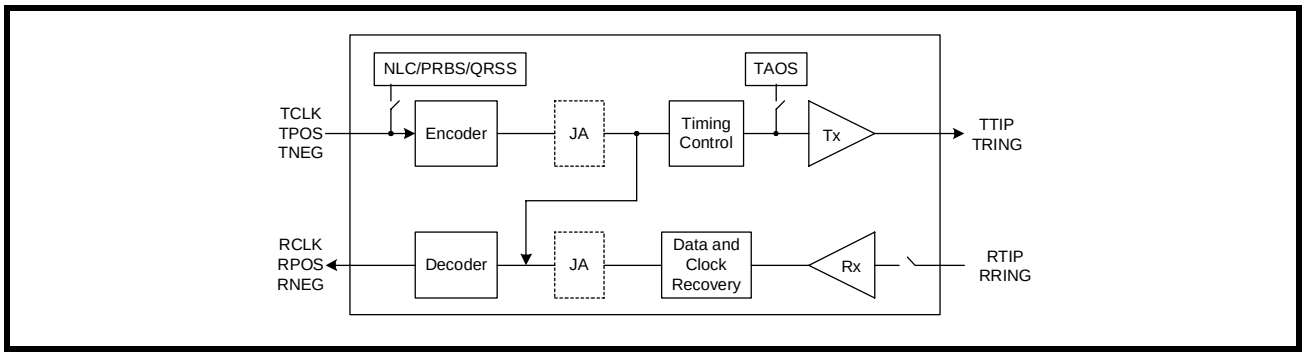
FIGURE 23. SIMPLIFIED BLOCK DIAGRAM OF REMOTE LOOPBACK



2.1.3 Digital Loopback

With digital loopback activated, the transmit input data at TCLK/TPOS/TNEG is looped back to the receive output data at RCLK/RPOS/RNEG. The digital loopback mode includes the Transmit JA (if enabled). The receive input data at RTIP/RRING is ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of digital loopback is shown in **Figure 24**.

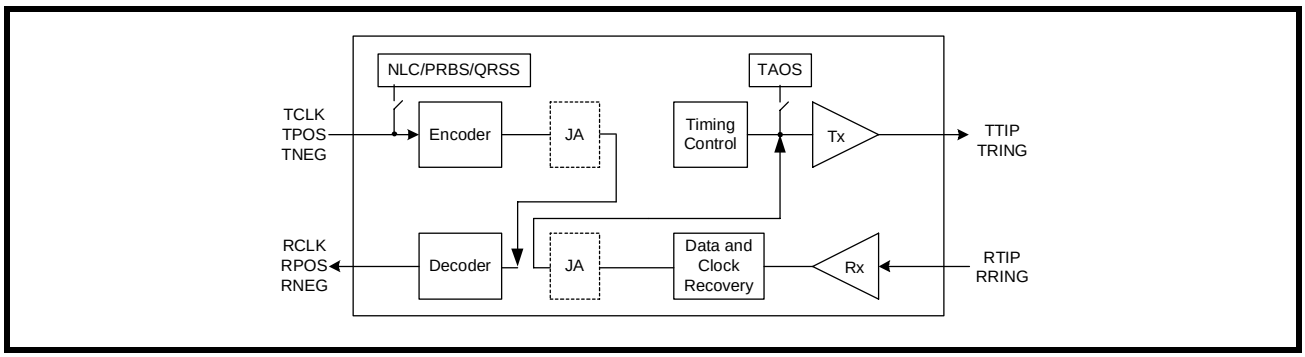
FIGURE 24. SIMPLIFIED BLOCK DIAGRAM OF DIGITAL LOOPBACK



2.1.4 Dual Loopback

With dual loopback activated, the remote loopback is combined with the digital loopback. A simplified block diagram of dual loopback is shown in **Figure 25**.

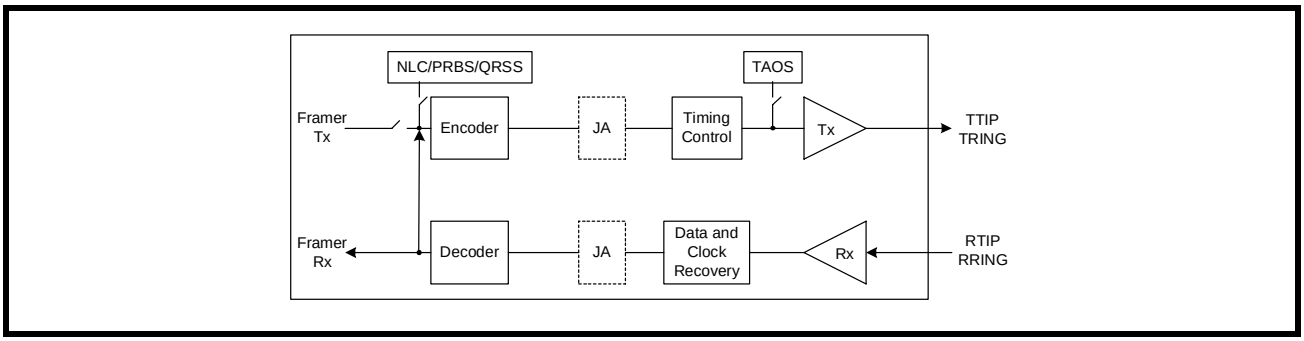
FIGURE 25. SIMPLIFIED BLOCK DIAGRAM OF DUAL LOOPBACK



2.1.5 Framer Remote Line Loopback

The Framer Remote Line Loopback is almost identical to the LIU physical interface Remote Loopback. The digital data enters the framer interface, however does not enter the framing blocks. The main difference between the Remote loopback and the Framer Remote Line loopback is that the receive digital data from the LIU is allowed to pass through the LIU Decoder/Encoder circuitry before returning to the line interface. A simplified block diagram of framer remote line loopback is shown in **Figure 26**.

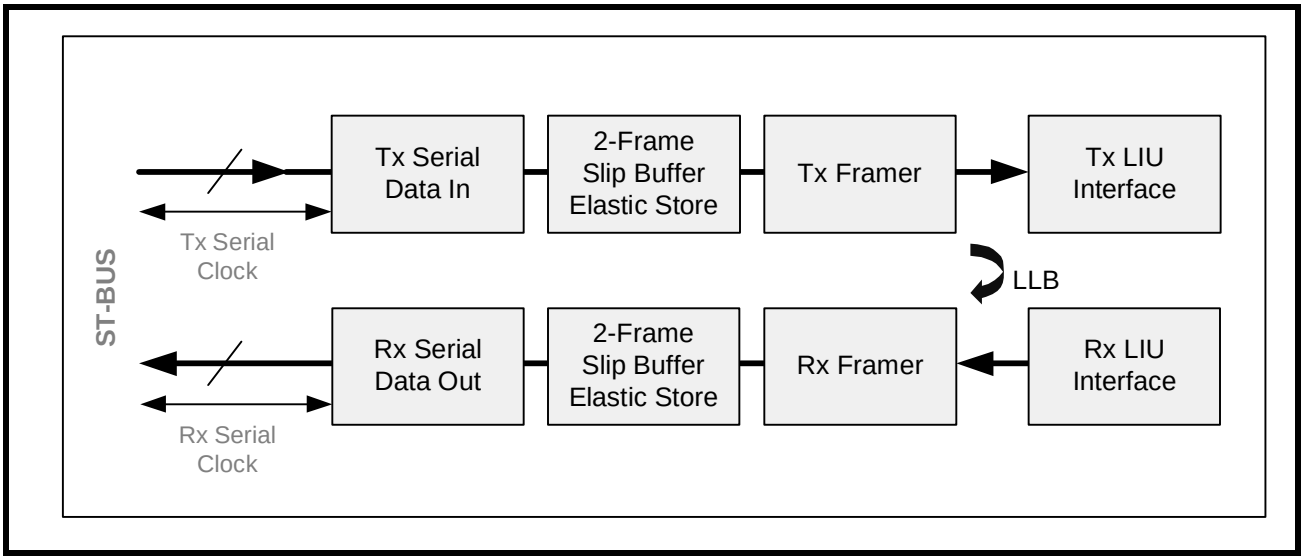
FIGURE 26. SIMPLIFIED BLOCK DIAGRAM OF THE FRAMER REMOTE LINE LOOPBACK



2.1.6 Framer Local Loopback

With framer local loopback activated, the transmit PCM input data is looped back to the receive PCM output data. The receive input data at RTIP/RRING is ignored while an All Ones Signal is transmitted out to the line interface. A simplified block diagram of framer remote line loopback is shown in **Figure 27**.

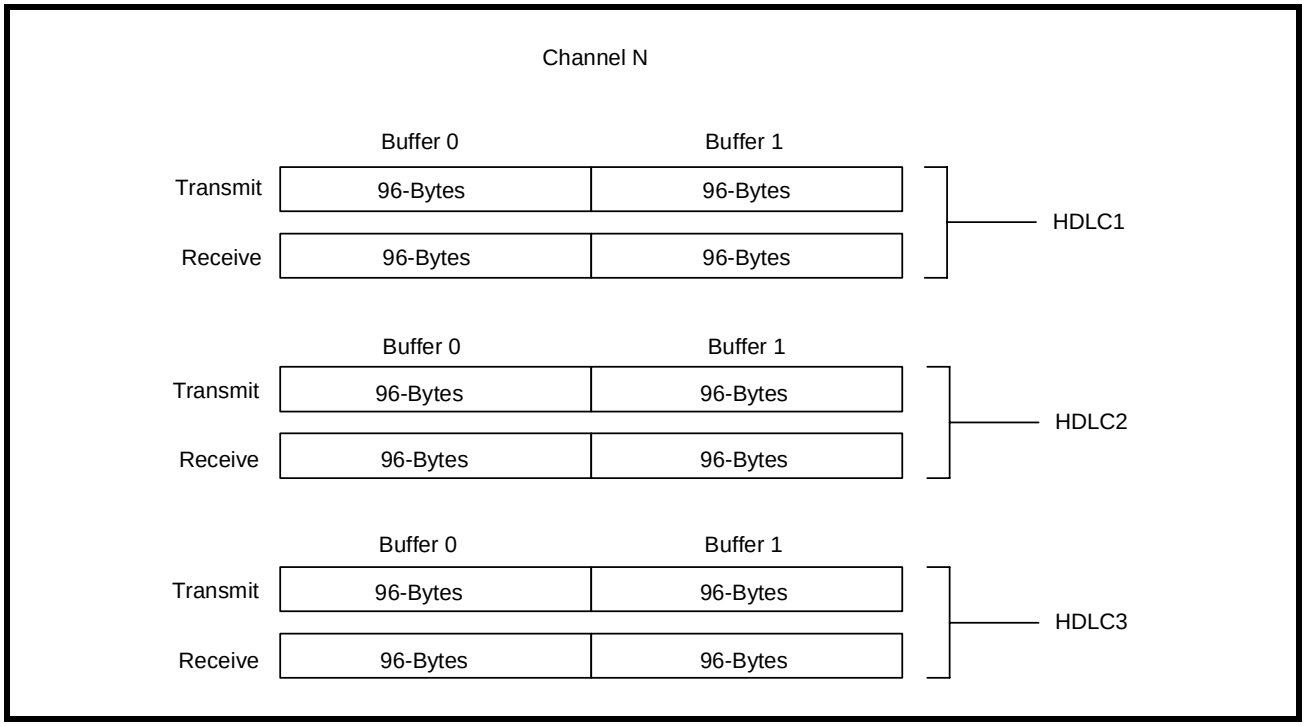
FIGURE 27. SIMPLIFIED BLOCK DIAGRAM OF THE FRAMER LOCAL LOOPBACK



3.0 HDLC CONTROLLERS AND LAPD MESSAGES

The purpose of the HDLC controllers is to allow messages to be stored for transport in the outbound transmit framer block or extracted from the receive framer block through the LAPD interface. Each channel within the Framer has 3 independent HDLC controllers. Each HDLC controller has two 96-Byte buffers for Transmit and two 96-Byte buffers for Receive. The buffers are used to insert messages into the out going data stream for Transmit or to extract messages from the incoming data stream from the Receive path. Total, there are twelve 96-Byte buffers per channel. This allows multiple HDLC messages to be transported to and from EXAR's framing device.

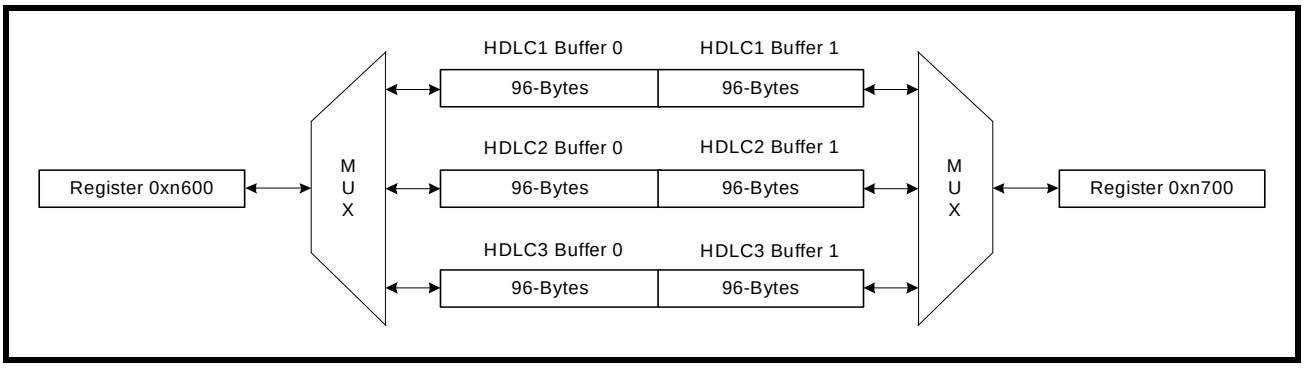
FIGURE 28. HDLC CONTROLLERS



3.1 Storing and Retrieving Message Contents

Each buffer has its own dedicated internal holding register. To access the contents of these buffers or to store messages, the XRT86VL3x utilizes a multiplexed access. The buffers are broken down into Buffer 0 or Buffer 1. Register 0xn600 is used to Read or Write to Buffer 0 of the selected HDLC controller, while register 0xn700 is used to Read or Write to Buffer 1 of the selected HDLC controller. Although, each HDLC controller has its own dedicated register set for control, the message contents of only one controller can be accessed at one time through the microprocessor or DMA interface.

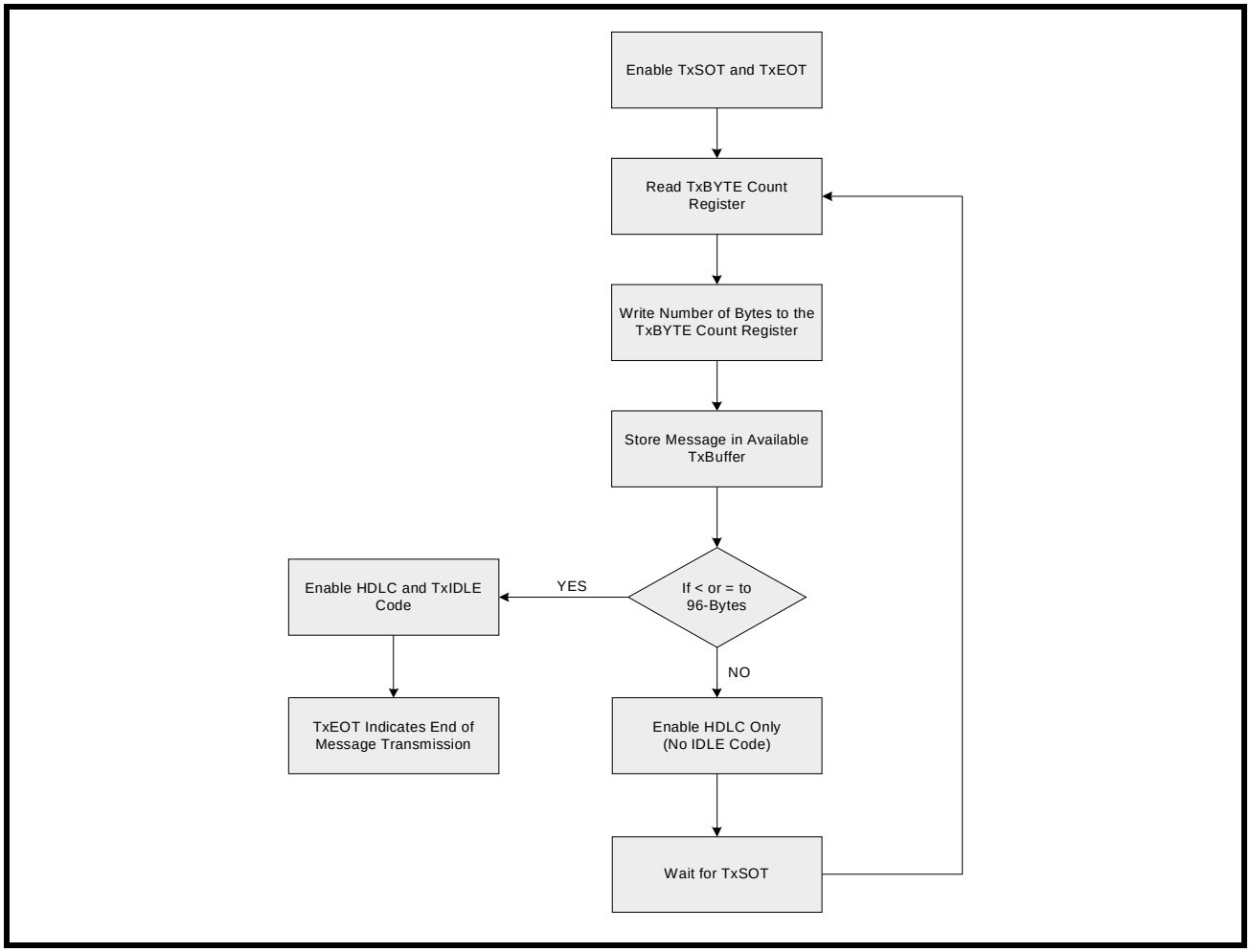
FIGURE 29. STORING AND RETRIEVING MESSAGE CONTENTS



3.2 Programming Sequence for Sending HDLC Messages

Once the data link source and the type of message has been chosen, the following programming sequence can be followed to send any length message.

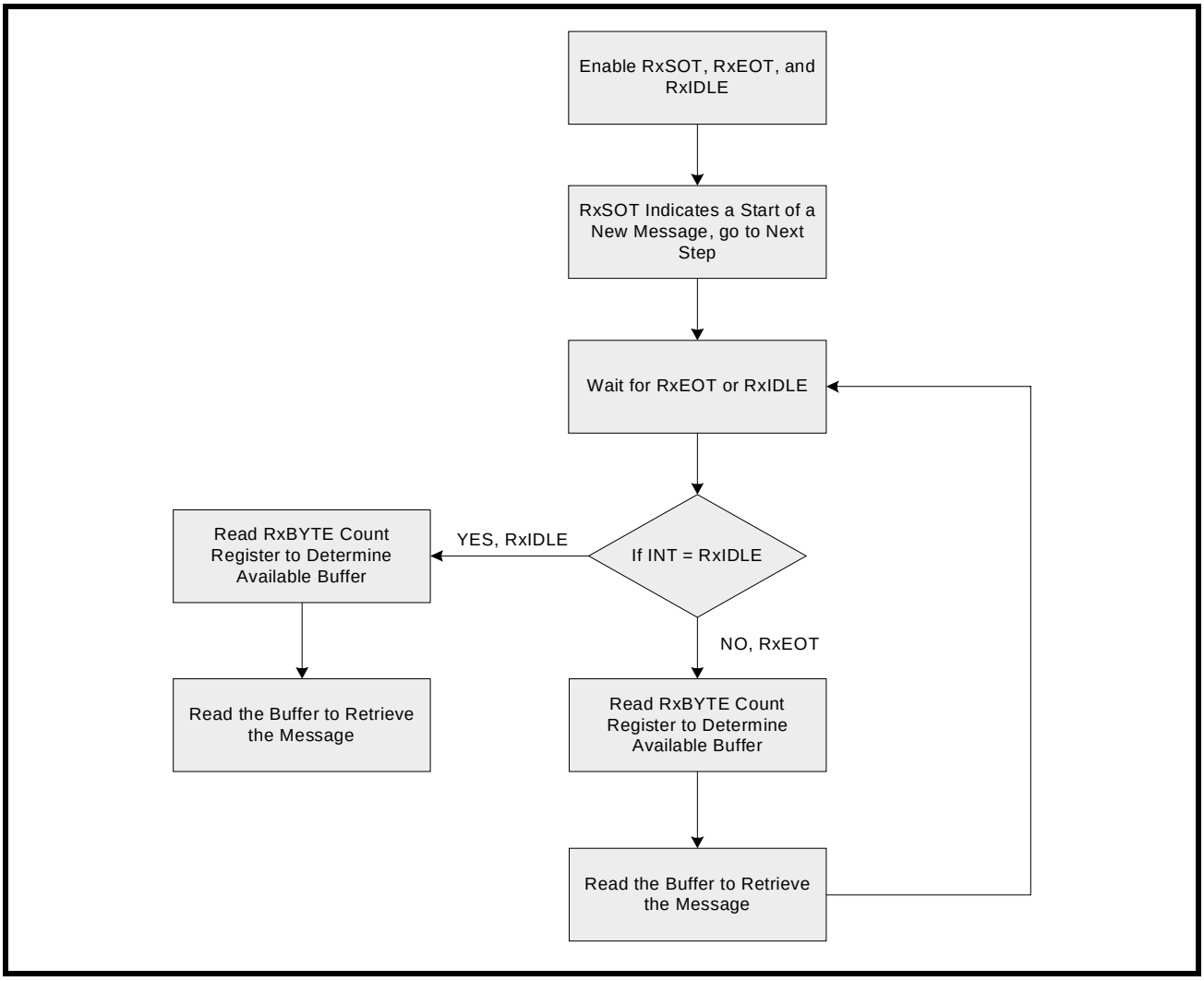
FIGURE 30. SENDING HDLC MESSAGES



3.3 Programming Sequence for Receiving LAPD Messages

The XRT86VL3x can extract data link information from incoming DS1 frames from either the datalink bits themselves or the D/E time slots within the PCM input data. To extract a LAPD message, the following programming sequence can be used as a reference.

FIGURE 31. RECEIVING HDLC MESSAGES



3.4 Receive HDLC Event Timing

The following figure shows the event timing of RxEOT and RxIDLE when receiving HDLC message.

FIGURE 32. RECEIVE HDLC EVENT TIMING

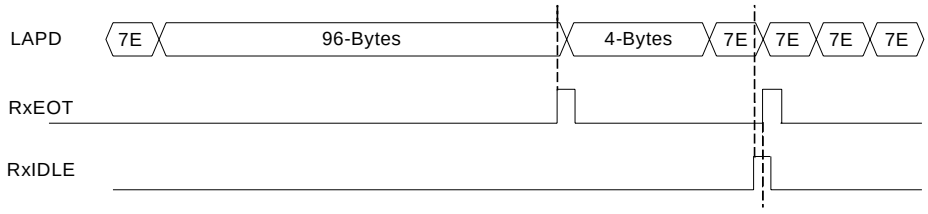


Figure a. Receiving a 100-Byte Message

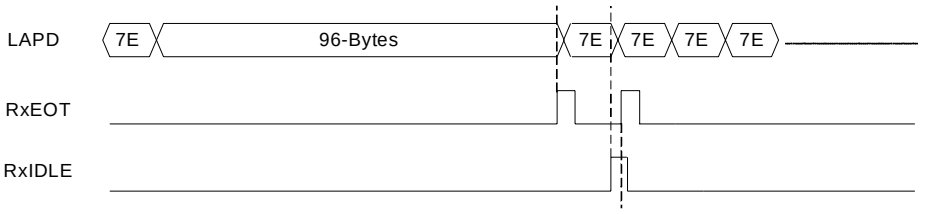


Figure b. Receiving a 96-Byte Message

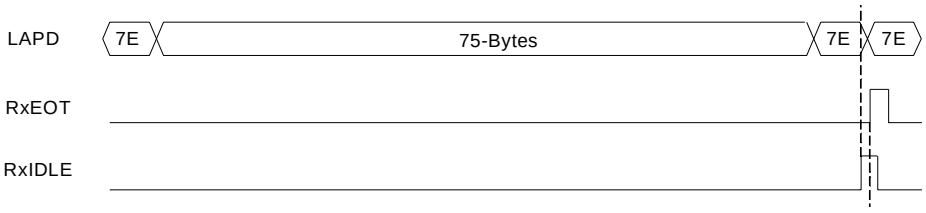


Figure c. Receiving a 75-Byte Message

3.5 SS7 (Signaling System Number 7) for ESF in DS1 Only

To support SS7 specifications while receiving LAPD messages, EXAR's Framer will generate an interrupt (if SS7 is enabled) once the HDLC controllers have received more than 276 bytes within two flag sequences (0x7E) of a LAPD message. Each HDLC controller supports SS7. For example: To enable SS7 for all HDLC controllers, registers 0xnB11 (LAPD1), 0xnB19 (LAPD2), 0xnB29 (LAPD3) must be set to 0x01.

3.6 DS1/E1 Datalink Transmission Using the HDLC Controllers

The transmit framer block can insert data link information to outbound DS1/E1 frames. The data link information can be inserted from the following sources.

- Transmit Overhead Input Interface (TxOH)
- Transmit HDLC1 Controller
- Transmit Serial Input Interface (TxSER)

NOTE: *HDLC1 is the dedicated controller for transmission of LAPD messages through the datalink bits. If the datalink bits are not used for LAPD messages, then HDLC1 can be used through the D/E time slots as with HDLC2 and HDLC3.*

The Transmit Data Link Source Select bits within the Transmit Data Link Select Register (TSDLSR) determine the source for the data link bits in ESF, SLC®96, or T1DM for DS1 and CRC multi frame for E1. Each Transmit HDLC Controller contains four major functional modules.

- Bit-Oriented Signaling Processor
- LAPD Controller
- SLC®96 Data Link Controller
- Automatic Performance Report (APR) Generation

3.7 Transmit BOS (Bit Oriented Signaling) Processor

The Transmit BOS Processor handles transmission of BOS messages through the data link channel. The processor can be set for a specific amount of repetitions a certain BOS message will be transmitted, or it may be placed in an infinite loop. The processor can also insert a BOS IDLE flag sequence and/or an ABORT sequence to be transmitted on the data link channel.

3.7.1 Description of BOS

Bit-Oriented Signaling messages are a 16-bit pattern of which a 6-bit message is embedded as shown in the following table.

BOS MESSAGE FORMAT															
0	D5	D4	D3	D2	D1	D0	0	1	1	1	1	1	1	1	1

Where D5 is the MSB and D0 is the LSB. The rightmost "1" is transmitted first. BOS is classified into the following two groups.

- Priority Codeword Message
- Command and Response Information

3.7.2 Priority Codeword Message

A Priority Codeword Message is preemptive and has the highest priority among all data link information. A Priority Codeword indicates a condition that is affecting the quality of service and thus shall be transmitted until the condition no longer exists. The duration of transmission should not be less than one second. A priority codeword may be interrupted by software for 100 milliseconds to send maintenance commands with a minimum interval of one second between interruptions. Yellow alarm (00000000 11111111) is the only priority message defined in industry standards.

3.7.3 Command and Response Information

Command and Response Information is transmitted to perform various functions. The BOS Processor can send a command and response by transmitting a minimum of 10 repetitions of the appropriate codeword pattern. A Command and response data transmission initiates action at the remote end, while the remote end will respond by sending Bit-Oriented response message to acknowledge the received commands. The activation and deactivation of line remote loop-back and local payload loop-back functions are of this type.

3.8 Transmit MOS (Message Oriented Signaling) Processor

The Transmit LAPD controller implements the Message-Oriented protocol based on ITU Recommendation Q.921 Link Access Procedures on the D-channel. It provides the following functions.

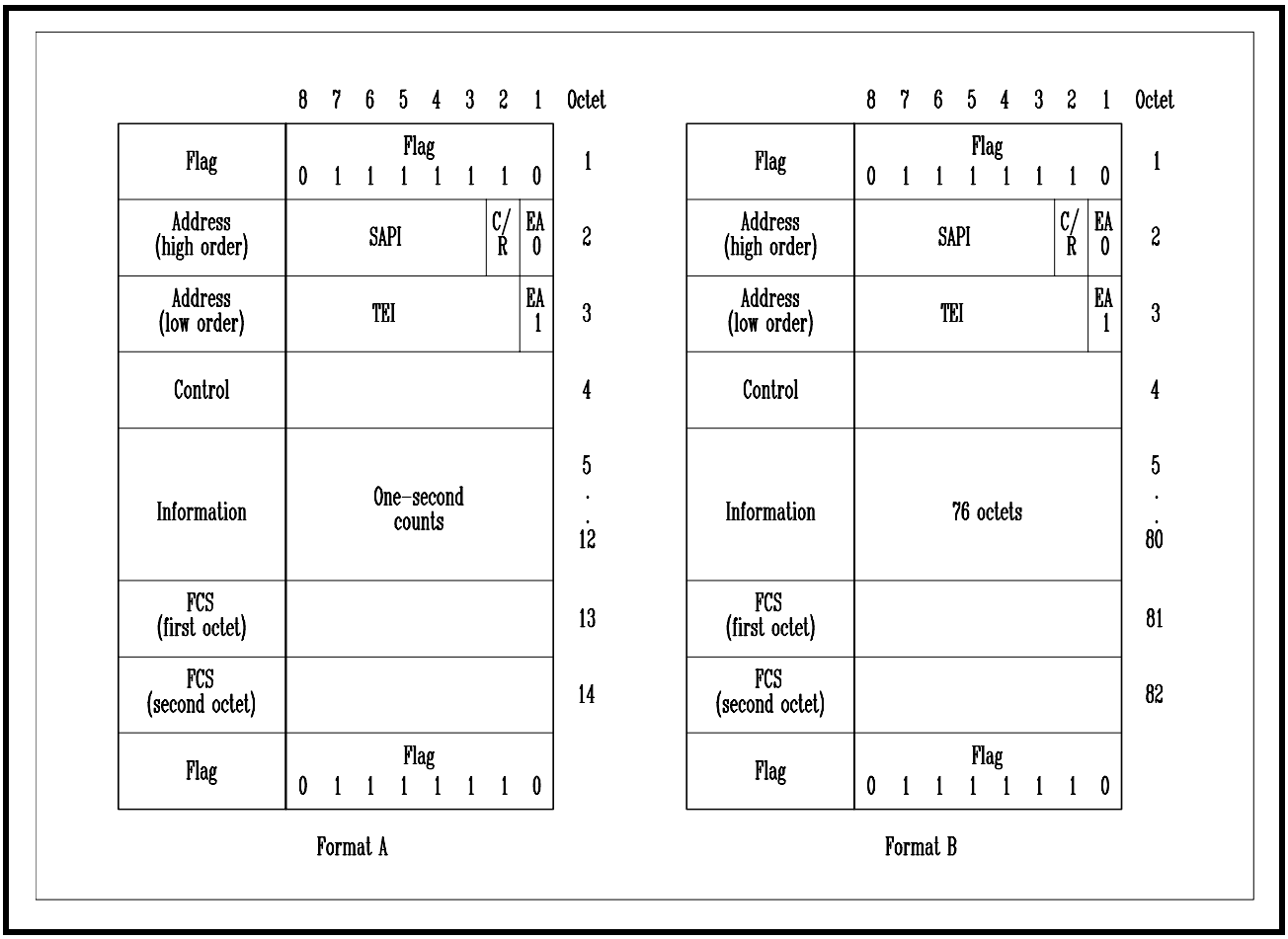
- Zero stuffing
- T1/E1 transmitter interface
- Transmit message buffer access
- Frame check sequence generation
- IDLE flag insertion
- ABORT sequence generation

Two 96-byte buffers in shared memory are allocated for each LAPD to reduce the frequency of microprocessor interrupts and alleviate the response time requirement for a microprocessor to handle each interrupt. There are no restrictions on the length of the message. However the 96-byte buffer is deep enough to hold one entire LAPD path or test signal identification message.

3.8.1 Discussion of MOS

Message-Oriented signals sent by the transmit LAPD Controller are messages conforming to ITU Recommendation Q.921 LAPD protocol. There are two types of Message-Oriented signals. One is a periodic performance report generated by the source or sink T1/E1 terminals as defined by ANSI T1.403. The other is a path or test signal identification message that may be optionally generated by a terminal or intermediate equipment on a T1/E1 circuit. The message structures of the performance report and path or test signal identification message are shown in **Figure 33** for format A and format B respectively.

FIGURE 33. LAPD FRAME STRUCTURE



3.8.2 Periodic Performance Report

The ANSI T1.403 standard requires that the status of the transmission quality be reported in one-second intervals. The one-second timing may be derived from the DS1 signal or from a separate equally accurate (±32ppm) source. The phase of the one-second periods does not depend on the time of occurrence of any error event. A total of four seconds of information is transmitted so that recovery operations may be initiated in case an error corrupts a message. Counts of events shall be accumulated in each contiguous one-second interval. At the end of each one-second interval, a modulo-4 counter shall be incremented, and the appropriate performance bits shall be set in bytes 5 and 6 in Format A. These octets and the octets that carry the performance bits of the preceding three one-second intervals form the periodic performance report.

The periodic performance report is made up of 14 bytes of data. Bytes 1 to 4, 13, and 14 are the message header and bytes 5 to 12 contain data regarding the four most-recent one-second intervals. The periodic performance report message uses the SAPI/TEI value of 0x14.

3.8.3 Transmission-Error Event

Occurrences of transmission-error events indicate the quality of transmission. The occurrences that shall be detected and reported are:

- CRC Error Event: A CRC-6 error event is the occurrence of a received CRC code that is not identical to the corresponding locally calculated code.
- Severely Errored Framing Event: A severely-errored-framing event is the occurrence of two or more framing-bit-pattern errors within a 3-ms period. Contiguous 3-ms intervals shall be examined. The 3-ms period may coincide with the ESF. The severely-errored-framing event, while similar in form to criteria for declaring a

terminal has lost framing, is only designed as a performance indicator; existing terminal out-of-frame criteria will continue to serve as the basis for terminal alarms.

- Frame-Synchronization-Bit Error Event: A frame-synchronization-bit-error event is the occurrence of a received framing-bit-pattern not meeting the severely-errored-framing event criteria.
- Line-Code Violation event: A line-code violation event is a bipolar violation of the incoming data. A line-code violation event for an B8ZS-coded signal is the occurrence of a received excessive zeros (EXZ) or a bipolar violation that is not part of a zero-substitution code.
- Controlled Slip Event: A controlled-slip event is a replication, or deletion, of a T1 frame by the receiving terminal. A controlled slip may occur when there is a difference between the timing of a synchronous receiving terminal and the received signal.

3.8.4 Path and Test Signal Identification Message

The path identification message is used to identify the path between the source terminal and the sink terminal. The test signal identification message is used by test signal generating equipment. Both identification messages are made up of 82 bytes of data. Byte 1 to 4, 81 and 82 are the message header and bytes 5 to 80 contain six data elements. These messages use the SAPI/TEI value of 0x15 to differentiate themselves from the performance report message.

3.8.5 Frame Structure

The message structure of message-oriented signal is shown in **Figure 33**. Two format types are shown in the figure: format A for frames which are sending performance report message and format B for frames which containing a path or test signal identification message. The following abbreviations are used:

- SAPI: Service Access Point Identifier
- C/R: Command or Response
- EA: Extended Address
- TEI: Terminal Endpoint Identifier
- FCS: Frame Check Sequence

3.8.6 Flag Sequence

All frames shall start and end with the flag sequence consisting of one 0 bit followed by six contiguous 1 bits and one 0 bit. The flag preceding the address field is defined as the opening flag. The flag following the Frame Check Sequence (FCS) field is defined as the closing flag. The closing flag may also serve as the opening flag of the next frame, in some applications. However, all receivers must be able to accommodate receipt of one or more consecutive flags.

3.8.7 Address Field

The address field consists of two octets. A single octet address field is reserved for LAPB operation in order to allow a single LAPB data link connection to be multiplexed along with LAPD data link connections.

3.8.8 Address Field Extension bit (EA)

The address field range is extended by reserving bit 1 of the address field octets to indicate the final octet of the address field. The presence of a 1 in bit 1 of an address field octet signals that it is the final octet of the address field. The double octet address field for LAPD operation shall have bit 1 of the first octet set to a 0 and bit 1 of the second octet set to 1.

3.8.9 Command or Response bit (C/R)

The Command or Response bit identifies a frame as either a command or a response. The user side shall send commands with the C/R bit set to 0, and responses with the C/R bit set to 1. The network side shall do the opposite; That is, commands are sent with C/R bit set to 1, and responses are sent with C/R bit set to 0.

3.8.10 Service Access Point Identifier (SAPI)

The Service Access Point Identifier identifies a point at which data link layer services are preceded by a data link layer entity type to a layer 3 or management entity. Consequently, the SAPI specifies a data link layer entity type that should process a data link layer frame and also a layer 3 or management entity, which is to receive information carried by the data link layer frame. The SAPI allows 64 service access points to be specified, where bit 3 of the address field octet containing the SAPI is the least significant binary digit and bit 8 is the most significant. SAPI values are 0x14 and 0x15 for performance report message and path or test signal identification message respectively.

3.8.11 Terminal Endpoint Identifier (TEI)

The TEI sub-field allows 128 values where bit 2 of the address field octet containing the TEI is the least significant binary digit and bit 8 is the most significant binary digit. The TEI sub-field bit pattern 111 1111 (=127) is defined as the group TEI. The group TEI is assigned permanently to the broadcast data link connection associated with the addressed Service Access Point (SAP). TEI values other than 127 are used for the point-to-point data link connections associated with the addressed SAP. Non-automatic TEI values (0-63) are selected by the user, and their allocation is the responsibility of the user. The network automatically selects and allocates TEI values (64-126).

3.8.12 Control Field

The control field identifies the type of frame which will be either a command or response. The control field shall consist of one or two octets. Three types of control field formats are specified: 2-octet numbered information transfer (I format), 2-octet supervisory functions (S format), and single-octet unnumbered information transfers and control functions (U format). The control field for T1/E1 message is categorized as a single-octet unacknowledged information transfer having the value 0x03.

3.8.13 Frame Check Sequence (FCS) Field

The source of either the performance report or an identification message shall generate the frame check sequence. The FCS field shall be a 16-bit sequence. It shall be the ones complement of the sum (modulo 2) of:

- The remainder of xk (x15 + x14 + x13 + x12 + x11 + x10 + x9 + x8 + x7 + x6 + x5 + x4 + x3 + x2 + x + 1) divided (modulo 2) by the generator polynomial x16 + x12 + x5 + 1, where k is the number of bits in the frame existing between, but not including, the final bit of the opening flag and the first bit of the FCS, excluding bits inserted for transparency, and
- The remainder of the division (modulo 2) by the generator polynomial x16 + x12 + x5 + 1, of the product of x16 by the content of the frame existing between, but not including, the final bit of the opening flag and the first bit of the FCS, excluding bits inserted for transparency.

As a typical implementation at the transmitter, the initial content of the register of the device computing the remainder of the division is preset to all 1s and is then modified by division by the generator polynomial on the address, control and information fields; the ones complement of the resulting remainder is transmitted as the 16-bit FCS.

As a typical implementation at the receiver, the initial content of the register of the device computing the remainder is preset to all 1s. The final remainder, after multiplication by x16 and then division (modulo 2) by the generator polynomial x16 + x12 + x5 + 1 of the serial incoming protected bits and the FCS, will be 0001110100001111 (x15 through x0, respectively) in the absence of transmission errors.

3.8.14 Transparency (Zero Stuffing)

A transmitting data link layer entity shall examine the frame content between the opening and closing flag sequences, (address, control, information and FCS field) and shall insert a 0 bit after all sequences of five contiguous 1 bits (including the last five bits of the FCS) to ensure that an IDLE flag or an Abort sequence is not simulated within the frame. A receiving data link layer entity shall examine the frame contents between the opening and closing flag sequences and shall discard any 0 bit which directly follows five contiguous 1 bits.

3.9 Transmit SLC®96 Data link Controller

The SLC®96 T1 format is invented by AT&T and is used between the Digital Switch and a SLC®96 formatted remote terminal. The purpose of the SLC®96 product is to provide standard telephone service or Plain Old Telephone Service (POTS) in areas of high subscriber density but back-haul the traffic over T1 facilities.

To support the SLC®96 formatted remote terminal equipment, which is likely in an underground location, the T1 framer must:

- Indicate equipment failures of the equipment to maintenance personal
- Indicate failures of the POTS lines
- Test the POTS lines
- Provide redundancy on the T1s

The SLC®96 framing format is a D4 Super-frame (SF) format with specialized data link information bits. These data link information bits take the position of the Super-frame Alignment (Fs) bit positions. These bits consist of the following.

- Concentrator bits (C, bit position 1 to 11)
- First Spoiler bits (FS, bit position 12 to 14)
- Maintenance bits (M, bit position 15 to 17)
- Alarm bits (A, bit position 18 to 19)
- Protection Line Switch bits (S, bit position 20 to 23)
- Second Spoiler bit (SS, bit position 24)
- Resynchronization pattern (000111000111)

In SLC®96 mode, a six 6-bit datalink message will generate a one 9-ms frame of the SLC®96 message format. The format of the datalink message is given in BELLCORE TR-TSY-000008. When SLC®96 mode is enabled, the Fs bit is replaced by the data link message read from memory at the beginning of each D4 super-frame. The XRT86VL3x allocates two 6-byte buffers to provide the SLC®96 Data Link Controller an alternating access mechanism for information transmission. The bit ordering and usage is shown in the following table; and the LSB is sent first. Note that these registers are memory-based storage and they need to be initialized.

TABLE 1: BIT ORDERING AND USAGE

BYTE	5	4	3	2	1	0
1	0	1	1	1	0	0
2	C1	1	1	1	0	0
3	C7	C6	C5	C4	C3	C2
4	1	0	C11	C10	C9	C8
5	A2	A1	M3	M2	M1	0
6	0	1	S4	S3	S2	S1

Each register is read out of memory once every six SF super-frames. The memory holding these registers owns a shared memory structure that is used by multiple devices. These include DS1 transmit module, DS1 receive module, Transmit LAPD Controller, Transmit SLC®96 Data Link controller, Bit-Oriented Signaling Processor, Receive LAPD Controller, Receive SLC®96 Data Link Controller, Receive Bit-Oriented Signaling Processor and microprocessor interface module.

3.10 D/E Time Slot Transmit HDLC Controller Block V5.1 or V5.2 Interface

V5.2 protocol specifies a provision for transmitting simultaneous LAPD messages. Since only one message can be sent through the datalink bits at one time, an alternative path for communication is offered within the framer block. This alternative path is known as D or E channel which can be transmitted through one or more of the DS-0 time slots. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations. A range of time slots can be dedicated to HDLC1, while a different range of time slots can be dedicated to HDLC2 to support V5.2. In addition, HDLC3 can be used to transmit a third LAPD message if desired. The HDLC controllers are implemented in the same manner as the datalink described above with the exception of the data link source select bits.

3.11 Automatic Performance Report (APR)

The APR feature allows the system to transmit PMON status within a LAPD Framing format A at one second intervals or within a single shot report. The data octets 5 through 12 within the LAPD frame are replaced with the PMON status for the previous one second interval.

TABLE 2: FRAMING FORMAT FOR PMON STATUS INSERTED WITHIN LAPD BY INITIATING APR

Octet Number	8	7	6	5	4	3	2	1	Time (s)
1	Flag = 01111110								
2	SAPI = 001110						CR	EA=0	
3	TEI = 0000000							EA=1	
4	Control = 00000011 = Unacknowledged Frame								
5	G3	LV	G4	U1	U2	G5	SL	G6	T_0
6	FE	SE	LB	G1	R	G2	Nm	Ni	
7	G3	LV	G4	U1	U2	G5	SL	G6	T_0 - 1
8	FE	SE	LB	G1	R	G2	Nm	Ni	
9	G3	LV	G4	U1	U2	G5	SL	G6	T_0 - 2
10	FE	SE	LB	G1	R	G2	Nm	Ni	
11	G3	LV	G4	U1	U2	G5	SL	G6	T_0 - 3
12	FE	SE	LB	G1	R	G2	Nm	Ni	
13	FCS								
14	FCS								
15	Flag = 01111110								

NOTE: *The right most bit (bit 1) is transmitted first for all fields except for the two bytes of the FCS that are transmitted left most bit (bit 8) first.*

3.11.1 Bit Value Interpretation

G1 = 1 if number of CRC error events is equal to 1

G2 = 1 if number of CRC error events is greater than 1 or equal to 5

G3 = 1 if number of CRC error events is greater than 5 or equal to 10

G4 = 1 if number of CRC error events is greater than 10 or equal to 100

G5 = 1 if number of CRC error events is greater than 100 or equal to 319

G6 = 1 if number of CRC error events is equal to 320

SE = 1 if a severely errored framing event occurs (FE shall be 0)

FE = 1 if a framing synchronization bit error event occurs (SE shall be 0)

LV = 1 if a line code violation event occurs

SL = 1 if slip event within the slip buffer occurs

LB = 1 if payload loopback is activated

U1 = If SPRM is used, this bit is controlled by register 0xN142 (default = 0)

U2 = If SPRM is used, this bit is controlled by register 0xN142 (default = 0)

R = If SPRM is used, these bits are controlled by register 0xN142 (default = 0000)

NmNi = One second report module 4 count

4.0 OVERHEAD INTERFACE BLOCK

The XRT86VL3x has the ability to extract or insert DS1 data link information from or into the following:

- Facility Data Link (FDL) bits in ESF framing format mode
- Signaling Framing (Fs) bits in SLC®96 and N framing format mode
- Remote Signaling (R) bits in T1DM framing format mode

The source and destination of these inserted and extracted data link bits would be from either the internal HDLC Controller or the external device accessible through DS1 Overhead Interface Block. The operation of the Transmit Overhead Input Interface Block and the Receive Overhead Output Interface Block will be discussed separately.

4.1 DS1 Transmit Overhead Input Interface Block

4.1.1 Description of the DS1 Transmit Overhead Input Interface Block

The DS1 Transmit Overhead Input Interface Block will allow an external device to be the provider of the Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in the SLC96 and N framing format mode and Remote Signaling (R) bit in T1DM framing format mode. This interface provides interface signals and required interface timing to shift in proper data link information at proper time.

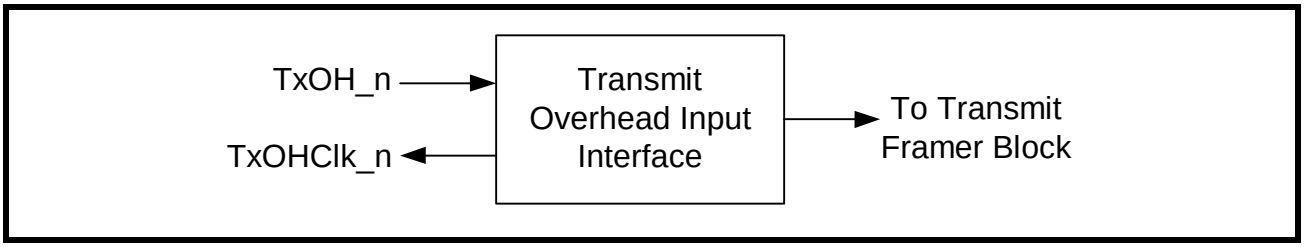
The Transmit Overhead Input Interface for a given Framer consists of two signals.

- TxOHClk_n: The Transmit Overhead Input Interface Clock Output signal
- TxOH_n: The Transmit Overhead Input Interface Input signal.

The Transmit Overhead Input Interface Clock Output pin (TxOHCLK_n) generates a rising clock edge for each data link bit position according to configuration of the framer. The Data Link equipment interfaced to the Transmit Overhead Input Interface block should update the data link bits on the TxOH_n line upon detection of the rising edge of TxOHClk_n. The Transmit Overhead Input Interface block will sample and latch the data link bits on the TxOH_n line on the falling edge of TxOHClk_n. The data link bits will be included and transmitted via the outgoing DS1 frames.

The figure below shows block diagram of the DS1 Transmit Overhead Input Interface of XRT86VL3x.

FIGURE 34. BLOCK DIAGRAM OF THE DS1 TRANSMIT OVERHEAD INPUT INTERFACE OF THE XRT86VL3X



4.1.2 Configure the DS1 Transmit Overhead Input Interface module as source of the Facility Data Link (FDL) bits in ESF framing format mode

The FDL bits in ESF framing format mode can be inserted from:

- DS1 Transmit Overhead Input Interface Block
- DS1 Transmit HDLC Controller
- DS1 Transmit Serial Input Interface.

The Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR) controls the insertion of data link bits into the FDL bits in ESF framing format mode. The table below shows configuration of the Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR).

TRANSMIT DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Data Link Source Select	R/W	00 - The Facility Data Link bits are inserted into the framer through either the LAPD controller or the SLC®96 buffer. 01 - The Facility Data Link bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 10 - The Facility Data Link bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The Facility Data Link bits are forced to one by the framer.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 10, the Transmit Overhead Input Interface Block becomes input source of the FDL bits.

The XRT86VL3x allows the user to select bandwidth of the Facility Data Link Channel in ESF framing format mode. The FDL can be either a 4KHz or 2KHz data link channel. The Transmit Data Link Bandwidth Select bits of the Transmit Data Link Select Register (TDLSR) determine the bandwidth of FDL channel in ESF framing format mode.

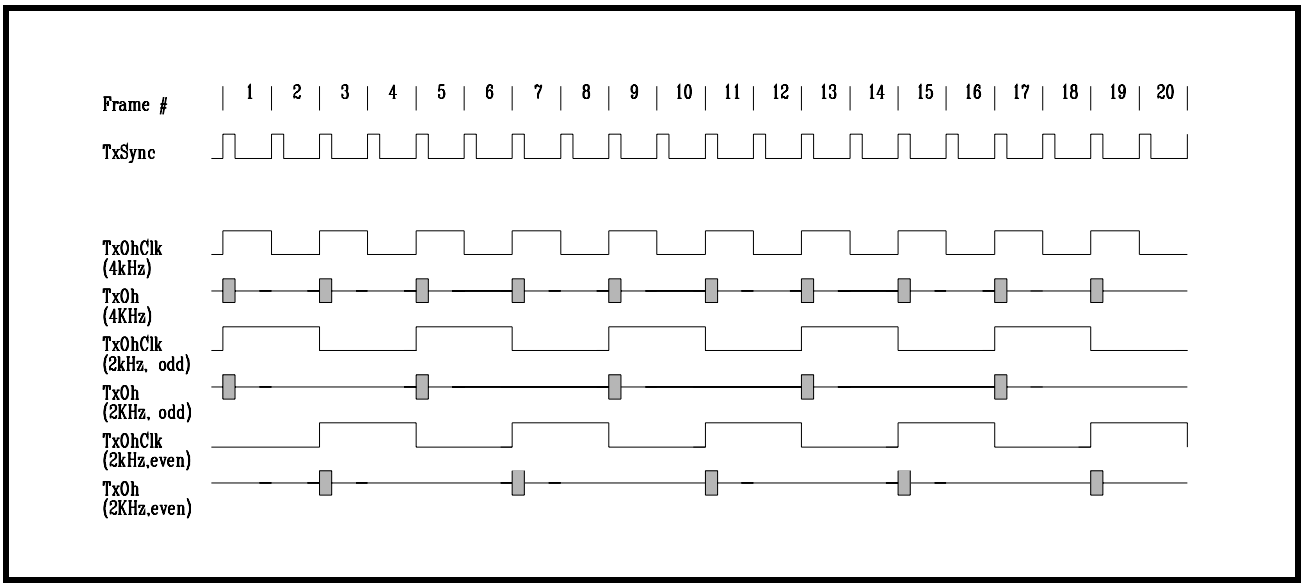
The table below shows configuration of the Transmit Data Link Bandwidth Select bits of the Transmit Data Link Select Register (TDLSR).)

TRANSMIT DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Transmit Data Link Bandwidth Select	R/W	00 - The Facility Data Link is a 4KHz channel. All available FDL bits (first bit of every other frame) are used as data link bits. 01 - The Facility Data Link is a 2KHz channel. Only the odd FDL bits (first bit of frame 1, 5, 9…) are used as data link bits. 10 - The Facility Data Link is a 2KHz channel. Only the even FDL bits (first bit of frame 3, 7, 11…) are used as data link bits.

Figure 35 below shows the timing diagram of the input and output signals associated with the DS1 Transmit Overhead Input Interface module in ESF framing format mode.

FIGURE 35. DS1 TRANSMIT OVERHEAD INPUT INTERFACE TIMING IN ESF FRAMING FORMAT MODE



4.1.3 Configure the DS1 Transmit Overhead Input Interface module as source of the Signaling Framing (Fs) bits in N or SLC®96 framing format mode

The Fs bits in SLC®96 and N framing format mode can be inserted from:

- DS1 Transmit Overhead Input Interface Block
- DS1 Transmit HDLC Controller
- DS1 Transmit Serial Input Interface.

The Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR) controls the insertion of data link bits into the Fs bits in N or SLC®96 framing format mode. The table below shows configuration of the Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR).

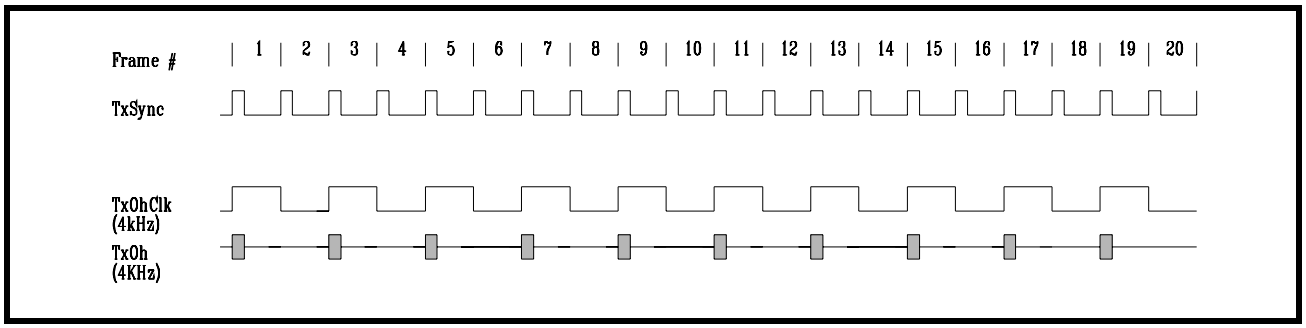
TRANSMIT DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Data Link Source Select	R/W	00 - The Signaling Framing bits are inserted into the framer through either the LAPD controller or the SLC®96 buffer. 01 - The Signaling Framing bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 10 - The Signaling Framing bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The Signaling Framing bits are forced to one by the framer.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 10, the Transmit Overhead Input Interface Block becomes input source of the Fs bits.

Figure 36 below shows the timing diagram of the input and output signals associated with the DS1 Transmit Overhead Input Interface module in N or SLC®96 framing format mode.

FIGURE 36. DS1 TRANSMIT OVERHEAD INPUT TIMING IN N OR SLC®96 FRAMING FORMAT MODE



4.1.4 Configure the DS1 Transmit Overhead Input Interface module as source of the Remote Signaling (R) bits in T1DM framing format mode

The R bits in T1DM framing format mode can be inserted from:

- DS1 Transmit Overhead Input Interface Block
- DS1 Transmit HDLC Controller
- DS1 Transmit Serial Input Interface.

The Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR) controls the insertion of data link bits into the R bits in T1DM framing format mode. The table below shows configuration of the Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR).

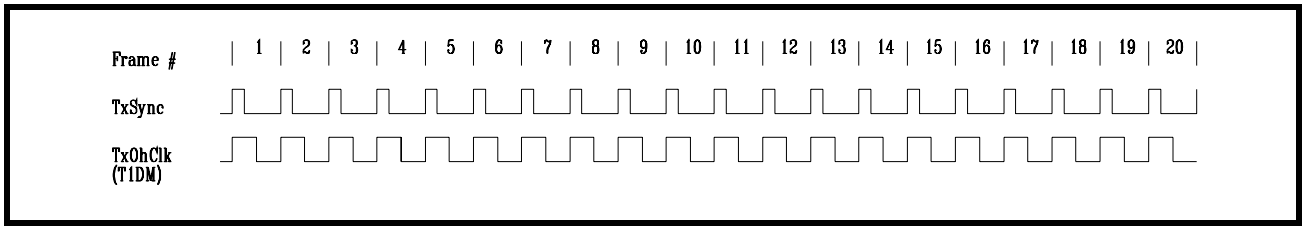
TRANSMIT DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Data Link Source Select	R/W	00 - The Remote Signaling bits are inserted into the framer through either the LAPD controller or the SLC®96 buffer. 01 - The Remote Signaling bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 10 - The Remote Signaling bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The Remote Signaling bits are forced to one by the framer.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 10, the Transmit Overhead Input Interface Block becomes input source of the R bits. Since R bit presents in Timeslot 24 of every T1DM frame, therefore, bandwidth of T1DM data link channel is 8KHz.

Figure 37 below shows the timing diagram of the input and output signals associated with the DS1 Transmit Overhead Input Interface module in T1DM framing format mode.

FIGURE 37. DS1 TRANSMIT OVERHEAD INPUT INTERFACE MODULE IN T1DM FRAMING FORMAT MODE



4.2 DS1 Receive Overhead Output Interface Block

4.2.1 Description of the DS1 Receive Overhead Output Interface Block

The DS1 Receive Overhead Output Interface Block allows an external device to be the consumer of the Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in the SLC96 and N framing format mode and Remote Signaling (R) bit in T1DM framing format mode This interface provides interface signals and required interface timing to shift out proper data link information at proper time.

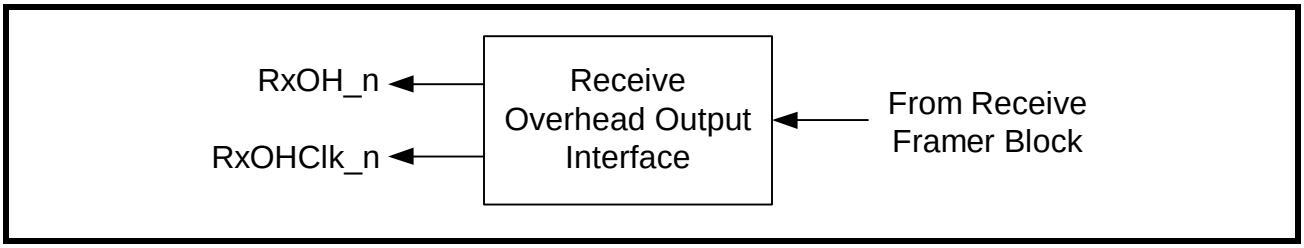
The Receive Overhead Output Interface for a given Framer consists of two signals.

- RxOHClk_n: The Receive Overhead Output Interface Clock Output signal
- RxOH_n: The Receive Overhead Output Interface Output signal.

The Receive Overhead Output Interface Clock Output pin (RxOHCLK_n) generates a rising clock edge for each data link bit position according to configuration of the framer. The data link bits extracted from the incoming T1 frames are outputted from the Receive Overhead Output Interface Output pin (RxOH_n) at the rising edge of RxOHClk_n. The Data Link equipment should sample and latch the data link bits at the falling edge of RxOHClk_n.

The figure below shows block diagram of the Receive Overhead Output Interface of XRT86VL3x.

FIGURE 38. BLOCK DIAGRAM OF THE DS1 RECEIVE OVERHEAD OUTPUT INTERFACE OF XRT86VL3X



4.2.2 Configure the DS1 Receive Overhead Output Interface module as destination of the Facility Data Link (FDL) bits in ESF framing format mode

The FDL bits in ESF framing format mode can be extracted to:

- DS1 Receive Overhead Output Interface Block
- DS1 Receive HDLC Controller
- DS1 Receive Serial Output Interface.

The Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR) controls the extraction of FDL bits in ESF framing format mode. The table below shows configuration of the Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR).

RECEIVE DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Receive Data Link Destination Select	R/W	00 - The extracted Facility Data Link bits are stored in either the LAPD controller or the SLC®96 buffer. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 01 - The extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 10 - The extracted Facility Data Link bits are outputted from the framer through the Receive Overhead Output Interface via the RxOH_n pins. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 11 - The Facility Data Link bits are forced to one by the framer.

If the Receive Data Link Source Select bits of the Receive Data Link Select Register are set to 10, the Receive Overhead Output Interface Block becomes Output source of the FDL bits.

The XRT86VL3x allows the user to select bandwidth of the Facility Data Link Channel in ESF framing format mode. The FDL can be either a 4KHz or 2KHz data link channel. The Receive Data Link Bandwidth Select bits of the Receive Data Link Select Register (RDLSR) determine the bandwidth of FDL channel in ESF framing format mode.

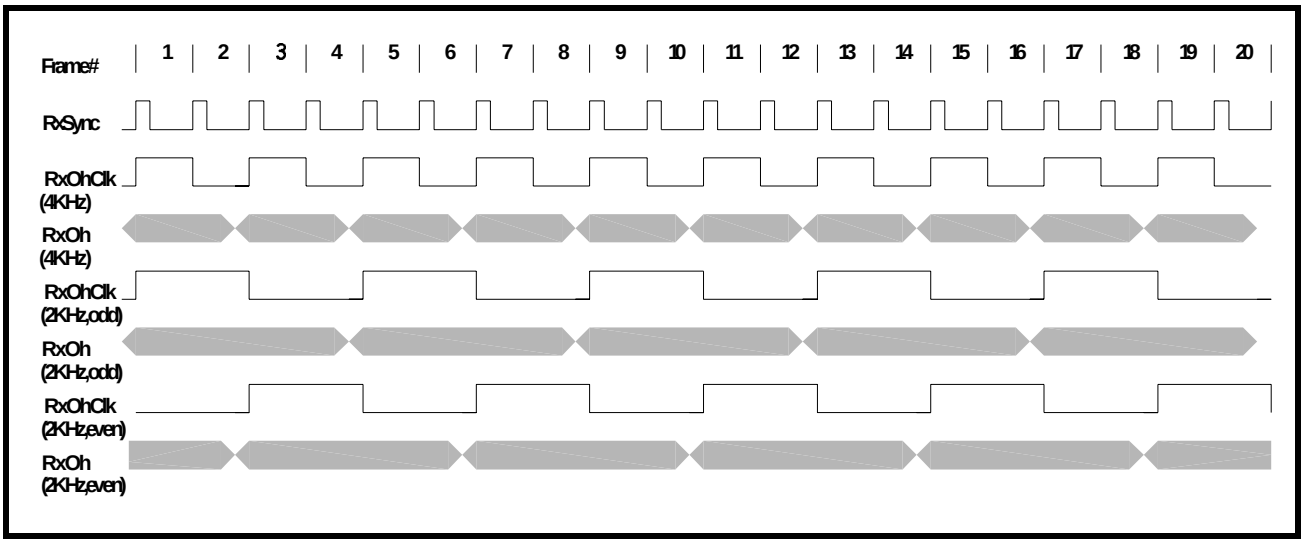
The table below shows configuration of the Receive Data Link Bandwidth Select bits of the Receive Data Link Select Register (TDLSR).

RECEIVE DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Receive Data Link Bandwidth Select	R/W	00 - The Facility Data Link is a 4KHz channel. All available FDL bits (first bit of every other frame) are used as data link bits. 01 - The Facility Data Link is a 2KHz channel. Only the odd FDL bits (first bit of frame 1, 5, 9…) are used as data link bits. 10 - The Facility Data Link is a 2KHz channel. Only the even FDL bits (first bit of frame 3, 7, 11…) are used as data link bits.

Figure 39 below shows the timing diagram of the Output and output signals associated with the DS1 Receive Overhead Output Interface module in ESF framing format mode.

FIGURE 39. DS1 RECEIVE OVERHEAD OUTPUT INTERFACE MODULE IN ESF FRAMING FORMAT MODE



4.2.3 Configure the DS1 Receive Overhead Output Interface module as destination of the Signaling Framing (Fs) bits in N or SLC®96 framing format mode

The Fs bits in SLC®96 and N framing format mode can be extracted to:

- DS1 Receive Overhead Output Interface Block
- DS1 Receive HDLC Controller
- DS1 Receive Serial Output Interface.

The Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR) controls the destination of Fs bits in N or SLC®96 framing format mode. The table below shows configuration of the Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR).

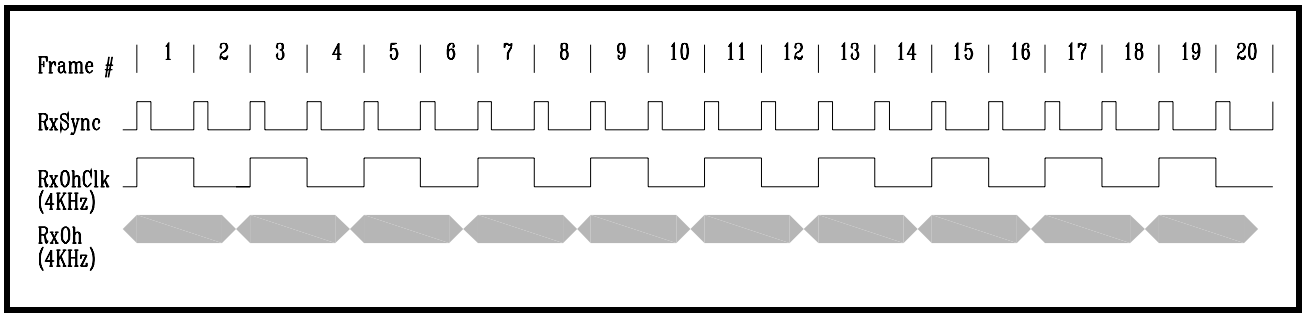
RECEIVE DATA LINK SELECT REGISTER (TDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Receive Data Link Source Select	R/W	00 - The extracted Facility Data Link bits are stored in either the LAPD controller or the SLC®96 buffer. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 01 - The extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 10 - The extracted Facility Data Link bits are outputted from the framer through the Receive Overhead Output Interface via the RxOH_n pins. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 11 - The Facility Data Link bits are forced to one by the framer.

If the Receive Data Link Source Select bits of the Receive Data Link Select Register are set to 10, the Receive Overhead Output Interface Block outputs Fs bits extracted from the incoming T1 data stream.

Figure 40 below shows the timing diagram of the output signals associated with the DS1 Receive Overhead Output Interface module in N or SLC®96 framing format mode.

FIGURE 40. DS1 RECEIVE OVERHEAD OUTPUT INTERFACE TIMING IN N OR SLC®96 FRAMING FORMAT MODE



4.2.4 Configure the DS1 Receive Overhead Output Interface module as destination of the Remote Signaling (R) bits in T1DM framing format mode

The R bits in T1DM framing format mode can be extracted to:

- DS1 Receive Overhead Output Interface Block
- DS1 Receive HDLC Controller
- DS1 Receive Serial Output Interface.

The Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR) controls the destination of R bits in T1DM framing format mode. The table below shows configuration of the Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR).

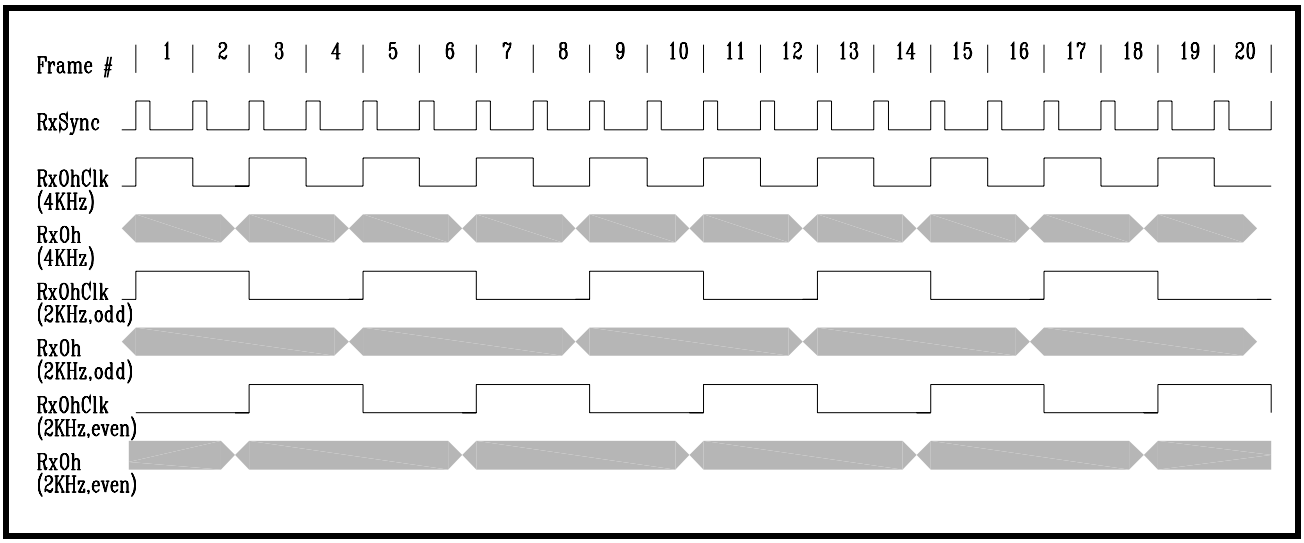
RECEIVE DATA LINK SELECT REGISTER (RDLSR) (ADDRESS = 0XN10AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Receive Data Link Source Select	R/W	00 - The extracted Facility Data Link bits are stored in either the LAPD controller or the SLC®96 buffer. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 01 - The extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 10 - The extracted Facility Data Link bits are outputted from the framer through the Receive Overhead Output Interface via the RxOH_n pins. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 11 - The Facility Data Link bits are forced to one by the framer.

If the Receive Data Link Source Select bits of the Receive Data Link Select Register are set to 10, the Receive Overhead Output Interface Block outputs the R bits extracted from the incoming T1 data stream. Since R bit presents in Timeslot 24 of every T1DM frame, therefore, bandwidth of T1DM data link channel is 8KHz.

Figure 41 below shows the timing diagram of the output signals associated with the DS1 Receive Overhead Output Interface module in T1DM framing format mode.

FIGURE 41. DS1 RECEIVE OVERHEAD OUTPUT INTERFACE TIMING IN T1DM FRAMING FORMAT MODE



4.3 E1 Overhead Interface Block

The XRT86VL3x has the ability to extract or insert E1 data link information from or into the E1 National bit sequence. The source and destination of these inserted and extracted data link bits would be from either the internal HDLC Controller or the external device accessible through E1 Overhead Interface Block. The operation of the Transmit Overhead Input Interface Block and the Receive Overhead Output Interface Block will be discussed separately.

4.4 E1 Transmit Overhead Input Interface Block

4.4.1 Description of the E1 Transmit Overhead Input Interface Block

The E1 Transmit Overhead Input Interface Block will allow an external device to be the provider of the E1 National bit sequence. This interface provides interface signals and required interface timing to shift in proper data link information at proper time.

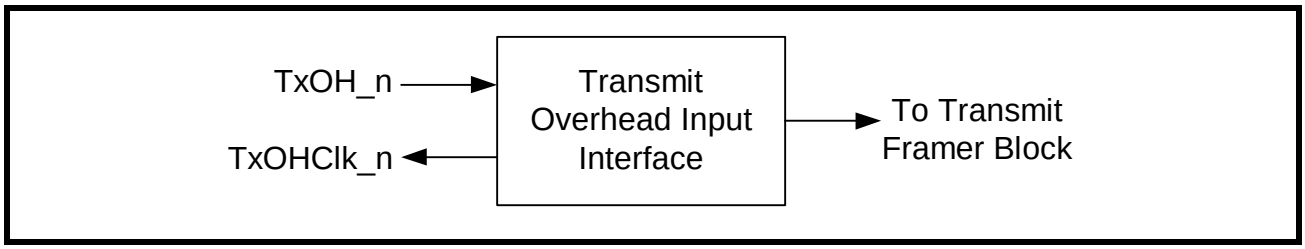
The Transmit Overhead Input Interface for a given Framer consists of two signals.

- TxOHClk_n: The Transmit Overhead Input Interface Clock Output signal
- TxOH_n: The Transmit Overhead Input Interface Input signal.

The Transmit Overhead Input Interface Clock Output pin (TxOHCLK_n) generates a rising clock edge for each National bit that is configured to carry Data Link information according to setting of the framer. The Data Link equipment interfaced to the Transmit Overhead Input Interface should update the data link bits on the TxOH_n line upon detection of the rising edge of TxOHClk_n. The Transmit Overhead Input Interface block will sample and latch the data link bits on the TxOH_n line on the falling edge of TxOHClk_n. The data link bits will be included in and transmitted via the outgoing E1 frames.

The figure below shows block diagram of the DS1 Transmit Overhead Input Interface of XRT86VL3x.

FIGURE 42. BLOCK DIAGRAM OF THE E1 TRANSMIT OVERHEAD INPUT INTERFACE OF XRT86VL3X



4.4.2 Configure the E1 Transmit Overhead Input Interface module as source of the National Bit Sequence in E1 framing format mode

The National Bit Sequence in E1 framing format mode can be inserted from:

- E1 Transmit Overhead Input Interface Block
- E1 Transmit HDLC Controller
- E1 Transmit Serial Input Interface

The purpose of the Transmit Overhead Input Interface is to permit Data Link equipment direct access to the Sa4 through Sa8 National bits that are to be transported via the outbound frames. The Transmit Data Link Source Select [1:0] bits, within the Synchronization MUX Register (SMR) determine source of the Sa4 through Sa8 National bits to be inserted into the outgoing E1 frames.

The table below shows configuration of the Transmit Data Link Source Select [1:0] bits of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (ADDRESS = 0XN109H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit Data Link Source Select [1:0]	R/W	00 - The Sa4 through Sa8 National bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 01 - The Sa4 through Sa8 National bits are inserted into the framer through the Transmit LAPD Controller. 10 - The Sa4 through Sa8 National bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The Sa4 through Sa8 National bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 10, the Transmit Overhead Input Interface Block becomes input source of the FDL bits.

The XRT86VL3x allows the user to decide on the following:

- How many of the National Bits will be used to carry the Data Link information bits
- Which of these National Bits will be used to carry the Data Link information bits.

The Transmit Sa Data Link Select bits of the Transmit Signaling and Data Link Select Register (TSDLSR) determine which ones of the National bits are configured as Data Link bits in E1 framing format mode. Depending upon the configuration of the Transmit Signaling and Data Link Select Register, either of the following cases may exists:

- None of the National bits are used to transport the Data Link information bits (That is, data link channel of XRT86VL3x is inactive).

- Any combination of between 1 and all 5 of the National bits can be selected to transport the Data Link information bits.

The table below shows configuration of the Transmit Sa Data Link Select bits of the Transmit Signaling and Data Link Select Register (TSDLSR).

TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) (ADDRESS = 0XN10AH)

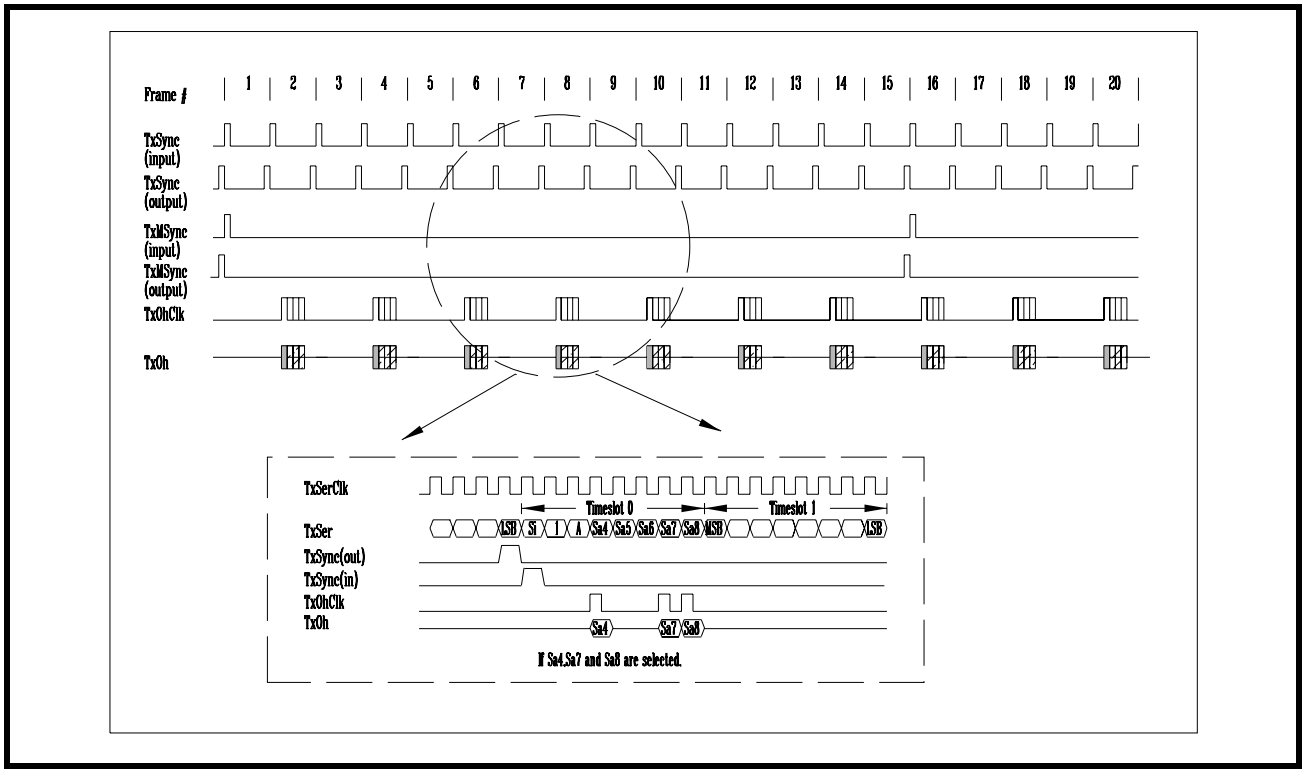
BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Transmit Sa8 Data Link Select	R/W	0 - Source of the Sa8 Nation bit is not from the data link interface. 1 - Source the Sa8 National bit from the data link interface.
6	Transmit Sa7 Data Link Select	R/W	0 - Source of the Sa7 Nation bit is not from the data link interface. 1 - Source the Sa7 National bit from the data link interface.
5	Transmit Sa6 Data Link Select	R/W	0 - Source of the Sa6 Nation bit is not from the data link interface. 1 - Source the Sa6 National bit from the data link interface.
4	Transmit Sa5 Data Link Select	R/W	0 - Source of the Sa5 Nation bit is not from the data link interface. 1 - Source the Sa5 National bit from the data link interface.
3	Transmit Sa4 Data Link Select	R/W	0 - Source of the Sa4 Nation bit is not from the data link interface. 1 - Source the Sa4 National bit from the data link interface.

For every Sa bit that is selected to carry Data Link information, the Transmit Overhead Input Interface will supply a clock pulse, via the TxOHClk_n output pin, such that:

- The Data Link equipment interfaced to the Transmit Overhead Input Interface should update the data on the TxOH_n line upon detection of the rising edge of TxOHClk_n.
- The Transmit Overhead Input Interface will sample and latch the data on the TxOH_n line on the falling edge of TxOHClk_n.

Figure 43 below shows the timing diagram of the input and output signals associated with the E1 Transmit Overhead Input Interface module in E1 framing format mode.

FIGURE 43. E1 TRANSMIT OVERHEAD INPUT INTERFACE TIMING



4.5 E1 Receive Overhead Interface

4.5.1 Description of the E1 Receive Overhead Output Interface Block

The E1 Receive Overhead Output Interface Block will allow an external device to be the consumer of the E1 National bit sequence. This interface provides interface signals and required interface timing to shift out proper data link information at proper time.

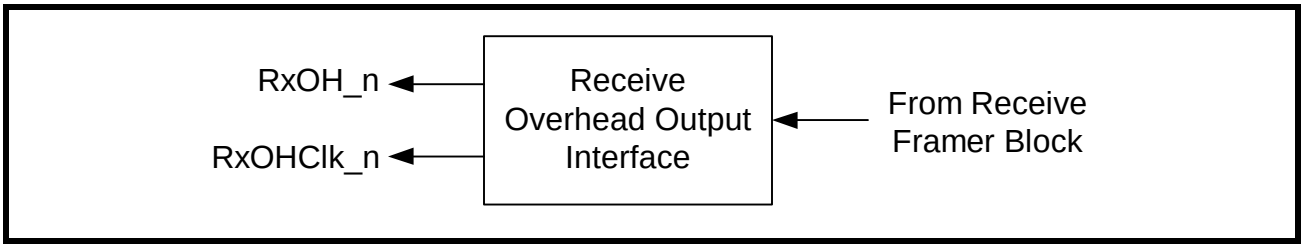
The Receive Overhead Output Interface for a given Framer consists of two signals.

- RxOHClk_n: The Receive Overhead Output Interface Clock Output signal
- RxOH_n: The Receive Overhead Output Interface Output signal.

The Receive Overhead Output Interface Clock Output pin (RxOHCLK_n) generates a rising clock edge for each National bit that is configured to carry Data Link information according to setting of the framer. The data link bits extracted from the incoming E1 frames are outputted from the Receive Overhead Output Interface Output pin (RxOH_n) before the rising edge of RxOHClk_n. The Data Link equipment should sample and latch the data link bits at the rising edge of RxOHClk_n.

The figure below shows block diagram of the Receive Overhead Output Interface of XRT86VL3x.

FIGURE 44. BLOCK DIAGRAM OF THE E1 RECEIVE OVERHEAD OUTPUT INTERFACE OF XRT86VL3X



4.5.2 Configure the E1 Receive Overhead Output Interface module as source of the National Bit Sequence in E1 framing format mode

The National Bit Sequence in E1 framing format mode can be extracted and directed to:

- E1 Receive Overhead Output Interface Block
- E1 Receive HDLC Controller
- E1 Receive Serial Output Interface

The purpose of the Receive Overhead Output Interface is to permit Data Link equipment to have direct access to the Sa4 through Sa8 National bits that are extracted from the incoming E1 frames. Independent of the availability of the E1 Receive HDLC Controller module, the XRT86VL3x always output the received National bits through the Receive Overhead Output Interface block.

The XRT86VL3x allows the user to decide on the following:

- How many of the National Bits is used to carry the Data Link information bits
- Which of these National Bits is used to carry the Data Link information bits.

The Receive Sa Data Link Select bits of the Receive Signaling and Data Link Select Register (TSDLSR) determine which ones of the National bits are configured as Data Link bits in E1 framing format mode. Depending upon the configuration of the Receive Signaling and Data Link Select Register, either of the following cases may exists:

- None of the received National bits are used to transport the Data Link information bits (That is, data link channel of XRT86VL3x is inactive).
- Any combination of between 1 and all 5 of the received National bits are used to transport the Data Link information bits.

The table below shows configuration of the Receive Sa Data Link Select bits of the Receive Signaling and Data Link Select Register (RSDLSR).

RECEIVE SIGNALING AND DATA LINK SELECT REGISTER (RSDLSR) (ADDRESS = 0XN10CH)

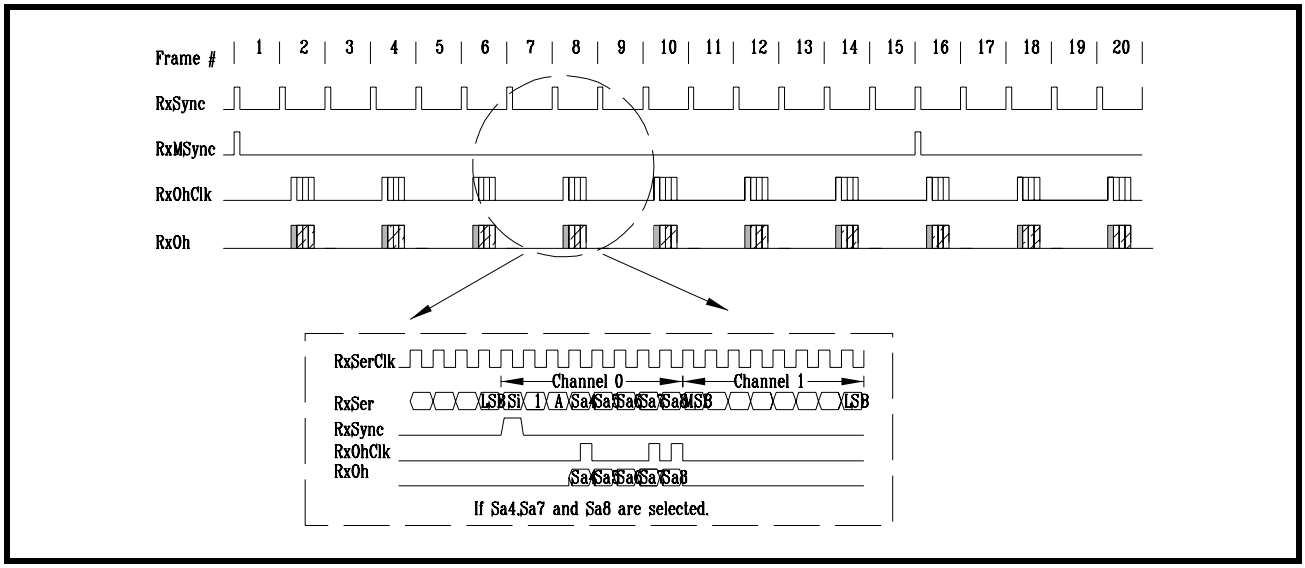
BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Sa8 Data Link Select	R/W	0 - The received Sa8 Nation bit is not extracted to the data link interface. 1 - The received Sa8 Nation bit is extracted to the data link interface.
6	Receive Sa7 Data Link Select	R/W	0 - The received Sa7 Nation bit is not extracted to the data link interface. 1 - The received Sa7 Nation bit is extracted to the data link interface.
5	Receive Sa6 Data Link Select	R/W	0 - The received Sa6 Nation bit is not extracted to the data link interface. 1 - The received Sa6 Nation bit is extracted to the data link interface.
4	Receive Sa5 Data Link Select	R/W	0 - The received Sa5 Nation bit is not extracted to the data link interface. 1 - The received Sa5 Nation bit is extracted to the data link interface.
3	Receive Sa4 Data Link Select	R/W	0 - The received Sa4 Nation bit is not extracted to the data link interface. 1 - The received Sa4 Nation bit is extracted to the data link interface.

For every received Sa bit that is determined to carry Data Link information, the Receive Overhead Output Interface will supply a clock pulse, via the RxOHClk_n output pin, such that:

- The Receive Overhead Output interface should update the data on the RxOH_n line before the rising edge of RxOHClk_n.
- The external Data Link equipment interfaced to the Receive Overhead Output Interface will sample and latch the data on the RxOH_n line on the rising edge of RxOHClk_n.

Figure 45 below shows the timing diagram of the output signals associated with the E1 Receive Overhead Output Interface module in E1 framing format mode.

FIGURE 45. E1 RECEIVE OVERHEAD OUTPUT INTERFACE TIMING



5.0 LIU TRANSMIT PATH

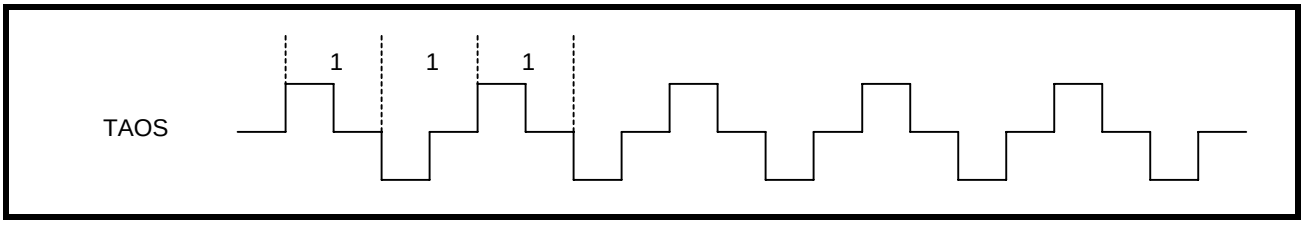
5.1 Transmit Diagnostic Features

In addition to TAOS, the XRT86VL3x offers multiple diagnostic features for analyzing network integrity such as ATAOS, Network Loop Code generation, and QRSS on a per channel basis by programming the appropriate registers. These diagnostic features take priority over the digital data provided by the Framer block. The transmitters will send the diagnostic code to the line and will be maintained in the digital loopback if selected.

5.1.1 TAOS (Transmit All Ones)

The XRT86VL3x has the ability to transmit all ones on a per channel basis by programming the appropriate channel register. This function takes priority over the digital data provided by the Framer block. For example: If a fixed "0011" pattern is provided by the Framer block and TAOS is enabled, the transmitter will output all ones. **Figure 46** is a diagram showing the all ones signal at TTIP and TRING.

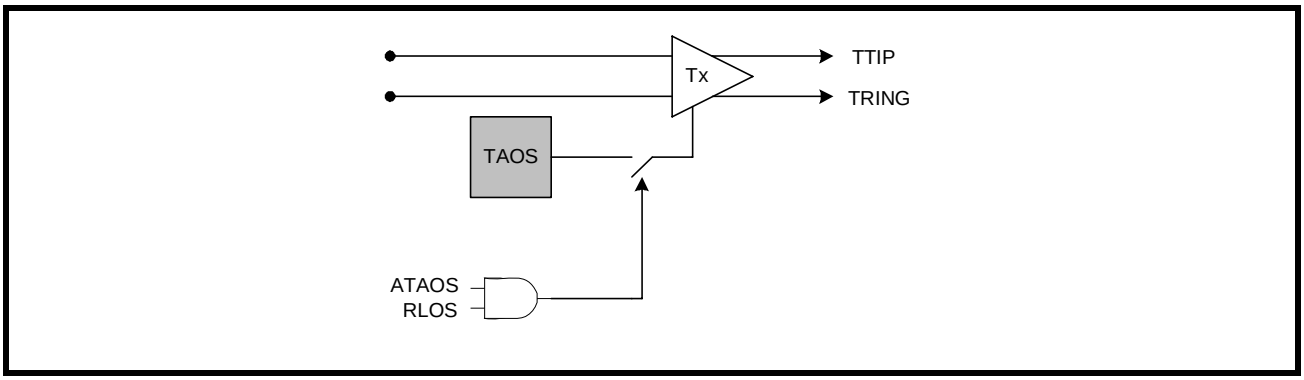
FIGURE 46. TAOS (TRANSMIT ALL ONES)



5.1.2 ATAOS (Automatic Transmit All Ones)

If ATAOS is selected by programming the appropriate global register, an AMI all ones signal will be transmitted for each channel that experiences an RLOS condition. If RLOS does not occur, the ATAOS will remain inactive until an RLOS on a given channel occurs. A simplified block diagram of the ATAOS function is shown in **Figure 47**.

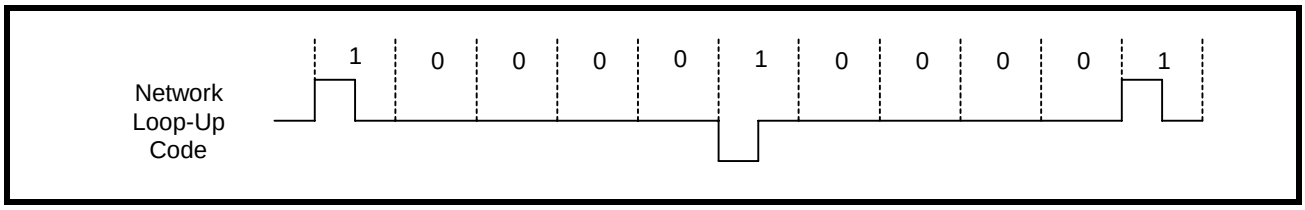
FIGURE 47. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION



5.1.3 Network Loop Up Code

By setting the LIU to generate a NLUC, the transmitters will send out a repeating "00001" pattern. The output waveform is shown in **Figure 48**.

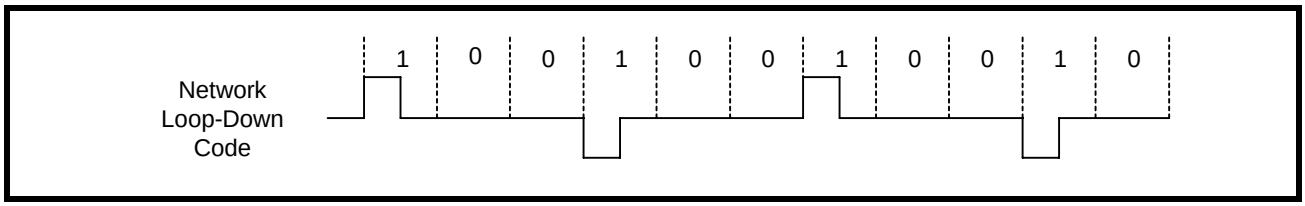
FIGURE 48. NETWORK LOOP UP CODE GENERATION



5.1.4 Network Loop Down Code

By setting the LIU to generate a NLDC, the transmitters will send out a repeating "001" pattern. The output waveform is shown in **Figure 49**.

FIGURE 49. NETWORK LOOP DOWN CODE GENERATION



5.1.5 QRSS Generation

The XRT86VL3x can transmit a QRSS random sequence to a remote location from TTIP/TRING. The polynomial is shown in **Table 3**.

TABLE 3: RANDOM BIT SEQUENCE POLYNOMIALS

RANDOM PATTERN	T1	E1
QRSS/PRBS	$2^{20} - 1$	$2^{15} - 1$

5.2 T1 Long Haul Line Build Out (LBO)

The long haul transmitter output pulses are generated using a 7-Bit internal DAC (6-Bits plus the MSB sign bit). The line build out can be set to -7.5dB, -15dB, or -22dB cable attenuation by programming the appropriate channel register. The long haul LBO consist of 32 discrete time segments extending over four consecutive periods of TCLK. As the LBO attenuation is increased, the pulse amplitude is reduced so that the waveform complies with ANSI T1.403 specifications. A long haul pulse with -7.5dB attenuation is shown in **Figure 50**, a pulse with -15dB attenuation is shown in **Figure 51**, and a pulse with -22.5dB attenuation is shown in **Figure 52**.

FIGURE 50. LONG HAUL LINE BUILD OUT WITH -7.5DB ATTENUATION

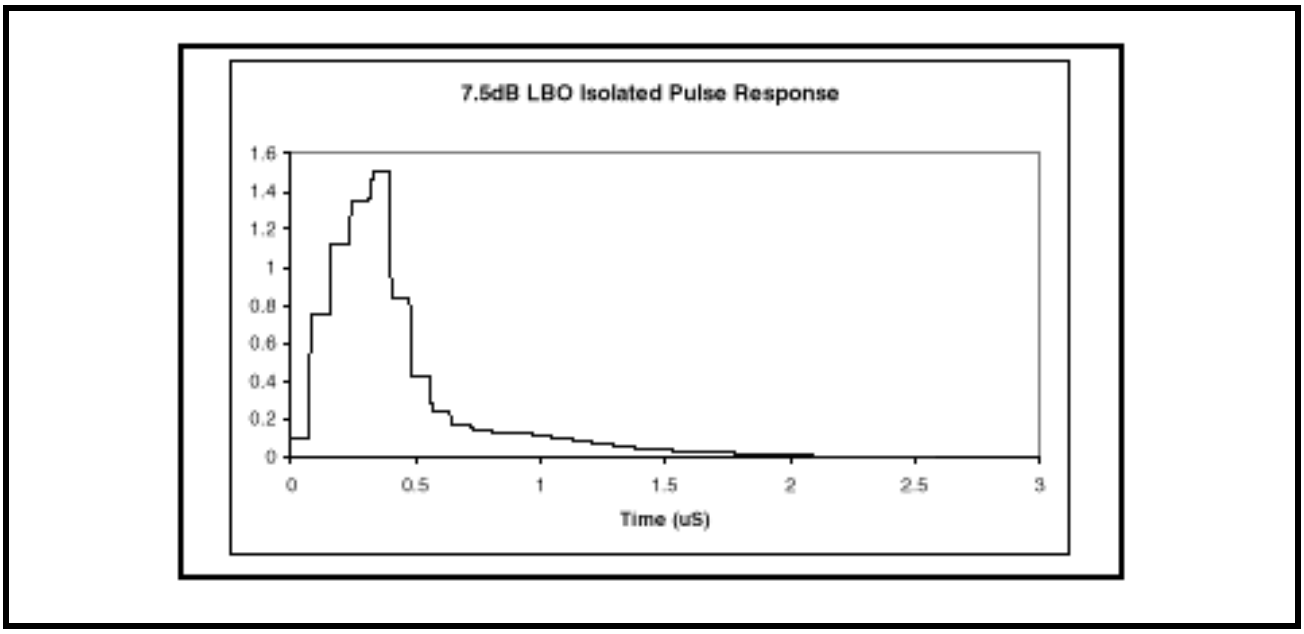


FIGURE 51. LONG HAUL LINE BUILD OUT WITH -15DB ATTENUATION

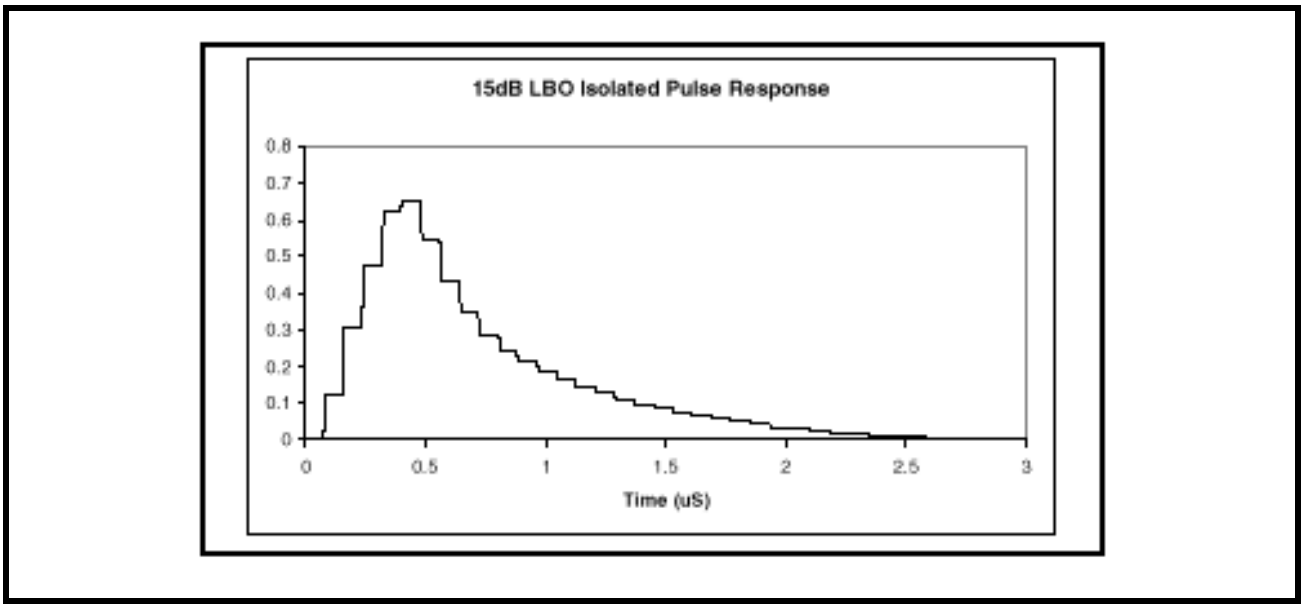
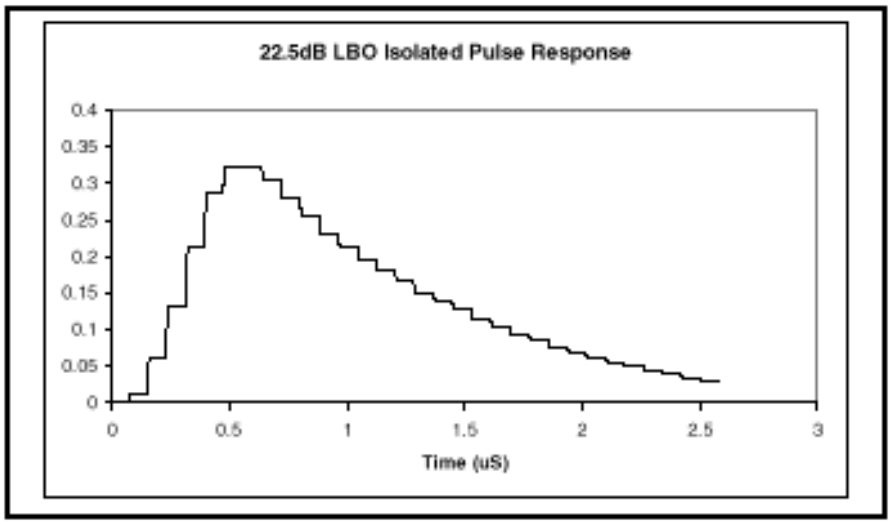


FIGURE 52. LONG HAUL LINE BUILD OUT WITH -22.5DB ATTENUATION



5.3 T1 Short Haul Line Build Out (LBO)

The short haul transmitter output pulses are generated using a 7-Bit internal DAC (6-Bit plus the MSB sign bit). The line build out can be set to interface to five different ranges of cable attenuation by programming the appropriate channel register. The pulse shape is divided into eight discrete time segments which are set to fixed values to comply with the pulse template. To program the eight segments individually to optimize a special line build out, see the arbitrary pulse section of this datasheet. The short haul LBO settings are shown in **Table 4**

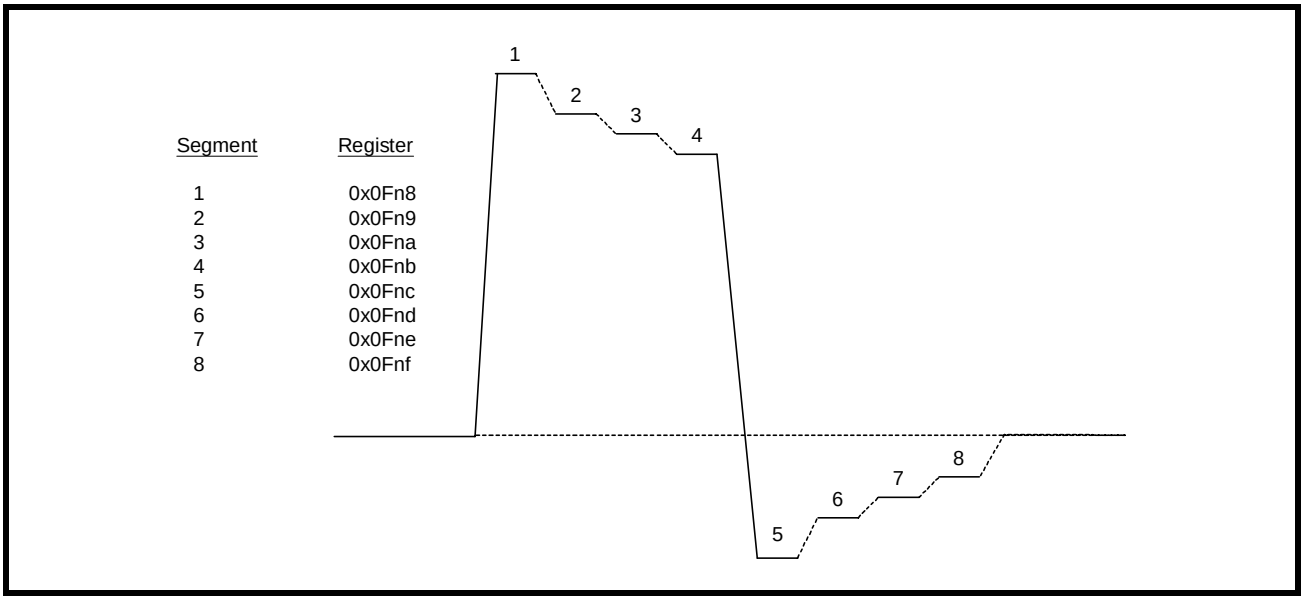
TABLE 4: SHORT HAUL LINE BUILD OUT

LBO SETTING EQC[4:0]	RANGE OF CABLE ATTENUATION
08h (01000)	0 - 133 Feet
09h (01001)	133 - 266 Feet
0Ah (01010)	266 - 399 Feet
0Bh (01011)	399 - 533 Feet
0Ch (01100)	533 - 655 Feet

5.3.1 Arbitrary Pulse Generator

The arbitrary pulse generator divides the pulse into eight individual segments. Each segment is set by a 7-Bit binary word by programming the appropriate channel register. This allows the system designer to set the overshoot, amplitude, and undershoot for a unique line build out. The MSB (bit 7) is a sign-bit. If the sign-bit is set to "0", the segment will move in a positive direction relative to a flat line (zero) condition. If this sign-bit is set to "1", the segment will move in a negative direction relative to a flat line condition. The resolution of the DAC is typically 60mV per LSB. Thus, writing 7-bit = 1111111 will clamp the output at either voltage rail corresponding to a maximum amplitude. A pulse with numbered segments is shown in **Figure 53**.

FIGURE 53. ARBITRARY PULSE SEGMENT ASSIGNMENT



NOTE: *By default, the arbitrary segments are programmed to 0x00h. The transmitter outputs will result in an all zero pattern to the line interface.*

5.3.2 DMO (Digital Monitor Output)

The driver monitor circuit is used to detect transmit driver failures by monitoring the activities at TTIP/TRING outputs. Driver failure may be caused by a short circuit in the primary transformer or system problems at the transmit inputs. If the transmitter of a channel has no output for more than 128 clock cycles, DMO goes "High" until a valid transmit pulse is detected. If the DMO interrupt is enabled, the change in status of DMO will cause the interrupt pin to go "Low". Once the status register is read, the interrupt pin will return "High" and the status register will be reset (RUR).

5.3.3 Transmit Jitter Attenuator

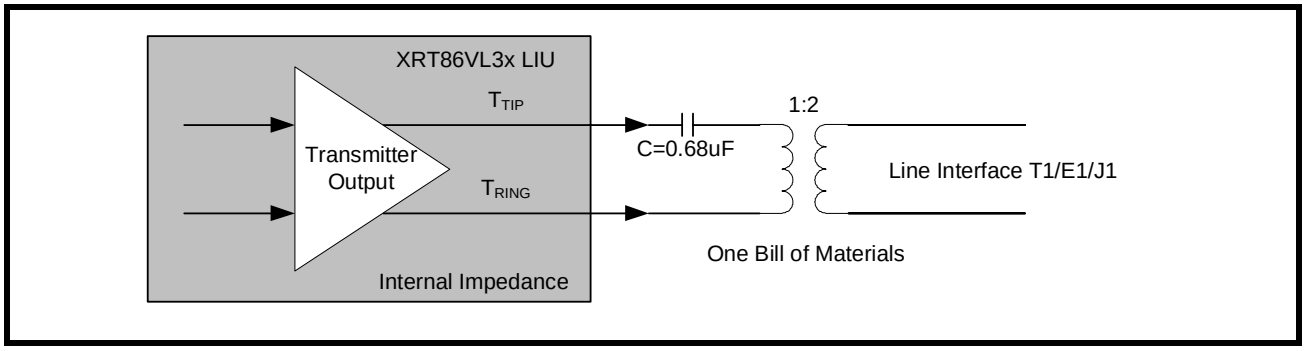
The transmit path has a dedicated jitter attenuator to reduce phase and frequency jitter in the transmit clock. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth of 32-bit or 64-bit. When the Read and Write pointers of the FIFO are within 2-Bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this condition occurs, the jitter attenuator will not attenuate input jitter until the Read/Write pointer's position is outside the 2-Bit window. In T1 mode, the bandwidth of the JA is always set to 3Hz. In E1 mode, the bandwidth is programmable to either 10Hz or 1.5Hz (1.5Hz automatically selects the 64-Bit FIFO depth). The JA has a clock delay equal to ½ of the FIFO bit depth.

NOTE: *The Receive Path has a dedicated jitter attenuator. See the Receive Path Line Interface Section.*

5.4 Line Termination (TTIP/TRING)

The output stage of the transmit path generates standard return-to-zero (RZ) signals to the line interface for T1/E1/J1 twisted pair or E1 coaxial cable. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The transmitter outputs only require one DC blocking capacitor of 0.68µF. For redundancy applications (or simply to tri-state the transmitters), set TxTSEL to a "1" in the appropriate channel register. A typical transmit interface is shown in **Figure 54**.

FIGURE 54. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



6.0 LIU RECEIVE PATH

6.1 Line Termination (RTIP/RRING)

6.1.1 Internal Termination

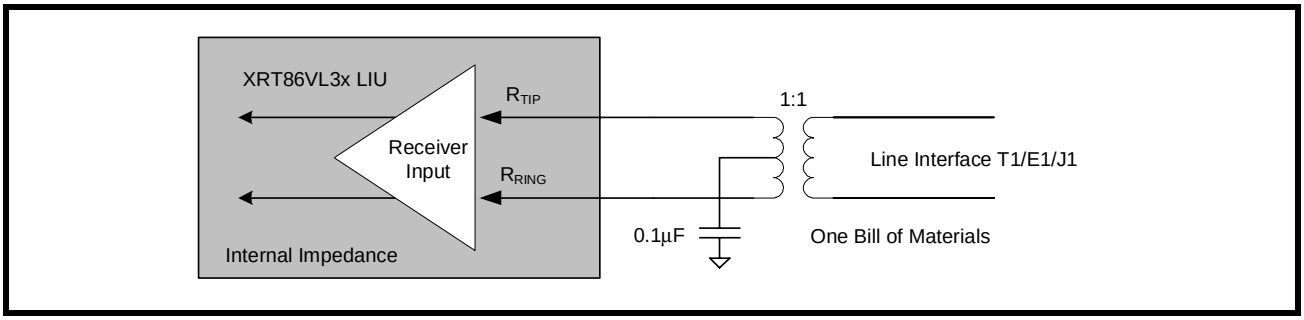
The input stage of the receive path accepts standard T1/E1/J1 twisted pair or E1 coaxial cable inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The receive termination impedance is selected by programming TERSEL[1:0] to match the line impedance. Selecting the internal impedance is shown in **Table 5**.

TABLE 5: SELECTING THE INTERNAL IMPEDANCE

TERSEL[1:0]	RECEIVE TERMINATION
0h (00)	100Ω
1h (01)	110Ω
2h (10)	75Ω
3h (11)	120Ω

The XRT86VL3x has the ability to switch the internal termination to "High" impedance by programming RxTSEL in the appropriate channel register, if the RxTSEL hardware pin is “High”. For internal termination, set RxTSEL to "1". By default, RxTSEL is set to "0" ("High" impedance). For redundancy applications, a dedicated hardware pin (RxTSEL) is available to control the receive termination for all channels simultaneously. This hardware pin is AND-ed with the register bit. Both, the register bit and the hardware pin must be set active for the receiver to be configured for internal impedance. **Figure 55** shows a typical connection diagram using the internal termination.

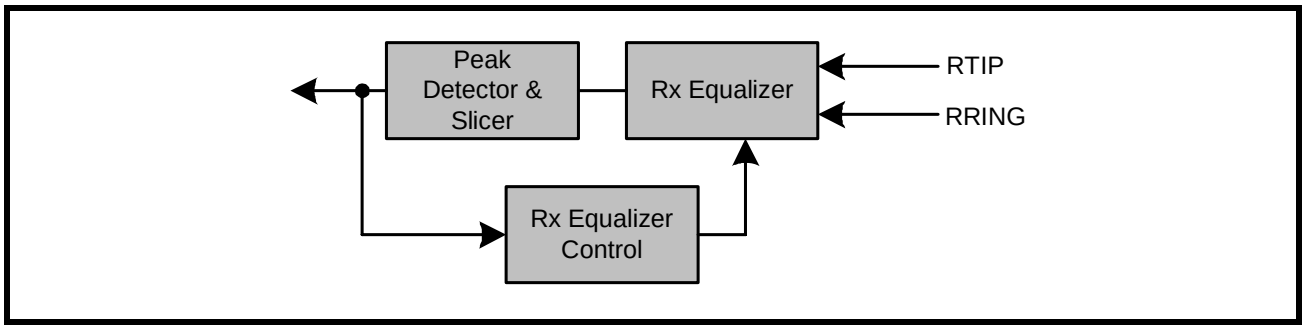
FIGURE 55. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



6.1.2 Equalizer Control

The main objective of the equalizer is to amplify an input attenuated signal to a pre-determined amplitude that is acceptable to the peak detector circuit. Using feedback from the peak detector, the equalizer will gain the input up to the maximum value specified by the equalizer control bits, in the appropriate channel register, normalizing the signal. Once the signal has reached the pre-determined amplitude, the signal is then processed within the peak detector and slicer circuit. A simplified block diagram of the equalizer and peak detector is shown in **Figure 56**.

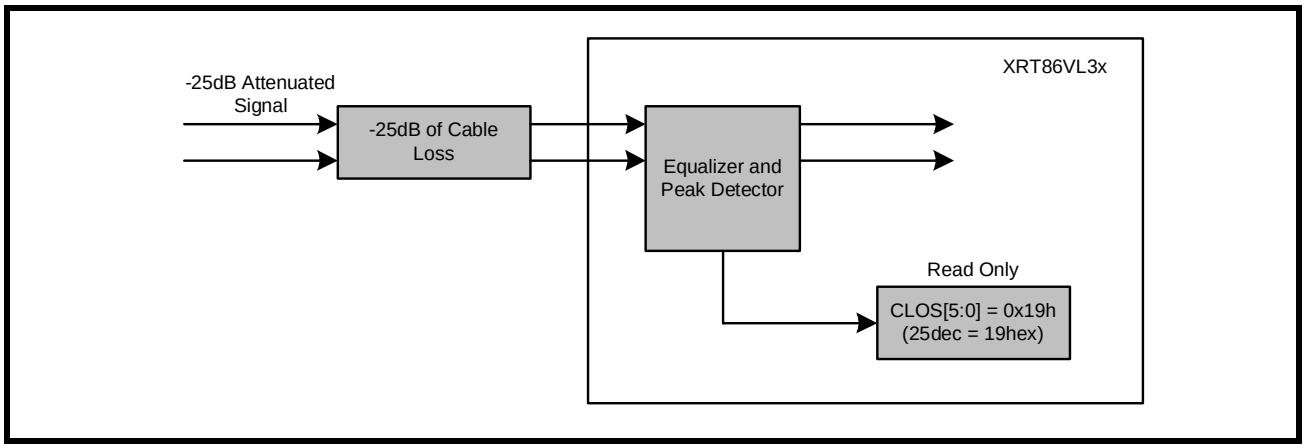
FIGURE 56. SIMPLIFIED BLOCK DIAGRAM OF THE EQUALIZER AND PEAK DETECTOR



6.1.3 Cable Loss Indicator

The ability to monitor the cable loss attenuation of the receiver inputs is a valuable feature. The XRT86VL3x contains a per channel, read only register for cable loss indication. CLOS[5:0] is a 6-Bit binary word that reports the value of cable loss in 1dB steps with an absolute accuracy of ±1dB. An example of -25dB cable loss attenuation is shown in **Figure 57**.

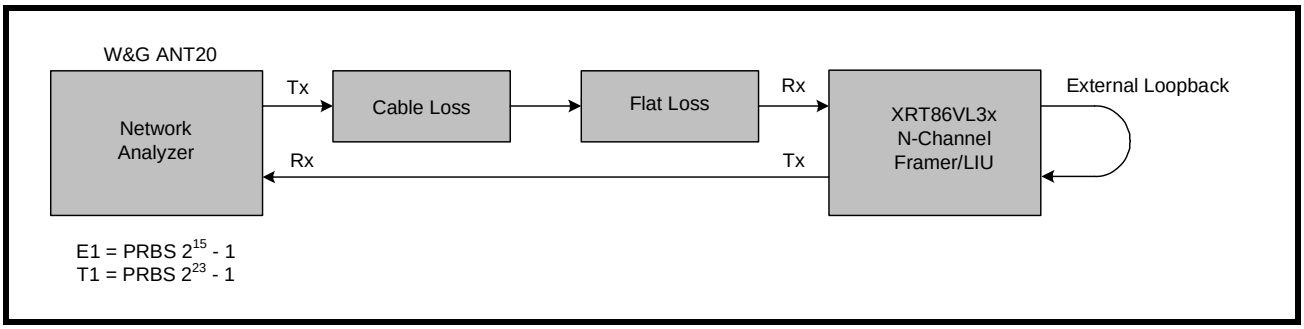
FIGURE 57. SIMPLIFIED BLOCK DIAGRAM OF THE CABLE LOSS INDICATOR



6.2 Receive Sensitivity

To meet Long Haul receive sensitivity requirements, the XRT86VL3x can accept T1/E1/J1 signals that have been attenuated by 43dB cable attenuation in E1 mode or 36dB cable attenuation in T1 mode without experiencing bit errors, LOF, pattern synchronization, etc. Short haul specifications are for 12dB of flat loss in E1 mode. T1 specifications are 655 feet of cable loss along with 6dB of flat loss in T1 mode. The XRT86VL3x can tolerate cable loss and flat loss beyond the industry specifications. The receive sensitivity in the short haul mode is approximately 4,000 feet without experiencing bit errors, LOF, pattern synchronization, etc. Although data integrity is maintained, the RLOS function (if enabled) will report an RLOS condition according to the receiver loss of signal section in this datasheet. The test configuration for measuring the receive sensitivity is shown in **Figure** .

FIGURE 58. TEST CONFIGURATION FOR MEASURING RECEIVE SENSITIVITY



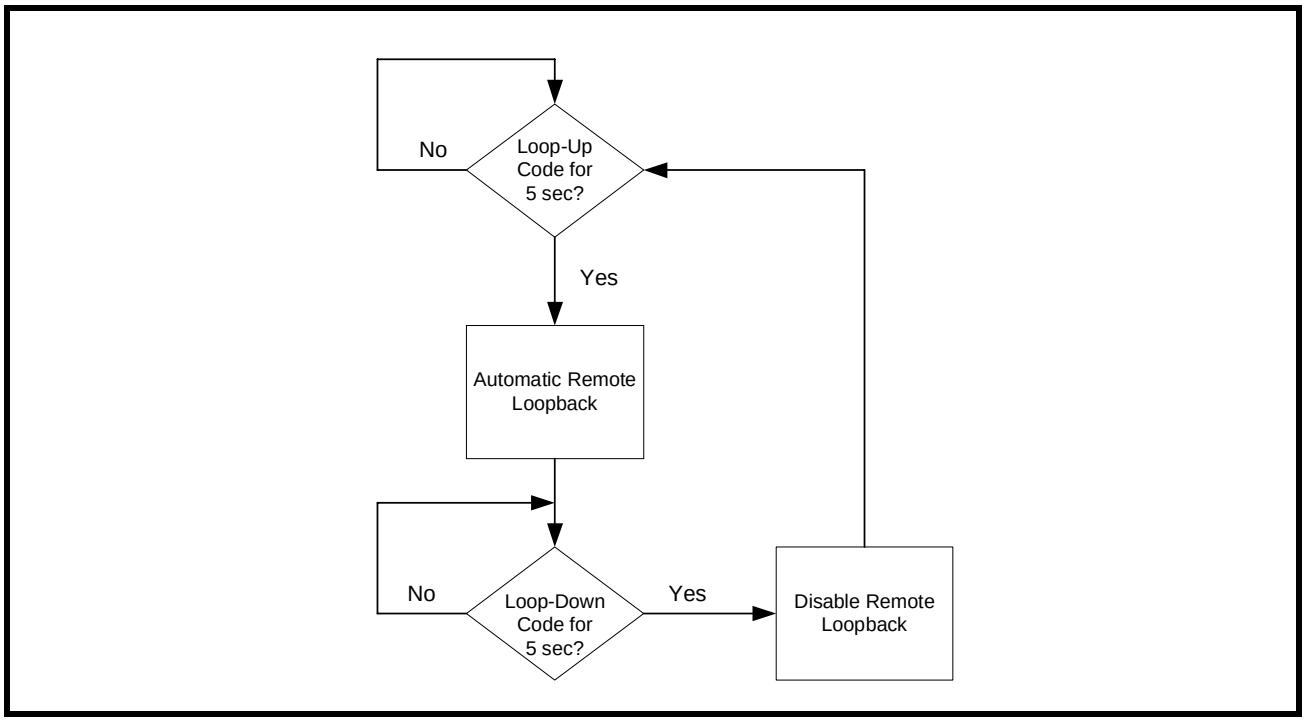
6.2.1 AIS (Alarm Indication Signal)

The XRT86VL3x adheres to the ITU-T G.775 specification for an all ones pattern. The alarm indication signal is set to "1" if an all ones pattern (at least 99.9% ones density) is present for T, where T is 3ms to 75ms in T1 mode. AIS will clear when the ones density is not met within the same time period T. In E1 mode, the AIS is set to "1" if the incoming signal has 2 or less zeros in a 512-bit window. AIS will clear when the incoming signal has 3 or more zeros in the 512-bit window.

6.2.2 NLCD (Network Loop Code Detection)

The Network Loop Code Detection can be programmed to detect a Loop-Up, Loop-Down, or Automatic Loop Code. If the network loop code detection is programmed for Loop-Up, the NLCD will be set "High" if a repeating pattern of "00001" occurs for more than 5 seconds. If the network loop code detection is programmed for Loop-Down, the NLCD will be set "High" if a repeating pattern of "001" occurs for more than 5 seconds. If the network loop code detection is programmed for automatic loop code, the LIU is configured to detect a Loop-Up code. If a Loop-Up code is detected for more than 5 seconds, the XRT86VL3x will automatically program the channel into a remote loopback mode. The LIU will remain in remote loopback even if the Loop-Up code disappears. The channel will continue in remote loop back until a Loop-Down code is detected for more than 5 seconds (or, if the automatic loop code is disabled) and then automatically return to normal operation with no loop back. The process of the automatic loop code detection is shown in **Figure 59**.

FIGURE 59. PROCESS BLOCK FOR AUTOMATIC LOOP CODE DETECTION



6.2.3 FLSD (FIFO Limit Status Detection)

The purpose of the FIFO limit status is to indicate when the Read and Write FIFO pointers are within a pre-determined range (over-flow or under-flow indication). The FLSD is set to "1" if the FIFO Read and Write Pointers are within ±3-Bits.

6.2.4 Receive Jitter Attenuator

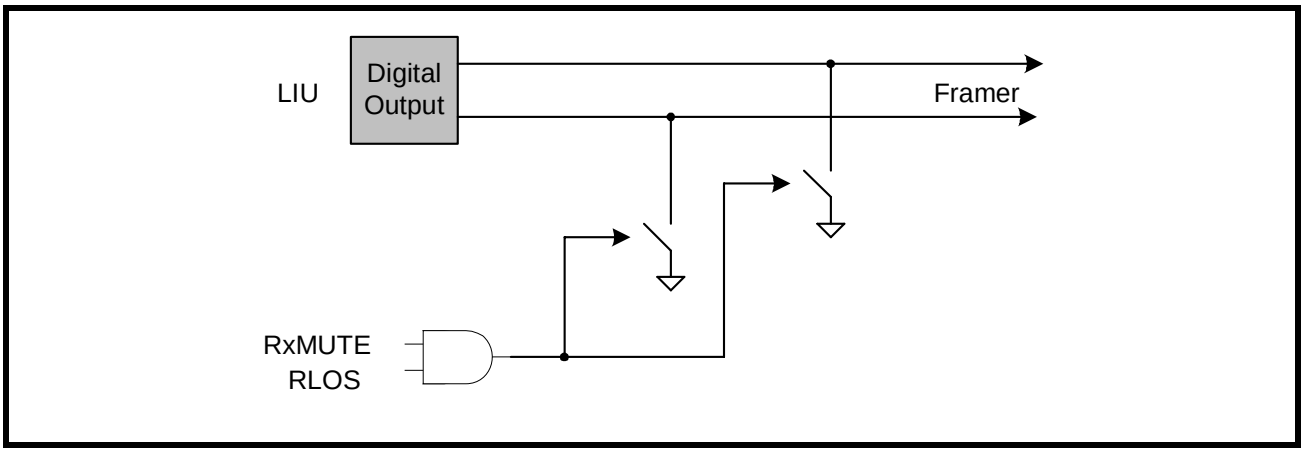
The receive path has a dedicated jitter attenuator to reduce phase and frequency jitter in the recovered clock. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth of 32-bit or 64-bit. If the LIU is used for line synchronization (loop timing systems), the JA should be enabled in the receive path. When the Read and Write pointers of the FIFO are within 2-Bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this condition occurs, the jitter attenuator will not attenuate input jitter until the Read/Write pointer's position is outside the 2-Bit window. In T1 mode, the bandwidth of the JA is always set to 3Hz. In E1 mode, the bandwidth is programmable to either 10Hz or 1.5Hz (1.5Hz automatically selects the 64-Bit FIFO depth). The JA has a clock delay equal to ½ of the FIFO bit depth.

NOTE: *The Transmit Path has a dedicated jitter attenuator. See the Transmit Path Line Interface Section.*

6.2.5 RxMUTE (Receiver LOS with Data Muting)

The receive muting function can be selected by setting RxMUTE to "1" in the appropriate global register. If selected, any channel that experiences an RLOS condition will automatically pull the output of the LIU section "Low" to prevent data chattering. If RLOS does not occur, the RxMUTE will remain inactive until an RLOS on a given channel occurs. The default setting for RxMUTE is "0" which is disabled. A simplified block diagram of the RxMUTE function is shown in **Figure 60**.

FIGURE 60. SIMPLIFIED BLOCK DIAGRAM OF THE RXMUTE FUNCTION



7.0 THE E1 TRANSMIT/RECEIVE FRAMER

7.1 Description of the Transmit/Receive Payload Data Input Interface Block

Each framer within the XRT86VL3x device includes a Transmit and Receive Payload Data Input Interface block. Although most configurations are independent for the Tx and Rx path, once E1 framing has been selected, both the Tx and Rx must operate in E1. The Payload Data Input Interface module (also known as the Back-plane Interface module) supports payload data to be taken from or presented to the system. In E1 mode, supported data rates are 2.048Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s, or H.100 16.384Mbit/s.

7.1.1 Brief Discussion of the Transmit/Receive Payload Data Input Interface Block Operating at XRT84V24 Compatible 2.048Mbit/s mode

Whether or not the transmit/receive interface signals have been chosen as inputs or outputs, the overall system timing diagrams remain the same. It is the responsibility of the Terminal Equipment to provide serial input data through the TxSER pin aligned with the Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal. **Figure 61** shows how to connect the Transmit Payload Data Input Interface block to local Terminal Equipment. **Figure 62** shows how to connect the Receive Payload Data Output Interface to local Terminal Equipment.

FIGURE 61. INTERFACING THE TRANSMIT PATH TO LOCAL TERMINAL EQUIPMENT

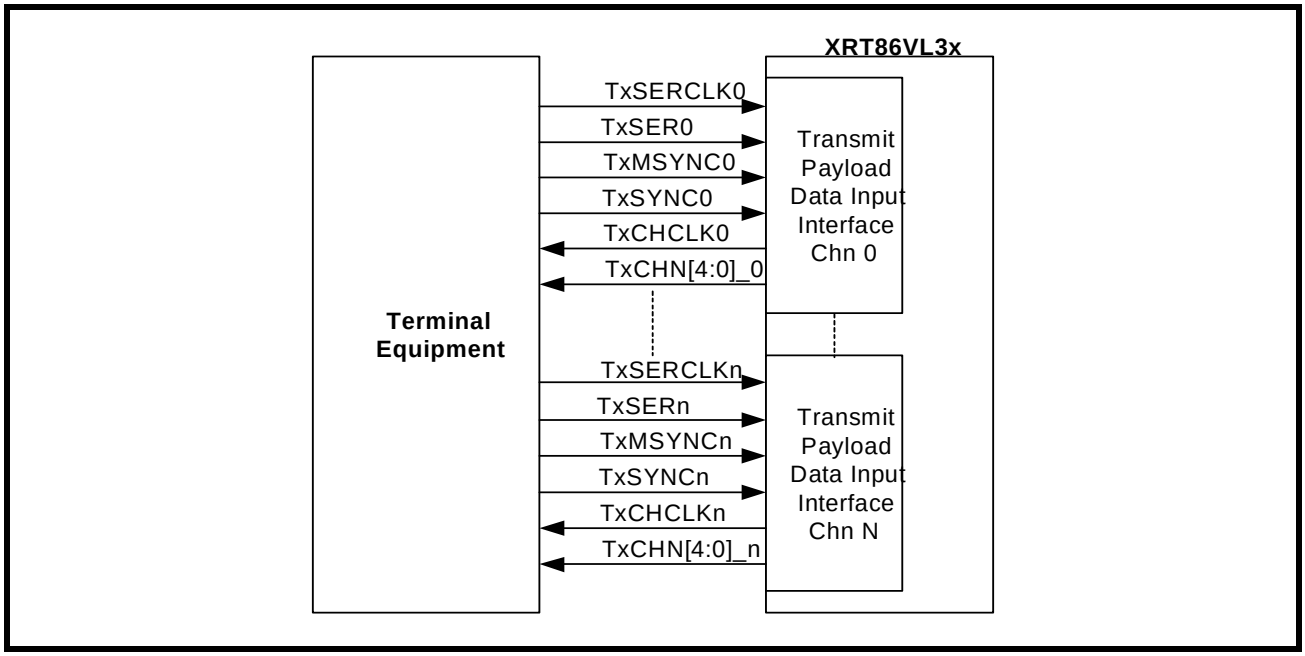


FIGURE 62. INTERFACING THE RECEIVE PATH TO LOCAL TERMINAL EQUIPMENT

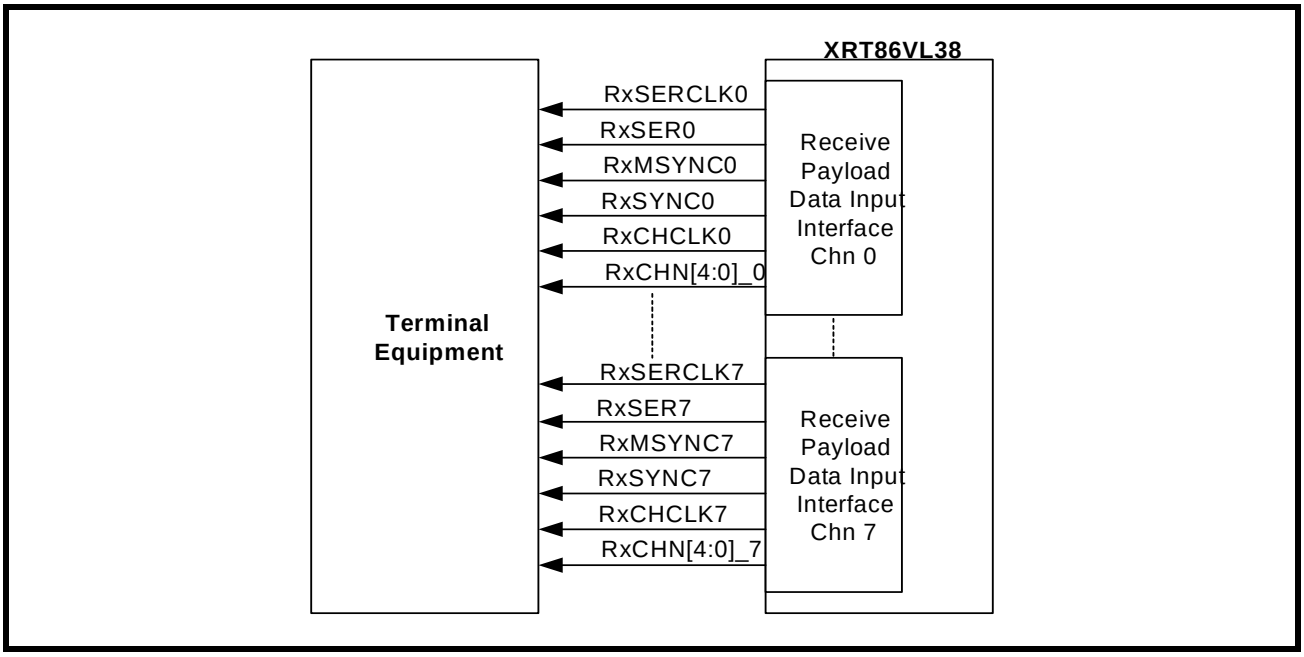


Figure 63 shows the waveforms for connecting the Transmit Payload Data Input Interface block to local Terminal Equipment. **Figure 64** shows the waveforms for connecting the Receive Payload Data Input Interface block to local Terminal Equipment.

FIGURE 63. WAVEFORMS FOR CONNECTING THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO LOCAL TERMINAL EQUIPMENT

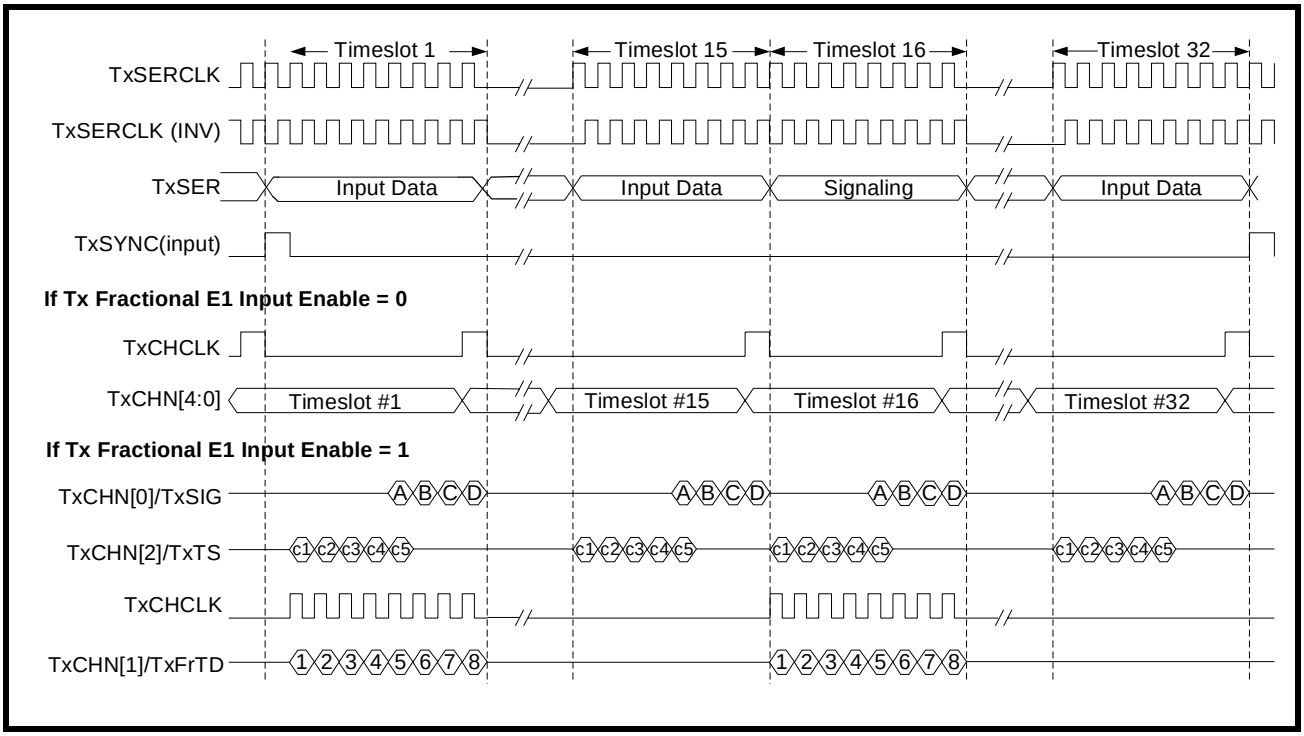
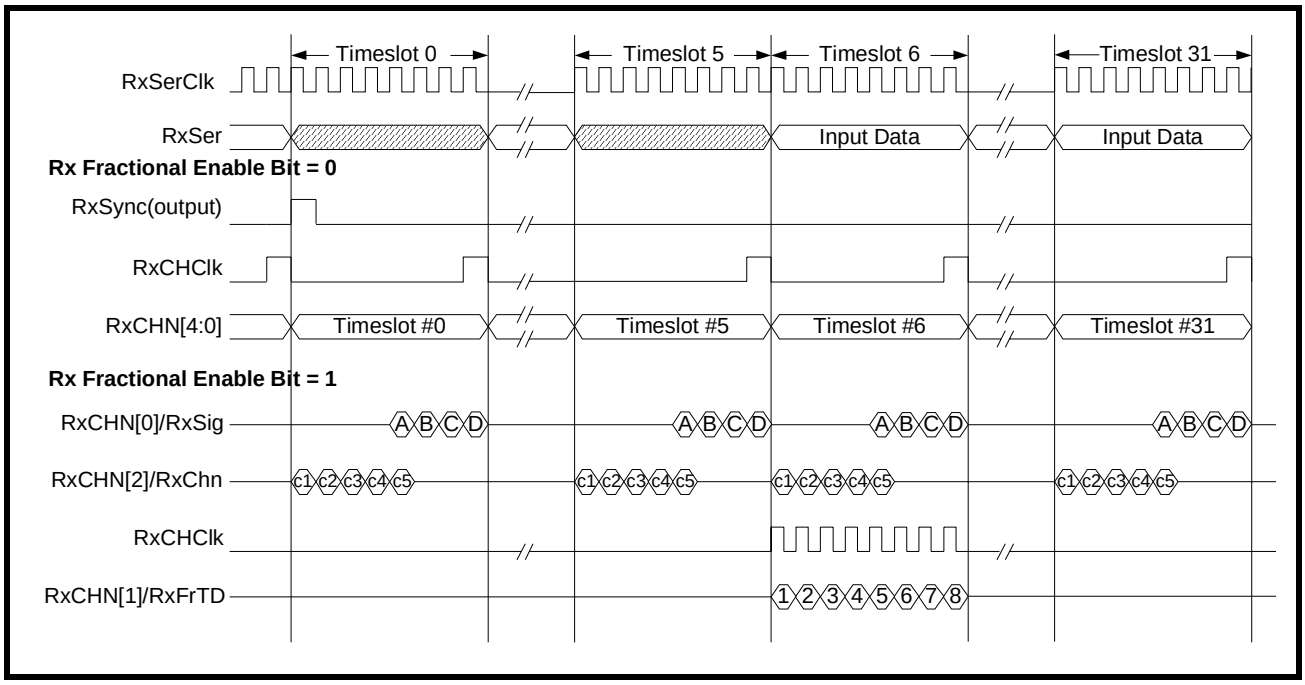


FIGURE 64. WAVEFORMS FOR CONNECTING THE RECEIVE PAYLOAD DATA INPUT INTERFACE BLOCK TO LOCAL TERMINAL EQUIPMENT



7.2 Transmit/Receive High-Speed Back-Plane Interface

The High-speed Back-plane Interface supports payload data to be taken from or presented to the Terminal Equipment at different data rates. In the non-multiplexed mode, payload data of each channel are interfaced to the Terminal Equipment separately. Each channel uses its own serial clock, serial data, single-frame synchronization signal and multi-frame synchronization signals.

7.2.1 Non-Multiplexed High-Speed Mode

When the Back-plane interface data rate is MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s, the interface signals are all configured as inputs, except the receive serial data on RxSER and the multi frame sync pulse provided by the framer. The Transmit Serial Clock for each channel is always an input clock with frequency of 2.048 MHz for all data rates so that it may be used as the timing reference for the transmit line rate. The TxMSYNC signal is configured as the Transmit Input Clock with frequencies of 2.048 MHz, 4.096 MHz and 8.192 MHz respectively. It serves as the primary clock source for the High-speed Back-plane Interface. **Figure 65** shows how to connect the Transmit non-multiplexed high-speed Input Interface block to local Terminal Equipment. **Figure 66** shows how to connect the Receive non-multiplexed high-speed Output Interface to local Terminal Equipment.

FIGURE 65. TRANSMIT NON-MULTIPLEXED HIGH-SPEED CONNECTION TO LOCAL TERMINAL EQUIPMENT USING MVIP 2.048MBIT/S, 4.096MBIT/S, OR 8.192MBIT/S

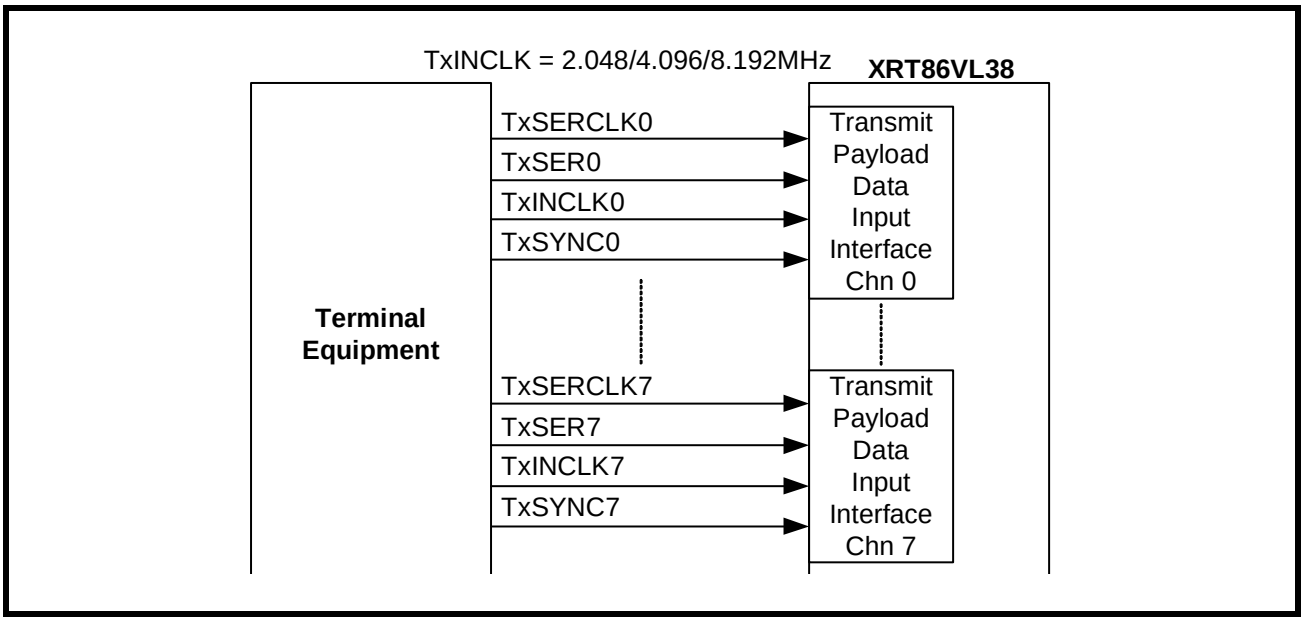


FIGURE 66. RECEIVE NON-MULTIPLEXED HIGH-SPEED CONNECTION TO LOCAL TERMINAL EQUIPMENT USING MVIP 2.048MBIT/S, 4.096MBIT/S, OR 8.192MBIT/S

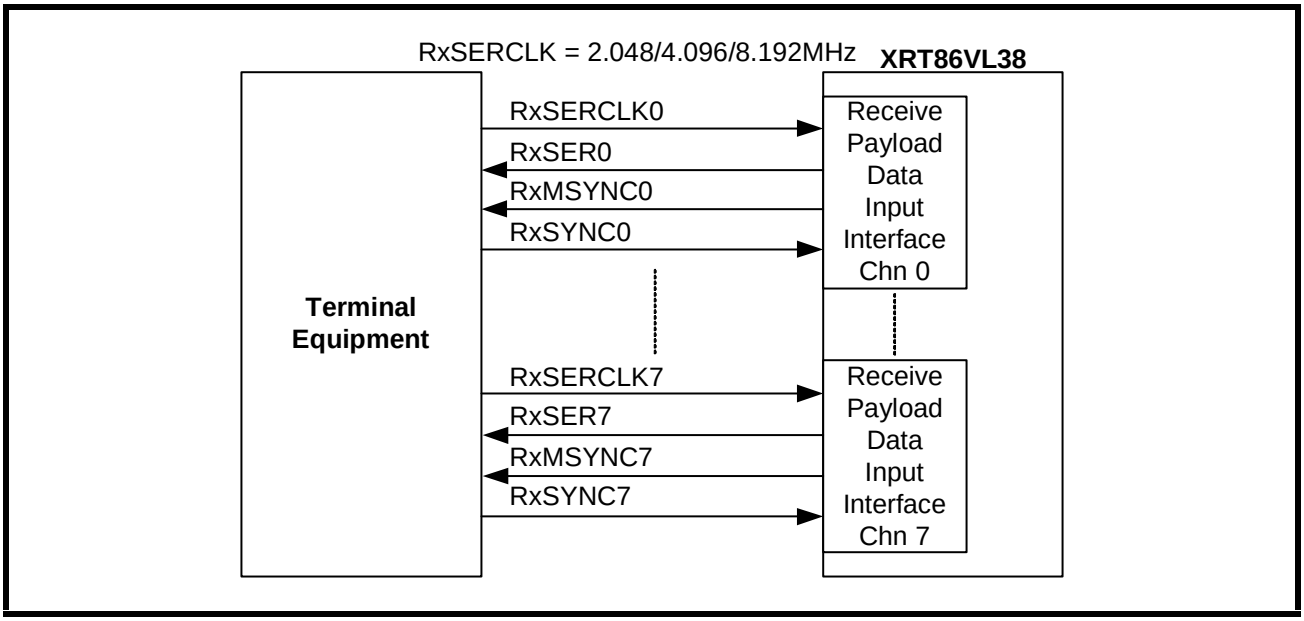


Figure 67 shows the waveforms for connecting the Transmit non-multiplexed high-speed Input Interface block to local Terminal Equipment. Figure 68 shows the waveforms for connecting the Receive non-multiplexed high-speed Input Interface block to local Terminal Equipment.

FIGURE 67. WAVEFORMS FOR CONNECTING THE TRANSMIT NON-MULTIPLEXED HIGH-SPEED INPUT INTERFACE AT MVIP 2.048MBIT/S, 4.096MBIT/S, AND 8.192MBIT/S

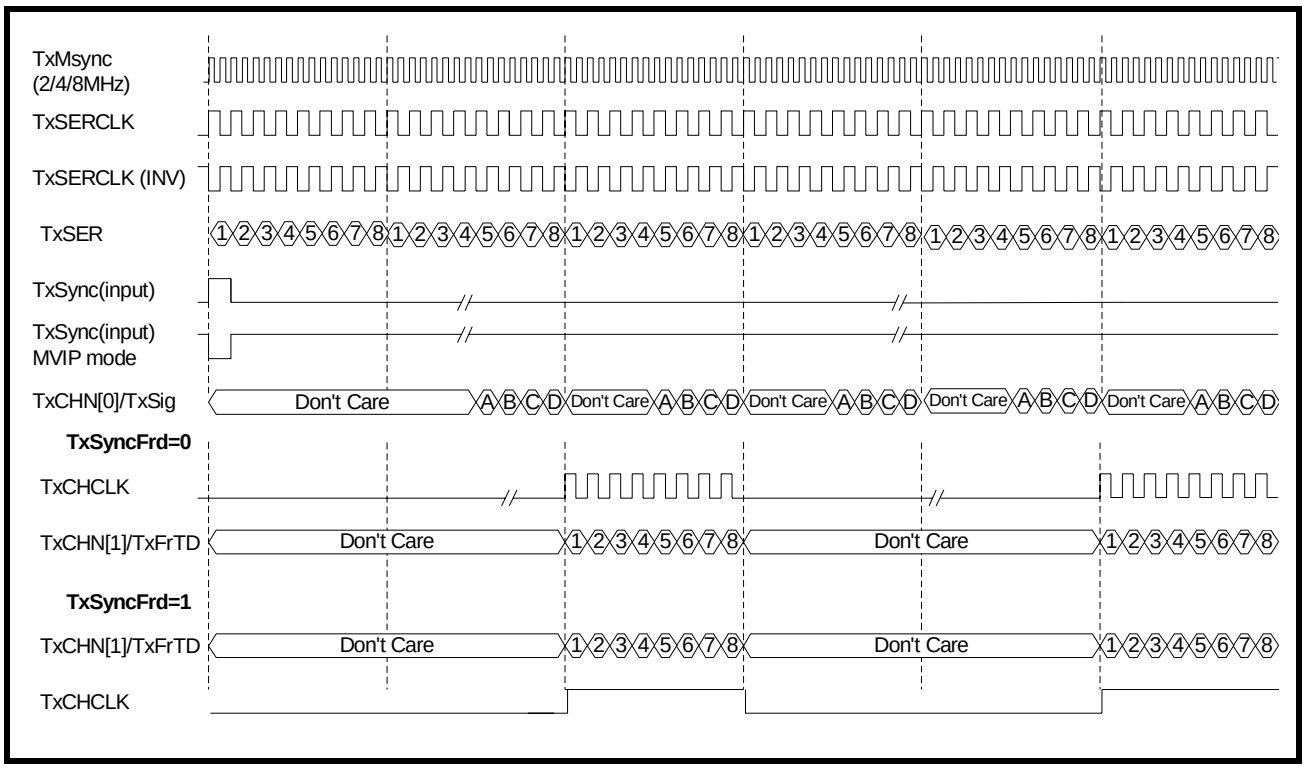
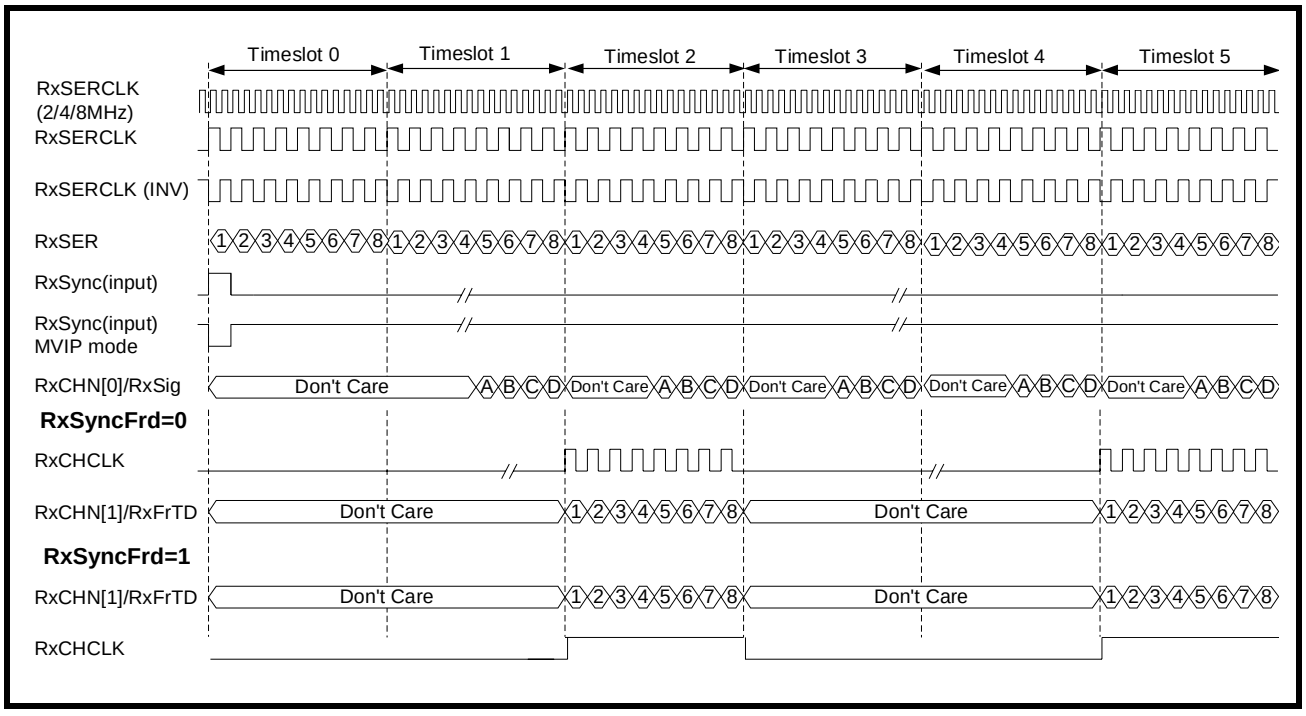


FIGURE 68. WAVEFORMS FOR CONNECTING THE RECEIVE NON-MULTIPLEXED HIGH-SPEED INPUT INTERFACE AT MVIP 2.048MBIT/S, 4.096MBIT/S, AND 8.192MBIT/S



7.2.2 Multiplexed High-Speed Mode

Bit-Multiplexed 16.384Mbit/s

When the Back-plane interface data rate is 16.384Mbit/s, HMVIP 16.384Mbit/s, and H.100 16.384Mbit/s, the interface signals are all configured as inputs, except the receive serial data on RxSER and the multi frame sync pulse provided by the framer. The Transmit Serial Clock for each channel is always an input clock with frequency of 2.048 MHz for all data rates so that it may be used as the timing reference for the transmit line rate. The TxMSYNC signal is configured as the Transmit Input Clock with frequency of 16.384 MHz. It serves as the primary clock source for the High-speed Back-plane Interface. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4. The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH at the beginning of the multiplexed frame with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH at the beginning of the multiplexed frame with data from Channel 4-7 multiplexed together. It is the responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse. Additionally, each channel requires the local Terminal Equipment to provide a free-running 2.048 MHz clock into the Transmit Serial Clock input. The local Terminal Equipment maps four 2.048Mbit/s E1 data streams into one 16.384Mbit/s serial data stream as described below:

1. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last.

After the first bit of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_3	1_3

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

X_Y: The Xth payload bit of Channel Y

2. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream.

When the Terminal Equipment is sending the fifth payload bit of one channel, instead of sending it twice, it inserts the signaling bit A of that corresponding channel. Similarly, the sixth payload bit is followed by the signaling bit B of that corresponding channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

3. After the first octet of all four channels are sent, the local Terminal Equipment start sending the second octets following the same rules of Step 1 and 2.

The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position of the multiplexed data stream with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed E1 frame. It is the responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT86VL3x device and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 2.048MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device. **Figure 69** shows how to connect the Transmit multiplexed high-speed Input Interface block to local Terminal Equipment. **Figure** shows the timing signals when framer is running at 16.384MHz Bit-Multiplexed mode.

HMVIP/ H100 16.384Mbit/s Byte-Multiplexed Mode

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 10, the Transmit Back-plane interface of framer is running at HMVIP 16.384MHz. When Transmit Interface Mode Select[1:0] bits are set to 11, the Transmit Back-plane interface is running at H100 16.384MHz mode.

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 16.384Mbit/s. The local Terminal Equipment multiplexes payload data of every four channels into one data stream. Payload data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 2.048Mbit/s E1 data streams into this 16.384Mbit/s data stream as described below:

1. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent last.

After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into one 16.384Mbit/s data stream

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

2. When the framer is running at HMVIP or H100 16.384MBit/s byte-mulitplexed mode, signaling information is inserted from the TxSig/TSb[0] pin or from the TSCR register (0xn340-n35F).

When the local terminal is sending the fifth payload bit of one channel, signaling bit A of that corresponding channel is repeated and sent through the TxSig/TSb[0] pin; Similarly, signaling bit B, C, and D of the corresponding channel is repeated and sent through the TxSig/TSb[0] pin when the local terminal is providing the sixth, seventh, and eighth payload bit respectively, as shown in **Figure 71**.

3. After the first octet of all four channels are sent, the local Terminal Equipment start sending the second octets following the same rules of Step 1 and 2.

For HMVIP mode, the Transmit Single-frame Synchronization signal should pulse HIGH for four clock cycles (the last two bit positions of the previous multiplexed frame and the first two bits of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. For H100 mode, the Transmit Single-frame Synchronization signal should pulse HIGH for two clock cycles (the last bit position of the previous multiplexed frame and the first bit position of the next multiplexed frame). The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH to identify the start of multiplexed data stream of Channel 4-7. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer

can position the beginning of the multiplexed E1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT86VL3x device and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 2.048MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

See Figure 69 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in HMVIP or H100 16.384Mbit/s mode. Figure 71 shows the timing signals when the framer is running at HMVIP or H100 16.384 MHz mode.

FIGURE 69. INTERFACING XRT86VL3X TRANSMIT TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S, HMVIP 16.384MBIT/S, AND H.100 16.384MBIT/S

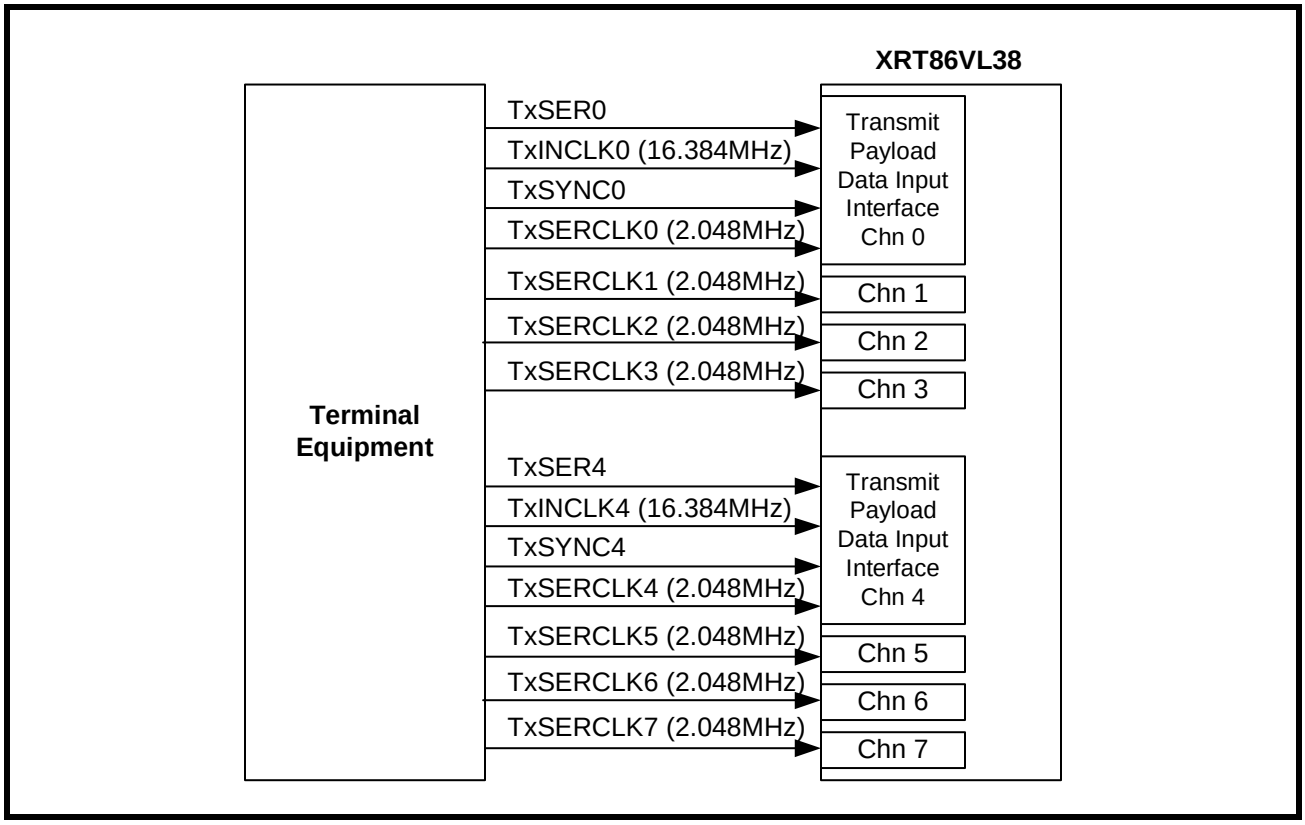


FIGURE 70. TIMING SIGNAL WHEN THE FRAMER IS RUNNING AT BIT-MULTIPLEXED 16.384MBIT/S MODE

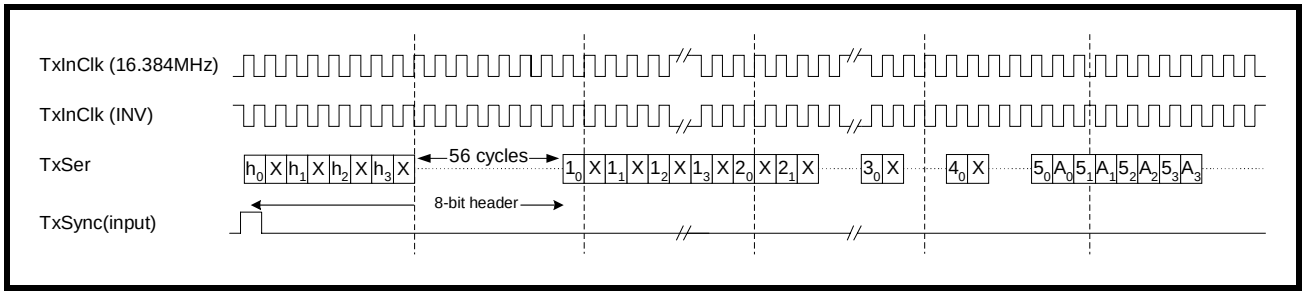
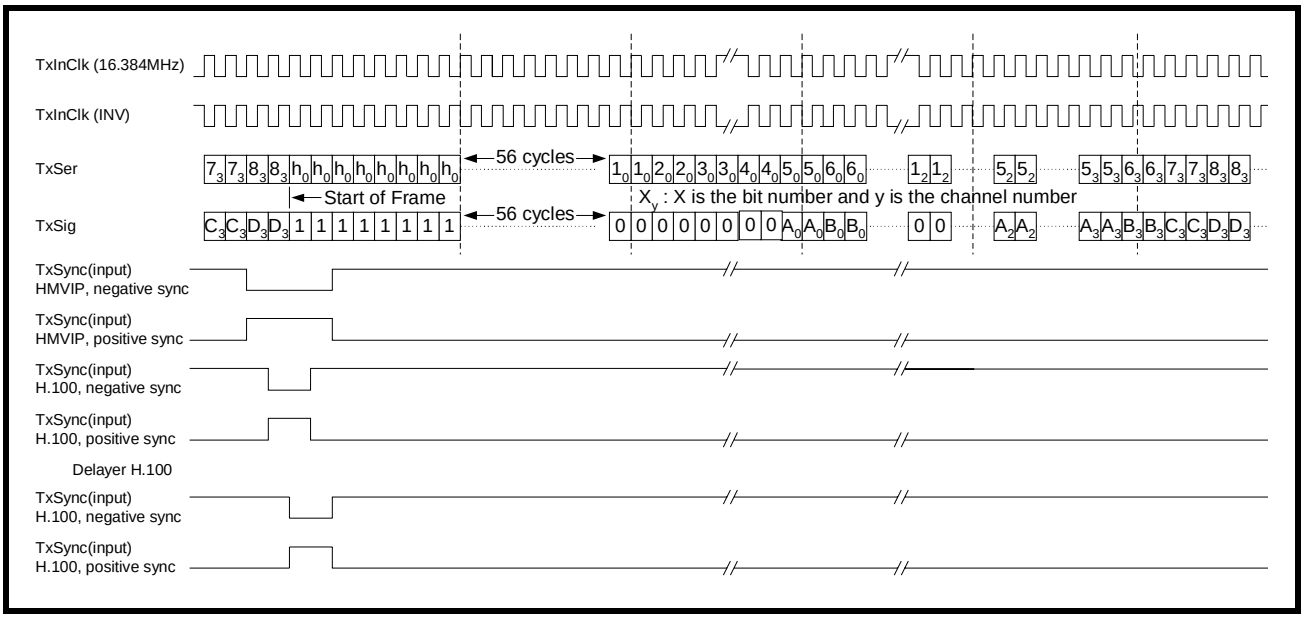


FIGURE 71. WAVEFORMS FOR CONNECTING THE TRANSMIT MULTIPLEXED HIGH-SPEED INPUT INTERFACE AT HMVIP AND H.100 16.384MBIT/S MODE



E1 Receive Multiplexed Mode

The interface consists of the following pins:

- Data Output (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 16.384Mbit/s. It multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock. Figure 72 shows the interface of the Recieve Payload Data Output Interface Block to the Terminal Equipment.

The multiplexed data output on RxSER_0 or RxSER_4 are very similar to the Multiplexed data input on TxSER_0 or TxSER_4 except when the receive framer is running at 16MHz Bit-Multiplexed mode. When the receive framer is running at 16MHz Bit-Multiplexed mode, the multiplexed data on RxSER_0 or RxSER_4 are return-to-zero data when the receive framer is processing the first four bits of each time slot data of each channel, as shown in Figure . Figure shows the timing signal when the receive framer is running at HMVIP or H.100 16.384 MHz mode.

FIGURE 72. INTERFACING XRT86VL3X RECEIVE TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S, HMVIP 16.384MBIT/S, AND H.100 16.384MBIT/S

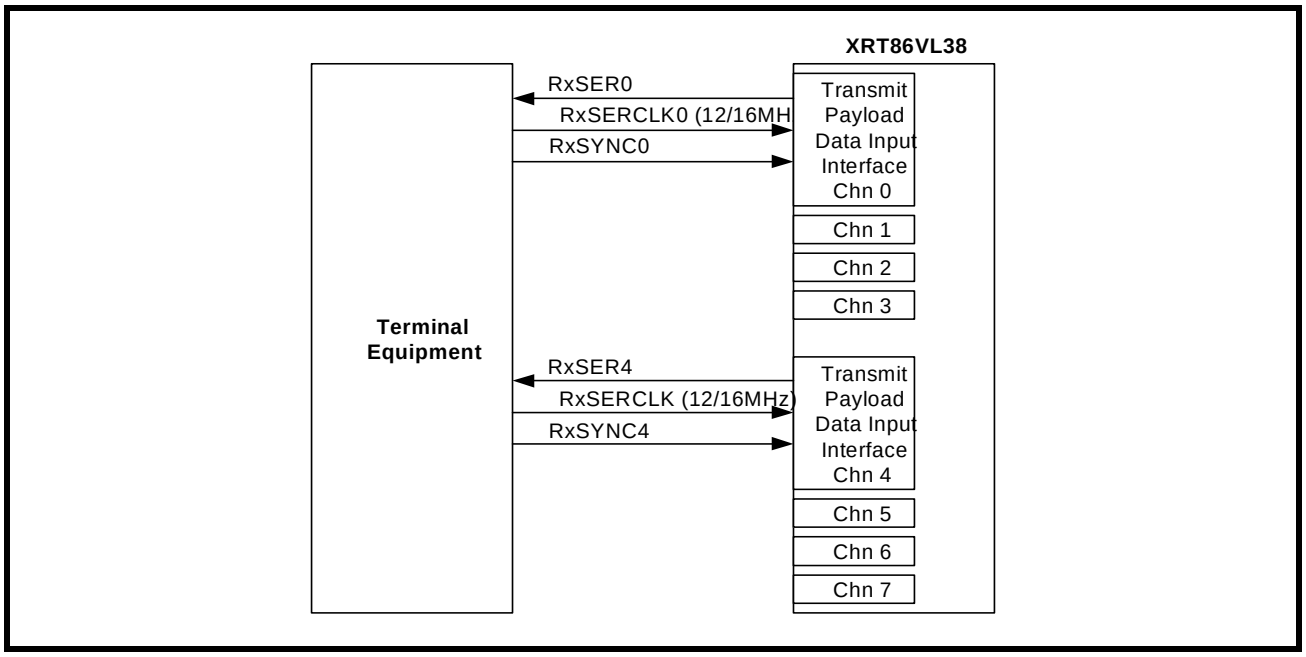


FIGURE 73. TIMING SIGNAL WHEN THE RECEIVE FRAMER IS RUNNING AT 16.384MHZ BIT-MULITPLEXED MODE

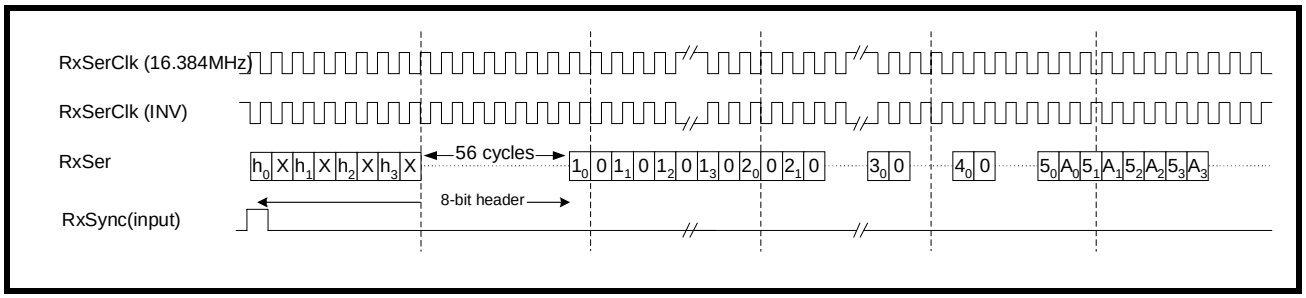
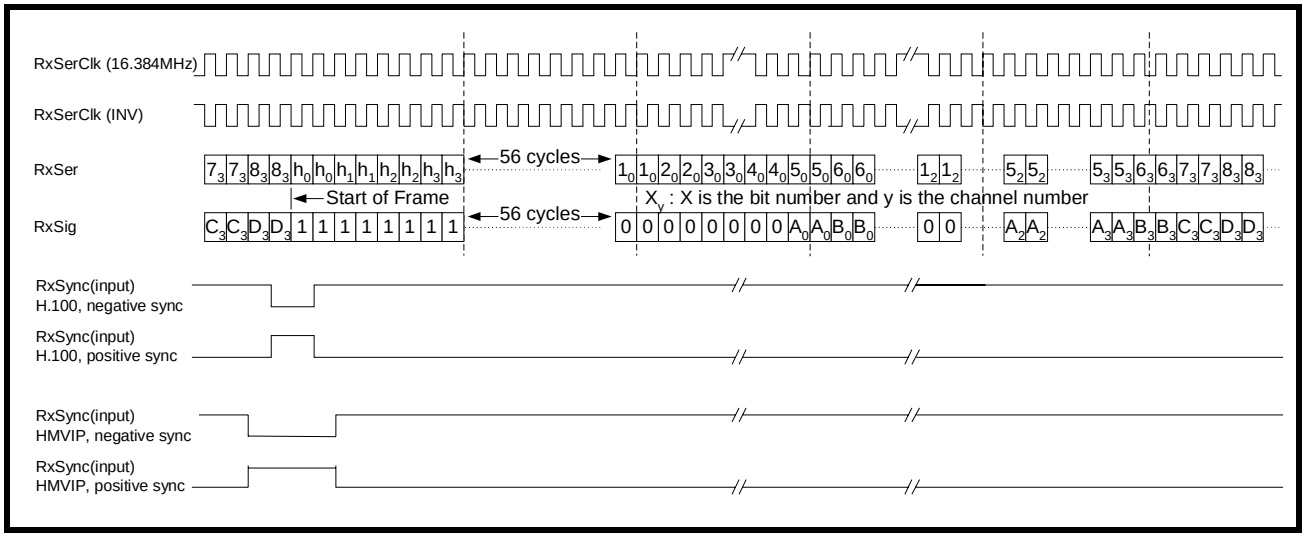


FIGURE 74. TIMING SIGNAL WEHN THE RECEIVE FRAMER IS RUNNING AT HMVIP AND H100 16.384MHZ MODE



7.3 Brief Discussion of Common Channel Signaling in E1 Framing Format

As the name referred, Common Channel Signaling is signaling information common to all thirty voice or data channels of an E1 trunk. Time slot 16 may be used to carry Common Channel Signaling data of up to a rate of 64kbits/s. The national bits of time slot 0 may also be used for Common Channel Signaling. Since there are five national bits of time slot 0 per every two E1 frames, the total bandwidth of the national bits is 20kbits/s. The Common Channel Signaling is essentially data link information that provides performance monitoring and a transmission quality report.

7.4 Brief Discussion of Channel Associated Signaling in E1 Framing Format

Signaling is required when dealing with voice and dial-up data services in E1 applications. Traditionally, signaling is provided on a dial-up telephone line across the talk-path. Signaling is used to tell the receiver where the call or route is destined. The signal is sent through switches along the route to a distant end. Common types of signals are:

- On hook
- Off hook
- Dial tone
- Dialed digits
- Ringing cycle
- Busy tone

A signal is consists of four bits namely A, B, C and D. These bits define the state of the call for a particular time slot. Time slot 16 of each E1 frame can carry CAS signals for two E1 voice or data channels. Therefore, sixteen E1 frames are needed to carry CAS signals for all 32 E1 channels. The sixteen E1 frames then forms a CAS Multi-frame.

7.5 Insert/Extract Signaling Bits from TSCR Register

The four most significant bits of the Transmit Signaling Control Register (TSCR) of each time slot can be used to store outgoing signaling data. The user can program these bits through microprocessor access. If the XRT86VL3x framer is configure to insert signaling bits from TSCR registers, the E1 Transmit Framer block will fill up the time slot 16 octet with the signaling bits stored inside the TSCR registers. The insertion of signaling bit into PCM data is done on a per-channel basis. The most significant bit (Bit 7) of TSCR register is used to store Signaling bit A. Bit 6 is used to hold Signaling bit B. Bit 5 is used to hold Signaling bit C. Bit 4 is used to hold Signaling bit D.

7.6 Insert/Extract Signaling Bits from TxCHN[0]_n/TxSIG Pin

The XRT86VL3x framer can be configured to insert/extract signaling bits provided by external equipment through the external signaling bus. When the Fractional E1 mode is enabled, this bus is configured as TxSIG and RxSIG. These pins act as an the signaling bus for the outbound E1 frames.

Figure 75 shows a timing diagram of the TxSIG input pin. **Figure 76** shows a timing diagram of the RxSIG output pin. Please note that the Signaling Bit A of a certain channel coincides with Bit 5 of the PCM data of that channel; Signaling Bit B coincides with Bit 6 of the PCM data; Signaling Bit C coincides with Bit 7 of the PCM data and Signaling Bit D coincides with Bit 8 (LSB) of the PCM data.

FIGURE 75. TIMING DIAGRAM OF THE TXSIG INPUT

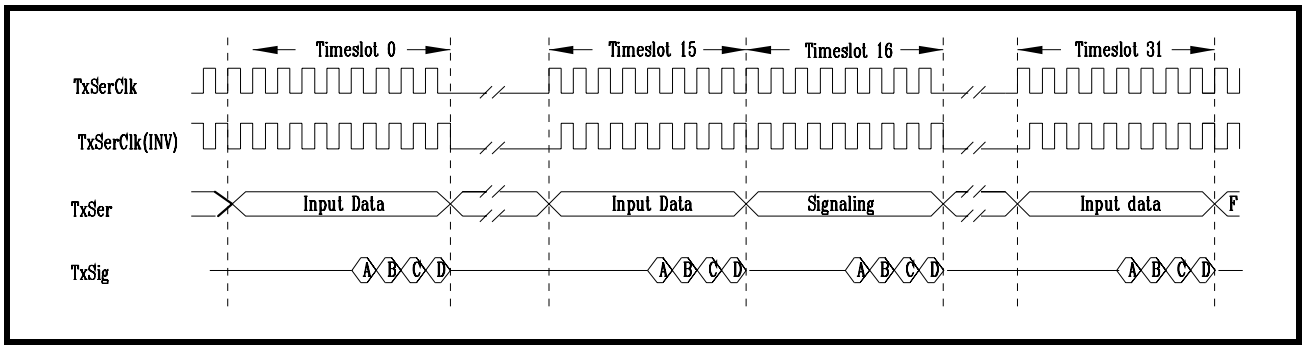
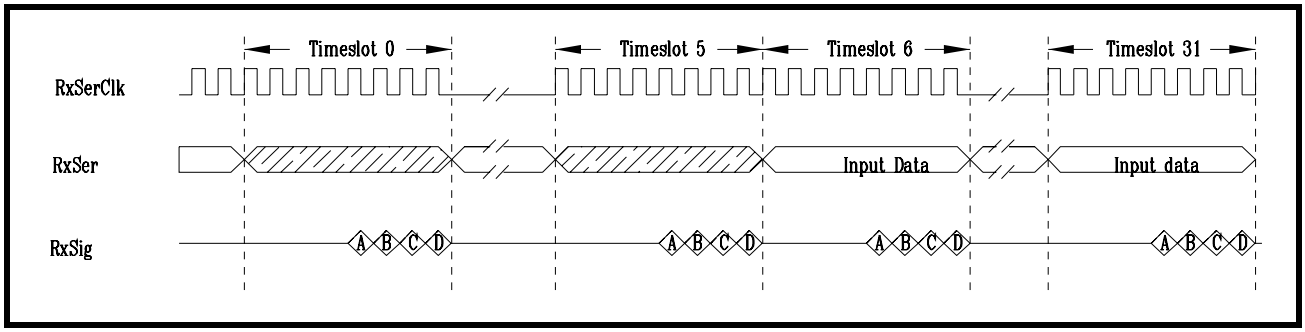


FIGURE 76. TIMING DIAGRAM OF THE RXSIG OUTPUT



7.7 Enable Channel Associated Signaling and Signaling Data Source Control

The Transmit Signaling Control Register (TSCR) of each channel selects source of signaling data to be inserted into the outgoing E1 frame and enables Channel Associated signaling. As we mentioned before, the signaling data can be inserted from Transmit Signaling Control Registers (TSCR) of each timeslot, from the TxSig_n input pin, from the TxOH_n input pin or from the TxSer_n input pin. The Transmit Signaling Data Source Select [1:0] bits of the Transmit Signaling Control Register (TSCR) determines from which sources the signaling data is inserted from.

8.0 THE DS1 TRANSMIT/RECEIVE FRAMER

8.1 Description of the Transmit/Receive Payload Data Input Interface Block

Each of the four framers within the XRT86VL3x device includes a Transmit and Receive Payload Data Input Interface block. Although most configurations are independent for the Tx and Rx path, once T1 framing has been selected, both the Tx and Rx must operate in T1. The Payload Data Input Interface module (also known as the Back-plane Interface module) supports payload data to be taken from or presented to the system. In T1 modes, supported data rates are 1.544Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 12.352Mbit/s, 16.384Mbit/s, HMVIP 16.384Mbit/s, or H.100 16.384Mbit/s.

8.1.1 Brief Discussion of the Transmit/Receive Payload Data Input Interface Block Operating at 1.544Mbit/s mode

Whether or not the transmit/receive interface signals have been chosen as inputs or outputs, the overall system timing diagrams remain the same. It is the responsibility of the Terminal Equipment to provide serial input data through the TxSER pin aligned with the Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal. **Figure 77** shows how to connect the Transmit Payload Data Input Interface block to local Terminal Equipment. **Figure 78** shows how to connect the Receive Payload Data Output Interface to local Terminal Equipment.

FIGURE 77. INTERFACING THE TRANSMIT PATH TO LOCAL TERMINAL EQUIPMENT

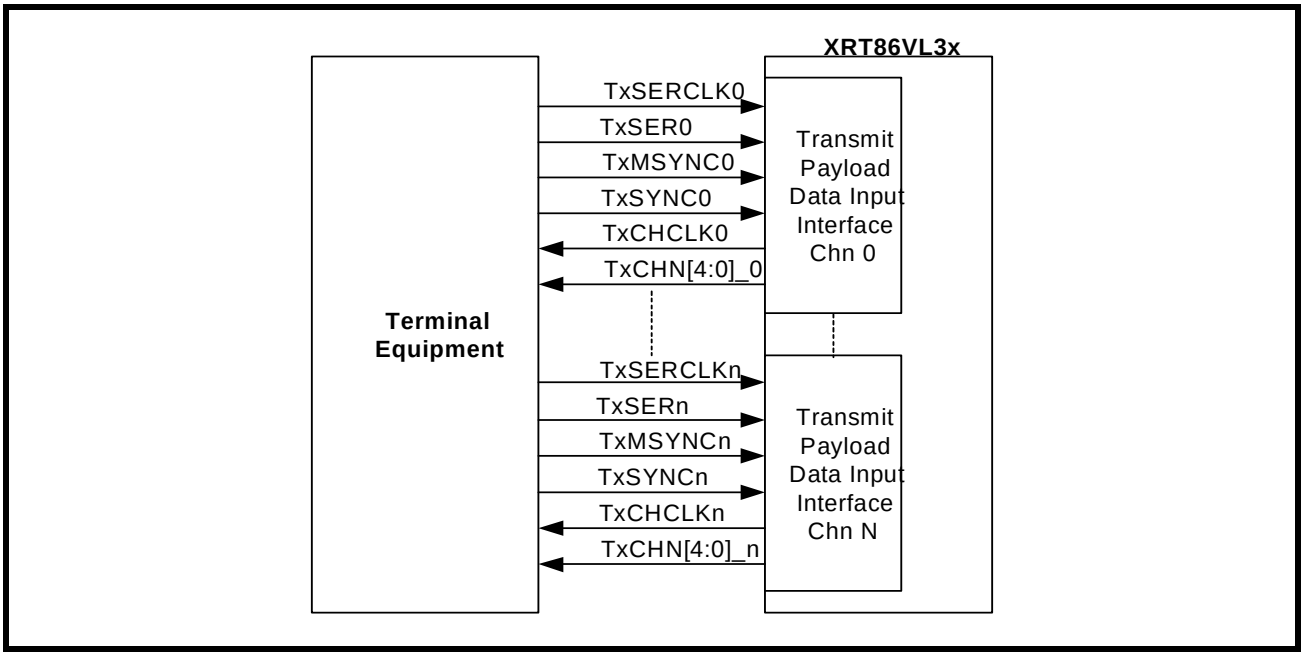


FIGURE 78. INTERFACING THE RECEIVE PATH TO LOCAL TERMINAL EQUIPMENT

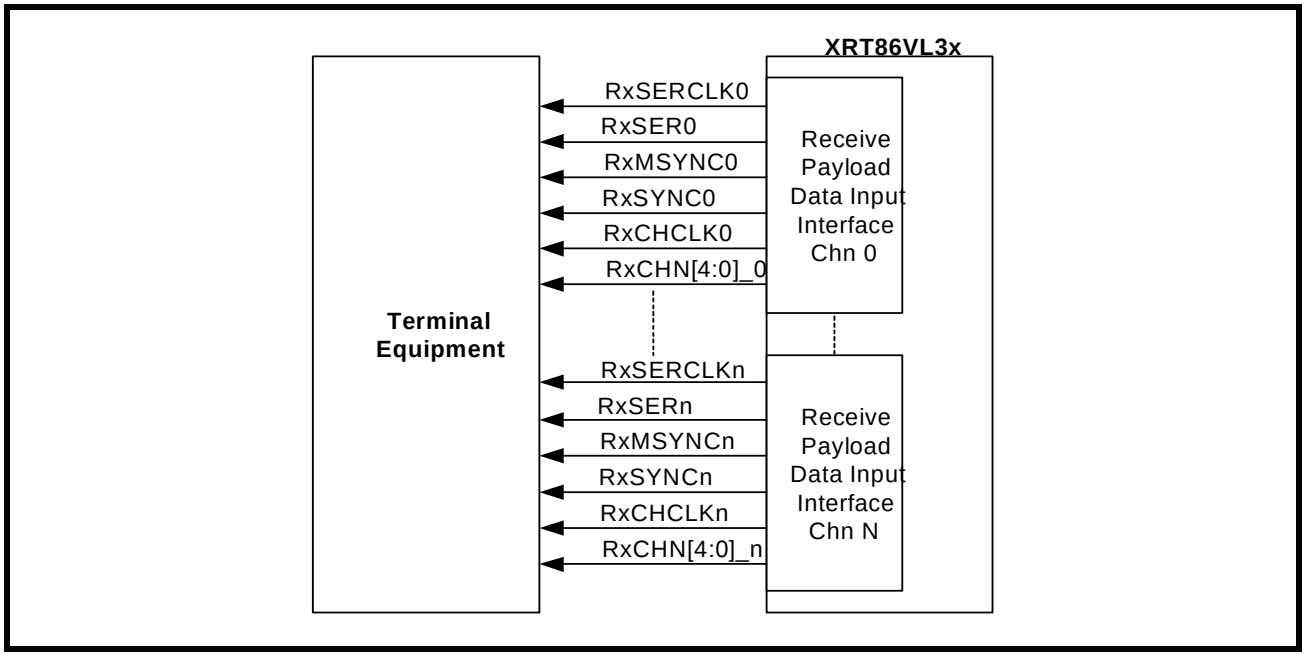


Figure 79 shows the waveforms for connecting the Transmit Payload Data Input Interface block to local Terminal Equipment. **Figure 80** shows the waveforms for connecting the Receive Payload Data Input Interface block to local Terminal Equipment.

FIGURE 79. WAVEFORMS FOR CONNECTING THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO LOCAL TERMINAL EQUIPMENT

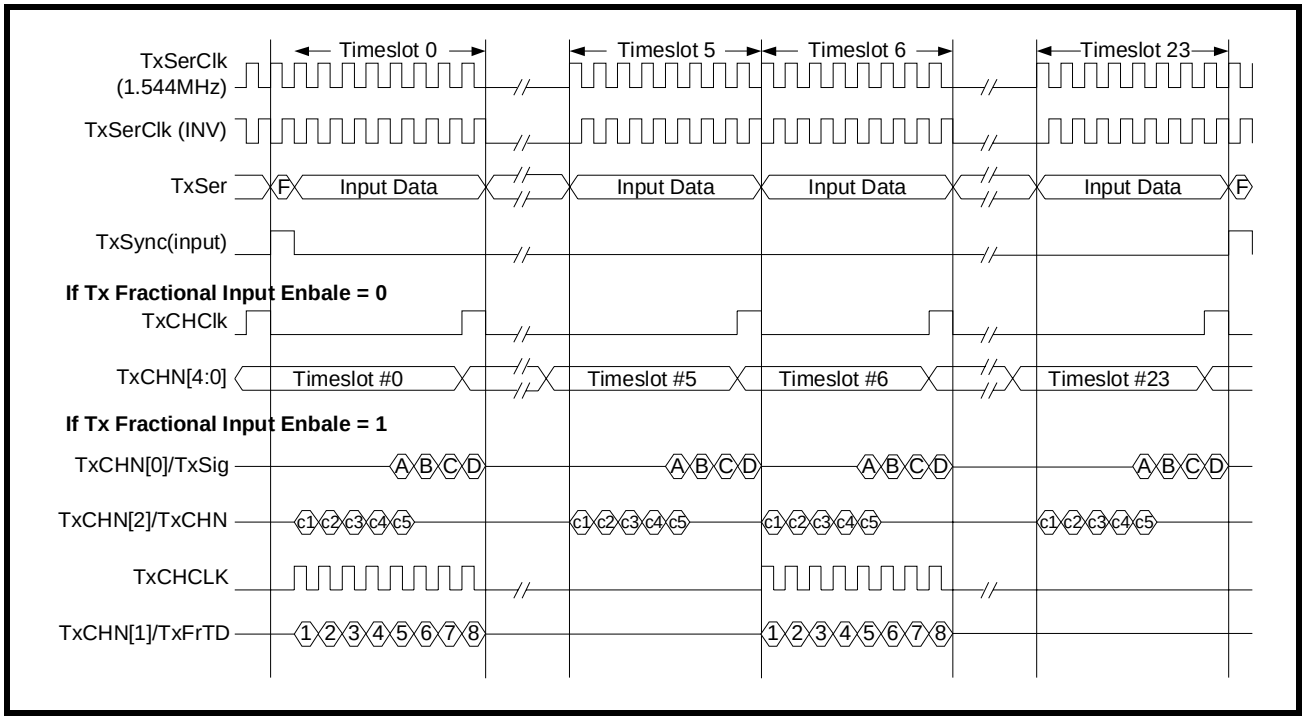
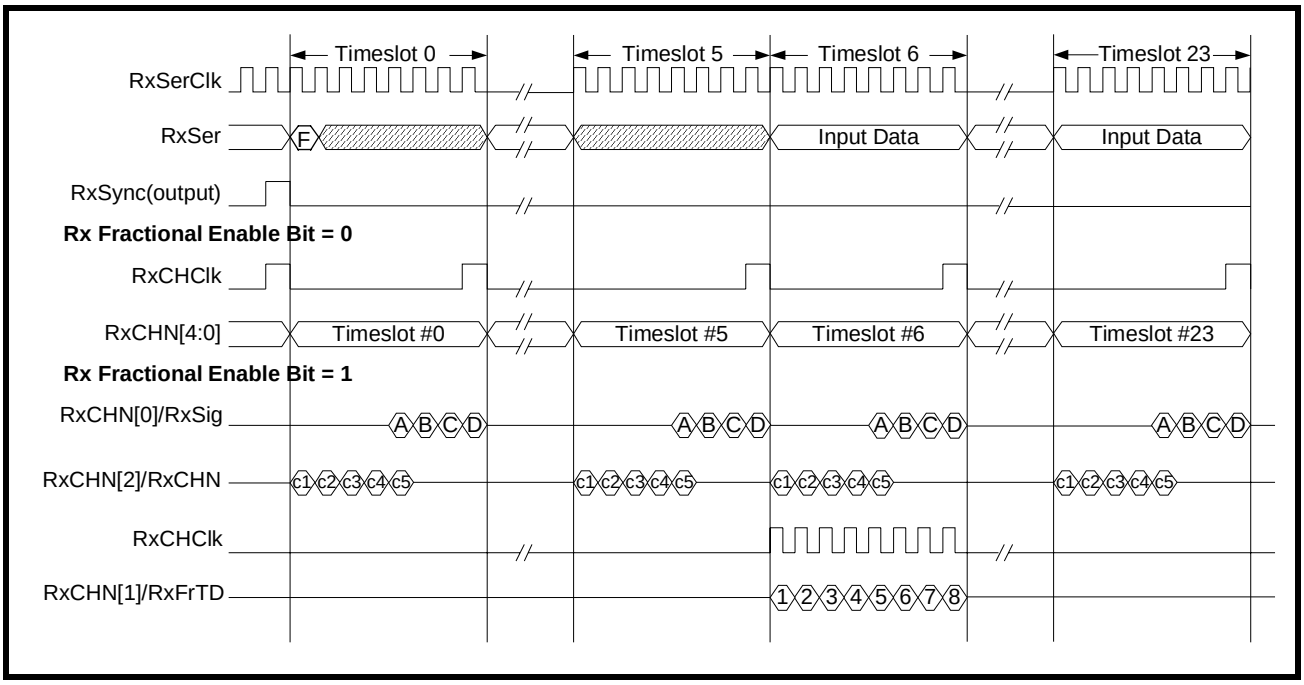


FIGURE 80. WAVEFORMS FOR CONNECTING THE RECEIVE PAYLOAD DATA INPUT INTERFACE BLOCK TO LOCAL TERMINAL EQUIPMENT



8.2 Transmit/Receive High-Speed Back-Plane Interface

The High-speed Back-plane Interface supports payload data to be taken from or presented to the Terminal Equipment at different data rates. In the non-multiplexed mode, payload data of each channel are interfaced to the Terminal Equipment separately. Each channel uses its own serial clock, serial data, single-frame synchronization signal and multi-frame synchronization signals.

8.2.1 T1 Transmit/Receive Interface - MVIP 2.048 MHz

The Back-plane interface is processing data at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment should pump in data grouped in 256-bit frame 8000 times every second. Each frame consists of thirty-two octets as in E1. The local Terminal Equipment maps a 193-bit T1 frame into this 256-bit format as described below:

1. The Framing (F-bit) is mapped into MSB of the first E1 Time-slot. The local Terminal Equipment will stuff the other seven bits of the first octet with don't care bits that would be ignored by the framer.
2. Payload data of T1 Time-slot 0, 1 and 2 are mapped into E1 Time-slot 1, 2 and 3.
3. The local Terminal Equipment will stuff E1 Time-slot 4 with eight don't care bits that would be ignored by the framer.
4. Following the same rules of Step 2 and 3, the local Terminal Equipment maps every three time-slots of T1 payload data into four E1 time-slots.

The mapping of T1 frame into E1 framing format is shown in the table below.

TABLE 6: MAPPING A T1 FRAME INTO AN E1 FRANE

T1	F-Bit	TS0	TS1	TS2	Don't Care Bits	TS3	TS4	TS5
E1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
T1	Don't Care Bits	TS6	TS7	TS8	Don't Care Bits	TS9	TS10	TS11
E1	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
T1	Don't Care Bits	TS12	TS13	TS14	Don't Care Bits	TS15	TS16	TS17
E1	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
T1	Don't Care Bits	TS18	TS19	TS20	Don't Care Bits	TS21	TS22	TS23
E1	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

8.2.2 Non-Multiplexed High-Speed Mode

When the Back-plane interface data rate is MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s, the interface signals are all configured as inputs, except the receive serial data on RxSER and the multi frame sync pulse (RxMSYNC) provided by the framer. The Transmit Serial Clock for each channel is always an input clock with frequency of 1.544 MHz for all data rates so that it may be used as the timing reference for the transmit line rate. The TxMSYNC signal is configured as the Transmit Input Clock with frequencies of 2.048 MHz, 4.096 MHz and 8.192 MHz respectively. It serves as the primary clock source for the High-speed Back-plane Interface. **Figure 81** shows how to connect the Transmit non-multiplexed high-speed Input Interface block to local Terminal Equipment. **Figure 82** shows how to connect the Receive non-multiplexed high-speed Output Interface to local Terminal Equipment.

FIGURE 81. TRANSMIT NON-MULTIPLEXED HIGH-SPEED CONNECTION TO LOCAL TERMINAL EQUIPMENT USING MVIP 2.048MBIT/S, 4.096MBIT/S, OR 8.192MBIT/S

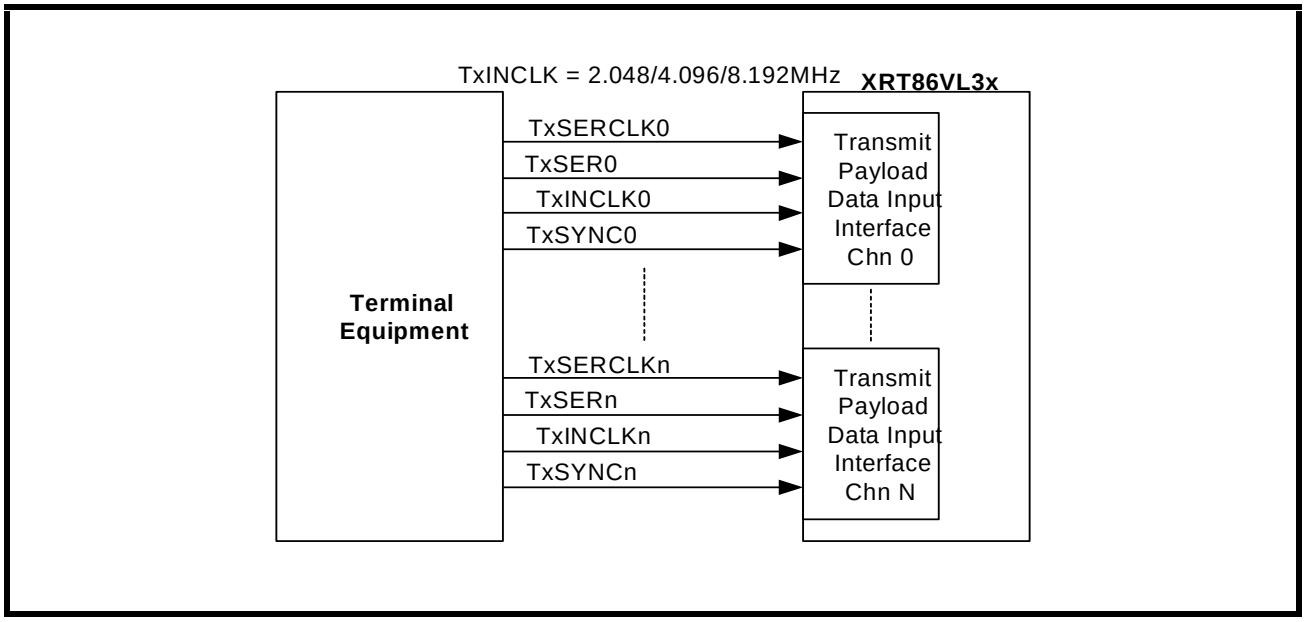


FIGURE 82. RECEIVE NON-MULTIPLEXED HIGH-SPEED CONNECTION TO LOCAL TERMINAL EQUIPMENT USING MVIP 2.048MBIT/S, 4.096MBIT/S, OR 8.192MBIT/S

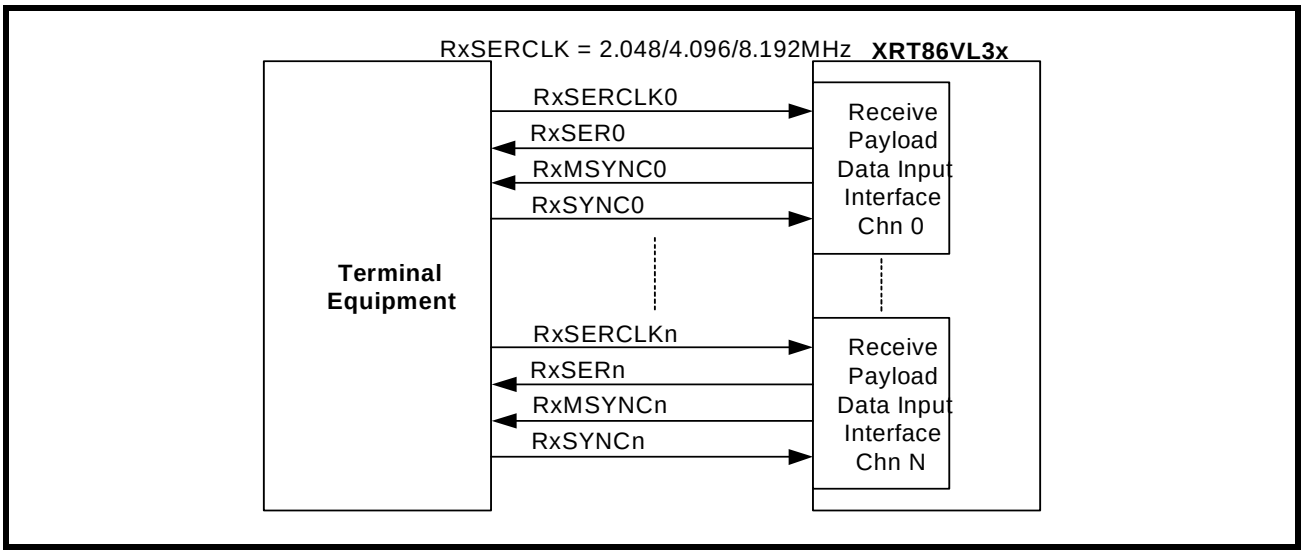


Figure 83 shows the waveforms for connecting the Transmit non-multiplexed high-speed Input Interface block to local Terminal Equipment. **Figure 84** shows the waveforms for connecting the Receive non-multiplexed high-speed Input Interface block to local Terminal Equipment.

FIGURE 83. WAVEFORMS FOR CONNECTING THE TRANSMIT NON-MULTIPLEXED HIGH-SPEED INPUT INTERFACE AT MVIP 2.048MBIT/S, 4.096MBIT/S, AND 8.192MBIT/S

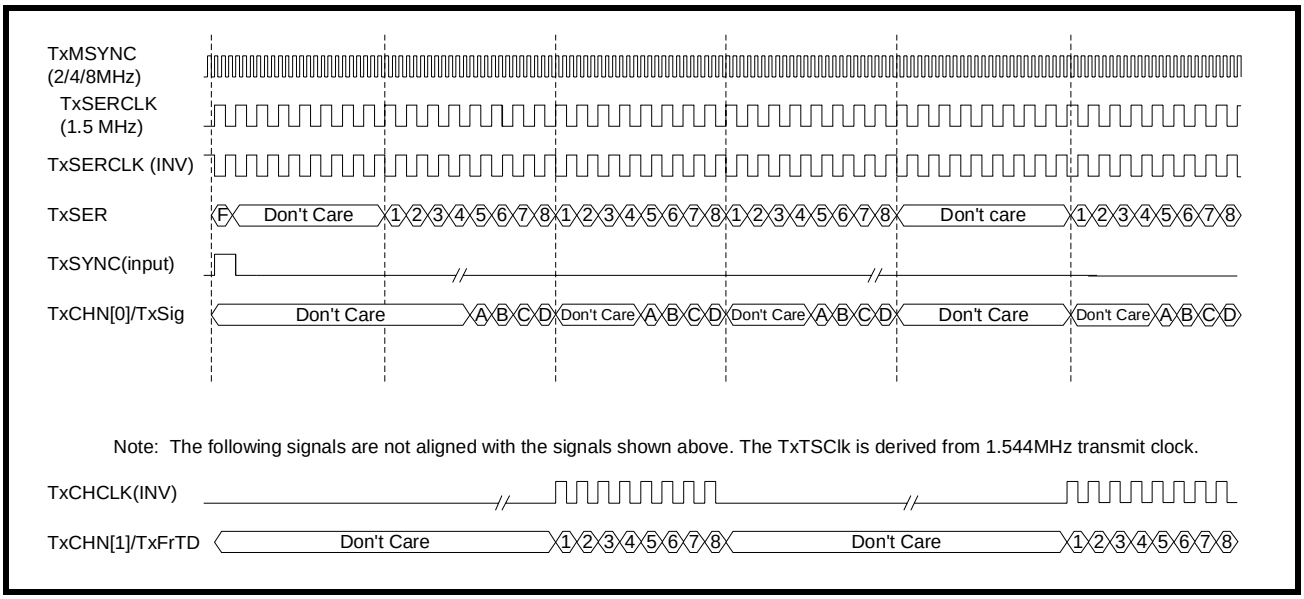
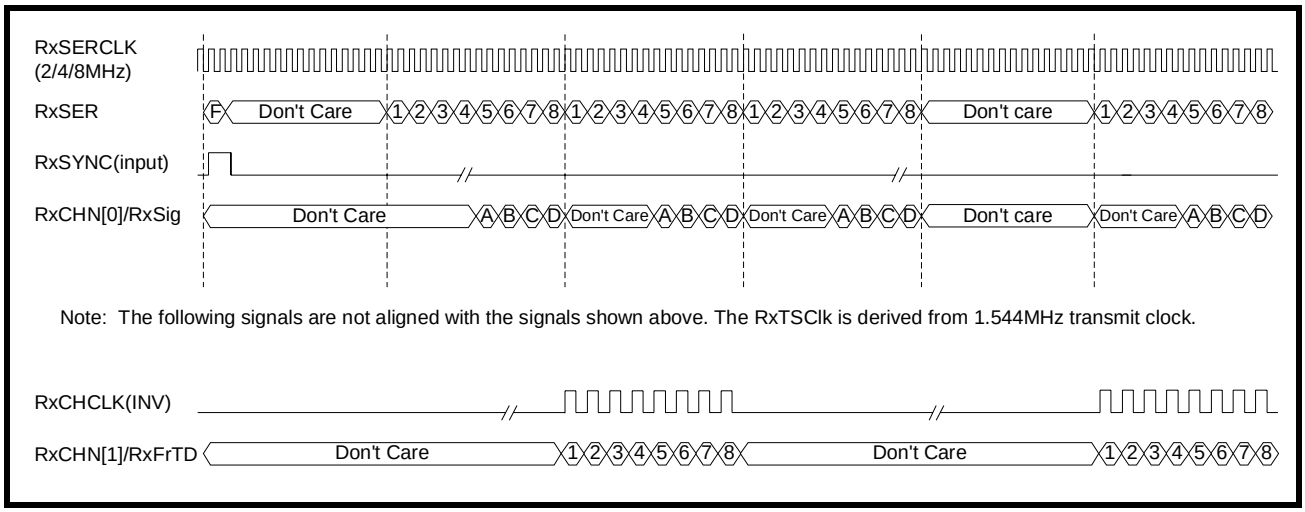


FIGURE 84. WAVEFORMS FOR CONNECTING THE RECEIVE NON-MULTIPLEXED HIGH-SPEED INPUT INTERFACE AT MVIP 2.048MBIT/S, 4.096MBIT/S, AND 8.192MBIT/S



8.2.3 Multiplexed High-Speed Mode

When the Back-plane interface data rate is 12.352Mbit/s, 16.384Mbit/s, HMVIP 16.384Mbit/s, and H.100 16.384Mbit/s, the interface signals are all configured as inputs, except the receive serial data on RxSER and the multi frame sync pulse provided by the framer. The Back-plane Interface is processing data through TxSER0 or TxSER4 pins at 12.352Mbit/s or 16.384Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one serial data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4. Free-running clocks of 12.352MHz are supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

Transmit 12.352 Bit-Multiplexed Mode

The local Terminal Equipment maps four 1.544Mbit/s DS1 data streams into one 12.352Mbit/s serial data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

BIT PATTERN OF THE FIRST OCTET

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last. After the first bits of Timeslot 0 of all four

channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 12.352Mbit/s data stream.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_3	1_3

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

X_Y: The Xth payload bit of Channel Y

3. The local Terminal Equipment also multiplexes signaling bits with payload bits and sends them together through the 12.352Mbit/s data stream. When the Terminal Equipment is sending the fifth payload bit of each channel, instead of sending it twice, it inserts the signaling bit A of that corresponding channel. Similarly, the sixth payload bit of a each channel is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 12.352Mbit/s data stream.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

4. Following the same rules of Step 2 and 3, the local Terminal Equipment continues to map the payload data and signaling data of four channels into a 12.352Mbit/s data stream.

The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position (F-bit of channel 0) of the multiplexed data stream with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position (F-bit of Channel 4) of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed DS1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT86VL3x and sent to each individual channel. These data will be processed by each individual framer and send to the LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device. **Figure 85** shows how to connect the Transmit multiplexed high-speed Input Interface block to local Terminal Equipment. **Figure 89** shows the timing signal when the transmit framer is running at 12.352 Bit-Multiplexed Mode

FIGURE 85. INTERFACING XRT86VL3X TRANSMIT TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S, HMVIP 16.384MBIT/S, AND H.100 16.384MBIT/S

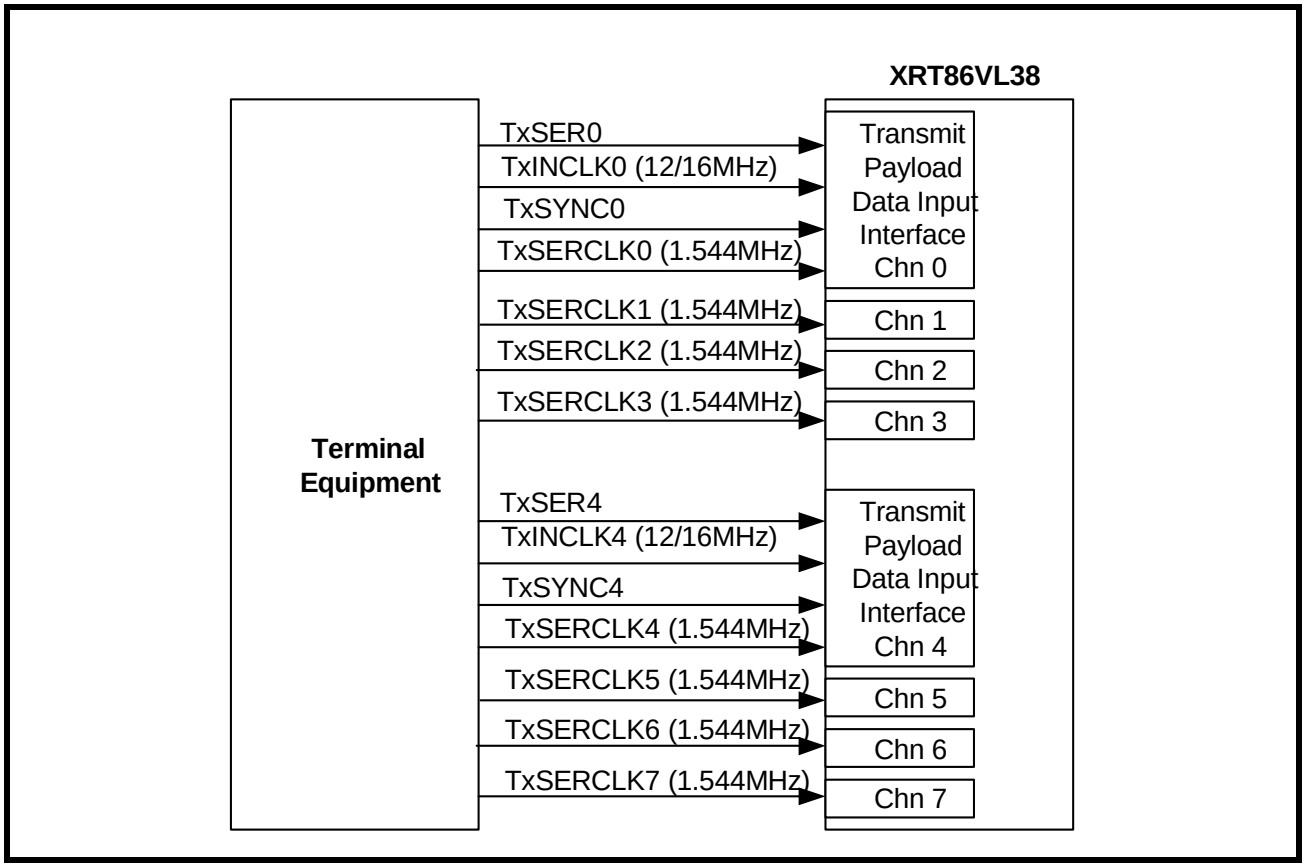
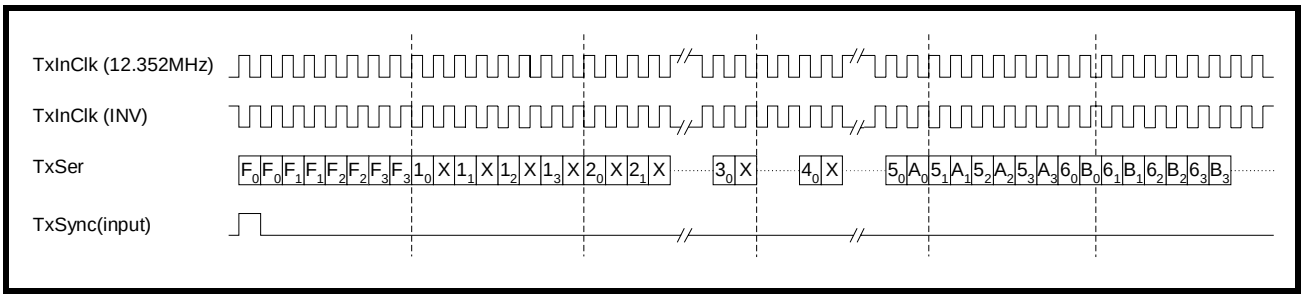


FIGURE 86. TIMING SIGNALS WHEN THE TRANSMIT FRAMER IS RUNNING AT 12.352 BIT-MULTIPLEXED MODE



Transmit 16.384 Bit-Multiplexed Mode

Please refer to Figure 85 for how to interface the transmit payload data input interface block to the terminal equipment. The local Terminal Equipment maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. After the first octet of data is sent, the local Terminal Equipment should insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.
3. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last. After the first bits of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_3	1_3

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

X_Y: The Xth payload bit of Channel Y

4. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream. When the Terminal Equipment is sending the fifth payload bit of each channel, instead of sending it twice, it inserts the signaling bit A of that corresponding channel. Similarly, the sixth payload bit of each channel is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

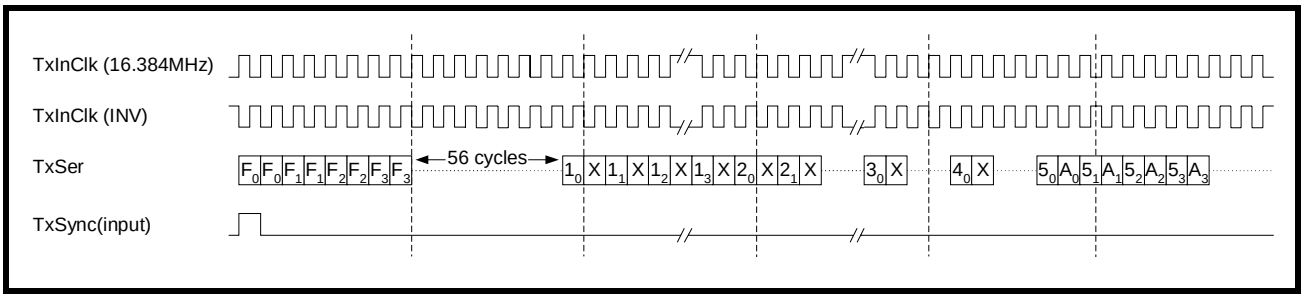
5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Terminal Equipment should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, the local Terminal Equipment stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position (F-bit of channel 0) of the data stream with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position (F-bit of Channel 4) of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed DS1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT86VL3x and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

Figure shows the timing signal when the transmit framer is running at 16.384 Bit-Multiplexed mode.

FIGURE 87. TIMING SIGNALS WHEN THE TRANSMIT FRAMER IS RUNNING AT 16.384 BIT-MULTIPLEXED MODE



Transmit HMVIP / H.100 Byte-Multiplexed mode at 16.384 MHz

Please refer to Figure 85 for how to interface the transmit payload data input interface block to the terminal equipment. The local Terminal Equipment maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. After the first octet of data is sent, the local Terminal Equipment should insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.
3. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last. After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

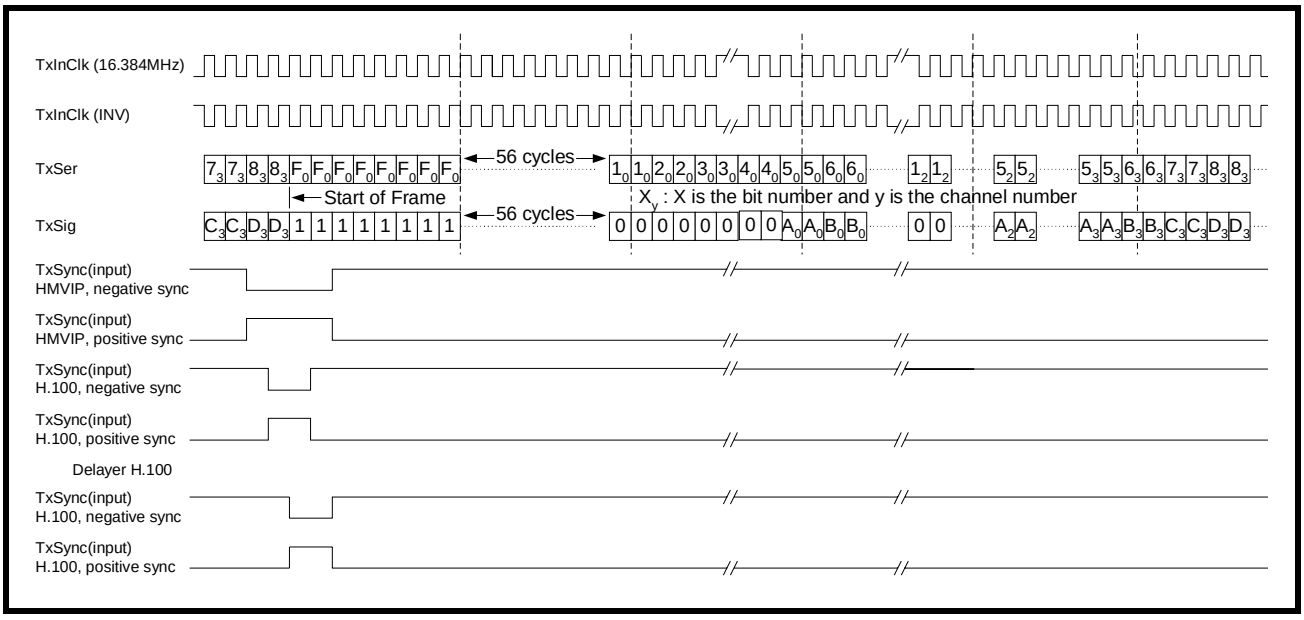
X_Y: The Xth payload bit of Channel Y

4. When the framer is running at HMVIP 16.384MBit/s byte-mulitplexed mode, signaling information is inserted from the TxSig/TxCHN[0] pin or from the TSCR register (0xn340-n357). When the local terminal is sending the fifth payload bit of one channel, signaling bit A of that corresponding channel is repeated and sent through the TxSig/TxCHN[0] pin; Similarly, signaling bit B, C, and D of the corresponding channel is repeated and sent through the TxSig/TxCHN[0] pin when the local terminal is providing the sixth, seventh, and eighth payload bit respectively, as shown in **Figure** .
5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Terminal Equipment should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, the local Terminal Equipment stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

For HMVIP mode, the Transmit Single-frame Synchronization signal should pulse HIGH for four clock cycles (the last two bit positions of the previous multiplexed frame and the first two bits of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. For H.100 mode, TxSYNC should pulse HIGH for two clock cycles (the last bit position of the previous multiplexed frame and the first bit of the next multiplexed frame). The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH to identify the start of multiplexed data stream of Channel 4-7. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed DS1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT86VL3x and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

FIGURE 88. TIMING SIGNALS WHEN THE TRANSMIT FRAMER IS RUNNING AT HMVIP / H.100 16.384MHZ MODE



T1 Receive Multiplexed Mode

The interface consists of the following pins:

- Data Output (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 12.352Mbit/s or 16.384Mbit/s. It multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 12.352MHz or 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock. Figure 89 shows the interface of the Recieve Payload Data Output Interface Block to the Terminal Equipment.

The multiplexed data output on RxSER_0 or RxSER_4 are very similar to the Multiplexed data input on TxSER_0 or TxSER_4 except when the receive framer is running at 12.352MHz or 16.384MHz Bit-Multiplexed mode. When the receive framer is running at 12MHz or 16MHz Bit-Multiplexed mode, the multiplexed data on RxSER_0 or RxSER_4 are return-to-zero data when the receive framer is processing the first four bits of each time slot data of each channel, as shown in Figure 90 and Figure 91. Figure 92 shows the timing signal when the receive framer is running at HMVIP or H.100 16.384 MHz mode.

FIGURE 89. INTERFACING XRT86VL3X RECEIVE TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S, HMVIP 16.384MBIT/S, AND H.100 16.384MBIT/S

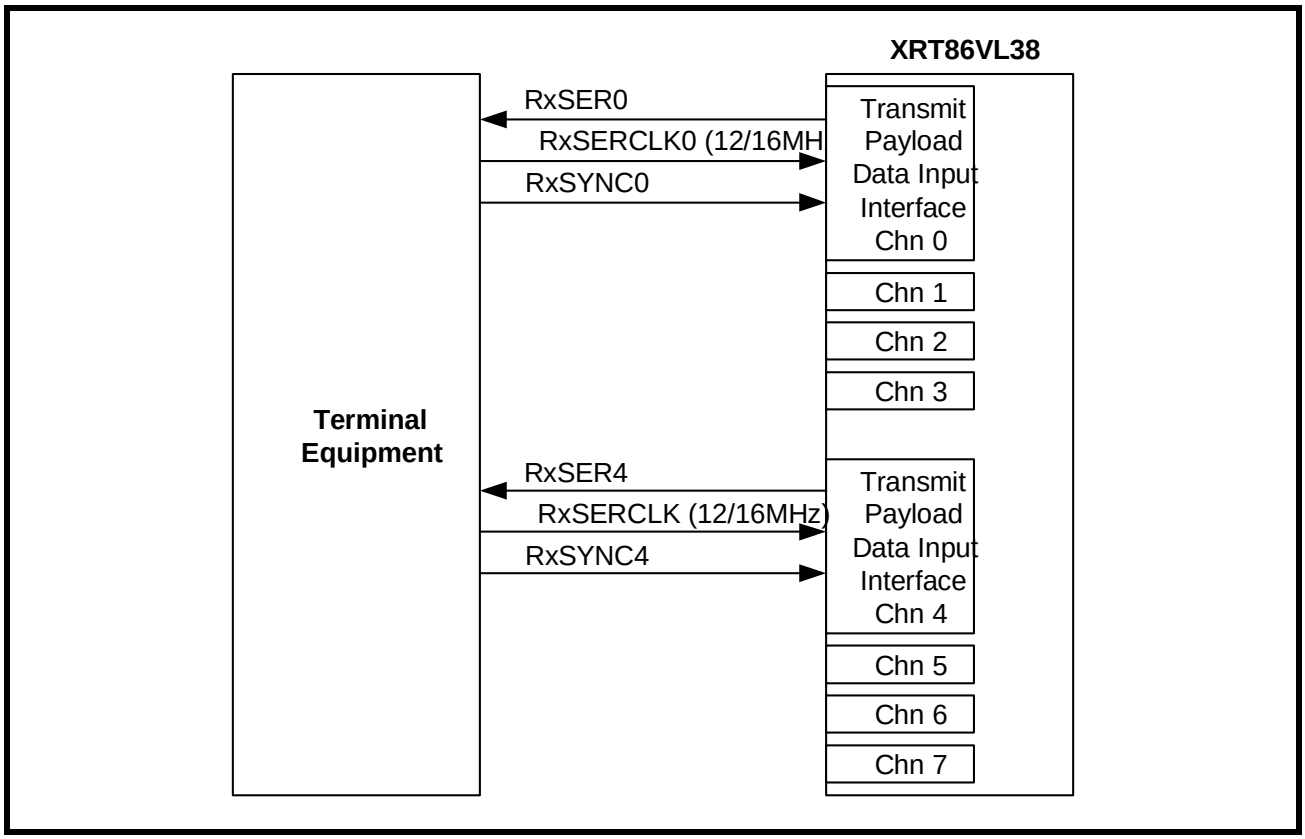


FIGURE 90. WAVEFORMS FOR CONNECTING THE RECEIVE MULTIPLEXED HIGH-SPEED INPUT INTERFACE AT 12.352MBIT/S MODE

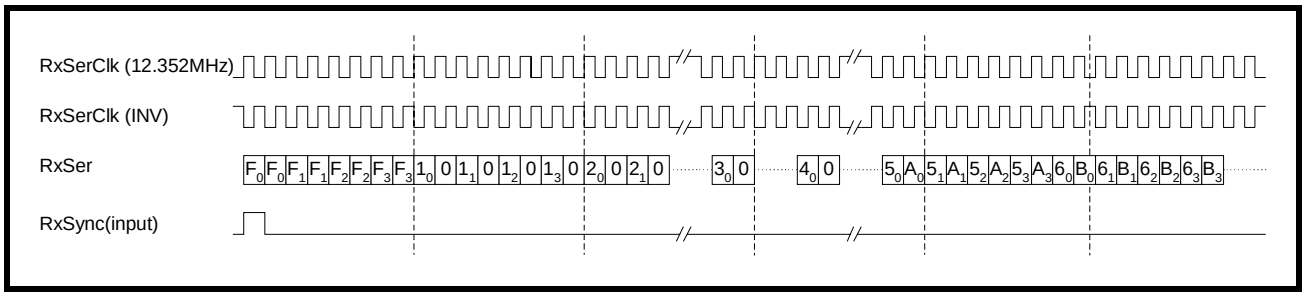


FIGURE 91. WAVEFORMS FOR CONNECTING THE RECEIVE MULTIPLEXED HIGH-SPEED INPUT INTERFACE AT 16.384MBIT/S MODE

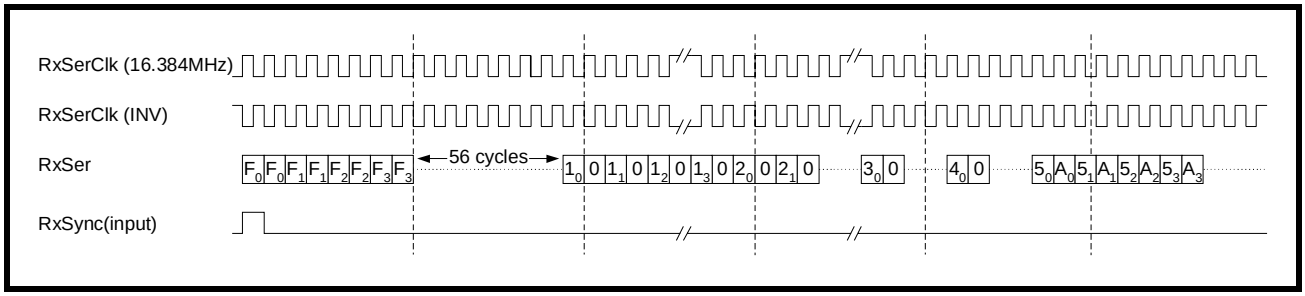
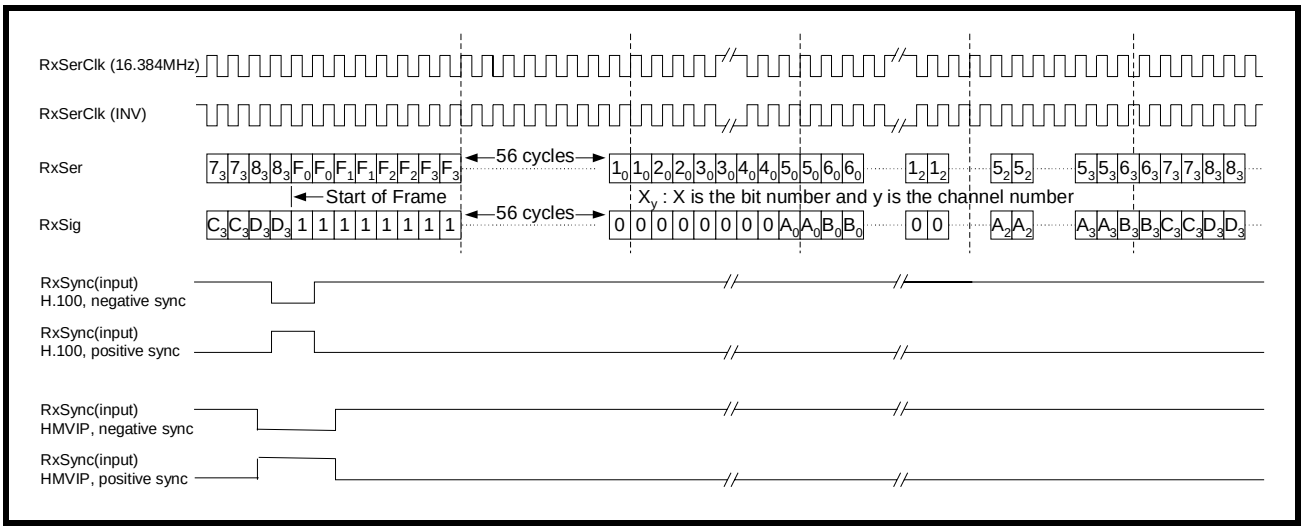


FIGURE 92. WAVEFORMS FOR CONNECTING THE RECEIVE MULTIPLEXED HIGH-SPEED INPUT INTERFACE AT HMVIP AND H.100 16.384MBIT/S MODE



8.3 Brief Discussion of Robbed-bit Signaling in DS1 Framing Format

Signaling is required when dealing with voice and dial-up data services in DS1 applications. Traditionally, signaling is provided on a dial-up telephone line, across the talk-path. Bit robbing, or stealing the least significant bit (8th bit) in each of the twenty-four voice channels in the signaling frames allows enough bits to signal between the transmitting and receiving end. That is where the name Robbed-bit signaling comes from. These ends can be CPE to central office (CO) for switched services, or CPE to CPE for PBX-to-PBX connections.

Signaling is used to tell the receiver where the call or route is destined. The signal is sent through switches along the route to a distant end. Common types of signals are:

- On hook
- Off hook
- Dial tone
- Dialed digits
- Ringing cycle
- Busy tone

Robbed-bit Signaling is supported in three DS1 framing formats.

- Super-Frame (SF)
- SLC®96
- Extended Super-Frame (ESF)

In Super-Frame or SLC®96 framing mode, frame number 6 and frame number 12 are signaling frames. In channelized DS1 applications, these frames are used to contain the signaling information. In frame number 6 and 12, the least significant bit of all twenty-four timeslots is 'robbed' to carry call state information. The bit in frame 6 is called the A bit and the bit in frame 12 is called the B bit. The combination of A and B defines the state of the call for the particular timeslot that these two bits are located in.

FRAME NUMBER	SIGNALING BIT
6	A
12	B

In Extended Super-Frame framing mode, frame number 6, 12, 18 and 24 are signaling frames. In these frames, the least significant bit of all twenty-four timeslots is 'robbed' to carry call state information. The bit in frame 6 is called the A bit, the bit in frame 12 is called the B bit, the bit in frame 18 is called the C bit and the bit in frame 24 is called the D bit. The combination of A, B, C and D defines the state of the call for the particular timeslot that these signaling bits are located in.

FRAME NUMBER	SIGNALING BIT
6	A
12	B
18	C
24	D

8.3.1 Configure the framer to transmit Robbed-bit Signaling

The XRT86VL3x framer supports transmission of Robbed-bit Signaling in ESF, SF and SLC®96 framing formats. Signaling bits can be inserted into the outgoing DS1 frame through the following:

- Signaling data is inserted from Transmit Signaling Control Registers (TSCR) of each timeslot
- Signaling data is inserted from TxSig_n pin
- Signaling data is embedded into the input PCM data coming from the Terminal Equipment

8.3.2 Insert Signaling Bits from TSCR Register

The four most significant bits of the Transmit Signaling Control Register (TSCR) of each timeslot can be used to store outgoing signaling data. The user can program these bits through the microprocessor access. If the XRT86VL3x framer is configured to insert signaling bits from the TSCR registers, the DS1 Transmit Framer block will strip off the least significant bits of each time slot in the signaling frames and replace it with the signaling bit stored inside the TSCR registers. The insertion of signaling bits into PCM data is done on a per-channel basis.

In SF or SLC®96 mode, the user can control the XRT86VL3x framer to transmit no signaling (transparent), two-code signaling, or four-code signaling. Two-code signaling is done by substituting the least significant bit (LSB) of the specific channel in frame 6 and 12 with the content of the Signaling bit A of the specific TSCR register.

Four-code signaling is done by substituting the LSB of channel data in frame 6 with the Signaling bit A and the LSB of channel data in frame 12 with the Signaling bit B of the specific channel's TSCR register. If sixteen-code signaling is selected in SF format, only the Signaling bit A and Signaling bit B information are used.

In ESF mode, the user can control the XRT86VL3x framer to transmit no signaling (transparent) by disable signaling insertion, two-code signaling, four-code signaling or sixteen code signaling. Two-code signaling is done by substituting the least significant bit (LSB) of the specific channel in frame 6, 12, 18 and 24 with the content of the Signaling bit A of the specific TSCR register.

Four-code signaling is done by substituting the LSB of channel data in frame 6 and frame 18 with the Signaling bit A and the LSB of channel data in frame 12 and frame 24 with the Signaling bit B of the specific channel's TSCR register.

Sixteen-code signaling is implemented by substituting the LSB of channel data in frames 6, 12, 18, and 24 with the content of Signaling bit A, B, C, and D of TSCR register respectively.

In N or T1DM modes, no robbed-bit signaling is allowed and the transmit data stream remains intact.

The table below shows the four most significant bits of the Transmit Signaling Control Register.

TRANSMIT SIGNALING CONTROL REGISTER (TSCR) (ADDRESS = 0XN340H - 0XN357H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Signaling Bit A	R/W	This bit is used to store Signaling Bit A that is sent as the least significant bit of timeslot of frame number 6.
6	Signaling Bit B	R/W	This bit is used to store Signaling Bit B that is sent as the least significant bit of timeslot of frame number 12.
5	Signaling Bit C	R/W	This bit is used to store Signaling Bit C that is sent as the least significant bit of timeslot of frame number 18.
4	Signaling Bit D	R/W	This bit is used to store Signaling Bit D that is sent as the least significant bit of timeslot of frame number 24.

8.3.3 Insert Signaling Bits from TxSig_n Pin

The XRT86VL3x framer can be configured to insert signaling bits provided by external equipment through the TxSig_n pins. This pin is a multiplexed I/O pin with two functions:

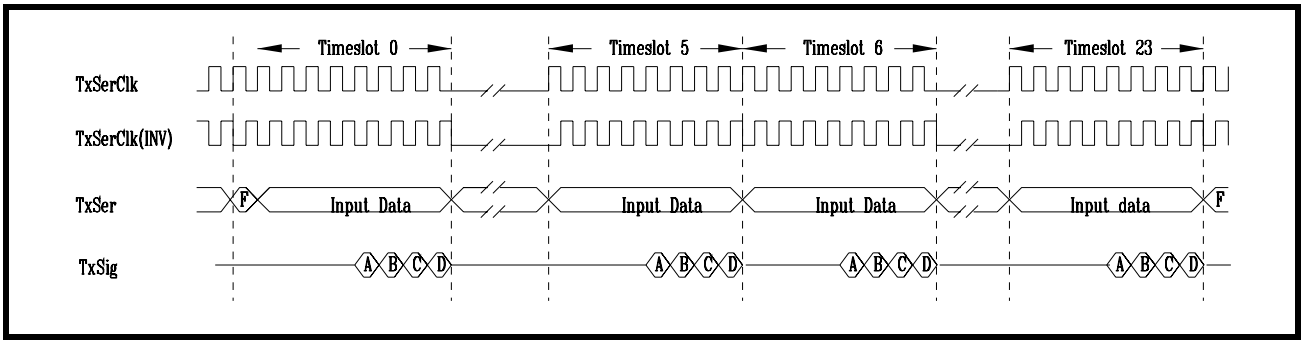
- TxCHN[0]_n - Transmit Timeslot Number Bit [0] Output pin
- TxSig_n - Transmit Signaling Input pin

When the Transmit Fractional DS1 bit of the Transmit Interface Control Register (TICR) is set to 0, this pin is configured as TxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the DS1 PCM data that is transmitting.

When the Transmit Fractional DS1 bit of the Transmit Interface Control Register (TICR) is set to 1, this pin is configured as TxSig_n pin, it acts as an input source for the signaling bits to be transmitted in the outbound DS1 frames.

Figure 93 below is a timing diagram of the TxSig_n input pin. Please note that the Signaling Bit A of a certain timeslot coincides with Bit 4 of the PCM data; Signaling Bit B coincides with Bit 5 of the PCM data; Signaling Bit C coincides with Bit 6 of the PCM data and Signaling Bit D coincides with Bit 7 (LSB) of the PCM data.

FIGURE 93. TIMING DIAGRAM OF THE TXSIG_N INPUT



The table below shows configurations of the Transmit Fractional DS1 bit of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR)(ADDRESS = 0XN120H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Transmit Fractional DS1	R/W	This READ/WRITE bit-field permits the user to determine which one of the two functions the multiplexed I/O pin of TxTSb[0]_n/TxSig_n is spotting. 0 - This pin is configured as TxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the DS1 PCM data that is transmitting. 1 - This pin is configured as TxSig_n pin, it acts as an input source for the signaling bits to be transmitted in the outbound DS1 frames

9.0 ALARMS AND ERROR CONDITIONS

The XRT86VL3x T1/J1/E1 Framer can be configured to monitor quality of received DS1 frames. It can generate error indicators if the local receive framer has received error frames from the remote terminal. If corresponding interrupt is enabled, the local microprocessor operation is interrupted by these error conditions. Upon microprocessor interruption, the user can intervene by looking into the error conditions.

At the same time, the user can configure the XRT86VL3x framer to transmit alarms and error indications to remote terminal. Different alarms and error indications will be transmitted depending on the error condition.

The section below gives a brief discussion of the error conditions that can be detected by the XRT86VL3x framer and error indications that will be generated.

9.1 AIS Alarm

As we discussed before, transmission of Alarm Indication Signal (AIS) or Blue Alarm by the intermediate node indicates that the equipment is still functioning but unable to offer services. It is an all ones (except for framing bits) pattern which can be used by the equipment further down the line to maintain clock recovery and timing synchronization.

The XRT86VL3x framer can detect two types of AIS in DS1 mode:

- Framed AIS
- Unframed AIS

Unframed AIS is an all ones pattern. If unframed AIS is sent, the equipment further down the line will be able to maintain timing synchronization and be able to recover clock from the received AIS signal. However, due to the lack of framing bits, the equipment farther down the line will not be able to maintain frame synchronization and will declare Loss of Frame (LOF).

On the other hand, the payload portion of a framed AIS pattern is all ones. However, a framed AIS pattern still has correct framing bits. Therefore, the equipment further down the line can still maintain frame synchronization as well as timing synchronization. In this case, no LOF or Red alarm will be declared.

The Alarm indication logic within the Receive Framer block of the XRT86VL3x framer monitors the incoming DS1 frames for AIS. AIS alarm condition are detected and declared according to the following procedure:

1. The incoming DS1 frames are monitored for AIS detection. AIS detection is defined as an unframed or framed pattern with less than three zeros in two consecutive frames.
2. An AIS detection counter within the Receive Framer block of the XRT86VL3x counts the occurrences of AIS detection over a 6 ms interval. It will indicate a valid AIS flag when twenty-two or more of a possible twenty-four AIS are detected.
3. Each 6 ms interval with a valid AIS flag increments a flag counter which declares AIS alarm when 255 valid flags have been collected.

Therefore, AIS condition has to be persisted for 1.53 seconds before AIS alarm condition is declared by the XRT86VL3x framer.

If there is no valid AIS flag over a 6ms interval, the Alarm indication logic will decrement the flag counter. The AIS alarm is removed when the counter reaches 0. That is, AIS alarm will be removed if over 1.53 seconds, there is no valid AIS flag.

The Alarm Indication Signal Detection Select bits of the Alarm Generation Register (AGR) enable the two types of AIS detection that are supported by the XRT86VL3x framer. The table below shows configurations of the Alarm Indication Signal Detection Select bits of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR) (ADDRESS = 0XN108H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	AIS Detection Select	R/W	00 - AIS alarm detection is disabled.When this bit is set to 01:Detection of unframed AIS alarm of all ones pattern is enabled. 10 - AIS alarm detection is disabled.When this bit is set to 00:Detection of framed AIS alarm of all ones pattern except for framing bits is enabled.

If detection of unframed or framed AIS alarm is enabled by the user and if AIS is present in the incoming DS1 frame, the XRT86VL3x framer can generate a Receive AIS State Change interrupt associated with the setting of Receive AIS State Change bit of the Alarm and Error Status Register to one.

To enable the Receive AIS State Change interrupt, the Receive AIS State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) have to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive AIS State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive AIS State Change Interrupt Enable	R/W	0 - The Receive AIS State Change interrupt is disabled. 1 - The Receive AIS State Change interrupt is enabled.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and AIS is present in the incoming DS1 frame, the XRT86VL3x framer will declare AIS by doing the following:

- Set the read-only Receive AIS State bit of the Alarm and Error Status Register (AESR) to one indicating there is AIS alarm detected in the incoming DS1 frame.
- Set the Receive AIS State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of AIS. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive AIS State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive AIS State Change	RUR / WC	0 - There is no change of AIS state in the incoming DS1 payload data. 1 - There is change of AIS state in the incoming DS1 payload data.

The Receive AIS State bit of the Alarm and Error Status Register (AESR), on the other hand, is a read-only bit indicating there is AIS alarm detected in the incoming DS1 frame.

The table below shows the Receive AIS State status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Receive AIS State	R	0 - There is no AIS alarm condition detected in the incoming DS1 payload data. 1 - There is AIS alarm condition detected in the incoming DS1 payload data.

9.2 Red Alarm

The Alarm indication logic within the Receive Framer block of the XRT86VL3x framer monitors the incoming DS1 frames for red alarm or Loss of Frame (LOF) condition. Red alarm condition are detected and declared according to the following procedure:

1. The red alarm is detected by monitoring the occurrence of Loss of Frame (LOF) over a 6 ms interval.
2. An LOF valid flag will be posted on the interval when one or more LOF occurred during the interval.
3. Each interval with a valid LOF flag increments a flag counter which declares RED alarm when 63 valid intervals have been accumulated.
4. An interval without valid LOF flag decrements the flag counter. The Red alarm is removed when the counter reaches zero.

If LOF condition is present in the incoming DS1 frame, the XRT86VL3x framer can generate a Receive Red Alarm State Change interrupt associated with the setting of Receive Red Alarm State Change bit of the Alarm and Error Status Register to one.

To enable the Receive Red Alarm State Change interrupt, the Receive Red Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Red Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Red Alarm State Change Interrupt Enable	R/W	0 - The Receive Red Alarm State Change interrupt is disabled. No Receive Red Alarm interrupt will be generated upon detection of Red Alarm condition. 1 - The Receive Red Alarm State Change interrupt is enabled. Receive Red Alarm interrupt will be generated upon detection of Red Alarm condition.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and Red Alarm is present in the incoming DS1 frame, the XRT86VL3x framer will declare Red Alarm by doing the following:

- Set the read-only Receive Red Alarm State bit of the Alarm and Error Status Register (AESR) to one indicating there is Red Alarm detected in the incoming DS1 frame.
- Set the Receive Red Alarm State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of Red Alarm. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Red Alarm State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Red Alarm State Change	RUR / WC	0 - There is no change of Red Alarm state in the incoming DS1 payload data. 1 - There is change of Red Alarm state in the incoming DS1 payload data.

The Receive Red Alarm State bit of the Alarm and Error Status Register (AESR), on the other hand, is a read-only bit indicating there is Red Alarm detected in the incoming DS1 frame.

The table below shows the Receive Red Alarm State status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Red Alarm State	R	0 - There is no Red Alarm condition detected in the incoming DS1 payload data. 1 - There is Red Alarm condition detected in the incoming DS1 payload data.

9.3 Yellow Alarm

The Alarm indication logic within the Receive Framer block of the XRT86VL3x framer monitors the incoming DS1 frames for Yellow Alarm condition. The yellow alarm is detected and declared according to the following procedure:

1. Monitor the occurrence of Yellow Alarm pattern over a 6 ms interval. A YEL valid flag will be posted on the interval when Yellow Alarm pattern occurred during the interval.
2. Each interval with a valid YEL flag increments a flag counter which declares YEL alarm when 80 valid intervals have been accumulated.
3. An interval without valid YEL flag decrements the flag counter. The YEL alarm is removed when the counter reaches zero.

If Yellow Alarm condition is present in the incoming DS1 frame, the XRT86VL3x framer can generate a Receive Yellow Alarm State Change interrupt associated with the setting of Receive Yellow Alarm State Change bit of the Alarm and Error Status Register to one.

To enable the Receive Yellow Alarm State Change interrupt, the Receive Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Receive Yellow Alarm State Change Interrupt Enable	R/W	0 - The Receive Yellow Alarm State Change interrupt is disabled. Any state change of Receive Yellow Alarm will not generate an interrupt. 1 - The Receive Yellow Alarm State Change interrupt is enabled. Any state change of Receive Yellow Alarm will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and Yellow Alarm is present in the incoming DS1 frame, the XRT86VL3x framer will declare Yellow Alarm by doing the following:

- Set the read-only Receive Yellow Alarm State bit of the Alarm and Error Status Register (AESR) to one indicating there is Yellow Alarm detected in the incoming DS1 frame.
- Set the Receive Yellow Alarm State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of Yellow Alarm. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Yellow Alarm State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR)(ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Receive Yellow Alarm State Change	RUR / WC	0 - There is no change of Yellow Alarm state in the incoming DS1 payload data. 1 - There is change of Yellow Alarm state in the incoming DS1 payload data.

The table below shows the Receive AIS State Change status bits of the Alarm and Error Status Register.

The Receive Yellow Alarm State bit of the Alarm and Error Status Register (AESR), on the other hand, is a read-only bit indicating there is Yellow Alarm detected in the incoming DS1 frame.

The table below shows the Receive Yellow Alarm State status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Yellow Alarm State	R	0 - There is no Yellow Alarm condition detected in the incoming DS1 payload data. 1 - There is Yellow Alarm condition detected in the incoming DS1 payload data.

9.4 Bipolar Violation

The line coding for the DS1 signal should be bipolar. That is, a binary "0" is transmitted as zero volts while a binary "1" is transmitted as either a positive or negative pulse, opposite in polarity to the previous pulse. A Bipolar Violation or BPV occurs when the alternate polarity rule is violated. The Alarm indication logic within the Receive Framer block of the XRT86VL3x framer monitors the incoming DS1 frames for Bipolar Violations.

If a Bipolar Violation is present in the incoming DS1 frame, the XRT86VL3x framer can generate a Receive Bipolar Violation interrupt associated with the setting of Receive Bipolar Violation bit of the Alarm and Error Status Register to one.

To enable the Receive Bipolar Violation interrupt, the Receive Bipolar Violation Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Bipolar Violation Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Bipolar Violation Interrupt Enable	R/W	0 - The Receive Bipolar Violation interrupt is disabled. Occurrence of one or more bipolar violations will not generate an interrupt. 1 - The Receive Bipolar Violation interrupt is enabled. Occurrence of one or more bipolar violations will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and one or more Bipolar Violations are present in the incoming DS1 frame, the XRT86VL3x framer will declare Receive Bipolar Violation by doing the following:

- Set the Receive Bipolar Violation bit of the Alarm and Error Status Register to one indicating there are one or more Bipolar Violations. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Bipolar Violation status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Bipolar Violation State Change	RUR / WC	0 - There is no change of Bipolar Violation state in the incoming DS1 payload data. 1 - There is change of Bipolar Violation state in the incoming DS1 payload data.

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (ADDRESS = 0XNB03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Loss of Signal Interrupt Enable	R/W	0 - The Receive Loss of Signal interrupt is disabled. Occurrence of Loss of Signals will not generate an interrupt. 1 - The Receive Loss of Signal interrupt is enabled. Occurrence of Loss of Signals will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (ADDRESS = 0XNB01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and one or more Loss of Signals are present in the incoming DS1 frame, the XRT86VL3x framer will declare Receive Loss of Signal by doing the following:

- Set the Receive Loss of Signal bit of the Alarm and Error Status Register to one indicating there is one or more Loss of Signals. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Loss of Signal status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (ADDRESS = 0XNB02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Loss of Signal State	RUR / WC	0 - There is no change of Loss of Signal state in the incoming DS1 payload data. 1 - There is change of Loss of Signal state in the incoming DS1 payload data.

9.5 E1 Brief discussion of alarms and error conditions

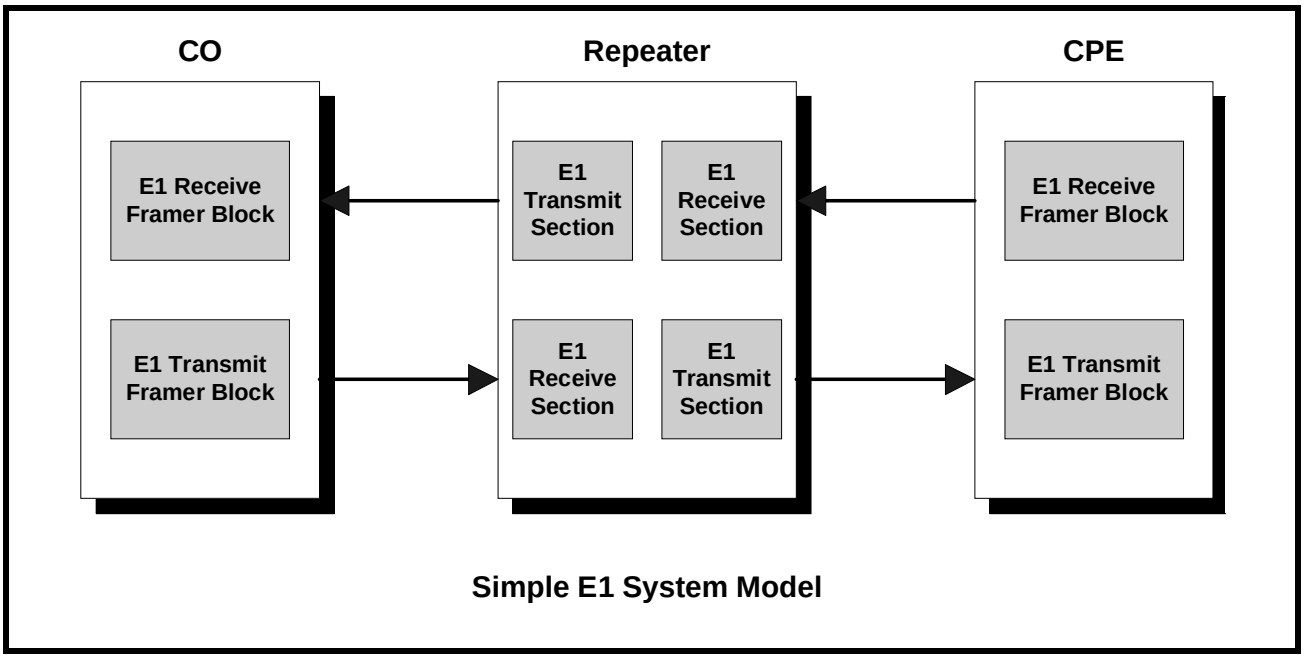
As defined in E1 specification, alarm conditions are created from defects. Defects are momentary impairments present on the E1 trunk. If a defect is present for a sufficient amount of time (called the integration time), then the defect becomes an alarm. Once an alarm is declared, the alarm is present until after the defect clears for a sufficient period of time. The time it takes to clear an alarm is called the de-integration time.

Alarms are used to detect and warn maintenance personnel of problems on the E1 trunk. There are three types of alarms:

- Red alarm or Service Alarm Indication (SAI) Signal
- Blue alarm or Alarm Indication Signal (AIS)
- Yellow alarm or Remote Alarm Indication (RAI) Signal

To explain the error conditions and generation of different alarms, let us create a simple E1 system model. In this model, an E1 signal is sourced from the Central Office (CO) through a Repeater to the Customer Premises Equipment (CPE). At the same time, an E1 signal is routed from the CPE to the Repeater and back to the Central Office. **Figure 94** below shows the simple E1 system model.

FIGURE 94. SIMPLE DIAGRAM OF E1 SYSTEM MODEL

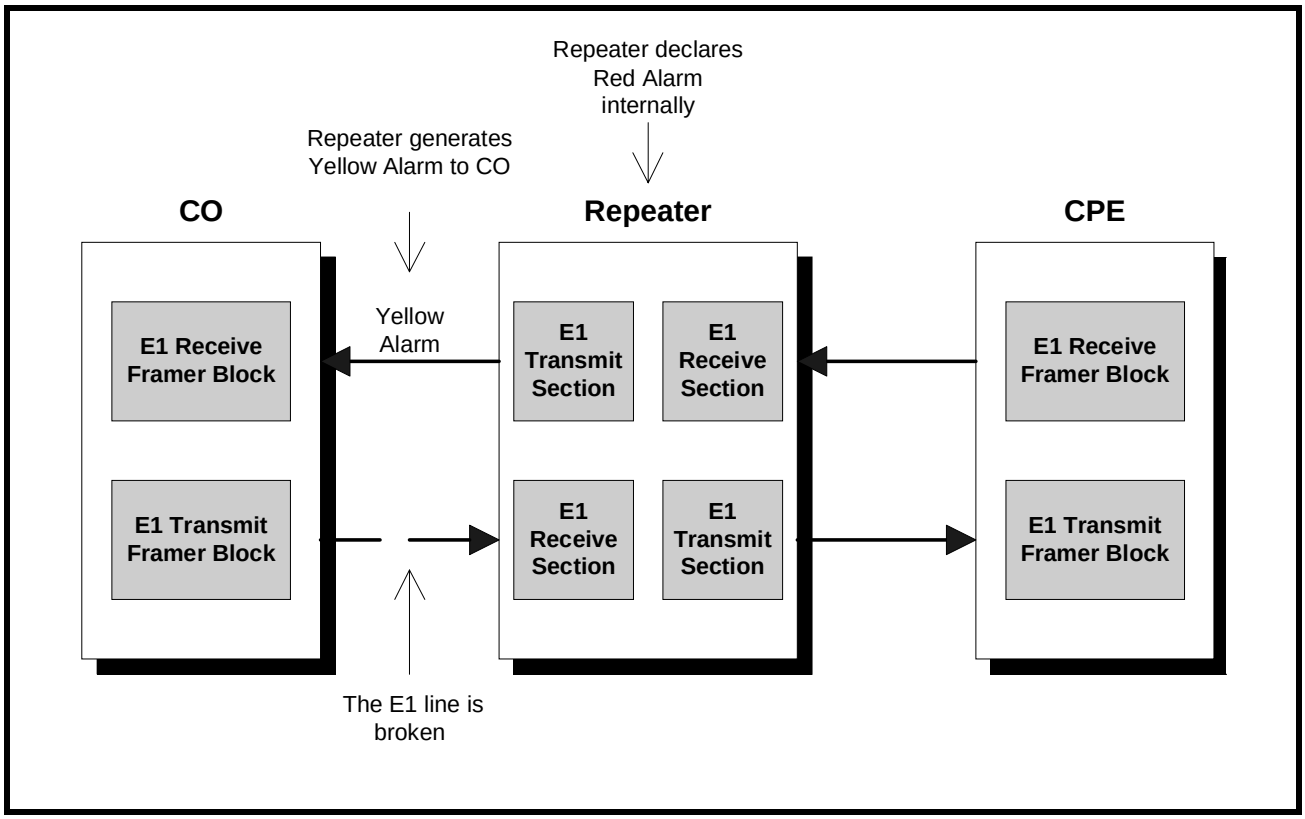


When the E1 system runs normally, that is, when there is no Loss of Signal (LOS) or Loss of Frame (LOF) detected in the line, no alarm will be generated. Sometimes, intermittent outburst of electrical noises on the line might result in Bipolar Violation or bit errors in the incoming signals, but these errors in general will not trigger the equipment to generate alarms. They will, depending on the system requirements, trigger the framer to generate interrupts that would cause the local microprocessor to create performance reports of the line.

Now, consider a case in which the E1 line from the CO to the Repeater is broken or interrupted, resulting in completely loss of incoming data or severely impaired signal quality. Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the Repeater will generate an internal Red Alarm, also known as the Service Alarm Indication. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

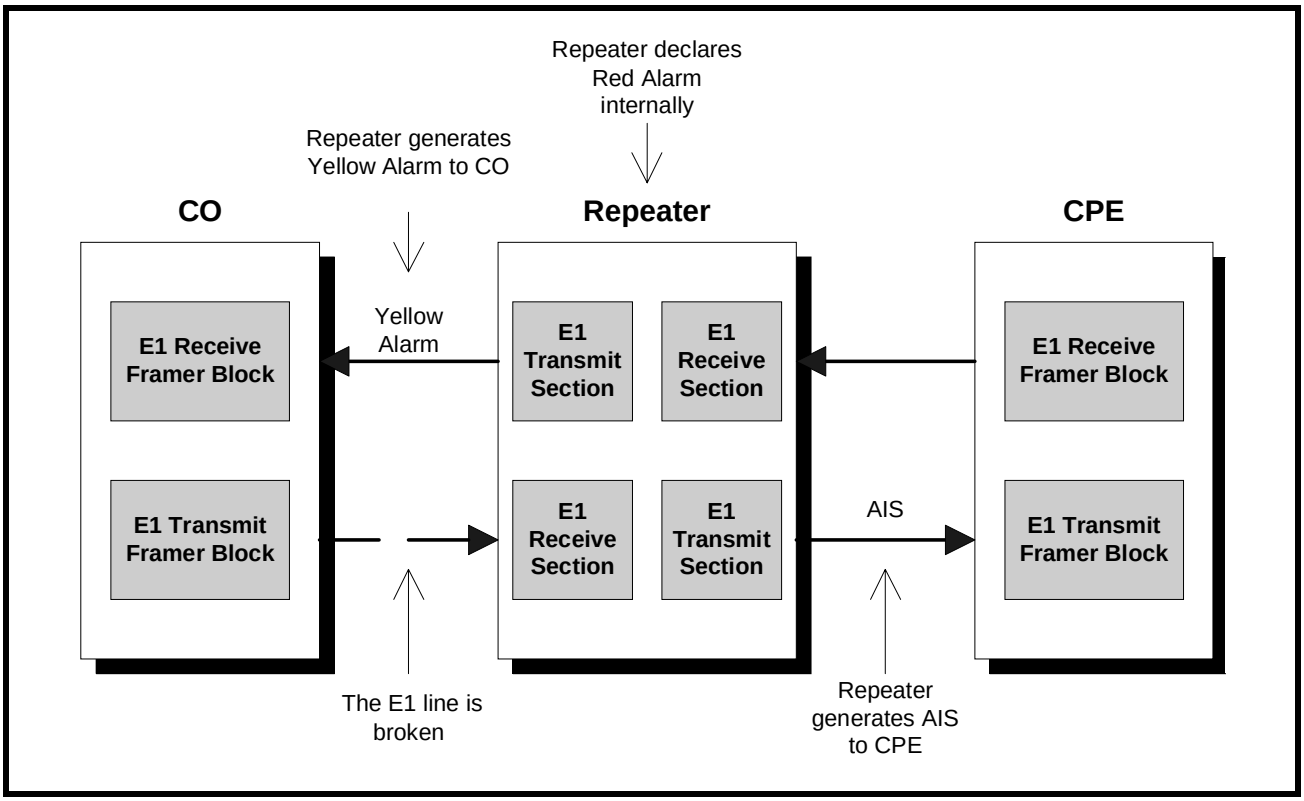
When the Repeater is in the Red Alarm state, it will transmit the Yellow Alarm to the CO indicating the loss of an incoming signal or loss of frame synchronization. This Yellow Alarm informs the CO that there is a problem further down the line and its transmission is not being received at the Repeater. **Figure 95** below illustrates the scenario in which the E1 connection from the CO to the Repeater is broken.

FIGURE 95. GENERATION OF YELLOW ALARM BY THE REPEATER UPON DETECTION OF LINE FAILURE



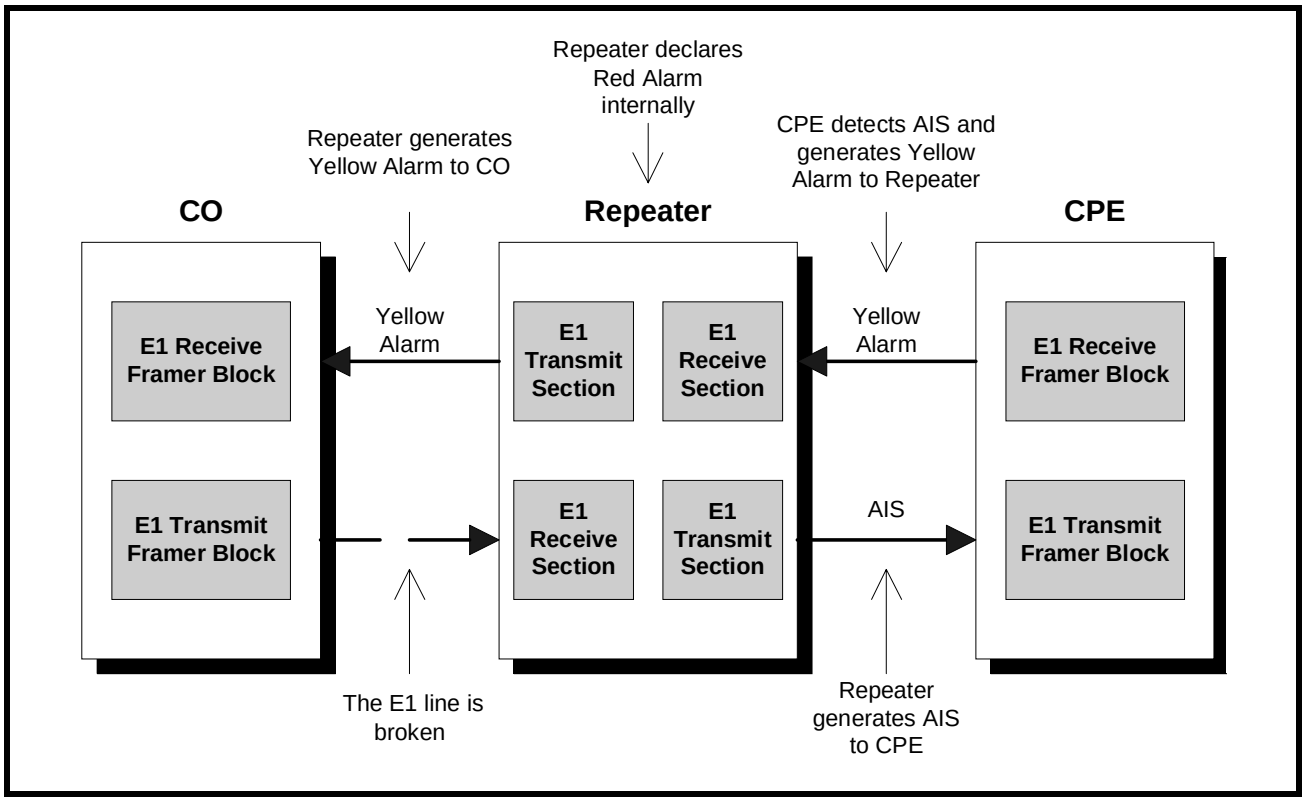
The Repeater will also transmit a Blue Alarm, also known as Alarm Indication Signal (AIS) to the CPE. Blue alarm is an all ones pattern indicating that the equipment is functioning but unable to offer service due to failures originated from remote side. It is sent such that the equipment downstream will not lose clock synchronization even though no meaningful data is received. **Figure 96** below illustrates this scenario in which the Repeater is sending an AIS to the CPE upon detection of line failure from the CO.

FIGURE 96. GENERATION OF AIS BY THE REPEATER UPON DETECTION OF LINE FAILURE



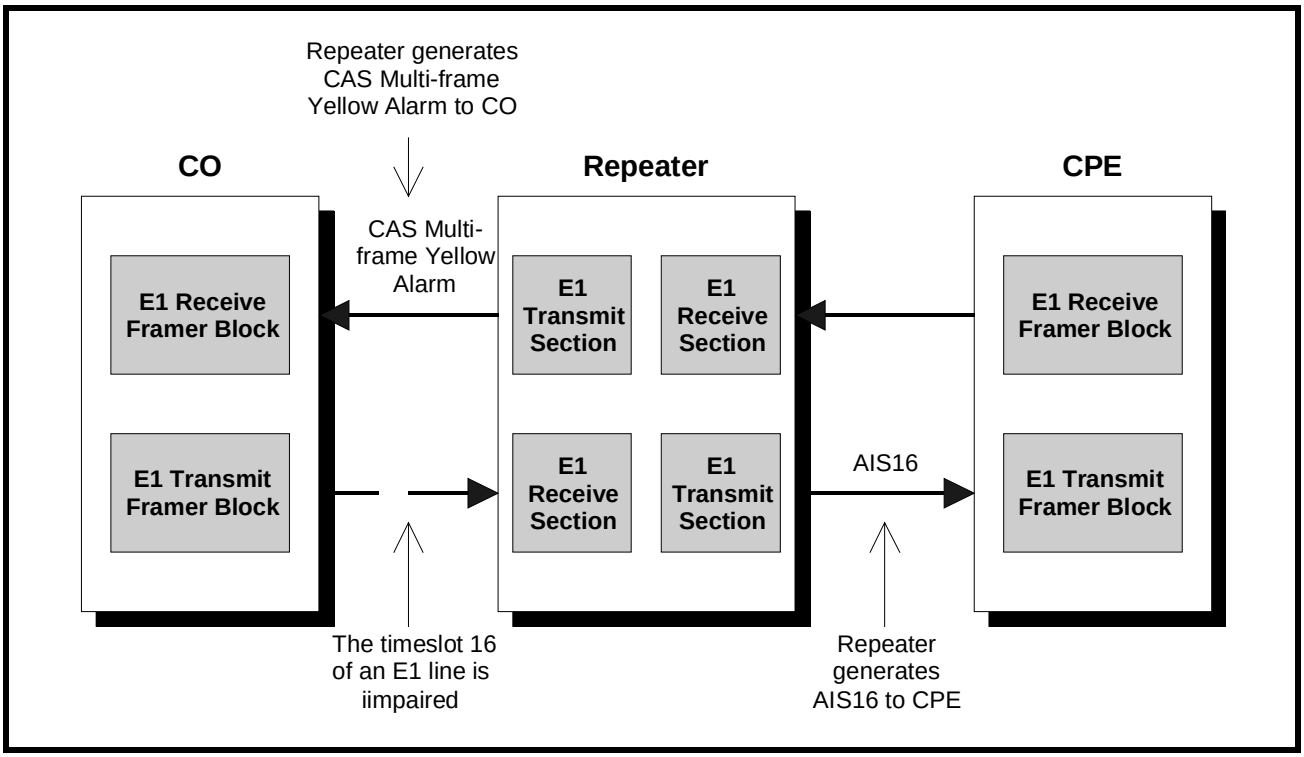
Now, the CPE uses the AIS signal sent by the Repeater to recover received clock and remain in synchronization with the system. Upon detecting the incoming AIS signal, the CPE will generate a Yellow Alarm automatically to the Repeater to indicate the loss of incoming data. **Figure 97** below illustrates this scenario in which the Repeater is sending an AIS to the CPE and the CPE is sending a Yellow Alarm back to the Repeater.

FIGURE 97. GENERATION OF YELLOW ALARM BY THE CPE UPON DETECTION OF AIS ORIGINATED BY THE REPEATER



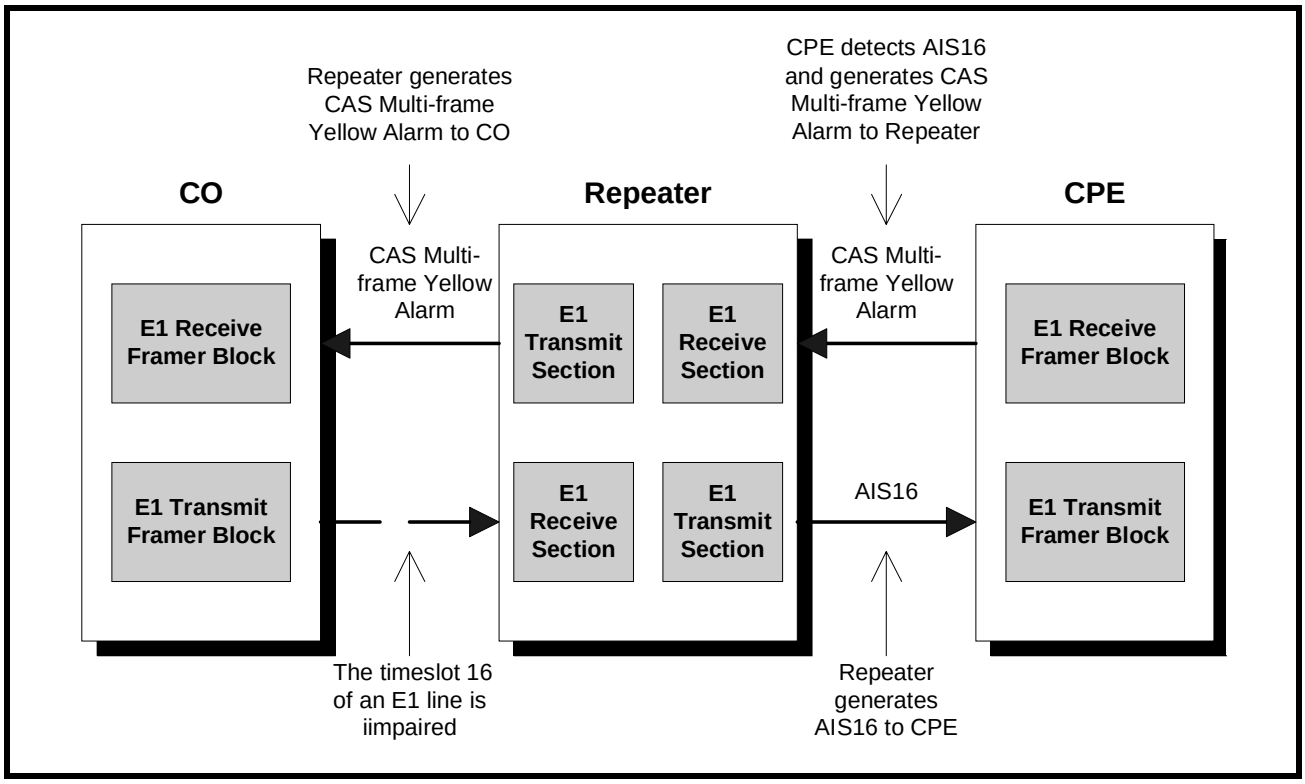
Next, let us consider the scenario in which the signaling and data link channel (the time slot 16) of an E1 line between a far-end terminal (for example, the CO) and a near-end terminal (for example, the repeater) is impaired. In this case, the CAS signaling data received by the repeater is corrupted. The Repeater will then send an all ones pattern in time slot 16 (AIS16) downstream to the CPE. The repeater will also generate a CAS Multi-frame Yellow Alarm upstream to the CO to indicate the loss of CAS Multi-frame synchronization. **Figure 98** below illustrates this scenario in which the Repeater is sending an "AIS16" pattern to the CPE while sending a CAS Multi-frame Yellow Alarm to the CO.

FIGURE 98. GENERATION OF CAS MULTI-FRAME YELLOW ALARM AND AIS16 BY THE REPEATER



The CPE, upon detecting the incoming AIS16 signal, will generate a CAS Multi-frame Yellow Alarm to the Repeater to indicate the loss of CAS Multi-frame synchronization. **Figure 99** below illustrates the CPE sending a CAS Multi-frame Yellow Alarm back to the Repeater.

FIGURE 99. GENERATION OF CAS MULTI-FRAME YELLOW ALARM BY THE CPE UPON DETECTION OF "AIS16" PATTERN SENT BY THE REPEATER



In summary, AIS or Blue Alarm is sent by a piece of E1 equipment downstream indicating that the incoming signal from upstream is lost. Yellow Alarm is sent by a piece of E1 equipment upstream upon detection of Loss of Signal, Loss of Frame or when it is receiving AIS.

Similarly, an "AIS16" pattern is sent by a piece of E1 equipment downstream indicating that the incoming data link channel from upstream is damaged. The CAS Multi-frame Yellow Alarm is sent by a piece of E1 equipment upstream upon detection of Loss of CAS Multi-frame synchronization or when it is receiving an "AIS16" pattern.

9.5.1 How to configure the framer to transmit AIS

As we discussed in the previous section, Alarm Indication Signal (AIS) or Blue Alarm is transmitted by the intermediate node to indicate that the equipment is still functioning but unable to offer services. It is an all ones (except for framing bits) pattern which can be used by the equipment further down the line to maintain clock recovery and timing synchronization.

The XRT86VL3x framer can generate three types of AIS when it is running in E1 format:

- Framed AIS
- Unframed AIS
- AIS16

Unframed AIS is an all ones pattern. If unframed AIS is sent, the equipment further down the line will be able to maintain timing synchronization and be able to recover clock from the received AIS signal. However, due to the lack of framing bits, the equipment farther down the line will not be able to maintain frame synchronization and will declare Loss of Frame (LOF).

On the other hand, the payload portion of a framed AIS pattern is all ones. However, a framed AIS pattern still has correct framing bits. Therefore, the equipment further down the line can still maintain frame synchronization as well as timing synchronization. In this case, no LOF or Red alarm will be declared.

"AIS16" is an AIS alarm that is supported only in E1 framing format. It is an all ones pattern in time slot 16 of each E1 frame. As we mentioned before, time slot 16 is usually used for signaling and data link in E1, therefore, an "AIS16" alarm is transmitted by the intermediate node to indicate that the data link channel is having a problem. Since all the other thirty one time slots are still transmitting normal data (that is, framing information and PCM data), the equipment further down the line can still maintain frame synchronization, timing synchronization as well as receive PCM data. In this case, no LOF or Red alarm will be declared by the equipment further down the line. However, a CAS Multi-frame Yellow Alarm will be sent by the equipment further down the line to indicate the loss of CAS Multi-frame alignment.

The Transmit Alarm Indication Signal Select bits of the Alarm Generation Register (AGR) enable the three types of AIS transmission that are supported by the XRT86VL3x framer. The table below shows configurations of the Transmit Alarm Indication Signal Select bits of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR) (ADDRESS = 0XN108H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit AIS Select	R/W	These READ/WRITE bit-fields allows the user to choose which one of the three AIS pattern supported by the XRT86VL3x framer will be transmitted. 00 - No AIS alarm is generated. 01 - Enable unframed AIS alarm of all ones pattern. 11 - AIS16 pattern is generated. Only time slot 16 is carrying the all ones pattern. The other time slots still carry framing and PCM data. 11 - Enable framed AIS alarm of all ones pattern except for framing bits.

9.5.2 How to configure the framer to generate Red Alarm

Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the Repeater will generate an internal Red Alarm when enabled. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

The Loss of Frame Declaration Enable bit of the Alarm Generation Register (AGR) enable the generation of Red Alarm. The table below shows configurations of the of Frame Declaration Enable bit of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR) (ADDRESS = 0XN108H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Loss of Frame Declaration Enable	R/W	This READ/WRITE bit-field permits the framer to declare Red Alarm in case of Loss of Frame Alignment (LOF). When receiver module of the framer detects Loss of Frame Alignment in the incoming data stream, it will generate a Red Alarm. The framer will also generate an RxLOFs interrupt to notify the microprocessor that an LOF condition is occurred. A Yellow Alarm is then returned to the remote transmitter to report that the local receiver detects LOF. 0 - Red Alarm declaration is disabled. 1 - Red Alarm declaration is enabled.

9.5.3 How to configure the framer to transmit Yellow Alarm

The XRT86VL3x framer supports transmission of both Yellow Alarm and CAS Multi-frame Yellow Alarm in E1 mode.

Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the receiver will transmit the Yellow Alarm back to the source indicating the loss of an incoming signal. This Yellow Alarm informs the source that there is a problem further down the line and its transmission is not being received at the destination.

On the other hand, upon detection of Loss of CAS Multi-frame alignment pattern, the receiver section of the XRT86VL3x framer will transmit a CAS Multi-frame Yellow Alarm back to the source indicating the Loss of CAS Multi-frame synchronization.

The Yellow Alarm Generation Select bits of the Alarm Generation Register (AGR) enable transmission of different types of Yellow alarm that are supported by the XRT86VL3x framer.

9.5.4 Transmit Yellow Alarm

The Yellow Alarm bits are located at bit 2 of time slot 0 of non-FAS frames. A logic one of this bit denotes the Yellow Alarm and a logic zero of this bit denotes normal operation. The XRT86VL3x supports transmission of Yellow Alarm automatically or manually.

When the Yellow Alarm Generation Select bits of the Alarm Generation Register are set to 01, the Yellow Alarm bit is transmitted by echoing the received FAS alignment pattern. If the correct FAS alignment is received, the Yellow Alarm bit is set to zero. If the FAS alignment pattern is missing or corrupted, the Yellow Alarm bit is set to one while Loss of Frame Synchronization is declared.

When the Yellow Alarm Generation Select bits of the Alarm Generation Register are set to 10, the Yellow Alarm bit is transmitted as zero.

When the Yellow Alarm Generation Select bits of the Alarm Generation Register are set to 11, the Yellow Alarm bit is transmitted as one.

9.5.5 Transmit CAS Multi-frame Yellow Alarm

Within the sixteen-frame CAS Multi-frame, the CAS Multi-frame Yellow Alarm bits are located at bit 6 of time slot 16 of frame number 0. A logic one of this bit denotes the CAS Multi-frame Yellow Alarm and a logic zero of this bit denotes normal operation. The XRT86VL3x supports transmission of CAS Multi-frame Yellow Alarm automatically or manually.

When the CAS Multi-frame Yellow Alarm Generation Select bits of the Alarm Generation Register are set to 01, the CAS Multi-frame Yellow Alarm bit is transmitted by echoing the received CAS Multi-frame alignment pattern (the four zeros pattern). If the correct CAS Multi-frame alignment is received, the CAS Multi-frame Yellow Alarm bit is set to zero. If the CAS Multi-frame alignment pattern is missing or corrupted, the CAS Multi-frame Yellow Alarm bit is set to one while Loss of CAS Multi-frame Synchronization is declared.

When the CAS Multi-frame Yellow Alarm Generation Select bits of the Alarm Generation Register are set to 10, the CAS Multi-frame Yellow Alarm bit is transmitted as zero.

When the CAS Multi-frame Yellow Alarm Generation Select bits of the Alarm Generation Register are set to 11, the CAS Multi-frame Yellow Alarm bit is transmitted as one.

9.6 T1 Brief discussion of alarms and error conditions

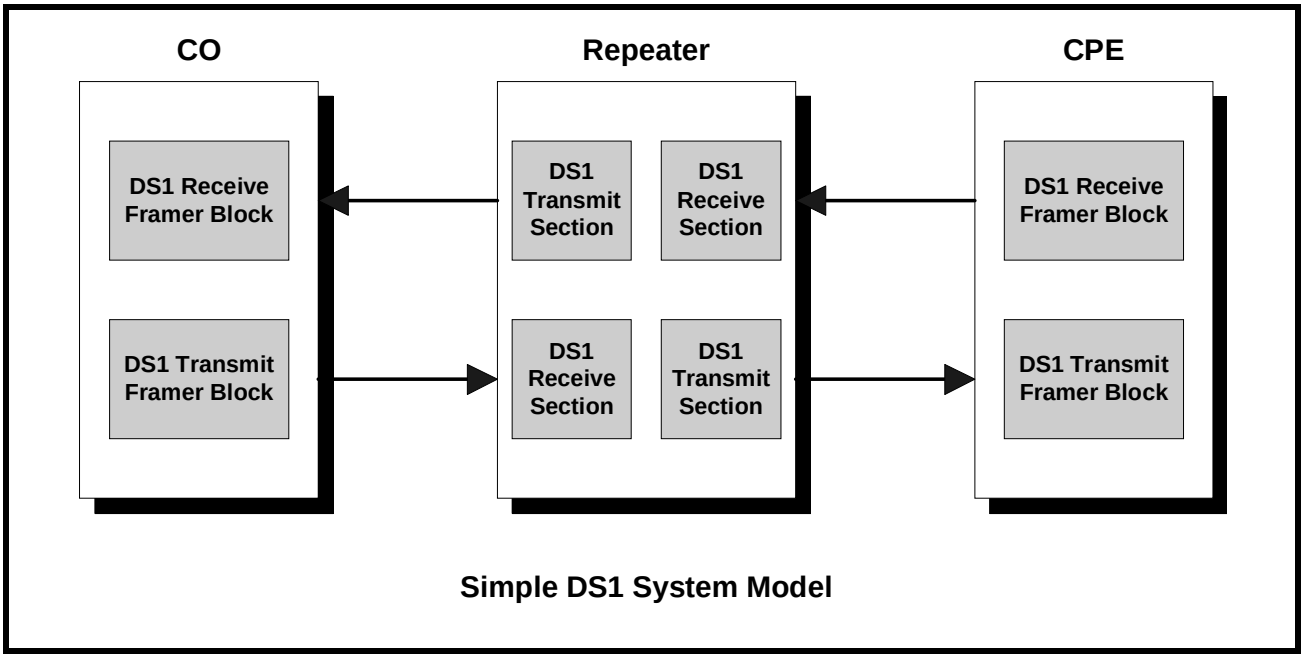
As defined in ANSI T1.231 specification, alarm conditions are created from defects. Defects are momentary impairments present on the DS1 trunk. If a defect is present for a sufficient amount of time (called the integration time), then the defect becomes an alarm. Once an alarm is declared, the alarm is present until after the defect clears for a specified period of time. The time it takes to clear an alarm is called the de-integration time.

Alarms are used to detect and warn maintenance personnel of problems on the DS1 trunk. There are three types of alarms:

- Red alarm or Service Alarm Indication (SAI) Signal
- Blue alarm or Alarm Indication Signal (AIS)
- Yellow alarm or Remote Alarm Indication (RAI) Signal

A simple DS1 system model is shown in **Figure 100** to explain the error conditions and generation of different alarms, let us create. In this model, a DS1 signal is sourced from the Central Office (CO) through a Repeater to the Customer Premises Equipment (CPE). At the same time, a DS1 signal is routed from the CPE to the Repeater and back to the Central Office.

FIGURE 100. SIMPLE DIAGRAM OF DS1 SYSTEM MODEL



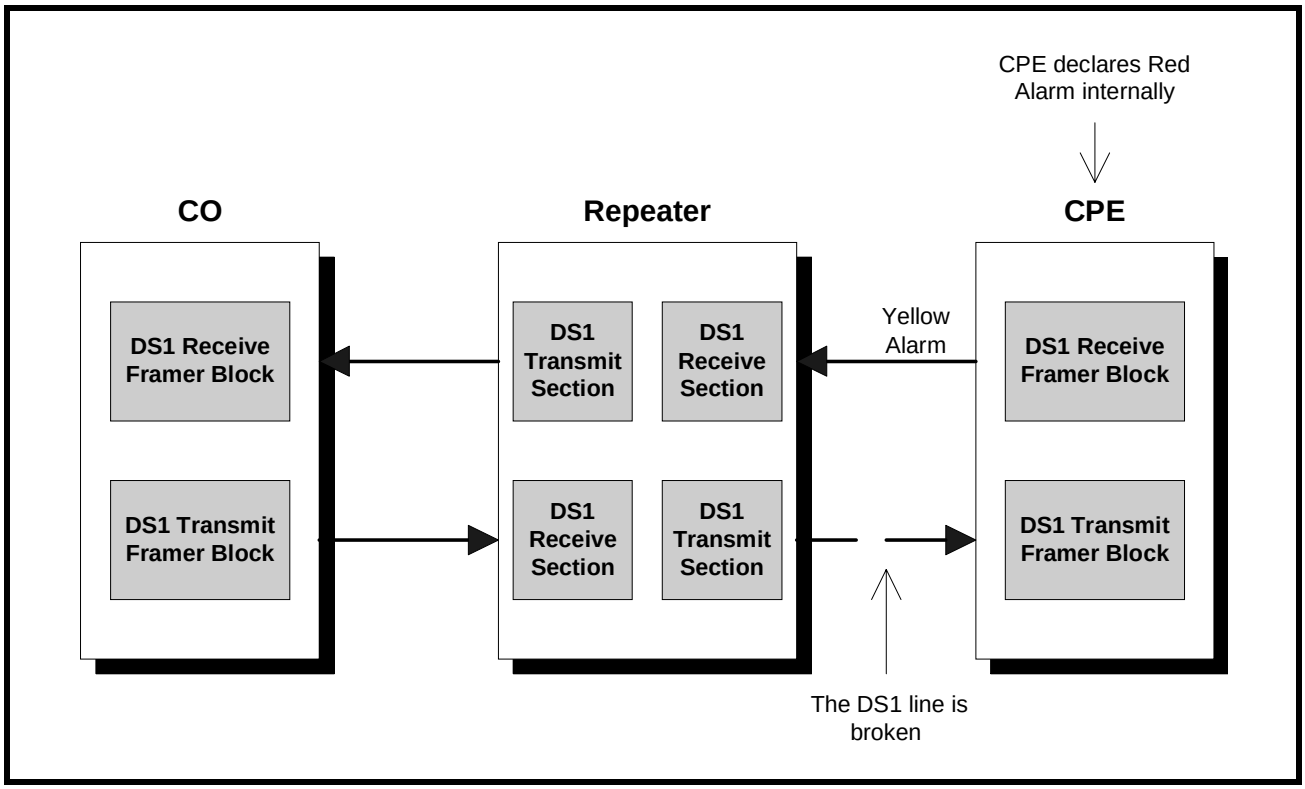
When the DS1 system runs normally, i.e., when there is no Loss of Signal (LOS) or Loss of Frame (LOF) detected in the line, no alarm will be generated. Sometimes, intermittent outburst of electrical noises on the line might result in Bipolar Violation or bit errors in the incoming signals, but these errors in general will not trigger the equipment to generate alarms. They will at most trigger the framer to generate interrupts which would cause the local microprocessor to interrupt as well as add statistics in the performance monitoring accumulator registers.

Now, consider a case in which the DS1 line from the Repeater to CPE is broken or interrupted, resulting in a complete loss of incoming data or a severely impaired signal quality. Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the CPE will generate an internal Red Alarm, also known as the Service Alarm Indication. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

When the CPE is in the Red Alarm state, it will transmit the Yellow Alarm to the Repeater indicating the loss of an incoming signal or loss of frame synchronization. This Yellow Alarm informs the Repeater that there is a

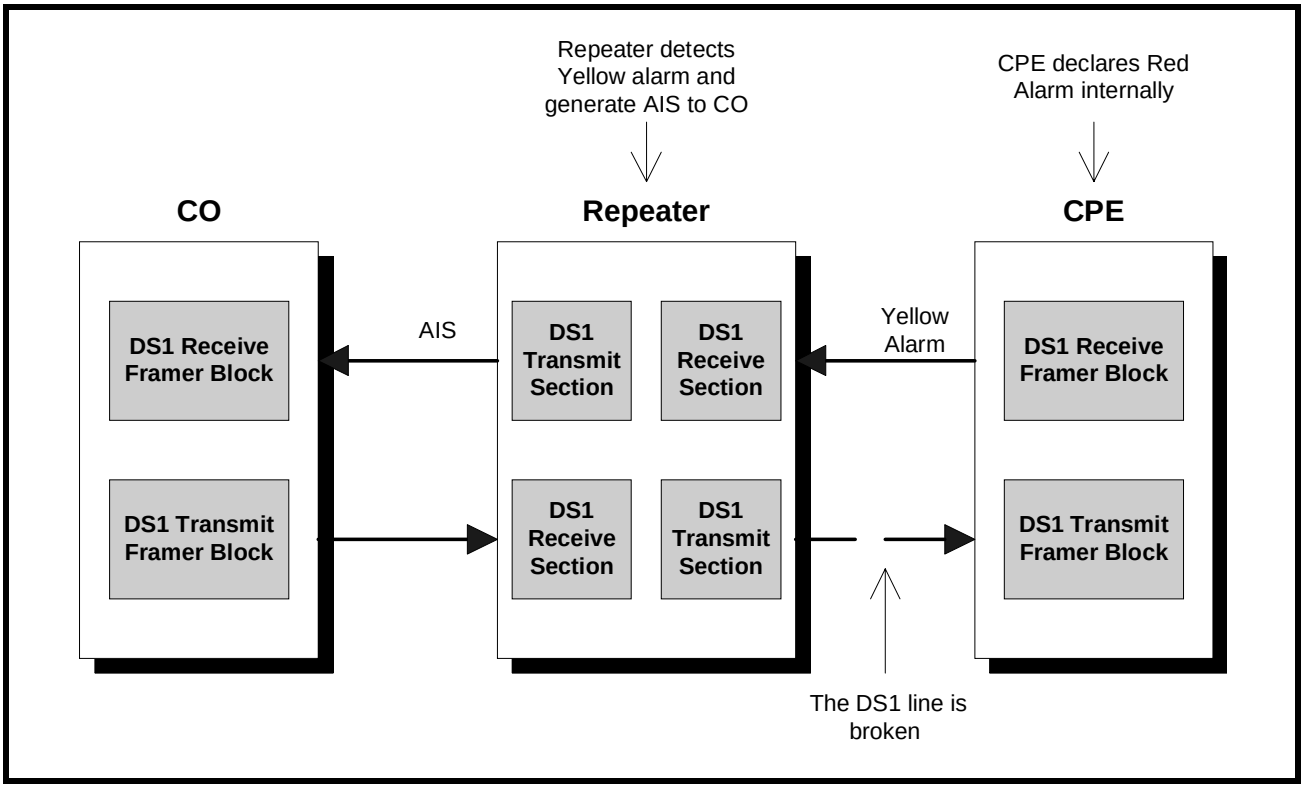
problem further down the line and its transmission is not being received at the CPE. The Figure below illustrates the scenario in which the DS1 connection from the Repeater to CPE is broken.

FIGURE 101. GENERATION OF YELLOW ALARM BY THE CPE UPON DETECTION OF LINE FAILURE



The Repeater, upon detection of Yellow Alarm originated from the CPE, will transmit a Blue Alarm, also known as Alarm Indication Signal (AIS) to the CO. Blue alarm is an all ones pattern indicating that the equipment is functioning but unable to offer service due to failures originated from remote side. It is sent such that the equipment downstream will not lose clock synchronization even though no meaningful data is received. The Figure below illustrates this scenario in which the Repeater is sending an AIS to CO upon detection of Yellow alarm originated from the CPE.

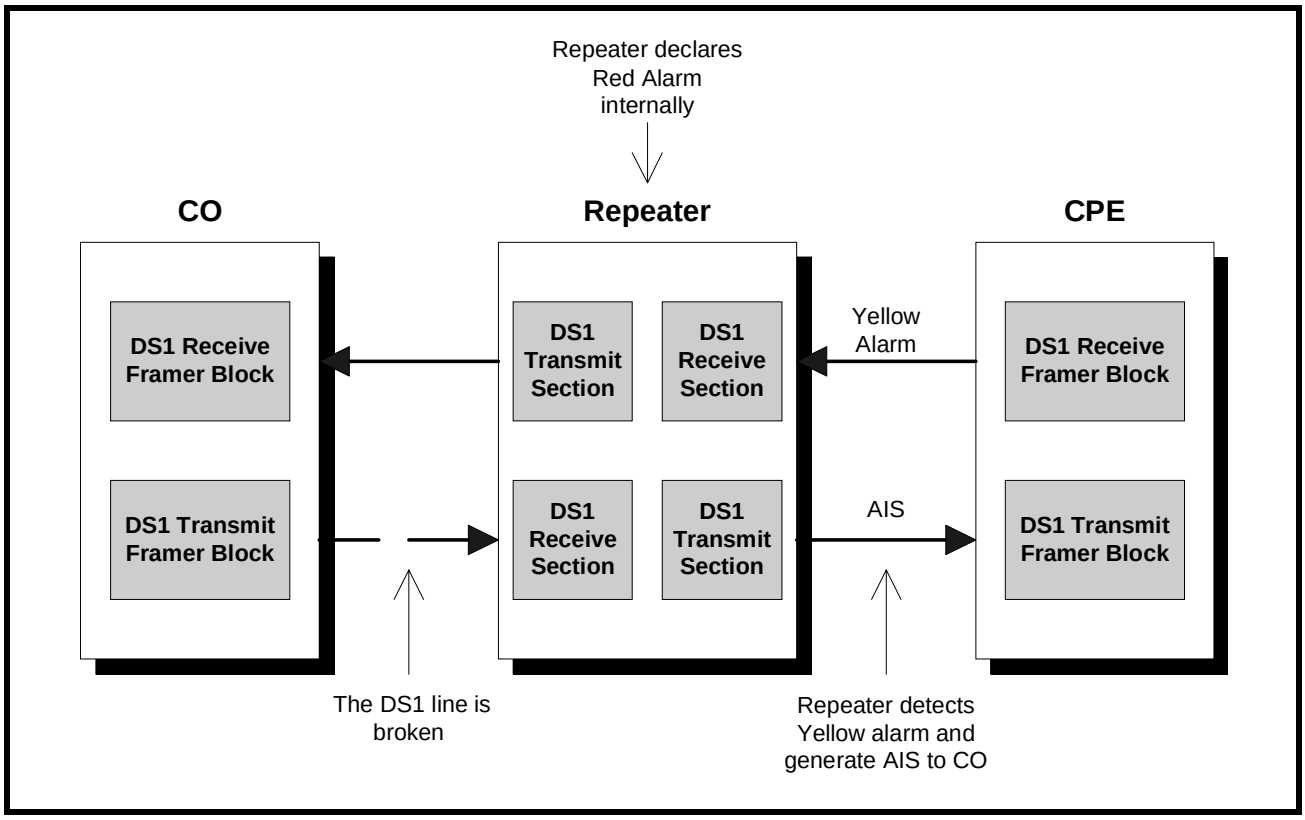
Generation of AIS by the Repeater upon detection of Yellow Alarm originated by the CPE



Now let us consider another scenario in which the DS1 line between CO and the Repeater is broken. Again, upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the Repeater will generate an internal Red Alarm. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

The Repeater will also send an all ones AIS pattern downstream to the CPE and a Yellow Alarm back to the CO. The CPE uses the AIS signal to recover received clock and remain in synchronization with the system. Upon detecting the incoming AIS signal, the CPE will generate a Yellow Alarm to the Repeater to indicate the loss of incoming signal. The Figure below illustrates this scenario in which the Repeater is sending an AIS to the CPE and the CPE is sending a Yellow Alarm back to the Repeater.

FIGURE 102. GENERATION OF YELLOW ALARM BY THE CPE UPON DETECTION OF AIS ORIGINATED BY THE REPEATER



9.6.1 How to configure the framer to transmit AIS

As we discussed in the previous section, Alarm Indication Signal (AIS) or Blue Alarm is transmitted by the intermediate node to indicate that the equipment is still functioning but unable to offer services. It is an all ones (except for framing bits) pattern which can be used by the equipment further down the line to maintain clock recovery and timing synchronization.

The XRT86VL3x framer can generate two types of AIS:

- Framed AIS
- Unframed AIS

Unframed AIS is an all ones pattern. If unframed AIS is sent, the equipment further down the line will be able to maintain timing synchronization and be able to recover clock from the received AIS signal. However, due to the lack of framing bits, the equipment farther down the line will not be able to maintain frame synchronization and will declare Loss of Frame (LOF).

On the other hand, the payload portion of a framed AIS pattern is all ones. However, a framed AIS pattern still has correct framing bits. Therefore, the equipment further down the line can still maintain frame synchronization as well as timing synchronization. In this case, no LOF or Red alarm will be declared.

The Transmit Alarm Indication Signal Select bits of the Alarm Generation Register (AGR) enable the two types of AIS transmission that are supported by the XRT86VL3x framer. The table below shows configurations of the Transmit Alarm Indication Signal Select bits of the Alarm Generation Register (AGR)

ALARM GENERATION REGISTER (AGR)(ADDRESS = 0XN108H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit AIS Select	R/W	These READ/WRITE bit-fields allows the user to choose which one of the two AIS pattern supported by the XRT86VL3x framer will be transmitted. 00 - No AIS alarm is generated. 01 - Enable unframed AIS alarm of all ones pattern. 10 - Enable framed AIS alarm of all ones pattern except for framing bits. 11 - No AIS alarm is generated.

9.6.2 How to configure the framer to generate Red Alarm

Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the Repeater will generate an internal Red Alarm when enabled. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

The Loss of Frame Declaration Enable bit of the Alarm Generation Register (AGR) enables the generation of Red Alarm. The table below shows configurations of the of Frame Declaration Enable bit of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR)(ADDRESS = 0XN108H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Loss of Frame Declaration Enable	R/W	This READ/WRITE bit-field permits the framer to declare Red Alarm in case of Loss of Frame Alignment (LOF). When receiver module of the framer detects Loss of Frame Alignment in the incoming data stream, it will generate a Red Alarm. The framer will also generate an RxLOFs interrupt to notify the microprocessor that an LOF condition is occurred. A Yellow Alarm is then returned to the remote transmitter to report that the local receiver detects LOF. 0 - Red Alarm declaration is disabled. 1 - Red Alarm declaration is enabled.

9.6.3 How to configure the framer to transmit Yellow Alarm

Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the receiver will transmit the Yellow Alarm back to the source indicating the loss of an incoming signal. This Yellow Alarm informs the source that there is a problem further down the line and its transmission is not being received at the destination.

The XRT86VL3x framer supports transmission of Yellow Alarm when running at the following framing formats:

- SF Mode
- ESF Mode
- N Mode
- T1DM Mode

Yellow alarm is transmitted in different forms for various framing formats. The Yellow Alarm Generation Select bits of the Alarm Generation Register (AGR) enable transmission of different types of Yellow alarm that are supported by the XRT86VL3x framer.

9.6.4 Transmit Yellow Alarm in SF Mode

In SF mode, the XRT86VL3x supports transmission of Yellow Alarm in two ways. When the Yellow Alarm Generation Select bits of the Alarm Generation Register are set to 01 or 11, the second MSB of all DS0 channels is transmitted as zero. This is Yellow Alarm for DS1 standard.

When the Yellow Alarm Generation Select bits of the Alarm Generation Register are set to 10, the Framing bit of Frame 12 is transmitted as one. This is Yellow Alarm for J1 standard.

9.6.5 Transmit Yellow Alarm in ESF Mode

In ESF mode, the XRT86VL3x transmits Yellow Alarm on the 4Kbit/s data link channel. The Facility Data Link bits are sent in the pattern of eight ones followed by eight zeros. The number of repetitions of this pattern depends on the duration of Yellow Alarm Generation Select bits of the Alarm Generation Register. When these select bits are set to 01 or 11, the following scenario will happen:

1. If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns.
2. If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW.
3. A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm.

NOTE: *To pulse Bit 0, this bit must be programmed to "1" and then reset back to "0". The pulse width is the duration in time that this bit remains at "1".*

When these select bits are set to 10, Bit 1 of the Yellow Alarm Generation Select forms a pulse that controls the duration of Yellow Alarm transmission. The alarm continues until Bit 1 goes LOW.

When these select bits are set to 01, the following scenario will happen:

1. If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns.
2. If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW.
3. A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm.

9.6.6 Transmit Yellow Alarm in N Mode

In N mode, when the Yellow Alarm Generation Select bits of the Alarm Generation Register are set to 01, 10 or 11, the second MSB of all DS0 channels is transmitted as zero.

9.6.7 Transmit Yellow Alarm in T1DM Mode

In T1DM mode, when the Yellow Alarm Generation Select bits of the Alarm Generation Register are set to 01, 10 or 11, the Yellow Alarm bit (the third LSB of Timeslot 23) is set to zero.The table below shows configurations of the Yellow Alarm Generation Select bits of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR)(ADDRESS = 0XN108H)

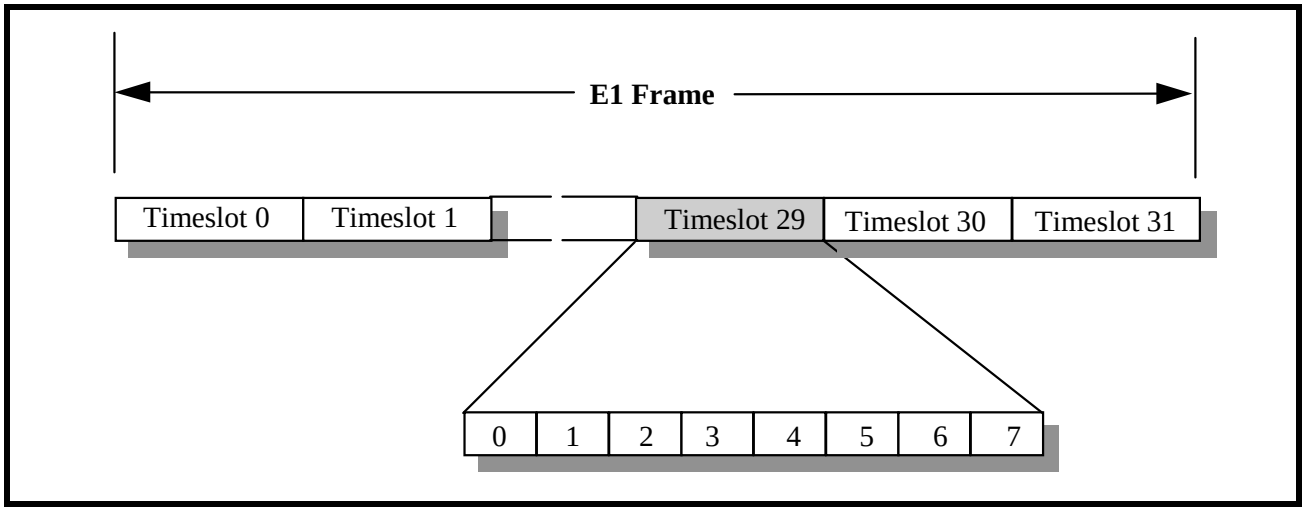
BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Yellow Alarm Generation Select	R/W	00 - Transmission of Yellow Alarm is disabled. 01 - The framer transmits Yellow Alarm by converting the second MSB of all outgoing twenty-four DS0 channel into zero. 10 - The framer transmits Yellow Alarm by sending the Super-frame Alignment Bit (Fs) of Frame 12 as one. 11 - The framer transmits Yellow Alarm by converting the second MSB of all outgoing twenty-four DS0 channel into zero. N Mode: 00 - Transmission of Yellow Alarm is disabled. 01, 10 or 11 - The framer transmits Yellow Alarm by converting the second MSB of all outgoing twenty-four DS0 channel into zero. ESF Mode: When the framer is in ESF mode, it transmits Yellow Alarm pattern of eight ones followed by eight zeros (1111_1111_0000_0000) through the 4Kbit/s data link bits. 00 - Transmission of Yellow Alarm is disabled. 01 - The following scenario will happen: **1.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns. **2.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW. **3.** A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm. 10 - Bit 1 of the Yellow Alarm Generation Select forms a pulse that controls the duration of Yellow Alarm transmission. The alarm continues until Bit 1 goes LOW. 11 - The following scenario will happen: **1.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns. **2.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW. **3.** A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm. T1DM Mode: 00 - Transmission of Yellow Alarm is disabled. 01, 10 or 11 - The framer transmits Yellow Alarm by setting the Yellow Alarm bit (Y-bit) to zero.

10.0 APPENDIX A: DS-1/E1 FRAMING FORMATS

10.1 The E1 Framing Structure

A single E1 frame consists of 256 bits which is created 8000 times per second. This yields a bit-rate of 2.048Mbps. The 256 bits within each E1 frame are grouped into 32 octets or timeslots. These timeslots are numbered from 0 to 31. Each timeslot is 8 bits in length and is transmitted most significant bit first, numbered bit 0. **Figure 103** presents a diagram of a single E1 frame.

FIGURE 103. SINGLE E1 FRAME DIAGRAM



Not all of these timeslots are available to transmit voice or user data. For instance, timeslot 0 is always reserved for system use and timeslot 16 is sometimes used (reserved) by the system. Hence, within each E1 frame, either 30 or 31 of the 32 timeslots are available for transporting user or voice data. In general, there are two types of E1 frames, FAS and Non-FAS. In any E1 data stream, the E1 frame begins with a FAS frame followed by Non-FAS frame and then alternates between the two.

10.1.1 FAS Frame

Timeslot 0 within the FAS E1 frame contains a framing alignment pattern and therefore supports framing. The bit-format of timeslot 0 is presented in **Table 7**. The Si bit within the FAS E1 Frame typically carries the results of a CRC-4 calculation. The fixed framing pattern (e.g., 0, 0, 1, 1, 0, 1, 1) will be used by the Receive E1 Framer at the Remote terminal for frame synchronization/alignment purposes.

TABLE 7: BIT FORMAT OF TIMESLOT 0 OCTET WITHIN A FAS E1 FRAME

BIT	0	1	2	3	4	5	6	7
Value	SI	0	0	1	1	0	1	1
Function	International Bit	Frame Alignment Signaling (FAS) Pattern						
Description-Operation	In practice, the Si bit within the FAS E1 Frame carries the results of a CRC-4 calculation, which is discussed in greater detail in Section 10.2.1.	The fixed framing pattern (e.g., 0, 0, 1, 1, 0, 1, 1) is used by the Receive E1 Framer at the Remote terminal for frame synchronization/alignment purposes.						

10.1.2 Non-FAS Frame

Timeslot 0 within the non-FAS E1 frame contains bits that support signaling or data link message transmission. The bit-format of timeslot 0 is presented in **Table 8**. The Si bit in the Non-FAS frame typically carries a specific value that will be used by the Receive E1 Framer for CRC Multi-frame alignment purposes.

TABLE 8: BIT FORMAT OF TIMESLOT 0 OCTET WITHIN A NON-FAS E1 FRAME

BIT	0	1	2	3	4	5	6	7
Value	Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
Function6	International Bit	Fixed Value	Yellow Alarm	National bits				
Description-Operation	International Bit The Si bit within the non-FAS E1 Frame typically carries a specific value that will be used by the Receive E1 Framer for CRC Multi-frame alignment purposes.	Fixed at “1” Bit-field “1” contains a fixed value “1”. This bit-field will be used for FAS framing synchronization/alignment purposes by the Remote Receive E1 Framer.	FAS Frame Yellow Alarm Bit This bit-field is used to transmit a Yellow alarm to the Remote Terminal. This bit-field is set to “0” during normal conditions, and is set to “1” whenever the Receive E1 Framer detects an LOS (Loss of Signal) or LOF (Loss of Framing) condition in the incoming E1 frame data.	National Bits These bit-fields can be used to carry data link information from the Local transmitting terminal to the Remote receiving terminal. Since the National bits only exist in the non-FAS frames, they offer a maximum signaling data link bandwidth of 20kbps.				

10.2 The E1 Multi-frame Structure

There are two types of E1 Multi-frame structures, CRC Multi-frame and CAS Multi-frame. The CAS Multi-frame can be considered a subset of the CRC Multi-frame, in that CAS is an option to carry signaling information within the CRC Multi-frame structure.

10.2.1 The CRC Multi-frame Structure

A CRC Multi-frame consists of 16 consecutive E1 frames, with the first of these frames being a FAS frame. From a Frame Alignment point of view, timeslot 0 of each of these E1 frames within the Multi-frame are the most important 16 octets. **Table 9** presents the bit-format for all timeslot 0 octets within a 16 frame CRC Multi-frame.

TABLE 9: BIT FORMAT OF ALL TIMESLOT 0 OCTETS WITHIN A CRC MULTI-FRAME

SMF	FRAME NUMBER	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1	0	C1	0	0	1	1	0	1	1
	1	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	2	C2	0	0	1	1	0	1	1
	3	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	4	C3	0	0	1	1	0	1	1
	5	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	6	C4	0	0	1	1	0	1	1
	7	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
2	8	C1	0	0	1	1	0	1	1
	9	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	10	C2	0	0	1	1	0	1	1
	11	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	12	C3	0	0	1	1	0	1	1
	13	E	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	14	C4	0	0	1	1	0	1	1
	15	E	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

The CRC Multi-frame is divided into 2 sub Multi-Frames. Sub-Multi-Frame 1 is designated as SMF1 and Sub-Multi-Frame 2 is designated as SMF2. SMF1 and SMF2 each consist of 8 E1 frames having 4 FAS frames and 4 non-FAS frames. There are two interesting things to note in **Table 9**. First, all of the bit-field 0 positions within each of the FAS frames (within each SMF) are designated as C1, C2, C3 and C4. These four bit-fields contain the CRC-4 values which have been computed over the previous SMF. Hence, while the Transmit E1 Framer is assembling a given SMF, it computes the CRC-4 value for that SMF and inserts these results into the C1 through C4 bit-fields within the very next SMF. These CRC-4 values ultimately are used by the Remote Receive E1 Framer for error detection purposes.

NOTE: *This framing structure is referred to as a CRC Multi-Frame because it permits the remote receiving terminal to locate and verify the CRC-4 bit-fields.*

The second interesting thing to note regarding **Table 9** is that the bit-field 0 positions within each of the non-FAS frames (within the entire MF) are of a fixed 6-bit pattern 0, 0, 1, 0, 1, 1 along with two bits, each designated as “E”. This 6-bit pattern is referred to as the CRC Multi-Frame alignment pattern, which can ultimately be used by the Remote Receive E1 Framer for CRC Multi-Frame synchronization/alignment. The "E" bits are used to indicate that the Local Receive E1 framer has detected errored sub-Multi-Frames.

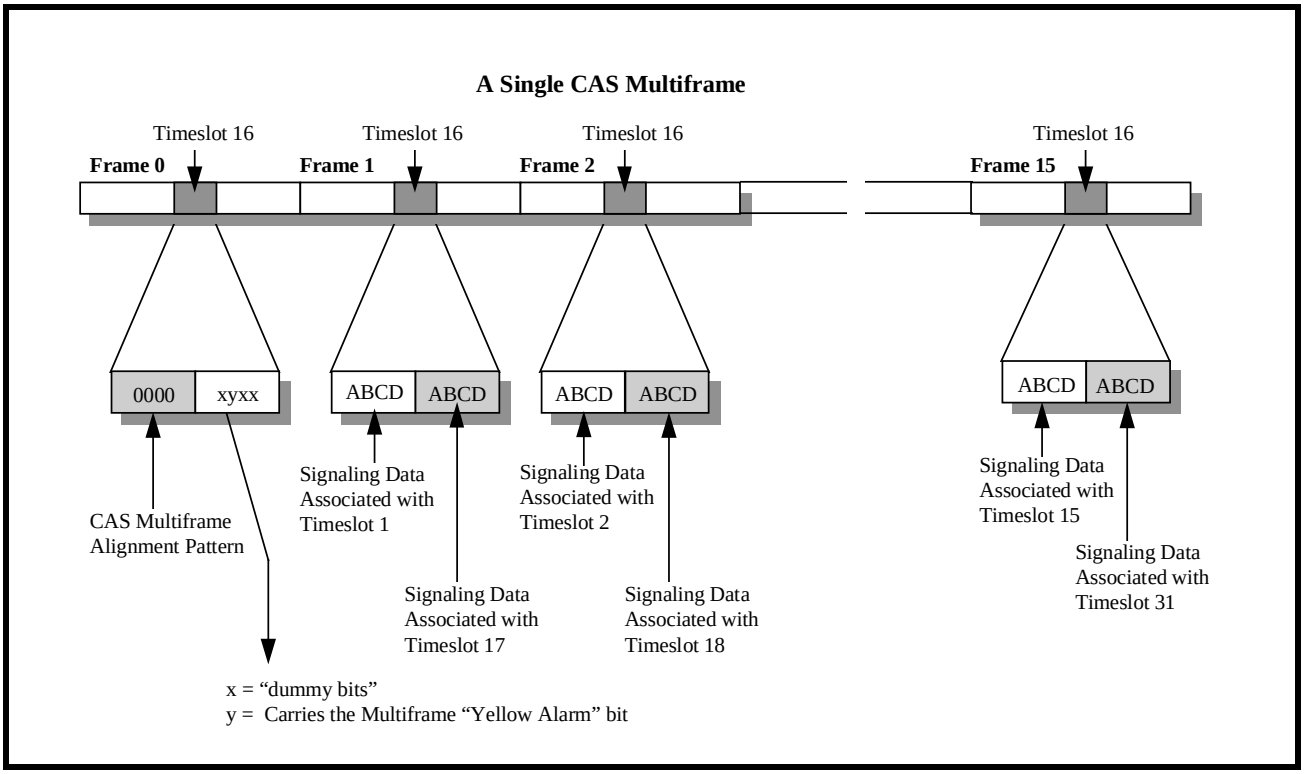
10.2.2 CAS Multi-Frames and Channel Associated Signaling

CAS Multi-Frames are only relevant if the user is using CAS or Channel Associated Signaling. If the user is implementing Common Channel Signaling then the CAS Multi-Frame is not available.

10.2.2.1 Channel Associated Signaling

If the user operates an E1 channel in Channel Associated Signaling, then timeslot 16 octets within each E1 frame will be reserved for signaling. Such signaling would convey information such as On-Hook, Off-Hook conditions, call set-up, control, etc. In CAS, this type of signaling data that is associated with a particular voice channel will be carried within timeslot 16 of a particular E1 frame within a CAS Multi-Frame. The CAS is carried in a Multi-Frame structure which consists of 16 consecutive E1 frames. The framing/byte format of a CAS Multi-Frame is presented in **Figure 104**.

FIGURE 104. FRAME/BYTE FORMAT OF THE CAS MULTI-FRAME STRUCTURE



Timeslot 16 within frame 0 is a special octet that is used to convey CAS Multi-Frame alignment information, and to convey Multi-Frame alarm information to the Remote Terminal. The bit-format of timeslot 16 within frame 0 of a CAS Multi-Frame is 0000 xyxx. The upper nibble of this octet contains all zeros and is used to identify itself as the CAS Multi-Frame alignment signal. If CAS is used, then the user is advised to insure that none of the other timeslot 16 octets contain the value "0000". The lower nibble of this octet contains the expression "xyxx". The x-bits are the spare bits and should be set to "0" if not used. The y-bit is used to indicate a Multi-Frame alarm condition to the Remote terminal. During normal operation, this bit-field is cleared to "0". However, if the Local Receive E1 Framer detects a problem with the incoming Multi-Frames, then the Local Transmit E1 Framer will set this bit-field within the next outbound CAS Multi-Frame to "1".

NOTE: *The Local Transmit E1 Framer will continue to set the y-bit to "1" for the duration that the Local Receive E1 Framer detects this problem.*

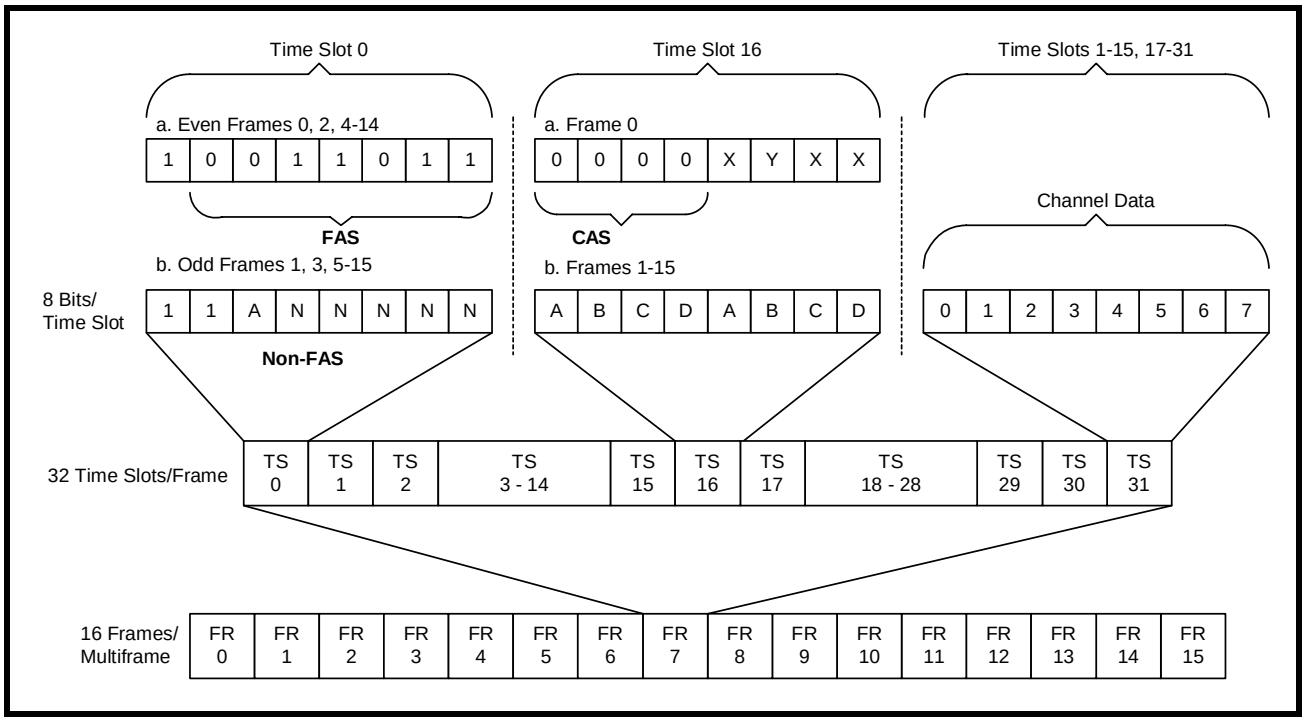
Timeslot 16 within Frame 1 of the CAS Multi-Frame contains 4 bits of signaling data for voice channel 1 and 4 bits of signaling data for voice channel 17. Timeslot 16 within Frame 2 contains 4 bits of signaling data for voice channel 2 and 4 bits of signaling data for voice channel 18, and this continues for all E1 frames.

10.2.2.2 Common Channel Signaling (CCS)

Common Channel Signaling is an alternative form of signaling from CAS. In CCS, whatever signaling data which is transported via the outbound E1 data stream, carries information that applies to all of the voice channels as a set (e.g., timeslots 1 through 15 and 17 through 31) in the E1 frame. There are numerous other variations of Common Channel Signaling that are available. Some of these are listed below.

- 31 Voice Channels with the common channel signaling being transported via the National Bits.
- 30 Voice Channels with the common channel signaling data being transported via the National Bits and CAS data being transported via timeslot 16.
- 30 Voice Channels with the Common Channel Signaling being processed via timeslot 16. (e.g., Primary Rate ISDN Signaling).

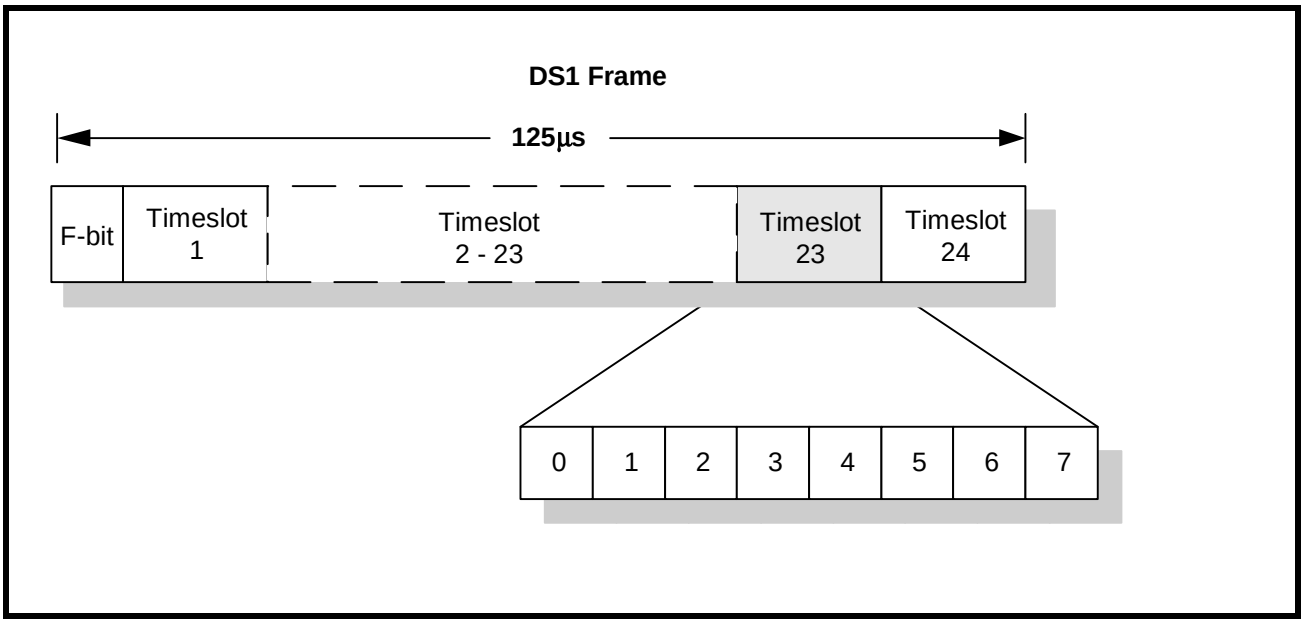
FIGURE 105. E1 FRAME FORMAT



10.3 The DS1 Framing Structure

A single T1 frame is 193 bits long and is transmitted at a frame rate of 8000Hz. This results in an aggregate bit rate of 1.544 Mbit/s. Basic frames are divided into 24 timeslots numbered 1 thru 24 and a framing bit as shown in **Figure 106**. Each timeslot is 8 bits in length and is transmitted most significant bit first, numbered bit 0. This results in a single timeslot data rate of 8 bits x 8000/sec = 64 kbit/s.

FIGURE 106. T1 FRAME FORMAT



10.4 T1 Super Frame Format (SF)

The Superframe Format (SF), is also referred to as the D4 format. The requirement for associated signaling in frames 6 and 12 dictates that the frames be distinguishable. This leads to a multiframe structure consisting of 12 frames per superframe (SF) as shown in **Figure 107** and **Table 10**. This structure of frames and multiframes is defined by the F-bit pattern. The F-bit is designated alternately as an Ft bit (terminal framing bit) or Fs bit (signalling framing bit). The Ft bit carries a pattern of alternating zeros and ones (101010) in odd frames that defines the boundaries so that one timeslot may be distinguished from another. The Fs bit carries a pattern of (001110) in even frames and defines the multiframe boundaries so that one frame may be distinguished from another.

FIGURE 107. T1 SUPERFRAME PCM FORMAT

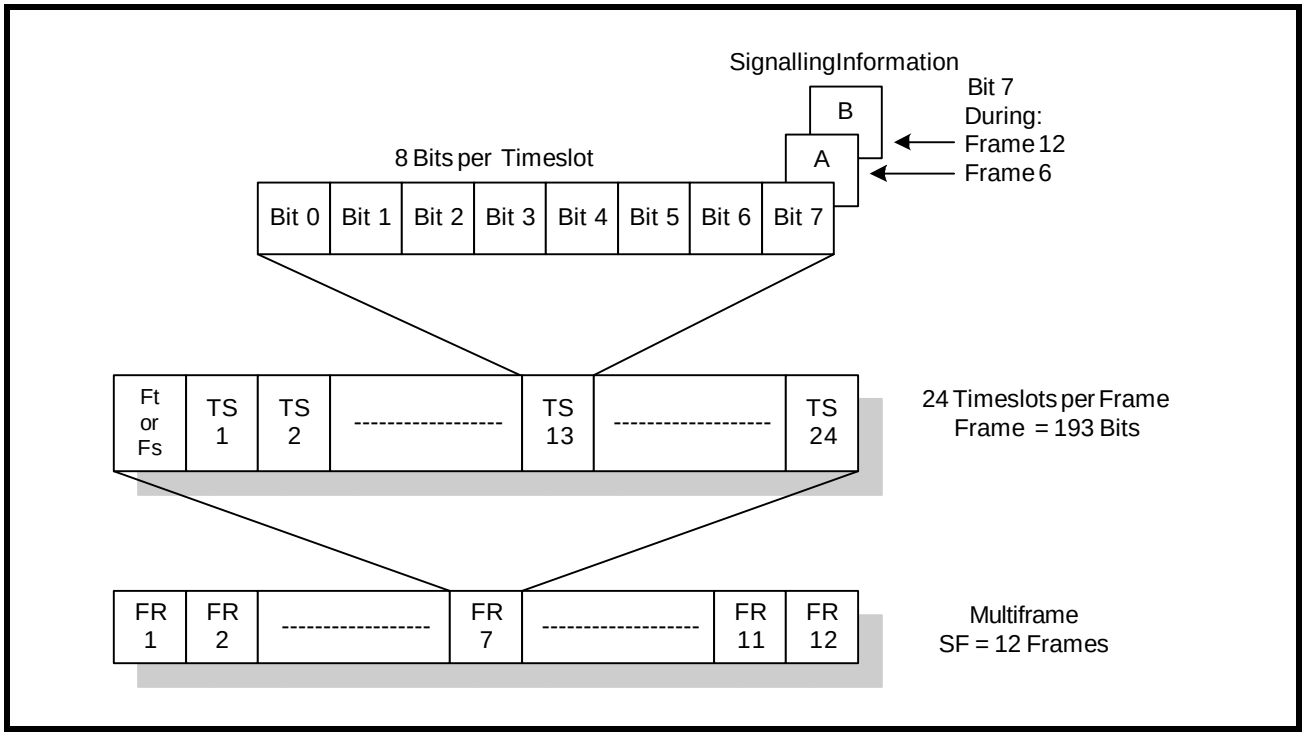


TABLE 10: SUPERFRAME FORMAT

FRAME	BIT	F-BITS		BIT USE IN EACH TIMESLOT		SIGNALLING CHANNEL
		TERMINAL FRAMING FT	TERMINAL FRAMING FS	TRAFFIC	SIG	
1	0	1	----	1-8	----	----
2	193	----	0	1-8	----	----
3	386	0	----	1-8	----	----
4	579	----	0	1-8	----	----
5	772	1	----	1-8	----	----
6	965	----	1	1-7	8	A
7	1158	0	----	1-8	----	----
8	1351	----	1	1-8	----	----

TABLE 10: SUPERFRAME FORMAT

FRAME	BIT	F-BITS		BIT USE IN EACH TIMESLOT		SIGNALLING CHANNEL
		TERMINAL FRAMING FT	TERMINAL FRAMING FS	TRAFFIC	SIG	
9	1544	1	----	1-8	----	----
10	1737	----	1	1-8	----	----
11	1930	0	----	1-8	----	----
12	2123	----	0	1-7	8	B

10.5 T1 Extended Superframe Format (ESF)

In Extended Superframe Format (ESF), as shown in **Figure 108** and **Table 11**, the multiframe structure is extended to 24 frames. The timeslot structure is identical to D4 (SF) format. Robbed-bit signaling is accommodated in frame 6 (A-bit), frame 12 (B-bit), frame 18 (C-bit) and frame 24 (D-bit).

The F-bit pattern of ESF contains three functions:

1. Framing Pattern Sequence (FPS), which defines the frame and multiframe boundaries.
2. Facility Data Link (FDL), which allows data such as error-performance to be passed within the T1 link.
3. Cyclic Redundancy Check (CRC), which allows error performance to be monitored and enhances the reliability of the receiver's framing algorithm.

FIGURE 108. T1 EXTENDED SUPERFRAME FORMAT

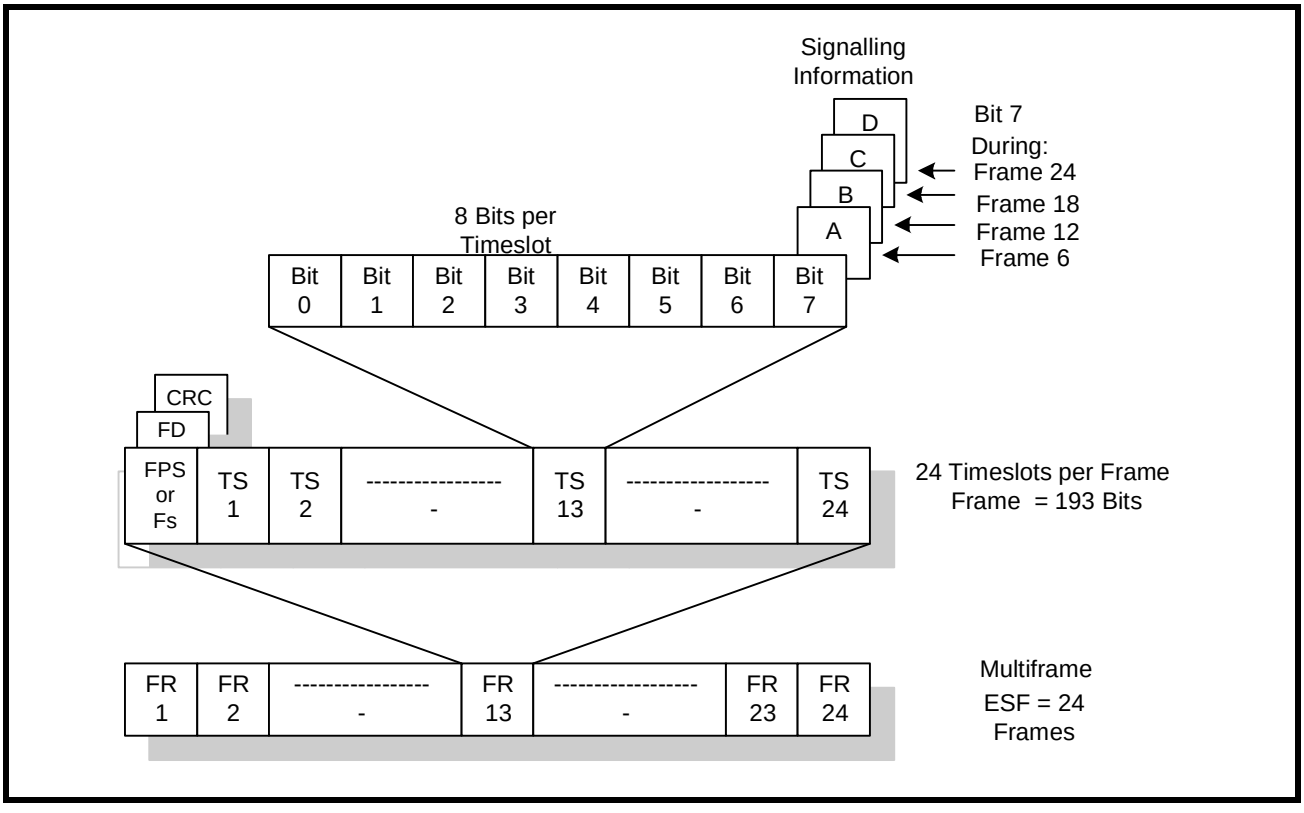


TABLE 11: EXTENDED SUPERFRAME FORMAT

FRAME	BIT	F-BITS			BIT USE IN EACH TIMESLOT		SIGNALLING CHANNEL		
		FPS	DL	CRC	TRAFFIC	SIG	16	4	2
1	0	----	m	----	1-8	----	----	----	----
2	193	----	----	C1	1-8	----	----	----	----
3	386	----	m	----	1-8	----	----	----	----
4	579	0	----	----	1-8	----	----	----	----
5	772	----	m	----	1-8	----	----	----	----
6	965	----	----	C2	1-7	8	A	A	A
7	1158	----	m	----	1-8	----	----	----	----
8	1351	0	----	----	1-8	----	----	----	----
9	1544	----	m	----	1-8	----	----	----	----
10	1737	----	----	C3	1-8	----	----	----	----
11	1930	----	m	----	1-8	----	----	----	----
12	2123	1	----	----	1-7	8	B	B	A
13	2316	----	m	----	1-8	----	----	----	----
14	2509	----	----	C4	1-8	----	----	----	----
15	2702	----	m	----	1-8	----	----	----	----
16	2895	0	----	----	1-8	----	----	----	----
17	3088	----	m	----	1-8	----	----	----	----
18	3281	----	----	C5	1-7	8	C	A	A
19	3474	----	m	----	1-8	----	----	----	----
20	3667	1	----	----	1-8	----	----	----	----
21	3860	----	m	----	1-8	----	----	----	----
22	4053	----	----	C6	1-8	----	----	----	----
23	4246	----	m	----	1-8	----	----	----	----
24	4439	1	----	----	1-7	8	D	B	A

NOTES:

1. *FPS indicates the Framing Pattern Sequence (...001011...)*
2. *DL indicates the 4kb/s Data Link with message bits m.*
3. *CRC indicates the cyclic redundancy check with bits C1 to C6*
4. *Signaling options include 16 state, 4 state and 2 state.*

10.6 T1 Non-Signaling Frame Format

The Non-Signaling (N) framing format is a simplified version of the T1 super frame. The N-Frame consists of four frames with two Fs bits and two Ft bits. The Fs bits can be used as a proprietary 4kbps data link transmission. Signaling is not supported in this framing format.

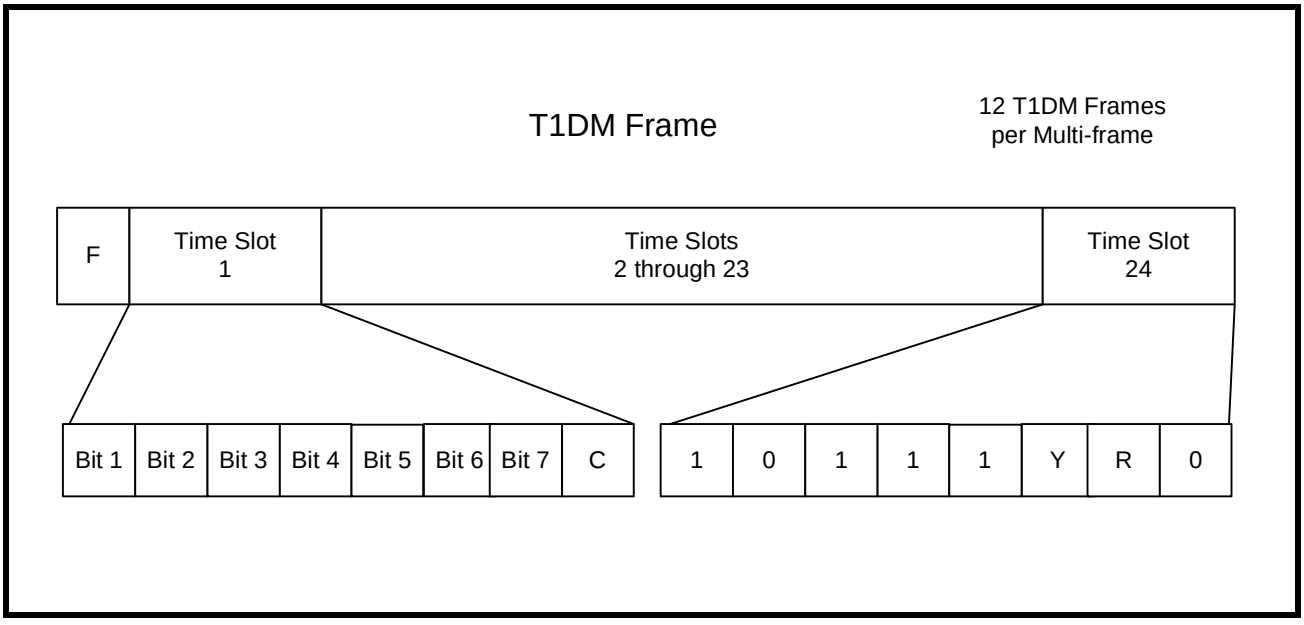
TABLE 12: NON-SIGNALING FRAMING FORMAT

FRAME	BIT	F-BITS	
		TERMINAL FRAMING FT	TERMINAL FRAMING FS
1	0	1	----
2	193	----	X
3	386	0	----
4	579	----	X

10.7 T1 Data Multiplexed Framing Format (T1DM)

T1DM uses a similar framing structure as the SF (D4), such that the Fs and Ft bits on the individual frame boundaries remain the same. The differentiation between T1DM and SF is within the payload time slots. Time slot 24 cannot be used for data when configured for T1DM. Time slot 24 is dedicated for a special synchronization byte as shown in **Figure 109**. The Y-bit is to carry the status of the Yellow Alarm. The R-bit is dedicated for a remote signaling bit typically not used. However, the framer allows this bit to carry an HDLC message. Time slots 1 through 23 are used to carry the seven bit word from each of the 23 DS-0 signals.

FIGURE 109. T1DM FRAME FORMAT



10.8 SLC-96 Format (SLC-96)

SLC framing mode allows synchronization to the SLC®96 data link pattern. This pattern described in Bellcore TR-TSY-000008, contains both signaling information and a framing pattern that overwrites the Fs bit of the SF framer pattern. See **Table 13**.

TABLE 13: SLC®96 FS BIT CONTENTS

FRAME #	FS BIT	FRAME #	FS BIT	FRAME #	FS BIT
2	0	26	C2	50	0
4	0	28	C3	52	M1
6	1	30	C4	54	M2
8	1	32	C5	56	M3
10	1	34	C6	58	A1
12	0	36	C7	60	A2
14	0	38	C8	62	S1
16	0	40	C9	64	S2
18	1	42	C10	66	S3
20	1	44	C11	68	S4
22	1	46	0	70	1
24	C1	48	1	72	0

NOTES:

1. *The SLC®96 frame format is similar to that of SF as shown in* **Table 10** *with the exceptions shown in this table.*
2. *C1 to C11 are concentrator bit fields.*
3. *M1 to M3 are Maintenance bit fields.*
4. *A1 and A2 are alarm bit fields.*
5. *S1 to S4 are line switch bit fields.*
6. *The Fs bits in frames 46, 48 and 70 are spoiler bit switch are used to protect against false multiframing.*

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUMS

Power Supply..... VDD_{IO} .. .. -0.5V to +3.465V VDD_{CORE}.....-0.5V to +1.890V		Power Rating PBGA Package.....1.39W (XRT86VL32/VL34) Power Rating STBGA and PBGA Package 2.4W (XRT86VL38)
Storage Temperature .....-65°C to 150°C		Input Logic Signal Voltage (Any Pin) .....-0.5V to + 5.5V
Operating Temperature Range.....-40°C to 85°C		ESD Protection (HBM).....>2000V
Supply Voltage ..... GND-0.5V to +VDD + 0.5V		Input Current (Any Pin) ..... ± 100mA

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C, VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{LL}	Data Bus Tri-State Bus Leakage Current	-10		+10	µA	
V_{IL}	Input Low voltage			0.8	V	
V_{IH}	Input High Voltage	2.0		VDD	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = -1.6mA
V_{OH}	Output High Voltage	2.4		VDD	V	I_{OH} = 40µA
I_{OC}	Open Drain Output Leakage Current				µA	
I_{IH}	Input High Voltage Current	-10		10	µA	V_{IH} = VDD
I_{IL}	Input Low Voltage Current	-10		10	µA	V_{IL} = GND

TABLE 14: XRT86VL32 POWER CONSUMPTION

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5% , T_A=25°C, UNLESS OTHERWISE SPECIFIED

MODE	SUPPLY VOLTAGE	IMPEDANCE	TERMINATION RESISTOR	TRANSFORMER RATIO		TYP.	MAX.	UNIT	TEST CONDITIONS
				RECEIVER	TRANSMITTER				
E1	3.3V	75Ω	Internal	1:1	1:2	776		mW	PRBS Pattern
E1	3.3V	120Ω	Internal	1:1	1:2	724		mW	PRBS Pattern
T1	3.3V	100Ω	Internal	1:1	1:2	829		mW	PRBS Pattern

TABLE 15: XRT86VL34 POWER CONSUMPTION

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5% , T_A=25°C, UNLESS OTHERWISE SPECIFIED									
MODE	SUPPLY VOLTAGE	IMPEDANCE	TERMINATION RESISTOR	TRANSFORMER RATIO		TYP.	MAX.	UNIT	TEST CONDITIONS
				RECEIVER	TRANSMITTER				
E1	3.3V	75Ω	Internal	1:1	1:2	1.035		W	PRBS Pattern
E1	3.3V	120Ω	Internal	1:1	1:2	0.965		W	PRBS Pattern
T1	3.3V	100Ω	Internal	1:1	1:2	1.105		W	PRBS Pattern

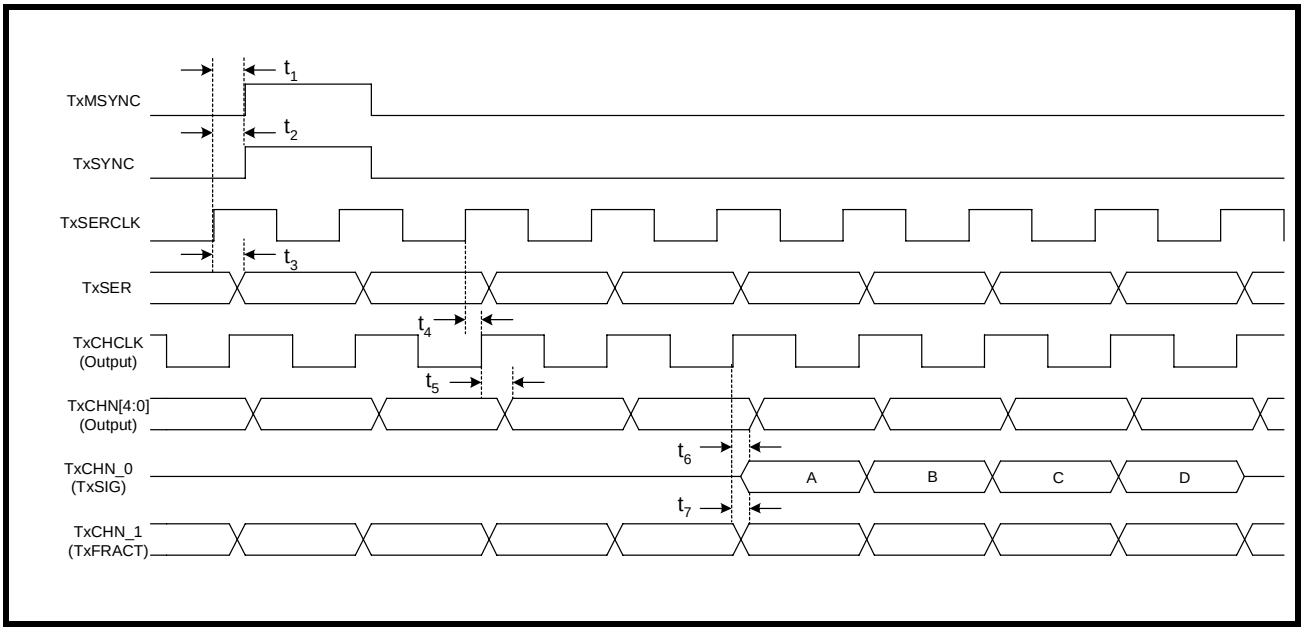
TABLE 16: XRT86VL38 POWER CONSUMPTION

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5% , T_A=25°C, UNLESS OTHERWISE SPECIFIED									
MODE	SUPPLY VOLTAGE	IMPEDANCE	TERMINATION RESISTOR	TRANSFORMER RATIO		TYP.	MAX.	UNIT	TEST CONDITIONS
				RECEIVER	TRANSMITTER				
E1	3.3V	75Ω	Internal	1:1	1:2	2.070		W	PRBS Pattern
E1	3.3V	120Ω	Internal	1:1	1:2	1.930		W	PRBS Pattern
T1	3.3V	100Ω	Internal	1:1	1:2	2.210		W	PRBS Pattern

AC ELECTRICAL CHARACTERISTICS TRANSMIT FRAMER (BASE RATE/NON-MUX)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
t_1	TxSERCLK to TxMSYNC delay			234	nS	
t_2	TxSERCLK to TxSYNC delay			230	nS	
t_3	TxSERCLK to TxSER data delay			230	nS	
t_4	Rising Edge of TxSERCLK to Rising Edge of TxCH-CLK			13	nS	
t_5	Rising Edge of TxCHCLK to Valid TxCHN[4:0] Data			6	nS	
t_6	TxSERCLK to TxSIG delay			230	nS	
t_7	TxSERCLK to TxFRACT delay			110	nS	

FIGURE 110. FRAMER SYSTEM TRANSMIT TIMING DIAGRAM (BASE RATE/NON-MUX)



AC ELECTRICAL CHARACTERISTICS RECEIVE FRAMER (BASE RATE/NON-MUX)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
RxSERCLK as an Output						
t_8	Rising Edge of RxSERCLK to Rising Edge of RxCASYNC			4	nS	
t_9	Rising Edge of RxSERCLK to Rising Edge of RxCRCSYNC			4	nS	
t_{10}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			4	nS	
t_{11}	Rising Edge of RxSERCLK to Rising Edge of RxSER			6	nS	
t_{12}	Rising Edge of RxSERCLK to Rising Edge of Valid RxCHN[4:0] data			6	nS	
RxSERCLK as an Input						
t_{13}	Rising Edge of RxSERCLK to Rising Edge of RxCASYNC			8	nS	
t_{14}	Rising Edge of RxSERCLK to Rising Edge of RxCRCSYNC			8	nS	
t_{15}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			10	nS	
t_{15}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Input)			230	nS	
t_{16}	Rising Edge of RxSERCLK to Rising Edge of RxSER			10	nS	
t_{17}	Rising Edge of RxSERCLK to Rising Edge of Valid RxCHN[4:0] data			9	nS	

FIGURE 111. FRAMER SYSTEM RECEIVE TIMING DIAGRAM (RXSERCLK AS AN OUTPUT)

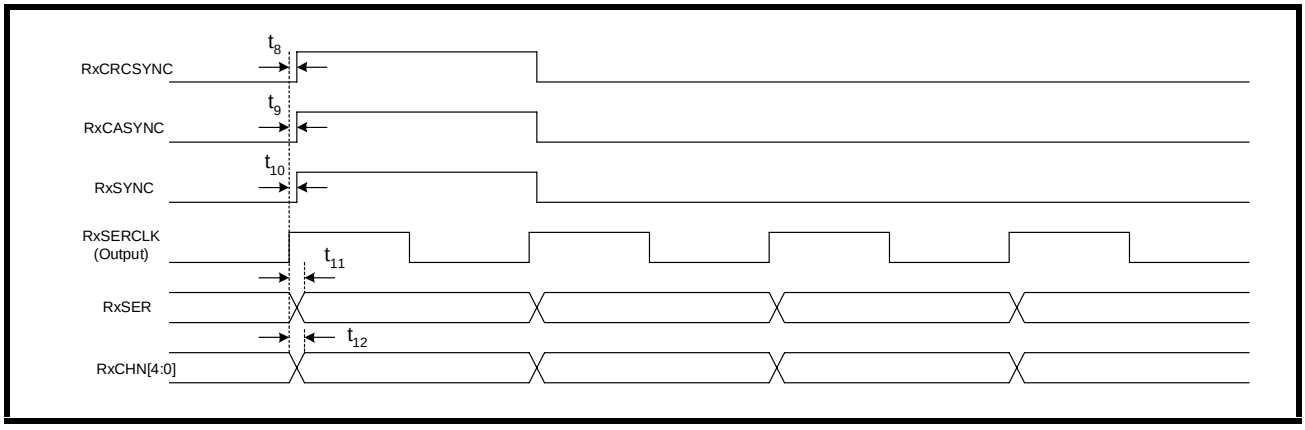
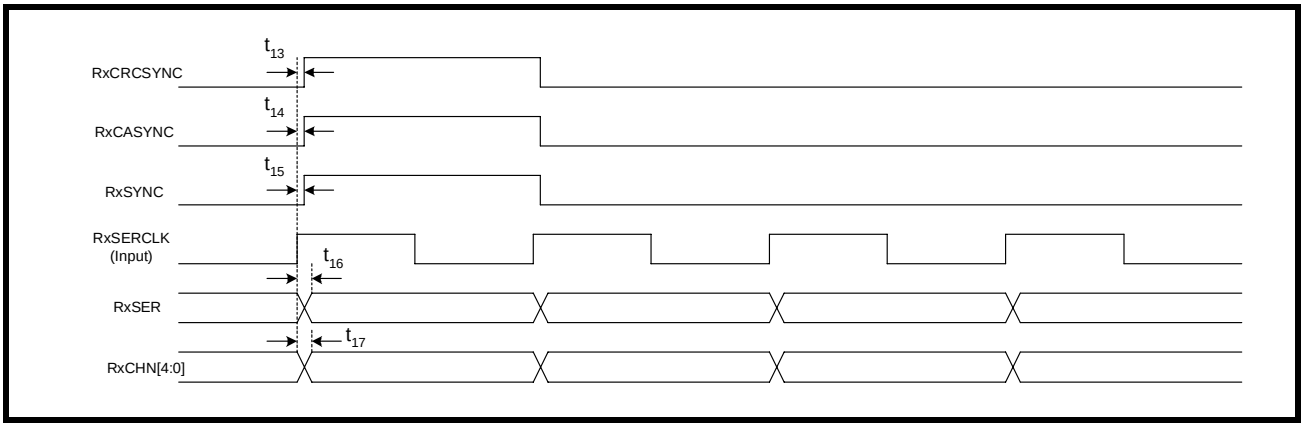


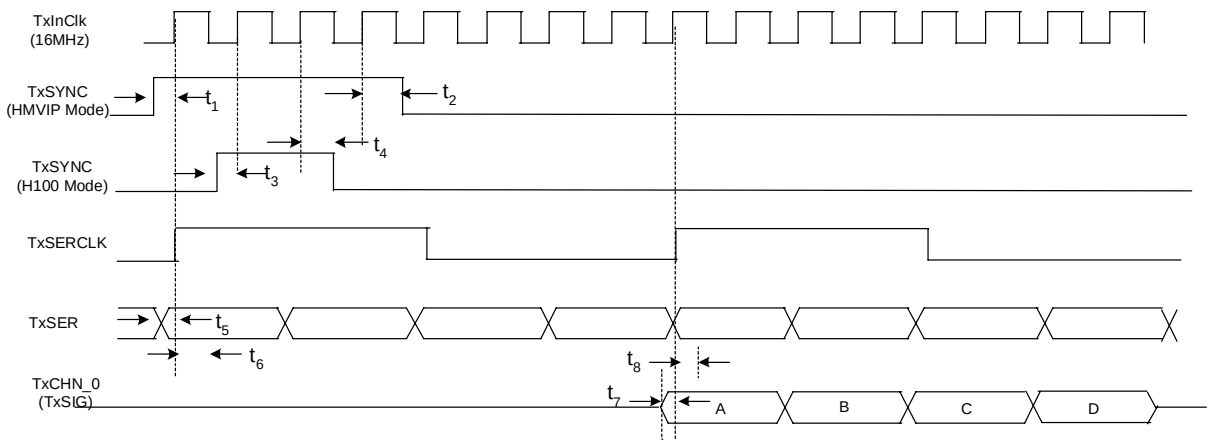
FIGURE 112. FRAMER SYSTEM RECEIVE TIMING DIAGRAM (RXSERCLK AS AN INPUT)



AC ELECTRICAL CHARACTERISTICS TRANSMIT FRAMER (HMVIP/H100 MODE)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
t_1	TxSYNC Setup Time - HMVIP Mode	7			nS	
t_2	TxSYNC Hold Time - HMVIP Mode	4			nS	
t_3	TxSYNC Setup Time - H100 Mode	7			nS	
t_4	TxSYNC Hold Time - H100 Mode	4			nS	
t_5	TxSER Setup Time - HMVIP and H100 Mode	6			nS	
t_6	TxSER Hold Time - HMVIP and H100 Mode	3			nS	
t_7	TxSIG Setup Time - HMVIP and H100 Mode	6			nS	
t_8	TxSIG Hold Time - HMVIP and H100 Mode	3			nS	

FIGURE 113. FRAMER SYSTEM TRANSMIT TIMING DIAGRAM (HMVIP AND H100 MODE)



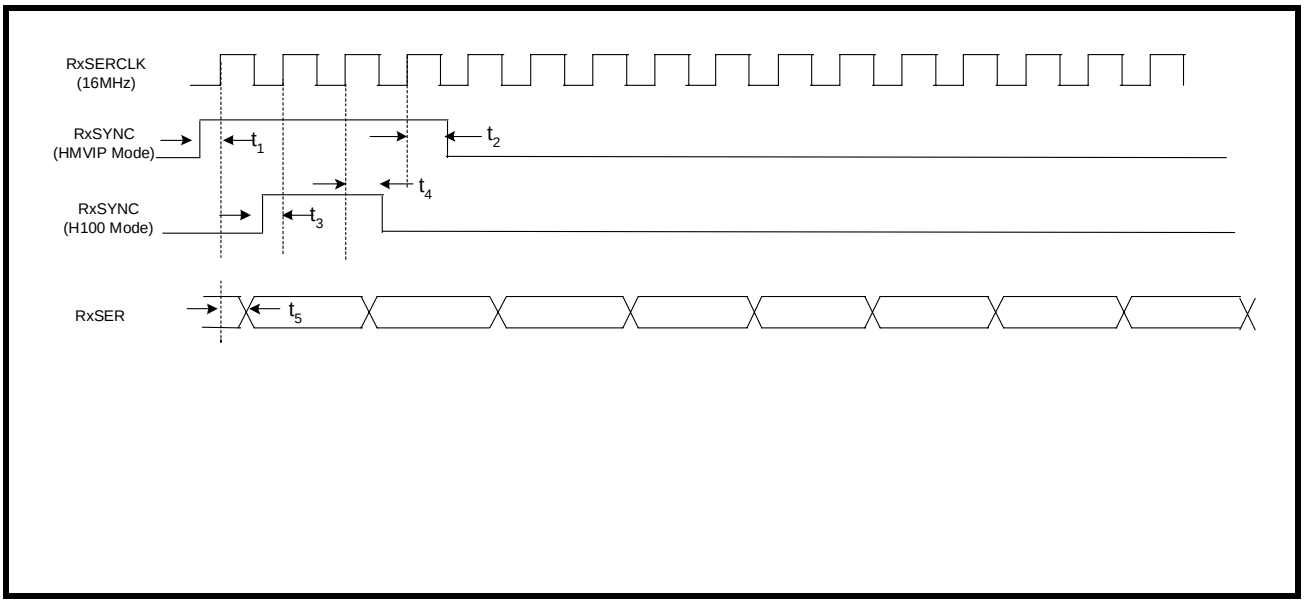
NOTE: *Setup and Hold time is not valid from TxInClk to TxSERCLK as TxInClk is used as the timing source for the back plane interface and TxSERCLK is used as the timing source on the line side.*

AC ELECTRICAL CHARACTERISTICS RECEIVE FRAMER (HMVIP/H100 MODE)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_1	RxSYNC Setup Time - HMVIP Mode	4			nS	
t_2	RxSYNC Hold Time - HMVIP Mode	3			nS	
t_3	RxSYNC Setup Time - H100 Mode	5			nS	
t_4	RxSYNC Hold Time - H100 Mode	3			nS	
t_5	Rising Edge of RxSERCLK to Rising Edge of RxSER delay			11	nS	

NOTE: *Both RxSERCLK and RxSYNC are inputs*

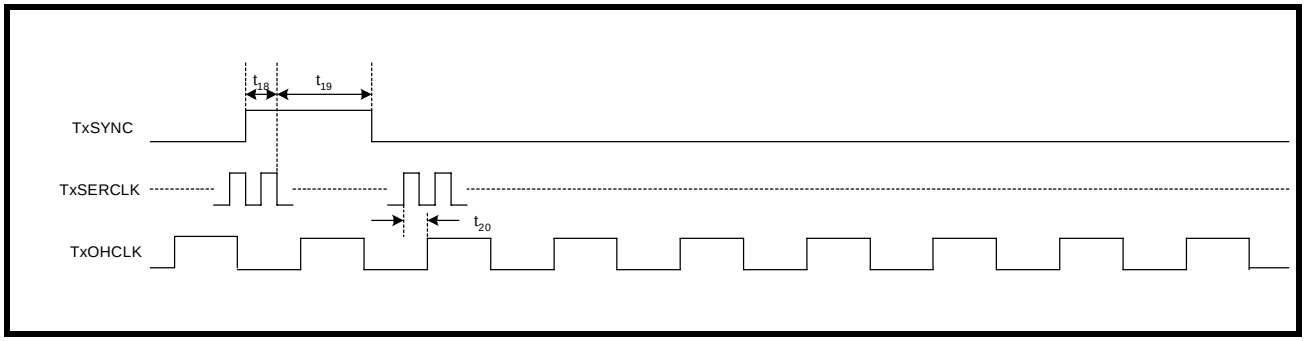
FIGURE 114. FRAMER SYSTEM RECEIVE TIMING DIAGRAM (HMVIP/H100 MODE)



AC ELECTRICAL CHARACTERISTICS TRANSMIT OVERHEAD FRAMER

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
t_{18}	TxSYNC Setup Time (Falling Edge TxSERCLK)	6			nS	
t_{19}	TxSYNC Hold Time (Falling Edge TxSERCLK)	4			nS	
t_{20}	Rising Edge of TxSERCLK to TxOHCLK			12	nS	

FIGURE 115. FRAMER SYSTEM TRANSMIT OVERHEAD TIMING DIAGRAM



AC ELECTRICAL CHARACTERISTICS RECEIVE OVERHEAD FRAMER

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
RxSERCLK as an Output						
t_{21}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			4	nS	
t_{22}	Rising Edge of RxSERCLK to Rising Edge of RxO-HCLK			6	nS	
t_{23}	Rising Edge of RxSERCLK to Rising Edge of RxOH			8	nS	
RxSERCLK as an Input						
t_{24}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			12	nS	
t_{24}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Input)			230	nS	
t_{25}	Rising Edge of RxSERCLK to Rising Edge of RxO-HCLK			12	nS	
t_{26}	Rising Edge of RxSERCLK to Rising Edge of RxOH			15	nS	

FIGURE 116. FRAMER SYSTEM RECEIVE OVERHEAD TIMING DIAGRAM (RXSERCLK AS AN OUTPUT)

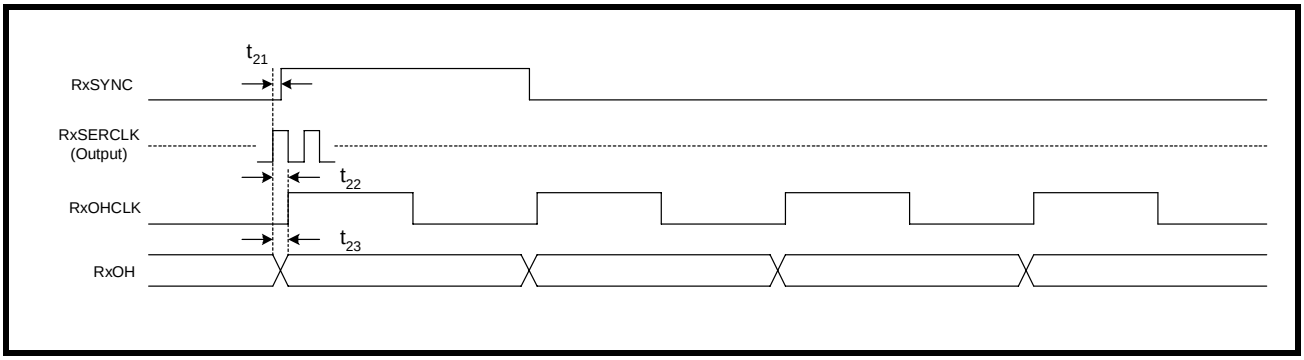


FIGURE 117. FRAMER SYSTEM RECEIVE OVERHEAD TIMING DIAGRAM (RXSERCLK AS AN INPUT)

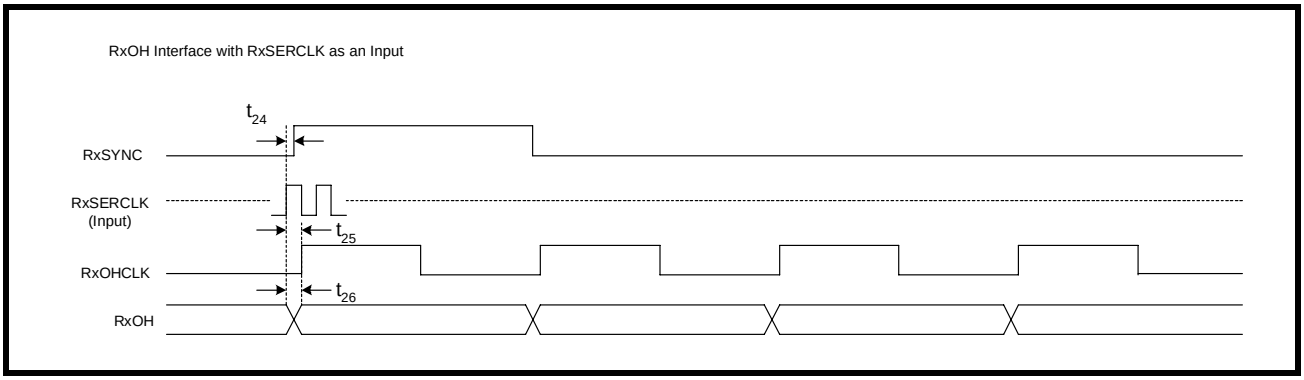


TABLE 17: E1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A= -40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal: Number of consecutive zeros before RLOS is set Input signal level at RLOS RLOS De-asserted	 15 12.5	 32 20		 dB % ones	Cable attenuation @1024kHz ITU-G.775, ETSI 300 233
Receiver Sensitivity (Short Haul with cable loss)	11			dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Receiver Sensitivity (Long Haul with cable loss)	0		43	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Input Impedance		15		kΩ	
Input Jitter Tolerance: 1 Hz 10kHz-100kHz	 37 0.2			 UIpp UIpp	 ITU G.823
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	 -	 20	 0.5	 kHz dB	 ITU G.736
Jitter Attenuator Corner Frequency (-3dB curve) (JABW=0) (JABW=1)	-	10 1.5	-	Hz Hz	ITU G.736
Return Loss: 51kHz - 102kHz 102kHz - 2048kHz 2048kHz - 3072kHz	 12 8 8	 -	 -	 dB dB dB	 ITU-G.703

TABLE 18: T1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal:					
Number of consecutive zeros before RLOS is set		175			
Input signal level at RLOS	15	20	-	dB	Cable attenuation @772kHz
RLOS Clear	12.5	-	-	% ones	ITU-G.775, ETSI 300 233
Receiver Sensitivity (Short Haul with cable loss)	12	-		dB	With nominal pulse amplitude of 3.0V for 100Ω termination
Receiver Sensitivity (Long Haul with cable loss)		-			With nominal pulse amplitude of 3.0V for 100Ω termination
Normal	0		36	dB	
Extended	0		45	dB	
Input Impedance		15	-	kΩ	
Jitter Tolerance:					
1Hz	138	-	-	UIpp	AT&T Pub 62411
10kHz - 100kHz	0.4	-	-		
Recovered Clock Jitter					
Transfer Corner Frequency	-	10	-	KHz	TR-TSY-000499
Peaking Amplitude	-		0.1	dB	
Jitter Attenuator Corner Frequency (-3dB curve)	-	6		-Hz	AT&T Pub 62411
Return Loss:					
51kHz - 102kHz	-	14	-	dB	
102kHz - 2048kHz	-	20	-	dB	
2048kHz - 3072kHz	-	16	-	dB	

TABLE 19: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude: 75Ω Application 120Ω Application	 2.13 2.70	 2.37 3.00	 2.60 3.30	 V V	Transformer with 1:2 ratio.
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05	-	ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05	-	ITU-G.703
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss: 51kHz -102kHz 102kHz-2048kHz 2048kHz-3072kHz	 8 8 8	 - - -	 - - -	 dB dB dB	 ETSI 300 166

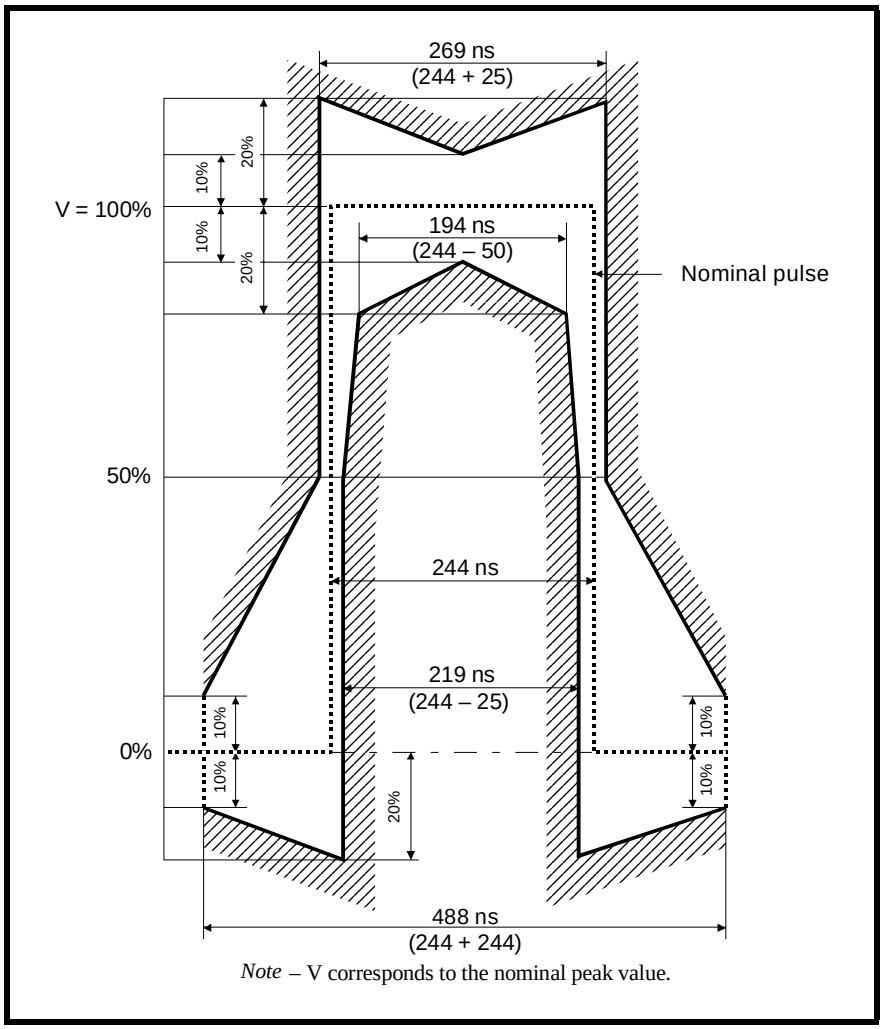
TABLE 20: E1 TRANSMIT RETURN LOSS REQUIREMENT

FREQUENCY	RETURN LOSS
	ETS 300166
51-102kHz	6dB
102-2048kHz	8dB
2048-3072kHz	8dB

TABLE 21: T1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude:	2.4	3.0	3.60	V	Transformer with 1:2 ratio.
Output Pulse Width	338	350	362	ns	ANSI T1.102
Output Pulse Width Imbalance	-	-	20	-	ANSI T1.102
Output Pulse Amplitude Imbalance	-	-	±200	mV	ANSI T1.102
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss: 51kHz -102kHz 102kHz-2048kHz 2048kHz-3072kHz	 - - -	 17 12 10	 - - -	 dB dB dB	

FIGURE 118. ITU G.703 PULSE TEMPLATE



Note – V corresponds to the nominal peak value.

TABLE 22: TRANSMIT PULSE MASK SPECIFICATION

Test Load Impedance	75Ω Resistive (Coax)	120Ω Resistive (twisted Pair)
Nominal Peak Voltage of a Mark	2.37V	3.0V
Peak voltage of a Space (no Mark)	0 ± 0.237V	0 ± 0.3V
Nominal Pulse width	244ns	244ns
Ratio of Positive and Negative Pulses Imbalance	0.95 to 1.05	0.95 to 1.05

FIGURE 119. DSX-1 PULSE TEMPLATE (NORMALIZED AMPLITUDE)

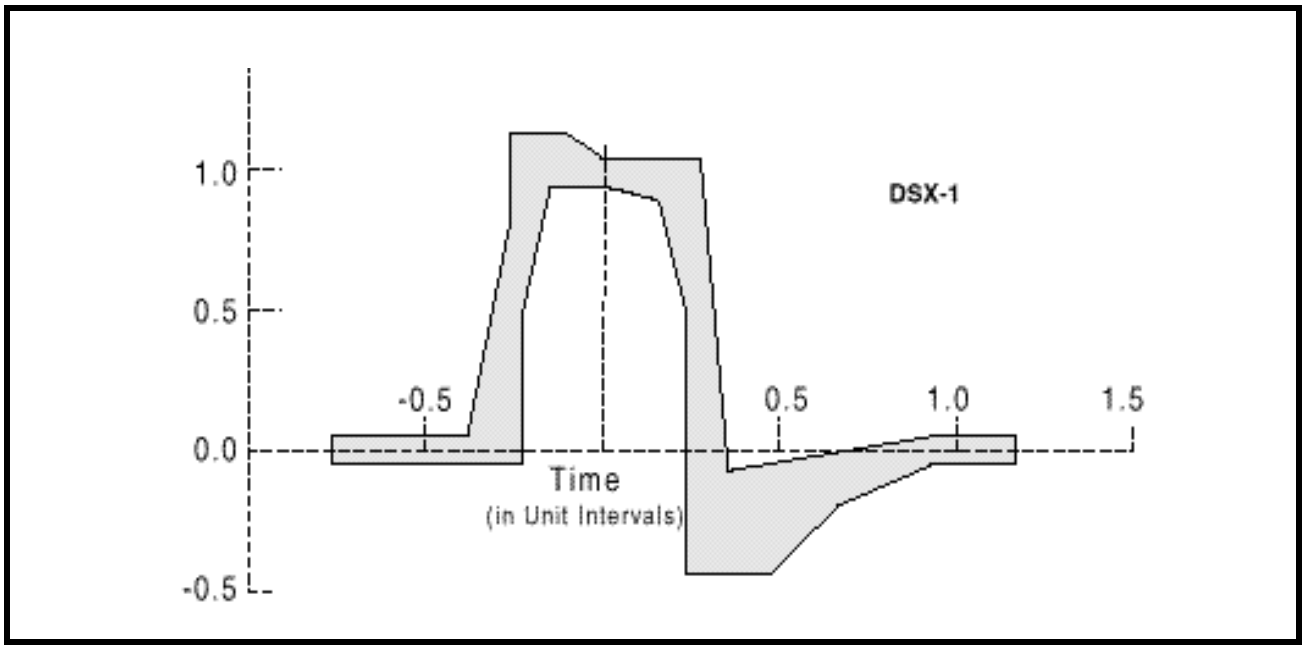


TABLE 23: DSX1 INTERFACE ISOLATED PULSE MASK AND CORNER POINTS

MINIMUM CURVE		MAXIMUM CURVE	
TIME (UI)	NORMALIZED AMPLITUDE	TIME (UI)	NORMALIZED AMPLITUDE
-0.77	-.05V	-0.77	.05V
-0.23	-.05V	-0.39	.05V
-0.23	0.5V	-0.27	.8V
-0.15	0.95V	-0.27	1.15V
0.0	0.95V	-0.12	1.15V
0.15	0.9V	0.0	1.05V
0.23	0.5V	0.27	1.05V
0.23	-0.45V	0.35	-0.07V
0.46	-0.45V	0.93	0.05V
0.66	-0.2V	1.16	0.05V
0.93	-0.05V		
1.16	-0.05V		

TABLE 24: AC ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, TA=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
MCLKIN Clock Duty Cycle		40	-	60	%
MCLKIN Clock Tolerance		-	±50	-	ppm

MICROPROCESSOR INTERFACE I/O TIMING

INTEL INTERFACE TIMING - ASYNCHRONOUS

The signals used for the Intel microprocessor interface are: Address Latch Enable (ALE), Read Enable ($\overline{RD}$), Write Enable ($\overline{WR}$), Chip Select ($\overline{CS}$), Address and Data bits. The microprocessor interface uses minimum external glue logic and is compatible with the timings of the 8051 or 80188 family of microprocessors. The ALE signal can be tied 'HIGH' if this signal is not available, and the corresponding timing interface is shown in **Figure 121** and **Table 26.**

FIGURE 120. INTEL µP INTERFACE TIMING DURING PROGRAMMED I/O READ AND WRITE OPERATIONS WHEN ALE IS NOT TIED 'HIGH'

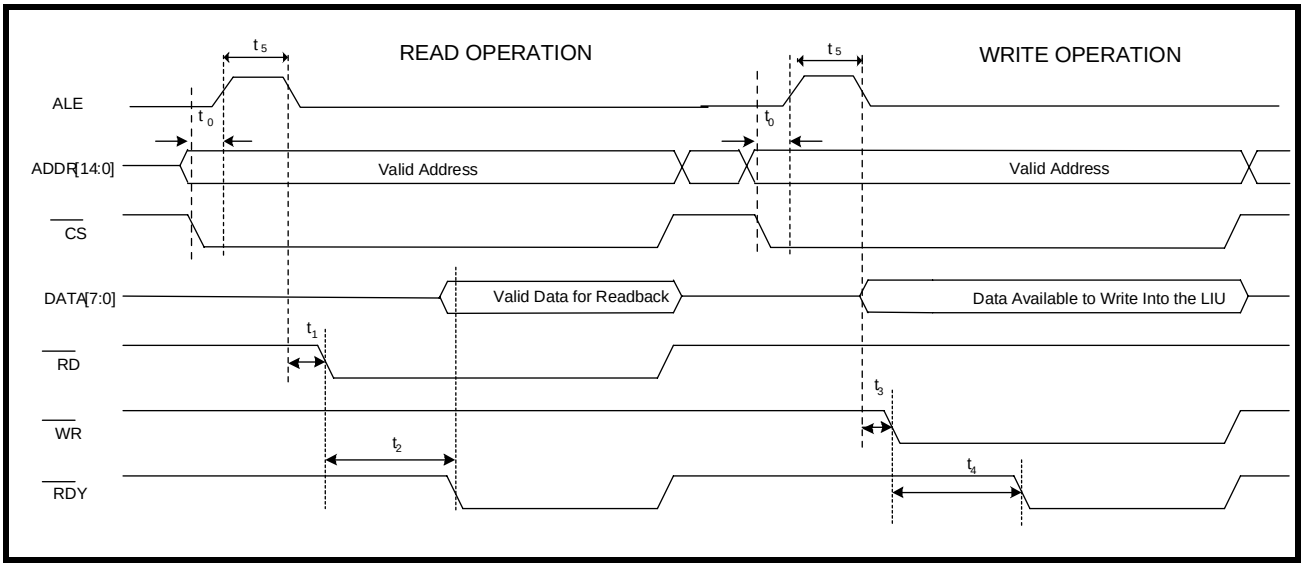


TABLE 25: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge and ALE Rising Edge	0	-	ns
t_1	ALE Falling Edge to $\overline{RD}$ Assert	5	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{RD}$ Pulse Width (t_2)	320	-	ns
t_3	ALE Falling Edge to $\overline{WR}$ Assert	5	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	320	ns

TABLE 25: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
NA	$\overline{WR}$ Pulse Width (t_4)	320	-	ns
t_5	ALE Pulse Width(t_5)	10		ns

FIGURE 121. INTEL µP INTERFACE TIMING DURING PROGRAMMED I/O READ AND WRITE OPERATIONS WHEN ALE IS TIED 'HIGH'

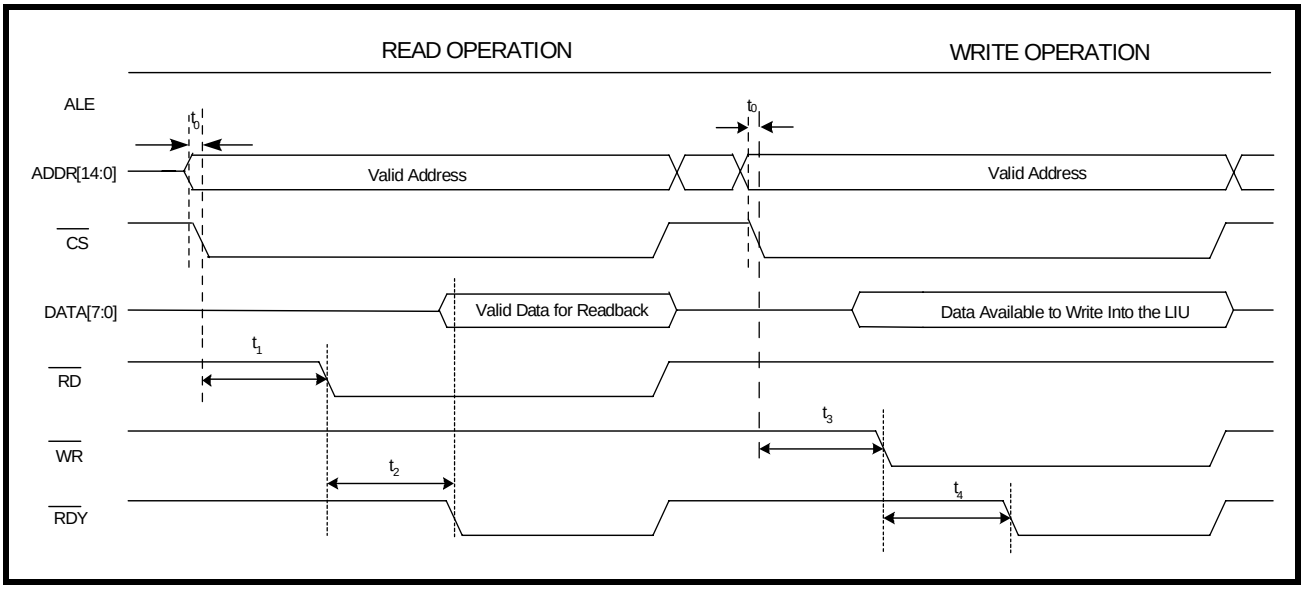


TABLE 26: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	0	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{RD}$ Pulse Width (t_2)	320	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	0	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{WR}$ Pulse Width (t_4)	320	-	ns

MOTOROLA ASYCHRONOUS INTERFACE TIMING

The signals used in the Motorola microprocessor interface mode are: Address Strobe (AS), Data Strobe ($\overline{DS}$), Read/Write Enable (R/$\overline{W}$), Chip Select ($\overline{CS}$), Address and Data bits. The interface is compatible with the timing of a Motorola 68000 microprocessor family. The interface timing is shown in **Figure 122**. The I/O specifications are shown in **Table 27**.

FIGURE 122. MOTOROLA ASYCHRONOUS MODE INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

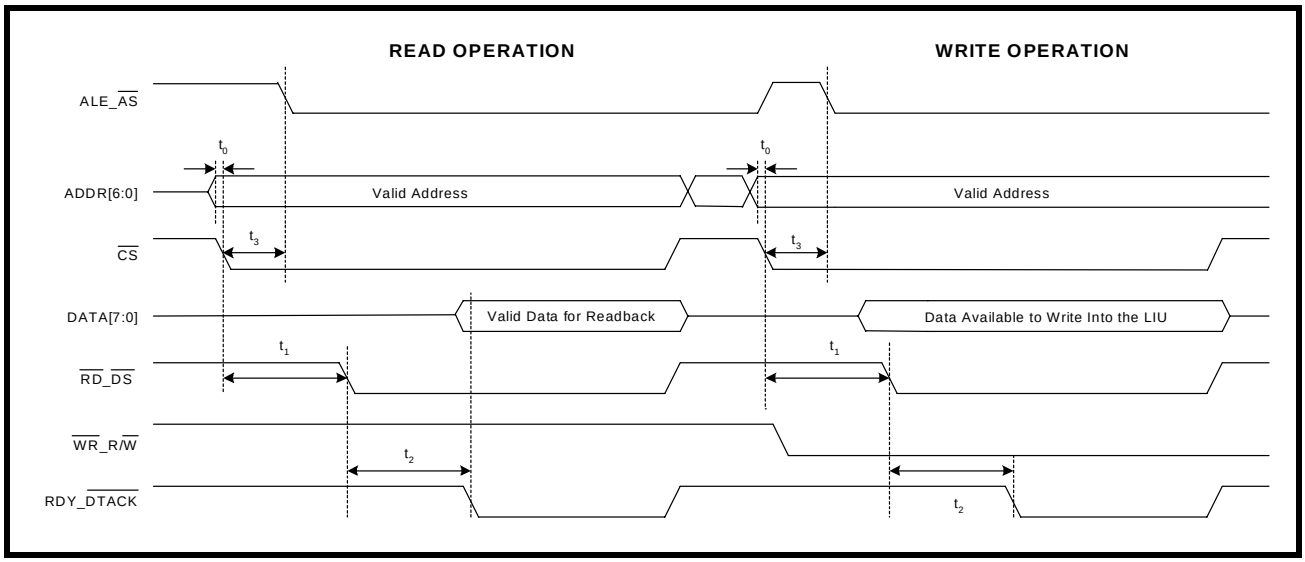


TABLE 27: MOTOROLA ASYCHRONOUS MODE MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{DS}$ (Pin $\overline{RD}_\overline{DS}$) Assert	0	-	ns
t_2	$\overline{DS}$ Assert to $\overline{DTACK}$ Assert	-	320	ns
NA	$\overline{DS}$ Pulse Width (t_2)	320	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{AS}$ (Pin ALE_AS) Falling Edge	0	-	ns

POWER PC 403 SYCHRONOUS INTERFACE TIMING

The signals used in the Power PC 403 Synchronus microprocessor interface mode are: Address Strobe (AS), Microprocessor Clock (uPCLK), Data Strobe ($\overline{DS}$), Read/Write Enable (R/$\overline{W}$), Chip Select ($\overline{CS}$), Address and Data bits. The interface timing is shown in **Figure 123**. The I/O specifications are shown in **Table 28**.

FIGURE 123. POWER PC 403 INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

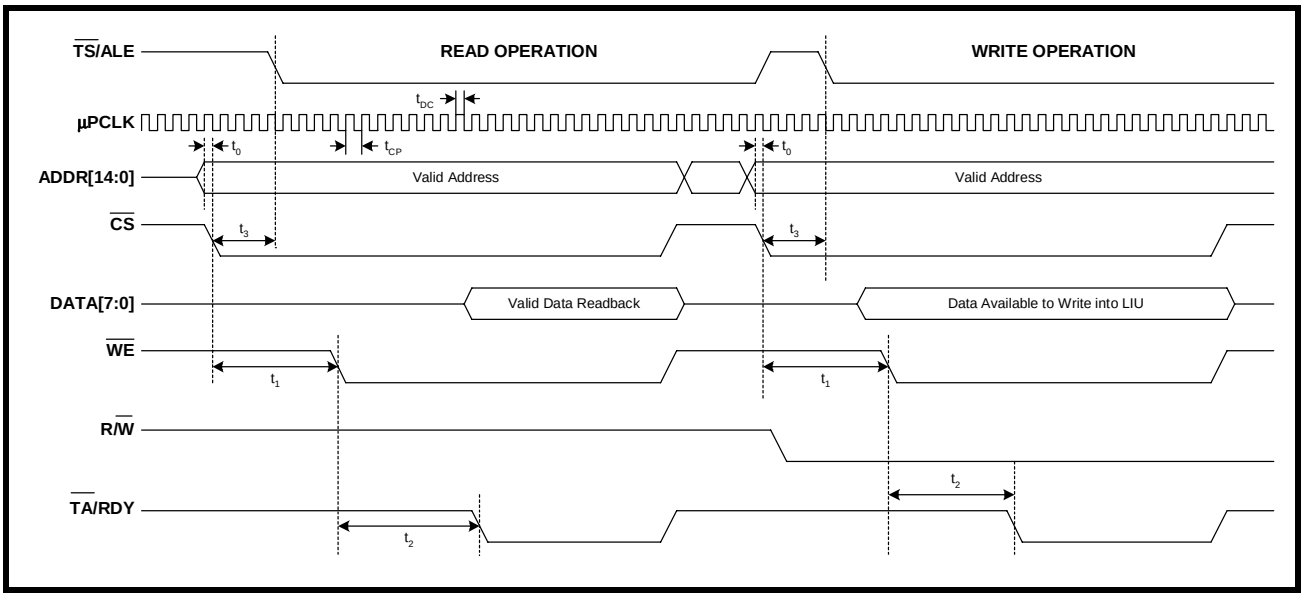


TABLE 28: POWER PC 403 MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{WE}$ Assert	0	-	ns
t_2	$\overline{WE}$ Assert to $\overline{TA}$ Assert	-	320	ns
NA	$\overline{WE}$ Pulse Width (t_2)	320	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{TS}$ Falling Edge	0	-	
t_{dc}	µPCLK Duty Cycle	40	60	%
t_{cp}	µPCLK Clock Period	20	-	ns

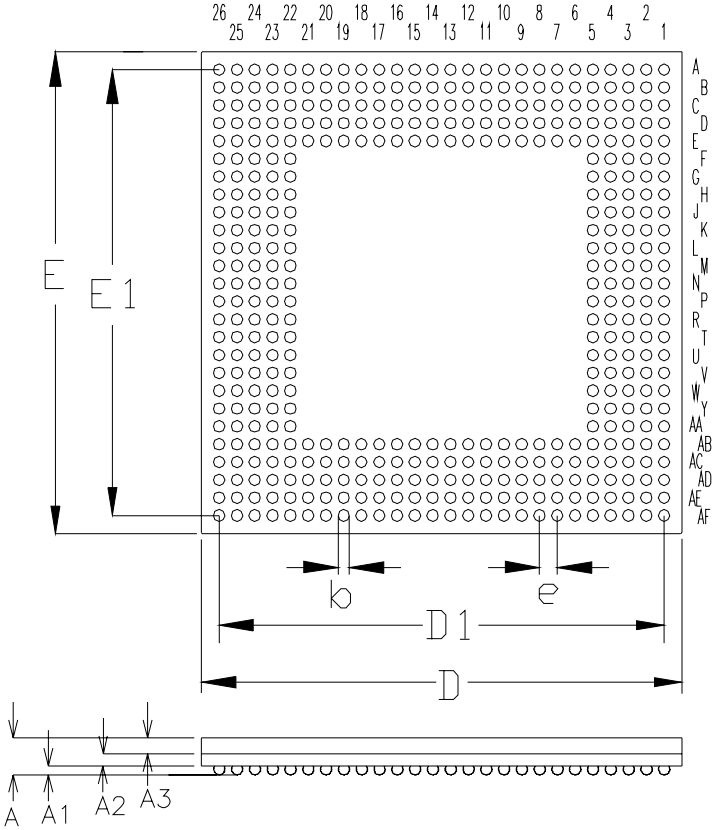
ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VL38IB	420 Plastic Ball Grid Array	-40°C to +85°C
XRT86VL38IB484	484 Shrink Thin Ball Grid Array	-40°C to +85°C
XRT86VL34IB	225 Plastic Ball Grid Array	-40°C to +85°C
XRT86VL32IB	225 Plastic Ball Grid Array	-40°C to +85°C

PACKAGE DIMENSIONS FOR 420 PLASTIC BALL GRID ARRAY

420 PLASTIC Thin Ball Grid Array
(35.0 mm x 35.0 mm, PBGA)

Rev. 1.00



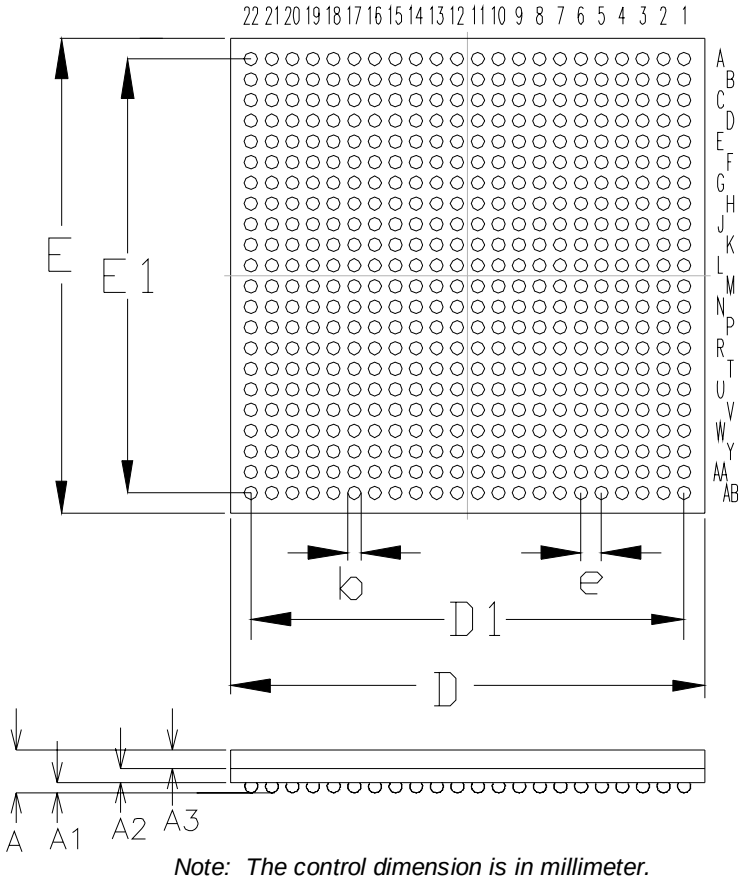
Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.085	0.098	2.16	2.50
A1	0.020	0.028	0.50	0.70
A2	0.020	0.024	0.51	0.61
A3	0.045	0.047	1.15	1.19
D	1.370	1.386	34.80	35.20
D1	1.2500 BSC		31.75 BSC	
E	1.370	1.386	34.80	35.20
E1	1.2500 BSC		31.75 BSC	
b	0.024	0.035	0.60	0.90
e	0.0500 BSC		1.27 TYP.	

PACKAGE DIMENSIONS FOR 484 SHRINK THIN BALL GRID ARRAY

484 Shrink Thin Ball Grid Array
(23.0 mm x 23.0 mm, STBGA)

Rev. 1.00



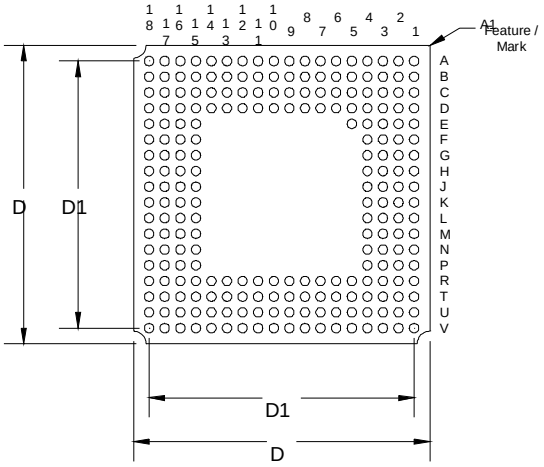
Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.071	0.082	1.80	2.08
A1	0.019	0.022	0.47	0.57
A2	0.019	0.022	0.48	0.56
A3	0.033	0.037	0.85	0.95
D	0.898	0.913	22.80	23.20
D1	0.8268 BSC		21.00 BSC	
E	0.898	0.913	22.80	23.20
E1	0.8268 BSC		21.00 BSC	
b	0.024	0.028	0.60	0.70
e	0.0394 BSC		1.00 BSC	

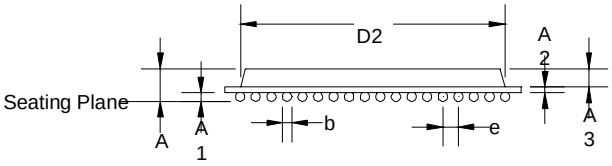
PACKAGE DIMENSIONS FOR 225 BALL PLASTIC BALL GRID ARRAY

225 Ball Plastic Ball Grid Array (19.0 mm x 19.0 mm, 1.0mm pitch PBGA)

Rev. 1.00



(A1 corner feature is mfger option)



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.049	0.096	1.24	2.45
A1	0.016	0.024	0.40	0.60
A2	0.013	0.024	0.32	0.60
A3	0.020	0.048	0.52	1.22
D	0.740	0.756	18.80	19.20
D1	0.669 BSC		17.00 BSC	
D2	0.665	0.669	16.90	17.00
b	0.020	0.028	0.50	0.70
e	0.039 BSC		1.00 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
1.2.0	7/14/06	First release of the XRT86VL3x Architecture Description.
1.2.1	7/25/06	Corrected TA/RDY waveform in figure 119.
1.2.2	1/25/07	Changed RD to RDY delay spec in the electrical timing specs. Clarified the HDLC controller section.

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