

## SWITCHING P-CHANNEL POWER MOS FET

### DESCRIPTION

The  $\mu$ PA2713GR is P-channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

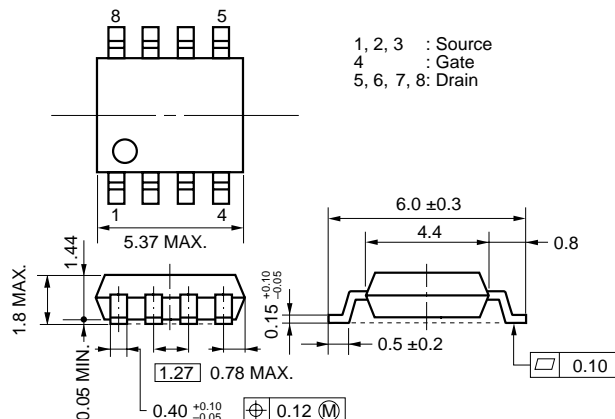
### FEATURES

- Low on-state resistance  
 $R_{DS(on)1} = 16 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -4.0 \text{ A)}$   
 $R_{DS(on)2} = 25 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -4.0 \text{ A)}$   
 $R_{DS(on)3} = 30 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -4.0 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 1600 \text{ pF TYP.}$
- Small and surface mount package (Power SOP8)

### ORDERING INFORMATION

| PART NUMBER    | PACKAGE    |
|----------------|------------|
| $\mu$ PA2713GR | Power SOP8 |

### PACKAGE DRAWING (Unit: mm)



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , All terminals are connected.)

|  |                |             |                  |
|--|----------------|-------------|------------------|
| Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ ) | $V_{DSS}$      | -30         | V                |
| Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )  | $V_{GSS}$      | $\pm 20$    | V                |
| Drain Current (DC)                                 | $I_{D(DC)}$    | $\pm 8$     | A                |
| Drain Current (pulse) <sup>Note1</sup>             | $I_{D(pulse)}$ | $\pm 32$    | A                |
| Total Power Dissipation <sup>Note2</sup>           | $P_{T1}$       | 2           | W                |
| Total Power Dissipation <sup>Note3</sup>           | $P_{T2}$       | 2           | W                |
| Channel Temperature                                | $T_{ch}$       | 150         | $^\circ\text{C}$ |
| Storage Temperature                                | $T_{stg}$      | -55 to +150 | $^\circ\text{C}$ |
| Single Avalanche Current <sup>Note4</sup>          | $I_{AS}$       | 8           | A                |
| Single Avalanche Energy <sup>Note4</sup>           | $E_{AS}$       | 6.4         | mJ               |

**Notes** 1.  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

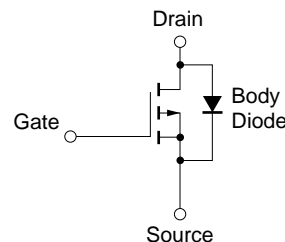
2. Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 2.2 \text{ mm}$

3. Mounted on a glass epoxy board (1 inch x 1 inch x 0.8 mm),  $PW = 10 \text{ sec}$

4. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = -15 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $L = 100 \mu\text{H}$ ,  $V_{GS} = -20 \rightarrow 0 \text{ V}$

**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

### EQUIVALENT CIRCUIT



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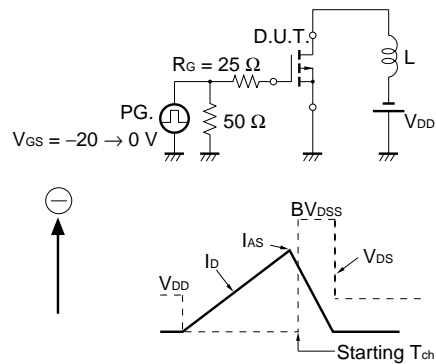
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**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)**

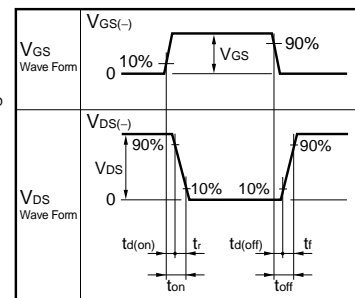
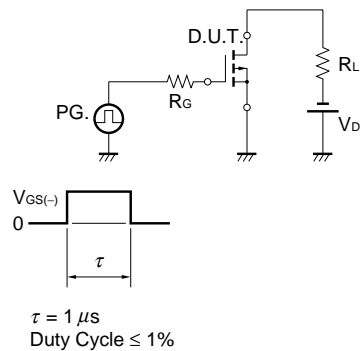
| CHARACTERISTICS                                     | SYMBOL               | TEST CONDITIONS                                   | MIN. | TYP. | MAX. | UNIT |
|---|----------------------|---|------|------|------|------|
| Zero Gate Voltage Drain Current                     | I <sub>DSS</sub>     | V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V    |      |      | -1   | μA   |
| Gate Leakage Current                                | I <sub>GSS</sub>     | V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V    |      |      | ±100 | nA   |
| Gate Cut-off Voltage <sup>Note</sup>                | V <sub>GS(off)</sub> | V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA   | -1.0 |      | -2.5 | V    |
| Forward Transfer Admittance <sup>Note</sup>         | y <sub>fs</sub>      | V <sub>DS</sub> = -10 V, I <sub>D</sub> = -4.0 A  | 6    | 14   |      | S    |
| Drain to Source On-state Resistance <sup>Note</sup> | R <sub>DS(on)1</sub> | V <sub>GS</sub> = -10 V, I <sub>D</sub> = -4.0 A  |      | 12   | 16   | mΩ   |
|   | R <sub>DS(on)2</sub> | V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -4.0 A |      | 17   | 25   | mΩ   |
|   | R <sub>DS(on)3</sub> | V <sub>GS</sub> = -4.0 V, I <sub>D</sub> = -4.0 A |      | 20   | 30   | mΩ   |
| Input Capacitance                                   | C <sub>iss</sub>     | V <sub>DS</sub> = -10 V                           |      | 1600 |      | pF   |
| Output Capacitance                                  | C <sub>oss</sub>     | V <sub>GS</sub> = 0 V                             |      | 450  |      | pF   |
| Reverse Transfer Capacitance                        | C <sub>rss</sub>     | f = 1 MHz   |      | 270  |      | pF   |
| Turn-on Delay Time                                  | t <sub>d(on)</sub>   | V <sub>DD</sub> = -15 V, I <sub>D</sub> = -4.0 A  |      | 9    |      | ns   |
| Rise Time   | t <sub>r</sub>       | V <sub>GS</sub> = -10 V                           |      | 15   |      | ns   |
| Turn-off Delay Time                                 | t <sub>d(off)</sub>  | R <sub>G</sub> = 10 Ω                             |      | 83   |      | ns   |
| Fall Time   | t <sub>f</sub>       |   |      | 43   |      | ns   |
| Total Gate Charge                                   | Q <sub>G</sub>       | V <sub>DD</sub> = -24 V                           |      | 35   |      | nC   |
| Gate to Source Charge                               | Q <sub>GS</sub>      | V <sub>GS</sub> = -10 V                           |      | 4.8  |      | nC   |
| Gate to Drain Charge                                | Q <sub>GD</sub>      | I <sub>D</sub> = 8 A                              |      | 10   |      | nC   |
| Body Diode Forward Voltage                          | V <sub>F(S-D)</sub>  | I <sub>F</sub> = 8 A, V <sub>GS</sub> = 0 V       |      | 0.81 |      | V    |
| Reverse Recovery Time                               | t <sub>rr</sub>      | I <sub>F</sub> = 8 A, V <sub>GS</sub> = 0 V       |      | 43   |      | ns   |
| Reverse Recovery Charge                             | Q <sub>rr</sub>      | di/dt = 100 A/μs                                  |      | 29   |      | nC   |

**Note** Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

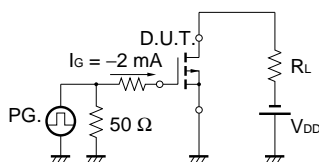
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



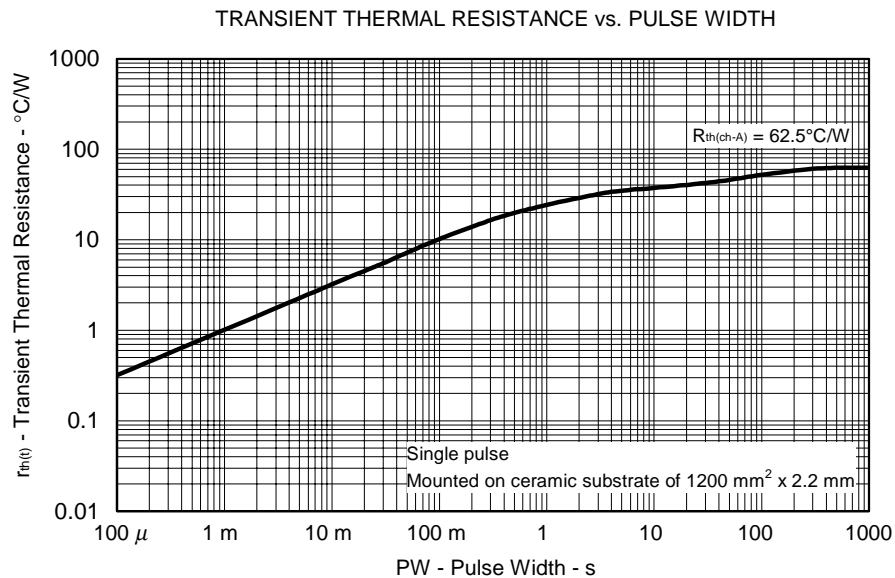
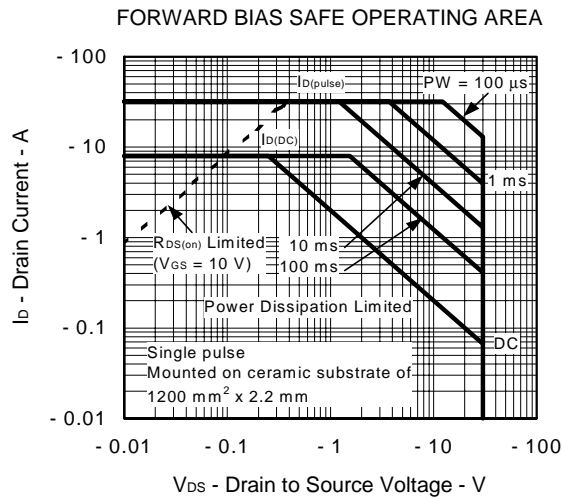
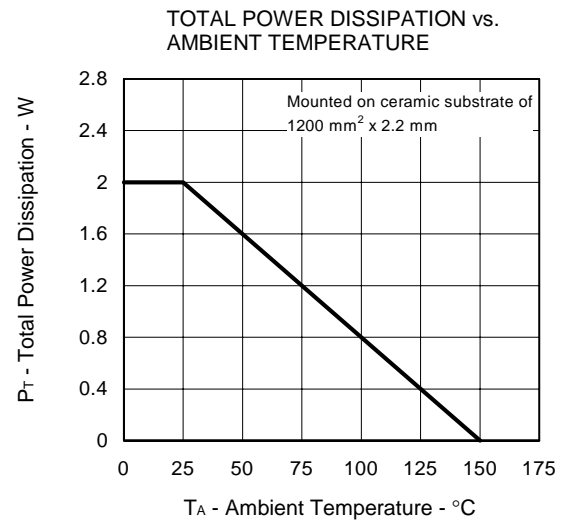
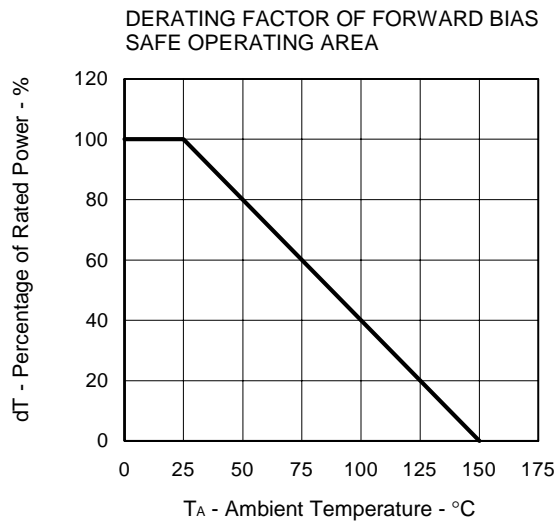
**TEST CIRCUIT 2 SWITCHING TIME**



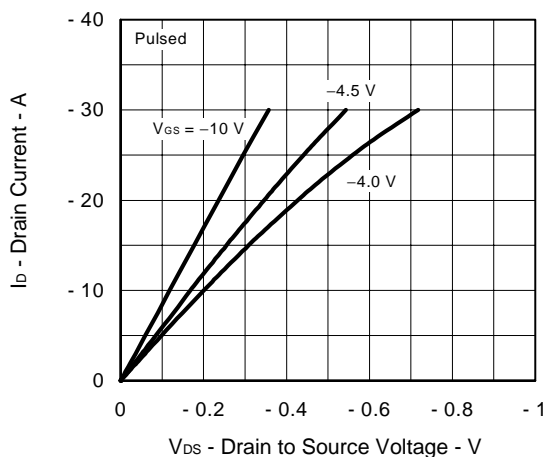
**TEST CIRCUIT 3 GATE CHARGE**



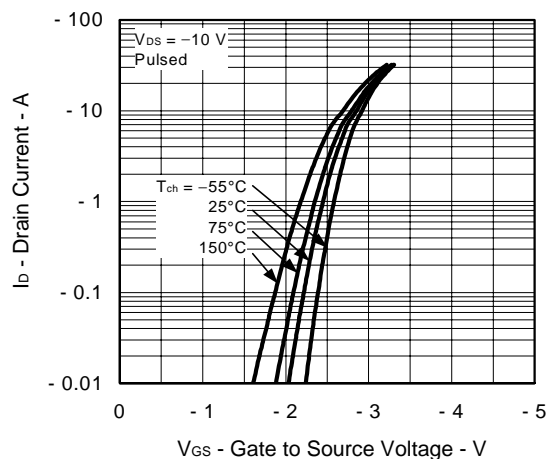
**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , All terminals are connected.)**



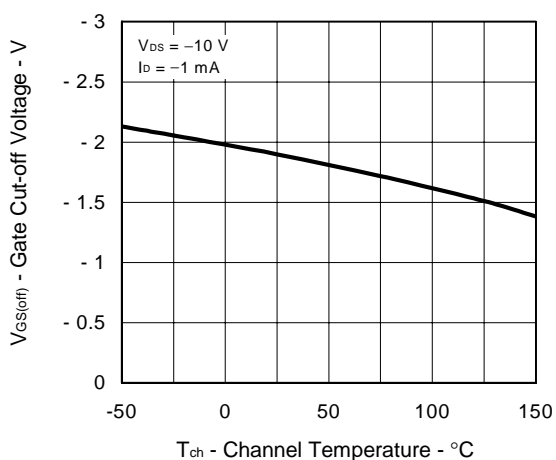
DRAIN CURRENT vs.  
DRAIN TO SOURCE VOLTAGE



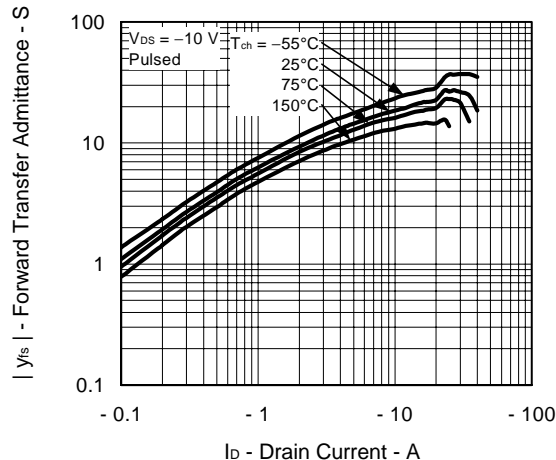
FORWARD TRANSFER CHARACTERISTICS



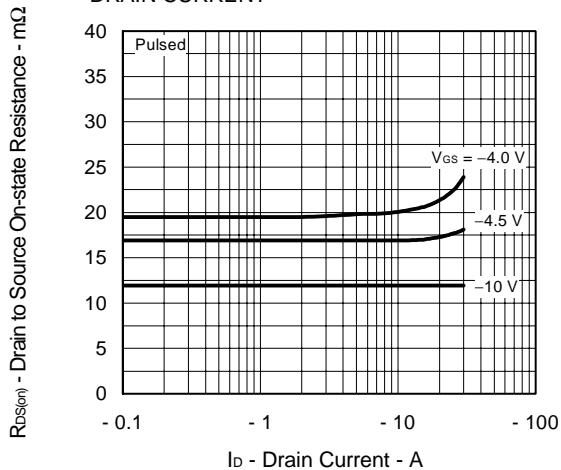
GATE CUT-OFF VOLTAGE vs.  
CHANNEL TEMPERATURE



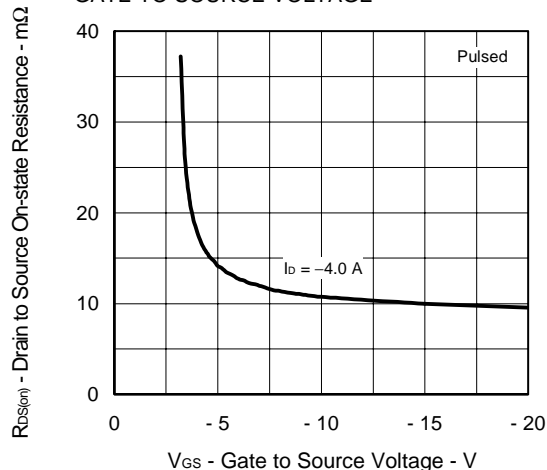
FORWARD TRANSFER ADMITTANCE vs.  
DRAIN CURRENT



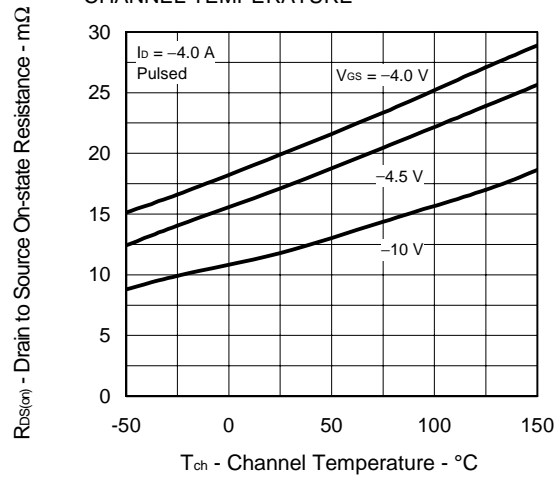
DRAIN TO SOURCE ON-STATE RESISTANCE vs.  
DRAIN CURRENT



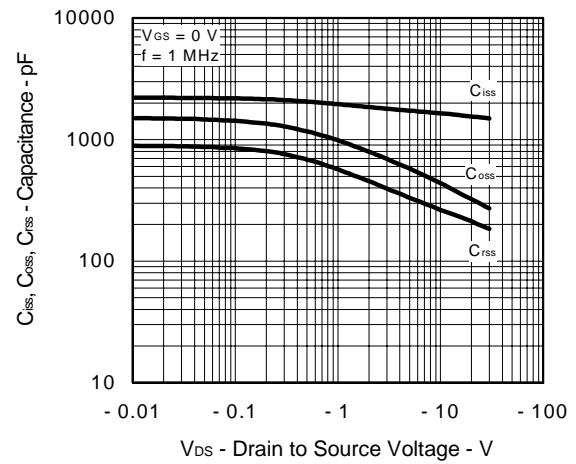
DRAIN TO SOURCE ON-STATE RESISTANCE vs.  
GATE TO SOURCE VOLTAGE



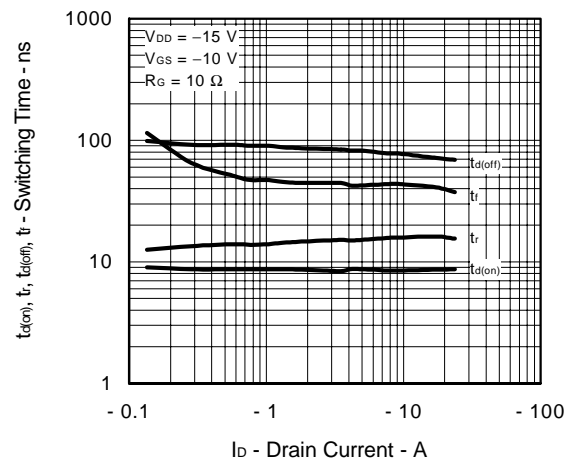
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



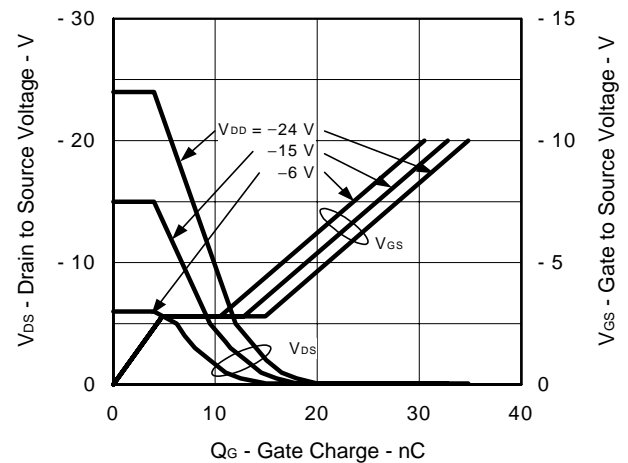
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



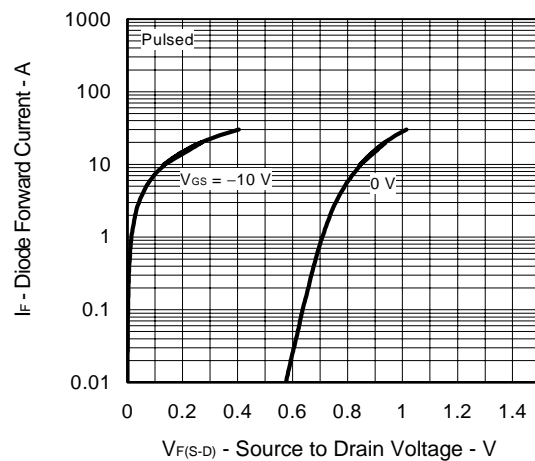
SWITCHING CHARACTERISTICS



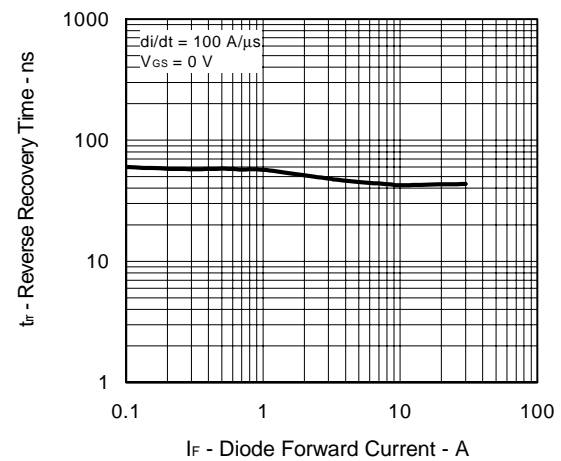
DYNAMIC INPUT/OUTPUT CHARACTERISTICS

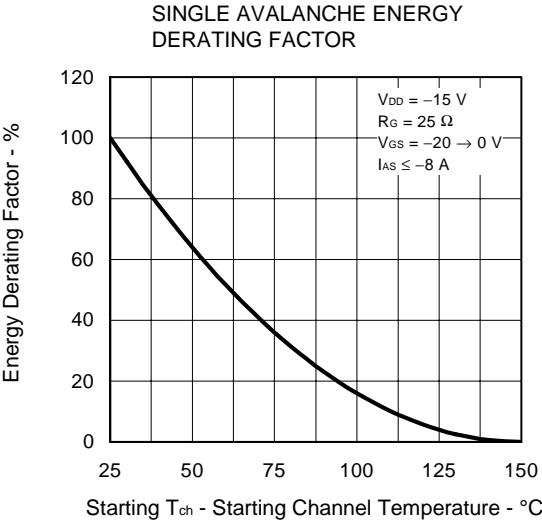
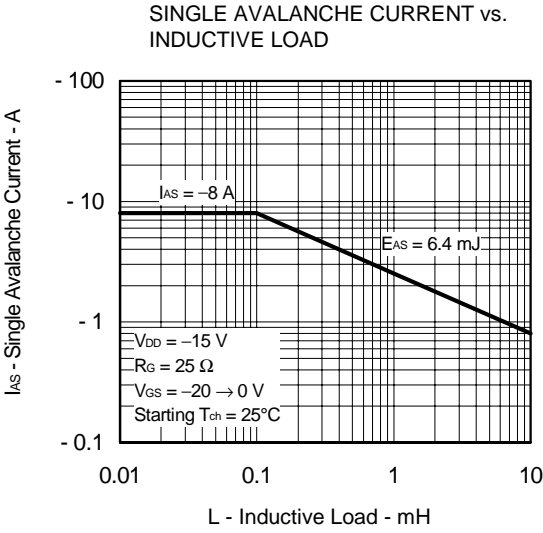


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT





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