ICS570A
Multiplier and Zero Delay Buffer

Description

The ICS570A is a high performance Zero Delay Buffer (ZDB) which integrates ICS' proprietary analog/digital Phase Locked Loop (PLL) techniques. ICS introduced the world standard for these devices in 1992 with the debut of the AV9170. The ICS570A, part of ICS' ClockBlocks™ family, was designed as a performance upgrade to meet today's higher speed and lower voltage requirements. The zero delay feature means that the rising edge of the input clock aligns with the rising edges of both outputs, giving the appearance of no delay through the device. There are two outputs on the chip, one being a low-skew divide by two of the other. The chip has an all-chip power down/tri-state mode that stops the internal PLL and puts both outputs into the high impedance state.

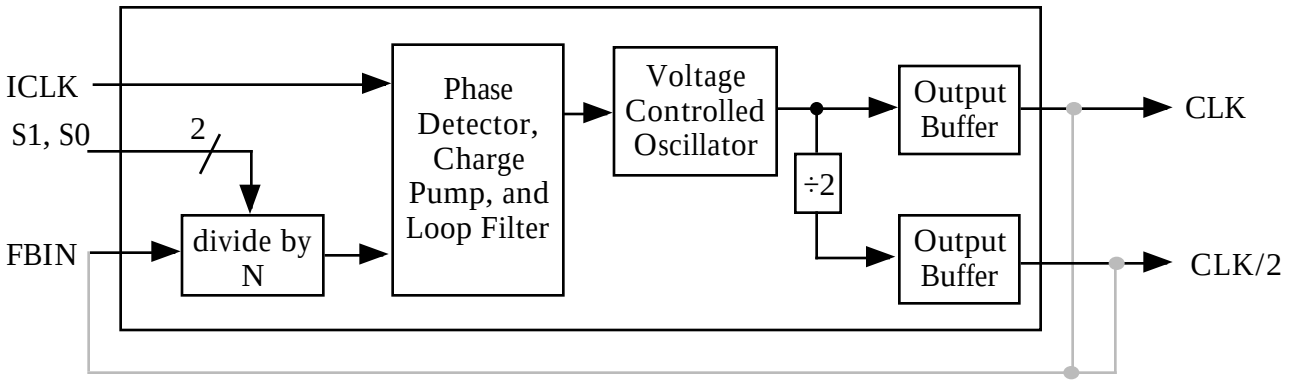
The chip is ideal for synchronizing outputs in a large variety of systems, from personal computers to data communications to video. By allowing off-chip feedback paths, the ICS570A can eliminate the delay through other devices.

The ICS570A was done to improve jitter from the original ICS570, and so it is recommended for all new designs.

Features

- Packaged in 8 pin SOIC.
- Pin-for-pin replacement and upgrade to ICS570
- Functional equivalent to AV9170 (not a pin-for-pin replacement).
- Low input to output skew of 500 ps max.
- Low skew (250 ps) outputs. One is ÷ 2 of other.
- Ability to choose between 14 different multipliers from 0.5X to 32X.
- Input clock frequency up to 150 MHz at 3.3V.
- Can recover poor input clock duty cycle.
- Output clock duty cycle of 45/55.
- Power Down and Tri-State Mode.
- Full CMOS clock swings with 25mA drive capability at TTL levels.
- Advanced, low power CMOS process.
- Operating voltage of 3.0 to 5.5 V.
- Industrial temperature version available

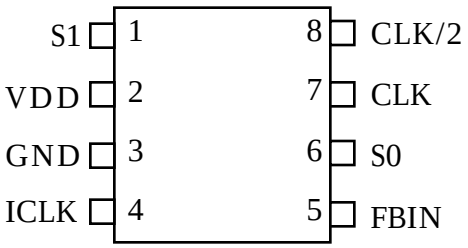
Block Diagram



External feedback can come from CLK or CLK/2 (see table on page 2).

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Pin Assignment



8 pin SOIC

Clock Multiplier Decoding Table

(Multiplies input clock by shown amount)

		FBIN from CLK		FBIN from CLK/2		ICLK Input Range
S1	S0	CLK	CLK/2	CLK	CLK/2	FB from CLK/2 *
#1	#6	pin # 7	pin # 8	pin # 7	pin # 8	(3.3V, MHz)
0	0	Power Down and Tri-State				-
0	M	x3	x1.5	x6	x3	2.5 to 25
0	1	x4	x2	x8	x4	2.5 to 19
M	0	x8	x4	x16	x8	2.5 to 9.5
M	M	x6	x3	x12	x6	2.5 to 12.5
M	1	x10	x5	x20	x10	2.5 to 7.5
1	0	x1	÷2	x2	x1	5 to 75
1	M	x16	x8	x32	x16	2.5 to 5
1	1	x2	x1	x4	x2	2.5 to 37.5

0 = connect directly to ground.
M = leave unconnected (self-biases to VDD/2).
1 = connect directly to VDD.
*Input range with CLK feedback is double that for CLK/2.

Pin Descriptions

Number	Name	Type	Description
1	S1	I	Select 1 for output clock. Connect to GND, VDD, or float per decoding table above.
2	VDD	P	Connect to +3.3V or +5V.
3	GND	P	Connect to ground.
4	ICLK	CI	Reference clock input.
5	FBIN	CI	Feedback clock input.
6	S0	I	Select 0 for output clock. Connect to GND, VDD, or float per decoding table above.
7	CLK	O	Clock output per Table above.
8	CLK/2	O	Clock output per Table above. Low skew divide by two of pin 7 clock.

Key: CI = clock input, I = input, O = output, P = power supply connection

External Components

The ICS570A requires a 0.01 µF decoupling capacitor to be connected between VDD and GND. It must be connected close to the ICS570A to minimize lead inductance. No external power supply filtering is required for this device. A 27 Ω terminating resistor can be used next to each output pin.

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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (Note 1)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Output	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature	ICS570M	0		70	°C
	ICS570MI	-40		85	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3V or 5.0V unless otherwise noted)					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH, VDD=5V	ICLK, FBIN	2			V
Input Low Voltage, VIL, VDD=5V	ICLK, FBIN			0.8	V
Input High Voltage, VIH	S0, S1	VDD-0.5			V
Input High Voltage, VIM (mid-level)	S0, S1		VDD/2		V
Input Low Voltage, VIL	S0, S1			0.5	V
Output High Voltage, VOH, CMOS level	IOH=-4mA	VDD-0.4			V
Output High Voltage, VOH	IOH=-12mA	2.4			V
Output Low Voltage, VOL	IOL=12mA			0.4	V
IDD Operating Supply Current, 50 in, 100 out	No Load, 5.0V		22		mA
IDD Operating Supply Current, 50 in, 100 out	No Load, 3.3V		12		mA
Short Circuit Current	Each Output		±50		mA
Input Capacitance, S1, S0			5		pF
AC CHARACTERISTICS (VDD = 3.3V or 5.0V unless otherwise noted)					
Input Frequency, ICLK (see table on page 2)		2.5		150	MHz
Output Clock Frequency, CLK		10		150	MHz
Skew of output clocks	Note 2		50	150	ps
Input skew, ICLK to FBIN Note 2	VDD=3.3V, CLK>10MHz	-500		500	ps
Input skew, ICLK to FBIN Note 2	VDD=3.3V, CLK<5MHz	-1.0		1.0	ns
Input skew, ICLK to FBIN Note 2	VDD=3.3V, CLK<10MHz	-750		750	ps
Input skew, ICLK to FBIN Note 2	VDD=5V, CLK<10MHz	-1.5		1.5	ns
Input skew, ICLK to FBIN Note 2	VDD=5V, CLK>10MHz	-1.0		1.0	ns
Output Clock Rise Time, 3.3V	0.8 to 2.0V, note 3		0.75		ns
Output Clock Fall Time, 3.3V	2.0 to 0.8V, note 3		0.75		ns
Output Clock Rise Time, 5V	0.8 to 2.0V, note 3		0.5		ns
Output Clock Fall Time, 5V	2.0 to 0.8V, note 3		0.5		ns
Output Clock Duty Cycle	at VDD/2	45	49 to 51	55	%

Notes 1. Stresses beyond these can permanently damage the device
2. Assumes clocks with same rise time, measured from rising edges at VDD/2.
3. With 27 Ω terminating resistor and 15 pF loads.

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All jitter values measured at 25 °C with 27Ω series termination resistors and 15pF loads on both CLK and CLK/2. The feedback is from CLK/2 to FBIN. Note that if an output is unused, it should be left unconnected. This will give lower output jitter.

One Sigma Clock Period Jitter (ps), VDD = 3.3 V

CLK

ICLK Frequency (MHz)	CLK Frequency (MHz)		
	<20	20 - 50	>50
<5	145	70	85
5 - 10	100	65	85
>10	—	50	85

CLK/2

ICLK Frequency (MHz)	CLK/2 Frequency (MHz)		
	<10	10 - 25	>25
<5	200	100	20
5 - 10	135	70	20
>10	—	50	20

Absolute Clock Period Jitter (ps), VDD = 3.3V

CLK

ICLK Frequency (MHz)	CLK Frequency (MHz)		
	<20	20 - 50	>50
<5	±850	±350	±180
5 - 10	±370	±270	±180
>10	—	±140	±180

CLK/2

ICLK Frequency (MHz)	CLK/2 Frequency (MHz)		
	<10	10 - 25	>25
<5	±1100	±600	±90
5 - 10	±500	±350	±90
>10	—	±160	±90

One Sigma Clock Period Jitter (ps), VDD = 5 V

CLK

ICLK Frequency (MHz)	CLK Frequency (MHz)		
	<20	20 - 50	>50
<5	130	100	120
5 - 10	120	100	120
>10	—	70	120

CLK/2

ICLK Frequency (MHz)	CLK/2 Frequency (MHz)		
	<10	10 - 25	>25
<5	50	25	20
5 - 10	60	35	20
>10	—	30	25

Absolute Clock Period Jitter (ps), VDD = 5 V

CLK

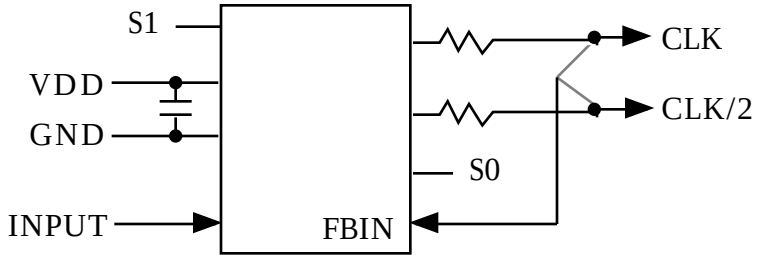
ICLK Frequency (MHz)	CLK Frequency (MHz)		
	<20	20 - 50	>50
<5	±270	±180	±230
5 - 10	±270	±220	±230
>10	—	±160	±230

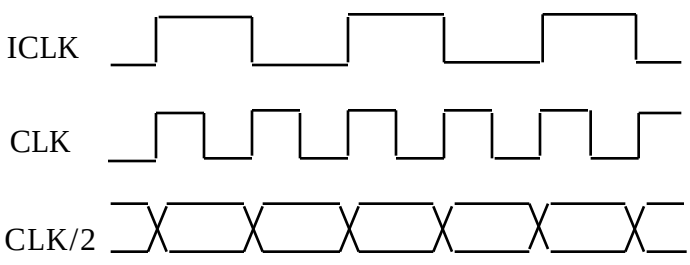
CLK/2

ICLK Frequency (MHz)	CLK/2 Frequency (MHz)		
	<10	10 - 25	>25
<5	±170	±100	±50
5 - 10	±210	±100	±80
>10	—	±100	±90

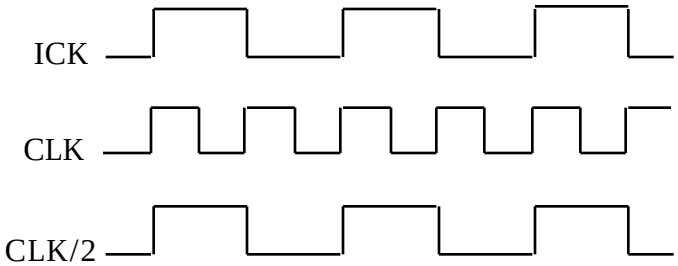
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Recommended Circuit:





x2 Mode (S1, S0 = 1, 1)
CLK Feedback

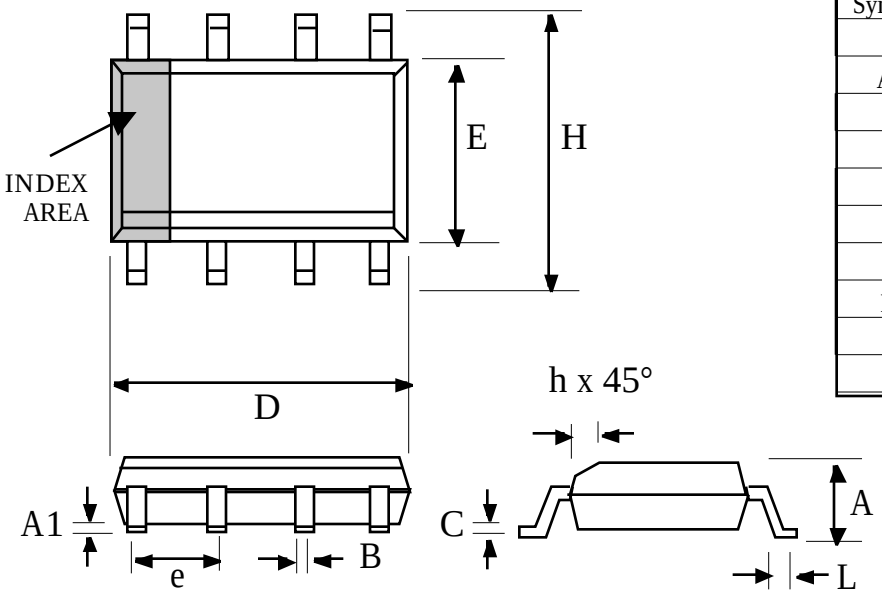


x2 Mode (S1, S0 = 1, 0)
CLK/2 Feedback

Using CLK as the feedback will always result in synchronized rising edges between ICLK and CLK. But the CLK/2 could be a falling edge compared with ICLK. Therefore, wherever possible, we recommend the use of CLK/2 feedback. This will synchronize the rising edges of all 3 clocks.

Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)



8 pin SOIC

	JEDEC Dimensions		Millimeters	
Symbol	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.004	0.0098	0.10	0.25
B	0.0130	0.0200	0.33	0.51
C	0.0075	0.0098	0.19	0.25
D	0.1890	0.1968	4.80	5.00
E	0.1497	0.1574	3.80	4.00
e	.050 BSC		1.27 BSC	
H	0.2284	0.2440	5.80	6.20
h	0.0099	0.0195	0.25	0.50
L	0.0160	0.0500	0.41	1.27

Ordering Information

Part/Order Number	Marking	Package	Temperature
ICS570A	ICS570A	8 pin SOIC	0 to 70 °C
ICS570AT	ICS570A	8 pin SOIC on tape and reel	0 to 70 °C
ICS570AI	ICS570AI	8 pin SOIC	-40 to +85 °C
ICS570AIT	ICS570AI	8 pin SOIC on tape and reel	-40 to +85 °C
ICS570M	ICS570M	8 pin SOIC	0 to 70 °C
ICS570MT	ICS570M	8 pin SOIC on tape and reel	0 to 70 °C
ICS570MI	ICS570I	8 pin SOIC	-40 to +85 °C
ICS570MIT	ICS570I	8 pin SOIC on tape and reel	-40 to +85 °C

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