STn8815P14

Mobile multimedia application processor

Data Brief

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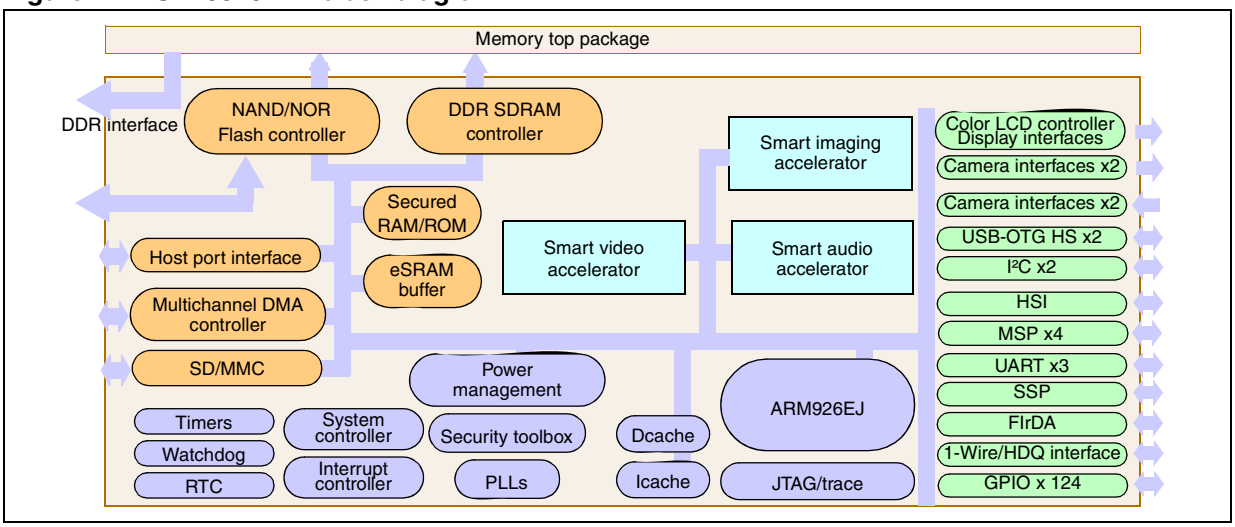
Features

- Smart video accelerator
  - MPEG-4 SP real-time encoding/decoding up to SDTV 30 fps
  - H.264/AVC real-time decoding up to VGA 30 fps and encoding up to VGA 15 fps
  - WM9/VC-1 encode/decode support
  - JPEG encode up to 30 Mpixel/s, decode up to 15 Mpixel/s
- Smart audio accelerator with extensive digital-audio software library
- Smart imaging accelerator
  - 5 Mpixel camera support
  - 2 SMIA CCP2 camera interfaces up to 650 Mbit/s and parallel camera CCIR-656 interface up to 80 MHz
  - Real-time image reconstruction up to 80 Mpixel/s and 10-bit raw Bayer interface
- Smart graphics accelerator
- Ultra low-power implementation
- TV output
- Advanced power management unit
- ARM926EJ® 32-bit RISC CPU, up to 393 MHz
  - 16-Kbyte instruction cache, 16-Kbyte data cache, 128-Kbyte level 2 cache
- On-chip SRAM: 512 Kbytes + 16 Kbytes with secured access + 1 Kbyte backup
- On-chip ROM: 32 Kbytes for boot + 64 Kbytes with secured access
- Enhanced security framework and protected access to secured ROM and RAM
- 16-bit DDR/SDR-SDRAM memory controller (up to 166 MHz)
- NOR Flash/NAND Flash/CompactFlash/CF+ controller
- VFBGA 14.0mm x 14.0mm x 1.0mm memory stackable package (PoP)

Description

The STn8815 application processor enables smart phones, mobile multimedia, internet appliances and in-car entertainment systems to playback media content, record video clips and pictures, receive mobile-TV and perform real-time bidirectional audio-visual communication.

Figure 1. STn8815P14 block diagram



For further information contact your local STMicroelectronics sales office. www.st.com

Contents

1 STn8815P14 overview 4

1.1 Key benefits 7
1.2 Main features 7
1.3 Low power consumption 8
1.4 Open platform strategy 8
1.5 Memory package interfaces 8

2 Architecture overview 9

2.1 Smart video accelerator (SVA) 10
2.2 Smart audio accelerator (SAA) 10
2.3 Smart imaging accelerator (SIA) 11
2.4 Smart graphics accelerator (SGA) 11
2.5 Advanced power management unit (PMU) 12
2.6 ARM926EJ processor 12
2.7 Embedded memory units 12
2.8 Advanced security 12
2.9 Flexible static memory controller (FSMC) 13
2.10 SDRAM memory controller (SDMC) 13
2.11 Real time clock (RTC) 13
2.12 Timers 13
2.13 Watchdog timer 13
2.14 Vectored interrupt controller (VIC) 13
2.15 System and reset controller (SRC) 13
2.16 Direct memory access (DMA) controllers 14
2.17 Universal asynchronous receivers-transmitters (UARTs) 14
2.18 Synchronous serial port (SSP) 14
2.19 Camera interfaces 14
2.20 TV interface 14
2.21 Liquid crystal display controller (LCDC) 15
2.22 Master display interface (MDIF) 15
2.23 Pulse width light modulator (PWL) 15

2.24 General purpose inputs/outputs (GPIOs) 15
2.25 Memory card interface (MMC/SD/MS) 16
2.26 USB-OTG high-speed interface 16
2.27 I^2C bus interface 16
2.28 Fast IrDA interface (FIrDA) 16
2.29 Multichannel serial ports (MSP) 17
2.30 Scroll key and keypad encoder (SKE) interface 17
2.31 High-speed serial interface (HSI) 17
2.32 Host port interface (HPI) 17

3 Package mechanical data 18

4 Ordering information 21

5 Revision history 21

1 STn8815P14 overview

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  - WM9/VC-1 encode/decode support
  - JPEG encode up to 30 Mpixel/s, decode up to 15 Mpixel/s
  - Ultra low-power implementation
- Smart audio accelerator
  - Extensive digital-audio software library
  - Ultra low-power implementation
- Smart imaging accelerator
  - 5 Mpixel camera support
  - 2 SMIA CCP2 camera interfaces up to 650 Mbit/s
  - Parallel camera CCIR-656 interface up to 80 MHz
  - Real-time image reconstruction up to 80 Mpixel/s
  - 10-bit raw Bayer interface
  - Ultra low-power implementation
- Smart graphics accelerator for 2-D and 3-D OSD
- TV output
- Advanced power management unit
  - Run, idle, doze and sleep modes
  - CPU clock with programmable frequency
  - Enhanced dynamic power-domain management
  - Dynamic voltage scaling
- ARM926EJ® 32-bit RISC CPU, up to 393 MHz
  - 16-Kbyte instruction cache, 16-Kbyte data cache
  - 128-Kbyte level 2 cache
  - 3 instruction sets: 32-bit for high performance, 16-bit (Thumb) for efficient code density, byte Java mode (Jazelle™) for direct execution of Java code
  - Embedded medium trace module (ETM Medium+)
- On-chip SRAM: 512 Kbytes + 16 Kbytes with secured access + 1 Kbyte backup
- On-chip ROM: 32 Kbytes for boot
  + 64 Kbytes with secured access
- Advanced security
  - Enhanced security framework
  - Protected access to secured ROM and RAM
- 16-bit DDR/SDR-SDRAM memory controller (up to 166 MHz)
- NOR Flash/NAND Flash/CompactFlash/CF+ controller
- High-speed MMC/SD Card/Memory Stick Pro host controller

- Color LCD controller for STN or TFT panels or display interface for display module
  - 24-bpp true color
  - MIPI™ legacy DBI and DPI
- Two high speed USB 2.0 On-The-Go controller interfaces (12 and 480 Mbit/s)
  - ULPI v1.1 compliance
  - ULPI SDR support, DDR not supported
- Host port interface
- I/O peripherals
  - 3 autobaud UARTs (one with modem control signals) up to 6 Mbit/s
  - One IrDA (SIR/MIR/FIR) interface up to 4 Mbit/s
  - One synchronous serial port (SSP) up to 24 Mbit/s
  - 4 multichannel serial ports (MSP) up to 48 Mbit/s
  - 3 I²C master/slave interfaces, 1 dedicated to SIA
  - Two 8-channel, full-duplex high-speed serial interfaces, 110 Mbit/s (MIPI legacy HSI)
  - Rotary encoder interface; keypad matrix interface
  - 1-Wire®/HDQ interface [a]
- 124 general-purpose I/Os (muxed with peripheral I/Os)
- System and peripheral controller
  - Multichannel DMA controller
  - 64-source interrupt controller
  - Eight 32-bit timers/counters
  - Real-time clock (RTC)
  - Real-time timer (RTT)
  - Watchdog timer
- Programmable PLL for CPU and system clocks
- Two crystal oscillators:
  32 kHz and 13/19.2 MHz
- JTAG IEEE 1149.1 boundary scan
- Supply voltages
  - 1.2 V to 1.4 V logic; 1.8 V to 2.5 V I/O, PLL analog; 2.5 V OTP
- VFBGA memory stackable (package on package)
  14 mm x 14 mm x 1.0 mm, pitch 0.5 mm, 464 balls

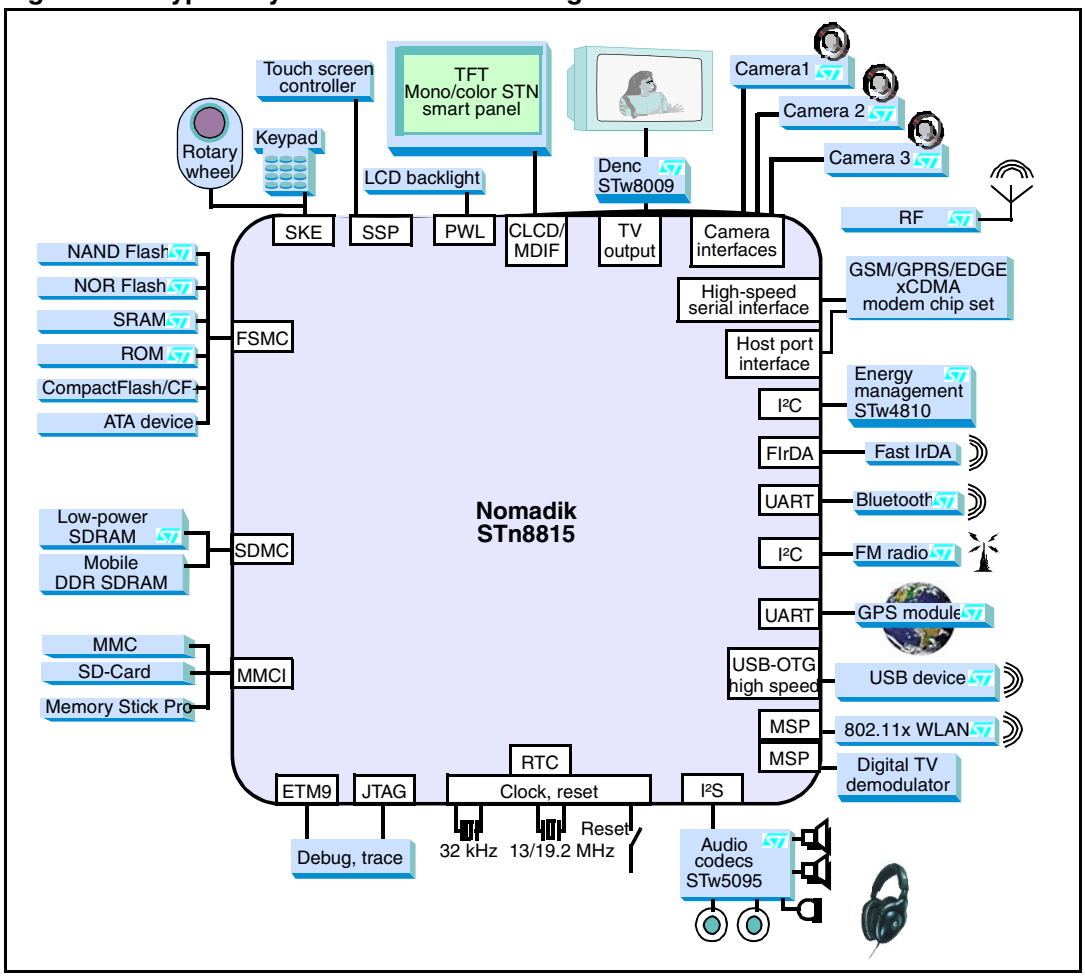
a. 1-Wire is a registered trademark of Dallas Semiconductor.

The convergence of computing, multimedia and mobile communications is well underway. Already the familiar voice phone is being transformed into a personal device with a wide range of multimedia capabilities. Soon mobile users will be able to benefit from a broad spectrum of multimedia features and services, to include capturing, sending and receiving images, videos and music. To deliver such data-heavy, processing-intensive services, portable handheld systems must be optimized for high performance but low power, space and cost.

In response to this need, the STn8815P14 processor platform from STMicroelectronics is a culmination of breakthroughs in video coding efficiency, inventive algorithms and chip implementation schemes. It will enable smart phones, wireless PDAs, internet appliances and car entertainment systems to play back media content, record pictures and video clips, and perform bidirectional audio-visual communication with other systems in real time.

The STn8815P14 focuses on the essential features to meet the future needs of mobile products and services: a high-performance multimedia capability coupled with low power consumption, and based on an open platform strategy.

Figure 2. Typical system architecture using the STn8815P14



1.1 Key benefits

The STn8815P14 brings the following key benefits to mobile manufacturers and consumers:

- Unsurpassed audio, video and imaging quality,
- Ultra-low power consumption for longer battery operation,
- Easier application development for shorter time-to-market,
- Scalability for multiple market segments and future multimedia applications.

1.2 Main features

The STn8815P14 processor platform enables compelling multimedia applications by means of its unique distributed-processing architecture.

The application processor features low-power smart accelerators which handle all audio, video and graphics functions. These free the main CPU for control and program flow tasks, or allow the CPU to enter power-saving modes to prolong battery life. The smart accelerators operate independently and concurrently to ensure the lowest absolute system power and deterministic high-performance.

The main features of the platform are:

- A smart video accelerator for SDTV video encoding and decoding, with MIPI and SMIA camera interfaces.
- A smart audio accelerator containing a comprehensive set of digital audio decoders and encoders, and offering a large number of 3-D surround effects.
- A smart imaging accelerator, providing real-time, programmable image reconstruction engine.
- A smart graphics accelerator.
- A dynamic, multi-mode power management unit.
- The ARM926EJ processor, a powerful industry-standard CPU with Java acceleration.
- On-chip ROM and SRAM memory devices, including a 3-Mbit frame buffer.
- Security framework for enhanced mobile security, including stronger DRM.
- Multichannel DMA controller for efficient data transfer without CPU intervention.
- A multi-layer AMBA crossbar interconnect for optimized data transfers between the CPU, accelerators, memory devices and peripherals.
- Hardware semaphores for flexible inter-process management.
- A wide range of peripheral interfaces (GPIO, USB-OTG high speed, UART, I²C, FIrDA, SD/high-speed MMC/Memory Stick Pro, fast serial ports, TV output, color LCD and camera interfaces, scroll-key encoder, key-pad scanner).
- Direct support for high-level operating system such as Symbian™, Linux and WinCE® operating systems (OSs).

1.3 Low power consumption

The new multimedia functionality of mobile products brings with it an increase in power consumption that is outpacing advances in battery technology. The STn8815P14 chip saves on power by avoiding the need for high clock speeds wherever possible, but its extremely low power consumption results from a systematic effort at all design levels to reduce power requirements. These include:

- The use of smart accelerators and distributed processing to off load from the CPU,
- Efficient code execution by means of innovative algorithms, energy-efficient instruction set architectures and Java acceleration,
- The efficient use of bandwidth for on-chip data transport, achieved by data compression, buffering and image scaling,
- Aggressive power management which includes turning off inactive parts of the chip and keeping the CPU in power-saving modes as much as possible.

1.4 Open platform strategy

STMicroelectronics is a founding member of the MIPI™ Alliance working towards mobile software and hardware interface standards.

Our open platform strategy provides manufacturers with roadmap flexibility, allowing them to avoid becoming locked into a proprietary CPU architecture or vendor technology. This approach is facilitated by the following design points.

- The STn8815P14 employs the third-party ARM® processor which is the standard CPU for mobile devices, with industry-wide application support.
- Open, standard APIs are provided for the development of application code on a level which is abstracted from the physical hardware. This allows the development of multimedia plug-ins that are portable between products and which can be reused on future products without modification.
- The STn8815P14 facilitates best-in-class algorithm development on its smart accelerators.
- The STn8815P14 is provided with development kits and tools that speed-up the integration of new operating systems, middleware, and signal processing algorithms.

1.5 Memory package interfaces

The STN8815P14 package supports package on package technology, allowing a memory package to be stacked on top of the bottom package. The bottom package includes the STn8815P14 specific balls.

Top lands of the STN8815P14 provide the following interfaces:

- mobile DDR SDRAM (16 bits data bus)
- OneNAND

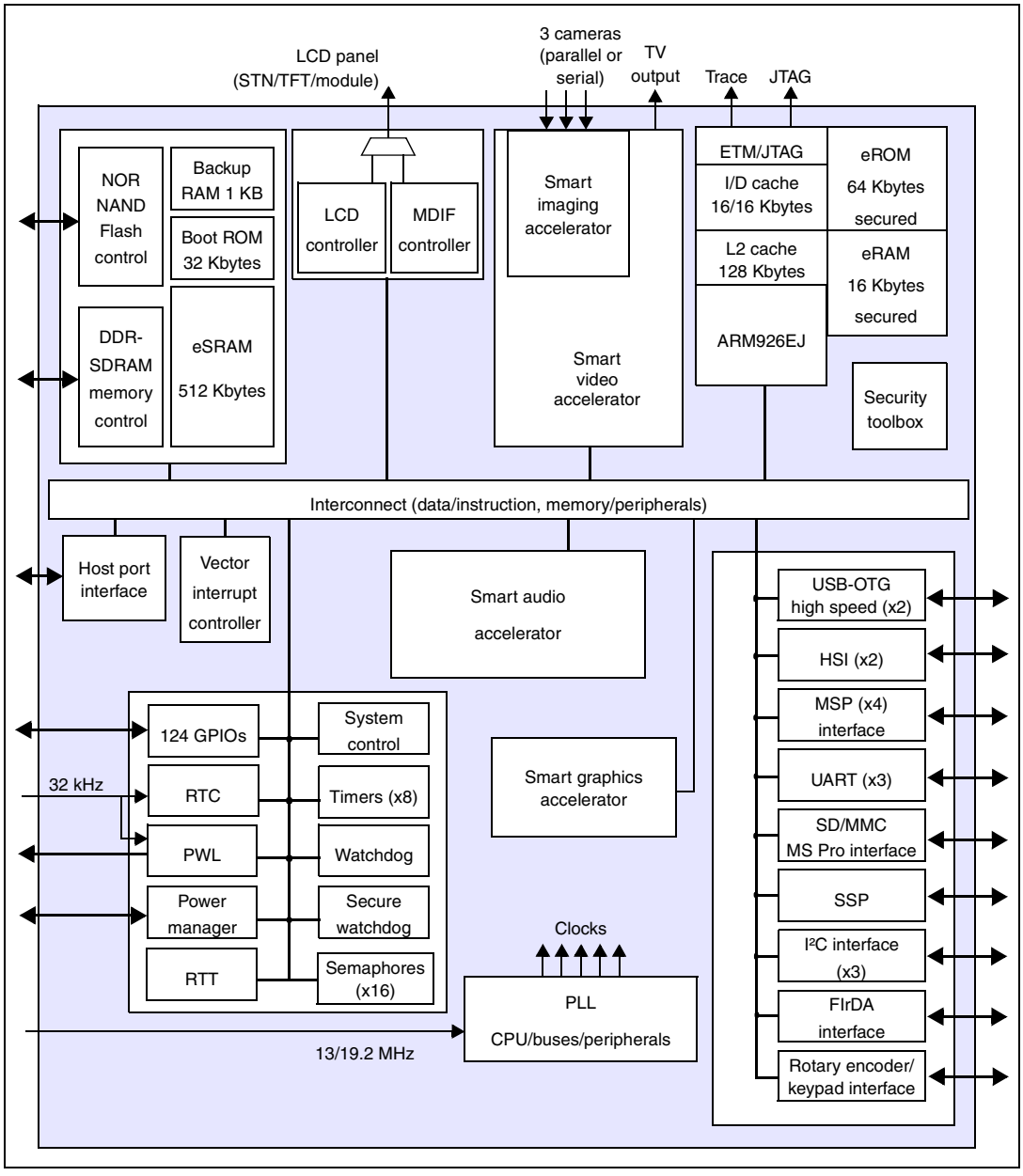
Some additional top lands can provide a complete mobile SDR/DDR interface connected directly to the bottom balls of the package, allowing an external processor to use memory from the top package.

2 Architecture overview

The STn8815P14 platform comprises an industry-standard ARM CPU supported by smart audio, video, imaging and graphics accelerators, on-chip memory and controllers, a rich set of peripheral interfaces, and a power management system. The processors, controllers, memory and peripheral interfaces are connected by a multi-layer advanced microcontroller bus architecture (AMBA) for efficient data transport between the components. The overall STn8815P14 architecture is illustrated in *Figure 3*.

The main hardware components of the STn8815P14 are listed and outlined in the sections below.

Figure 3. STn8815P14 block diagram



2.1 Smart video accelerator (SVA)

Using leading-edge technology, this block is a low-power, high-performance video accelerator that supports the following features:

- MPEG-4 simple profile level 5 video encoder and decoder; real-time up to SDTV 30 fps (encode only or decode only).
- MPEG-4 simple profile level 3 video simultaneous codec up to CIF 30 fps.
- H.264/AVC baseline profile level 3 decoding up to VGA 30 fps.
- H.264/AVC baseline profile level 2.2 encoding up to VGA 15 fps.
- H.264/AVC baseline profile level 2 simultaneous codec up to CIF 30 fps.
- WM9/VC-1 encode/decode support.
- JPEG baseline encoder acceleration up to 30 Mpixel/s.
- JPEG baseline and extended DCT-based decoder acceleration up to 15 Mpixel/s.
- Programmable DSP (MMDSP+) for intermediate level processing, clocked at up to 166 MHz.
- Picture pre-/post-processing.
- Ultra-low power implementation.

This list of codecs is non-exhaustive, and is a baseline for the SVA performances.

2.2 Smart audio accelerator (SAA)

This high-performance block is a flexible sophisticated audio accelerator based on the MMDSP+ programmable audio DSP, clocked up to 166 MHz, and features:

- 24-bit data path,
- ultra-low power implementation.

The audio accelerator handles:

- Speech and audio codecs: AMR (WB, NR), MP3, AAC, WMA and more,
- Sample-rate conversion to 8, 16, 32, 44.1 and 48 kHz,
- Extension of sound field and 3-D surround effects,
- Noise reduction and echo cancelling.

2.3 Smart imaging accelerator (SIA)

The smart imaging accelerator is provided by the image preprocessing module of the SVA. This flexible imaging engine provides real-time, programmable image processing, and features:

- Shot-to-shot performance (with CMOS sensor):
  - 3 Mpixel, up to 15 image/s,
  - 5 Mpixel, up to 9 image/s.
- Direct support for smart sensors (CMOS/CCD modules), unlimited resolution (YUV input with JPEG compression).
- Image reconstruction up to 80 Mpixel/s with raw Bayer input.
- With shutter, maximum sensor resolution depends on external SDRAM size and on target shot-to-shot delay.
- Auto-focus control, auto exposure control.
- Automatic white balance, contrast enhancement, brightness control.
- On-the-fly zoom, flash-gun control.
- Noise reduction, gamma correction, image sharpening.
- Ultra-low power implementation.

2.4 Smart graphics accelerator (SGA)

The smart graphics accelerator provides an efficient 2D and 3D drawing tool that enables next generation of games and user interfaces while minimizing power consumption.

2D features

- ROP4.
- Line drawing.
- Triangle and rectangle fill.
- Alpha blending bit blit.
- Stretch/scale/rotate/mirror bit blit.
- Gradient color fill (horizontal and vertical).
- Full picture anti-aliasing filter.
- Image resizing.
- Font-expansion and anti-aliasing text drawing.

3D features

- Texture mapping.
- Texture transparency/blending/clamping/wrapping/mirroring.
- Flat and Gouraud shading.
- 16-bit Z buffering.
- Fog and depth cueing.
- Embossed bump mapping texture generation.

2.5 Advanced power management unit (PMU)

The dynamic PMU optimizes power consumption of the STn8815P14. It delivers all the platform clocks, and handles reset management. It also manages GPIO levels during sleep mode and emergency self-refresh of SDRAM.

The PMU controls the external voltage regulator, in order to change its settings in different modes. In deep-sleep mode, only GPIOs, real-time clock (RTC), system and reset controller (SRC), PMU and secured RAM remain in operation.

Voltage scaling supports two modes: standard 1.2 V and overdrive 1.4 V.

The family of power manager ICs, STw481x companion chips, seamlessly interface with the Nomadik STn8815P14 and optimize global system power consumption leveraging on the PMU.

2.6 ARM926EJ processor

The STn8815P14 CPU is an ARM926EJ reduced instruction set computer (RISC) processor. This 32-bit processor core supports 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density.

The cached ARM CPU features a memory management unit (MMU) and is clocked at a frequency up to 350 MHz. It has a 16-Kbyte instruction cache, a 16-Kbyte data cache, and a 128-Kbyte level 2 cache, and supports the Jazelle™ extensions for Java acceleration.

It also includes an embedded trace module (ETM Medium+) for real-time CPU activity tracing and debugging. It supports 4-bit and 8-bit normal trace mode and 4-bit demultiplexed trace mode, with normal or half-rate clock.

2.7 Embedded memory units

- 32 Kbytes of public ROM (for boot purposes),
- 64 Kbytes of secured ROM (for security purposes),
- 512 Kbytes of public RAM,
- 16 Kbytes of secured RAM (for security code and/or data),
- 1 Kbyte backup.

2.8 Advanced security

The device contains 64 Kbytes of ROM and 16 Kbytes of RAM that are only accessible when the system is in a trusted environment. An advanced security framework enables M-commerce as well as authentication applications drawing on ST smart card expertise:

- SHA-1/MD5/AES/DES/3DES hardware accelerators,
- True random number generator (RNG),
- Secured watchdog timer,
- Unique die identification.

2.9 Flexible static memory controller (FSMC)

The FSMC interfaces to off-chip multiplexed burst NOR Flash memory devices and NAND Flash memory devices, and to CompactFlash/CF+ cards. The FSMC manages up to 4 chip-selects of NOR Flash memories, and up to 2 chip-selects of NAND Flash memories or CompactFlash/CF+ devices. The memory controller features error code correction accelerated by hardware that reduces host CPU workload to support NAND Flash very fast read/write transfers.

2.10 SDRAM memory controller (SDMC)

The SDMC is used to interface with simple-data rate synchronous dynamic random access memory (SDR-SDRAM) and double-data rate (DDR) SDRAM (133 MHz in standard mode and 166 MHz in overdrive mode). The SDMC manages up to two chip-selects of 16-bit wide SDR-SDRAM or DDR-SDRAM. It can address up to 1 Gbits of SDRAM.

2.11 Real time clock (RTC)

The RTC provides a 1-second resolution clock. This keeps time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

2.12 Timers

The STn8815P14 provides eight 16- or 32-bit (configurable) timers, as two groups of four. They generate the periodic and timed interrupts required by OS services.

2.13 Watchdog timer

This OS resource is used to trigger a system reset in the event of software failure.

2.14 Vectored interrupt controller (VIC)

The VIC allows the OS interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. There are 64 interrupt lines and the VIC uses a separate bit position for each interrupt source. Software controls each request line to generate software interrupts.

2.15 System and reset controller (SRC)

The SRC provides a control interface for clock generation components external to the subsystem. It also controls system-wide and peripheral-specific energy management features.

2.16 Direct memory access (DMA) controllers

Direct memory accesses can be employed for data transfers involving DMA peripherals. A DMA controller services FIFO fill/empty requests from these peripherals immediately without CPU interaction. Peripheral-to-peripheral and memory-to-memory DMAs are also supported. A multichannel DMA controller is provided for efficient and concurrent data transfers.

2.17 Universal asynchronous receivers-transmitters (UARTs)

The STn8815P14 provides three autobaud UARTs, one of which offers all modem control/status signals. They are enhanced versions of the industry-standard 16C550 UART with a high data rate up to 6 Mbit/s and an embedded hardware Xon/Xoff handshake.

2.18 Synchronous serial port (SSP)

The STn8815P14 provides one SSP for synchronous serial communication with external peripherals. SPI, MicroWire and TI protocols are supported, with programmable word length of up to 32 bits and data rate up to 24 Mbit/s.

The SSP has the following features in both master and slave configurations:

- Parallel-to-serial conversion of data written to an internal, 32-bit wide, 32-location deep, transmit FIFO.
- Serial-to-parallel conversion of received data, which is buffered in a 32-bit wide, 32-location deep, receive FIFO.
- Programmable data frame size from 4 to 32 bits.
- Programmable clock bit rate and prescaler.
- Programmable clock phase and polarity in SPI mode.
- Support for direct memory accesses.
- Support for serial LCD smart panels.

2.19 Camera interfaces

- 3 camera interfaces that can be selected alternately:
  - 2 serial SMIA CCP2 camera interfaces (mutually exclusive): up to 650 Mbit/s data strobe,
  - Parallel camera CCIR-656 interface up to 80-MHz with embedded/external sync.
- Direct support of 8-bit and 10-bit raw Bayer RGB data formats.
- High resolution up to 5 Mpixels for camera sensors (raw Bayer data).
- Unlimited resolution for camera modules with JPEG compression.

2.20 TV interface

The STn8815P14 interfaces seamlessly with the STw8009 companion-chip, which performs signal conversion and connects directly to a TV set.

The TV interface is compatible with video and S-video.

2.21 Liquid crystal display controller (LCDC)

This interface drives LCD panels, and supports the following displays:

- STN displays: single- or dual-panel with 8-bit color and 4- or 8-bit monochrome,
- TFT displays: 12-, 16-, 18- and 24-bit color.

The resolution can be set as follows:

- 1-, 2- or 4-bits-per-pixel (bpp) palettized for mono STN,
- 1-, 2-, 4- or 8-bpp palettized for color STN and TFT,
- 16-bpp true-color non-palettized for color STN and TFT,
- 24-bpp packed and non-packed true-color (non-palettized) for color TFT.

The interface supports frame modulation and directly supports Sharp HR-TFT panels.

2.22 Master display interface (MDIF)

This interface drives LCD display modules, that is, panels that include their own display memory and perform LCD panel refresh themselves. The MDIF is a parallel bidirectional interface that can send commands or data to or read data from the display panel logic. It has a DMA engine to automatically fetch data/commands from main memory without CPU intervention.

In addition, the MDIF includes a submode to drive serial LCD smart panels.

2.23 Pulse width light modulator (PWL)

The PWL provides control of LCD backlighting. It produces a series of pulses that are fed to the backlighting, where the width (or duty cycle) of the pulses determines the perceived lighting level. An 8-bit random sequence generator decreases the spectral power at the modulator harmonic frequencies.

2.24 General purpose inputs/outputs (GPIOs)

The STn8815P14 provides 124 programmable inputs or outputs that have switchable pull-up and pull-down resistors and are controllable in two modes:

- Software mode through an APB bus interface,
- Hardware mode through a hardware control interface.

The GPIO interface provides the following individually programmable functions.

- Any number of pins may be configured as interrupt sources.
- Debouncing logic can be enabled for each GPIO to filter out glitches on I/Os.
- Any GPIO may be used to wake up the device from sleep mode independent of interrupt programming, and the input level that triggers wake-up is definable for each enabled GPIO.

2.25 Memory card interface (MMC/SD/MS)

This interface can directly control one of the following memory cards:

- SD card (without encryption/decryption logic),
- MultiMediaCard (high-speed rate 96 Mbit/s),
- Memory Stick and Memory Stick Pro.

It also supports several of each card type using the GPIOs for card selection.

2.26 USB-OTG high-speed interface

The STn8815P14 provides two USB-OTG high-speed interfaces. The USB-OTG features:

- High-speed signalling rate at 480 Mbit/s.
- Support for full-speed (12 Mbit/s) signaling bit rate.
- Support for session request protocol (SRP) and host negotiation protocol (HNP).
- Up to 16 bidirectional endpoints plus control endpoint 0.
- A digital interface to external PHY, such as the AOC018 companion chip.
- ULPI v1.1 compliant interface and ULPI DDR support.
- Backward compatibility with the STw481x family of power-manager ICs at full speed.

2.27 I^2C bus interface

The STn8815P14 provides three I²C bus interfaces, one of which is dedicated to the smart imaging accelerator. The I²C interfaces support the following features:

- Slave transmitter/receiver and master transmitter/receiver modes.
- Multi-master capability.
- 10-bit addressing.
- Standard (100 kHz) and fast (400 kHz) speeds.
- Compliance with I²C standards.

In addition to receiving and transmitting data, the interface converts data from serial to parallel format and vice-versa using an interrupt or polled handshake.

2.28 Fast IrDA interface (FIrDA)

This interface supports IrDA half-duplex communications. It performs modulation and demodulation of infrared signals, and the wrapping of IrLAP frames. The IrDA interface supports the following infrared modes and baud rates:

- Serial infrared (SIR): 9.6 Kbit/s, 19.2 Kbit/s, 38.4 Kbit/s, 57.6 Kbit/s and 115.2 Kbit/s,
- Medium infrared (MIR): 576 Kbit/s and 1.152 Mbit/s,
- Fast infrared (FIR): 4 Mbit/s.

2.29 Multichannel serial ports (MSP)

The STn8815P14 includes 4 MSP synchronous receive and transmit serial interfaces. The MSPs support a data rate of up to 48 Mbit/s with the following features:

- Philips I²S format: left aligned with one cycle between leading edge of frame synchronization and first data bit, 16 or 24 bits per sample.
- Sony format: right aligned, 48 cycles per frame, 16 or 24 bits per sample.
- Matsushita format: right aligned, 64 cycles per frame, 16 or 24 bits per sample.
- Programmable number of bit-clock cycles per frame: 32, 48 or 64.
- Programmable polarity of bit-clock and frame synchronization.
- Programmable number of bits per sample: 16, 18, 20 or 24 bits.

They also provide:

- µ-Law and A-Law compressing/expanding,
- Independent framing and clocking for receive and transmit.
- External shift clock or an internal, programmable frequency shift clock for data transfer.
- Support for DMA transfers.

2.30 Scroll key and keypad encoder (SKE) interface

- This interface supports up to 2 scroll-key inputs such as jog-dials or thumb wheels.
- The keypad interface supports auto-scanning with debouncing of a keypad matrix up to 8 x 8.

2.31 High-speed serial interface (HSI)

The STn8815P14 includes two full-duplex high-speed serial interfaces (MIPI legacy specification). These high-speed, 8-channel interfaces operate at up to 110 Mbit/s.

2.32 Host port interface (HPI)

The host port interface features:

- 16-bit parallel data bus.
- Multiplexed or non-multiplexed address/data bus.
- Indirect host access.
- Direct host access to a segment of STn8815P14 memory in multiplexed mode.

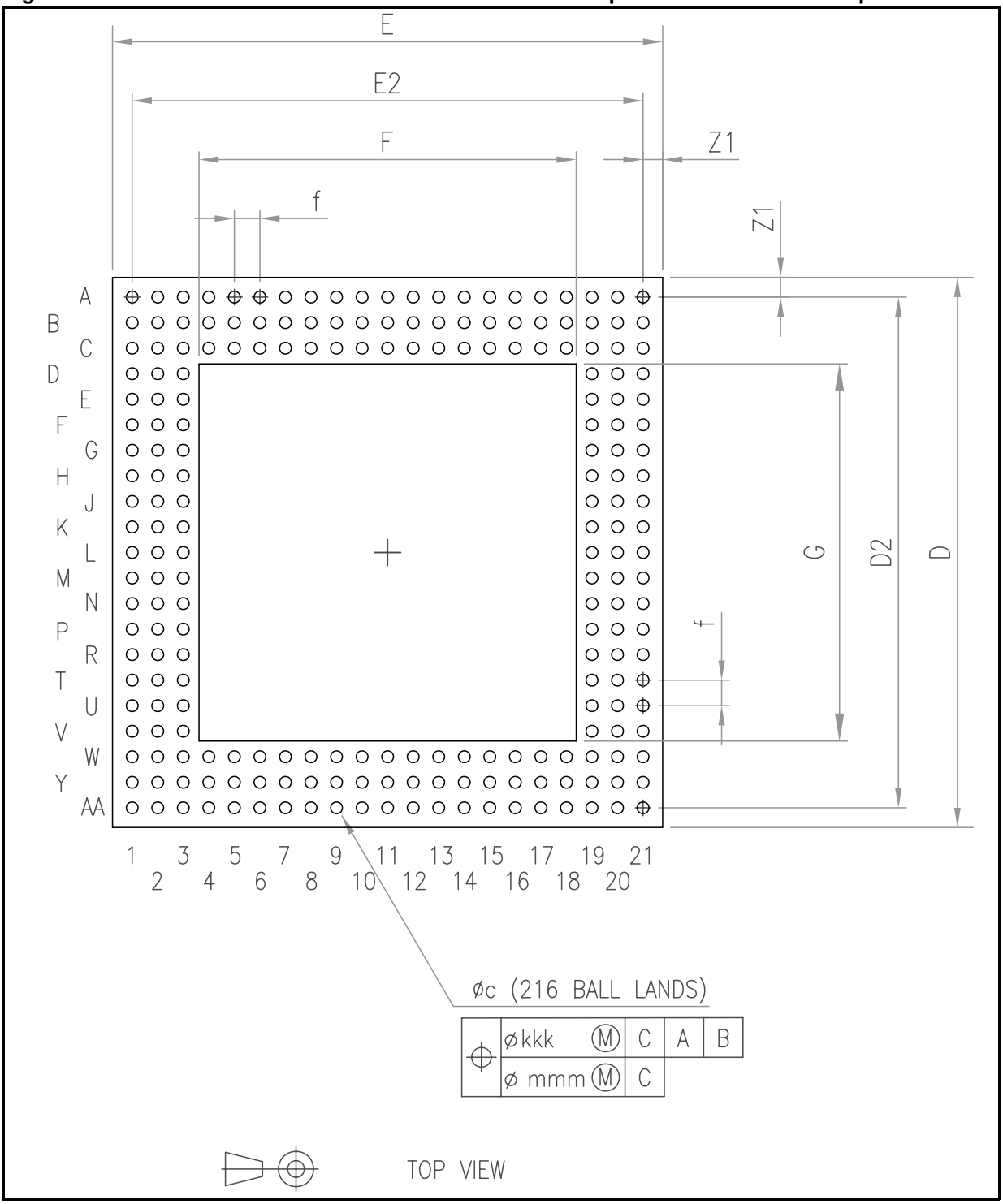
3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 1. Package dimensions

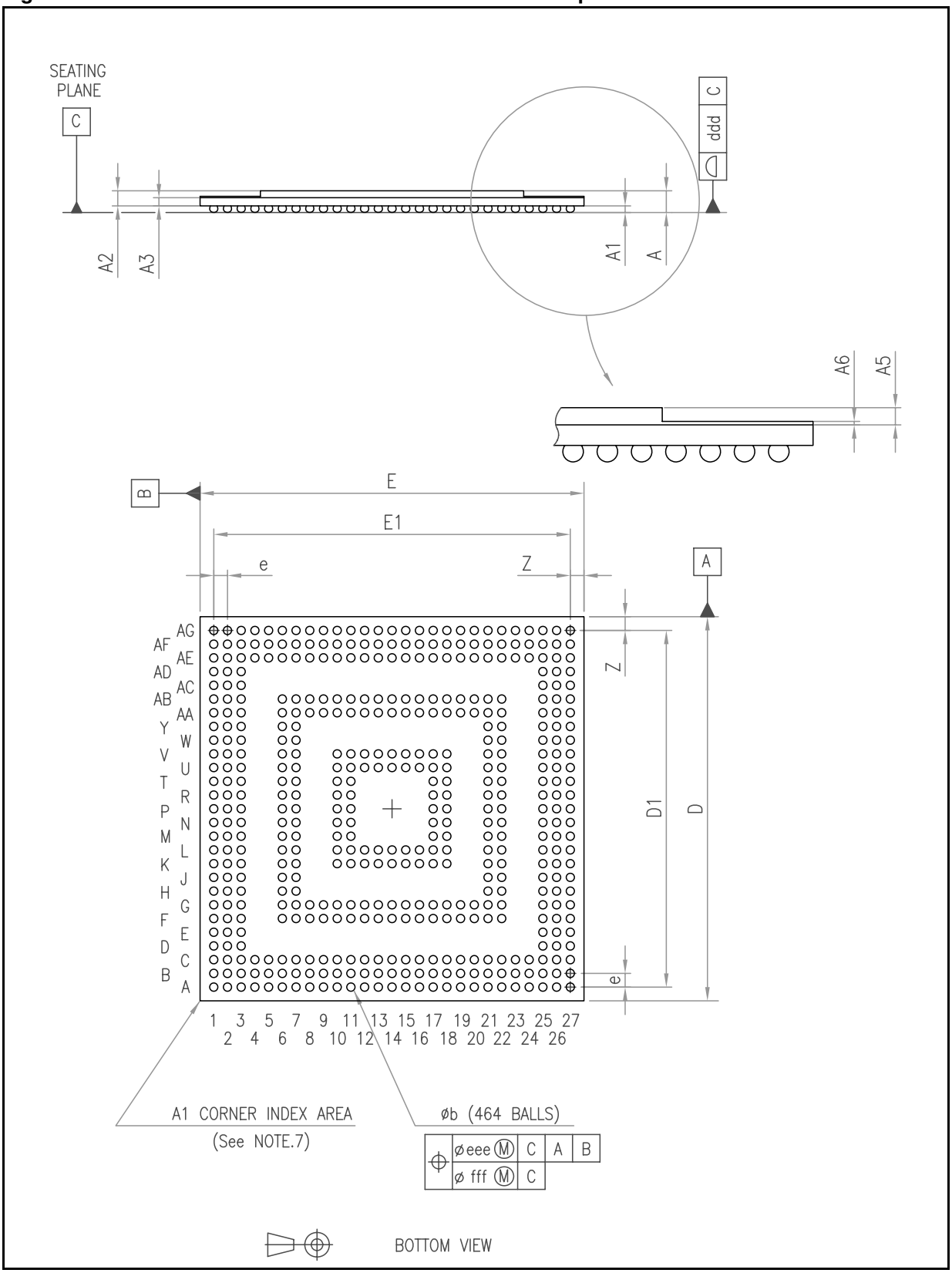
Ref.	Min	Typ	Max	Unit
A			1.00	mm
A1	0.15			mm
A2		0.60		mm
A3		0.30		mm
A5		0.30		mm
A6		0.05		mm
b	0.25	0.30	0.35	mm
c		0.32		mm
D	13.90	14.00	14.10	mm
D1		13.00		mm
D2		13.00		mm
F			9.75	mm
E	13.90	14.00	14.10	mm
E1		13.00		mm
E2		13.00		mm
G			9.75	mm
e		0.50		mm
f		0.65		mm
Z		0.50		mm
Z1		0.50		mm
ddd			0.10	mm
eee			0.15	mm
fff			0.05	mm
kkk			0.15	mm
mmm			0.08	mm

Figure 4. VFBGA 14 mm x 14 mm x 1.0 mm 464 3R27x27 pitch 0.5mm ball 0.3 - Top view



Note: The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Figure 5. VFBGA 14 mm x 14 mm x 1.0 mm 464 3R27x27 pitch 0.5mm ball 0.3 - Bottom view



4 Ordering information

Table 2. Ordering information

Order code	Package	Packing
STN8815D0P14H11E[1]	VFBGA 14 mm x 14 mm x 1.0 mm PoP, 0.5 mm pitch	Tray

1. ECOPACK® package

5 Revision history

Table 3. Document revision history

Date	Revision	Changes
28-Jan-2008	1	Initial release.

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