Complete Dual, 16-Bit High Accuracy, Serial Input, ±5 V DAC

Data Sheet **AD5763**

FEATURES

Complete dual, 16-bit DAC
Programmable output range
±4.096 V, ±4.201 V, or ±4.311 V
±1 LSB maximum INL error, ±1 LSB maximum DNL error
Low noise: 70 nV/√Hz
Settling time: 10 µs maximum
Integrated reference buffers
On-chip die temperature sensor
Output control during power-up/brownout
Programmable short-circuit protection
Simultaneous updating via $\overline{\text{LDAC}}$
Asynchronous clear to zero code
Digital offset and gain adjust
Logic output control pins
DSP-/microcontroller-compatible serial interface
Temperature range: −40°C to +105°C
***i*CMOS® process technology[1]**

APPLICATIONS

Industrial automation
Open-loop/closed-loop servo control
Process control
Data acquisition systems
Automatic test equipment
Automotive test and measurement
High accuracy instrumentation

GENERAL DESCRIPTION

The AD5763 is a dual, 16-bit, serial input, bipolar voltage output digital-to-analog converter (DAC) that operates from supply voltages of ±4.75 V up to ±5.25 V. The nominal full-scale output range is ±4.096 V. The AD5763 provides integrated output amplifiers, reference buffers, and proprietary power-up/power-down control circuitry. The part also features a digital I/O port, which is programmed via the serial interface. The part incorporates digital offset and gain adjust registers per channel.

The AD5763 is a high performance converter that offers guaranteed monotonicity, integral nonlinearity (INL) of ±1 LSB, low noise, and 10 µs settling time. During power-up (when the supply voltages are changing), the outputs are clamped to 0 V via a low impedance path.

The AD5763 uses a serial interface that operates at clock rates of up to 30 MHz and is compatible with DSP and microcontroller interface standards. Double buffering allows the simultaneous updating of all DACs. The input coding is programmable to either twos complement or offset binary formats. The asynchronous clear function clears all DAC registers to either bipolar zero or zero scale depending on the coding used. The AD5763 is ideal for both closed-loop servo control and open-loop control applications. The AD5763 is available in a 32-lead TQFP, and offers guaranteed specifications over the −40°C to +105°C industrial temperature range. Figure 1 contains a functional block diagram of the AD5763.

Table 1. Related Devices

Part No.	Description
AD5764	Complete quad, 16-bit, high accuracy, serial input, ±10 V output DAC
AD5765	Complete quad, 16-bit, high accuracy, serial input, ±5 V DAC

[1] *i*CMOS, Reg. U.S. Patent and Trademark Office.

Rev. C
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REVISION HISTORY

9/11—Rev. B to Rev. C

Changed 50 MHz to 30 MHz Throughout ... 1
Changes to t_1, t_2, and t_3 Parameters, Table 4 ... 6
Changes to Table 20 ... 25

7/11—Rev. A to Rev. B

Changed 30 MHz to 50 MHz Throughout ... 1
Changes to t_1, t_2, and t_3 Parameters, Table 4 ... 6
Changes to Table 20 ... 25

10/09—Rev. 0 to Rev. A

Deleted Endnote 1, Table 2 ... 4
Deleted Endnote 1, Table 3 ... 5
Deleted Endnote 1, Table 4 ... 6
Changes to t_6 Parameter, Table 4 ... 6

1/09—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

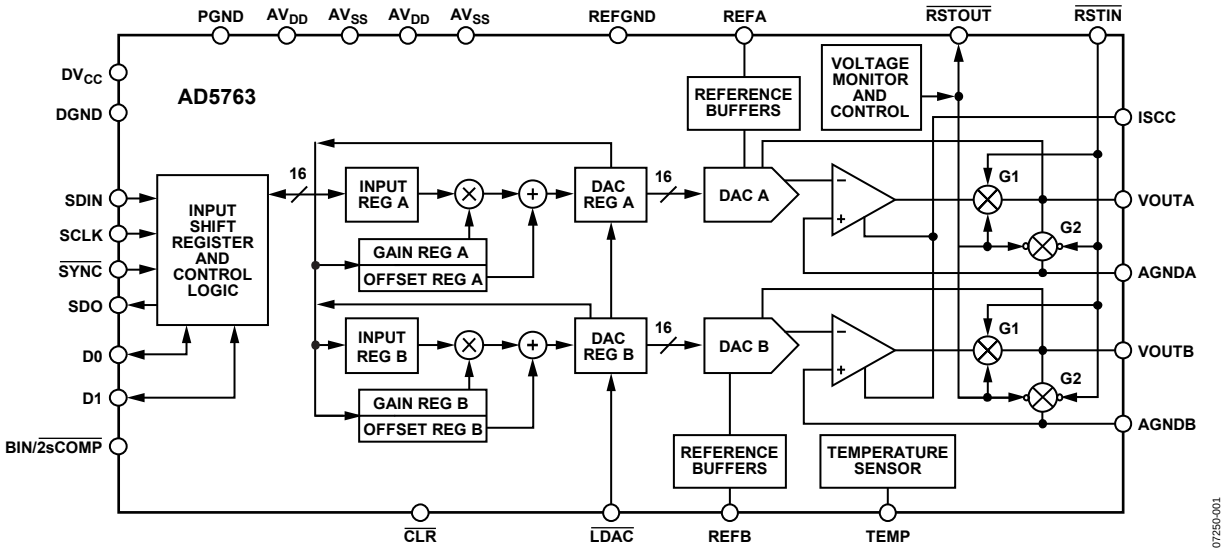


Figure 1.

SPECIFICATIONS

AV_{DD} = 4.75 V to 5.25 V, AV_{SS} = −5.25 V to −4.75 V, AGNDx = DGND = REFGND = PGND = 0 V, REFA = REFB = 2.048 V, DV_{CC} = 2.7 V to 5.25 V, R_{LOAD} = 5 kΩ, C_{LOAD} = 200 pF. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					Outputs unloaded
Resolution	16			Bits	
Relative Accuracy (INL)	−1		+1	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Bipolar Zero Error	−2		+2	mV	At 25°C
	−3		+3	mV	
Bipolar Zero Temperature Coefficient (TC)[1]		±1		ppm FSR/°C	
Zero-Scale Error	−2		+2	mV	At 25°C
	−3.5		+3.5	mV	
Zero-Scale Temperature Coefficient (TC)[1]		±1		ppm FSR/°C	
Gain Error	−0.03		+0.03	% FSR	At 25°C, coarse gain register = 0
	−0.04		+0.04	% FSR	Coarse gain register = 0
Gain Temperature Coefficient (TC)[1]		±1		ppm FSR/°C	
DC Crosstalk[1]			0.5	LSB	
REFERENCE INPUT[1]					
Reference Input Voltage		2.048		V nominal	±1% for specified performance
DC Input Impedance	1			MΩ	Typically 100 MΩ
Input Current		0.03	10	μA	
Reference Range	1		2.1	V	
OUTPUT CHARACTERISTICS[1]					
Output Voltage Range[2]	−4.31158		+4.31158	V	Coarse gain register = 2
	−4.20103		+4.20103	V	Coarse gain register = 1
	−4.096		+4.096	V	Coarse gain register = 0
	−4.42105		+4.42105	V	REFA = REFB = 2.1 V, coarse gain register = 2
Output Voltage Drift vs. Time		±32		ppm FSR/500 hrs	
		±37		ppm FSR/1000 hrs	
Short-Circuit Current		10		mA	RI_{SCC} = 6 kΩ, see Figure 23
Load Current	−1		+1	mA	For specified performance
Capacitive Load Stability					
R_{LOAD} = ∞			200	pF	
R_{LOAD} = 10 kΩ			1000	pF	
DC Output Impedance			0.3	Ω	
DIGITAL INPUTS[1]					JEDEC compliant
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current	−1		+1	μA	Per pin
Pin Capacitance			10	pF	Per pin
DIGITAL OUTPUTS (D0, D1, SDO)[1]					
Output Low Voltage			0.4	V	DV_{CC} = 5 V ± 5%, sinking 200 μA
Output High Voltage	DV_{CC} − 1			V	DV_{CC} = 5 V ± 5%, sourcing 200 μA
Output Low Voltage			0.4	V	DV_{CC} = 2.7 V to 3.6 V, sinking 200 μA
Output High Voltage	DV_{CC} − 0.5			V	DV_{CC} = 2.7 V to 3.6 V, sourcing 200 μA
High Impedance Leakage Current		±1		μA	SDO only
High Impedance Output Capacitance		5		pF	SDO only

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIE TEMPERATURE SENSOR					
Output Voltage at 25°C		1.44		V	
Output Voltage Scale Factor		3		mV/°C	
Output Voltage Range	1.175		1.9	V	
Output Load Current			200	µA	
Power-On Time		10		ms	
POWER REQUIREMENTS					
AV_{DD}/AV_{SS}	4.75		5.25	V	
DV_{CC}	2.7		5.25	V	
AI_{DD}		2.5	3.5	mA/channel	Outputs unloaded
AI_{SS}		2	3.25	mA/channel	Outputs unloaded
DI_{CC}		0.75	1.2	mA	$V_{IH} = DV_{CC}$, V_{IL} = DGND
Power Supply Sensitivity[1]					
$\Delta V_{OUT}/\Delta AV_{DD}$		−110		dB	
Power Dissipation		45		mW	±5 V operation output unloaded

[1] Guaranteed by design and characterization; not production tested.
[2] Output amplifier headroom requirement is 0.5 V minimum.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = 4.75 V to 5.25 V, AV_{SS} = −5.25 V to −4.75 V, AGNDx = DGND = REFGND = PGND = 0 V, REFA = REFB = 2.048 V, DV_{CC} = 2.7 V to 5.25 V, R_{LOAD} = 5 kΩ, C_{LOAD} = 200 pF. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[1]					
Output Voltage Settling Time		8		µs	Full-scale step to ±1 LSB
			10	µs	
		2		µs	512 LSB step settling
Slew Rate		5		V/µs	
Digital-to-Analog Glitch Energy		20		nV-sec	
Glitch Impulse Peak Amplitude		30		mV	
Channel-to-Channel Isolation		60		dB	
DAC-to-DAC Crosstalk		8		nV-sec	
Digital Crosstalk		2		nV-sec	
Digital Feedthrough		2		nV-sec	Effect of input bus activity on DAC outputs
Output Noise (0.1 Hz to 10 Hz)		0.1		LSB p-p	
Output Noise (0.1 Hz to 100 kHz)		50		µV rms	
1/f Corner Frequency		300		Hz	
Output Noise Spectral Density		70		nV/√Hz	Measured at 10 kHz
Complete System Output Noise Spectral Density[2]		80		nV/√Hz	Measured at 10 kHz

[1] Guaranteed by design and characterization; not production tested.
[2] Includes noise contributions from integrated reference buffers, 16-bit DAC, and output amplifier.

TIMING CHARACTERISTICS

AV_{DD} = 4.75 V to 5.25 V, AV_{SS} = −5.25 V to −4.75 V, AGNDx = DGND = REFGND = PGND = 0 V, REFA = REFB = 2.048 V, DV_{CC} = 2.7 V to 5.25 V, R_{LOAD} = 5 kΩ, C_{LOAD} = 200 pF. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5[4]	13	ns min	24th SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	90	ns min	Minimum $\overline{SYNC}$ high time
t_7	2	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	1.7	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (all DACs updated)
	480	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (single DAC updated)
t_{10}	10	ns min	$\overline{LDAC}$ pulse width low
t_{11}	500	ns max	$\overline{LDAC}$ falling edge to DAC output response time
t_{12}	10	µs max	DAC output settling time
t_{13}	10	ns min	$\overline{CLR}$ pulse width low
t_{14}	2	µs max	$\overline{CLR}$ pulse activation time
t_{15}[5, 6]	25	ns max	SCLK rising edge to SDO valid
t_{16}	13	ns min	$\overline{SYNC}$ rising edge to SCLK falling edge
t_{17}	2	µs max	$\overline{SYNC}$ rising edge to DAC output response time ($\overline{LDAC}$= 0)
t_{18}	170	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 2, Figure 3, and Figure 4.
[4] Standalone mode only.
[5] Measured with the load circuit of Figure 5.
[6] Daisy-chain mode only.

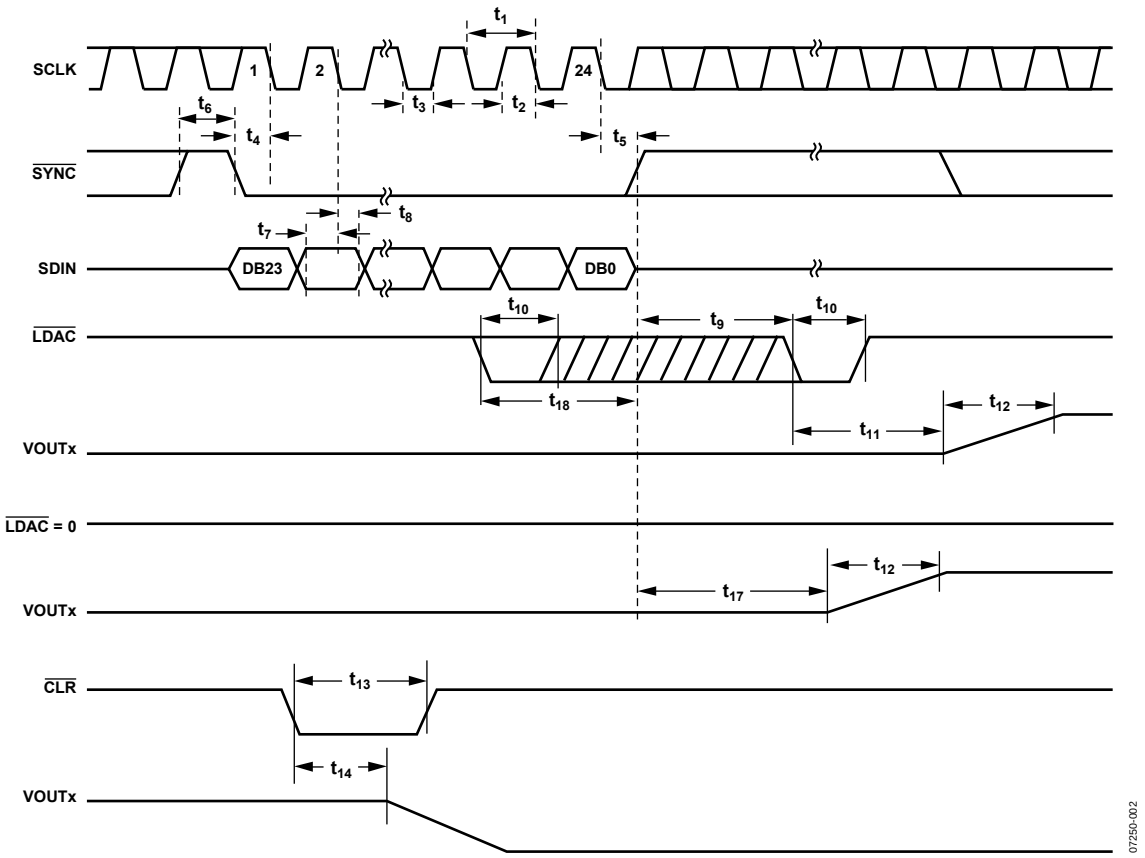


Figure 2. Serial Interface Timing Diagram

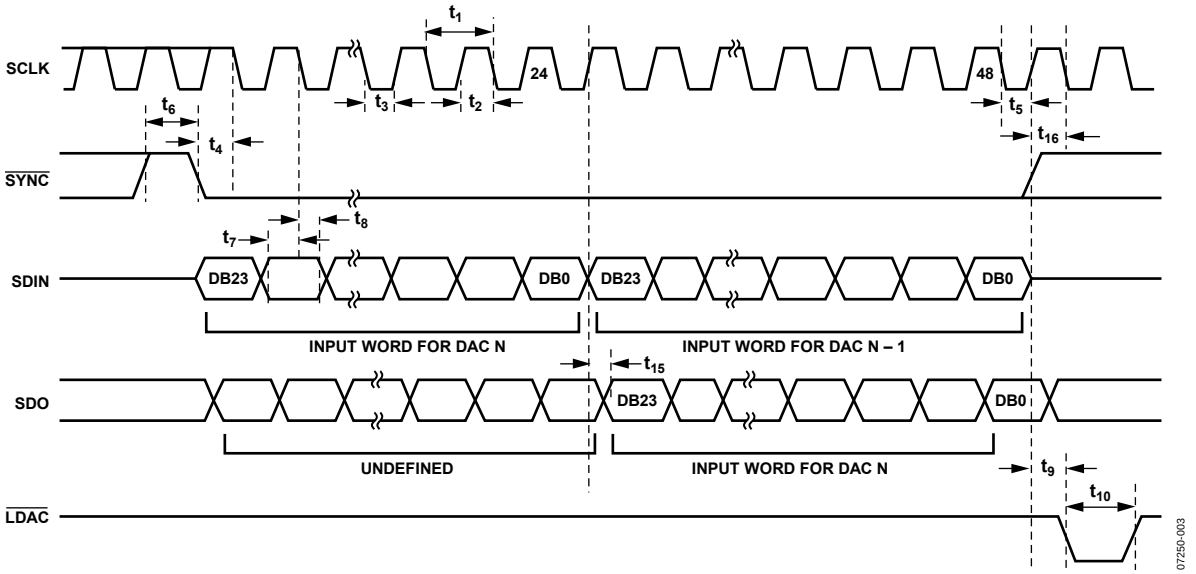


Figure 3. Daisy-Chain Timing Diagram

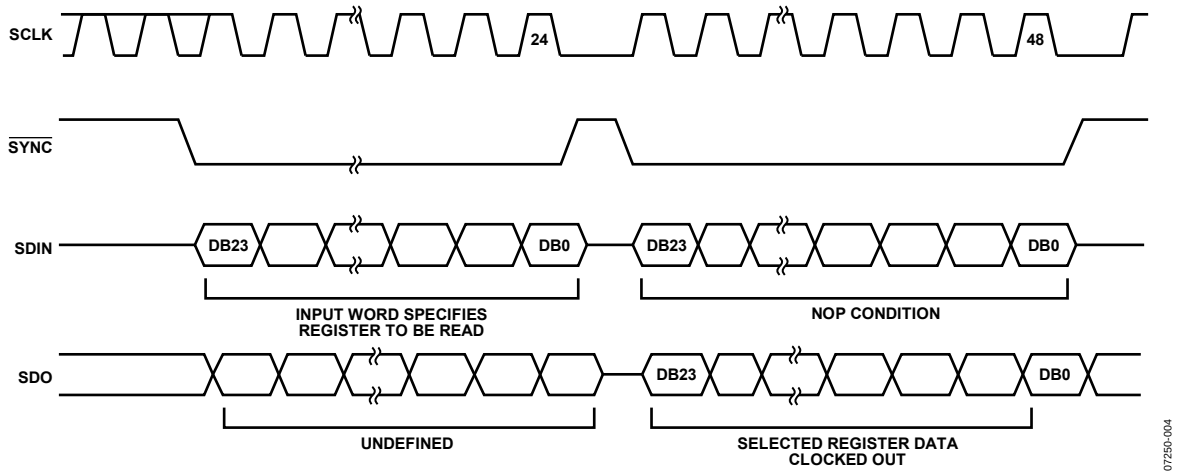


Figure 4. Readback Timing Diagram

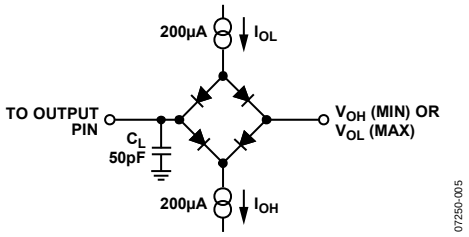


Figure 5. Load Circuit for SDO Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
AV_{DD} to AGNDx, DGND	−0.3 V to +7 V
AV_{SS} to AGNDx, DGND	+0.3 V to −7 V
DV_{CC} to DGND	−0.3 V to +7 V
DV_{CC} to AVDD	$-DV_{CC}$ to +0.25 V
Digital Inputs to DGND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Digital Outputs to DGND	−0.3 V to DV_{CC} + 0.3 V
REFx to AGNDx, PGND	−0.3 V to AV_{DD} + 0.3 V
VOUTx to AGNDx	AV_{SS} to AV_{DD}
AGNDx to DGND	−0.3 V to +0.3 V
Operating Temperature Range (T_A)	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
32-Lead TQFP	
θ_{JA} Thermal Impedance	65°C/W
θ_{JC} Thermal Impedance	12°C/W
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

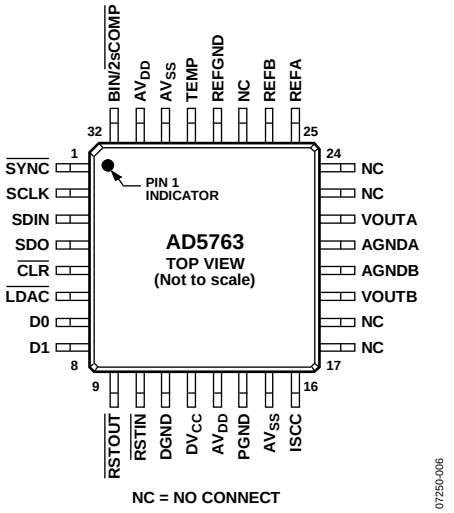


Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{SYNC}}$	Active Low Input. This pin is the frame synchronization signal for the serial interface. While $\overline{\text{SYNC}}$ is low, data is transferred in on the falling edge of SCLK.
2	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This pin operates at clock speeds up to 30 MHz.
3	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
4	SDO	Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode.
5[1]	$\overline{\text{CLR}}$	Negative Edge Triggered Input. Asserting this pin sets the DAC registers to 0x0000.[1]
6	$\overline{\text{LDAC}}$	Load DAC. Logic input. This pin is used to update the DAC registers and consequently the analog outputs. When $\overline{\text{LDAC}}$ is tied permanently low, the addressed DAC register is updated on the rising edge of $\overline{\text{SYNC}}$. If $\overline{\text{LDAC}}$ is held high during the write cycle, the DAC input register is updated but the output update is held off until the falling edge of $\overline{\text{LDAC}}$. In this mode, all analog outputs can be updated simultaneously on the falling edge of $\overline{\text{LDAC}}$. The $\overline{\text{LDAC}}$ pin must not be left unconnected.
7, 8	D0, D1	D0 and D1 form a digital I/O port. The user can set up these pins as inputs or outputs that are configurable and readable over the serial interface. When configured as inputs, these pins have weak internal pull-ups to DV_{CC}. When programmed as outputs, D0 and D1 are referenced by DV_{CC} and DGND.
9	$\overline{\text{RSTOUT}}$	Reset Logic Output. This pin is the output from the on-chip voltage monitor used in the reset circuit. If desired, it can be used to control other system components.
10	$\overline{\text{RSTIN}}$	Reset Logic Input. This input allows external access to the internal reset logic. Applying a Logic 0 to this input clamps the DAC outputs to 0 V. In normal operation, $\overline{\text{RSTIN}}$ should be tied to Logic 1. Register values remain unchanged.
11	DGND	Digital Ground Pin.
12	DV_{CC}	Digital Supply Pin. The voltage ranges from 2.7 V to 5.25 V.
13, 31	AV_{DD}	Positive Analog Supply Pins. The voltage ranges from 4.75 V to 5.25 V.
14	PGND	Ground Reference Point for Analog Circuitry.
15, 30	AV_{SS}	Negative Analog Supply Pins. The voltage ranges from −5.25 V to −4.75 V.
16	ISCC	This pin is used in association with an optional external resistor connected to AGND and programs the short-circuit current of the output amplifiers. See the Design Features section for further details.
17, 18, 23, 24, 27	NC	No Connect.
19	VOUTB	Analog Output Voltage of DAC B. Buffered output with a nominal full-scale output range of ±4.096 V. The output amplifier is capable of directly driving a 5 kΩ, 200 pF load.
20	AGNDB	Ground Reference Pin for the DAC B Output Amplifier.
21	AGNDA	Ground Reference Pin for the DAC A Output Amplifier.

Pin No.	Mnemonic	Description
22	VOUTA	Analog Output Voltage of DAC A. Buffered output with a nominal full-scale output range of ±4.096 V. The output amplifier is capable of directly driving a 5 kΩ, 200 pF load.
25	REFA	Reference Voltage Input. The reference input range is 1 V to 2.1 V. This pin programs the full-scale output voltage. REFA = 2.048 V for specified performance.
26	REFB	Reference Voltage Input. The reference input range is 1 V to 2.1 V. This pin programs the full-scale output voltage. REFB = 2.048 V for specified performance.
28	REFGND	Reference Ground Return for the Reference Generator and Buffers.
29	TEMP	This pin provides an output voltage proportional to temperature. The output voltage is 1.44 V typical at 25°C die temperature; variation with temperature is 3 mV/°C.
32	BIN/$\overline{2s\text{COMP}}$	Determines the DAC Coding. This pin should be hardwired to either DV_{CC} or DGND. When hardwired to DV_{CC}, the input coding is offset binary. When hardwired to DGND, the input coding is twos complement (see Table 7).

[1] Internal pull-up device on this logic input. Therefore, it can be left floating and defaults to a logic high condition.

TYPICAL PERFORMANCE CHARACTERISTICS

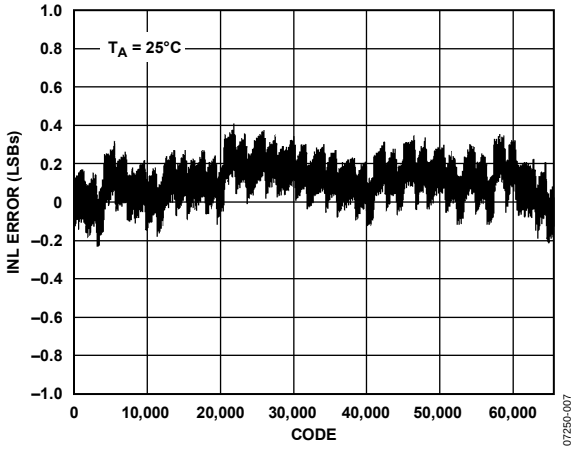


Figure 7. Integral Nonlinearity Error vs. Code

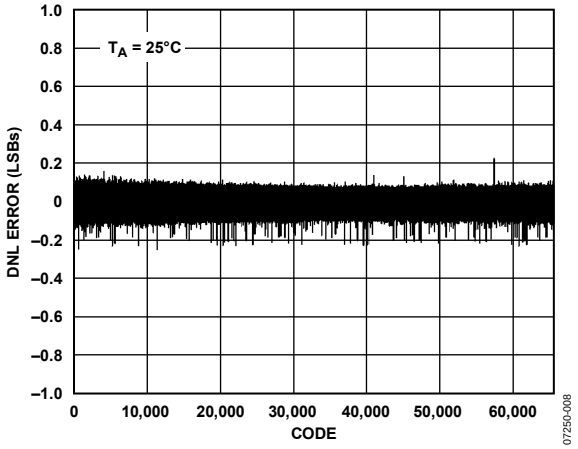


Figure 8. Differential Nonlinearity Error vs. Code

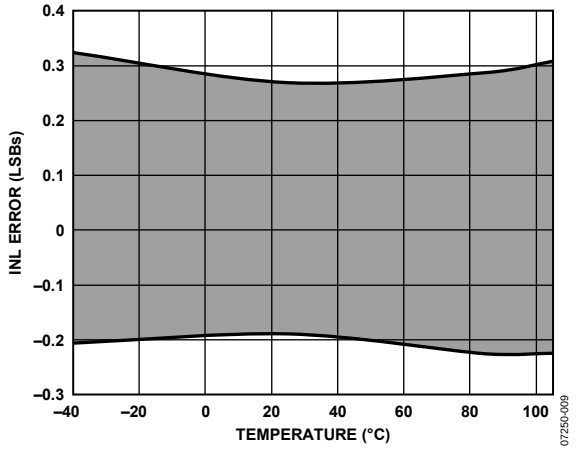


Figure 9. Integral Nonlinearity Error vs. Temperature

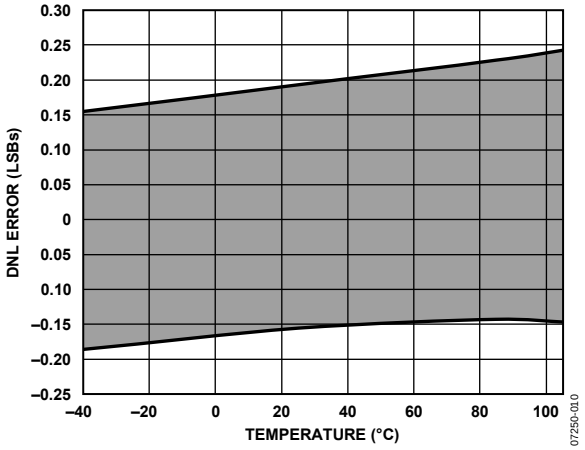


Figure 10. Differential Nonlinearity Error vs. Temperature

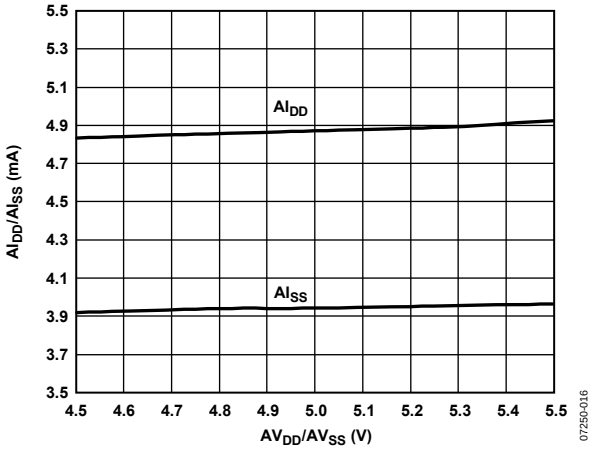


Figure 11. AI_{DD}/AI_{SS} vs. AV_{DD}/AV_{SS}

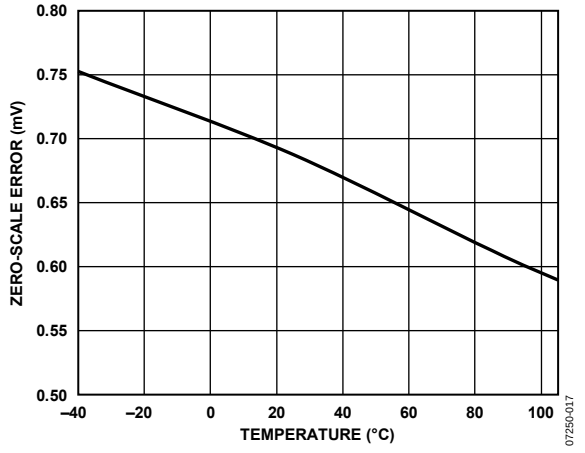


Figure 12. Zero-Scale Error vs. Temperature

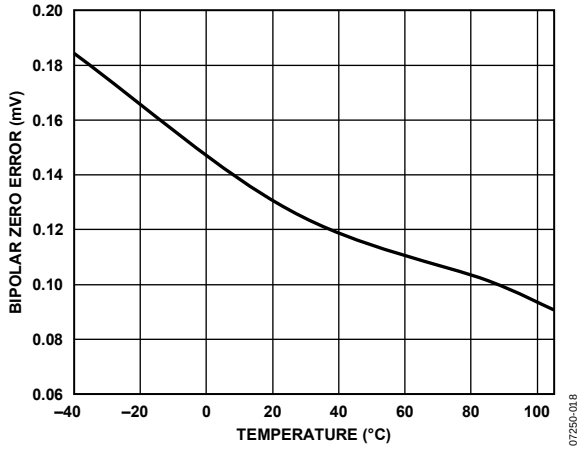


Figure 13. Bipolar Zero Error vs. Temperature

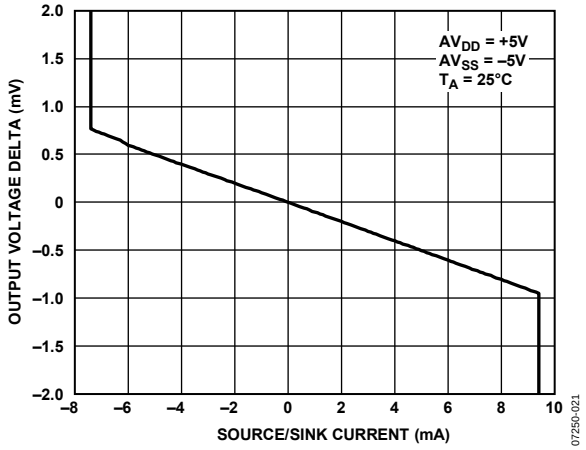


Figure 16. Source and Sink Capability of Output Amplifier with Positive Full-Scale Loaded

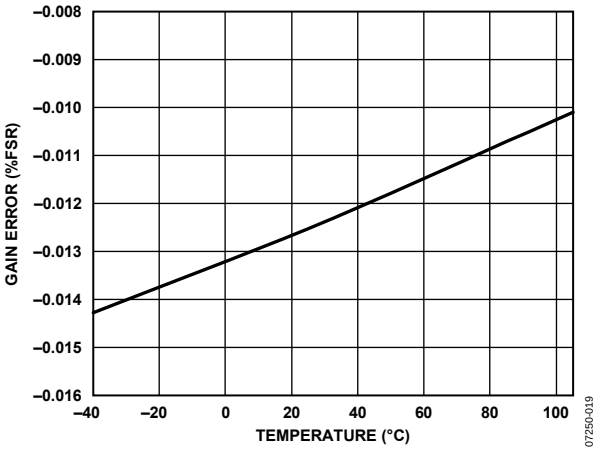


Figure 14. Gain Error vs. Temperature

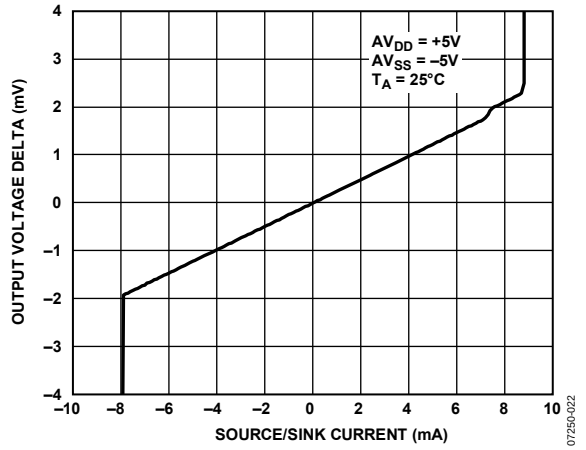


Figure 17. Source and Sink Capability of Output Amplifier with Negative Full-Scale Loaded

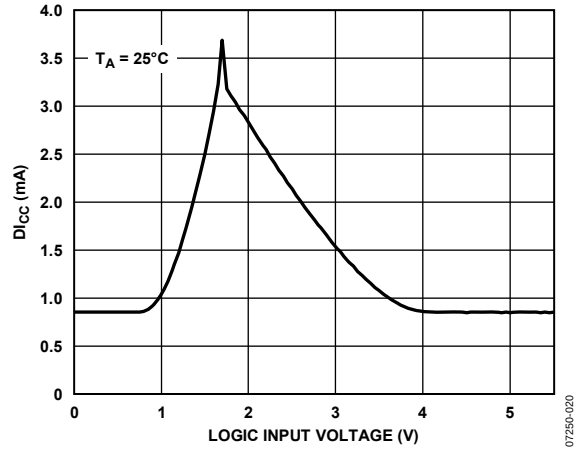


Figure 15. DI_{CC} vs. Logic Input Voltage

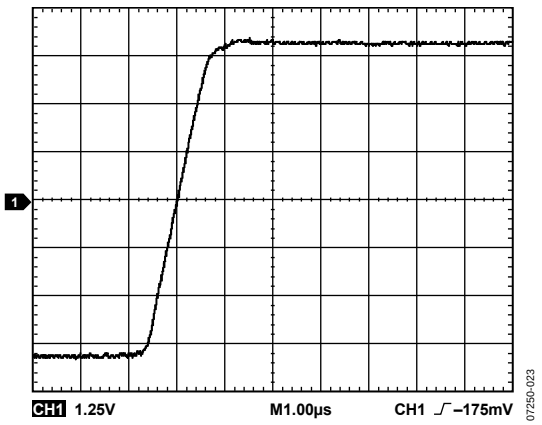


Figure 18. Positive Full-Scale Step

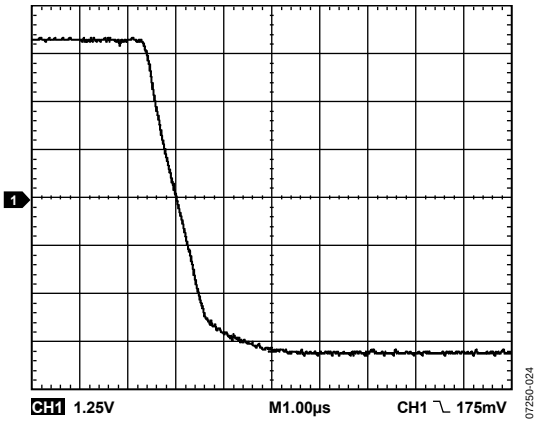


Figure 19. Negative Full-Scale Step

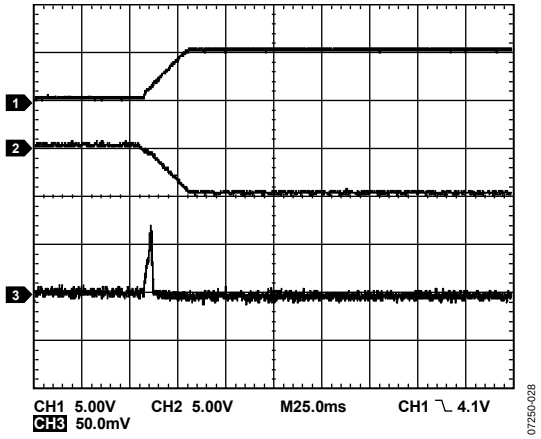


Figure 22. VOUTx vs. AV_{DD}/AV_{SS} on Power-Up

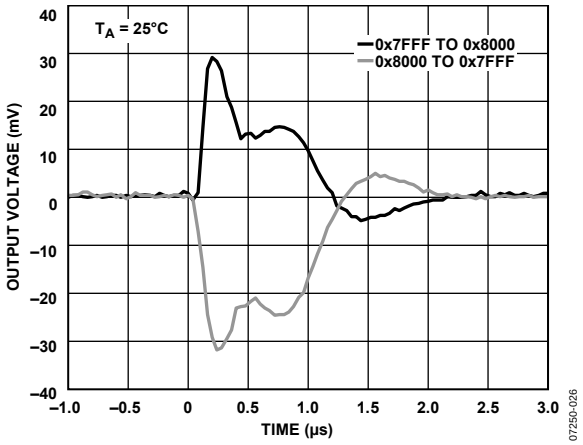


Figure 20. Major Code Transition Glitch Energy

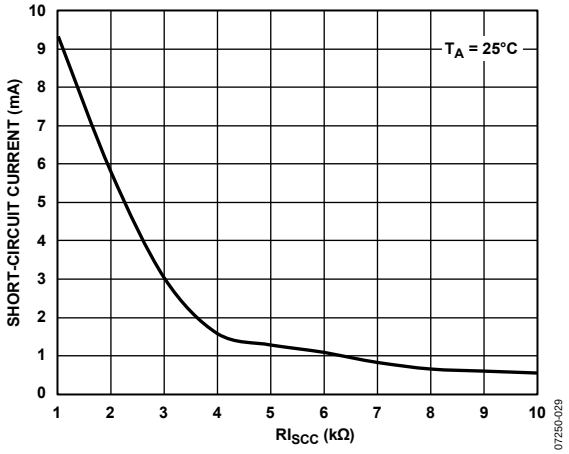


Figure 23. Short-Circuit Current vs. RI_{SCC}

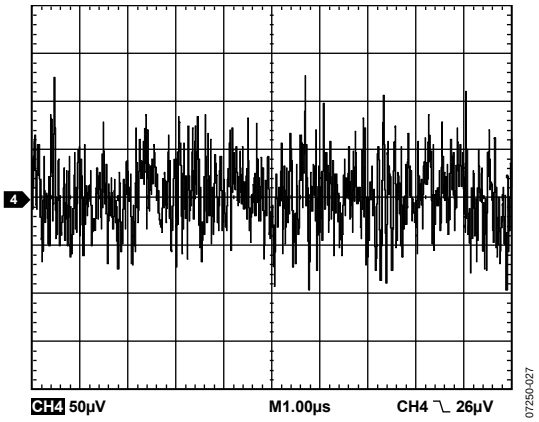


Figure 21. Peak-to-Peak Noise (100 kHz Bandwidth)

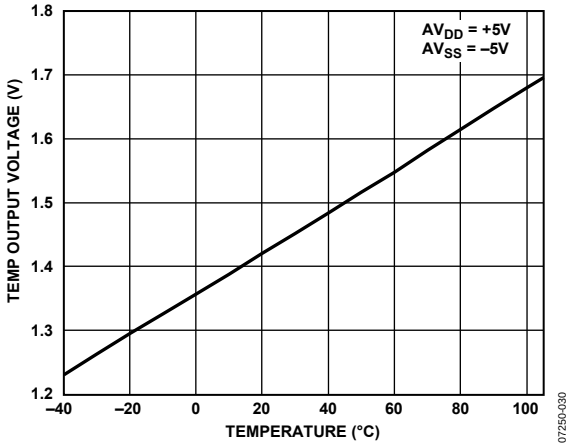


Figure 24. TEMP Output Voltage vs. Temperature

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or INL is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 7.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic. A typical DNL vs. code plot can be seen in Figure 8.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for the increasing digital input code. The AD5763 is monotonic over its full operating temperature range.

Bipolar Zero Error
Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (offset binary coding) or 0x0000 (twos complement coding). A plot of bipolar zero error vs. temperature can be seen in Figure 13.

Bipolar Zero Temperature Coefficient (TC)
Bipolar zero TC is the measure of the change in the bipolar zero error with a change in temperature. It is expressed in ppm FSR/°C.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output voltage should be $2 \times V_{REF} - 1$ LSB. Full-scale error is expressed in percentage of full-scale range.

Negative Full-Scale Error/Zero-Scale Error
Negative full-scale error is the error in the DAC output voltage when 0x0000 (offset binary coding) or 0x8000 (twos complement coding) is loaded to the DAC register. Ideally, the output voltage should be $-2 \times V_{REF}$. A plot of zero-scale error vs. temperature can be seen in Figure 12.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Slew Rate
The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage-output DAC is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is expressed in volts per microsecond.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range. A plot of gain error vs. temperature can be seen in Figure 14.

Total Unadjusted Error (TUE)
TUE is a measure of the output error considering all the various errors.

Zero-Scale Error Temperature Coefficient (TC)
Zero-scale error TC is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/°C.

Gain Error Temperature Coefficient (TC)
Gain error TC is a measure of the change in gain error with changes in temperature. Gain error TC is expressed in ppm FSR/°C.

Digital-to-Analog Glitch Energy
Digital-to-analog glitch energy is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition glitch (0x7FFF to 0x8000) (see Figure 20).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s, and vice versa.

Power Supply Sensitivity
Power supply sensitivity indicates how the output of the DAC is affected by changes in the power supply voltage.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC, and is expressed in LSB.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs by a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-sec.

Channel-to-Channel Isolation
Channel-to-channel isolation is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in decibels.

Digital Crosstalk
Digital crosstalk is a measure of the impulse injected into the analog output of one DAC from the digital inputs of another DAC, but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s, and vice versa.

THEORY OF OPERATION

The AD5763 is a dual, 16-bit, serial input, bipolar voltage output DAC and operates from supply voltages of ±4.75 V to ±5.25 V. The part has a specified buffered output voltage of up to ±4.311 V. Data is written to the AD5763 in a 24-bit word format via a 3-wire serial interface. The device also offers an SDO pin, which is available for daisy-chaining or readback.

The AD5763 incorporates a power-on reset circuit, which ensures that the DAC registers power-up loaded with 0x0000. The AD5763 features a digital I/O port that can be programmed via the serial interface, on-chip reference buffers, per channel digital gain, and offset registers.

DAC ARCHITECTURE

The DAC architecture of the AD5763 consists of a 16-bit current mode segmented R-2R ladder DAC. The simplified circuit diagram for the DAC section is shown in Figure 25.

The four MSBs of the 16-bit data-word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of the 15 matched resistors to either AGNDx or IOUT. The remaining 12 bits of the data-word drive Switch S0 to Switch S11 of the 12-bit R-2R ladder network.

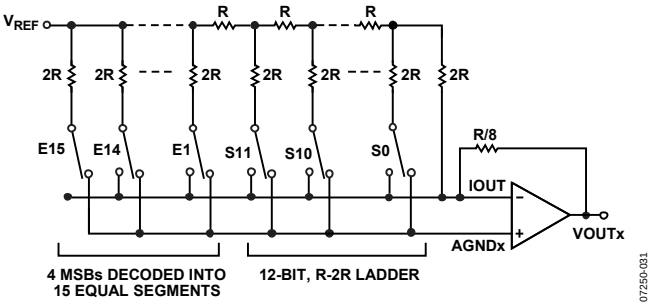


Figure 25. DAC Ladder Structure

REFERENCE BUFFERS

The AD5763 operates with an external reference. The reference inputs (REFA and REFB) have an input range up to 2.1 V. This input voltage is then used to provide a buffered positive and negative reference for the DAC cores. The positive reference (V_{REFP}) is given by

$$V_{REFP} = 2V_{REF}$$

The negative reference (V_{REFN}) to the DAC cores is given by

$$V_{REFN} = -2V_{REF}$$

These positive and negative reference voltages (along with the gain register values) define the output ranges of the DACs.

SERIAL INTERFACE

The AD5763 is controlled over a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI™, MICROWIRE™, and DSP standards.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. The input register consists of a read/write bit, three register select bits, three DAC address bits and 16 data bits as shown in Table 8. The timing diagram for this operation is shown in Figure 2.

Upon power-up, the DAC registers are loaded with zero code (0x0000) and the outputs are clamped to 0 V via a low impedance path. The outputs can be updated with the zero code value at this time by asserting either $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$. The corresponding output voltage depends on the state of the BIN/$\overline{\text{2sCOMP}}$ pin. If BIN/$\overline{\text{2sCOMP}}$ is tied to DGND, then the data coding is twos complement and the outputs update to 0 V. If the BIN/$\overline{\text{2sCOMP}}$ pin is tied to DV_{CC}, then the data coding is offset binary and the outputs update to negative full-scale. To have the outputs power-up with zero code loaded to the outputs, the $\overline{\text{CLR}}$ pin should be held low during power-up.

Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can only be used if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. Exactly 24 falling clock edges must be applied to SCLK before $\overline{\text{SYNC}}$ is brought high again. If $\overline{\text{SYNC}}$ is brought high before the 24th falling SCLK edge, then the data written is invalid. If more than 24 falling SCLK edges are applied before $\overline{\text{SYNC}}$ is brought high, then the input data is also invalid. The addressed input register is updated on the rising edge of $\overline{\text{SYNC}}$. For another serial transfer to take place, $\overline{\text{SYNC}}$ must be brought low again. After the end of the serial data transfer, data is automatically transferred from the input shift register to the addressed register.

When the data has been transferred into the chosen register of the addressed DAC, all DAC registers and outputs can be updated by taking $\overline{\text{LDAC}}$ low.

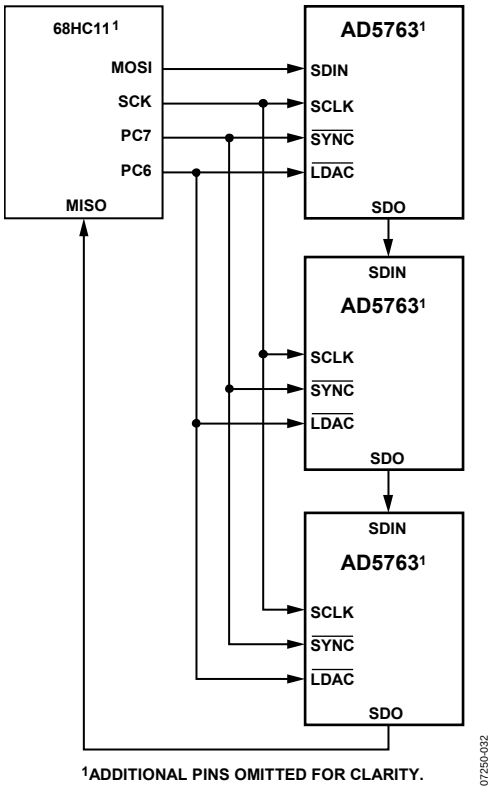


Figure 26. Daisy-Chaining the AD5763

Daisy-Chain Operation

For systems that contain several devices, the SDO pin can be used to daisy-chain multiple devices together. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24n, where n is the total number of AD5763 devices in the chain. When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register. The SCLK can be a continuous or a gated clock.

A continuous SCLK source can only be used if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data.

Readback Operation

Before a readback operation is initiated, the SDO pin must be enabled by writing to the function register and clearing the SDO disable bit; this bit is cleared by default. Readback mode is invoked by setting the R/$\overline{\text{W}}$ bit to 1 in the serial input register write. When R/$\overline{\text{W}}$ is 1, Bit A2 to Bit A0 select the register to be read in association with Bit REG2, Bit REG1, and Bit REG0. The remaining data bits in the write sequence are don't cares. During the next SPI write, the data appearing on the SDO output contains the data from the previously addressed register. For a read of a single register, the NOP command can be used in clocking out the data from the selected register on SDO. The readback diagram in Figure 4 shows the readback sequence. For example, to read back the fine gain register of Channel A on the AD5763, the following sequence should be implemented:

1. Write 0xA0XXXX to the AD5763 input register. This configures the AD5763 for read mode with the fine gain register of Channel A selected. Note that all the data bits, DB15 to DB0, are don't cares.
2. Follow this with a second write: 0x00XXXX, which is an NOP condition. During this write, the data from the fine gain register is clocked out on the SDO line, that is, data clocked out contains the data from the fine gain register in Bit DB5 to Bit DB0.

SIMULTANEOUS UPDATING VIA $\overline{\text{LDAC}}$

Depending on the status of both $\overline{\text{SYNC}}$ and $\overline{\text{LDAC}}$, and after data has been transferred into the input register of the DACs, there are two ways in which the DAC registers and DAC outputs can be updated.

Individual DAC Updating

In this mode, $\overline{\text{LDAC}}$ is held low while data is being clocked into the input shift register. The addressed DAC output is updated on the rising edge of $\overline{\text{SYNC}}$.

Simultaneous Updating of All DACs

In this mode, $\overline{\text{LDAC}}$ is held high while data is being clocked into the input shift register. All DAC outputs are updated by taking $\overline{\text{LDAC}}$ low any time after $\overline{\text{SYNC}}$ has been taken high. The update now occurs on the falling edge of $\overline{\text{LDAC}}$.

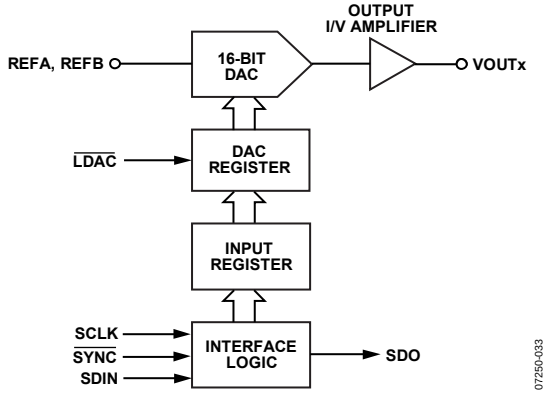


Figure 27. Simplified Serial Interface of Input Loading Circuitry for One DAC Channel

TRANSFER FUNCTION

Table 7 shows the ideal input code to output voltage relationship for the AD5763 for both offset binary and twos complement data coding.

Table 7. Ideal Output Voltage to Input Code Relationship

Digital Input				Analog Output
Offset Binary Data Coding				
MSB			**LSB**	**VOUTx**
1111	1111	1111	1111	$+2V_{REF} \times (32{,}767/32{,}768)$
1000	0000	0000	0001	$+2V_{REF} \times (1/32{,}768)$
1000	0000	0000	0000	0 V
0111	1111	1111	1111	$-2V_{REF} \times (1/32{,}768)$
0000	0000	0000	0000	$-2V_{REF} \times (32{,}767/32{,}768)$
Twos Complement Data Coding				
MSB			**LSB**	**VOUTx**
0111	1111	1111	1111	$+2V_{REF} \times (32{,}767/32{,}768)$
0000	0000	0000	0001	$+2V_{REF} \times (1/32{,}768)$
0000	0000	0000	0000	0 V
1111	1111	1111	1111	$-2V_{REF} \times (1/32{,}768)$
1000	0000	0000	0000	$-2V_{REF} \times (32{,}767/32{,}768)$

The output voltage expression for the AD5763 is given by

$$VOUTx = -2 \times V_{REFIN} + 4 \times V_{REFIN}\left[\frac{D}{65{,}536}\right]$$

where:
D is the decimal equivalent of the code loaded to the DAC.
V_{REFIN} is the reference voltage applied at the REFA and REFB pins.

ASYNCHRONOUS CLEAR ($\overline{CLR}$)

$\overline{CLR}$ is a negative edge triggered clear that allows the outputs to be cleared to either 0 V (twos complement coding) or negative full scale (offset binary coding). It is necessary to keep $\overline{CLR}$ low for a minimum amount of time for the operation to complete (see Figure 2). When the $\overline{CLR}$ signal is returned high, the output remains at the cleared value until a new value is programmed. If at power-on, $\overline{CLR}$ is at 0 V, all DAC outputs are updated with the clear value. A clear can also be initiated through software by writing a command, 0x04XXXX, to the AD5763.

Table 8. Input Register Format

MSB								**LSB**
DB23	**DB22**	**DB21**	**DB20**	**DB19**	**DB18**	**DB17**	**DB16**	**DB15:DB0**
R/$\overline{W}$	0	REG2	REG1	REG0	A2	A1	A0	Data

Table 9. Input Register Bit Functions

Bit	**Description**			
R/$\overline{W}$	Indicates a read from or a write to the addressed register			
REG2, REG1, REG0	These bits are used in association with the address bits to determine if a read or write operation is sent to the function register, data register, offset register, or gain register			
	REG2	**REG1**	**REG0**	**Function**
	0	0	0	Function register
	0	1	0	Data register
	0	1	1	Coarse gain register
	1	0	0	Fine gain register
	1	0	1	Offset register
A2, A1, A0	These bits are used to decode the DAC channels			
	A2	**A1**	**A0**	**Channel Address**
	0	0	0	DAC A
	0	0	1	DAC B
	1	0	0	Both DACs
D15:D0	Data bits			

FUNCTION REGISTER

The function register is addressed by setting the three REG bits to 000. The values written to the address bits and the data bits determine the function addressed. The functions available via the function register are outlined in Table 10 and Table 11.

Table 10. Function Register Options

REG2	REG1	REG0	A2	A1	A0	DB15:DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	NOP, data = don't care						
0	0	0	0	0	1	Don't care	Local-ground-offset adjust	D1 direction	D1 value	D0 direction	D0 value	SDO disable
0	0	0	1	0	0	Clear, data = don't care						
0	0	0	1	0	1	Load, data = don't care						

Table 11. Explanation of Function Register Options

Option	Description
NOP	No operation instruction used in readback operations.
Local-Ground-Offset Adjust	Set by the user to enable local-ground-offset adjust function. Cleared by the user to disable local-ground-offset adjust function (default). See the Design Features section for further details.
D0/D1 Direction	Set by the user to enable D0, D1 as outputs. Cleared by the user to enable D0, D1 as inputs (default). See the Design Features section for further details.
D0/D1 Value	I/O port status bits. Logic values written to these locations determine the logic outputs on the D0 and D1 pins when configured as outputs. These bits indicate the status of the D0 and D1 pins when the I/O port is active as an input. When enabled as inputs, these bits are don't cares during a write operation.
SDO Disable	Set by the user to disable the SDO output. Cleared by the user to enable the SDO output (default).
Clear	Addressing this function resets the DAC outputs to 0 V in twos complement mode and negative full scale in binary mode.
Load	Addressing this function updates the DAC registers and, consequently, the analog outputs.

DATA REGISTER

The data register is addressed by setting the three REG bits to 010. The DAC address bits select with which DAC channel the data transfer is to take place (see Table 9). The data bits are in Position DB15 to Position DB0 as shown in Table 12.

Table 12. Programming the Data Register

REG2	REG1	REG0	A2	A1	A0	DB15 … DB0
0	1	0	DAC address			16-bit DAC data

COARSE GAIN REGISTER

The coarse gain register is addressed by setting the three REG bits to 011. The DAC address bits select with which DAC channel the data transfer is to take place (see Table 9). The coarse gain register is a 2-bit register and allows the user to select the output range of each DAC as shown in Table 13 and Table 14.

Table 13. Programming the Coarse Gain Register

REG2	REG1	REG0	A2	A1	A0	DB15:DB2	DB1	DB0
0	1	1	DAC address			Don't care	CG1	CG0

Table 14. Output Range Selection

Output Range	CG1	CG0
±4.096 V (Default)	0	0
±4.20103 V	0	1
±4.31158 V	1	0

FINE GAIN REGISTER

The fine gain register is addressed by setting the three REG bits to 100. The DAC address bits select with which DAC channel the data transfer is to take place (see Table 9). The fine gain register is a 6-bit register and allows the user to adjust the gain of each DAC channel by −32 LSB to +31 LSB in 1 LSB increments as shown in Table 15 and Table 16. The adjustment is made to both the positive full-scale and negative full-scale points simultaneously, each point being adjusted by ½ of one step. The fine gain register coding is twos complement.

Table 15. Programming Fine Gain Register

REG2	REG1	REG0	A2	A1	A0	DB15:DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	DAC address			Don't care	FG5	FG4	FG3	FG2	FG1	FG0

Table 16. Fine Gain Register Options

Gain Adjustment	FG5	FG4	FG3	FG2	FG1	FG0
+31 LSB	0	1	1	1	1	1
+30 LSB	0	1	1	1	1	0
…	…	…	…	…	…	…
No Adjustment (Default)	0	0	0	0	0	0
…	…	…	…	…	…	…
−31 LSB	1	0	0	0	0	1
−32 LSB	1	0	0	0	0	0

OFFSET REGISTER

The offset register is addressed by setting the three REG bits to 101. The DAC address bits select with which DAC channel the data transfer is to take place (see Table 9). The AD5763 offset register is an 8-bit register and allows the user to adjust the offset of each channel by −16 LSB to +15.875 LSB in increments of ⅛ LSB as shown in Table 17 and Table 18. The offset register coding is twos complement.

Table 17. Programming the Offset Register

REG2	REG1	REG0	A2	A1	A0	DB15:DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	DAC address			Don't care	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0

Table 18. Offset Register Options

Offset Adjustment	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0
+15.875 LSB	0	1	1	1	1	1	1	1
+15.75 LSB	0	1	1	1	1	1	1	0
…	…	…	…	…	…	…	…	…
No Adjustment (Default)	0	0	0	0	0	0	0	0
…	…	…	…	…	…	…	…	…
−15.875 LSB	1	0	0	0	0	0	0	1
−16 LSB	1	0	0	0	0	0	0	0

WORKED EXAMPLE OF OFFSET AND GAIN ADJUSTMENT

Using the information provided in the previous section, the following worked example demonstrates how the functions of the AD5763 can be used to eliminate both offset and gain errors. Because the AD5763 is factory calibrated, offset and gain errors should be negligible. However, errors can be introduced by the system that the AD5763 is operating within; for example, a voltage reference value that is not equal to 2.048 V introduces a gain error. An output range of ±4.096 V and twos complement data coding is assumed.

Removing Offset Error

The AD5763 can eliminate an offset error in the range of −2 mV to +1.98 mV with a step size of ⅛ of a 16-bit LSB.

Calculate the step size of the offset adjustment using the following equation:

$$Offset\ Adjust\ Step\ Size = \frac{8.192}{2^{16} \times 8} = 15.625\ \mu V$$

Measure the offset error by programming 0x0000 to the data register and measuring the resulting output voltage. For this example, the measured value is 614 µV.

Calculate the number of offset adjustment steps that this value represents,

$$Number\ of\ Steps = \frac{Measured\ Offset\ Value}{Offset\ Step\ Size} = \frac{614\ \mu V}{15.625\ \mu V} = 40\ Steps$$

The offset error measured is positive, therefore, a negative adjustment of 40 steps is required. The offset register is 8 bits wide and the coding is twos complement. The required offset register value can be calculated as follows:

Convert adjustment value to binary: 00101000.

Convert this to a negative twos complement number by inverting all bits and adding 1: 11011000.

11011000 is the value that should be programmed to the offset register.

Note that this twos complement conversion is not necessary in the case of a positive offset adjustment. The value to be programmed to the offset register is simply the binary representation of the adjustment value.

Removing Gain Error

The AD5763 can eliminate a gain error at negative full-scale output in the range of −2 mV to +1.94 mV with a step size of ½ of a 16-bit LSB.

Calculate the step size of the gain adjustment

$$Gain\ Adjust\ Step\ Size = \frac{8.192}{2^{16} \times 2} = 62.5\ \mu V$$

Measure the gain error by programming 0x8000 to the data register and measure the resulting output voltage. The gain error is the difference between this value and −4.096 V; for this example, the gain error is −0.8 mV.

Calculate how many gain adjustment steps this value represents

$$Number\ of\ Steps = \frac{Measured\ Gain\ Value}{Gain\ Step\ Size} = \frac{0.8\ mV}{62.5\ \mu V} = 13\ Steps$$

The gain error measured is negative (in terms of magnitude); therefore, a positive adjustment of 13 steps is required. The gain register is six bits wide and the coding is twos complement, the required gain register value can be determined as follows:

Convert adjustment value to binary: 001101.

The value to be programmed to the gain register is simply this binary number.

DESIGN FEATURES

ANALOG OUTPUT CONTROL

In many industrial process control applications, it is vital that the output voltage be controlled during power-up and during brownout conditions. When the supply voltages change, the output pins are clamped to 0 V via a low impedance path. To prevent the output amp being shorted to 0 V during this time, Transmission Gate G1 is also opened (see Figure 28). These conditions are maintained until the power supplies stabilize and a valid word is written to the DAC register. At this time, G2 opens and G1 closes. Both transmission gates are also externally controllable via the reset logic ($\overline{\text{RSTIN}}$) control input. For instance, if $\overline{\text{RSTIN}}$ is driven from a battery supervisor chip, the $\overline{\text{RSTIN}}$ input is driven low to open G1 and close G2 on power-down or during a brownout. Conversely, the on-chip voltage detector output ($\overline{\text{RSTOUT}}$) is also available to the user to control other parts of the system. The basic transmission gate functionality is shown in Figure 28.

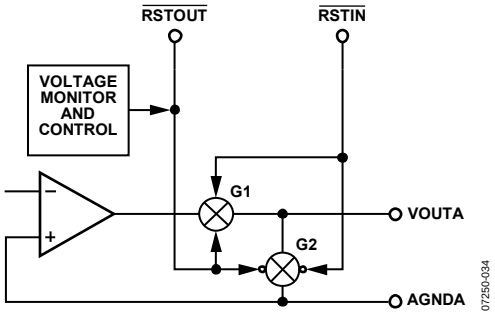


Figure 28. Analog Output Control Circuitry

DIGITAL OFFSET AND GAIN CONTROL

The AD5763 incorporates a digital offset adjust function with a ±16 LSB adjust range and 0.125 LSB resolution. The gain register allows the user to adjust the AD5763 full-scale output range. The full-scale output can be programmed to achieve full-scale ranges of ±4.096 V, ±4.201 V, or ±4.311 V. A fine gain trim is also provided.

PROGRAMMABLE SHORT-CIRCUIT PROTECTION

The short-circuit current, I_{SC}, of the output amplifiers can be programmed by inserting an external resistor between the ISCC pin and PGND. The programmable range for the current is 500 μA to 10 mA, corresponding to a resistor range of 120 kΩ to 6 kΩ. The resistor value is calculated by

$$R \approx \frac{60}{I_{SC}}$$

If the ISCC pin is left unconnected, the short-circuit current limit defaults to 5 mA. It should be noted that limiting the short circuit current to a small value can affect the slew rate of the output when driving into a capacitive load, therefore, the value of short-circuit current programmed should take into account the size of the capacitive load being driven.

DIGITAL I/O PORT

The AD5763 contains a 2-bit digital I/O port (D1 and D0). These pins can be configured as inputs or outputs independently, and can be driven or have their values read back via the serial interface. The I/O port signals are referenced to DV_{CC} and DGND. When configured as outputs, they can be used as control signals to multiplexers or can be used to control calibration circuitry elsewhere in the system. When configured as inputs, the logic signals from limit switches can be applied to D0 and D1 and can be read back via the digital interface.

DIE TEMPERATURE SENSOR

The on-chip die temperature sensor provides a voltage output that is linearly proportional to the centigrade temperature scale. Its nominal output voltage is 1.44 V at a 25°C die temperature, varying at 3 mV/°C and giving a typical output range of 1.175 V to 1.9 V over the full temperature range. Its low output impedance and linear output simplify interfacing to temperature control circuitry and ADCs. The temperature sensor is provided as more of a convenience rather than a precise feature; it is intended for indicating a die temperature change for recalibration purposes.

LOCAL GROUND OFFSET ADJUST

The AD5763 incorporates a local-ground-offset adjust feature which, when enabled in the function register, adjusts the DAC outputs for voltage differences between the individual DAC ground pins and the REFGND pin ensuring that the DAC output voltages are always with respect to the local DAC ground pin. For instance, if Pin AGNDA is at 5 mV with respect to the REFGND pin and VOUTA is measured with respect to AGNDA, then a −5 mV error results, enabling the local-ground-offset adjust feature which adjusts VOUTA by +5 mV, eliminating the error.

POWER-ON STATUS

The AD5763 has multiple power supply and digital input pins. It is important to consider the sequence in which the pins are powered up to ensure the AD5763 powers-on in the required state. The outputs will power-on either clamped to AGNDx, driving 0 V, or driving negative full-scale output (−4.096 V) depending on how the BIN/$\overline{\text{2sCOMP}}$, $\overline{\text{CLR}}$, and $\overline{\text{LDAC}}$ pins are configured during power-up. If the $\overline{\text{CLR}}$ pin is connected to DGND, it causes the DAC registers to be loaded with 0x0000 and the outputs to be updated. Consequently, the outputs are loaded with 0 V if BIN/$\overline{\text{2sCOMP}}$ is connected to DGND or negative full-scale (−4.096 V) if BIN/$\overline{\text{2sCOMP}}$ is connected to DV_{CC} corresponding respectively to the twos complement and binary voltages for the digital code 0x0000. During power-up the state of the $\overline{\text{LDAC}}$ pin has an identical effect to that of the $\overline{\text{CLR}}$ pin. If both the $\overline{\text{CLR}}$ and $\overline{\text{LDAC}}$ pins are connected to DV_{CC} during power-up the outputs power-on clamped to AGNDx and remain so until a valid write is made to the device. Table 19 outlines the possible output power-on states.

Table 19. Output Power-On State

BIN/$\overline{\text{2sCOMP}}$	$\overline{\text{CLR}}$	$\overline{\text{LDAC}}$	V_{OUT} at Power-On
DGND	DGND	DGND	0 V
DGND	DGND	DV_{CC}	0 V
DGND	DV_{CC}	DGND	0 V
DGND	DV_{CC}	DV_{CC}	Clamped to AGNDx
DV_{CC}	DGND	DGND	−4.096 V
DV_{CC}	DGND	DV_{CC}	−4.096 V
DV_{CC}	DV_{CC}	DGND	−4.096 V
DV_{CC}	DV_{CC}	DV_{CC}	Clamped to AGNDx

APPLICATIONS INFORMATION

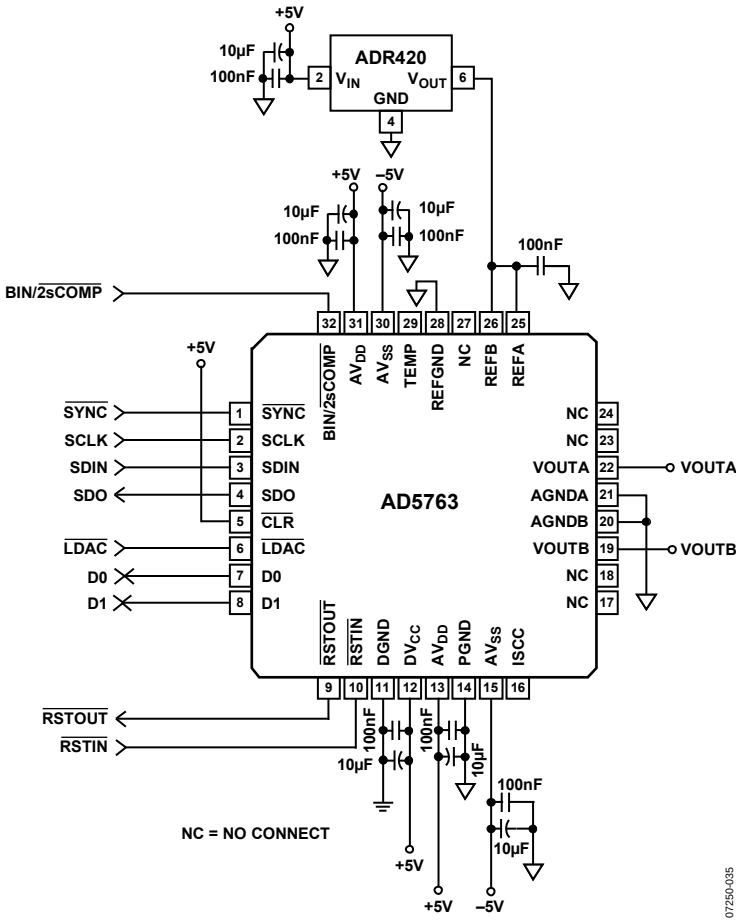


Figure 29. Typical Operating Circuit

TYPICAL OPERATING CIRCUIT

Figure 29 shows the typical operating circuit for the AD5763. The only external components needed for this precision 16-bit DAC are a reference voltage source, decoupling capacitors on the supply pins and reference inputs, and an optional short-circuit current setting resistor. Because the device incorporates reference buffers, it eliminates the need for an external bipolar reference and associated buffers. This leads to overall savings in both cost and board space.

In Figure 29, AV_{DD} is connected to +5 V and AV_{SS} is connected to −5 V and AGNDA and AGNDB are connected to REFGND.

Precision Voltage Reference Selection

To achieve the optimum performance from the AD5763 over its full operating temperature range, a precision voltage reference must be used. Give thought to the selection of a precision voltage reference. The AD5763 has two reference inputs, REFA and REFB. The voltages applied to the reference inputs are used to provide a buffered positive and negative reference for the DAC cores. Therefore, any error in the voltage reference is reflected in the outputs of the device.

There are four possible sources of error to consider when choosing a voltage reference for high accuracy applications: initial accuracy, temperature coefficient of the output voltage, long term drift, and output voltage noise.

Initial accuracy error on the output voltage of an external reference could lead to a full-scale error in the DAC. Therefore, to minimize these errors, a reference with a low initial accuracy error specification is preferred. Choosing a reference with an output trim adjustment, such as the ADR430, allows a system designer to trim system errors by setting the reference voltage to a voltage other than the nominal. The trim adjustment can also be used at temperatures to trim out any error.

Long-term drift is a measure of how much the reference output voltage drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains relatively stable over its entire lifetime.

The temperature coefficient of a reference output voltage affects INL, DNL, and TUE. A reference with a tight temperature coefficient specification should be chosen to reduce the dependence of the DAC output voltage on ambient conditions.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise needs to be considered. Choosing a reference with as low an output noise voltage as practical for the system resolution required is important. Precision voltage references such as the ADR420 (XFET® design) produce low output noise in the 0.1 Hz to 10 Hz region. However, as the circuit bandwidth increases, filtering the output of the reference may be required to minimize the output noise.

Table 20. Precision References Recommended for Use with the AD5763

Part No.	Initial Accuracy (mV Max)	Long-Term Drift (ppm Typ)	Temp Drift (ppm/°C Max)	0.1 Hz to 10 Hz Noise (µV p-p Typ)
ADR430	±1	40	3	3.5
ADR420	±1	50	3	1.75

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board (PCB) on which the AD5763 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5763 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. Establish the star ground point as close as possible to the device. The AD5763 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI) such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5763 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them. This is not required on a multilayer board, which has a separate ground plane, however, it is helpful to separate the lines. It is essential to minimize noise on the reference inputs, because it couples through to the DAC output. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is recommended, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane and signal traces are placed on the solder side.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that might occur. Iso-couplers provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5763 makes it ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 30 shows a 4-channel isolated interface to the AD5763 using an ADuM1400.

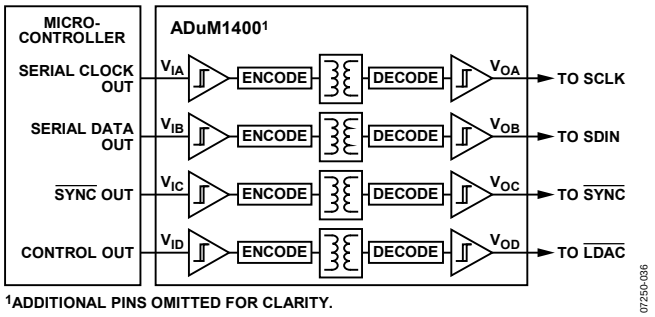


Figure 30. Isolated Interface

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5763 is via a serial bus using a standard protocol that is compatible with micro-controllers and DSP processors. The communications channel is a 3-wire minimum interface consisting of a clock signal, a data signal, and a synchronization signal. The AD5763 requires a 24-bit data-word with data valid on the falling edge of SCLK.

For all the interfaces, the DAC output update can be done automatically when all the data is clocked in, or it can be done under the control of LDAC. The contents of the DAC register can be read using the readback function.

AD5763 to Blackfin DSP Interface

Figure 31 shows how the AD5763 can be interfaced to an Analog Devices, Inc., Blackfin® DSP. The Blackfin has an integrated SPI port that can be connected directly to the SPI pins of the AD5763 and programmable I/O pins that can be used to set the state of a digital input such as the LDAC pin.

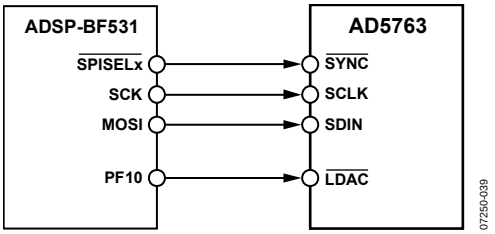
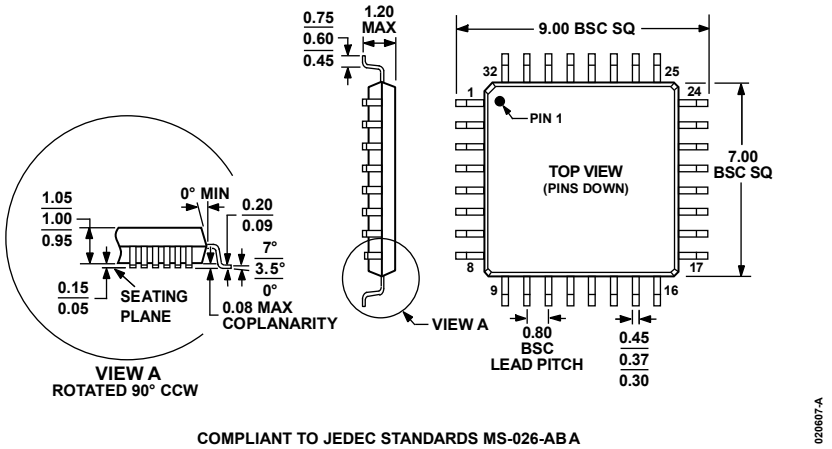


Figure 31. AD5763 to Blackfin Interface

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-ABA

Figure 32. 32-Lead Thin Plastic Quad Flat Package [TQFP]
(SU-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	INL	Temperature Range	Package Description	Package Option
AD5763CSUZ	± 2 LSB	−40°C to +105°C	32-lead Thin Plastic Flat Package [TQFP]	SU-32-2
AD5763CSUZ-REEL7	± 1 LSB	−40°C to +105°C	32-lead Thin Plastic Flat Package [TQFP]	SU-32-2

[1] Z = RoHS Compliant Part.

NOTES

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