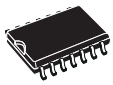
74VHCT03A

QUAD 2-INPUT OPEN DRAIN NAND GATE

- HIGH SPEED: t_{PZ} = 3.9 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION: I_{CC} = 2 µA (MAX.) at T_A=25°C
- COMPATIBLE WITH TTL OUTPUTS: V_{IH} = 2V (MIN.), V_{IL} = 0.8V (MAX)
- POWER DOWN PROTECTION ON INPUTS
- OPERATING VOLTAGE RANGE: V_{CC}(OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 03
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: V_{OLP} = 0.8V (MAX.)



SOP



TSSOP

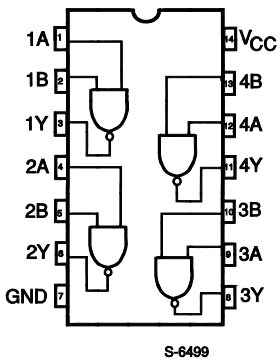
ORDER CODES

PACKAGE	TUBE	T & R
SOP	74VHCT03AM	74VHCT03AMTR
TSSOP		74VHCT03ATTR

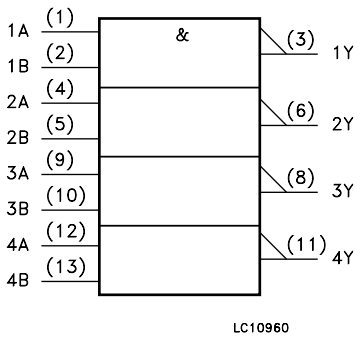
DESCRIPTION

The 74VHCT03A is an advanced high-speed CMOS QUAD 2-INPUT OPEN DRAIN NAND GATE fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.
The internal circuit is composed of 3 stages including buffer output, which provides high noise immunity and stable output.
This device can, with an external pull-up resistor, be used in wired AND configuration. This device can also be used as a led driver and in any other application requiring a current sink.
Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V since all inputs are equipped with TTL threshold.
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS

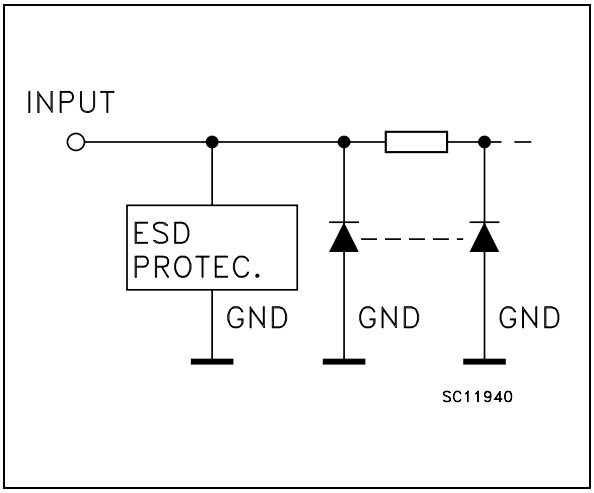


S-6499



LC10960

INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

TRUTH TABLE

A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (see note 3) (V_{CC} = 5.0 ± 0.5V)	0 to 20	ns/V

1) V_{IN} from 0.8V to 2V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5		2			2		2		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V_{OL}	Low Level Output Voltage	4.5	I_O=50 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=8 mA			0.36		0.44		0.44	
I_{OZ}	High Impedance Output Leakage Current	5.5	$V_I = V_{IH}$ or V_{IL} V_O = 0V to 5.5V			±0.25		± 2.5		± 2.5	µA
I_I	Input Leakage Current	0 to 5.5	V_I = 5.5V or GND			± 0.1		± 1.0		± 1.0	µA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND			2		20		20	µA
$\triangle I_{CC}$	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V_{CC} or GND			1.35		1.5		1.5	mA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3ns)

Symbol	Parameter	Test Condition			Value						Unit
		V_{CC} (*) (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C	
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PZL}	Propagation Delay Time	5.0	15			3.9	5.1	1.0	6.0	1.0	6.0	ns
		5.0	50			4.4	5.7	1.0	6.6	1.0	6.6	
t_{PLZ}	Propagation Delay Time	5.0	50			7.5	9.8	1.0	11.3	1.0	11.3	ns

(*) Voltage range is 5.0V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Value							Unit
			T_A = 25°C			-40 to 85°C		-55 to 125°C		
			Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance			5.8	10		10		10	pF
C_{OUT}	Output Capacitance			8.8						pF
C_{PD}	Power Dissipation Capacitance (note 1)			6						pF

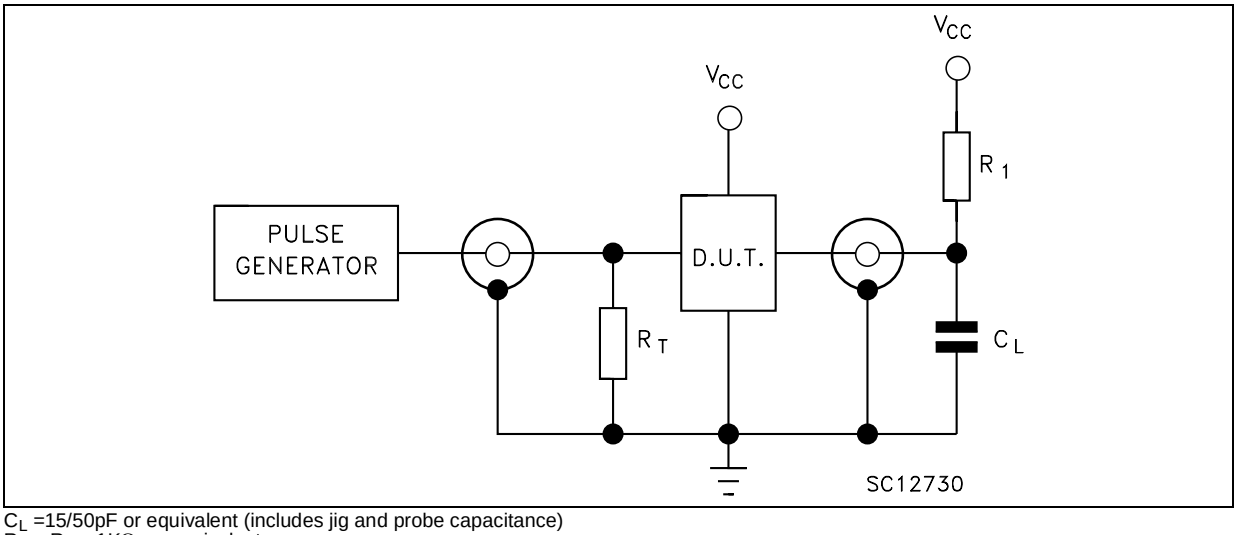
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$ (per gate)

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C_L = 50 pF		0.3	0.8					V
V_{OLV}				-0.8	-0.3						
V_{IHD}	Dynamic High Voltage Input (note 1, 3)	5.0		2.0							
V_{ILD}	Dynamic Low Voltage Input (note 1, 3)	5.0				0.8					

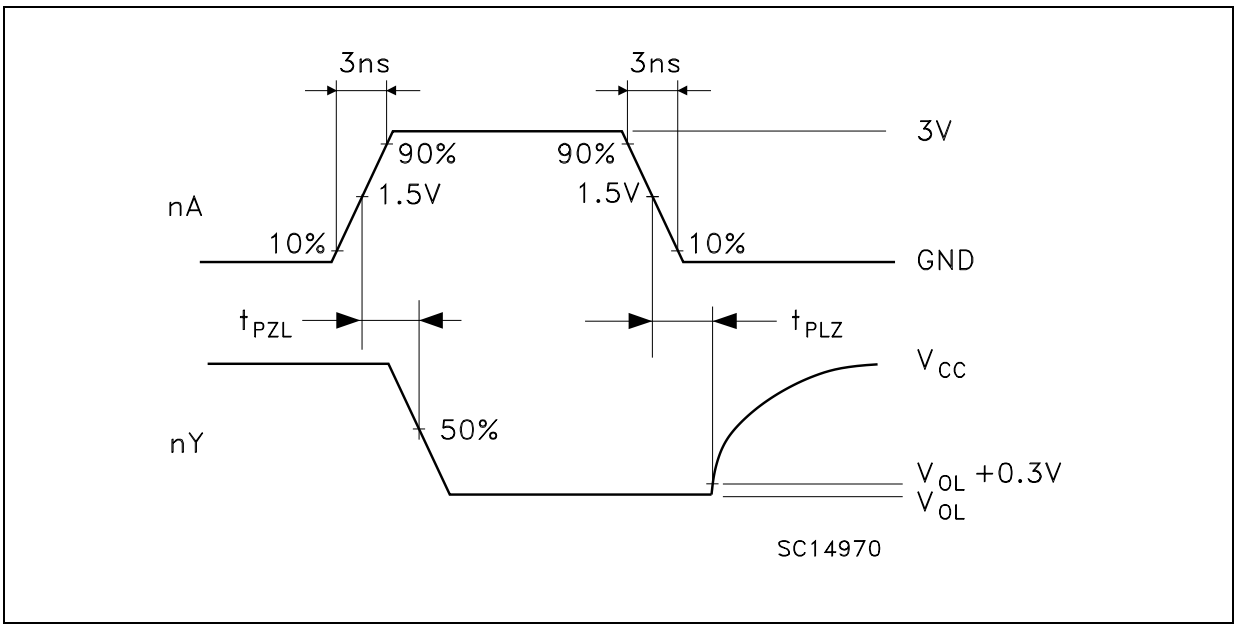
1) Worst case package.
2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.0V, (n-1) outputs switching and one output at GND.
3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.0V. Inputs under test switching: 3.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

TEST CIRCUIT



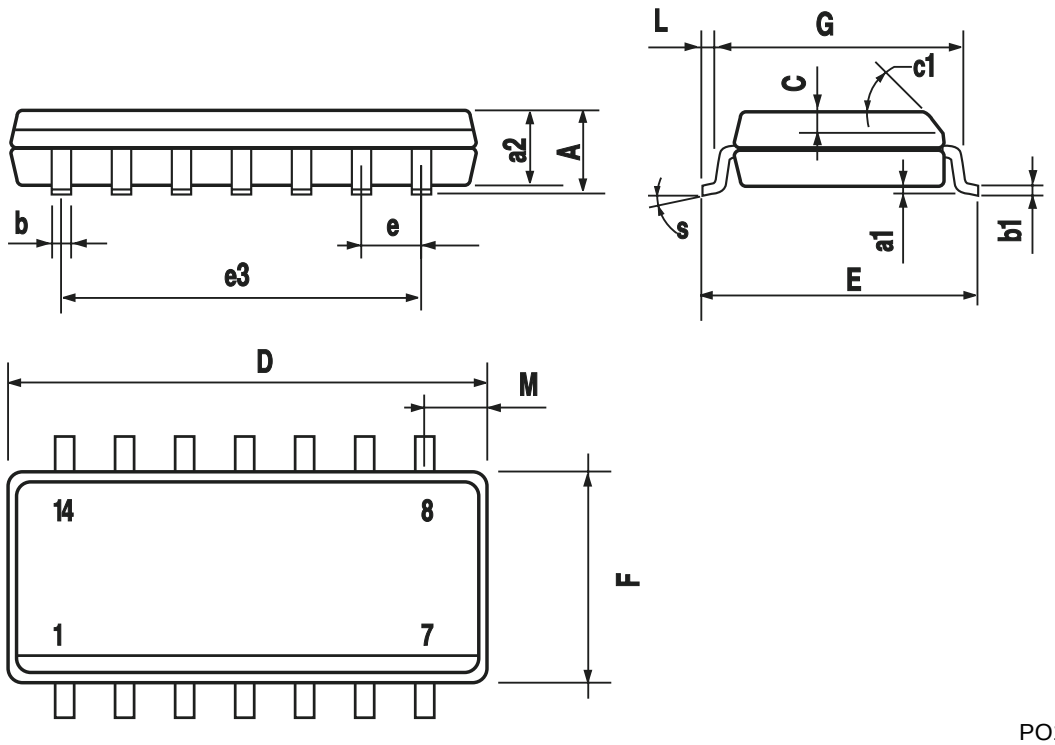
C_L =15/50pF or equivalent (includes jig and probe capacitance)
$R_L = R_1$ = 1KΩ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



SO-14 MECHANICAL DATA

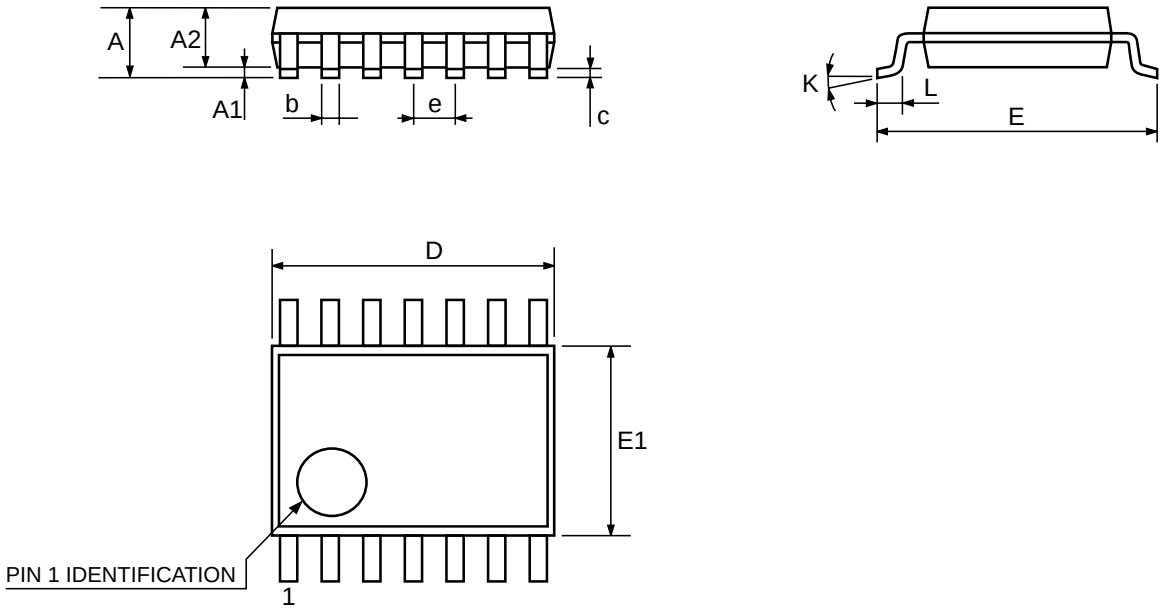
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PO13G

TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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