5-BIT PROGRAMMABLE SYNCHRONOUS BUCK, NON-SYNCHRONOUS, ADJUSTABLE LDO AND 200mA ON-BOARD LDO

FEATURES

- Provides Single Chip Solution for Vcore, GTL+, Clock Supply & 3.3V Switcher On-Board
- Second switcher provides simple control for the on-board 3.3V supply
- 200mA On-Board LDO Regulator
- Designed to meet Intel VRM 8.2 and 8.3 specification for Pentium II™
- On-Board DAC programs the output voltage from 1.3V to 3.5V
- Linear Regulator Controller On-Board for 1.5V GTL+ supply
- Loss-less Short Circuit Protection
- Synchronous Operation allows maximum efficiency
- Patented architecture allows fixed frequency operation as well as 100% duty cycle during dynamic load
- Minimum Part Count
- Soft-Start
- High current totem pole drivers for directly driving the external Power MOSFETs
- Power Good function monitors all outputs
- Over-Voltage Protection circuitry protects the switcher outputs and generates a fault output
- Thermal Shutdown

APPLICATIONS

- Total Power Solution for Pentium II processor application

DESCRIPTION

The IRU3007 controller IC is specifically designed to meet Intel specification for Pentium II™ microprocessor applications as well as the next generation of P6 family processors. The IRU3007 provides a single chip controller IC for the Vcore, LDO controller for GTL+ and an internal 200mA regulator for clock supply which are required for the Pentium II applications. It also contains a switching controller to convert 5V to 3.3V regulator for on-board applications that uses either AT type power supply or is desired not to rely on the ATX power supply's 3.3V output. These devices feature a patented topology that in combination with a few external components, as shown in the typical application circuit, will provide in excess of 14A of output current for an on-board DC/DC converter while automatically providing the right output voltage via the 5-bit internal DAC. The IRU3007 also features, loss-less current sensing for both switchers by using the $R_{DS(on)}$ of the high-side power MOSFET as the sensing resistor, internal current limiting for the clock supply, a Power Good window comparator that switches its open collector output low when any one of the outputs is outside of a pre-programmed window. Other features of the device are: Under-Voltage Lockout for both 5V and 12V supplies, an external programmable soft-start function, programming the oscillator frequency via an external resistor, Over-Voltage Protection (OVP) circuitry for both switcher outputs and an internal thermal shutdown.

TYPICAL APPLICATION

Note: Pentium II and Pentium Pro are trademarks of Intel Corp.

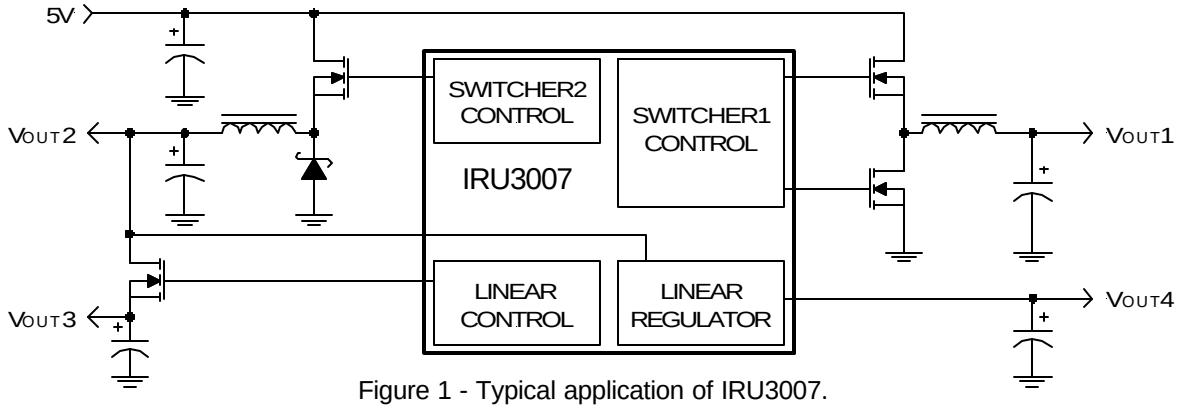


Figure 1 - Typical application of IRU3007.

PACKAGE ORDER INFORMATION

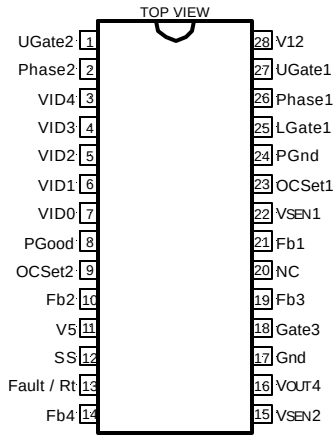
T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3007CW	28-pin Plastic SOIC WB (W)

ABSOLUTE MAXIMUM RATINGS

V5 Supply Voltage 7V
V12 Supply Voltage 20V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

28-PIN WIDE BODY PLASTIC SOIC (W)



θ_{JA} =80°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V12=12V, V5=5V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply UVLO Section						
UVLO Threshold-12V		Supply Ramping Up		10		V
UVLO Hysteresis-12V				0.4		V
UVLO Threshold-5V		Supply Ramping Up		4.3		V
UVLO Hysteresis-5V				0.3		V
Supply Current						
Operating Supply Current		V12 V5		6 30		mA
Switching Controllers; Vcore (V_{OUT}1) and I/O (V_{OUT}2)						
VID Section (Vcore only)						
DAC Output Voltage (Note 1)			0.99Vs	Vs	1.01Vs	V
DAC Output Line Regulation				0.1		%
DAC Output Temp Variation				0.5		%
VID Input LO					0.8	V
VID Input HI			2			V
VID Input Internal Pull-Up Resistor to V5			27			KΩ
V_{FB}2 Voltage				2		V
Oscillator Section (Internal)						KHz
Osc Frequency		Rt=Open		200		

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Comparator Section						
Input Bias Current					2	µA
Input Offset Voltage			-2		+2	mV
Delay to Output		V_{DIFF}=10mV			100	ns
Current Limit Section						
CS Threshold Set Current				200		µA
CS Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		C_{SS}=0.1µF		10		%
Output Drivers Section						
Rise Time		C_L=3000pF		70		ns
Fall Time		C_L=3000pF		70		ns
Dead Band Time Between High Side and Synch Drive (Vcore Switcher Only)		C_L=3000pF		200		ns
2.5V Regulator (V_{OUT}4)						
Reference Voltage	V_O4	T_A=25°C, V_{OUT}4=Fb4		1.260		V
Reference Voltage				1.260		V
Dropout Voltage		I_O=200mA		0.6		V
Load Regulation		1mA<I_O<200mA		0.5		%
Line Regulation		3.1V<$V_{I/O}$<4V, V_O=2.5V		0.2		%
Input Bias Current					2	µA
Output Current			200			mA
Current Limit			300			mA
Thermal Shutdown				145		°C
1.5V Regulator (V_{OUT}3)						
Reference Voltage	V_O3	T_A=25°C, Gate3=Fb3		1.260		V
Reference Voltage				1.260		V
Input Bias Current					2	µA
Output Drive Current			50			mA
Power Good Section						
Core UV Lower Trip Point		V_{SEN}1 Ramping Down		0.90Vs		V
Core UV Upper Trip Point		V_{SEN}1 Ramping Up		0.92Vs		V
Core UV Hysteresis				0.02Vs		V
Core OV Upper Trip Point		V_{SEN}1 Ramping Up		1.10Vs		V
Core OV Lower Trip Point		V_{SEN}1 Ramping Down		1.08Vs		V
Core OV Hysteresis				0.02Vs		V
I/O UV lower trip point		V_{SEN}2 Ramping Down		2.4		V
I/O UV Upper Trip Point		V_{SEN}2 Ramping Up		2.6		V
Fb4 Lower Trip Point		Fb4 Ramping Down		0.95		V
Fb4 Upper Trip Point		Fb4 Ramping Up		1.05		V
Fb3 Lower Trip Point		Fb3 Ramping Down		0.95		V
Fb3 Upper Trip Point		Fb3 Ramping Up		1.05		V
Power Good Output LO		R_L=3mA		0.4		V
Power Good Output HI		R_L=5K Pull Up to 5V		4.8		V
Fault (Over-Voltage) Section						
Core OV Upper Trip Point		V_{SEN}1 Ramping Up		1.17Vs		V
Core OV Lower Trip Point		V_{SEN}1 Ramping Down		1.15Vs		V
Soft-Start Section						
Pull-Up Resistor to 5V		OCSet=0V, Phase=5V		23		KΩ
I/O OV Upper Trip Point		V_{SEN}2 Ramping Up		4.3		V
I/O OV Lower Trip Point		V_{SEN}2 Ramping Down		4.2		V
Fault Output HI		I_O=3mA		10		V

Note 1: Vs refers to the set point voltage given in Table 1

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	2.0
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

Table 1 - Set point voltage vs. VID codes

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	UGate2	Output driver for the high-side power MOSFET for the I/O supply.
2	Phase2	This pin is connected to the Source of the power MOSFET for the I/O supply and it provides the negative sensing for the internal current sensing circuitry.
3	VID4	This pin selects a range of output voltages for the DAC. When in the LO state the range is 1.3V to 2.05V and when it switches to HI state the range is 2.0V to 3.5V. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
4	VID3	MSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
5	VID2	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
6	VID1	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
7	VID0	LSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
8	PGood	This pin is an open collector output that switches LO when any of the outputs are outside of the specified under voltage trip point. It also switches low when $V_{SEN}1$ pin is more than 10% above the DAC voltage setting.
9	OCSet2	This pin is connected to the Drain of the power MOSFET of the I/O supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the CS threshold depending on the R_{DS} of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.

PIN#	PIN SYMBOL	PIN DESCRIPTION
10	Fb2	This pin provides the feedback for the non-synchronous switching regulator. A resistor divider is connected from this pin to $V_{OUT}2$ and ground that sets the output voltage. The value of the resistor connected from $V_{OUT}2$ to Fb2 must be less than 100Ω.
11	V5	5V supply voltage. A high frequency capacitor (0.1 to 1μF) must be placed close to this pin and connected from this pin to the ground plane for noise free operation.
12	SS	This pin provides the soft-start for the 2 switching regulators. An internal resistor charges an external capacitor that is connected from 5V supply to this pin which ramps up the outputs of the switching regulators, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft-Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.
13	Fault / Rt	This pin has dual function. It acts as an output of the OVP circuitry or it can be used to program the frequency using an external resistor. When used as a fault detector, if any of the switcher outputs exceed the OVP trip point, the Fault pin switches to 12V and the soft-start cap is discharged. If the Fault pin is to be connected to any external circuitry, it needs to be buffered as shown in the application circuit.
14	Fb4	This pin provides the feedback for the internal LDO regulator that its output is $V_{OUT}4$.
15	$V_{SEN}2$	This pin is connected to the output of the I/O switching regulator. It is an input that provides sensing for the Under/Over-voltage circuitry for the I/O supply as well as the power for the internal LDO regulator.
16	$V_{OUT}4$	This pin is the output of the internal LDO regulator.
17	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane.
18	Gate3	This pin controls the gate of an external transistor for the 1.5V GTL+ linear regulator.
19	Fb3	This pin provides the feedback for the linear regulator that its output drive is Gate3.
20	NC	No connection.
21	Fb1	This pin provides the feedback for the synchronous switching regulator. Typically this pin can be connected directly to the output of the switching regulator. However, a resistor divider is recommended to be connected from this pin to $V_{OUT}1$ and ground to adjust the output voltage for any drop in the output voltage that is caused by the trace resistance. The value of the resistor connected from $V_{OUT}1$ to Fb1 must be less than 100Ω.
22	$V_{SEN}1$	This pin is internally connected to the undervoltage and overvoltage comparators sensing the Vcore status. It must be connected directly to the Vcore supply.
23	OCSet1	This pin is connected to the Drain of the power MOSFET of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the CS threshold depending on the R_{DS} of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
24	PGnd	This pin serves as the Power ground pin and must be connected directly to the ground plane close to the source of the synchronous MOSFET. A high frequency capacitor (typically 1μF) must be connected from V12 pin to this pin for noise free operation.
25	LGate1	Output driver for the synchronous power MOSFET for the Core supply.
26	Phase1	This pin is connected to the Source of the power MOSFET for the Core supply and it provides the negative sensing for the internal current sensing circuitry.
27	UGate1	Output driver for the high-side power MOSFET for the Core supply.
28	V12	This pin is connected to the 12V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (typically 1μF) must be placed close to this pin and PGnd pin and be connected directly from this pin to the ground plane for noise free operation.

BLOCK DIAGRAM

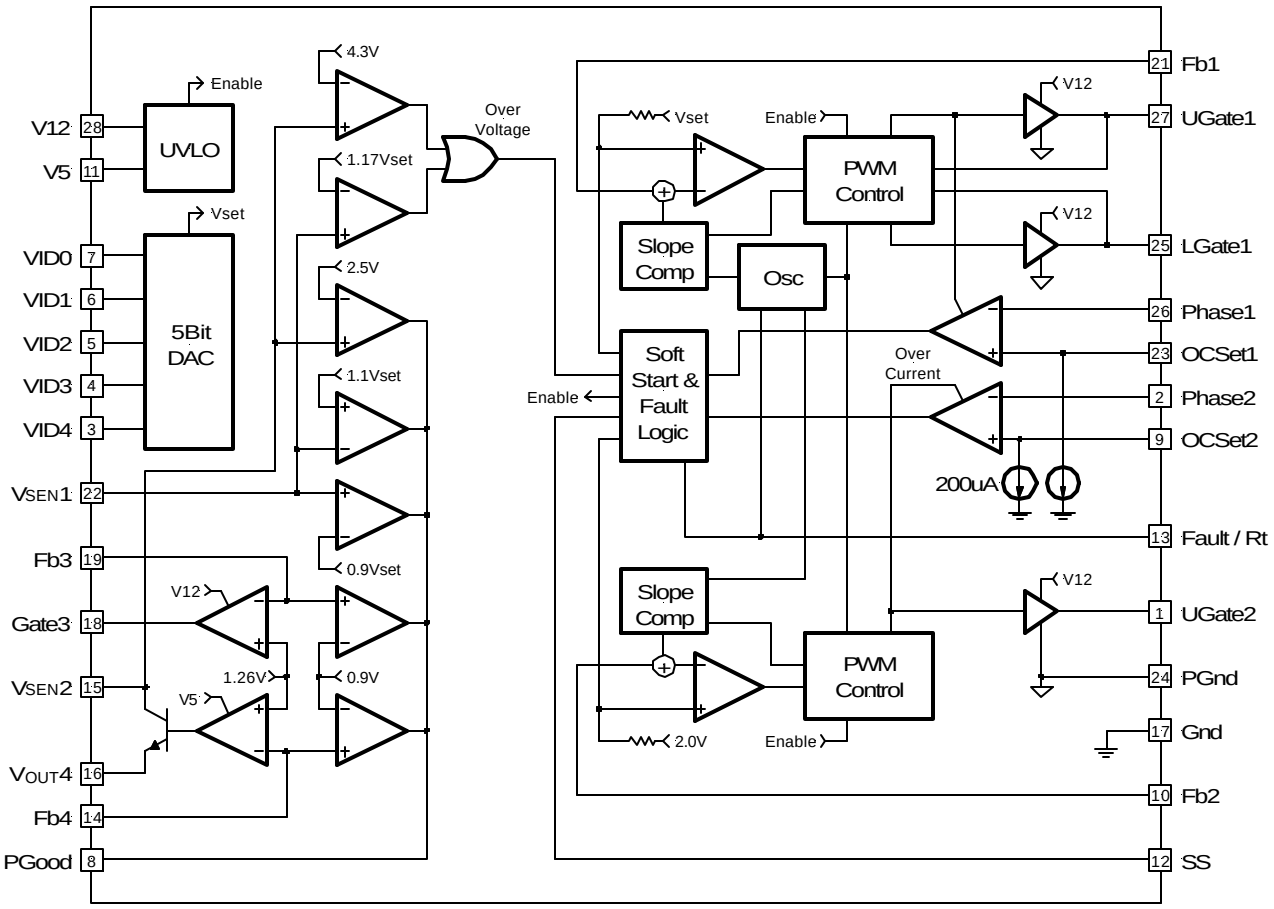


Figure 2 - Simplified block diagram of the IRU3007.

TYPICAL APPLICATION

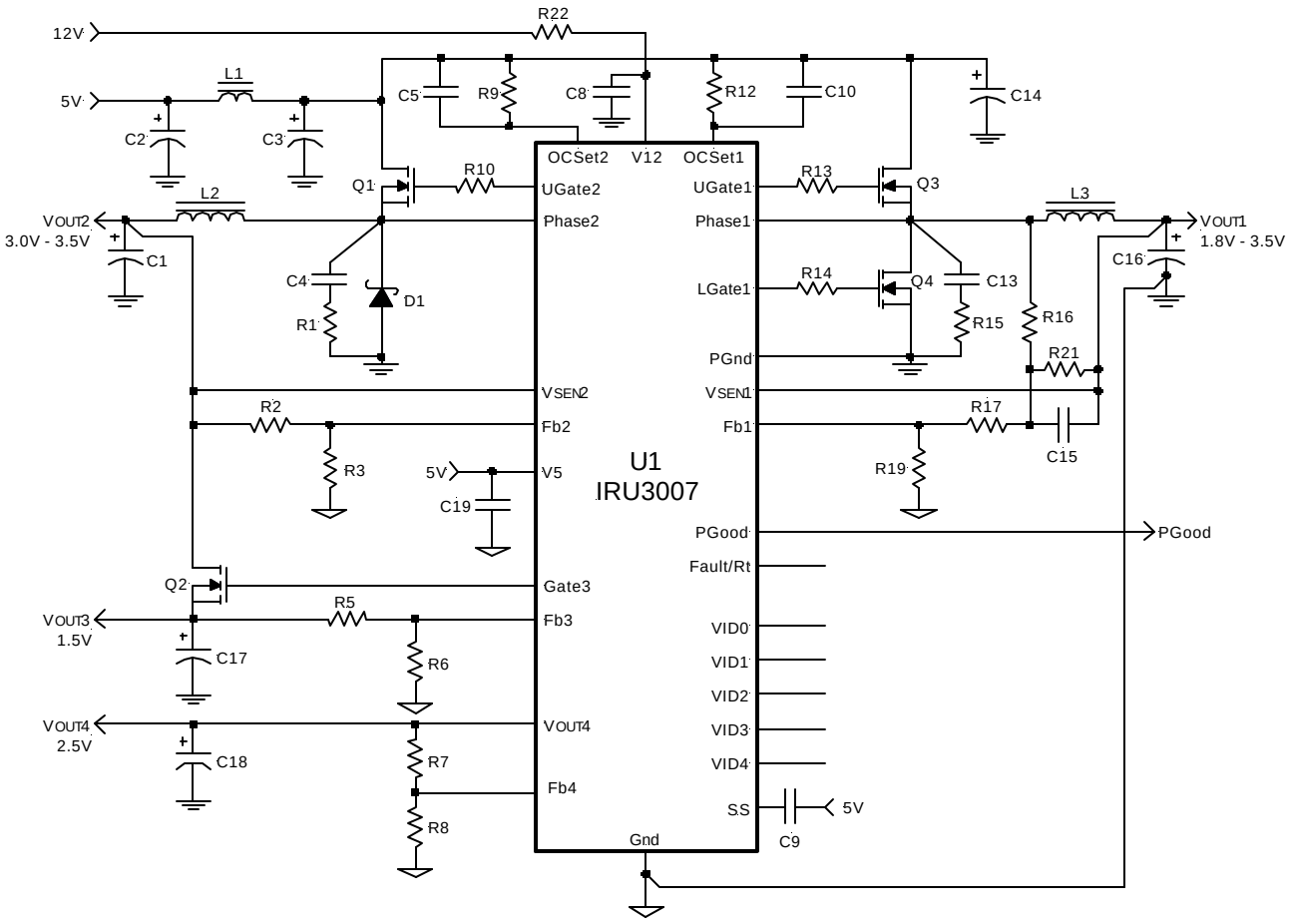


Figure 3 - Typical application of IRU3007 for an on-board DC-DC converter providing power for the Vcore, GTL+, Clock supply as well as an on-board 3.3V I/O supply for the Deschutes and the next generation processor applications.

IRU3007 APPLICATION PARTS LIST

Ref Desig	Description	Qty	Part #	Manuf
Q1	MOSFET	1	IRL3103S, TO-263 package	IR
Q2	MOSFET	1	IRLR024, TO-252 package	IR
Q3	MOSFET	1	IRL3103S, TO-263 package	IR
Q4	MOSFET with Schottky	1	IRL3103D1S, TO-263 package	IR
D1	Diode	1	MBRB1035, TO-263 package	IR
L1	Inductor	1	L=1μH, 5052 core with 4 turns of 1.0mm wire	Micro Metal
L2	Inductor	1	L=4.7μH, 5052 core with 11 turns of 1.0mm wire	Micro Metal
L3	Inductor	1	L=2.7μH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1	Capacitor, Electrolytic	2	6MV1500GX, 1500μF, 6.3V	Sanyo
C2	Capacitor, Electrolytic	1	10MV470GX, 470μF, 10V	Sanyo
C3	Capacitor, Electrolytic	1	10MV1200GX, 1200μF, 10V	Sanyo
C4, 13	Capacitor, Ceramic	2	1000pF, 0603	
C5, 10	Capacitor, Ceramic	2	220pF, 0603	
C8	Capacitor, Ceramic	1	1μF, 0805	
C9, 15, 19	Capacitor, Ceramic	3	1μF, 0603	
C14	Capacitor, Electrolytic	2	10MV1200GX, 1200μF, 10V	Sanyo
C16	Capacitor, Electrolytic	6	6MV1500GX, 1500μF, 6.3V	Sanyo
C17	Capacitor, Electrolytic	1	6MV1000GX, 1000μF, 6.3V	Sanyo
C18	Capacitor, Electrolytic	1	6MV150GX, 150μF, 6.3V	Sanyo
R1, 5, 13, 14	Resistor	4	4.7Ω, 5%, 1206	
R2	Resistor	1	75Ω, 1%, 0603	
R3, 6, 7, 8	Resistor	4	100Ω, 1%, 0603	
R5	Resistor	1	19.1Ω, 1%, 0603	
R9	Resistor	1	1.5KΩ, 5%, 0603	
R10	Resistor	1	10Ω, 5%, 1206	
R12	Resistor	1	3.3KΩ, 5%, 0603	
R16, 17, 21	Resistor	3	2.2KΩ, 1%, 0603	
R19	Resistor	1	220KΩ, 1%, 0603	
R22	Resistor	1	10Ω, 5%, 0603	

TYPICAL APPLICATION

(Dual Layout with HIP6019)

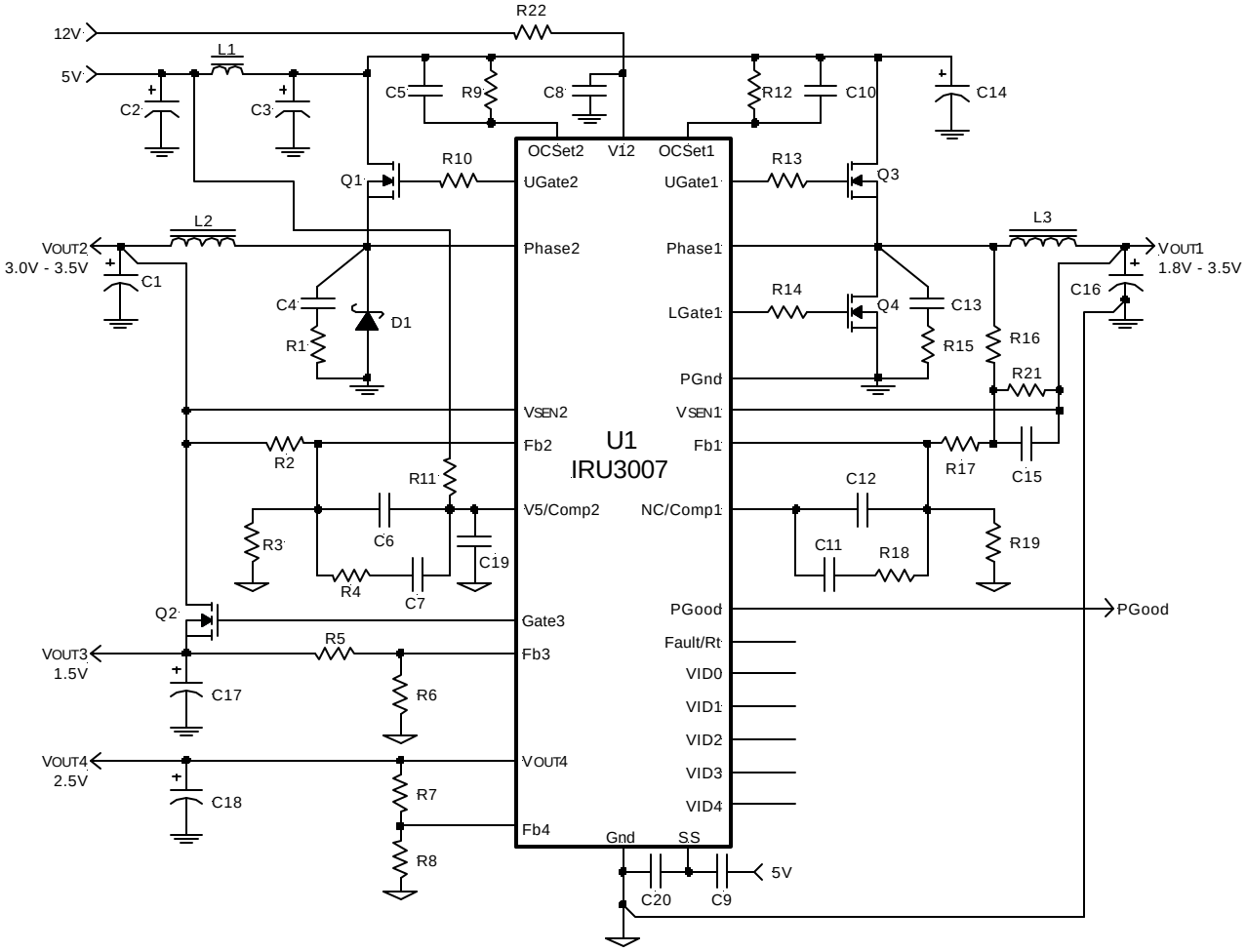


Figure 4 - Typical application of IRU3007 in a dual layout with HIP6019 for an on-board DC-DC converter providing power for the Vcore, GTL+, Clock supply as well as an on-board 3.3V I/O supply for the Deschutes and the next generation processor application.

Components that need to be modified to make the dual layout work for HIP6019 and IRU3007:

Part #	R4	R11	R18	C6	C7	C9	C11	C12	C19	C20
HIP6019	V	O	V	V	V	O	V	V	O	V
IRU3007	O	S	O	O	O	V	O	O	V	O

S - Short O - Open V - See IR or Harris parts list for the value

Table 2 - Dual layout component table.

IRU3007 APPLICATION PARTS LIST

Dual Layout with HIP6019

Ref Desig	Description	Qty	Part #	Manuf
Q1	MOSFET	1	IRL3103S, TO-263 package	IR
Q2	MOSFET	1	IRLR024, TO-252 package	IR
Q3	MOSFET	1	IRL3103S, TO-263 package	IR
Q4	MOSFET with Schottky	1	IRL3103D1S, TO-263 package	IR
D1	Diode	1	MBRB1035, TO-263 package	IR
L1	Inductor	1	L=1μH, 5052 core with 4 turns of 1.0 mm wire	Micro Metal
L2	Inductor	1	L=4.7μH, 5052 core with 11 turns of 1.0mm wire	Micro Metal
L3	Inductor	1	L=2.7μH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1	Capacitor, Electrolytic	2	6MV1500GX, 1500μF, 6.3V	Sanyo
C2	Capacitor, Electrolytic	1	10MV470GX, 470μF, 10V	Sanyo
C3	Capacitor, Electrolytic	1	10MV1200GX, 1200μF, 10V	Sanyo
C4, 13	Capacitor, Ceramic	2	1000pF, 0603	
C5, 10	Capacitor, Ceramic	2	220pF, 0603	
C6,7,11,12 20	Capacitor, Ceramic	5	See Table 2, dual layout component 0603 × 5	
C8	Capacitor, Ceramic	1	1μF, 0805	
C9,15,19	Capacitor, Ceramic	3	1μF, 0603	
C14	Capacitor, Electrolytic	2	10MV1200GX, 1200μF, 10V	Sanyo
C16	Capacitor, Electrolytic	6	6MV1500GX, 1500μF, 6.3V	Sanyo
C17	Capacitor, Electrolytic	1	6MV1000GX, 1000μF, 6.3V	Sanyo
C18	Capacitor, Electrolytic	1	6MV150GX, 150μF, 6.3V	Sanyo
R1,13,14 15	Resistor	4	4.7Ω, 5%, 1206	
R2	Resistor	1	75Ω, 1%, 0603	
R3,6,7,8	Resistor	4	100Ω, 1%, 0603	
R4, 18	Resistor	2	See Table 2, dual layout component 0603 × 2	
R5	Resistor	1	19.1Ω, 1%, 0603	
R9	Resistor	1	1.5KΩ, 5%, 0603	
R10	Resistor	1	10Ω, 5%, 1206	
R11	Resistor	1	0Ω, 0603	
R12	Resistor	1	3.3KΩ, 5%, 0603	
R16,17,21	Resistor	3	2.2KΩ, 1%, 0603	
R19	Resistor	1	220KΩ, 1%, 0603	
R22	Resistor	1	10Ω, 5%, 0603	

APPLICATION INFORMATION

An example of how to calculate the components for the application circuit is given below.

Assuming, two set of output conditions that this regulator must meet for Vcore:

a) Vo=2.8V , Io=14.2A, ΔVo=185mV, ΔIo=14.2A

b) Vo=2V , Io=14.2A, ΔVo=140mV, ΔIo=14.2A

Also, the on-board 3.3V supply must be able to provide 10A load current and maintain less than ±5% total output voltage variation.

The regulator design will be done such that it meets the worst case requirement of each condition.

Output Capacitor Selection

Vcore

The first step is to select the output capacitor. This is done primarily by selecting the maximum ESR value that meets the transient voltage budget of the total ΔVo specification. Assuming that the regulators DC initial accuracy plus the output ripple is 2% of the output voltage, then the maximum ESR of the output capacitor is calculated as:

$$ESR \leq \frac{100}{14.2} = 7m\Omega$$

The Sanyo MVGX series is a good choice to achieve both the price and performance goals. The 6MV1500GX, 1500μF, 6.3V has an ESR of less than 36mΩ typical. Selecting 6 of these capacitors in parallel has an ESR of ≈ 6mΩ which achieves our low ESR goal.

Other type of Electrolytic capacitors from other manufacturers to consider are the Panasonic FA series or the Nichicon PL series.

3.3V supply

For the 3.3V supply, since there is not a fast transient requirement, 2 of the 1500μF capacitors is sufficient.

Reducing the Output Capacitors Using Voltage Level Shifting Technique

The trace resistance or an external resistor from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transitioning from light load to full load and vice versa. To accomplish this, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the IRU3007 is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting. This intentional voltage level shifting during the load transient eases the requirement for the output capacitor ESR at the cost of load regulation. One can show that the new ESR requirement eases up by half the total trace resistance. For example, if the ESR requirement of the output capacitors without voltage level shifting must be 7mΩ then after level shifting the new ESR will only need to be 8.5mΩ if the trace resistance is 5mΩ (7+5/2=9.5). However, one must be careful that the combined "voltage level shifting" and the transient response is still within the maximum tolerance of the Intel specification. To insure this, the maximum trace resistance must be less than:

$$Rs \leq 2 \times \frac{(Vspec - 0.02 \times Vo - \Delta Vo)}{\Delta I}$$

Where :

Rs = Total maximum trace resistance allowed

Vspec = Intel total voltage spec

Vo = Output voltage

ΔVo = Output ripple voltage

ΔI = load current step

For example, assuming:

Vspec = ±140mV = ±0.1V for 2V output

Vo = 2V

ΔVo = assume 10mV = 0.01V

ΔI = 14.2A

Then the Rs is calculated to be:

$$Rs \leq 2 \times \frac{(0.140 - 0.02 \times 2 - 0.01)}{14.2} = 12.6m\Omega$$

However, if a resistor of this value is used, the maximum power dissipated in the trace (or if an external resistor is being used) must also be considered. For example if Rs=12.6mΩ, the power dissipated is:

$$Io^2 \times Rs = 14.2^2 \times 12.6 = 2.54W$$

This is a lot of power to be dissipated in a system. So, if the Rs=5mΩ, then the power dissipated is about 1W, which is much more acceptable. If level shifting is not implemented, then the maximum output capacitor ESR was shown previously to be 7mΩ which translated to ≈ 6

of the 1500μF, 6MV1500GX type Sanyo capacitors. With Rs=5mΩ, the maximum ESR becomes 9.5mΩ which is equivalent to ≈ 4 caps. Another important consideration is that if a trace is being used to implement the resistor, the power dissipated by the trace increases the case temperature of the output capacitors which could seriously affect the life span of the output capacitors.

Output Inductor Selection

The output inductance must be selected such that under low line and the maximum output voltage condition, the inductor current slope times the output capacitor ESR is ramping up faster than the capacitor voltage is drooping during a load current step. However, if the inductor is made too small, the output ripple current and ripple voltage will become too large. One solution to bring the ripple current down is to increase the switching frequency, however that will be at the cost of reduced efficiency and higher system cost. The following set of formulas are derived to achieve optimum performance without many design iterations.

The maximum output inductance is calculated using the following equation:

$$L = ESR \times C \times \frac{(V_{IN(MIN)} - Vo_{(MAX)})}{(2 \times \Delta I)}$$

Where:

$V_{IN(MIN)}$ = Minimum input voltage

For Vo = 2.8V and ΔI = 14.2A, we get:

$$L = 0.006 \times 9000 \times \frac{(4.75 - 2.8)}{(2 \times 14.2)} = 3.7\mu H$$

Assuming that the programmed switching frequency is set at 200KHz, an inductor is designed using the Micrometals' powder iron core material. The summary of the design is outlined below:

The selected core material is Powder Iron, the selected core is T50-52D from Micro Metal wound with 8 turns of #16 AWG wire, resulting in 3μH inductance with ≈ 3 mΩ of DC resistance.

Assuming L=3μH and Fsw=200KHz (switching frequency), the inductor ripple current and the output ripple voltage is calculated using the following set of equations:

T ≡ Switching Period
D ≡ Duty Cycle
Vsw ≡ High-side MOSFET ON Voltage
R_{DS} ≡ MOSFET On-Resistance
Vsync ≡ Synchronous MOSFET ON Voltage
ΔIr ≡ Inductor Ripple Current
ΔVo ≡Output Ripple Voltage

$T = 1 / Fsw$

$Vsw = Vsync = Io \times R_{DS}$

$D \approx (Vo + Vsync) / (V_{IN} - Vsw + Vsync)$

$T_{ON} = D \times T$

$T_{OFF} = T - T_{ON}$

$\Delta Ir = (Vo + Vsync) \times T_{OFF} / L$

$\Delta Vo = \Delta Ir \times ESR$

In our example for Vo = 2.8V and 14.2 A load, assuming IRL3103 MOSFET for both switches with maximum on resistance of 19mΩ, we have:

$T = 1 / 200000 = 5\mu s$

$Vsw = Vsync = 14.2 \times 0.019 = 0.27V$

$D \approx (2.8 + 0.27) / (5 - 0.27 + 0.27) = 0.61$

$T_{ON} = 0.61 \times 5 = 3.1\mu s$

$T_{OFF} = 5 - 3.1 = 1.9\mu s$

$\Delta Ir = (2.8 + 0.27) \times 1.9 / 3 = 1.94A$

$\Delta Vo = 1.94 \times 0.006 = 0.011V = 11mV$

Power Component Selection

Vcore

Assuming IRL3103 MOSFETs as power components, we will calculate the maximum power dissipation as follows:

For high side switch the maximum power dissipation happens at maximum Vo and maximum duty cycle.

$D_{MAX} \approx (2.8 + 0.27) / (4.75 - 0.27 + 0.27) = 0.65$

$P_{DH} = D_{MAX} \times Io^2 \times R_{DS(MAX)}$

$P_{DH} = 0.65 \times 14.2^2 \times 0.029 = 3.8W$

$R_{DS(MAX)}$=Maximum $R_{DS(ON)}$ of the MOSFET at 125°C

For synch MOSFET, maximum power dissipation happens at minimum Vo and minimum duty cycle.

$D_{MIN} \approx (2 + 0.27) / (5.25 - 0.27 + 0.27) = 0.43$

$P_{DS} = (1 - D_{MIN}) \times Io^2 \times R_{DS(MAX)}$

$P_{DS} = (1 - 0.43) \times 14.2^2 \times 0.029 = 3.33W$

3.3V Supply

Again, for high side switch the maximum power dissipation happens at maximum Vo and maximum duty cycle. The duty cycle equation for non synchronous replaces the forward voltage of the diode with the Synch MOSFET on voltage. In equations below:

Vf = 0.5V

$D_{MAX} \approx (3.3 + 0.5) / (4.75 - 0.27 + 0.5) = 0.76$

$P_{DH} = D_{MAX} \times Io^2 \times R_{DS(MAX)}$

$P_{DH} = 0.76 \times 10^2 \times 0.029 = 2.21W$

$R_{DS(MAX)}$ = Maximum $R_{DS(ON)}$ of the MOSFET at 125°C

For diode, the maximum power dissipation happens at minimum Vo and minimum duty cycle.

$D_{MIN} \approx (3.3 + 0.5) / (5.25 - 0.27 + 0.5) = 0.69$

$P_{DD} = (1 - D_{MIN}) \times Io \times Vf$

$P_{DD} = (1 - 0.69) \times 10 \times 0.5 = 1.55W$

Switcher Current Limit Protection

The IRU3007 uses the MOSFET $R_{DS(ON)}$ as the sensing resistor to sense the MOSFET current and compares to a programmed voltage which is set externally via a resistor (Rcs) placed between the drain of the MOSFET and the "CS+" terminal of the IC as shown in the application circuit.

For example, if the desired current limit point is set to be 22A for the synchronous and 16A for the non synchronous, and from our previous selection, the maximum MOSFET $R_{DS(ON)}$=19mW, then the current sense resistor Rcs is calculated as:

Vcore

$Vcs = I_{CL} \times R_{DS} = 22 \times 0.019 = 0.418V$

$Rcs = Vcs / I_B = (0.418V) / (200\mu A) = 2.1K\Omega$

Where:
I_B=200μA is the internal current setting of the IRU3007

3.3V supply

$Vcs = I_{CL} \times R_{DS} = 16 \times 0.019 = 0.3V$

$Rcs = Vcs / I_B = (0.3V) / (200\mu A) = 1.50K\Omega$

1.5V, GTL+ Supply LDO Power MOSFET Selection

The first step in selecting the power MOSFET for the 1.5V linear regulator is to select its maximum $R_{DS(ON)}$ of the pass transistor based on the input to output Dropout voltage and the maximum load current.

For Vo = 1.5V, V_{IN} = 3.3V and I_L = 2A:

$R_{DS(MAX)} = (V_{IN} - Vo) / I_L = (3.3 - 1.5) / 2 = 0.9\Omega$

Note: Since the MOSFETs $R_{DS(ON)}$ increases with temperature, this number must be divided by ≈ 1.5, in order to find the $R_{DS(ON)}$ max at room temperature. The Motorola MTP3055VL has a maximum of 0.18Ω $R_{DS(ON)}$ at room temperature, which meets our requirement.

To select the heat sink for the LDO MOSFET the first step is to calculate the maximum power dissipation of the device and then follow the same procedure as for the switcher.

Where:
P_D = Power Dissipation of the Linear Regulator
I_L = Linear Regulator Load Current

For the 1.5V and 2A load:

$P_D = (V_{IN} - Vo) \times I_L$

$P_D = (3.3 - 1.5) \times 2 = 3.6W$

Assuming $T_{J(MAX)}$ = 125°C:

$Ts = T_J - P_D \times (\theta_{JC} + \theta cs)$

$Ts = 125 - 3.6 \times (1.8 + 0.05) = 118°C$

With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated as follows:

Assuming T_A = 35°C:

$\Delta T = Ts - T_A = 118 - 35 = 83°C$
Temperature Rise Above Ambient

$\theta_{SA} = \Delta T / P_D = 83 / 3.6 = 23°C/W$

The same heat sink as the one selected for the switcher MOSFETs is also suitable for the 1.5V regulator.

2.5V Clock Supply

The IRU3007 provides a complete 2.5V regulator with a minimum of 200mA current capability. The internal regulator has short circuit protection with internal thermal shutdown.

1.5V and 2.5V Supply Resistor Divider Selection

Since the internal voltage reference for the linear regulators is set at 1.26V for IRU3007, there is a need to use external resistor dividers to step up the voltage. The resistor dividers are selected using the following equations:

$Vo = (1 + Rt / R_B) \times V_{REF}$

Where:
Rt = Top resistor divider
R_B = Bottom resistor divider
V_{REF} = 1.26V typical

For 1.5V supply
Assuming R_B = 1KΩ:

$Rt = R_B \times [(Vo / V_{REF}) - 1]$

$Rt = 1 \times [(1.5 / 1.26) - 1] = 191\Omega$

For 2.5V supply

Assuming R_B = 1.02KΩ:

$$Rt = R_B \times [(Vo / V_{REF}) - 1]$$

$$Rt = 1.02 \times [(2.5 / 1.26) - 1] = 1K\Omega$$

Switcher Output Voltage Adjust

Vcore

As it was discussed earlier, the trace resistance from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transitioning from light load to full load and vice versa. To account for the DC drop, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the IRU3007 is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting. To do this, the top resistor of the resistor divider (R12 in the application circuit) is set at 100Ω, and the R19 is calculated. For example, if DAC voltage setting is for 2.8V and the desired output under light load is 2.835V, then R19 is calculated using the following formula:

$$R19 = 100 \times [V_{DAC} / (Vo - 1.004 \times V_{DAC})] \quad (\Omega)$$

$$R19 = 100 \times [2.8 / (2.835 - 1.004 \times 2.800)] = 11.76K\Omega$$

Select 11.8KΩ, 1%

Note: The value of the top resistor must not exceed 100Ω**.** The bottom resistor can then be adjusted to raise the output voltage.

3.3V supply

The loop gain for the non-synchronous switching regulator is intentionally set low to take advantage of the level shifting technique to reduce the number of output capacitors. Typically there is a 1% drop in the output voltage from light load (discontinuous conduction mode) to full load (continuous conduction mode) in the 3.3V supply. To account for this, the output voltage is set at 3.5V typically. The same procedure as for the synchronous is applied to the non-synch with the exception that the internal voltage reference of this regulator is internally set at 2V. The following is the set of equations to use for the output voltage setting for the non-synchronous assuming the Vo=3.5V and R2=75Ω (R2 is the top resistor in the application circuit).

The bottom resistor, R3 is calculated as follows:

$$R3 = R2 \times [2 / (Vo - 2)] \quad (\Omega)$$

$$R3 = 75 \times [2 / (3.5 - 2)] = 100\Omega, 1\%$$

Note: The value of the top resistor, R2 must not exceed 100Ω**.**

Soft-Start Capacitor Selection

The soft-start capacitor must be selected such that during the start up when the output capacitors are charging up, the peak inductor current does not reach the current limit threshold. A minimum of 1μF capacitor insures this for most applications. An internal 10μA current source charges the soft-start capacitor which slowly ramps up the inverting input of the PWM comparator Vfb3. This insures the output voltage to ramp at the same rate as the soft-start cap thereby limiting the input current. For example, with 1μF and the 10μA internal current source the ramp up rate is (ΔV/Δt)=I/C=1V/100ms. Assuming that the output capacitance is 9000μF, the maximum start up current will be:

$$I = 9000\mu F \times (1V / 100ms) = 0.09A$$

Input Filter

It is highly recommended to place an inductor between the system 5V supply and the input capacitors of the switching regulator to isolate the 5V supply from the switching noise that occurs during the turn on and off of the switching components. Typically an inductor in the range of 1 to 3μH will be sufficient in this type of application.

External Shutdown

The best way to shutdown the IRU3007 is to pull down on the soft-start pin using an external small signal transistor such as 2N3904 or 2N7002 small signal MOSFET. This allows slow ramp up of the output, the same as the power up.

Layout Considerations

Switching regulators require careful attention to the layout of the components, specifically power components since they switch large currents. These switching components can create large amount of voltage spikes and high frequency harmonics if some of the critical components are far away from each other and are connected with inductive traces. The following is a guideline of how to place the critical components and the connections between them in order to minimize the above issues.

Start the layout by first placing the power components:

1) Place the input capacitors C3 and C14 and the high side MOSFETs, Q1 and Q3 as close to their respective input caps as possible.

2) Place the synchronous MOSFET, Q2 and the Q3 as close to each other as possible with the intention that the source of Q3 and drain of the Q4 has the shortest length. Repeat this for the Q1 and D1 for the non-synchronous.

3) Place the snubber R15 and C13 between Q4 and Q3. Repeat this for R1 and C4 with respect to the Q1 and D1 for the non-synchronous.

4) Place the output inductor , L3 and the output capacitors, C16 between the MOSFET and the load with output capacitors distributed along the slot 1 and close to it. Repeat this for L2 with respect to the C1 for the non-synchronous.

5) Place the bypass capacitors, C8 and C19 right next to 12V and 5V pins. C8 next to the 12V, pin 28 and C19 next to the 5V, pin 11.

6) Place the IRU3007 such that the pwm output drives, pins 27 and 25 are relatively short distance from gates of Q3 and Q4. The non-synch MOSFET must also be situated such that the distance from its gate to the pin 1 of the IRU3007 is also relatively short.

7) Place all resistor dividers close to their respective feedback pins.

8) Place the 2.5V output capacitor, C18 close to the pin 16 of the IC and the 1.5V output capacitor, C17 close to the Q2 MOSFET.

   Note: It is better to place the 1.5V linear regulator components close to the IRU3007 and then run a trace from the output of the regulator to the load. However, if this is not possible then the trace from the linear drive output pin, pin 18 must be run away from any high frequency data signals.

   It is critical, to place high frequency ceramic capacitors close to the clock chip and termination resistors to provide local bypassing.

9) Place R12 and C10 close to pin 23 and R9 and C5 close to pin 9.

10) Place C9 close to pin 12

Component connections:

Note: It is extremely important that no data bus should be passing through the switching regulator section specifically close to the fast transition nodes such as PWM drives or the inductor voltage.

Using the 4 layer board, dedicate one layer to ground, another layer as the power layer for the 5V, 3.3V, Vcore, 1.5V and if it is possible, for the 2.5V.

Connect all grounds to the ground plane using direct vias to the ground plane.

Use large low inductance/low impedance plane to connect the following connections either using component side or the solder side.

a) C14 to Q3 Drain and C3 to Q1 drain
b) Q3 Source to Q4 Drain and Q1 Source to D1 cathode
c) Q4 drain to L3 and D1 cathode to L2
d) L3 to the output capacitors, C16 and L2 to the output capacitors, C1
e) C16 to the load, slot 1
f) Input filter L1 to the C16 and C3
g) C1 to Q2 drain
h) C17 to the Q2 source
I) A minimum of 0.2 inch width trace from the C18 capacitor to pin 16

Connect the rest of the components using the shortest connection possible.

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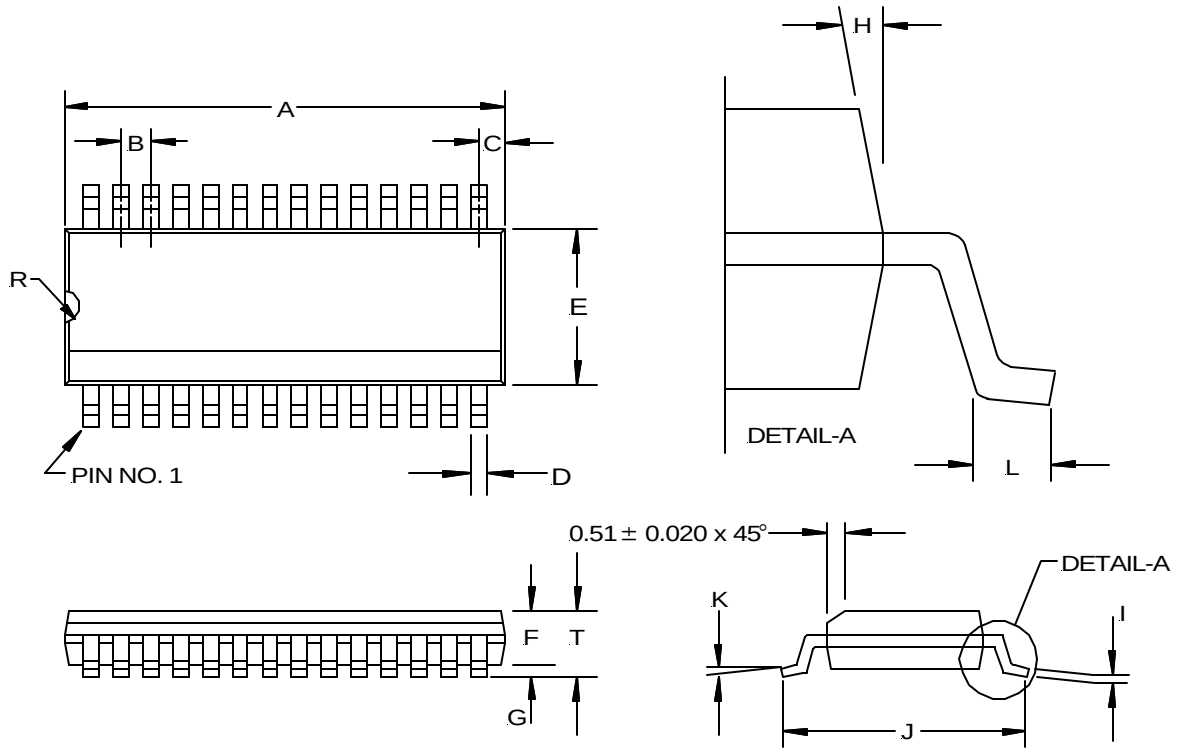
(W) SOIC Package
28-Pin Surface Mount, Wide Body

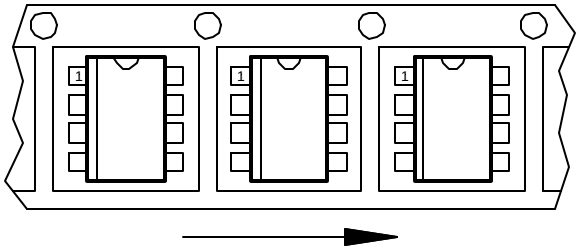


SYMBOL	28-PIN	
	MIN	MAX
A	17.73	17.93
B	1.27 BSC	
C	0.66 REF	
D	0.36	0.46
E	7.40	7.60
F	2.44	2.64
G	0.10	0.30
I	0.23	0.32
J	10.11	10.51
K	0°	8°
L	0.51	1.01
R	0.63	0.89
T	2.44	2.64

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
W	SOIC, Wide Body	28	27	1000	Fig A



Feed Direction
Figure A