

N-Channel 30V Fast Switching MOSFET

General Description

The QM3090M6 is the highest performance trench N-channel MOSFET with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The QM3090M6 meet the RoHS and Green Product requirement.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Green Device Available

Product Summary

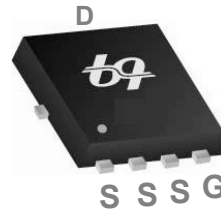
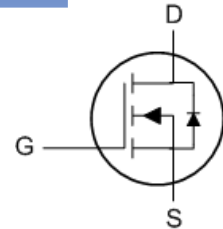


BVDSS	RDSON (VGS=10V)	ID (Tc=25°C)
30V	6.4mΩ	82A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

PRPAK5X6 Pin Configuration



Absolute Maximum Ratings(T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	82	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	52	A
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	13	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	11	A
I _{DM}	Pulsed Drain Current ²	164	A
EAS	Single Pulse Avalanche Energy ³	79.6	mJ
I _{AS}	Avalanche Current	39.9	A
P _D @T _C =25°C	Total Power Dissipation ⁴	73	W
P _D @T _A =25°C	Total Power Dissipation ⁴	2	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	62	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	1.7	°C/W

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Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	0.03	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=30A$	---	5.1	6.4	$m\Omega$
		$V_{GS}=4.5V$, $I_D=15A$	---	7.1	9.0	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.2	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.7	---	$mV/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=24V$, $V_{GS}=0V$	---	---	1	μA
		$V_{DS}=24V$, $V_{GS}=0V$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V$, $I_D=30A$	---	37	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1MHz$	---	1	---	Ω
Q_g	Total Gate Charge (10V)	$V_{DS}=15V$, $V_{GS}=10V$, $I_D=15A$	---	22.9	---	nC
Q_g	Total Gate Charge (4.5V)	$V_{DS}=15V$, $V_{GS}=4.5V$, $I_D=15A$	---	11.2	---	nC
Q_{gs}	Gate-Source Charge		---	4	---	
Q_{gd}	Gate-Drain Charge		---	4.3	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V$, $V_{GS}=10V$, $R_G=3.3\Omega$ $I_D=15A$	---	8.2	---	ns
T_r	Rise Time		---	41.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	29.2	---	
T_f	Fall Time		---	10.6	---	
C_{iss}	Input Capacitance	$V_{DS}=15V$, $V_{GS}=0V$, $f=1MHz$	---	1377	---	pF
C_{oss}	Output Capacitance		---	201	---	
C_{rss}	Reverse Transfer Capacitance		---	131	---	

Guaranteed Avalanche Characteristics($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	$V_{DD}=25V$, $L=0.1mH$, $I_{AS}=28A$	39.2	---	---	mJ

Diode Characteristics($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,6}	$V_G=V_D=0V$, Force Current	---	---	82	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	164	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=1A$	---	---	1.2	V
T_{rr}	Reverse Recovery Time	$IF=15A$, $di/dt=100A/\mu s$	---	10.2	---	nS
Q_{rr}	Reverse Recovery Charge		---	0.9	---	nC

Note :

1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V$, $V_{GS}=10V$, $L=0.1mH$.

4.The power dissipation is limited by 150°C junction temperature

5.The Min. value is 100% EAS tested guarantee.

6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

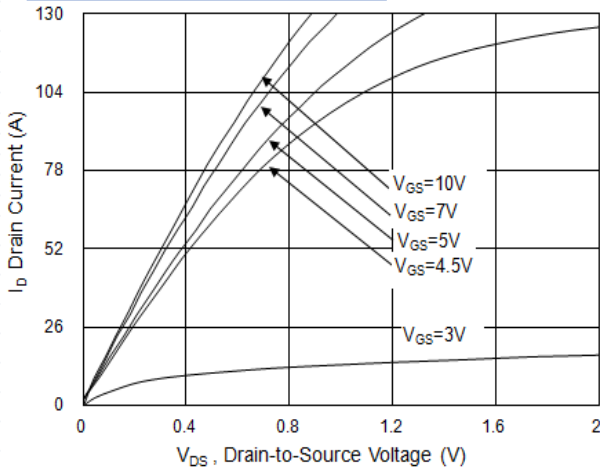


Fig.1 Typical Output Characteristics

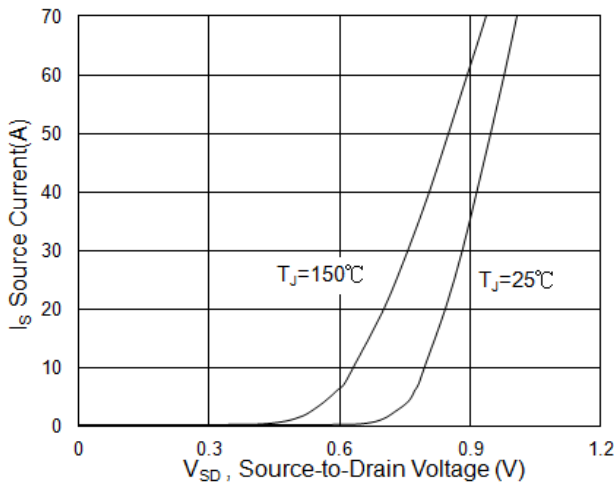


Fig.3 Forward Characteristics of Reverse

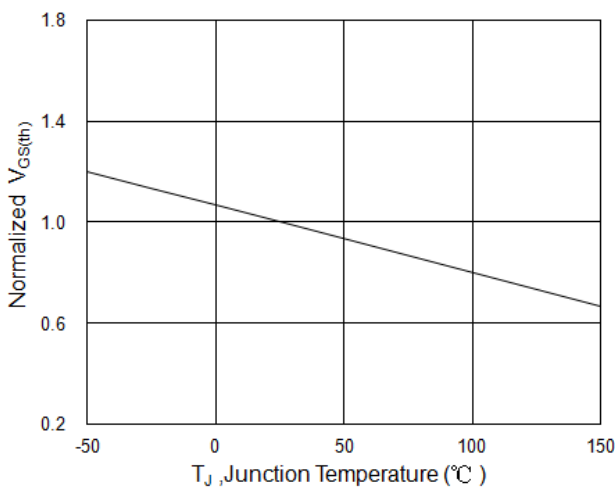


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

N-Channel 30V Fast Switching MOSFET

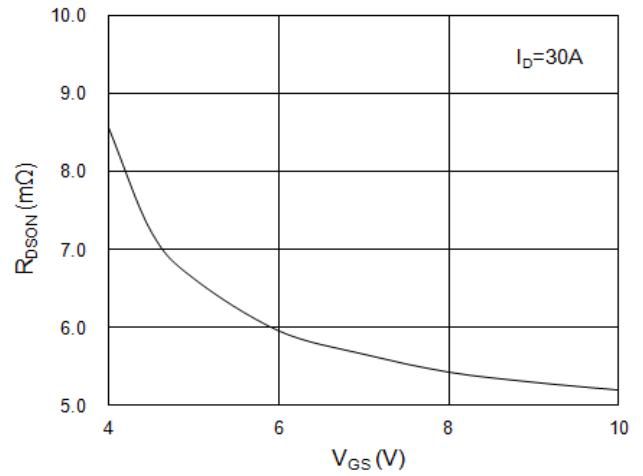


Fig.2 On-Resistance vs. Gate-Source

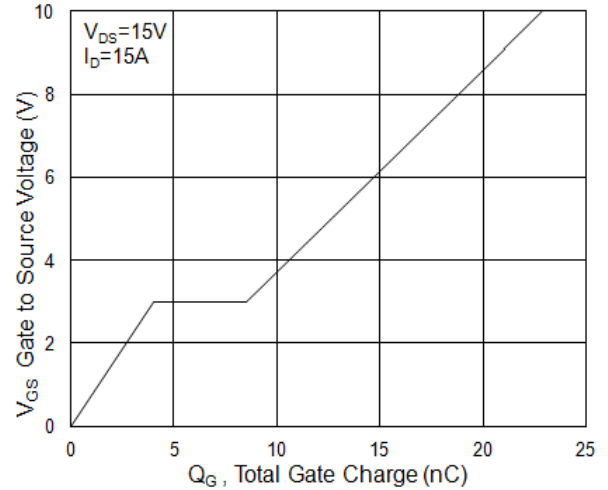


Fig.4 Gate-Charge Characteristics

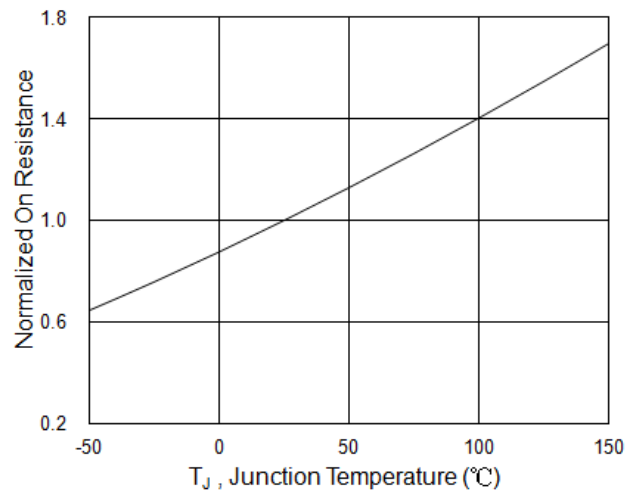


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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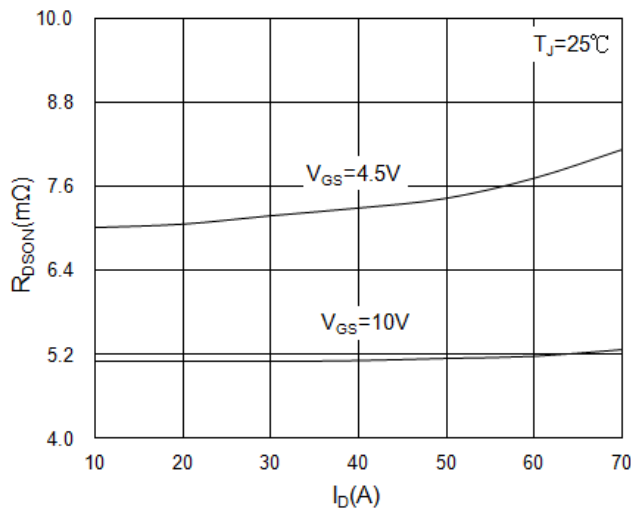


Fig.7 Drain-Source On-State Resistance

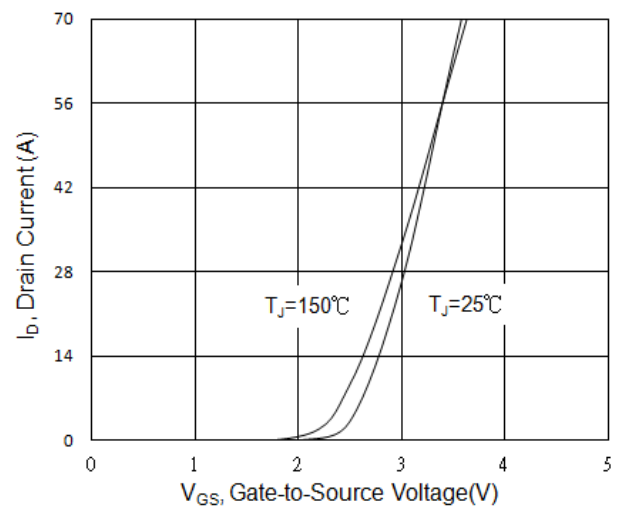


Fig.8 Transfer Characteristics

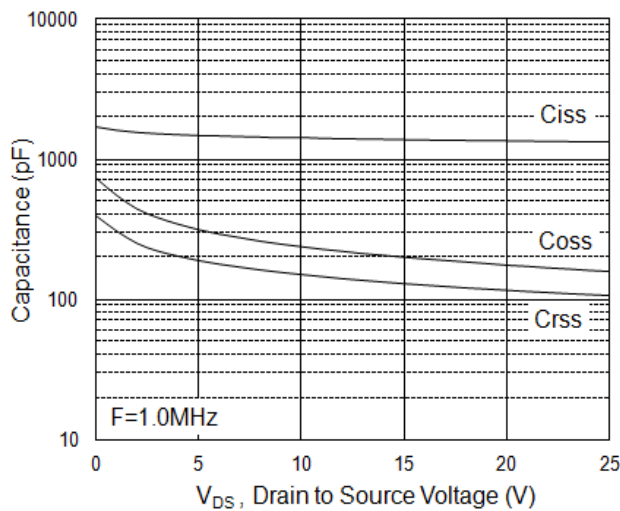


Fig.9 Capacitance

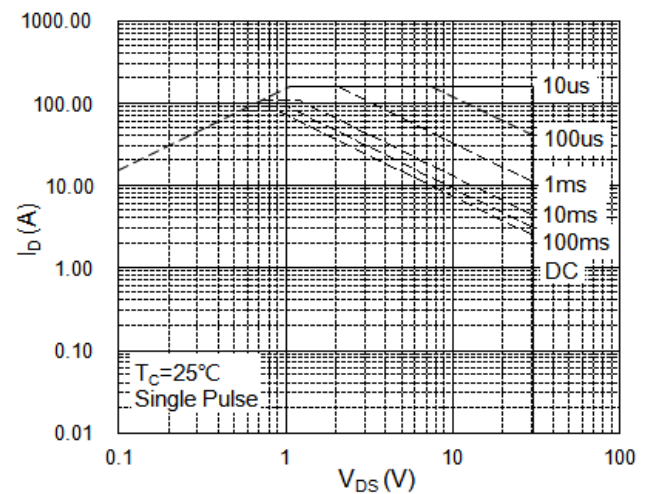


Fig.10 Safe Operating Area

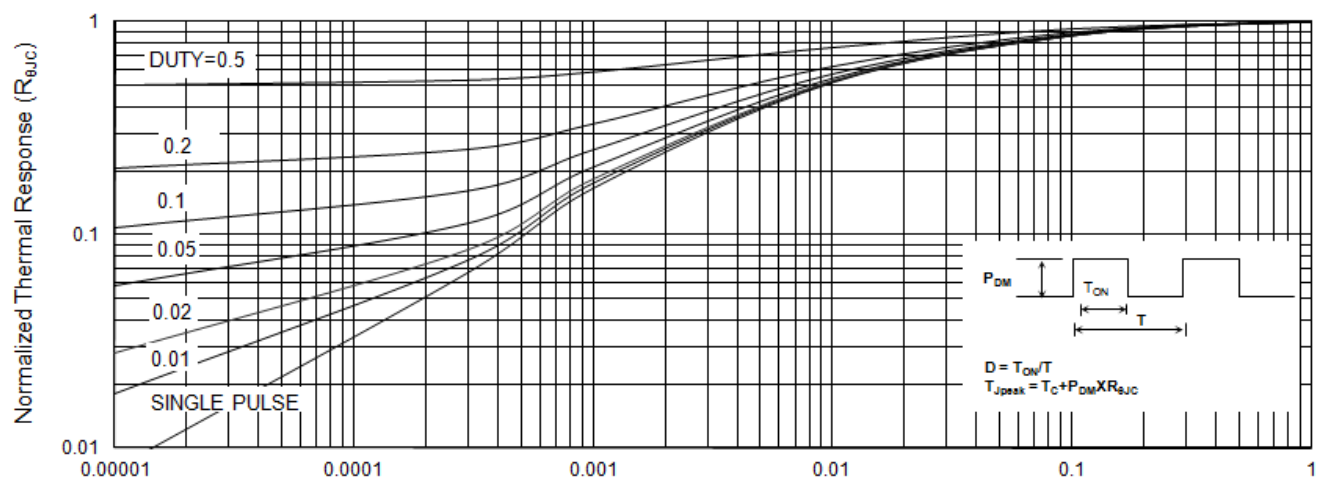
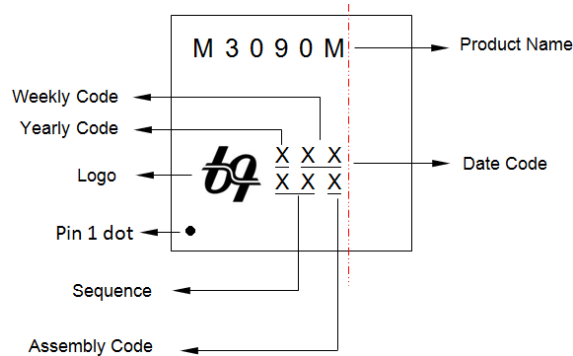
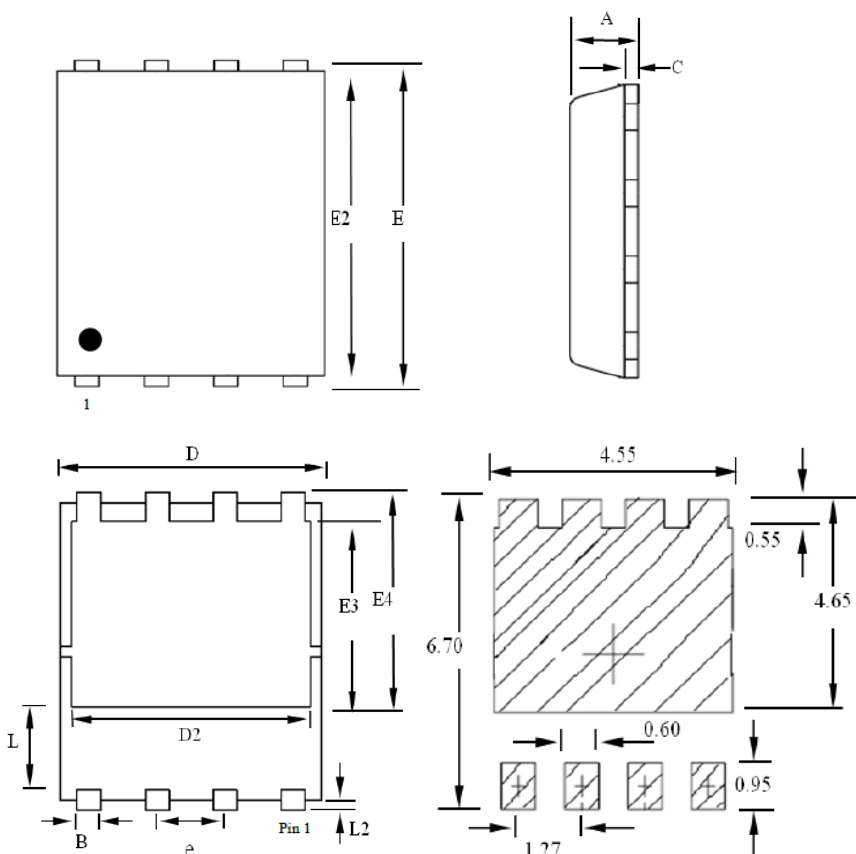


Fig.11 Normalized Maximum Transient Thermal Impedance

Top Marking



PRPAK5X6 Package Outline Drawing



LAND PATTERN RECOMMENDATION (Unit : mm)

SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.00	1.20
B	0.33	--	0.51
C	0.20	--	0.34
D	4.50	--	5.10
D2	3.60	--	4.22
E	5.90	--	6.13
E2	5.50	--	5.84
E3	3.18	--	4.30
E4	3.69	--	4.39
L	1.10	--	1.39
L2	0.02	--	0.33
e	--	1.27	--

Note:

1. ALL DIMENSIONS LISTED ON THE DRAWING MEETING JEDEC STANDARD.
2. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
3. RECOMMENDED LAND PATTERN DESIGN IS ONLY FOR REFERENCE