



# PSMN038-100YL

N-channel 100 V 37.5 mΩ logic level MOSFET in LFPACK56

1 May 2013

Product data sheet

## 1. General description

Logic level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in LFPACK56 package. This product has been designed and qualified for use in a wide range of industrial, communications and domestic equipment.

## 2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive
- LFPACK56 package is footprint compatible with other Power-SO8 types
- Qualified to 175 °C

## 3. Applications

- DC-to-DC converters
- Load switch
- TV power supplies

## 4. Quick reference data

Table 1. Quick reference data

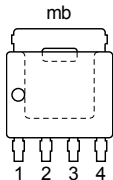
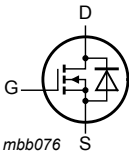
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	100	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	30	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	94.9	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 175\text{ °C}; \text{Fig. 13}; \text{Fig. 12}$	-	-	103.5	mΩ
		$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}; \text{Fig. 12}$	-	30.2	37.5	mΩ
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{GS} = 5\text{ V}; I_D = 5\text{ A}; V_{DS} = 80\text{ V}; T_j = 25\text{ °C}; \text{Fig. 14}; \text{Fig. 15}$	-	21.6	-	nC
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; V_{DS} = 80\text{ V}; T_j = 25\text{ °C}; \text{Fig. 14}; \text{Fig. 15}$	-	8.3	-	nC



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 30\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; unclamped; <a href="#">Fig. 3</a>	-	-	45.1	mJ

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LPAK56; Power-SO8 (SOT669)</b></p>	 <p><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN038-100YL	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN038-100YL	038100

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ }^\circ\text{C}$ ; $T_j \leq 175\text{ }^\circ\text{C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$T_{mb} = 25\text{ }^\circ\text{C}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 1</a>	-	30	A

N-channel 100 V 37.5 mΩ logic level MOSFET in LPAK56

Symbol	Parameter	Conditions	Min	Max	Unit
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V}; \text{Fig. 1}$	-	21.3	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}; \text{pulsed}; t_p \leq 10\text{ }\mu\text{s}; \text{Fig. 4}$	-	120	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	94.9	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	79	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$	-	120	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 30\text{ A}; V_{sup} \leq 100\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; \text{unclamped};$ <a href="#">Fig. 3</a>	-	45.1	mJ

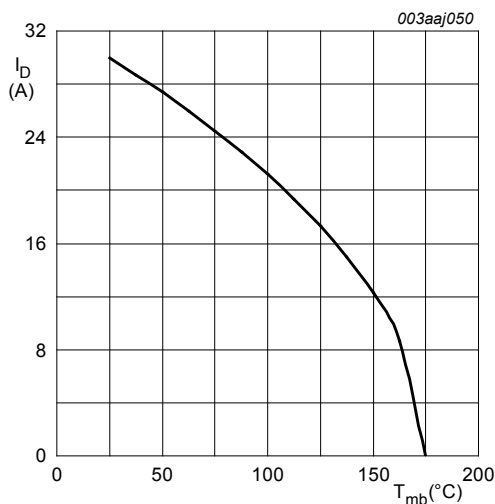


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

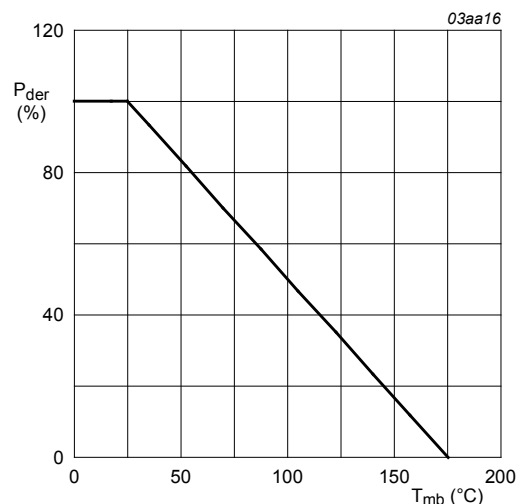


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ }^\circ\text{C})}} \times 100\%$$

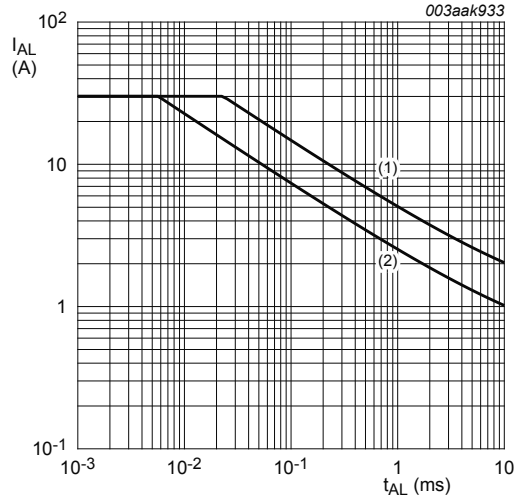


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j (init)} = 25^{\circ}C$ ; (2)  $T_{j (init)} = 100^{\circ}C$

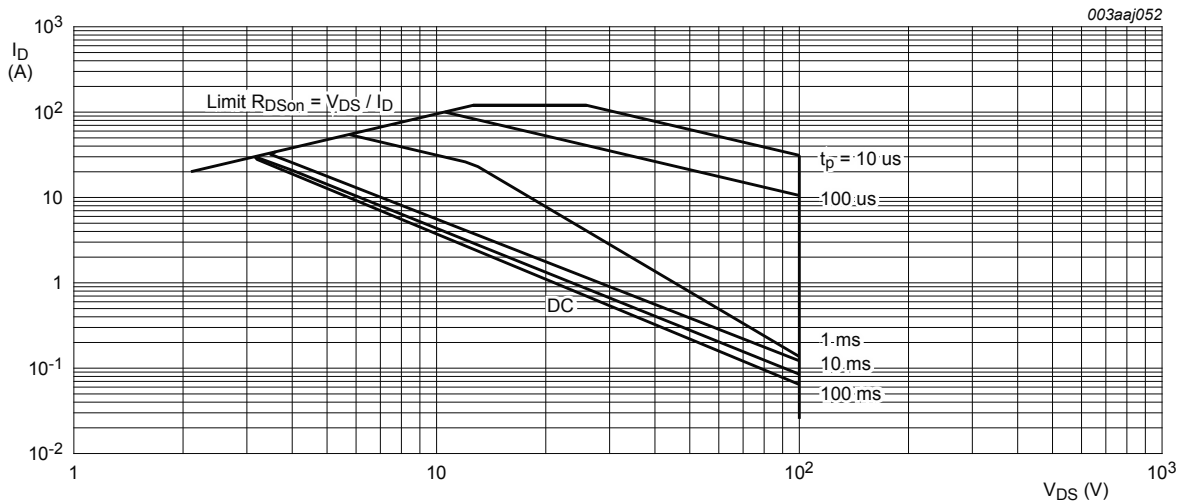


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	1.44	1.58	K/W

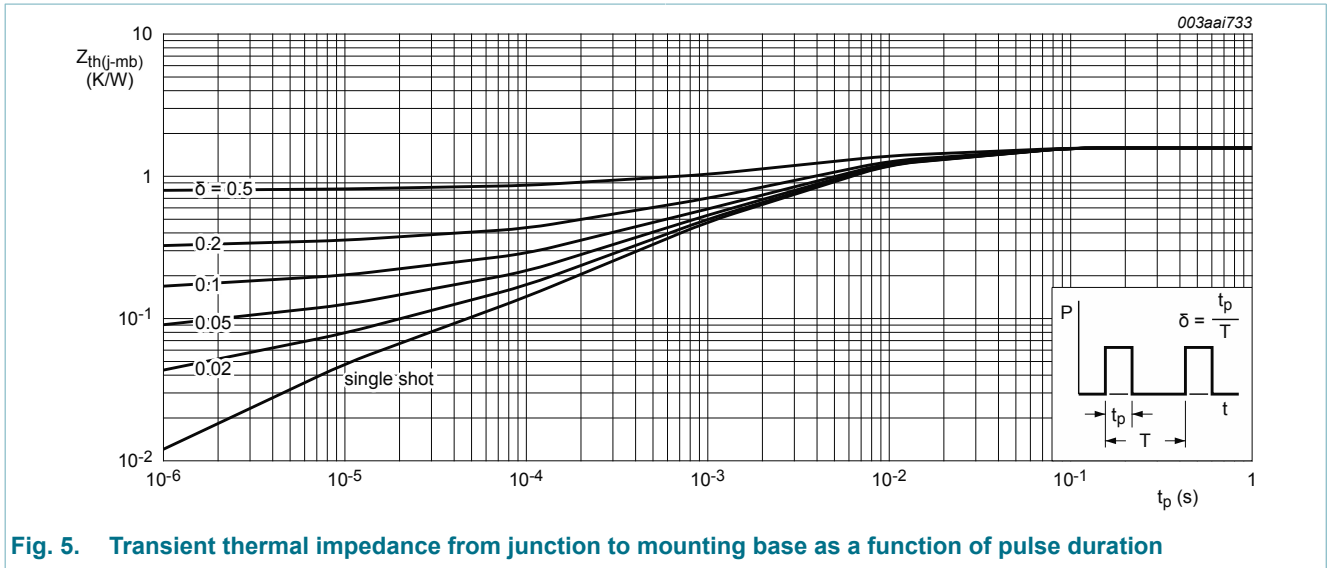


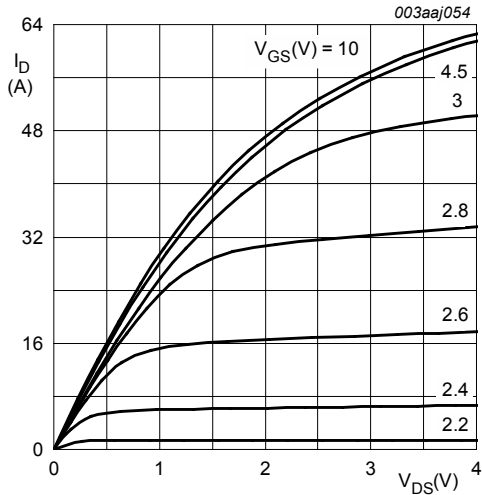
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

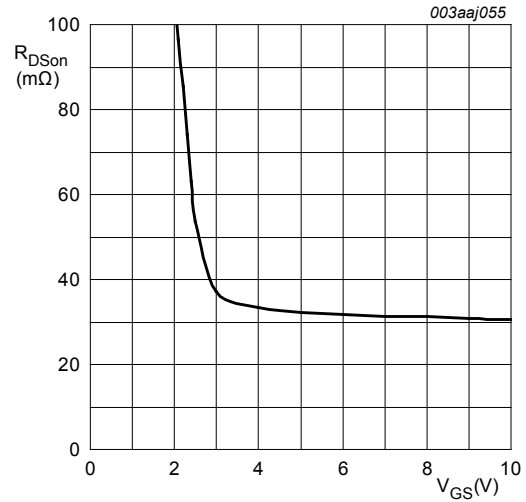
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.02	1	$\mu A$
		$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 V; I_D = 5 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	31.3	38	mΩ
		$V_{GS} = 10 V; I_D = 5 A; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 12</a>	-	-	103.5	mΩ
		$V_{GS} = 10 V; I_D = 5 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	30.2	37.5	mΩ
		$V_{GS} = 5 V; I_D = 5 A; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 12</a>	-	-	105	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1.64	-	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	39.2	-	nC
		I <sub>D</sub> = 5 A; V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 5 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	21.6	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	3.8	-	nC
Q <sub>GD</sub>	gate-drain charge		-	8.3	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge		-	2.7	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	1.1	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 80 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	2.3	-	V
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>	-	1905	-	pF
C <sub>oss</sub>	output capacitance		-	137	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	90	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 80 V; R <sub>L</sub> = 10 Ω; V <sub>GS</sub> = 5 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C	-	10	-	ns
t <sub>r</sub>	rise time		-	18	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	31	-	ns
t <sub>f</sub>	fall time		-	18	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 5 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 17</a>	-	0.78	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 10 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; T <sub>j</sub> = 25 °C	-	31	-	ns
Q <sub>r</sub>	recovered charge		-	44	-	nC



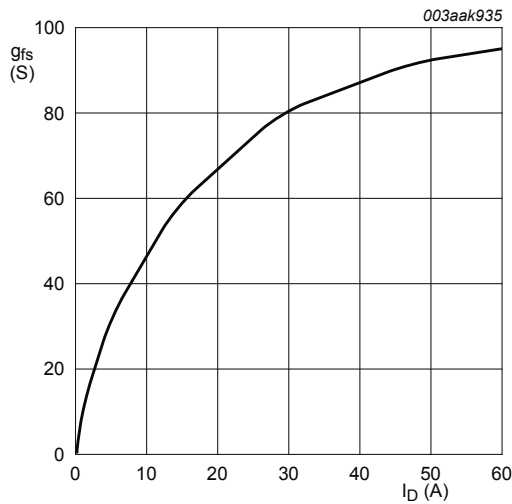
$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$

**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



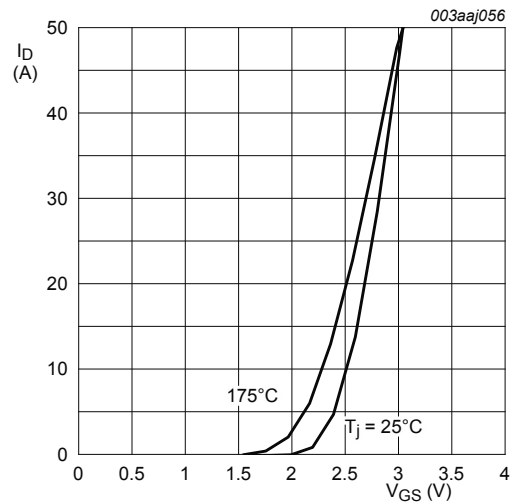
**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25^\circ\text{C}; I_D = 5\text{A}$



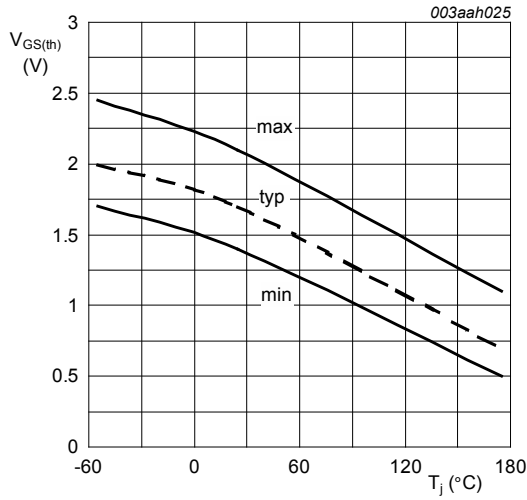
**Fig. 8. Forward transconductance as a function of drain current; typical values**

$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$



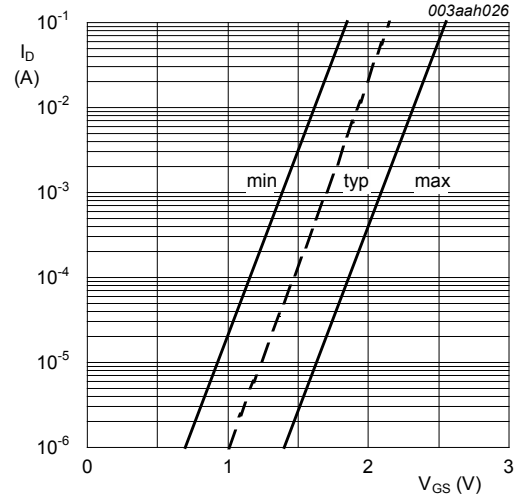
**Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10\text{V}$



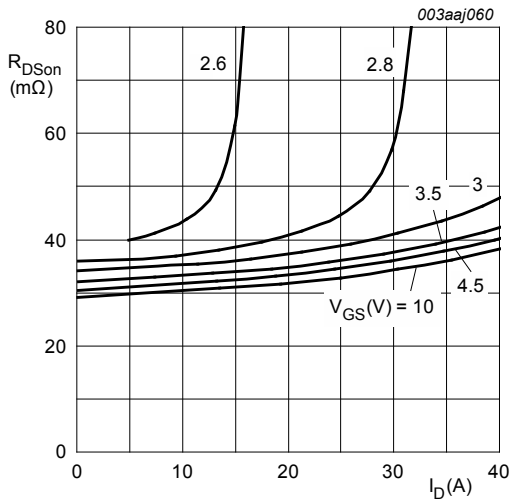
**Fig. 10. Gate-source threshold voltage as a function of junction temperature**

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$



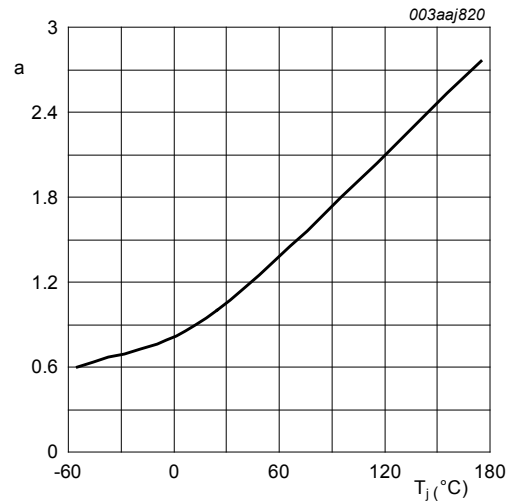
**Fig. 11. Sub-threshold drain current as a function of gate-source voltage**

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$



$$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$$

**Fig. 12. Drain-source on-state resistance as a function of drain current; typical values**



**Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$



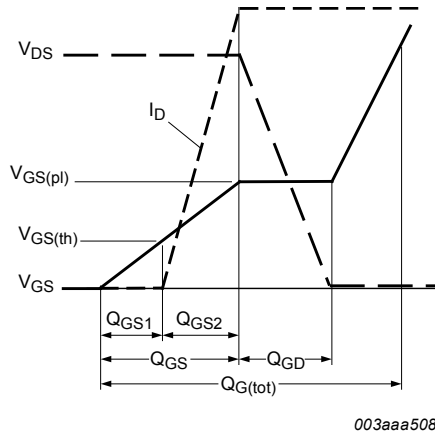


Fig. 14. Gate charge waveform definitions

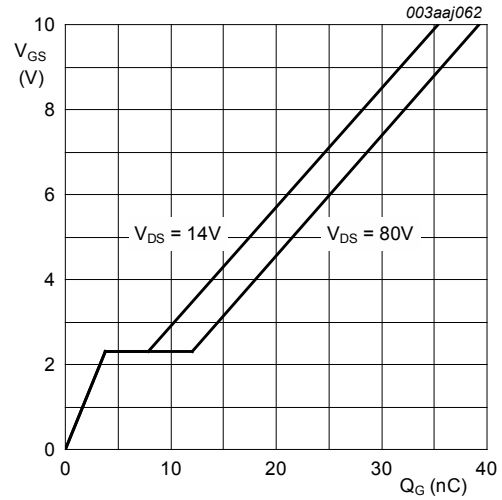


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ C; I_D = 5A$

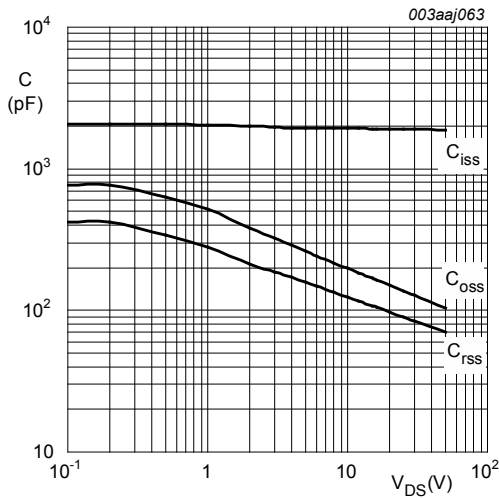


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

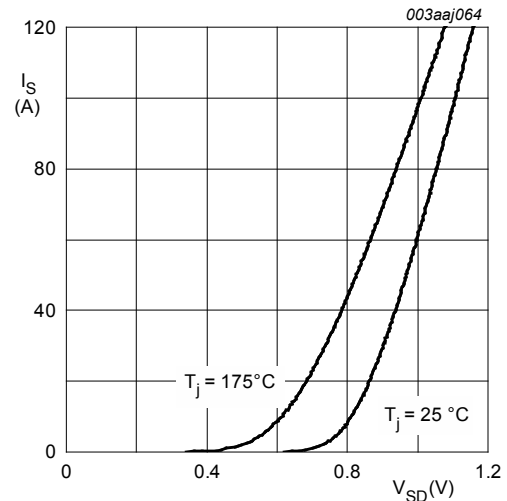


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0V$

### 11. Package outline

Plastic single-ended surface-mounted package (LFAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

Unit <sup>(1)</sup>	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3		
nom				0.25											1.27					0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note  
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				-11-03-25- 13-02-27

Fig. 18. Package outline LFAK56; Power-SO8 (SOT669)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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## 13. Contents

1	General description .....	1
2	Features and benefits .....	1
3	Applications .....	1
4	Quick reference data .....	1
5	Pinning information .....	2
6	Ordering information .....	2
7	Marking .....	2
8	Limiting values .....	2
9	Thermal characteristics .....	4
10	Characteristics .....	5
11	Package outline .....	10
12	Legal information .....	11
12.1	Data sheet status .....	11
12.2	Definitions .....	11
12.3	Disclaimers .....	11
12.4	Trademarks .....	12

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